OPERATION OF A SINGLE-PHASE GRID CONNECTED INVERTER WITH LARGE DC BUS VOLTAGE RIPPLE FOR DISTRIBUTED GENERATION

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ABSTRACT

Operation of a Single-Phase Grid Connected Inverter with Large DC Bus Voltage Ripple for Distributed Generation

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Distributed generation (DG) looks promising for meeting the increasing energy demand with reduced environmental impact. Traditionally, the electric power plants are located far from load centers. DG units based on Photovoltaic (PV), wind, fuel cell etc. can be installed at the distribution level close to the loads, thus reducing investments in the utility's infrastructure. Distributed energy resources, DG plus storage, are connected to the grid by means of power electronic converters. Normally, a single-phase voltage source inverter (VSI) is used as a power interface for low power (< 10 kVA) consumer owned DG units. Its main function is to transfer active power to the grid, but it can also provide reactive power compensation adding value to the DG unit. The reliability of single-phase VSI is relatively low due to the large electrolytic capacitors required at the dc bus for attenuating the 2^{nd} order voltage ripple. This Thesis discusses a control scheme suitable for the VSI operating with large dc bus ripple, when a small and high reliability thin film capacitor can be used. It is based on a dc bus voltage ripple estimator and a voltage control loop with higher bandwidth. Different types of current controllers were tested for the inner loop but did not affect much the system's performance. An experimental set-up was implemented to show that a variable power factor inverter with a small dc capacitor can perform better than a conventional inverter regarding the transient response and the low frequency harmonic distortion in the ac side current.

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Last but not least, the author is very grateful towards his parents whose constant support made it possible to finish the project.

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LIST OF ACRONYMS

A	Ampere
AC	Alternating Current
ADC	Analogue to Digital Converter
APF	Active Power Filter
CCM	Continuous Conduction Mode
dB	Decibel
DAC	Digital to Analogue Converter
DC	Direct Current
DG	Distributed Generation
D-Q	Direct Quadrature
DSP	Digital Signal Processor
ESR	Equivalent Series Resistance
GI	Generalized Integrator
HC	Harmonic Compensator
HCC	Hysteresis Current Controller
Hz	Hertz
IGBT	Insulated-Gate Bipolar Transistor
I/O	Input/Output
MPPT	Maximum Power Point Tracking
PCC	Point of Common Coupling
PF	Power Factor

PI	Proportional Integral
PLL	Phase Locked Loop
PM	Phase Margin
PR	Proportional Resonant
PV	Photovoltaic
PWM	Pulse Width Modulation
RMS	Root-Mean-Square value
RES	Renewable Energy Sources
SAS	Solar Array Simulator
SPWM	Sinusoidal Pulse Width Modulation
STATCOM	STATic synchronous COMpensator
THD	Total Harmonic Distortion
V	Volt
VA	Volt-Ampere
VARIAC	Variable Auto Transformer
VAR	Variable Reactive Power
VSI	Voltage Source Inverter
W	Watt

LIST OF PRINCIPAL SYMBOLS

C_{dc}	DC side capacitance
ΔV	Dead-time compensation voltage
E_c	Capacitor energy
FF	Feedforward gain
f_x	Cross-over frequency
f_{sw}	Switching Frequency
f	Frequency
$G_p(s)$	Transfer function of plant
$G_c(s)$	Transfer function of controller
$\hat{I}_{2f_{sw}}$	Peak value of dominant switching frequency voltage
i_{d2}^*	2nd order current supplied from dc link
I_r	RMS value of the active component of current
I_q	RMS value of the reactive component of current
I_{ref}	Referenence Current
I_{out}	Output Current
I_g	Grid current
$\hat{I}_g$	Peak value of grid fundamental current
$\hat{I}_r$	Peak value of the injected active component of current
K_p	Proportional gain

K_i	Integral Gain
L	Inductance
m_a	Modulation Index
PI_v	Output of voltage loop controller
P_{grid}	Average injected power to the grid
P_{grid}	Power at the grid
P	Active Power
p_{ac}	Instantaneous ac side power
P_c	Capacitor power
p_{dc}	Instantaneous dc side power
p_{inv}	Instantaneous inverter output power
ϕ	Phase angle of the dc bus voltage ripple
Q	Reactive Power
R	Resistance
s	Laplace variable
φ	Phase angle of inverter output voltage
t	Time
t_d	Dead-time
t_{off}	Switch turn-off delay time
t_{on}	Switch turn-on delay time
T	Period
T_s	Simulation sampling time

T_c	PWM carrier period
τ	Integral Constant of PI controller
θ	Phase difference between grid voltage and current
$\hat{v}_{ripple}$	Peak value of the 2nd order harmonic in dc link
$\hat{V}_{2f_{SW}}$	Peak value of dominant switching frequency voltage
$\hat{V}_{tri}$	Peak value of the triangular carrier signal for the SPWM inverter
V_{comp}	Compensating voltage for dc voltage controller
V_{dc}	DC Bus Voltage
V_{dc0}	Average dc link voltage
V_{dc_max}	Maximum value of the dc link ripple
V_{dc_min}	Minimum value of the dc link ripple
V_g	Grid voltage
V_{inv}	Inverter output voltage
$\hat{V}_g$	Peak value of grid voltage
V_{sat}	On state voltage drop across the switch
V_d	Diode forward voltage drop
V^*	Commanded or actual modulation signal
$\hat{V}_{inv}$	Peak value of inverter output voltage
ω	Angular frequency
ω	Resonant frequency of PR controller
ω_x	Angular cross-over frequency

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

The energy demand in the world is steadily increasing. Nowadays, fossil fuel is the main energy supplier of the worldwide economy, but it is a major cause of environmental problems (such as global warming, air pollution etc.). The necessity of producing more energy combined with the interest in clean technologies results in an increased development of power distribution systems using renewable energy sources (RES) such as wind energy, hydro, solar, biomass, wave energy, tidal power, ocean thermal energy and geothermal energy [1]. Solar irradiance is a major contributor to the global renewable energy supply. The photovoltaic (PV) cell converts sunlight to electrical current cleanly, without any form of mechanical or thermal interlink. A tremendous surge in PV technology, efficiency and cost reduction in recent years has resulted in a large scope for PV power in distributed generation (DG) system. The number of PV installations has had an exponential growth as shown in Fig. 1-1, mainly due to the governments and utility companies who support the idea of green energy. Due to the latest development in power and digital electronics, the market for small PV power generation system connected to the domestic grid is increasing rapidly. However there are still a number of issues to be worked out, such as the reliability of the power electronic interface where the large electrolytic dc capacitors are the weak link in terms of life span. Besides, the incorporation of features such as reactive power compensation,

voltage regulation and active power filtering would add value to the PV, further motivating their deployment. This thesis deals with some of these issues.

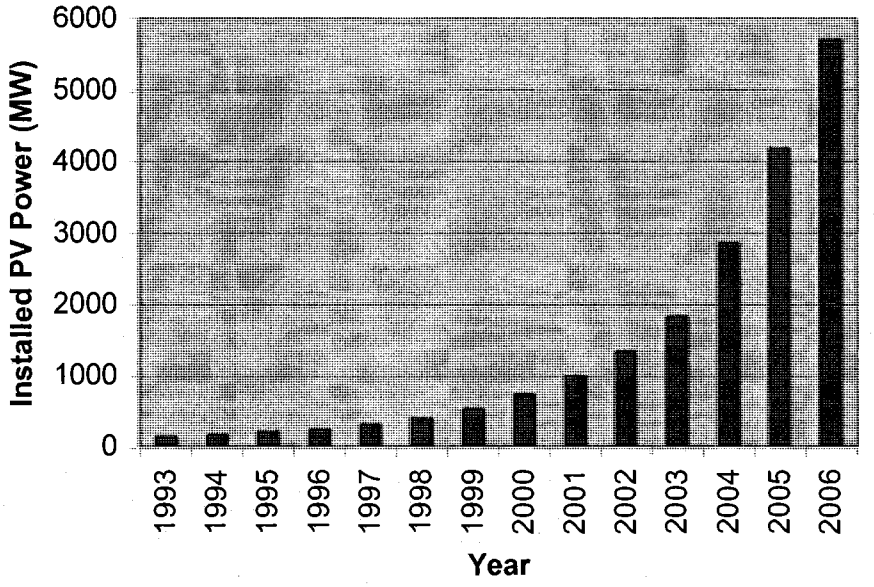
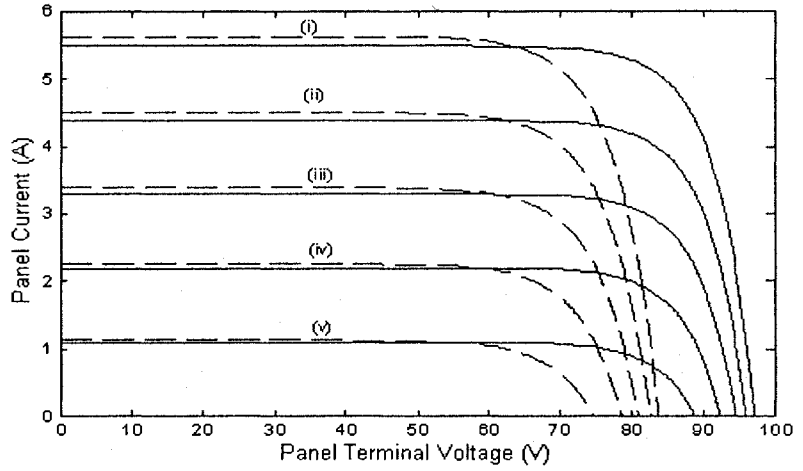


Fig. 1-1 Cumulative installed PV power in the reporting countries [2]

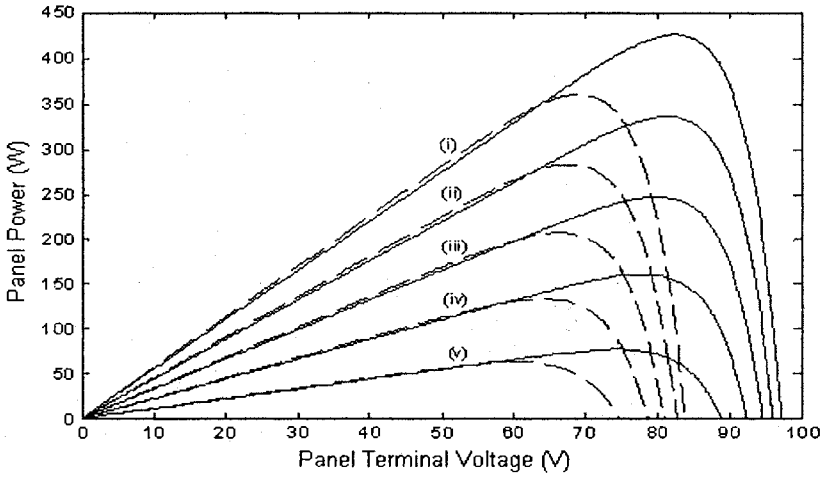
1.2 OVERVIEW OF PV POWER SYSTEMS

1.2.1 PHOTOVOLTAIC (PV) PANELS

PV modules convert solar irradiance in dc power. The amount of generated power varies with the solar irradiance, incidence angle and temperature. PV modules present a non-linear characteristic. The output voltage and consequently the output power varies with the output current as shown in Fig. 1-2. As the solar irradiance varies, the voltage and current that leads to maximum power vary. In order to draw as much power as possible from a PV module, maximum power point tracking (MPPT) algorithms are often included in a power electronic converter placed between the PV module and a load, a battery bank or the ac utility grid.



(a)



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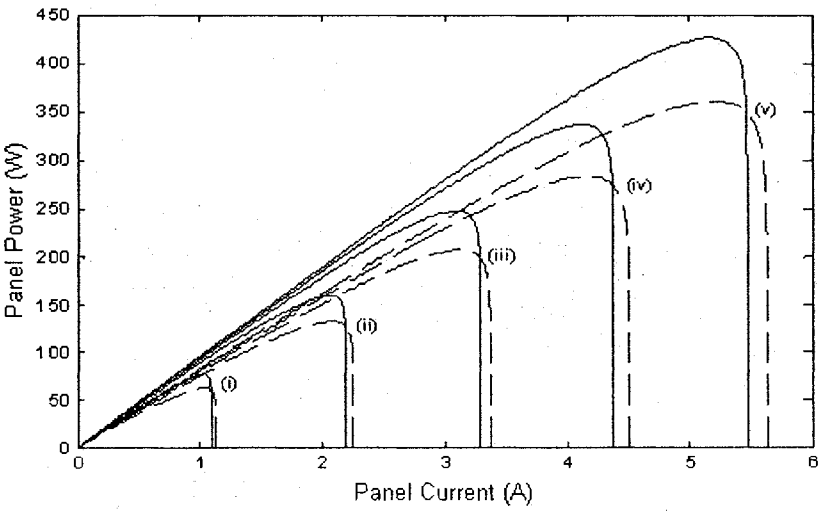


(c)

Fig. 1-2 Output characteristic curves of PV panels

1.2.2 COMMON CONFIGURATIONS OF GRID INTERFACES FOR PV SYSTEMS

This thesis is concerned with low power (< 10 kW) grid interfaces for PV or other sources that produce dc power. In such a system, one has to use a dc-ac converter or inverter to inject power into the ac grid. The grid interface should present the highest possible efficiency, the lowest cost and superior performance in terms of power quality. The electrical distribution system around the world is based on ac voltage, with a few exceptions. Voltage levels are usually around 120 V or 230 V at the residential distribution grid. The grid interface can be categorized into four broad groups: centralized technology, string technology, multi-string technology and ac module technology [3].

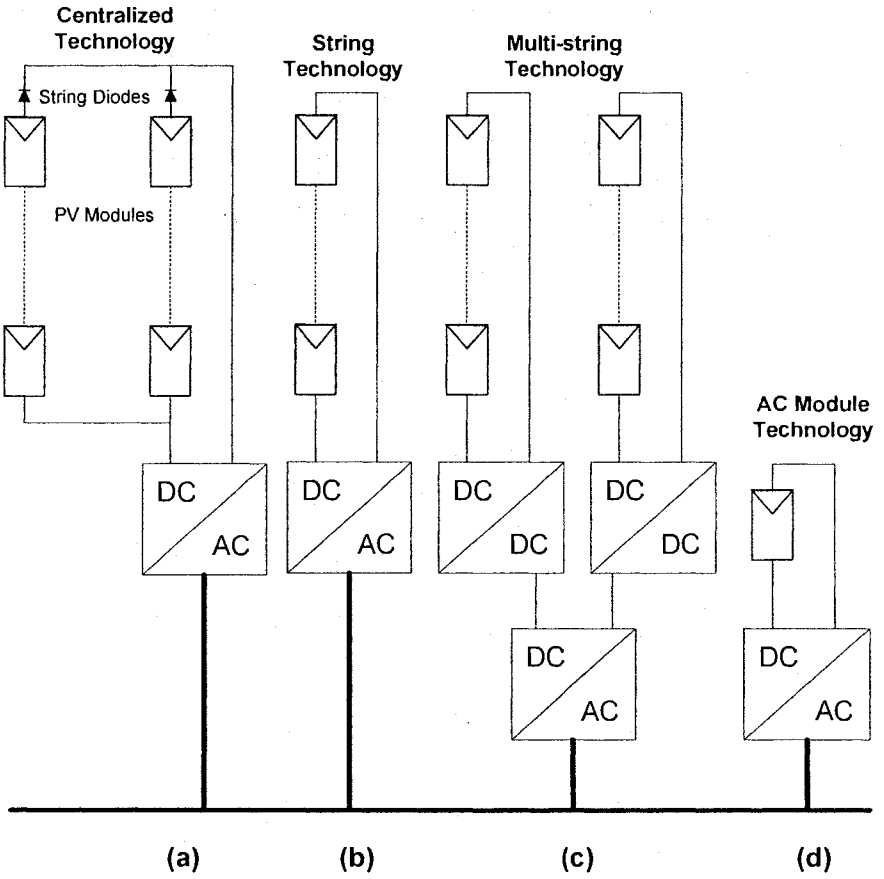


Fig. 1-3 PV inverters. (a) Centralized technology, (b) String technology, (c) Multi-string technology, (d) Ac-module technology.

In centralized technology, a large number of PV modules are interfaced to the grid through a single inverter as shown in Fig. 1-3(a). The PV modules are connected in series (known as string), each generating a sufficiently high voltage to avoid further amplification. These strings are then connected in parallel in order to reach high power levels. The string inverter, shown in Fig. 1-3(b), is a reduced version of the centralized inverter, where a single string of PV modules is connected to the inverter. The input voltage is usually high enough to avoid voltage amplification by means of a 60 Hz transformer. The multi-string inverter is the further development of the string inverter, where several strings are connected with their own dc-dc converter to a common inverter, as shown in Fig. 1-3(c). This is a typical example of an interface. The main advantage is that the strings can have different characteristics such as voltage level or orientation. The dc-dc converters are used to decouple the different strings allowing them to operate independently at their maximum power point. Besides, the dc-dc converter can also allow electrical isolation and voltage amplification if it incorporates a high frequency transformer. Finally, the ac cell inverter system is the case where one PV panel of a few hundred watts is connected to a single inverter, as shown in Fig. 1-3(d).

All approaches have advantages and disadvantages [4-5] regarding complexity, efficiency, flexibility, reliability, safety, modularity and cost. However, for residential PV installations, the most suitable configuration seems to be the string or the multi-string technologies. These enable minimization of losses associated with the string diodes compared to the centralized technology. Moreover, they can also increase the overall efficiency under special circumstances like partial shading.

1.2.3 ISSUES WITH SINGLE-PHASE VOLTAGE SOURCE INVERTERS (VSI)

One of the main issues of single-phase inverters is a second order component that appears at its dc side. This will be briefly described in the following paragraphs.

If the grid voltage v_g and fundamental current i_g is described by,

$$\begin{aligned} v_g &= \hat{V}_g \sin(\omega t) \\ i_g &= \hat{I}_g \sin(\omega t + \theta) \end{aligned} \tag{1-1}$$

The instantaneous power injected into the grid can be determined as,

$$\begin{aligned} p_{grid} &= v_g i_g \\ &= \hat{V}_g \sin(\omega t) \cdot \hat{I}_g \sin(\omega t + \theta) \\ &= \frac{\hat{V}_g \hat{I}_g}{2}\left[\cos\theta - \cos(2\omega t + \theta)\right] \\ &= P_{grid}\left[\cos\theta - \cos(2\omega t + \theta)\right] \end{aligned} \tag{1-2}$$

Where $\hat{V}_g$ is the peak value of grid voltage, $\hat{I}_g$ is the peak value of grid fundamental current, θ is the phase difference between grid voltage and current, P_{grid} is the average injected power, ω is the angular frequency and t is the time. Therefore, there are two components of the instantaneous power which must be supplied from the PV inverter. The average value or the first part of the instantaneous power will be supplied from the PV array. The oscillatory power component tends to create a large ripple in the dc bus which can be minimized with a large reactive element such as an inductor or a capacitor. Usually PV inverters are of the voltage source type, presenting an electrolytic capacitor in the dc bus. This component is the main limiting factor of the lifetime of the system [6]. Thus, replacing electrolytic capacitors with other technologies such as thin film, can improve the reliability of PV inverters. The problem is that these capacitors present low

capacitance and the inverter would have to be designed to operate with large dc bus voltage ripple.

The output voltage of the inverter consists of pulses with a fundamental component and harmonics. A low pass filter is connected between the grid and the inverter to attenuate the high frequency switching harmonics that would appear in the ac side current. Usually, the line filter consists of an inductor but other combinations of capacitors and inductors such as LC or LCL-filters can be used as shown in Fig. 1-4.

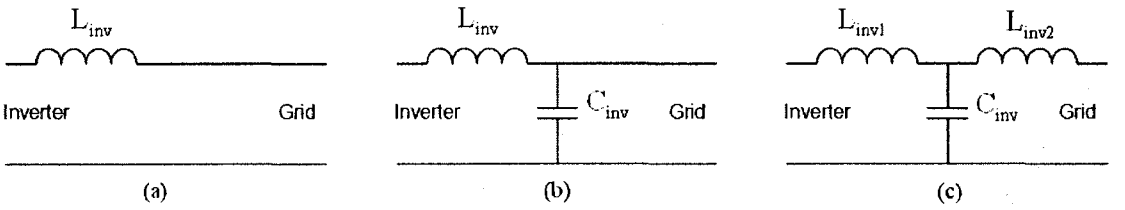


Fig. 1-4 Three different types of grid-connected filters. (a) L-filter, (b) LC-filter, (c) LCL-filter

The L filter has excellent high frequency switching harmonics rejection capability. It is a suitable choice for low power applications. For applications above several kilowatts, it becomes quite expensive to realize higher value filter reactors. The LC-filter also shows same good performance for high frequency switching harmonics as the L-filter if the grid impedance (not shown in figure) is high compared to the capacitor reactance [7]. On the other hand, the filter capacitor may be exposed to line voltage harmonics, which may result in large current. The LCL filter shares the good properties with the L and LC filters. However, the capacitor is no more exposed to line voltage distortion. Besides, it allows using quite small value of inductors and capacitors, for high power application (hundreds of kW) [8].

The current injected into the grid must comply with the regulations, such as, the IEEE std. 1547 [9], which state the maximum allowable current harmonic injection into the utility/grid. It permits a maximum of 5% for the current total harmonic distortion (THD) factor with individual limits of 4% for each odd harmonic from 3^{rd} to 9^{th} and 2% for each 11^{th} to 17^{th} harmonic.

Grid interface inverters should behave as sinusoidal current sources with the same frequency of the grid. Therefore, one key part of this system is the current control circuit. Different types of current controllers have been reported for VSI. The most common ones are the hysteresis current controllers (HCC) and the sinusoidal pulse width modulator (SPWM) with a PID type controller [10-11]. The first is well known for excellent transient response, inherent peak current limiting capability and their stability and robustness under varying load conditions, but the problem is that it gives a variable switching frequency what complicates the filter design. The second one yields a fixed switching frequency and superior harmonic characteristics, but it cannot achieve completely satisfactory quality of harmonic compensation in active power filter applications.

When the reference current is a dc signal, as in the dc motor drive, zero steady state error can be achieved through a conventional proportional integral (PI) controller. When the reference current is a sinusoidal signal, as in the grid connected PV system or off-grid system, however, straight forward use of the conventional PI controller would lead to steady state error. It cannot provide a very high gain at the concerned frequency, so it results in steady state error and poor disturbance rejection capability. The steady-state error of the PI type controller of current-controlled PV inverters can be significantly

reduced with a grid voltage feedforward scheme. An alternative solution to overcome the drawbacks of PI is presented in [12], where a second order generalized integrator (GI) is used. The GI is a double integrator that achieves an "infinite" gain at a certain frequency (resonance frequency), and almost no attenuation exists outside this frequency. Therefore, it can act as a notch filter for selective harmonic compensation. Recently a new type of stationary-frame controller known as proportional resonant (PR) controller has been reported in [13], where the classical PI dc-compensator is transformed into an equivalent ac-compensator having the same frequency response characteristics in the bandwidth of concern. The use of these types of linear current controllers for current control of VSI is advantageous because it uses a fixed switching frequency and provides superior harmonic characteristics. It is considered nowadays the most suitable for PV inverters.

The basic function of a PV inverter is to inject the real power from the PV system into the ac grid. However, it can also be used as power conditioner for reactive power and harmonic compensation for the local load connected to the point of common coupling (PCC). This can add value to the PV system making it more attractive for potential users.

1.3 OBJECTIVES AND CHALLENGES

This thesis deals with small consumer owned single-phase grid-connected voltage source inverters (VSI) without energy storage element, such as a battery, for distributed power generation (DG). A two stage converter system as shown in Fig. 1-5 is considered. A dc-dc converter with MPPT algorithm maximizes the power generated from the PV array. It sources maximum dc power to the dc link of the inverter. A single-phase full

bridge inverter transfers the power from the dc link to the ac grid. The dc-ac inverter can also compensate for reactive power of the utility system. A capacitor is placed in the dc link to buffer the instantaneous power difference between the ac side power and the power supplied from the dc-dc converter. At the absence of the real power, such as in the night time, the system can still work as a power conditioner by supplying or absorbing reactive power to the grid.

The main focus of the thesis is on the control of the single phase full bridge inverter so as to allow the use of small, non-electrolytic capacitors in the dc bus for increased reliability while complying with the power quality standards using sinusoidal pulse width modulation (SPWM). The inverter control system should control the ac grid current $i_g(t)$ to supply the available real power and commanded reactive power to the utility $v_g(t)$, while at the same time, dc link voltage $v_{dc}(t)$ should be regulated and kept equal to its reference value.

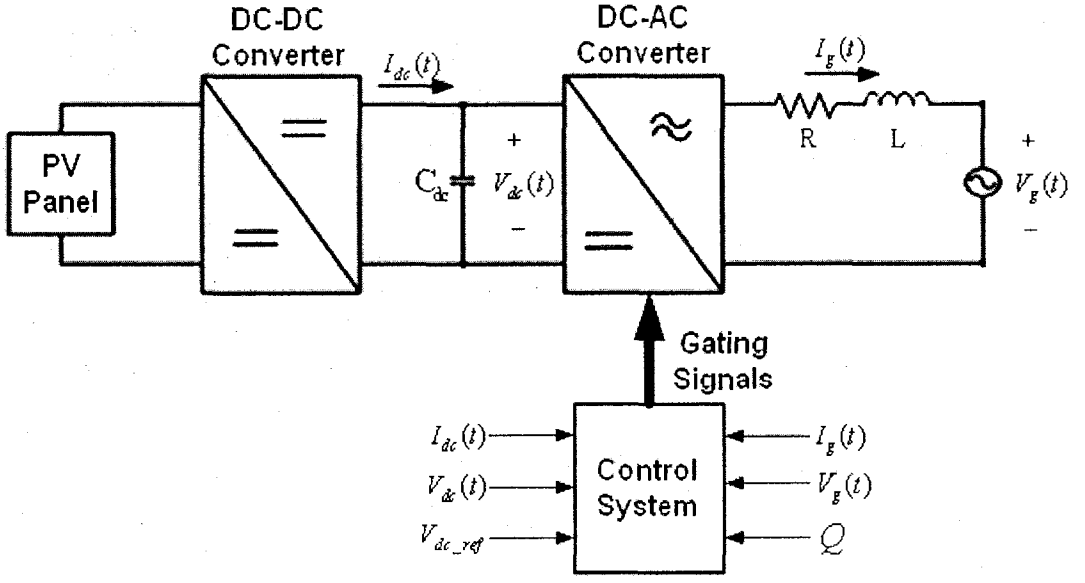


Fig. 1-5 Detailed diagram of the PV inverter system

The inverter is connected to the grid through an L filter. The inverter is switched using unipolar pulse-width modulation (PWM) scheme, for doubling the frequency of the switching harmonics, where a sinusoidal modulating signal is compared with a triangular signal to generate the gating signal for the switches.

The specific issues that will be covered in this thesis are:

1. Systematic design procedure of the passive components of the VSI system.
2. Derivation of the system's transfer function, design of controller for the two loops (dc bus voltage control and ac side current control) and analysis of the effect of the controller parameters on the response of the system.
3. The investigation of a voltage ripple estimator for operation with a large cross-over frequency and small capacitor.

1.4 CONTRIBUTION OF THE THESIS

The major contributions of this thesis are:

1. Design of a voltage ripple estimator to estimate the dc bus voltage ripple when the inverter operates with different values of power factor. The estimated ripple is cancelled from the voltage feedback signal, thus allowing operation with a small dc link capacitor. It also ensures low ac grid current distortion in steady state and fast response speed in the transient state.

2. A step by step design procedure for the passive components (filter) of the inverter is presented. Also modeling of the control loops and design of the controllers for regulation of dc bus voltage and ac side current is provided.
3. Implementation of a 100 VA (volt ampere) VSI system with the proposed estimator and calculated controllers. Extensive testing with different combinations of real power and reactive power supplied to the grid is carried out to verify the theoretical analysis and computer simulations. Simulation and experimental work is carried out to compare the proposed system with a standard scheme using a large dc link capacitor, in terms of steady state and transient response.

1.5 THESIS OUTLINE

The contents of this thesis are organized in 5 Chapters.

The first Chapter provides an overview of the PV power system. Specific issues, such as, PV system interconnection to the grid, ac side filter, harmonic regulation for distributed power generation, different types of current controllers, are addressed.

In the second Chapter, a systematic design procedure for power circuit components of the inverter is presented. Modeling of the control loops (dc voltage and ac current) is presented and then the controllers are designed to meet the required specification of the system. The step by step design procedure for a proportional integral (PI) controller and proportional resonant (PR) controller is presented. Finally the concept of the voltage ripple estimator for operation with a large cross-over frequency and small capacitor is discussed.

The third Chapter provides the simulation results. The proposed system is compared with a standard system with a large capacitor. Steady state and transient responses are presented. Besides, the effect of dead time of the driver circuit of the switches and dc bus voltage ripple are analyzed and compensation techniques are implemented and tested.

The fourth Chapter presents experimental results based on a 100 W prototype. Extensive laboratory tests are performed to see the effect of dc bus voltage and ac side current regulation of the inverter system with variations in real and reactive power.

The fifth Chapter summarizes the work carried out in this Thesis and the final conclusions. Suggestions for future work on this topic are presented.

CHAPTER 2

MODELING AND CONTROL OF THE GRID INTERFACE

2.1 INTRODUCTION

Low-power (< 10 kW) distributed energy resources (DER) are usually connected to the ac grid through a single-phase voltage source inverter (VSI) at low voltage (110-220V). A major drawback of single-phase VSIs is the double line-frequency voltage ripple on the dc bus. A large electrolytic capacitor, which is a limiting factor for system reliability, is usually employed at the dc terminal to attenuate this low order component [14]. DERs based on photovoltaic (PV) and fuel cells usually employ a two-stage power converter as shown in Fig. 2-1. This reduces the impact of the dc bus voltage ripple on the power source. The use of small non-electrolytic capacitors require an effective means for preventing the large low frequency ripple from propagating through the inverter via the dc bus voltage regulation loop and envelope of the switched inverter voltage that tend to distort the line current. Besides, it is also important to increase the speed of response of the dc bus voltage control loop to avoid large voltage excursions due to active power variations.

A dc-dc converter is used to implement maximum power point tracking (MPPT) on the PV array. In this Thesis, it is assumed that the PV array is decoupled from the dc link by means of the dc-dc MPPT converter and that the dc bus voltage ripple does not interfere with the PV power generation. In principle, the dc-dc converter could be

considered as a dc current source connected to the dc link of the inverter. This assumption is verified by simulation in Appendix-1.

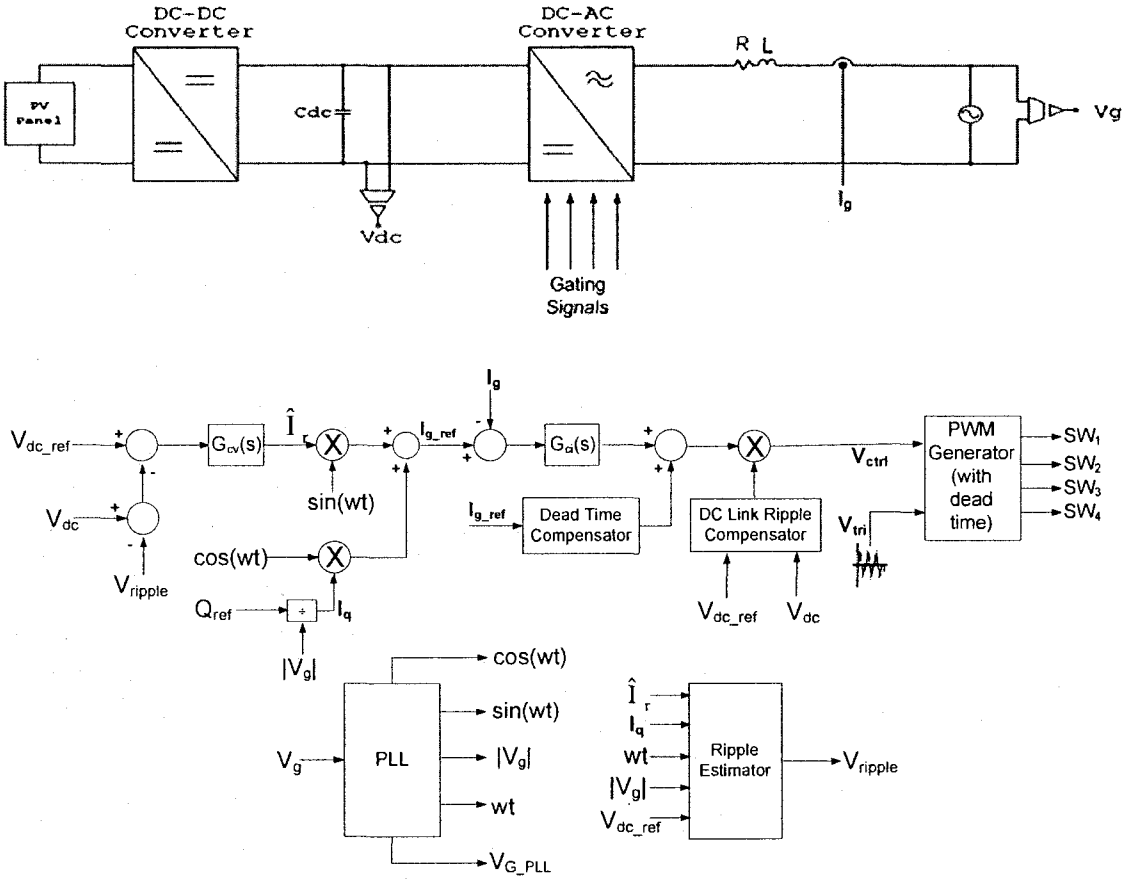


Fig. 2-1 Two-stage single-phase grid interface for DERs

A number of solutions have been proposed in the literature for dealing with the double line-frequency voltage ripple in the dc bus. It was shown in [15] that a dc bus voltage can operate with large voltage ripple (peak to peak 25%) without causing distortion in the ac grid current when the voltage control loop bandwidth is designed to be only 10 Hz. The double line-frequency dc bus voltage harmonic is highly attenuated but the voltage loop has a slow speed of response making the dc bus voltage more susceptible to large variations due to sudden active power variations in the system. This

issue was not discussed in [15]. Some schemes as in [16] employ an extra converter such as a high frequency current-fed type active power filter (APF) to circulate the harmonics. In this way, there are no second-order harmonics circulating through the capacitor which can then be made small without resulting in large dc bus voltage ripple. The shortcoming of this solution is the additional cost of the APF. Regarding the problem of propagation of the double-line-frequency component of the dc bus voltage loop, this can be reduced by using a tuned notch filter as proposed in [17]. The main limitation of this technique is that the notch filter is tuned at a given frequency while the grid frequency is allowed to vary in a certain range: $59.4\,\text{Hz} \le f_{grid} \le 60.5\,\text{Hz}$, resulting in reduced effectiveness.

The approach presented in this Thesis is based on the principle of voltage ripple cancellation [18]. The voltage ripple of the dc bus voltage is estimated and subtracted from the actual dc bus voltage as shown in Fig. 2-1. In this way, the feedback signal used in the regulation of the average value of the dc voltage should be ripple free in the steady state and no distortion would appear at the reference current for the sinusoidal pulse-width modulation (SPWM) control of the single-phase VSI.

2.2 DESIGN OF THE POWER CIRCUIT

This section discusses the design of a 100 W, 120 V, 60 Hz single-phase grid interface for DERs for operation with large dc bus voltage ripple. A 21 V to 120 V transformer is used between the inverter and grid. The rated value of the dc bus voltage is selected as 48 V. In this case, even with a large dc voltage ripple, say 6 V peak, the minimum instantaneous dc bus voltage is larger than the peak voltage at the low voltage

side of the transformer, thus avoiding current distortion in the ac side. A full-bridge inverter operating with unipolar-SPWM and a triangular carrier (5 kHz and 10 V peak) is considered. The rated output current of the inverter is 4.7 A (rms) at the low voltage side of the transformer. The input current to the dc link for rated power is 2.083 A. The following subsections, present details of the design of the passive power components.

2.2.1 AC SIDE INDUCTOR

The ac side inductor is selected assuming ideal conditions: The dc bus voltage and the ac grid voltage are ripple free and the modulating signal of the PWM is purely sinusoidal. The inductor is designed so as to limit the magnitude of the switching current harmonics (dominant voltage harmonics in case of SPWM inverters) to a certain percentage of the rated fundamental component. For a good dynamic response, the size of the inductor must be as small as possible. Nevertheless, if the inductor is too small, it cannot suppress the switching ripple current. For high switching frequency and unity power factor (PF) operation, the output voltage of the inverter is approximately equal to the utility voltage. The flow of active power is due to a phase angle between the fundamental component of the inverter voltage and the voltage at the low voltage side of the transformer. In such a case, the modulation index is 0.625 for a dc bus voltage of 48 V. By simulation, one obtains that the magnitude of the dominant voltage harmonic, at twice the switching frequency, is 17.58 V (peak). Considering a 3% allowable dominant switching harmonic current component, the inductor value can be calculated.

$$X_{2f_{sw}} = 2\pi(2f_{sw})L = \frac{\hat{V}_{2f_{sw}}}{\hat{I}_{2f_{sw}}} \tag{2-1}$$

$$L = \frac{\hat{V}_{2f_{sw}}}{\hat{I}_{2f_{sw}}} \cdot \frac{1}{2\pi(2f_{sw})} = \frac{17.58V}{(0.03 \cdot 4.7A) \cdot \sqrt{2}} \cdot \frac{1}{2\pi(2 \cdot 5k)}$$
$$= 1.4\,mH$$

An inductor (L) of 1.5 mH was selected and an internal resistance (R) of 0.15 Ω was assumed.

2.2.2 DC SIDE CAPACITOR

The dc link capacitor is calculated considering the maximum allowable second order harmonic in the dc bus when the converter operates with rated apparent power.

The power supplied from the dc link to the inverter switches can be given as,

$$p_{dc} = V_{dc} i_d^* \tag{2-2}$$

Where, V_{dc} and i_d^* are the dc link average voltage and current supplied from the dc link respectively. Considering the inverter to be a lossless system, it will be equal to the ac side power as given by equation (1-2). Therefore,

$$\begin{aligned} V_{dc} i_d^* &= \frac{\hat{V}_g \hat{I}_g}{2}\left[\cos\theta - \cos(2\omega t + \theta)\right] \\ i_d^* &= \frac{\hat{V}_g \hat{I}_g}{2V_{dc}}\left[\cos\theta - \cos(2\omega t + \theta)\right] = I_d + i_{d2}^* \end{aligned} \tag{2-3}$$

Therefore, the current supplied from the dc link has a 2nd order harmonic i_{d2}^* and its magnitude is given by $\hat{V}_g \hat{I}_g / 2V_{dc}$ for all PFs. Therefore, at rated apparent power operation, the dc link capacitor can be calculated considering any one operating condition.

For unity power factor operation and neglecting the energy stored in the ac inductor, the instantaneous power flowing through the inverter is given by

$$
\begin{aligned}
p_{ac} &= v_g(t) i_r(t) = \left(\hat{V}_g \sin \omega t\right)\left(\hat{I}_r \sin \omega t\right) \\
&= \hat{V}_g \hat{I}_r \sin^2 \omega t = \frac{\hat{V}_g \hat{I}_r}{2} 2\sin^2 \omega t \\
&= P\left(1 - \cos(2\omega t)\right)
\end{aligned}
\tag{2-4}
$$

Where, $\hat{I}_r$ is the peak value of the injected active component of current, $\hat{V}_g$ is the peak value of the grid voltage and P is the average value of the active power injected into the grid.

The difference between the instantaneous and the average active power in the ac side of the inverter produces a voltage ripple at twice the line frequency on the dc bus. So the dc capacitor needs to buffer the power difference between the power supplied by the dc-dc converter and that absorbed by the ac grid. The maximum charging or discharging period of the dc capacitor is T/4 (T=1/60 s). The capacitance of the dc bus capacitor that limits this ripple to a desired value can be calculated considering the power balance concept [19]:

$$
\frac{1}{2} C_{dc} \left({V_{dc\_\max}}^2 - {V_{dc\_\min}}^2 \right) = \int_{-T/8}^{T/8} \left(p_{ac} - P \right) dt \tag{2-5}
$$

Where $V_{dc\_\max}$ and $V_{dc\_\min}$ are the maximum and minimum value of the dc link ripple and C_{dc} is the capacitance required for active component of the current. So

$$
\begin{aligned}
C_{dc} &= \left| \frac{2\int_{-T/8}^{T/8} \left(p_{ac} - P \right) dt}{{V_{dc\_\max}}^2 - {V_{dc\_\min}}^2} \right| \\
&= \left| \frac{2\int_{-T/8}^{T/8} -P\cos(2\omega t) dt}{{V_{dc\_\max}}^2 - {V_{dc\_\min}}^2} \right|
\end{aligned}
\tag{2-6}
$$

The 2nd order voltage ripple is symmetrical around the nominal dc link voltage. Hence

$$C_{dc} = \frac{2P/\omega}{4V_{dc}\hat{v}_{ripple}} = \frac{P}{2\omega V_{dc}\hat{v}_{ripple}} \tag{2-7}$$

Where, V_{dc} is the rated dc link voltage and $\hat{v}_{ripple}$ is the peak value of the 2nd order harmonic in dc link.

The dc link capacitor is calculated assuming a maximum peak value of 15% for the second order harmonic in the dc bus when the converter operates with rated power. So the minimum dc capacitor size is

$$C_{dc} = \frac{100}{2 \cdot 2\pi \cdot 60 \cdot 48 \cdot (0.15 \cdot 48)} = 384\mu F$$

So a $384\,\mu F$ capacitor will ensure ±15% ripple of nominal dc link voltage for rated input power to the dc bus. In reality, the actual dc capacitor is $500\,\mu F$, which is the only available volume at hand that is most close to the value obtained in the design. Hence in that case, the system operates with a dc link ripple of 11.5%. The ESR of the dc bus capacitor is less than 0.1 Ω. This value is less than 2% of the capacitive reactance at 120 Hz.

2.3 MODELING AND ANALYSIS OF THE CONTROL SYSTEM

Grid-connected single phase inverters are usually required to control the magnitude of the dc bus voltage and inject a sinusoidal current into the grid. The control system is usually of the cascaded type with PI controllers employed in both outer voltage and inner current loops, as shown in Fig. 2-1. Unipolar SPWM, which doubles the

effective switching frequency and its associated switching harmonics of the converter, is commonly used for gating signal generation of the power switches. Typically, the inverter operates with unity power factor, but operation with variable power factor for ac bus voltage regulation and load power factor compensation is also possible. The outer loop is intended to regulate the dc bus voltage. Ideally, the output of the voltage controller is a dc value which is multiplied by a sinusoidal template obtained with a phase-locked loop (PLL). It represents the active component of the reference current which indicates the amount of power that is available to the dc link from the PV system or the amount of power supplied to the inverter system to overcome the losses of the system during reactive power compensation mode. The reactive component of the current is determined from the reference reactive power. The total reference current for the current control loop is the sum of active and reactive components of the current. Thus the reference signal for the current loop is a sinusoid with variable magnitude and phase, in the steady-state. The current loop presents a large bandwidth, for fast transient response, and should ideally result in zero magnitude and phase error for the sinusoidal output inverter current.

2.3.1 INNER CURRENT LOOP

The most common types of control schemes used for the inner current loop are: PI controller with feedforward [12] and the proportional resonant (PR) [20]. The main advantage of the latter is that it does not need to feedback the grid voltage, only the injected current which is required for regulating the output current anyway. In the steady-state, they provide the same performance for an ideal (harmonic free) ac grid. When the grid presents low order voltage harmonics, a harmonic compensator (HC) can be

included in parallel with the PR controller for minimizing the current distortion [20]. The speed of response of the two schemes is very similar provided that they are designed with the same specifications, such as the bandwidth and phase margin (PM).

The converter operates at high frequency so that the PWM block and power inverter can be represented by a simple gain with a processing delay, usually equal to half of the carrier period. It represents the relationship between the control voltage (V_{ctrl}) and the fundamental component of the output voltage of the inverter (V_{inv1}).

$$G_{pwm}(s) = \frac{V_{inv1}(s)}{V_{ctrl}(s)} = \frac{V_{dc}}{\hat{V}_{tri}} \cdot \frac{1}{1+sT_s} \tag{2-8}$$

Where $\hat{V}_{tri}$ is the peak value of the triangular carrier signal for the SPWM inverter.

The output current of the inverter is given as,

$$Ri_g(t) + L\frac{di_g(t)}{dt} = v_{inv}(t) - v_g(t) \tag{2-9}$$

The utility voltage $v_g(t)$ can be considered as a disturbance for the current loop, therefore,

$$I_g(s)(sL+R) = V_{inv1}(s)$$

$$\frac{I_g(s)}{V_{inv1}(s)} = \frac{1}{sL+R} \tag{2-10}$$

So the uncompensated current loop is give by,

$$G_p(s) = \frac{I_g(s)}{v_{ctrl}(s)} = \frac{I_g(s)}{V_{inv1}(s)} \frac{V_{inv1}(s)}{v_{ctrl}(s)} = \frac{1}{sL+R} \cdot \frac{V_{dc}}{\hat{V}_{tri}} \cdot \frac{1}{1+sT_s} \tag{2-11}$$

Fig. 2-2 illustrates the block diagram of the ac current control loop. The bode diagram of the system is provided in Fig. 2-3. The cross-over frequency of the current

loop controller is chosen as 600 Hz. At the desired cross-over frequency, the system presents 0.834 dB gain and -98.146° phase.

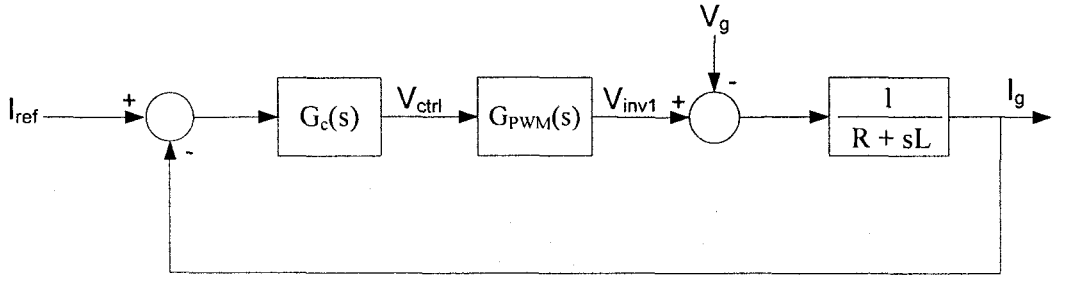


Fig. 2-2 Block diagram of the current control loop

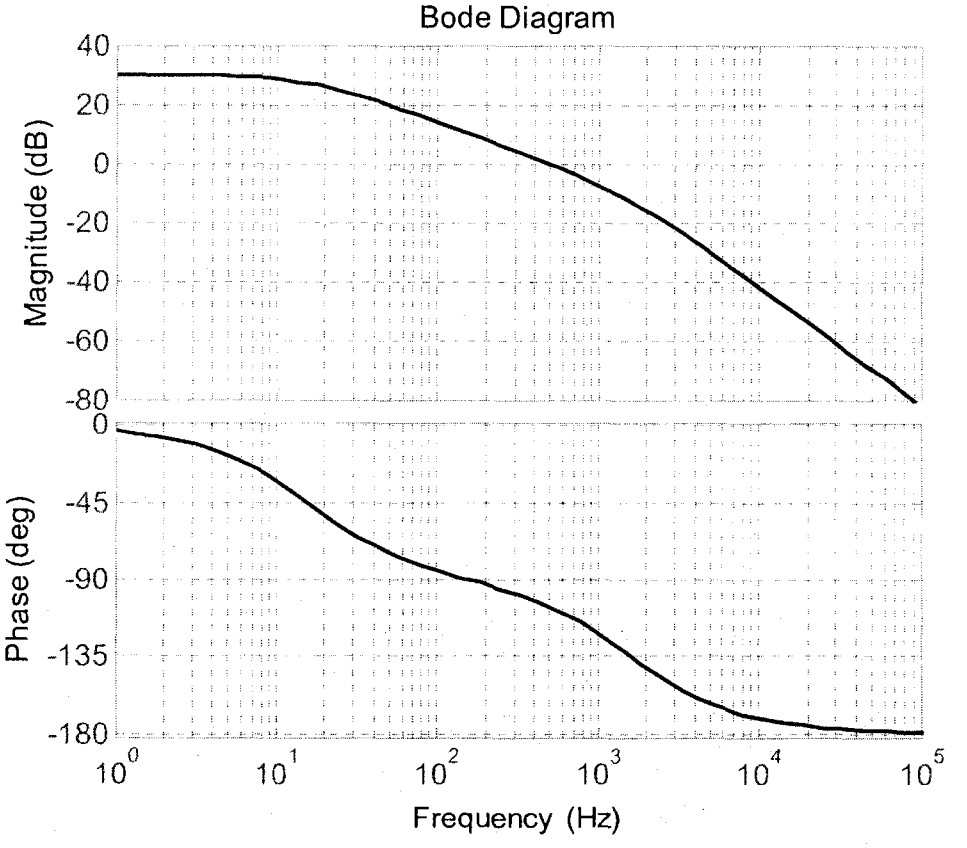


Fig. 2-3 Bode plot of the uncompensated current loop

2.3.1.1 PI WITH FEEDFORWARD OF GRID VOLTAGE

Since utility voltage acts as a disturbance for the current loop, therefore neglecting the effect of this will create a steady state phase error when the current controller is implemented with a classical PI controller. So to overcome this problem, a grid voltage feedforward should be adopted as shown in Fig. 2-4. The feedforward gain for the grid voltage is given by,

$$FF = \frac{\hat{V}_{tri}}{V_{dc}} \tag{2-12}$$

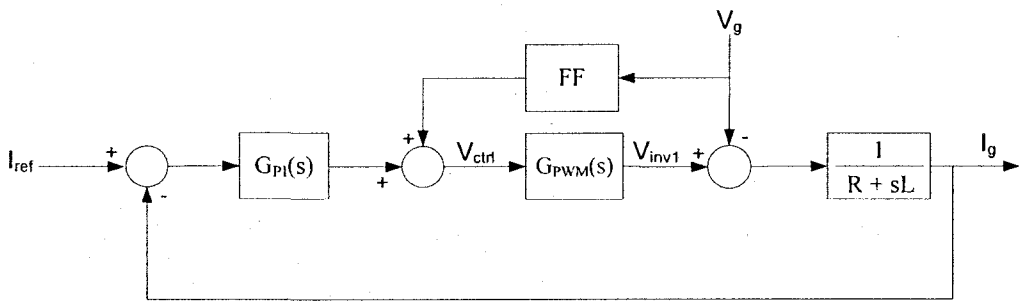


Fig. 2-4 Block diagram of the inner current loop with PI controller

The PI current controller is given by,

$$G_{PI}(s) = \frac{K(1+s\tau)}{s\tau} \tag{2-13}$$

The phase margin (PM) of the loop transfer function (including PI controller) should be 55°, at the cross-over frequency (f_x) of 600 Hz ($\omega_x = 2\pi f_x = 3777 rad/s$). Therefore,

$$\angle G_{PI} + \angle G_P = -180^0 + PM \tag{2-14}$$

$$\angle G_{PI} = -26.854^0$$

Since $$\tan\left(\angle G_{PI} + 90^0\right) = \tau\omega_x \tag{2-15}$$

$$\tau = 5.229\times10^{-4}$$

Let K=1, the magnitude of the loop transfer function (including the PI controller) at the cross-over point is -0.587 dB. The controller should provide sufficient gain at desired cross-over frequency to make the total gain of the current control loop to be 0 dB. So the gain of the controller is,

$$K = 10^{\frac{gain(dB)}{20}} = 1.079 \tag{2-16}$$

The bode diagram of the compensated current loop and controller is presented in Fig. 2-5.

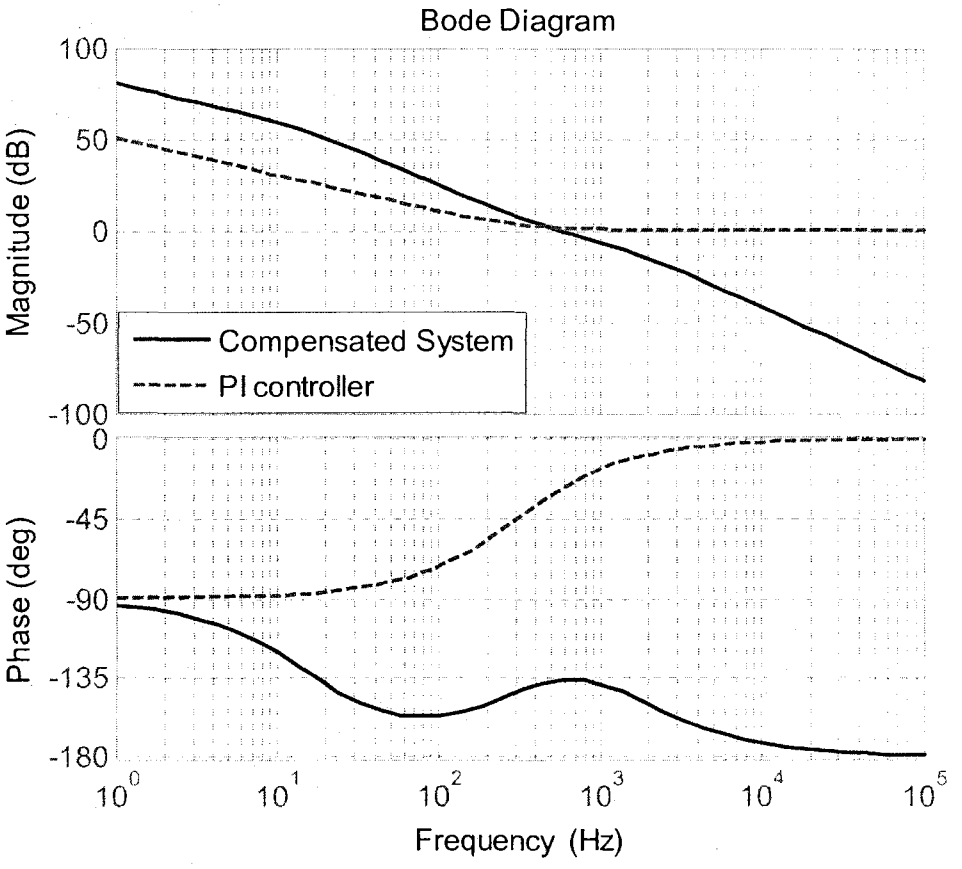


Fig. 2-5 Bode diagram of the compensated current loop and PI current controller

2.3.1.2 PROPORTIONAL RESONANT (PR) CONTROLLER

Stationary frame controllers are less satisfactory for ac current regulation since they suffer from significant steady state amplitude and phase errors because of gain limitations at the reference fundamental frequency. In contrast, synchronous frame controllers act on dc signals and are therefore usually considered to be superior to stationary frame controllers since operation with zero steady state error is theoretically possible. In three phase system D-Q transformation is used for this purpose. Recently the PR controller has been reported in some literature which gives similar performance as the PI used in D-Q co-ordinate (synchronous reference frame). PR controller attracted an increased interest due to its superior behavior over the traditional PI controllers, when regulating sinusoidal signals. Removal of the steady state error in single phase system, no need for voltage feedforward and easy tuning stands as its main advantages. The transfer function for a PR controller is given as

$$G_C(s) = K_p + K_i \frac{2s}{s^2 + \omega^2} \tag{2-17}$$

Where K_p is the proportional gain, K_i is the resonant part gain and ω is the resonant frequency of the controller.

This kind of controller can achieve very high gain in a narrow frequency band around the resonance frequency. Fig. 2-6 shows the bode plot of resonant controller tuned for resonance frequency of 60 Hz.

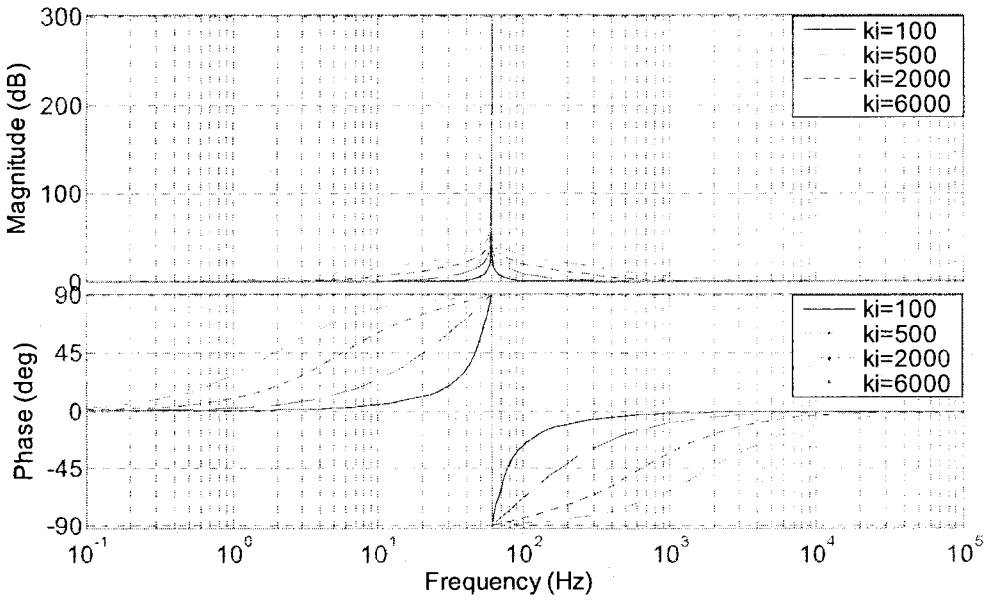


Fig. 2-6 Bode plot of resonant controller tuned for 60 Hz with different integral gains

The desired sinusoidal signal's frequency is chosen as the resonance frequency. The size of the integral constant determines the gain and the bandwidth centered at the concerned resonant frequency. For applications potentially with certain fundamental frequency variation, the integral constant may be oversized accordingly. Infinite gain as well as phase leads or lags of up to 90 degrees can be created at the concerned frequency and the vicinities. Size of the proportional constant decides: 1) stability of the simple proportional system; 2) the sinusoid frequency that can be regulated without violating the stability limits; 3) cross-over frequency and dynamic response; and 4) reduction of the harmonics at other frequencies [21].

Fig. 2-7 shows the block diagram of the current control loop with PR controller. At first, a trial value for the proportional part is determined considering the resonant part to be zero (the controller acting as a proportional controller only). Since the

uncompensated current loop has -1.578 dB gain at the desired cross-over frequency, so an initial value of the proportional part is given as,

$$K_p = 10^{-\frac{gain(db)}{20}} = 1.199$$

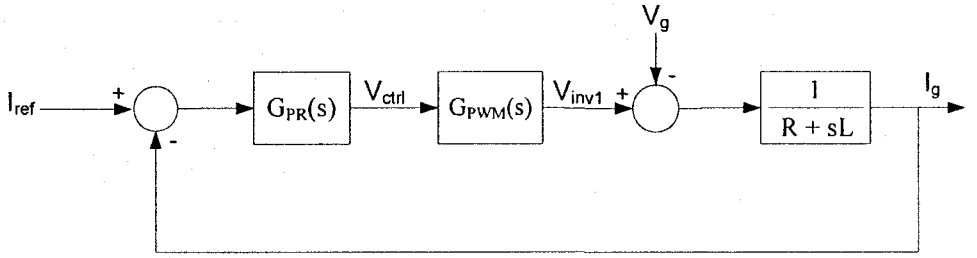


Fig. 2-7 Block diagram of the current control loop with PR controller

The resonant frequency of the controller should be 60 Hz ($\omega = 377 rad/s$). Now by trial and error the values of K_p and K_i for the desired PM of 55° at the cross-over frequency of 600 Hz, can be determined.

$$K_p = 1.073 \ \& \ K_i = 1000$$

The bode diagram of the controller and compensated system is provided in Fig. 2-8. The given PR controller is difficult to implement, because it means a resonant circuit with infinite quality factor. So instead of that one, a more practical one is used for real time application,

$$G_C(s) = K_p + K_i \frac{2\omega_{cut} s}{s^2 + 2\omega_{cut} s + \omega^2} \tag{2-18}$$

In practice, ω_{cut} values of 5~15 rad/s have been found to provide a good compromise [21]. ω_{cut} was chosen as 10. Following the same procedure the parameters

for the controller were determined ($K_p = 1.07$ & $K_i = 100$). The bode diagram of the controller and compensated system is provided in Fig. 2-8.

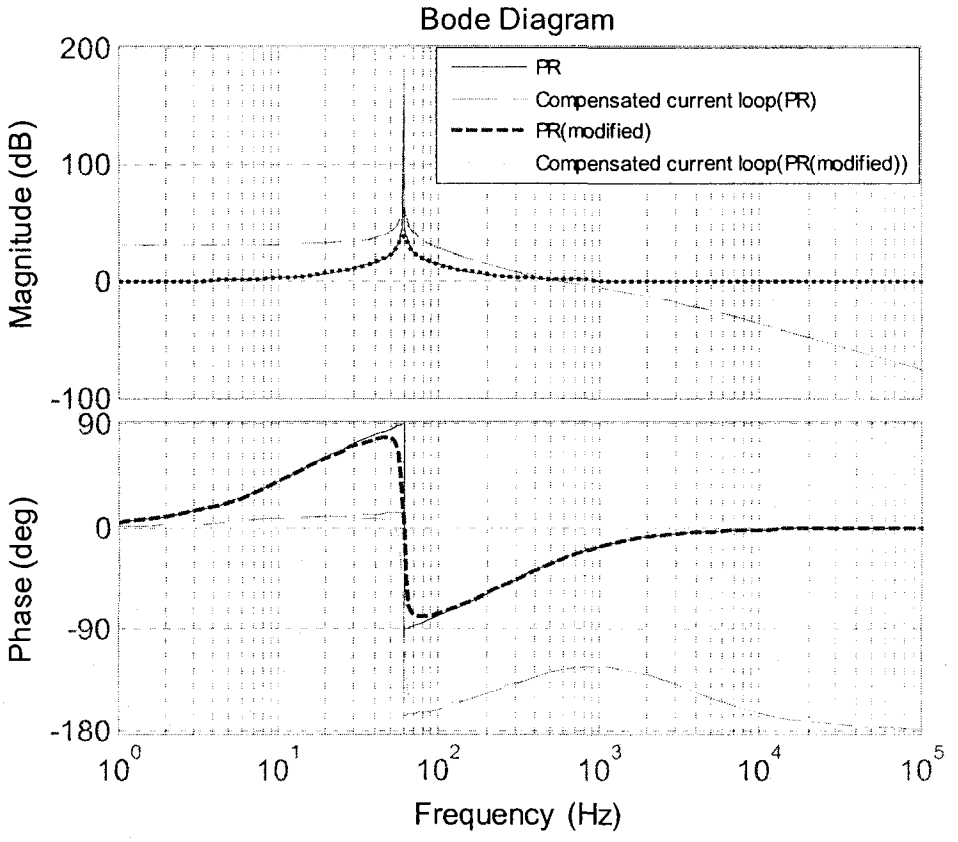


Fig. 2-8 Bode diagram of PR controller and compensated current loop

2.3.2 OUTER VOLTAGE LOOP

The dc link voltage must be regulated to a desired average value. Normally with a dc bus voltage ripple of 1-3 % [22] of the rated dc bus voltage value, the PI controller of the voltage loop is designed for a low cross-over frequency (10 – 20 Hz) in order to attenuate the magnitude of the 120 Hz component that is fed back from the dc bus voltage. This component, after being amplified by the PI controller, is multiplied by the 60 Hz component of the sinusoidal template producing a 180 Hz reference current

component that will certainly appear at the output of the inverter. For operation with a larger dc bus voltage ripple while keeping the magnitude of the 3rd order current harmonic low, the crossover frequency of the voltage loop needs to be further reduced, making the transient response of the dc bus voltage control loop even slower than before. The main problem is that the active power supplied by the first stage to the dc bus can suddenly change resulting in large excursions in the dc bus voltage. In order to deal with the two issues, a voltage ripple estimator is used along with a PI controller designed for a larger bandwidth (~50 Hz). The ripple estimator will calculate the magnitude and phase of the 120 Hz component at the dc bus voltage, which is then subtracted from the signal feedback from the dc bus. This way, the error signal will contain very little of the 120 Hz component and a larger crossover frequency can be used for the dc bus voltage regulating loop, without creating distortions in the ac current.

The inner current loop, that presents a bandwidth of at least an order of magnitude above that of the outer voltage loop with unity feedback, can be represented by a unity gain, at the frequency range considered for the voltage loop. The relationship between variations in the magnitude of the fundamental component of the output current of the inverter and the average value of the dc bus voltage can be calculated using the power balance equations and assuming that the converter is lossless. That is

$$P_{dc} = P_c + P_{ac} \tag{2-19}$$

Where P_{dc} is the power supplied to the dc bus by the dc-dc converter, P_c is the capacitor power and P_{ac} is the active power injected by the inverter into the ac grid.

For determining the impact of the variation of the magnitude of the active part of the reference current, that reflects P_{ac}, on the average value of the dc bus voltage, one neglects P_{dc}. Thus,

$$P_c = -P_{ac} \tag{2-20}$$

The energy stored in the capacitor and the power are given as,

$$\begin{aligned} E_c &= \frac{1}{2} C_{dc} V_{dc}^{\ 2} \\ P_c &= \frac{dE_C}{dt} = \frac{d}{dt}\left(\frac{1}{2} C_{dc} V_{dc}^{\ 2}\right) \end{aligned} \tag{2-21}$$

Therefore,

$$\frac{d}{dt}\left(\frac{1}{2} C_{dc} V_{dc}^{\ 2}\right) = -\frac{\hat{V}_g \hat{I}_r}{2} \tag{2-22}$$

Applying small perturbations around the operating point

$$\frac{d}{dt}\left(\frac{1}{2} C_{dc} (V_{dc} + v_{dc})^2\right) = -\frac{\hat{V}_g (\hat{I}_r + \hat{i}_r)}{2} \tag{2-23}$$

Neglecting steady-state values and square of small perturbations,

$$\frac{d}{dt}\left(\frac{1}{2} C_{dc} \cdot 2 V_{dc} v_{dc}\right) = -\frac{\hat{V}_g \hat{i}_r}{2}$$

$$s C_{dc} V_{dc} V_{dc}(s) = -\frac{\hat{V}_g \hat{I}_r(s)}{2} \tag{2-24}$$

Therefore,

$$\frac{V_{dc}(s)}{\hat{I}_r(s)} = \frac{-\hat{V}_g}{2 s C_{dc} V_{dc}} \tag{2-25}$$

The block diagram used for the design of the voltage loop controller is shown in Fig. 2-9.

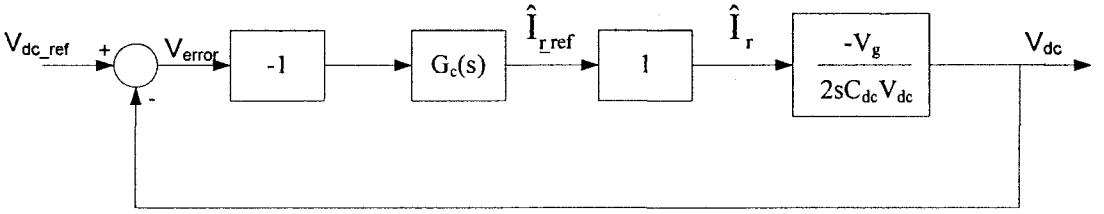


Fig. 2-9 Block diagram of the outer voltage loop

The bode plot of the uncompensated voltage loop is shown in Fig. 2-10. The cross-over frequency (f_x) of the voltage loop was chosen as 50 Hz ($\omega_x = 2\pi f_x = 314.159 rad/s$). The phase margin (PM) of the open-loop system (including PI controller) should be 45°. At this frequency the plant has a gain of 5.975 dB and a phase of -90°. The PI current controller is given by,

$$G_{PI}(s) = \frac{K(1+s\tau)}{s\tau} \tag{2-26}$$

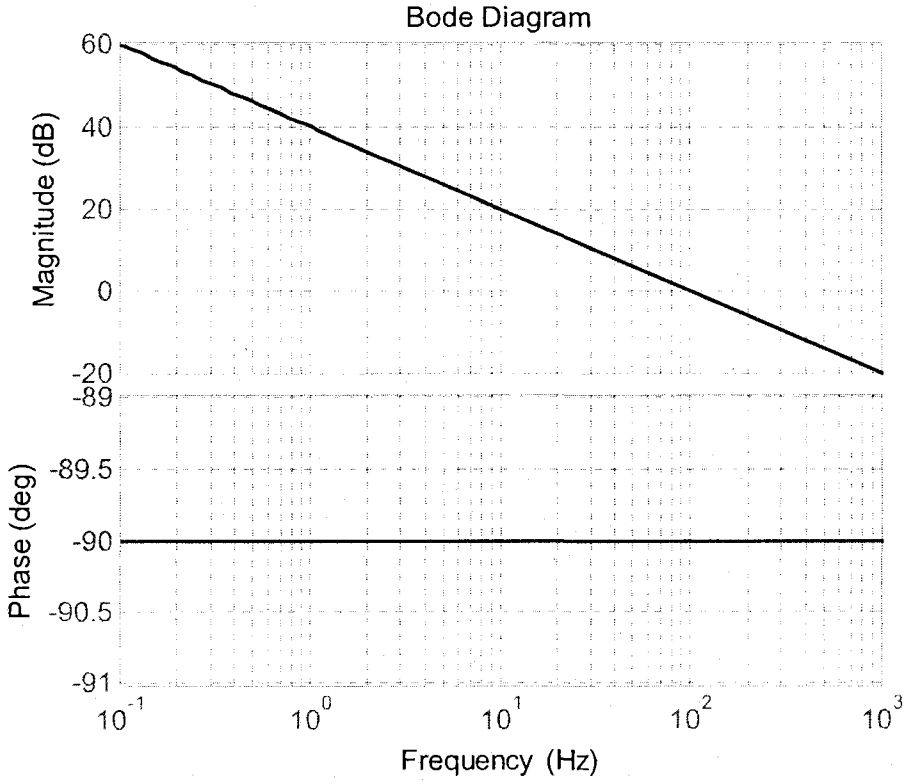


Fig. 2-10 Bode plot of uncompensated voltage loop

Therefore,

$$\angle G_{PI} + \angle G_P = -180^0 + PM \tag{2-27}$$

$$\angle G_{PI} = -45^0$$

Since

$$\tan\left(\angle G_{PI} + 90^0\right) = \tau\omega_x \tag{2-28}$$

$$\tau = 3.183 \times 10^{-3}$$

Let K=1, the magnitude of the open loop system (including the PI controller) at the cross-over point is 5.985 dB. The controller should provide sufficient gain at desired cross-over frequency to make the total gain of the current control loop to be 0 dB. So the gain of the controller is,

$$K = 10^{-\frac{gain(dB)}{20}} = 0.355 \tag{2-29}$$

The bode diagram of the compensated voltage loop and controller is presented in Fig. 2-11.

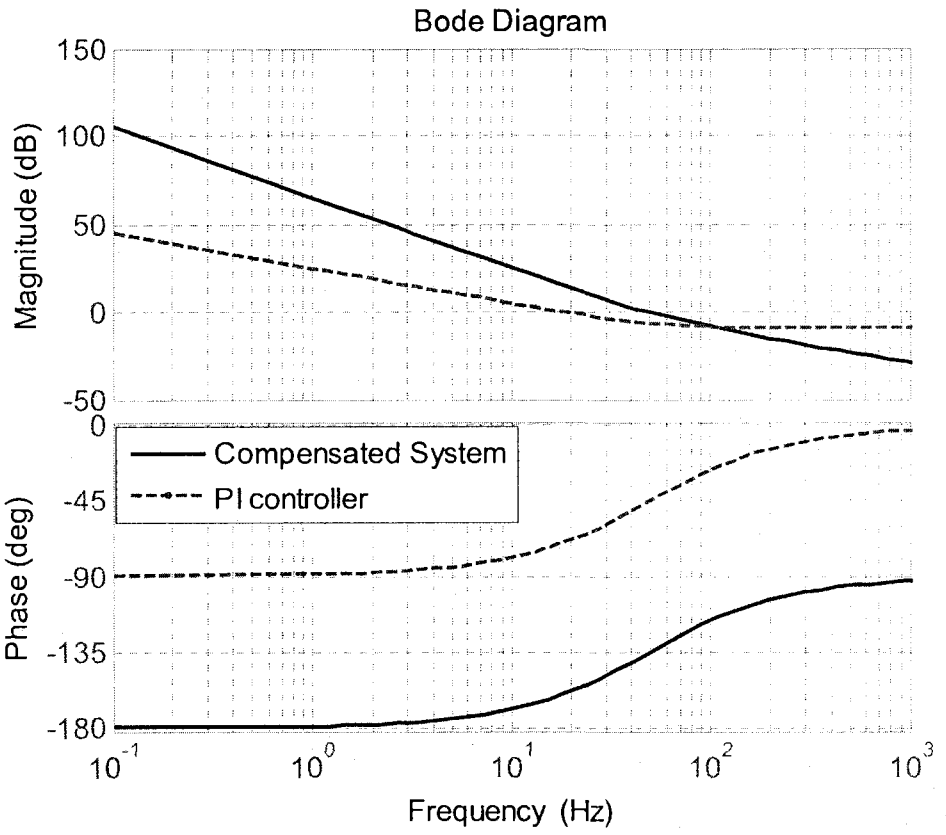


Fig. 2-11 Bode diagram of the compensated voltage loop and PI voltage controller

2.4 DC BUS VOLTAGE RIPPLE ESTIMATOR

The instantaneous power that appears in the dc side of the inverter can be represented by

$$p_{dc}(t) = V_{dc} I_{dc} + C_{dc} V_{dc} \frac{dv_{ripple}}{dt} \tag{2-30}$$

Where I_{dc} is the dc output current of the dc-dc converter.

If $v_g(t)$, $i_g(t)$ and $v_{inv}(t)$ are the grid voltage, grid current and inverter output voltage respectively,

$$v_g(t) = \hat{V}_g \sin(\omega t)$$

$$i_g(t) = \hat{I}_g \sin(\omega t + \theta) \tag{2-31}$$

$$v_{inv}(t) = \hat{V}_{inv} \sin(\omega t + \varphi)$$

The instantaneous power at the output of the inverter is given as

$$\begin{aligned} p_{inv}(t) &= v_{inv}(t) i_g(t) \\ &= \hat{V}_{inv} \sin(\omega t + \varphi) \cdot \hat{I}_g \sin(\omega t + \theta) \\ &= \frac{\hat{V}_{inv} \hat{I}_g}{2} \left[\cos(\varphi - \theta) - \cos(2\omega t + \varphi + \theta) \right] \end{aligned} \tag{2-32}$$

Neglecting the losses in the system, one can say that the ac component of power in the dc side is approximately equal to that at the ac side. From equation (2-30) and equation (2-32) one obtains

$$C_{dc} V_{dc} \frac{dv_{ripple}}{dt} = -\frac{\hat{V}_{inv} \hat{I}_g}{2} \cos(2\omega t + \varphi + \theta) \tag{2-33}$$

$$\frac{dv_{ripple}}{dt} = -\frac{\hat{V}_{inv} \hat{I}_g}{2 C_{dc} V_{dc}} \cos(2\omega t + \varphi + \theta)$$

$$v_{ripple} = \int -\frac{\hat{V}_{inv} \hat{I}_g}{2 C_{dc} V_{dc}} \cos(2\omega t + \varphi + \theta) dt \tag{2-34}$$

Finally,

$$v_{ripple}(t) = -\frac{\hat{V}_{inv} \hat{I}_g}{4 \omega C_{dc} V_{dc}} sin(2\omega t + \varphi + \theta) \tag{2-35}$$

Therefore, peak value $\left(\hat{V}_{ripple}\right)$ and phase angle (ϕ) of the dc bus voltage ripple can be expressed as,

$$\hat{V}_{ripple} = \frac{\hat{V}_{inv}\hat{I}_g}{4\omega C_{dc}V_{dc}} \tag{2-36}$$

$$\phi = \theta + \varphi \tag{2-37}$$

The parameters $\hat{V}_{inv}$ and $\hat{I}_g$ can be determined considering the following steps. The grid voltage is

$$V_g = \frac{\hat{V}_g}{\sqrt{2}} \tag{2-38}$$

The inverter output current can be given as,

$$I_g = I_r + jI_q \tag{2-39}$$

Where I_r and I_q are the rms value of the active and reactive component of the current.

So

$$\hat{I}_g = \sqrt{2}\sqrt{I_r^2 + I_q^2} \quad \text{and} \quad \theta = \tan^{-1}\left(\frac{I_q}{I_r}\right) \tag{2-40}$$

The impedance of the inverter output filter is given as,

$$Z_f = R + jX_l \tag{2-41}$$

Where R and $X_l = 2\pi fL$ are the output filter internal resistance and reactance respectively.

So

$$\begin{aligned} V_{inv} &= V_g + I_g Z_f \\ &= V_g + \left(I_r + jI_q\right)\left(R + jX_l\right) \\ &= \left(V_g + I_r R - I_q X_l\right) + j\left(I_q R + I_r X_l\right) \end{aligned} \tag{2-42}$$

Finally,

$$\hat{V}_{inv} = \sqrt{2}\sqrt{\left(V_g + I_r R - I_q X_l\right)^2 + \left(I_q R + I_r X_l\right)^2} \tag{2-43}$$

$$\varphi = \tan^{-1}\left(\frac{\left(I_q R + I_r X_l\right)}{\left(V_g + I_r R - I_q X_l\right)}\right) \tag{2-44}$$

A PLL synchronized to the utility, can be used to obtain the unity sinusoidal template for the reference current. Besides, the phase provided by the PLL can be used to generate the sin(2ωt) template. The PLL also provides the magnitude of the utility voltage. I_r and I_q can be obtained from the voltage loop controller and the reference reactive power respectively.

2.5 CONCLUSION

In this Chapter, a systematic approach was used for designing the power and control circuits of the single-phase grid interface. The study started with the design of the passive components for the single phase PV inverter. It was followed by the modeling of the dc bus voltage control and ac side current control. A step by step procedure is presented for the controller design to meet the specifications, such as, phase margin at the desired cross-over frequency. Two types of current controller (PI with feedforward and PR) have been presented. A simple PI controller design has been presented for the dc bus voltage regulation. Finally the theory of the dc bus voltage ripple estimator operation is mathematically presented. The performance achieved with the filters, controllers and ripple estimator for the single-phase grid-connected inverter will be verified by means of simulations in Chapter 3 and in an experimental set-up in Chapter 4.

CHAPTER 3

SIMULATION RESULTS

3.1 INTRODUCTION

This Chapter focuses on the preliminary verification and performance assessment of a single-phase grid interface for a distributed generation unit that operates with a large dc bus voltage ripple resulting from the use of a smaller dc bus capacitor. The power and main control circuits of the interface were discussed and designed in the previous Chapters. This study is carried out with simulations using the package PSIM® which is very user friendly. The main issue to be considered in the steady-state condition is the impact of the dc bus voltage ripple on the distortion of the current at the ac side of the interface. The voltage ripple estimator discussed in Section 2.4 should be capable of reducing the propagation of the dc bus voltage ripple through the dc bus voltage control loop leading to a reference current for the inner loop that is virtually sinusoidal. However, the envelope of the switched voltage at the ac side of the inverter will not be a square waveform. It presents the ripple of the dc bus, what can create low frequency non-characteristics current harmonics. A solution based on the modification of the modulating signal, which is made non-sinusoidal (distorted), will be included in the control system to minimize the ac side current distortion.

The simulation studies will also help understand and solve a problem that was identified during the implementation of the experimental set-up. The integrated gate drive circuit of the IGBTs of the inverter present a relatively large dead-time, for avoiding

short-circuits through an inverter leg, leading to distortions in the ac side current. This phenomenon is modeled in the simulation circuit, to allow a quantitative analysis of the distortion as a function of the dead-time and also to verify the effectiveness of a well-known compensating method.

Finally, the proposed system will be compared with a standard one in terms of steady state and transient performance.

3.2 Reducing AC Current Distortion in Single-Phase Inverters

The impact of the dc bus voltage ripple of single-phase inverters on low order current harmonics in the ac side of an inverter was discussed in the previous Chapter and a dc bus voltage ripple estimator was discussed and designed as a means for minimizing it. However, this is not the only way the dc bus voltage ripple can result in low frequency current harmonics in the ac side. These also appear when the inverter operates with sinusoidal pulse width modulation (SPWM) in open loop. The following section discusses an alternative solution for this problem. Then, the impact of the dead-time of the switch driver on the harmonics of the output voltage waveform of the inverter is investigated and an appropriate compensation scheme is presented.

3.2.1 Feedforward DC bus voltage ripple compensation

Sinusoidal pulse width modulation (SPWM) is a well known technique for generating the gating signals of inverters. It is usually assumed that the dc bus voltage is ripple free. In such a case, for a sinusoidal modulating signal the voltage at the ac side

will contain only harmonics at bands around multiples of the switching frequency that is usually of tens of kHz. Thus, the ac filters are relatively small, designed for high frequency (switching) harmonics. However, in real applications, the dc bus voltage can present a considerable ripple, depending on the inverter topology (single or three-phase), the dc capacitor size, the type of load and the operating conditions [23]. In such a case, the envelope of the switched voltage at the ac side of the inverter will not be a square waveform. It presents the ripple of the dc bus that can lead to low frequency non-characteristics current harmonics. This can be seen in Fig. 3-1 for the ideal and practical (dc bus voltage with ripple) cases. Note that the inverter operates with open loop carrier based unipolar SPWM.

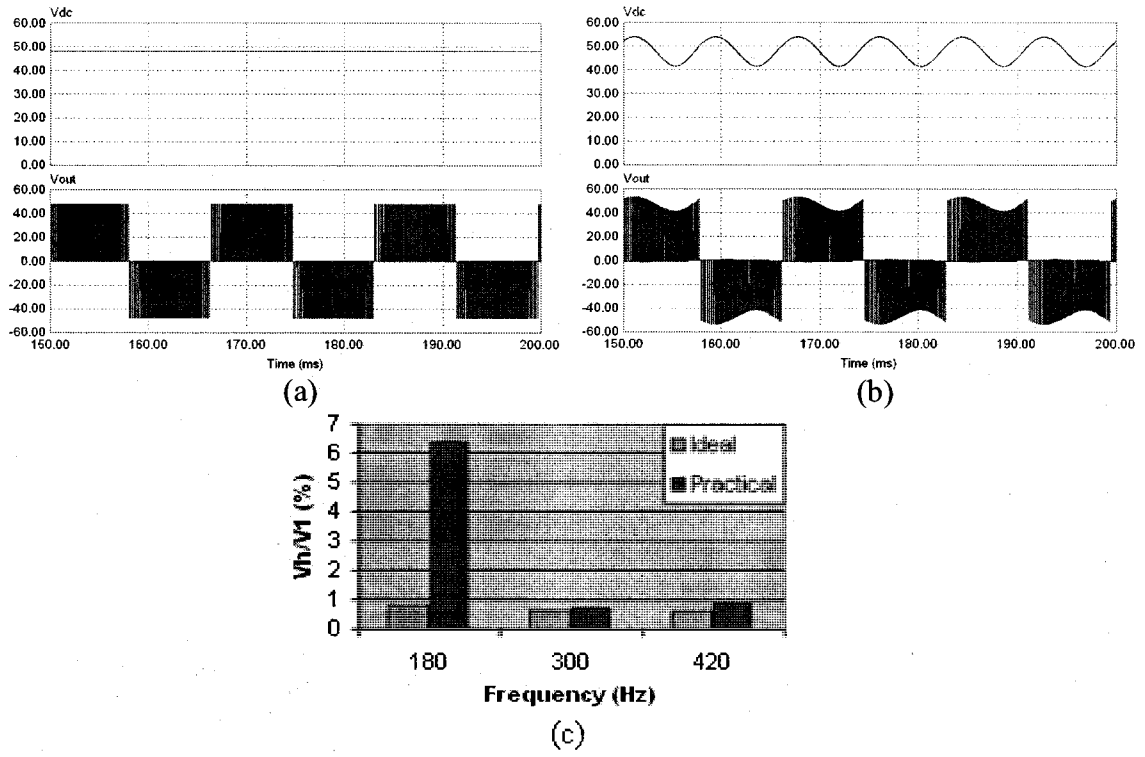


Fig. 3-1 Effect of dc link ripple on the inverter output voltage.
(a) Pure dc link, (b) Dc link with a large ripple, (c) Percentage harmonic component of output voltage with respect to fundamental

To correct this, the carrier signal can be modified accordingly to the dc link ripple [24]. So when the ripple increases then the carrier should be increased proportionally to compensate for the effect of the increased ripple on the inverter dc bus voltage and vice versa. Since the carrier frequency is much higher than the harmonic content of the ripple, the capacitor voltage can be considered constant over one carrier cycle. By simply measuring the capacitor voltage and dividing by the average dc value, we can obtain a normalized quantity. By multiplying this quantity to the normalized carrier, a modified carrier signal can be obtained scaled proportionally to the dc link fluctuation.

Considering that usually carriers and modulators are already available in digital signal processing (DSP) control boards, and that the PWM strategies are already implemented, it is not straightforward to implement the above algorithm. Instead, an inverse implementation, by modifying the reference signal, of the same feedforward mechanism can be implemented. This can be done by dividing the reference with the feedforward values instead of multiplying the corresponding carrier. So, mathematically the modified modulation index is given as,

$$m_a'(t) = m_a(t)\frac{V_{dc0}}{v_{dc}(t)} \tag{3-1}$$

Where $m_a(t)$ is the reference modulation index of the inverter, V_{dc0} is the average dc link voltage and $v_{dc}(t)$ is the dc link voltage. This dc-link feedforward compensation technique will be verified with simulation in Section 3.4.4.

3.2.2 DEAD-TIME COMPENSATION

In order to avoid shoot-through of the dc link through the switches included in the dc-ac inverter, a dead-time or blanking time must be introduced between the turn-off and turn-on gating signals. To ensure that both switches of the inverter leg never conduct simultaneously a small time delay is added to the gate signal of the turning on device. This delay introduces a load dependent magnitude and phase error in the output voltage. There are various solutions available for addressing the dead-time effect. The solution provided by [25] has been adopted for this research work. It can be understood by considering one of the inverter legs over one carrier period. Fig. 3-2 shows the idealized waveforms of the PWM carrier signal and reference voltages for positive current. The idealized gate signals v_{g+} and v_{g-}, ideal output voltage V_{AN}^{*}, actual output voltage V_{AN} without dead-time compensation , actual voltage V_{ANc} compensated for dead-time are also included. It shows there is an average voltage loss or gain per carrier period because of the dead-time.

The basic principle is to compensate for the average loss or gain of voltage over one carrier period. The volt-second error can be interpreted as the difference between the desired voltage V_{AN}^{*} and the actual voltage V_{AN}. The (+) and (-) signs in the bottom trace of Fig. 3-2 indicate that in part of the carrier cycle there is a gain of instantaneous average voltage and in part of it there is a loss of volt-seconds.

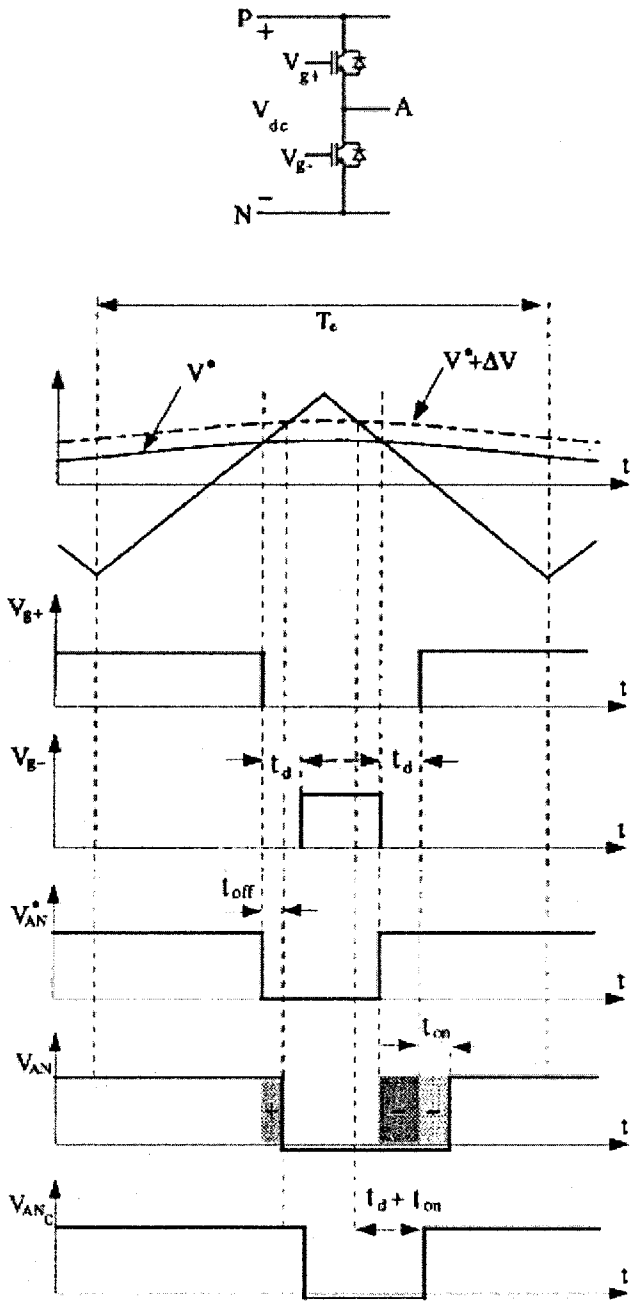


Fig. 3-2 PWM voltage waveforms for positive current.
(From top : reference voltage and carrier signal, gating signal of top switch, gating signal for bottom switch, ideal PWM output voltage, actual output voltage without compensation, actual voltage after compensation)

During the turn-off process the voltage transition is delayed t_{off} (switch turn-off delay time) seconds, hence increasing the average voltage (+ region). While the turn-on process is delayed by the dead-time t_d hence reducing the average voltage (first - region) and additionally, because of the turn-on delay, the voltage does not go high until after t_{on} (switch turn-on delay time), giving rise to an additional reduction in the voltage (second - region). When the current is positive, the net effect over one carrier cycle is the loss of average voltage given by ΔV [25]. The error due to the non-ideal switching of one leg is given as,

$$\Delta V = \frac{t_d + t_{on} + t_{off}}{T_c}\left[V_{dc} - V_{sat} + V_d\right] + \frac{V_{sat} - V_d}{V_{dc}} V^* + \frac{V_{sat} + V_d}{2} \tag{3-2}$$

Where T_c is the PWM carrier period, V_{sat} is the on state voltage drop across the switch, V_{dc} is the average dc link voltage, V_d is the diode forward voltage drop and V^* is the commanded or actual modulation signal.

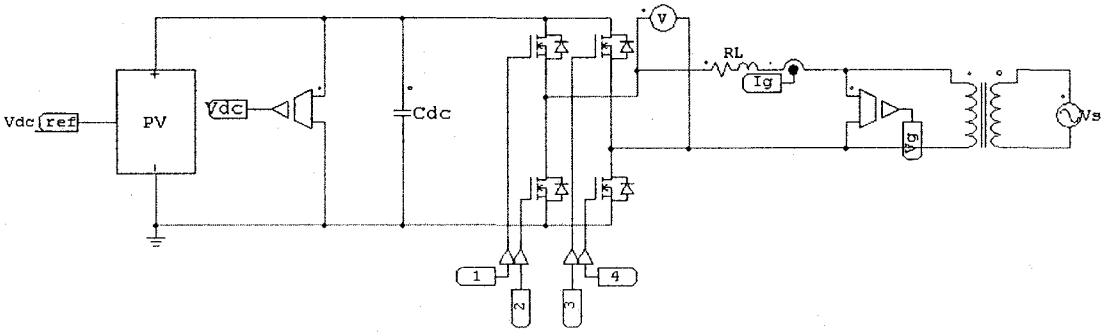
A similar analysis shows that, for negative current there is a net gain of average voltage ΔV. The voltage distortion increases with switching frequency as in equation (3-2). Therefore, the modulating voltage should be modified by ΔV, such that after passing through the inverter, the instantaneous average output voltage is equal to the desired one. This is accomplished by modifying the actual commanded voltage to be $V^* + \Delta V$ when the current is positive and $V^* - \Delta V$ when the current is negative. This approach will be verified by simulation in Section 3.4.3.

The dead-time of switches used in low voltage grid interfaces are usually very small ($t_d < 1\mu s$), not requiring dead-time compensation. However, in this case as the

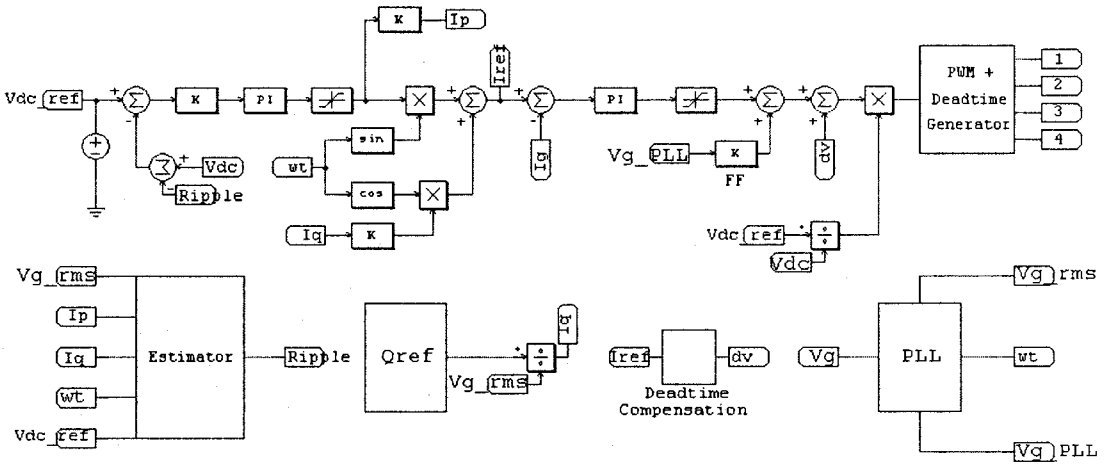
inverter used for the experimental set-up presents an inherent dead-time of 4.8 μs , a large total harmonic distortion (THD) appeared in the ac side current, requiring the use of dead-time compensation.

3.3 SIMULATION SCHEMATICS

The system described in Fig. 2-1 was modeled with PSIM as shown in Fig. 3-3. A PV array with dc-dc converter (average current mode controlled) is represented as a controlled current source to the dc link of the voltage source inverter. The dc capacitor (C_{dc}) is used to buffer the pulsating power of the system resulting from the ac side of the inverter. It decouples the ac side from the PV array. A step down transformer is used between the ac source and the inverter. The low voltage characteristic of the PV array and boost converter (~ 48 V) requires the use of a step up transformer for grid connection at 120 V. The inverter is connected to the low voltage side of the transformer through an L-filter. The filter (with internal resistance) is represented as a RL series impedance. The low voltage side of the transformer is considered as the reference voltage for the inverter control system.



(a) Power Circuit



(b) Control Circuit

Fig. 3-3 Complete PSIM model of the grid connected inverter system

Fig. 3-3 shows that the dc side voltage (V_{dc}) is measured and the estimated ripple ($Ripple$) is subtracted from it. The resulting signal ($V_{dc} - Ripple$) is passed through the voltage controller to regulate the dc bus voltage. The output of the controller is the peak value of the active part of the current and is multiplied with the sine template (in phase with the grid voltage) to obtain the instantaneous active current. The reactive component of the current is obtained from the reference reactive power and the rms value of the voltage. The actual reference current (I_g) is the sum of the active and reactive component of current. It is compared with the reference current and passed through the current controller which gives the modulating voltage of the SPWM inverter. Fig. 3-3 also shows that a PI controller with grid feedforward is used in this case. Dead-time compensation and dc bus voltage ripple compensation is implemented before passing the output of the current controller through the SPWM modulator to generate the gating signals.

A PLL synchronized to the low voltage side of the transformer is used to get the rms value. The PLL generates the orthogonal current templates using a structure based on second order generalized integrator [26]. The phase information provided from the PLL is used in the estimator for dc bus voltage ripple estimation. The schematic of the PLL is provided in Fig. 3-4.

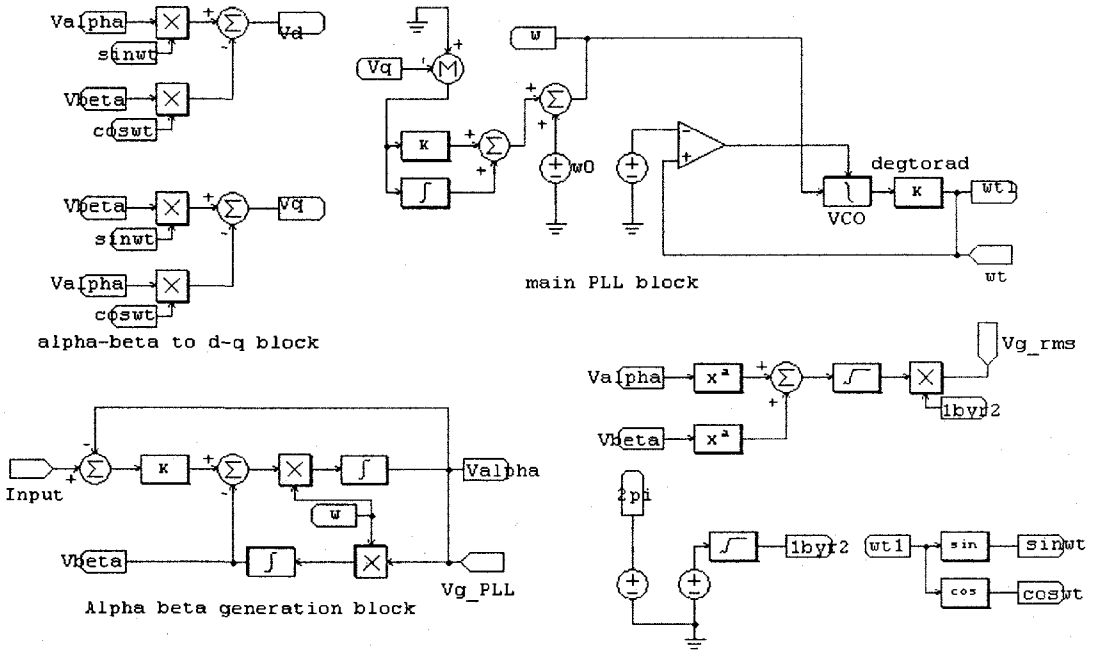


Fig. 3-4 Circuit diagram of the single-phase PLL

The schematic for the dc bus voltage ripple estimator is shown in Fig. 3-5. The inputs to the estimator block are the active (I_p) and reactive (I_q) components of current, the grid rms voltage (V_{g_rms}), the dc bus reference voltage (V_{dc_ref}) and the phase information (ωt) obtained from the PLL. Equation (2-40), equation (2-43) and equation (2-44) are used to implement these blocks. Finally the estimated ripple is given by equation (2-36) and equation (2-37).

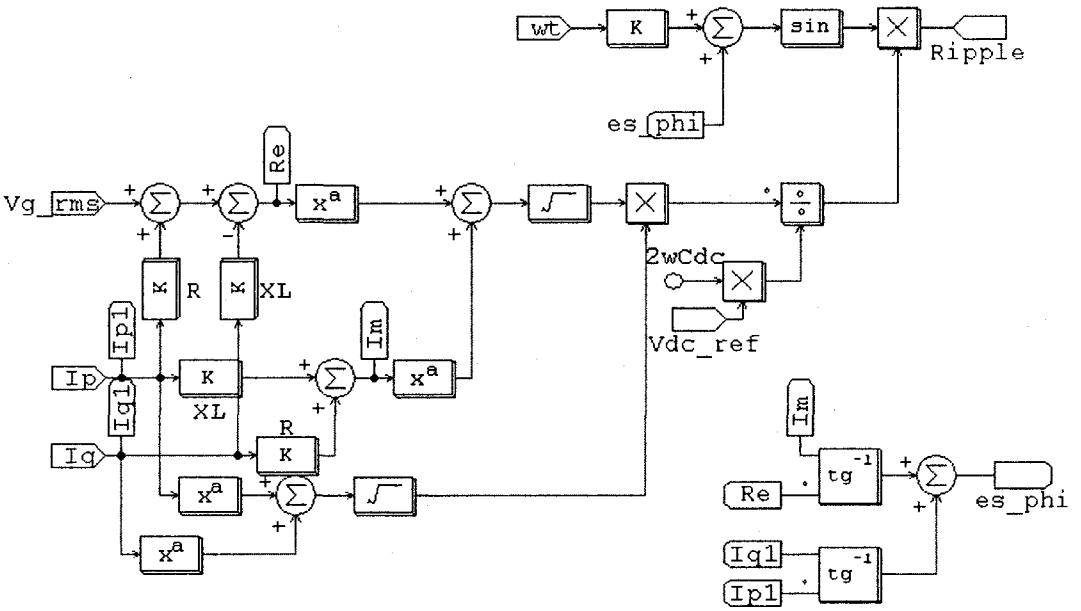


Fig. 3-5 Circuit diagram of the dc bus voltage ripple estimator

The dead-time compensation block is implemented according to equation (3-2). It depends on the dead-time value, switch turn-on and turn-off times, diode voltage drop, switch on state voltage drop, dc link voltage and the modulating voltage. These parameters of the experimental inverter system will be provided in the next Chapter. The switches were modeled with the same specifications and resulted in a dead-time compensation voltage of 1.1 V. Therefore it should be added to the actual control voltage when the current is positive and subtracted when the current is negative. This is implemented as shown in Fig. 3-6.

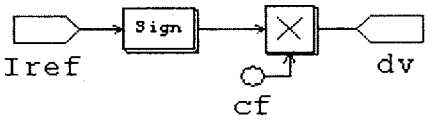


Fig. 3-6 Dead-time compensation circuit

Finally the modulator with dead-time circuit is provided in Fig. 3-7. The control voltage is compared with a 5 kHz triangular carrier signal. Dead-time is introduced between the gating pulses of the same leg to avoid short circuit of the dc bus. The dead-time circuit works on the principle of generating a short duration pulse by a mono-stable timer at each transition of the gating signal. Then the inverted output and the two gating signals of the same leg are passed through an AND gate to introduce the dead-time.

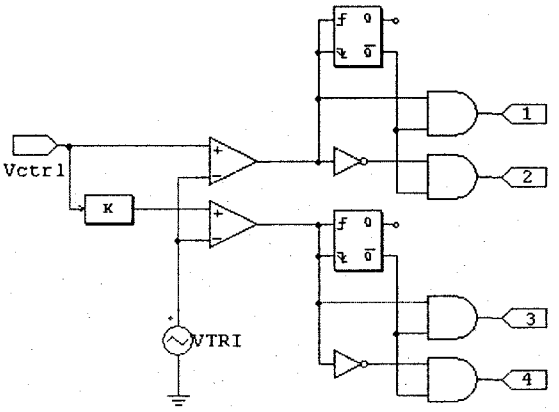


Fig. 3-7 PWM modulator and dead-time generation circuit

3.4 PERFORMANCE VERIFICATION

3.4.1 CURRENT CONTROLLER PERFORMANCE

The performance of the current controllers (PI, PI with grid feedforward and PR) are verified first. This is done by replacing the current source and capacitor in the dc side of the inverter with an ideal dc voltage source. Thus, there is no need for a dc bus voltage control loop and compensation of the dc bus voltage ripple. The dead-time circuit and compensator are disabled for the test of the current controller. An arbitrary sinusoidal reference current is created. Without the feedforward of the grid voltage the PI current

controller introduces a steady state error as shown in Fig. 3-8, which is not acceptable for a grid interface due to errors in the active and reactive power. Steady state and transient responses for the PI with grid voltage feedforward and PR current controller are provided in Fig. 3-8 and 3-9 respectively. They provide almost similar performances when they are designed with the same specifications (PM and cross-over frequency), as can be seen in the figures. There will be always a steady state current error for the PI current controller. With the feedforward, it can be significantly reduced to 0.08 A, but cannot be zero. It's because of the inability of the PI controller to provide a large gain at the concerned (grid) frequency. The PR controller overcomes this problem.

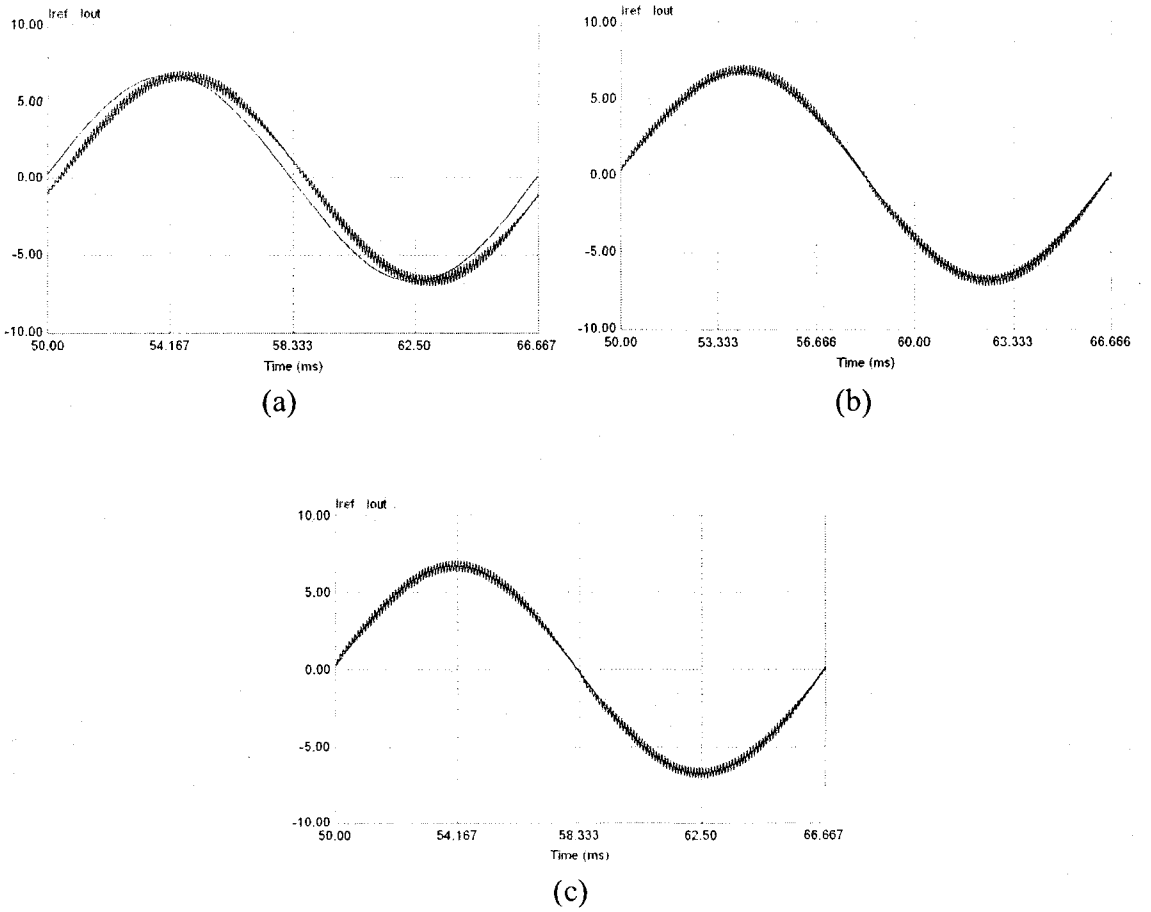
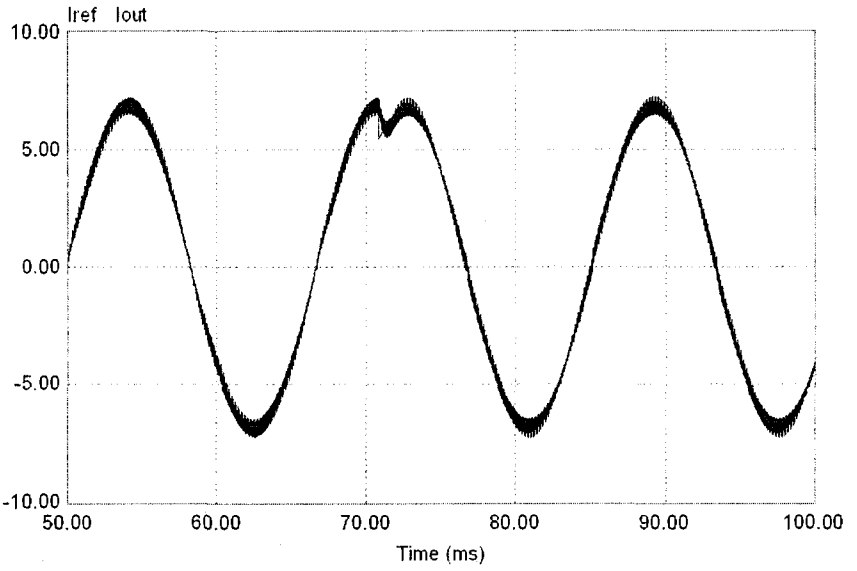
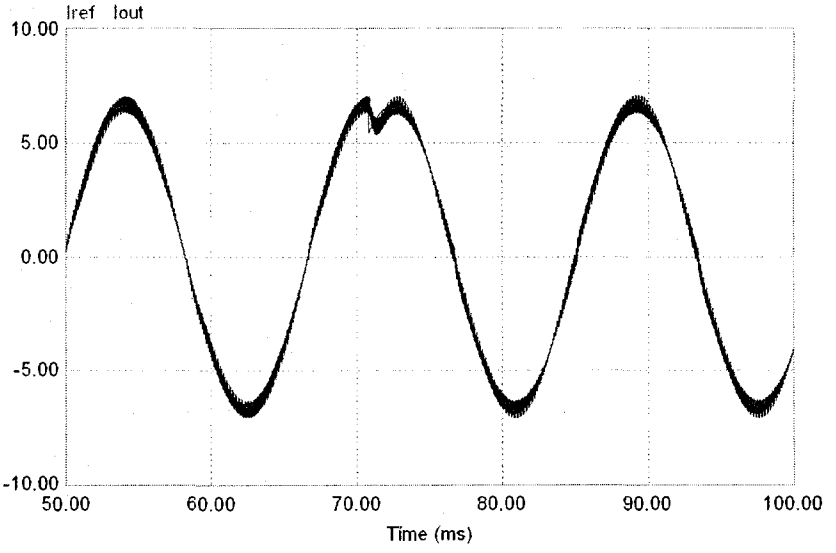


Fig. 3-8 Steady state reference and output current. (a) PI controller without grid voltage feedforward, (b) PI controller with grid voltage feedforward, (c) PR current controller



(a)

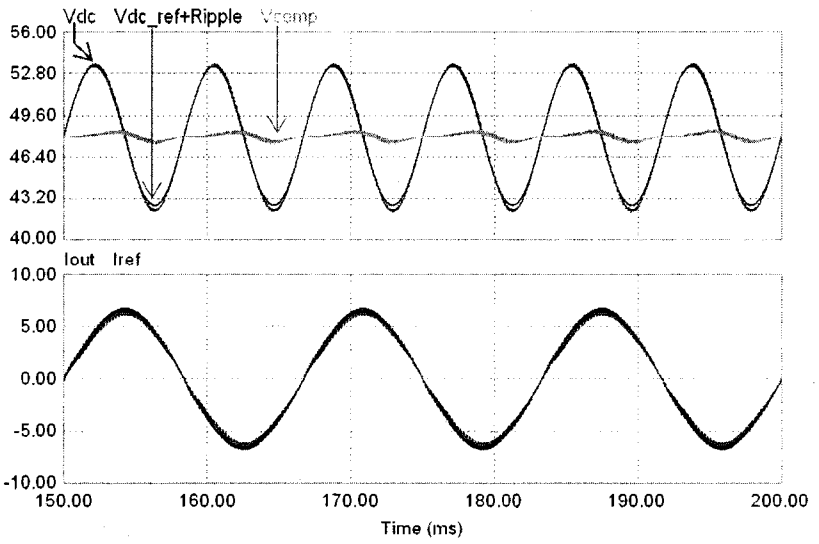


(b)

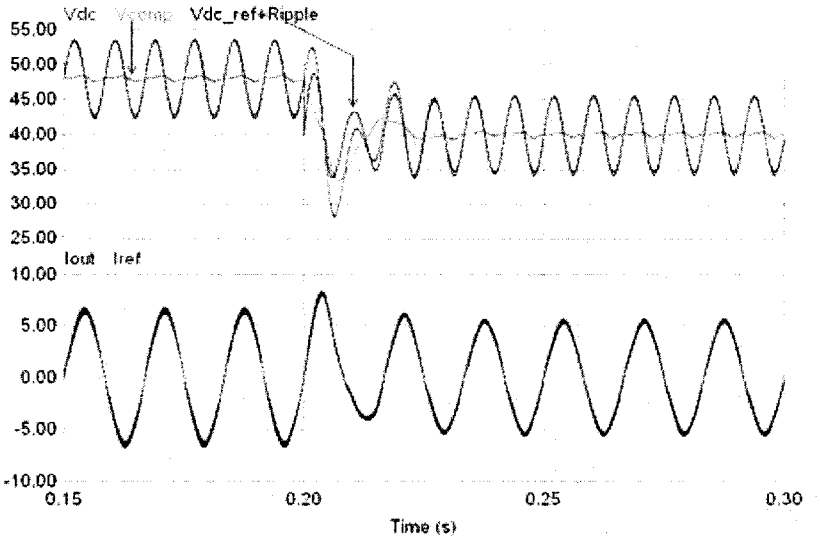
Fig. 3-9 Transient response of the current controller for a step change in PF from 1 to 0.8 lag at rated 100 VA. (a) PI controller with feedforward of grid voltage, (b) PR current controller

3.4.2 VOLTAGE CONTROLLER & ESTIMATOR PERFORMANCE

The voltage controller was designed with a PM of 45° and a cross-over frequency of 50 Hz. Fig. 3-10 shows the steady state and the transient response of the system. The dc bus voltage ripple feedforward compensation, dead-time circuit and compensator are not used for this test. Here V_{dc} is the dc link voltage, V_{comp} (= V_{dc} - *Ripple*) is the signal passed through the voltage loop controller to regulate the dc link voltage. In steady state V_{comp} is almost a ripple free signal. Therefore the voltage loop controller can operate with a higher cross-over frequency. In this case the output of the controller contains a small percentage of harmonics. Therefore, the active component of the reference current contains very low amounts of 3rd and 5th harmonic resulting in a low THD in the output current. The quantitative results showing the effectiveness of the ripple estimator and voltage loop controller are presented later in Table 3-2. For transient response, the dc link voltage is changed from 48V to 40V at 0.2 s while keeping the input current to the dc link the same as before. V_{comp} follows the average value of the dc bus voltage after the disturbance. The dc bus voltage reaches the steady state (settling time for 2 %) within less than 1.5 ac line cycles.



(a)



(b)

Fig. 3-10 Performance of the voltage loop controller with estimator.
(a) Steady state, (b) Transient

3.4.3 DEAD-TIME EFFECT

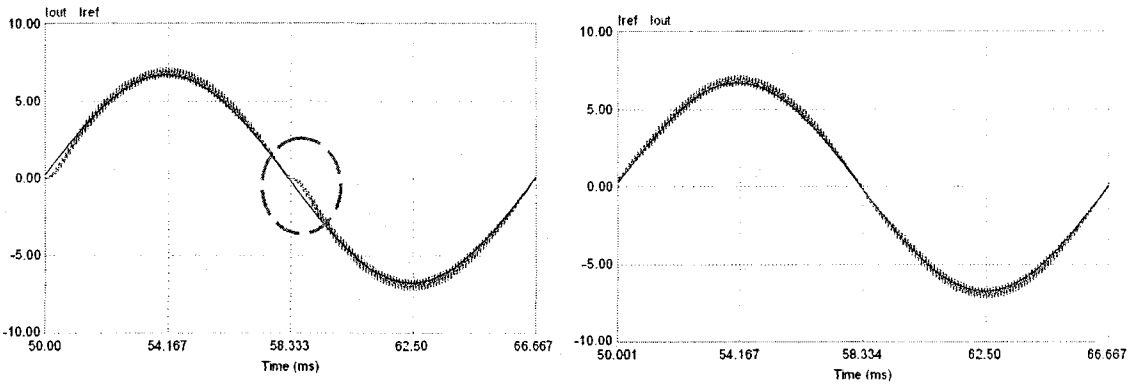
As mentioned before, the gate drive circuit of the inverter switches presents an inherent dead-time resulting in current distortions in the experimental set-up. The phenomenon was modeled in PSIM to allow the assessment of the impact of the dead-time on the current distortion and also for testing a solution for this problem. The same circuit as used for the PR current controller performance assessment is used for this test with the addition of the dead-time circuit and compensator. Table 3-1 presents the effect of dead-time on the THD of the output current when the reference current is a pure sinusoid of 60 Hz and rated value (with no compensation). The inverter switching frequency is 5 kHz.

Table 3-1 Effect of dead-time on THD of output current

Dead-time (μs)	THD (%)
0	0
1	0.35
2	0.88
3	1.44
4	2.08
5	2.66

Therefore, if the driver of the switches come with a relatively large value of dead-time, then it is necessary to compensate the effect of the dead-time. Otherwise, it will be difficult to cope with the requirement of the standards for distributed generation. Fig. 3-11 shows the output current waveform with and without dead-time compensation. Without compensation, around the zero-crossing point the current stays at zero for sometime and then starts following the reference current. Here one sees the distortion

around the zero-crossing of the waveform can be virtually eliminated with the circuit describe in Fig. 3-6 and where "*cf*" is chosen based on equation (3-2).



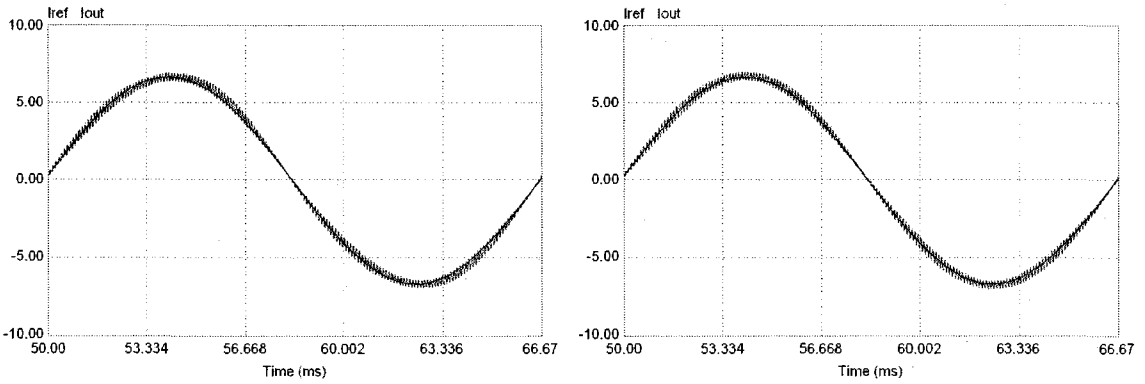
(a) Without compensation (b) With compensation

Fig. 3-11 Steady state reference and output current for a dead-time of 5 μs

3.4.4 EFFECT OF FEEDFORWARD RIPPLE COMPENSATION

As mentioned before (Fig. 3-1), the ripple of the dc link appear as a time varying envelop on the output voltage waveform of the inverter operating in open loop, introducing low order voltage harmonics which results in low order current harmonics in the ac side of the inverter. To address this phenomenon a simplified circuit was implemented where the dc bus is represented by a 48 V battery and a 6 V 120 Hz ac source. An arbitrary sinusoidal 60 Hz reference current and the PI current controller with grid voltage feedforward were used for assessing the impact of the dc bus voltage ripple on the ac side current. The block for the feedforward of the dc bus voltage ripple described by equation (3-1) was implemented as shown in Fig. 3-3 to modify the modulating signal of the inverter. Fig. 3-12 shows the waveforms of the reference current and output current for rated reference current (4.7 A) with and without dc link voltage feedforward block. Fig. 3-13 shows the percentage harmonic content of the current with

respect to the rated fundamental current of 4.7A with and without dc link voltage feedforward. The dominant 3rd harmonic reduces significantly from 3.2% to 0.3% of the rated fundamental current for feedforward ripple compensation, while the 5th harmonic reduces from 0.6% to 0.15%.



(a) Without compensation (b) With compensation

Fig. 3-12 Steady state reference and output current

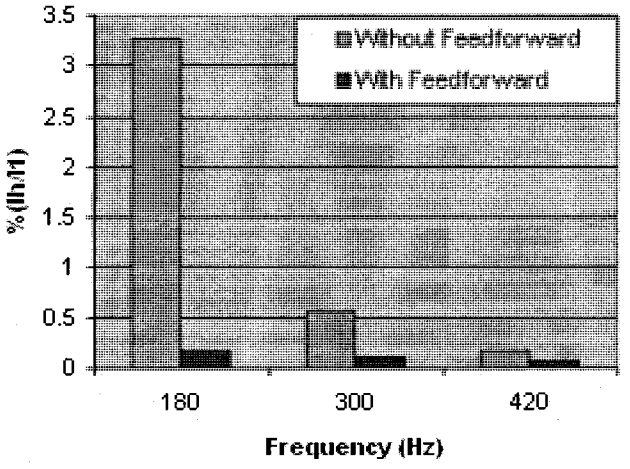


Fig. 3-13 Percentage harmonic current with respect to rated fundamental current

3.4.5 COMPARISON BETWEEN PROPOSED AND STANDARD SYSTEM

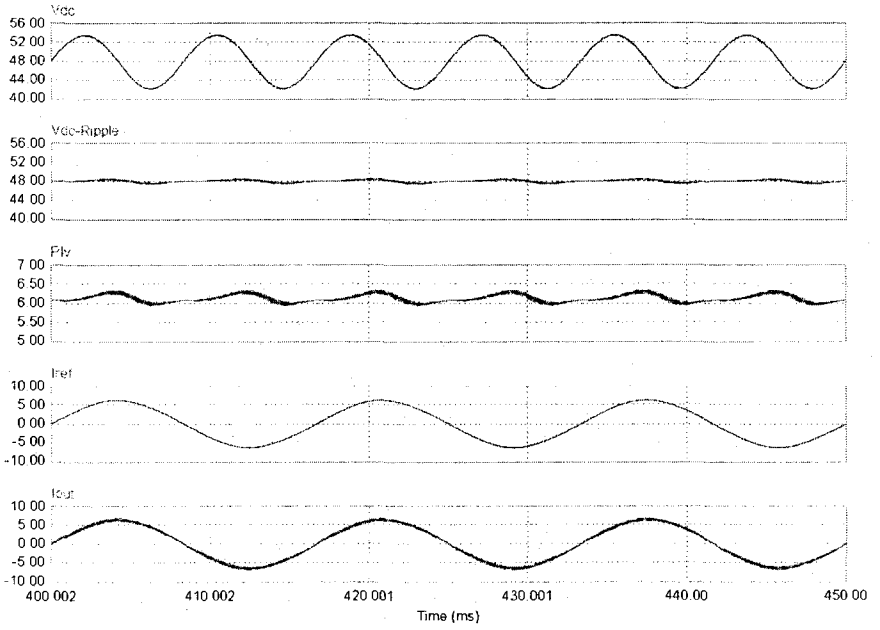
The performance of the single-phase grid connected PV inverter operating with a large dc bus voltage ripple, voltage control loop designed for a bandwidth of 50 Hz and with the voltage ripple estimator will be compared to that of a standard grid interface with a small dc bus voltage ripple and a low bandwidth for the voltage loop. This is done in the following subsections by means of simulations. According to equation (2-5), the dc capacitor of the standard scheme is equal to 1920 μF for a 3% dc bus voltage ripple at rated power. The parameters of its PI controller of the voltage loop, designed for a bandwidth of 10 Hz, using the approach described in Section 2.3.2, are $K_{PI} = 0.273$ and $\tau = 0.016$ s.

The entire circuit diagram as presented in Fig. 3-3 is considered for the proposed system, while for the standard scheme, the voltage ripple estimator is removed. The dc bus voltage is directly fed to the voltage loop controller designed with a low cross-over frequency.

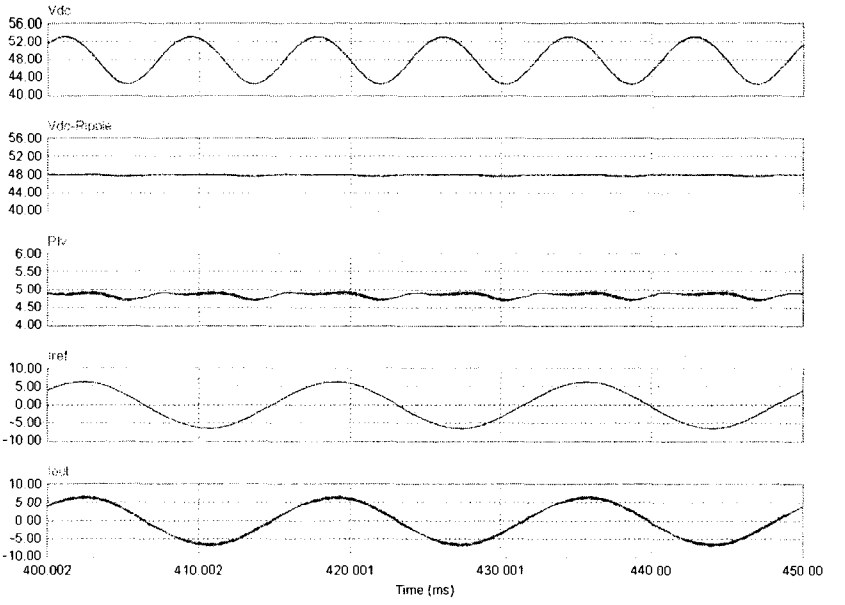
3.4.5.1 STEADY STATE

Fig. 3-14 shows some waveforms for the inverter operating with large dc bus voltage ripple and rated apparent power for different power factors. The waveforms included in the figure are the dc link voltage (V_{dc}), the compensated dc link voltage ($V_{comp} = V_{dc} - Ripple$) for dc link voltage regulation, the output of the voltage loop controller (PI_v), the reference current (I_{ref}) and the output current of the inverter (I_{out}). Since the inverter operates with rated VA, therefore, the magnitude of the ripple in the dc link are almost the same for the three cases, the difference being the variation of the

phase of the ripple with the phase of the output current. The voltage V_{comp} sent to the voltage loop controller is almost ripple free, which ensures low harmonics at its output. The output dc value of the voltage controller determines the magnitude of the active component of the current supplied to the grid, therefore, for 100 W and 80 W, it was 6.2 A and 4.92 A respectively. In case of operation as a STATCOM (reactive power compensator) during night time when no active power is produced by the PV panel, the output is – 0.57 A, i.e., it consumes power from the grid to compensate for the losses of the switches and the capacitor (ESR).



(a)



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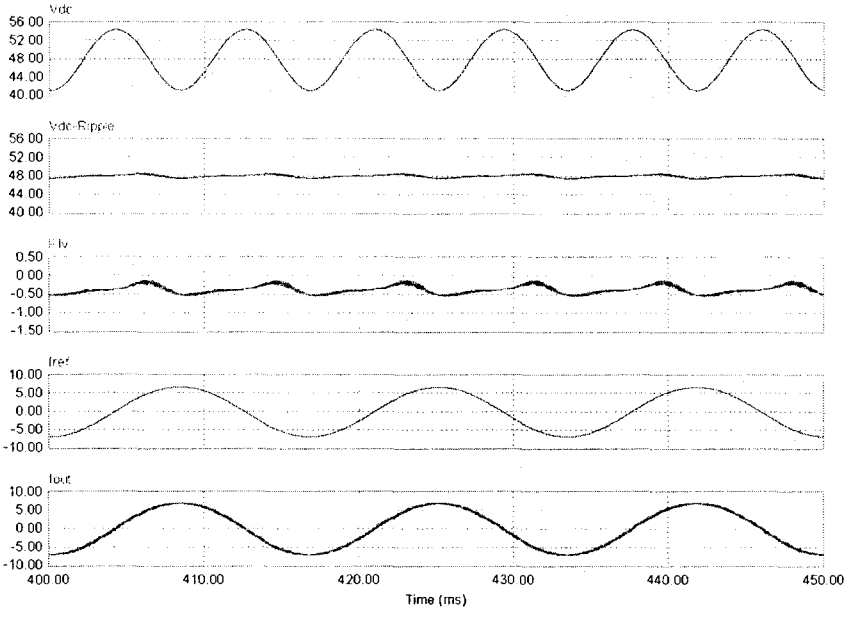
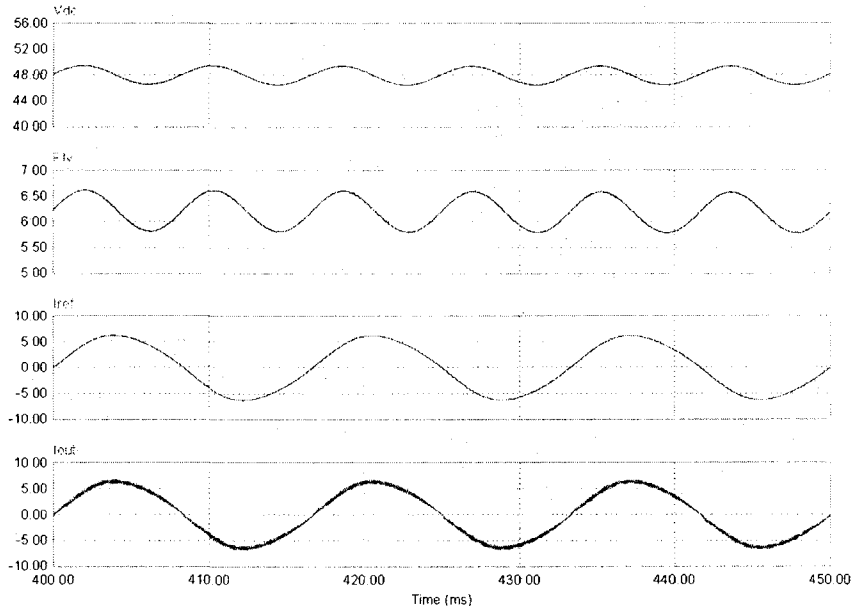


(c)

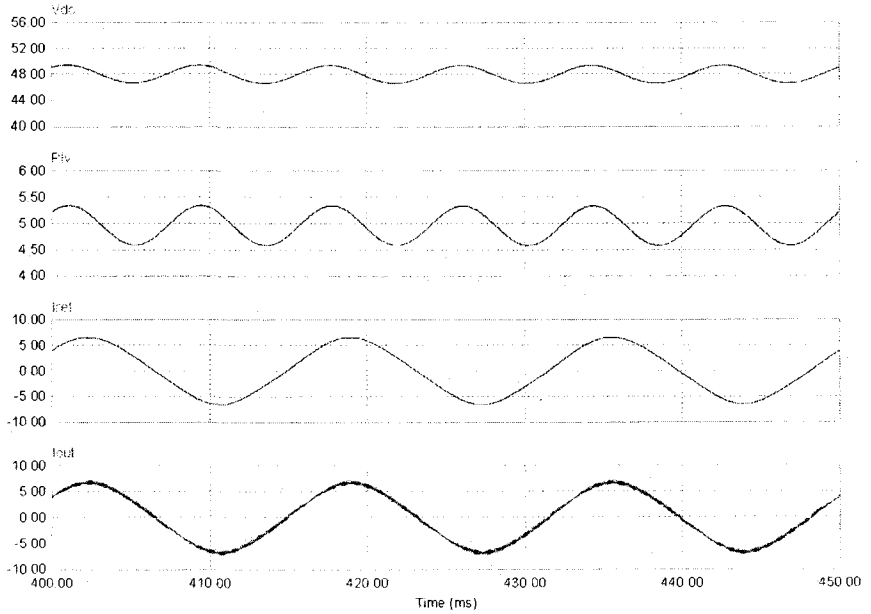
Fig. 3-14 Waveforms for the inverter operating with large dc bus voltage ripple. (a) P =100 W Q = 0 VAR, (b) P = 80 W Q = 60 VAR, (c) P = 0 W Q = -100 VAR

The results for the inverter operating with small dc bus voltage ripple for the same three cases are presented in Fig. 3-15. In this case, the dc bus voltage is directly sent to the voltage controller instead of the compensated dc bus voltage V_{comp} of the proposed

system. The feedback signal for the controller contains more ripple in this case. The output of the voltage controller presents more 2nd harmonic compared to the proposed system although the controller is designed with a lower cross-over frequency. Therefore the THD of the reference and output current are a little bit higher for the standard scheme compared to the proposed system.



(a)



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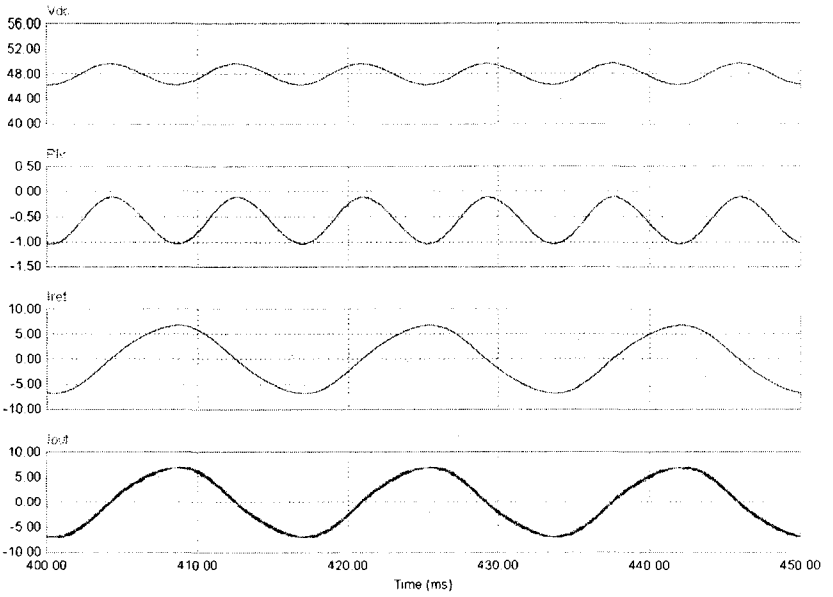


(c)

Fig. 3-15 Waveforms for the inverter operating with small dc bus voltage ripple. (a) P =100 W Q = 0 VAR, (b) P = 80 W Q = 60 VAR, (c) P = 0 W Q = -100 VAR

Table 3-2 presents a summary with the harmonic spectra obtained for the two systems (small and large dc capacitors) and for the three active and reactive power flow conditions shown in Fig. 3-14 and Fig. 3-15. There one can see that the ripple value in the dc bus is much bigger for the small capacitor system than for the large capacitor and that it varies a little bit with the operating conditions although the rated VA at the reference ac voltage point is the same. This could be caused by the different magnitude of the fundamental voltage that appears at the ac side of the inverter according to equation (2-38). Besides, in case of STATCOM operation, there is a small P (real power) supplied to the inverter due to the losses of converter and capacitor. Therefore, in rated reactive power operation, the losses will create a small active component of current resulting in the ripple to be a bit higher than the desired value. Nonetheless, the magnitude of the harmonic components in the output of the dc bus voltage controller is much smaller for the small capacitor system due to the voltage ripple estimator, but it is not zero. Recall

that the ripple estimator was designed for the dominant 2nd order harmonic in the dc bus and assuming an ideal dc capacitor and that all the 120 Hz current that comes from the dc side of the inverter circulates through the capacitor. In practice this is not the case since the capacitor presents an equivalent series resistance (ESR) and part of the 120 Hz current flows through the output part of the dc-dc converter, see Appendix 1.

The dc bus voltage also presents a small 4th order harmonic that appears due to the harmonic ac currents. The presence of small 2nd and 4th order harmonic at the output of the voltage loop controller creates the 3rd and 5th order components in the reference and in the output currents of the inverter. The magnitude of all odd harmonics are less than 3% and the total harmonic distortion (THD) is below 4% for the standard system, while for the proposed system, with small capacitor and ripple estimator, it is 2% and 3% respectively, considering the dominant low frequency harmonics in the output current.

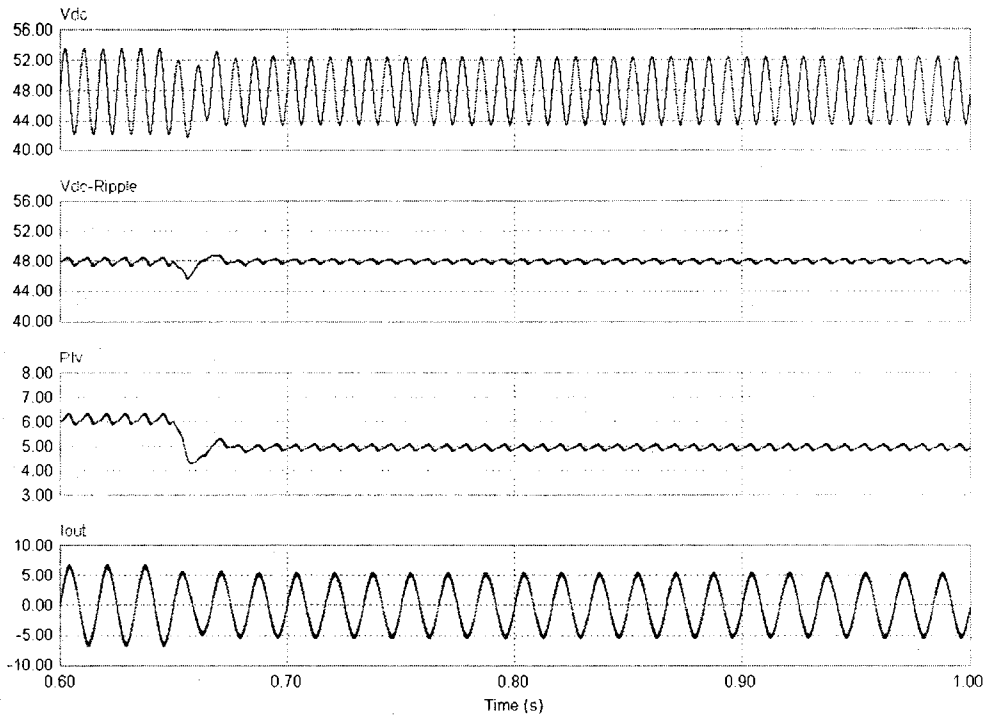
Table 3-2 Frequency spectrum data of the results shown in Fig. 3-14 and Fig. 3-15.

		P = 100 W Q = 0 VAR		P = 80 W Q = 60 VAR		P = 0 W Q =-100 VAR	
		Large C_{dc} and f_x at 10 Hz	Small C_{dc} and f_x at 50 Hz	Large C_{dc} and f_x at 10 Hz	Small C_{dc} and f_x at 50 Hz	Large C_{dc} and f_x at 10 Hz	Small C_{dc} and f_x at 50 Hz
Dc link Voltage	DC	48	48	48	48	48	48
	120Hz	1.44	5.6	1.37	5.24	1.68	5.24
Output of Voltage Controller	DC	6.2	6.13	4.96	4.85	0.57	0.37
	120Hz	0.4	0.12	0.38	0.07	0.46	0.13
	240Hz	0.004	0.06	0.003	0.05	0.01	0.07
Reference Current	60Hz	6.19	6.18	6.23	6.29	6.72	6.74
	180Hz	0.2	0.09	0.21	0.06	0.23	0.05
	300Hz	0.002	0.03	0.003	0.03	0.07	0.03
Output Current	60Hz	6.33	6.32	6.37	6.43	6.87	6.89
	180Hz	0.18	0.08	0.22	0.06	0.27	0.07
	300Hz	0.045	0.07	0.015	0.01	0.04	0.02

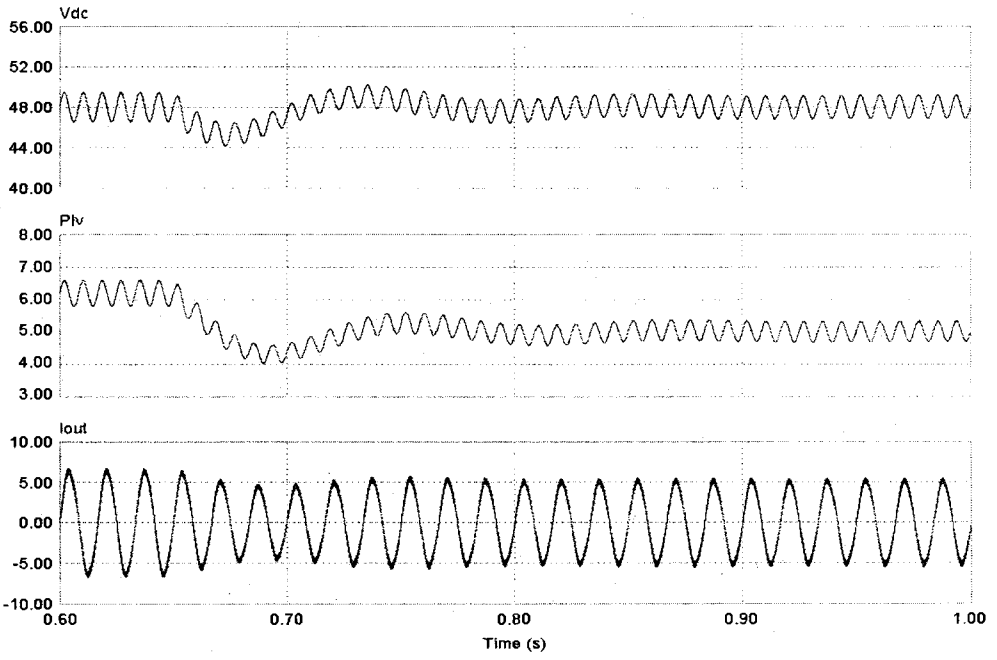
The dominant switching frequency harmonic current, not shown in previous table, was measured with different PF at rated VA and it is always around 0.13 A (< 3% of rated fundamental current), complying with the design specifications for the output L-filter.

3.4.5.2 TRANSIENT RESPONSE

The response of the two systems to a step decrease of 20% in the input power (100 W to 80 W while Q = 0 VAR) injected into the dc bus of the inverter by the dc-dc converter is shown in Fig. 3-16. As the input power supplied decreases at 0.65 s, the magnitude of the dc bus voltage ripple also decreases for both systems. The compensated dc bus voltage (V_{comp}) follows the average value of the dc bus voltage during the transient proving the effectiveness of the estimator for the proposed system. There one sees that the transient response of the system with a small capacitor (large ripple) and higher bandwidth is faster than that of the system with large capacitor and lower bandwidth. There was no significant voltage sag (undershoot) in the dc bus of the first unlike in the second one when there is a sudden change in the power supplied by the PV system. This shows that a fast voltage control loop can effectively prevent large voltage excursions in the dc bus voltage for the inverter with a small capacitor. Therefore, it should be possible to keep the instantaneous voltage at the dc bus above a desired value for a given maximum input power variation.



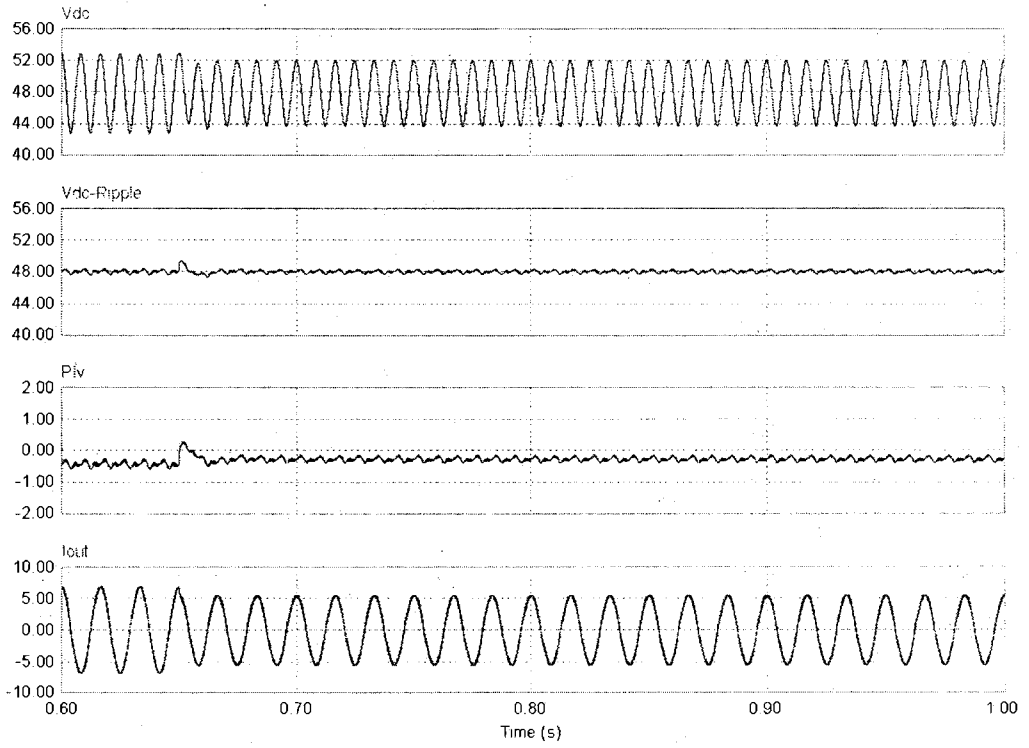
(a)



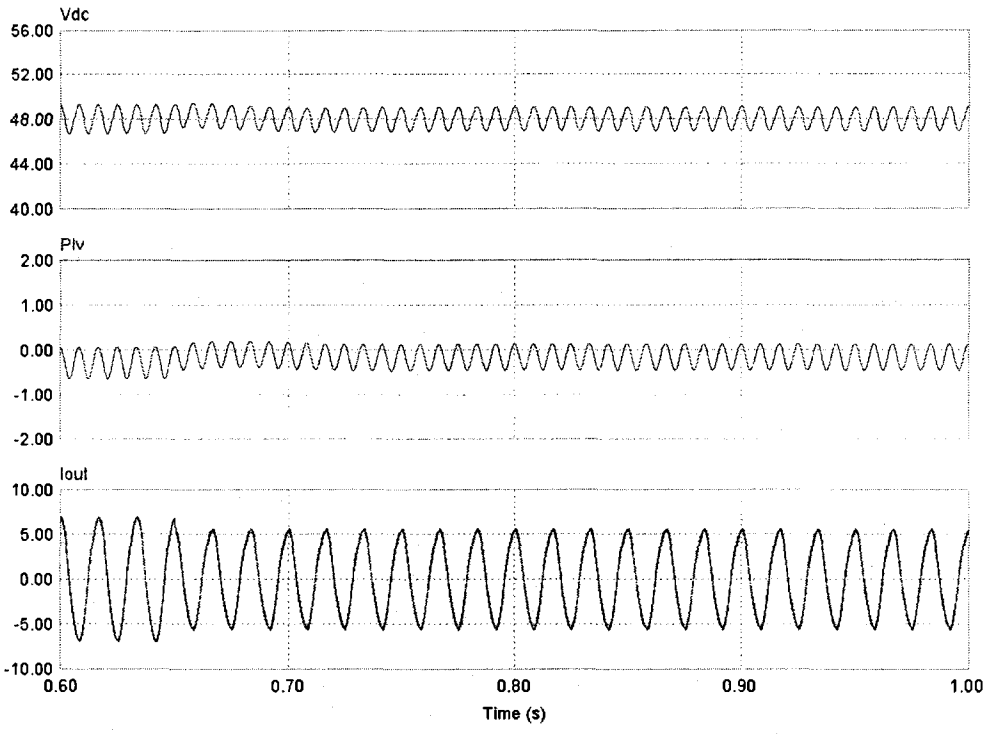
(b)

Fig. 3-16 The response of the inverter system for a step decrease in input power. (a) Small capacitor system, (b) Large capacitor system

The transient response of the inverter operating as a STATCOM (power conditioner) is shown in Fig. 3-17. The reactive power supplied by the inverter was reduced from 100 VAR to 80 VAR at 0.65 s. The variation of the dc bus voltage, output of the voltage loop controller and the ac output current of the inverter are included in the figures. There one sees that the dc bus voltage varies a bit in both cases and that the transient response is faster for the proposed system. As the reactive power decreases for the inverter, the magnitude of the current also decreases resulting in less losses in the inverter. Therefore, the active component of the current supplied to the inverter for regulating the dc bus voltage also decreases which becomes clear at the output of the voltage loop controller whose average value is decreased in magnitude.



(a)



(b)

Fig. 3-17 The response of the inverter system for a step change in reactive power. (a) Small capacitor system, (b) Large capacitor system

3.5 CONCLUSION

This Chapter has presented details of the circuit implementation in PSIM® of the grid-connected PV interface for small scale distributed power generation as well as reactive power compensation. The importance of the dead-time and dc bus voltage ripple compensation has been addressed and circuit implementation of the compensation techniques are presented. The effectiveness of the voltage ripple estimator, current controllers (PI with grid voltage feedforward and PR) and the dc bus voltage control loop are verified by simulation. The proposed system is compared with a standard system that operates with large dc bus capacitor and the voltage loop controller is designed with a

bandwidth at 10 Hz. In steady state the low order harmonics are analyzed, while in the transient, it is verified by amount of undershot/overshot and the settling time of the concerned parameters. The system is capable of working with large dc bus voltage ripple that allows the use of a small, non-electrolytic capacitor for increased reliability. The effect of the reduced inertia of the smaller dc capacitor on the magnitude of the voltage excursions during transients due to active power variations was compensated with a voltage control loop designed for a higher bandwidth. The voltage ripple estimator played an important role in allowing the bandwidth of the voltage loop to be increased without significantly increasing the distortion of the output current. Chapter 4 will present the experimental result of the simulation work.

CHAPTER 4

EXPERIMENTAL RESULTS

4.1 INTRODUCTION

This Chapter presents details of a laboratory prototype that was implemented to validate the simulation results discussed in the previous Chapter. It also allowed the identification of other problems that can arise in a practical system. For instance, the issue with the harmonic distortion in the ac side current due to the relatively large dead-time of the gate drive circuit of the inverter was identified at this stage. This was followed by supplemental simulation studies to obtain quantitative results between the dead-time and the low frequency harmonic distortion in the ac current. Besides, the impact of the ESR of the dc capacitor in the accuracy of the ripple estimator was observed as well as the effect of the finite speed of the digital signal processor (DSP). The experimental results for different operating conditions are presented and a comparison study in terms of steady state and transient response is provided with a standard system. Finally the conclusions are stated.

4.2 EXPERIMENTAL SETUP

Fig. 4-1 depicts the laboratory set-up used to obtain the experimental results. The single-phase full bridge inverter is implemented with a SEMISTACK system by SEMIKRON. It uses an IGBT module (SKM50GB123B, SEMIKRON) with a gate drive circuit (SKHI22, SEMIKRON) for the IGBT switches. A solar array simulator (E4350B,

Agilent) operating in the constant current mode emulates the dc-dc MPPT converter and PV array. It allows step variations of the current injected into the dc bus to verify the response of the system to variations of the PV power generation.

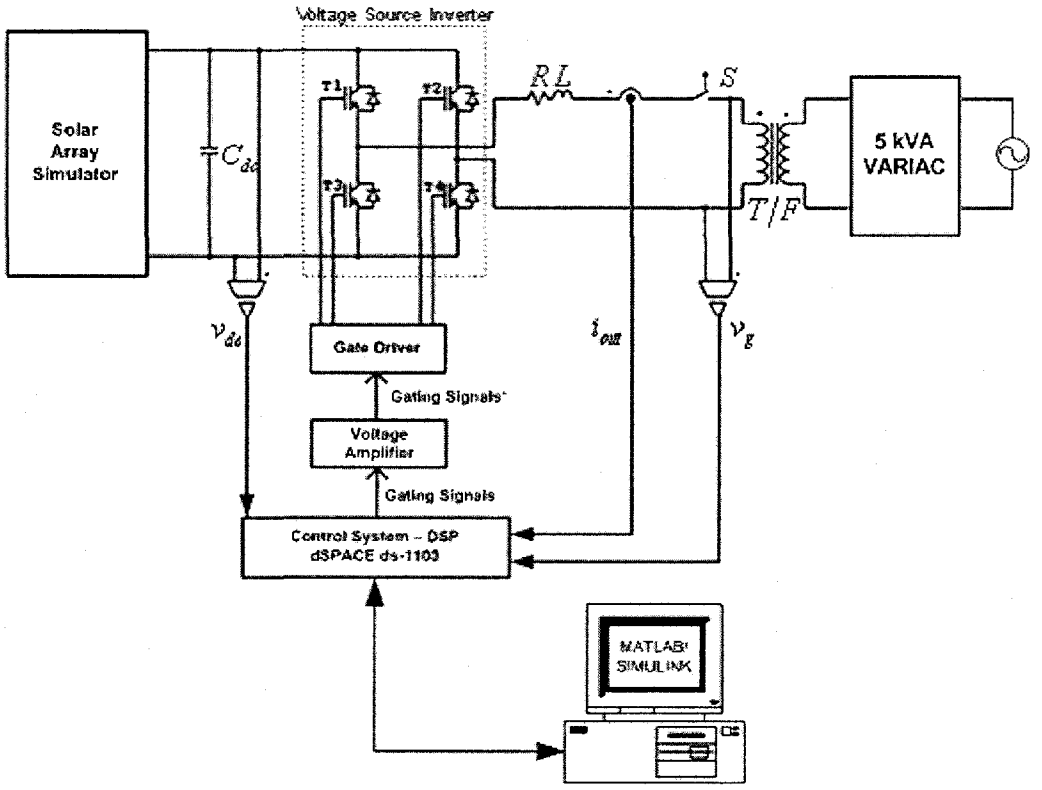


Fig. 4-1 Laboratory set-up used in the experiments

A *small* ($500\,\mu F$) dc bus capacitor is connected at the output of the solar array simulator when operating with the proposed control strategy (voltage ripple estimator and higher bandwidth for the dc bus voltage loop). A *large* ($1920\,\mu F$) capacitor is used for the analysis of a "standard system", where the voltage ripple estimator is deactivated and the bandwidth for the dc bus voltage loop is set at 10 Hz. The operation of the solar array simulator (SAS) is limited to a maximum capacitance of $2000\,\mu F$ at its output. Above this value, the SAS cannot behave as a current source. The maximum output voltage for the PV array simulator is 60 V. Thus the rated dc bus voltage was chosen as 48 V to

allow the operation of the inverter with a large dc link ripple, up to 12 V peak to peak for the proposed system operating at rated power.

At the ac side of the inverter one sees an $1.5mH$ inductor with an internal resistance of 0.15 Ω that is used to connect the inverter to the low voltage side of the single-phase transformer (120 V : 21 V) through an ac grid breaker. The high side of the transformer is connected to a $5kVA$ VARIAC (variable 3 phase autotransformer) used to represent the ac grid. It is worth mentioning that the dc bus voltage (48 V minus peak voltage ripple) of the inverter has to be higher than the peak value of the ac side voltage (30 V peak) for full control of the power flow. A Hall effect current sensor (LA55-P, LEM) is used to monitor the ac current of the inverter and provide a feedback signal to the ac current control loop. A voltage sensor (LV100, LEM) is employed to monitor the voltage at the low side of the transformer. It provides synchronism for the reference current of the inverter and also allows the measurement of the phase and magnitude of the voltage at that point. Another voltage sensor (LV100, LEM) is placed at the dc side of the inverter to provide feedback signal to dc bus voltage control loop.

A digital signal processor (DSP) development kit (DS-1103, dSPACE) was employed to monitor and implement the control circuit of the inverter. The inverter ac side voltage and current and the dc side voltage are sensed and acquired into the dSPACE controller board for processing. The gating signals generated by the dSPACE system that presents low voltage (0-5 V) and needs to be amplified (to 0-15 V) for the gate driver of the IGBTs.

The control circuit of the grid interface is implemented in SIMULINK as shown in Fig. 4-2. The ADC (analog to digital conversion) blocks are used to bring the external signals into SIMULINK. Appropriate gain adjustment of the feedback signal is done because of the sensor and dSPACE gains. The reference ac voltage is passed through the PLL to generate the phase, sine and cosine templates, reconstruct a noise free version of the reference voltage for feedforward control and also to provide the rms value of the grid voltage. The circuit diagram inside the PLL block is provided in Fig. 4-3. The ripple estimator circuit inside the main sub-system is shown in Fig. 4-4. It provides the ripple signal which is subtracted from the original dc link voltage. The resulting signal is compared with a reference voltage to regulate the dc link voltage at the desired value. The output signal of the dc bus voltage controller represents the active part of the ac current. The reactive part of the current is calculated from the reference reactive power and magnitude of the ac grid. These two currents are combined to create the actual reference ac current. The ac side current is compared with this and passed through the current controller. Finally the output of the current controller is the control (modulating) voltage for pulse-width modulator, after passing through the feedforward and dead-time compensation blocks. Fig. 4-5 and Fig. 4-6 present the blocks used for the implementation of the voltage and current loop controllers in SIMULINK.

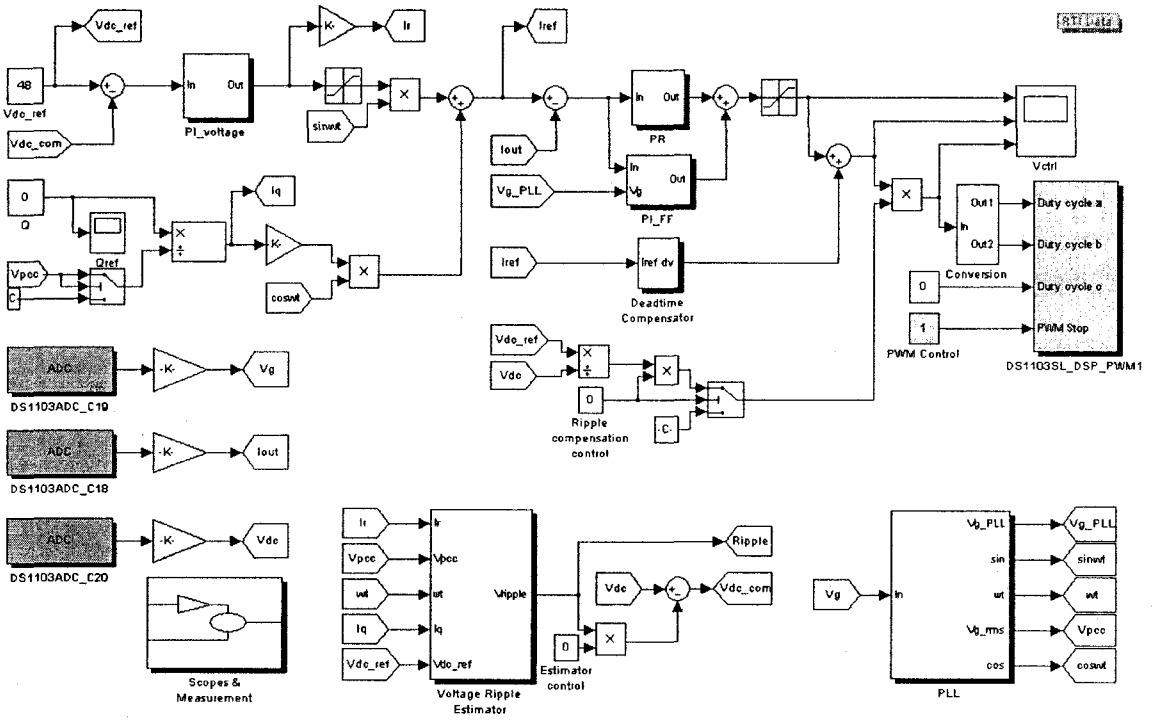


Fig. 4-2 SIMULINK implementation of the control system for the experimental setup

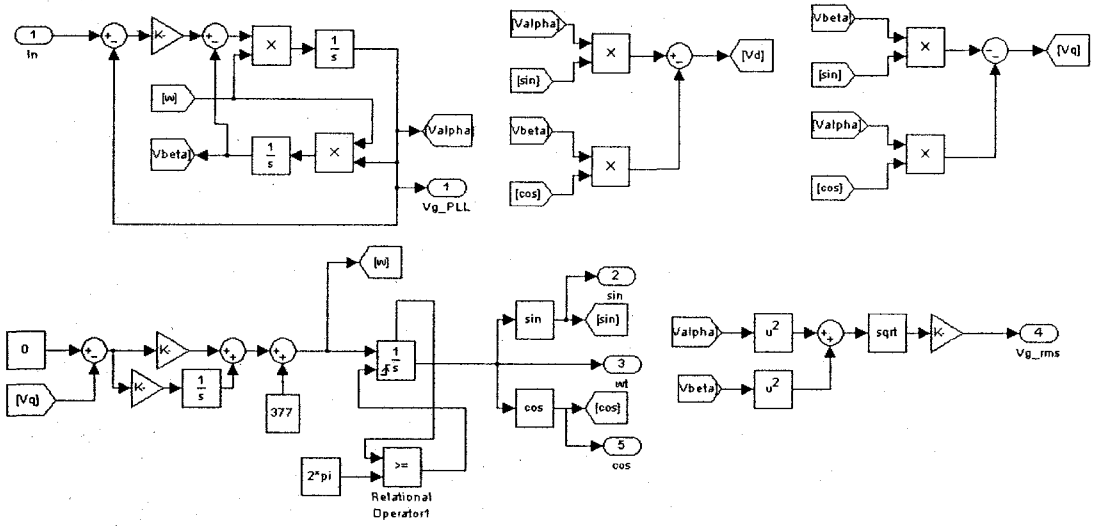


Fig. 4-3 PLL block inside sub-system

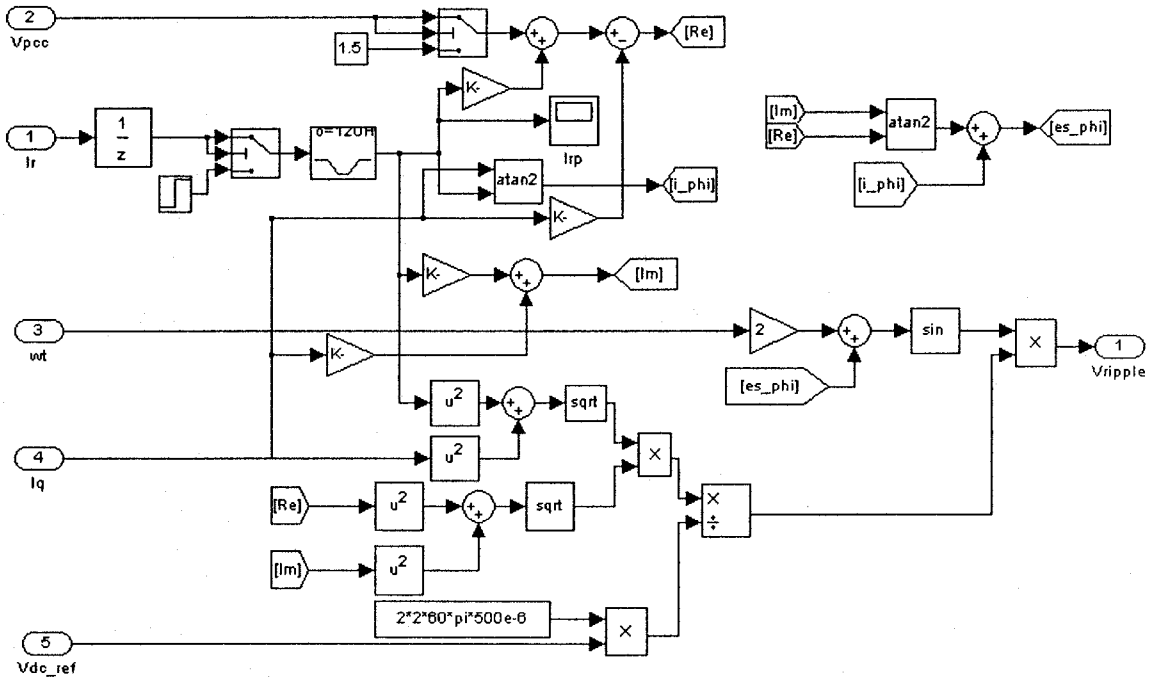


Fig. 4-4 Estimator circuit inside sub-system

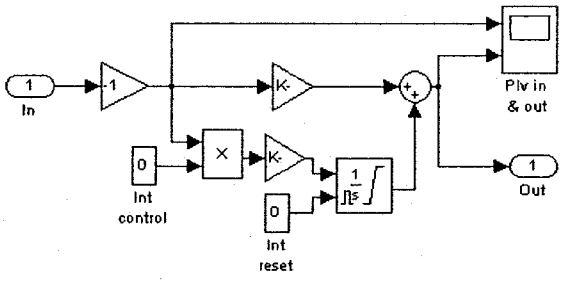
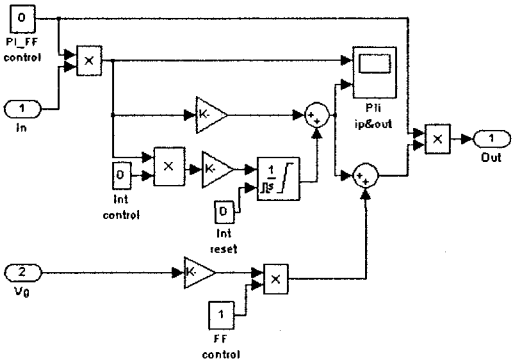
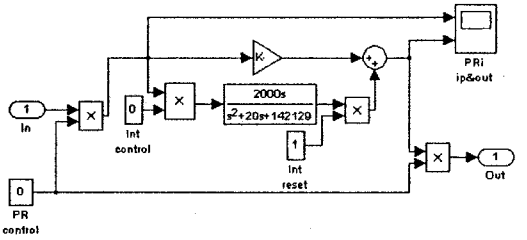


Fig. 4-5 SIMULINK implementation of PI voltage controller



(a)



(b)

Fig. 4-6 SIMULINK implementation of the current controller.
(a) PI with feedforward, (b) PR

The PWM block from dSPACE library of SIMULINK uses a triangular carrier signal whose amplitude varies between 0 and 1 V. Therefore, the zero level of the control voltage should be at 0.5 for this block. So a conversion circuit is used to modify the control voltage as shown in Fig. 4-7. The PWM block requires one control signal for each leg of the inverter. At first the actual input control signal is multiplied by a factor of 0.05, so that the peak value is within 0.5 for linear modulation. A dc offset of 0.5 is added to the modulating signal for the first leg. So the signal varies in between 0 and 1, while 0.5 represents the 0 level of the scaled down control voltage. For the second leg, the modulating signal is inverted first, by multiplying with a gain of -1, and then the offset value of 0.5 is added to it. Then the signals are sent to the PWM block to generate the gating signals of the 4 switches with unipolar SPWM.

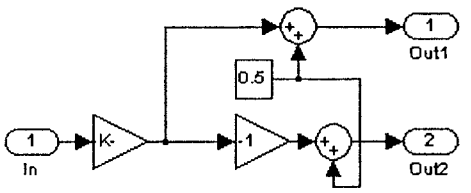


Fig. 4-7 Conversion circuit for the control voltage to use with PWM block

The dead-time compensation voltage is calculated using equation (3-2). The parameters of the equation are determined from the datasheet of the SEMISTACK module [27], and using these values the dead-time compensation voltage was found to be 1.1 V. The value of the parameters vary depending on the operating conditions, i.e., current, temperature etc. In our application the compensation voltage is calculated for the rated current and the temperature is considered as 25° C. Fig. 4-8 shows the dead-time compensation circuit used in the experiment.

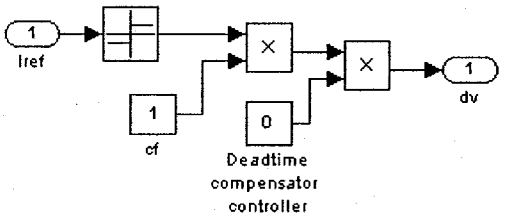


Fig. 4-8 Dead-time compensation circuit

4.3 THE DSP DEVELOPMENT SYSTEM

The dSPACE system is a common hardware architecture used for rapid prototyping of electrical control systems. It is composed of a DS-1103 PPC controller board and also equipped with a Motorola PowerPC 604e processor that allows for the simulation of large-scale floating-point control algorithms in real-time. A full range of I/O devices are available on-board. Automatic code can be generated from block

diagrams using the Real-Time Interface in SIMULINK. I/O functions are specified graphically as part of the simulation model. Therefore, the control circuit can be developed in MATLAB/SIMULINK for practical control of an external plant by the inclusion of I/O blocks in the control circuits.

4.3.1 HARDWARE ARCHITECTURE

The embedded Motorola PowerPC 604e processor allows fast floating-point calculation at 333 MHz. This high-performance superscalar microprocessor has three integer execution units, one floating-point arithmetic unit, and a separate load/store unit for fast memory access. It has 32 KByte on-chip cache for instruction and data. A 2 MByte local memory is used for program and data of the simulation model. The local memory is fully cached and cannot be accessed by the host PC in standard operation mode. For data buffering and exchange between PowerPC and the host, up to 128 MByte of non-cached global memory is available. The host interface of the board is used to perform board setups, program downloads, and runtime data transfer.

The board is suitable for a wide range of closed-loop applications due to its large number of I/O devices. High-resolution A/D converters (16-bits and 12 bits) with a sampling time of 4 μs and 800 ns, respectively, are available, as well as D/A output channels with a resolution of 14-bit and a 5 μs settling time. Besides, it also consists of 32 digital I/O channels and a serial line interface.

4.3.2 REAL-TIME INTERFACE TO SIMULINK

MATLAB/SIMULINK is widely used for modeling, analysis, design and off-line simulation. The Real-Time Interface enhances the SIMULINK block library with additional blocks, which provide the link between SIMULINK and the real-time hardware, as shown in Fig. 4-9. To graphically specify an I/O channel the corresponding block icon is picked up from the I/O block library and attached to the SIMULINK controller model. I/O parameters, such as voltage ranges or resolutions, can be set in appropriate dialog boxes. At first, The SIMULINK model is transferred into real-time code, using the Real-Time Workshop, state flow control, and the Real-Time Interface. Code generation includes the I/O channel specification and the multitasking setup, which are translated into appropriate function calls of the Real-Time Library. It is a C function library providing a high-level programming interface to the hardware.

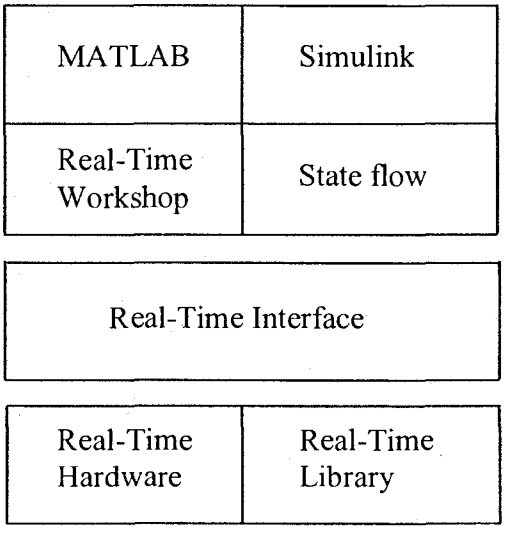


Fig. 4-9 The Real-Time Interface in the MATLAB/SIMULINK environment

4.3.3 SIMULINK BLOCK LIBRARY FOR DS-1103

Based on the microprocessor units on the board, the block library for the DS-1103 PowerPC Controller Board is subdivided into two major parts. The library shown in Fig. 4-10 comprises all I/O units that are directly served by the PowerPC master processor and it includes block icons for the standard I/O channels such as A/D, D/A converters, digital I/O and incremental encoder blocks. The slave DSP library, shown in Fig. 4-11, offers frequently used functions of the TMS320F240, such as single-phase and three-phase PWM signal generation, frequency measurement, A/D conversion, and digital I/O.

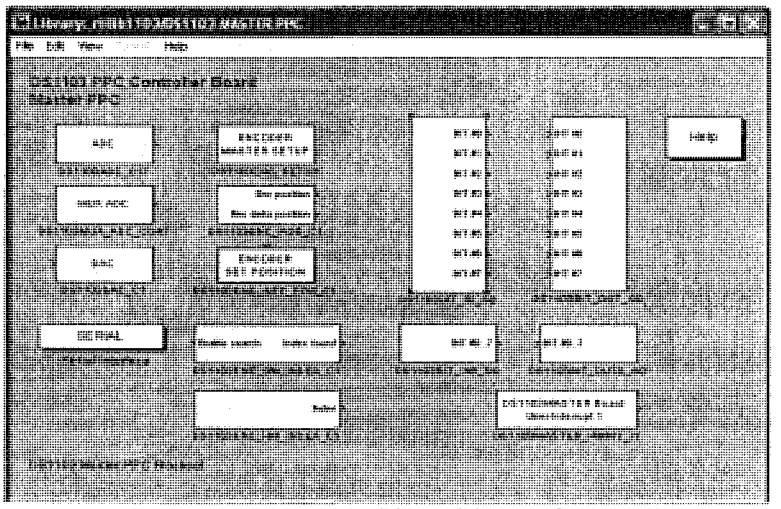


Fig. 4-10 Master Processor block library for SIMULINK

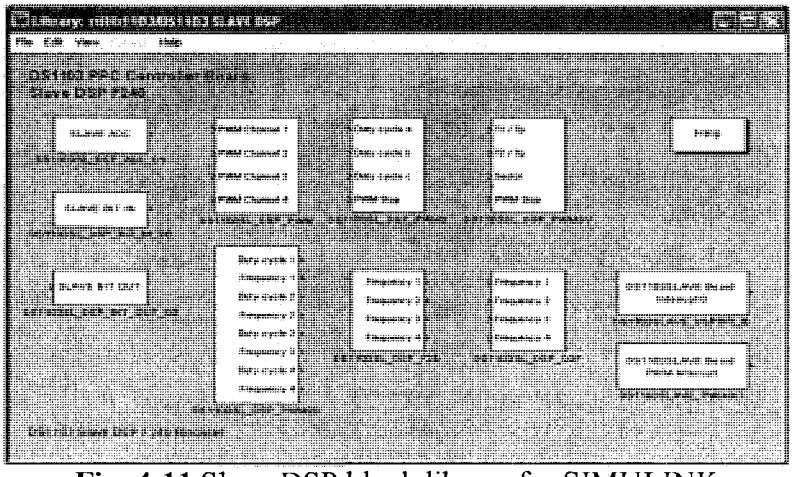


Fig. 4-11 Slave DSP block library for SIMULINK

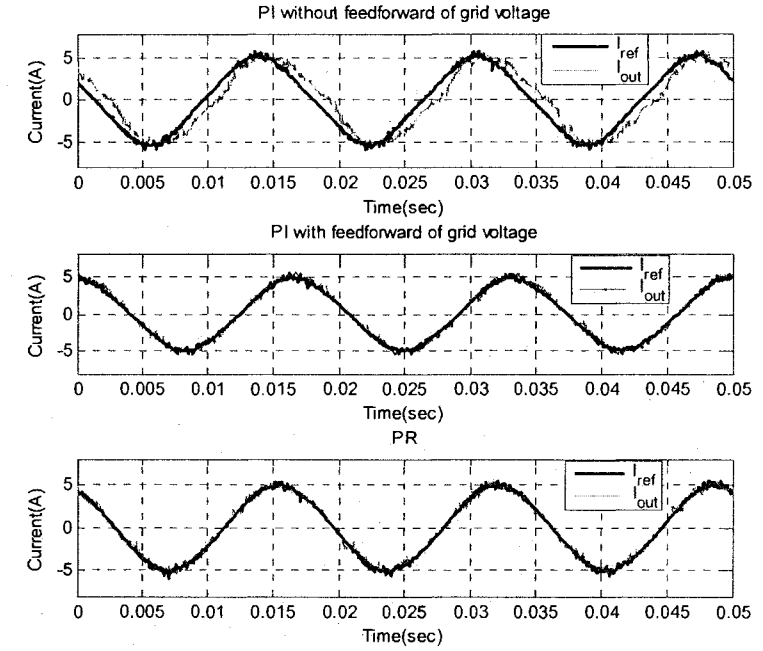
4.4 EXPERIMENTAL RESULTS

The results presented in the previous Chapter are verified in terms of the experimental result in this Section. Experimental results are provided to verify the performance of the proposed control strategy. The performance of the voltage controller, current controller, and estimator are verified. Finally the performance of the PV inverter with small dc link capacitor is compared with the standard scheme. The real power is provided to the dc link of the inverter from the SAS. The inverter supplies it to the grid. The reference reactive power input is provided in control desk of dSPACE and the inverter should supply or absorb that amount of reactive power.

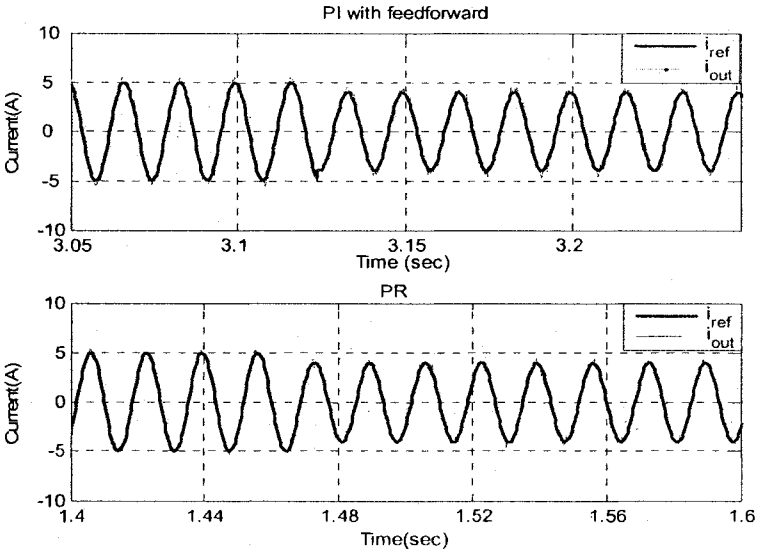
4.4.1 PERFORMANCE OF THE CURRENT CONTROLLER

The performance of the current controllers (PI, PI with grid feedforward and PR) was verified first. In this case, the SAS was disconnected, and a rectifier with a large dc capacitor was connected to the input of the inverter. So, the dc link behaves as a voltage source. Thus, there is no need for a dc bus voltage control loop and compensation for the dc bus voltage ripple. Since the dead-time is inherent in the gate drive circuit, the dead-time compensator is used for this test. An arbitrary reference current was created. Fig. 4-12(a) shows the reference current and output current for the three current control schemes. For the PI current controller alone, there is a large phase error between the reference and the output current without feedforward of grid voltage in steady-state. When the grid voltage feedforward signal is added, the phase error is significantly reduced. In case of PR current controller, the steady state error is zero. Fig. 4-12(b) shows the transient response for the PI with grid voltage feedforward and for the PR

current controller. The reference current is changed from rated value to 80% of rated value at 3.2 and 1.47 s for PI with feedforward and PR respectively (in their respective figure). The output current follows the reference current and settles down to the steady state almost instantaneously.



(a)

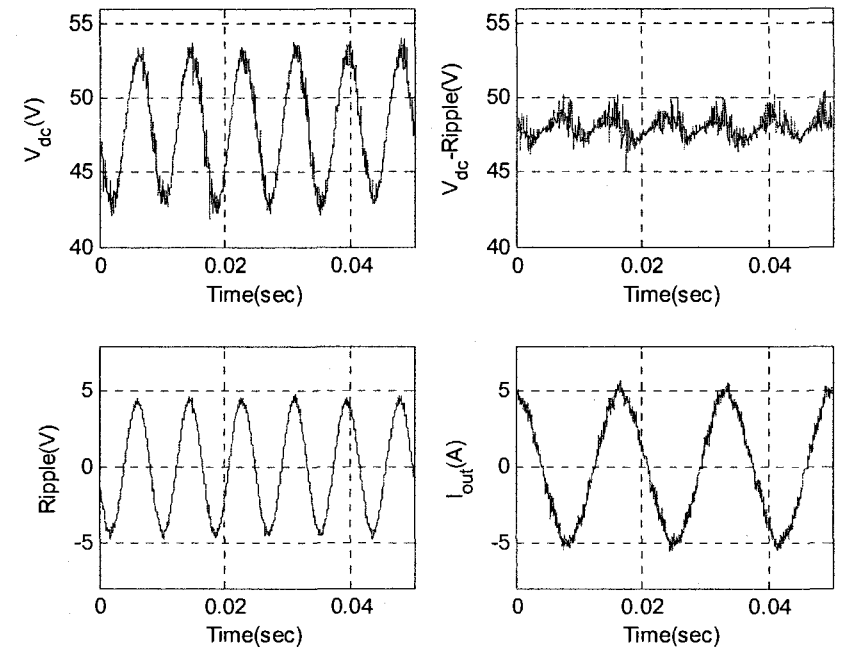


(b)

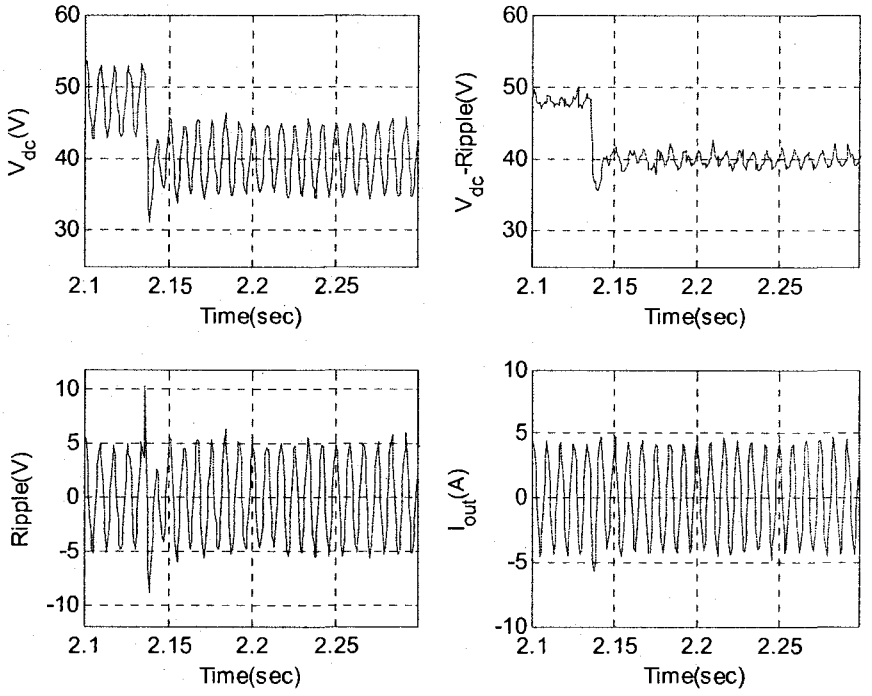
Fig. 4-12 Performance of current controller. (a) Steady state reference and output current, (b) Transient response for a 20% decrease in the reference current

4.4.2 PERFORMANCE OF VOLTAGE CONTROLLER AND ESTIMATOR

The performance of the voltage controller and estimator was determined using the control circuit of Fig. 4-2. In this case, the SAS supplies power to the dc link of the PV inverter and the voltage loop controller is designed for a PM of 45° at a cross-over frequency of 50 Hz for the small dc link capacitor. Fig. 4-13 shows the performance of the estimator for operation with large dc bus ripple. The steady state and the transient response of dc link voltage (V_{dc}), compensated signal for dc bus voltage control (V_{comp} (= V_{dc} - *Ripple*)), the estimated ripple (*Ripple*), and output current of the inverter (i_{out}) are included. In steady state, V_{comp} is almost a ripple free signal. This allows the operation of the controller with large cross-over frequency and low distorted output current. The reference value for the dc link voltage is changed from 48 V to 40 V at 2.13 s while keeping the input current to the dc link the same as before for analyzing the transient response of the system. V_{comp} follows the average value of the dc bus voltage after the disturbance, since the magnitude of the ripple depends on the instantaneous value of the active component of current. The dc bus voltage reaches the steady state within around 1.5 ac line cycles, which complies with the simulation result of the previous Chapter.



(a)



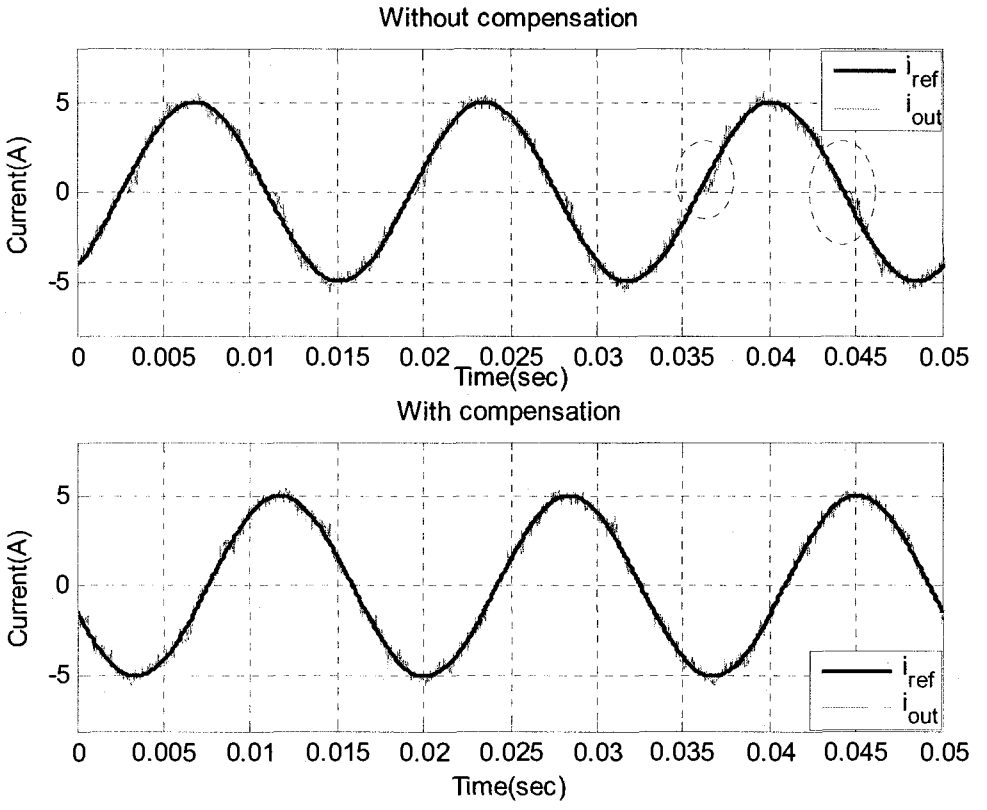
(b)

Fig. 4-13 Performance of the voltage loop controller with estimator.
(a) Steady state response, (b) Transient response for a step change of dc link reference voltage from 48 V to 40 V

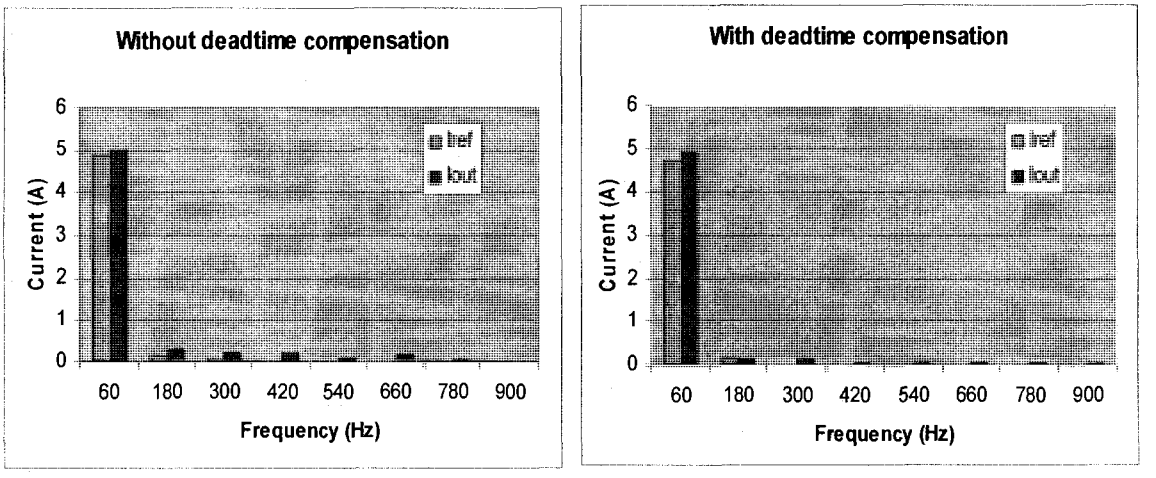
4.4.3 EFFECT OF THE DEAD-TIME AND DC BUS VOLTAGE RIPPLE

Fig. 4-14 presents the waveform of the reference and output current and their associated frequency spectrum to show the effect of the dead-time compensation. The circuit used for verifying the performance of the PR current controller, is used in this part. The THD of the output current is 6.5% without dead-time compensation, while with dead-time compensation it reduces to 2.4%. The distortion due to the dead-time is more severe around the zero crossing. This might occur because the dead-time of the driver circuit causes some pulses of the PWM signal to be too small at those points, making it difficult for the current to build up.

The same circuit used for verifying the performance of the voltage loop controller and dc bus voltage ripple estimator, is used in this part. Fig. 4-15 shows the experimental waveform of the current with and without dc bus voltage feedforward compensation. The third harmonic reduces from 3.1% to 2.6% of the fundamental component when feedforward ripple compensation is used. The improvement in the practical case is smaller than that obtained in the simulation studies. This might be due to sampling (computation) delay between the measurement of dc bus voltage and the execution of the modified modulated signal that is the key operation of the dc bus voltage ripple feedfoward compensation scheme.



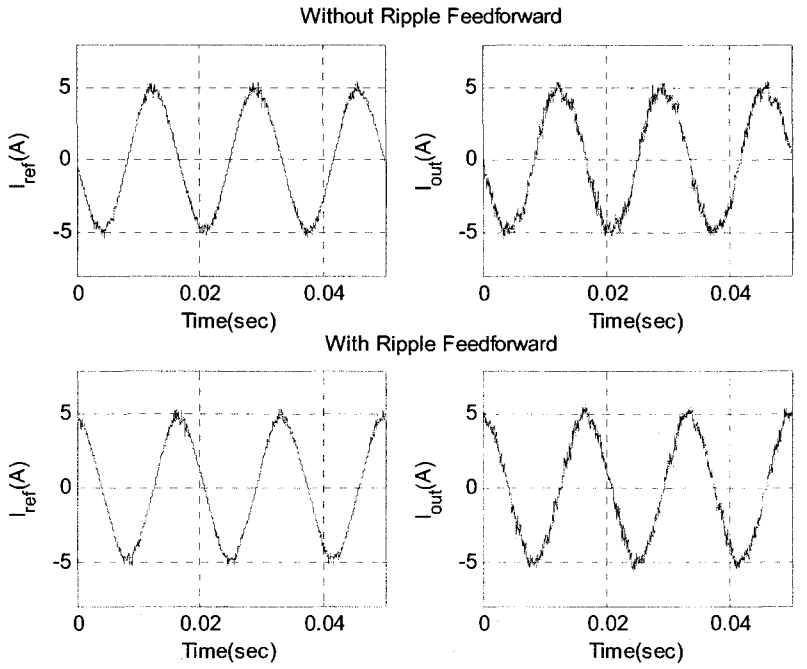
(a)



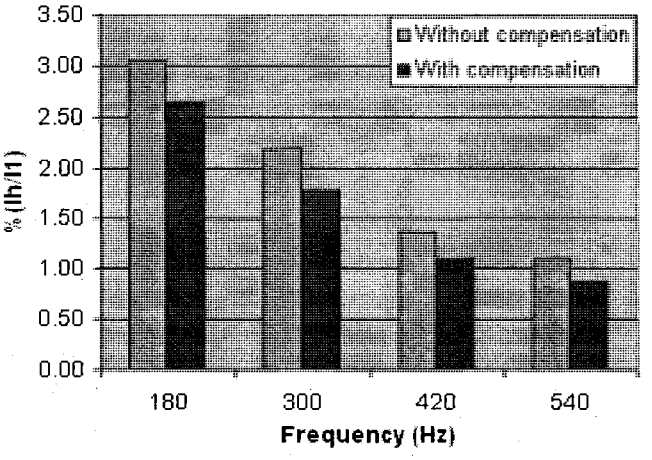
(b)

Fig. 4-14 Effect of dead-time compensation on the output ac current.

(a) Time domain waveform, (b) Frequency spectrum



(a)



(b)

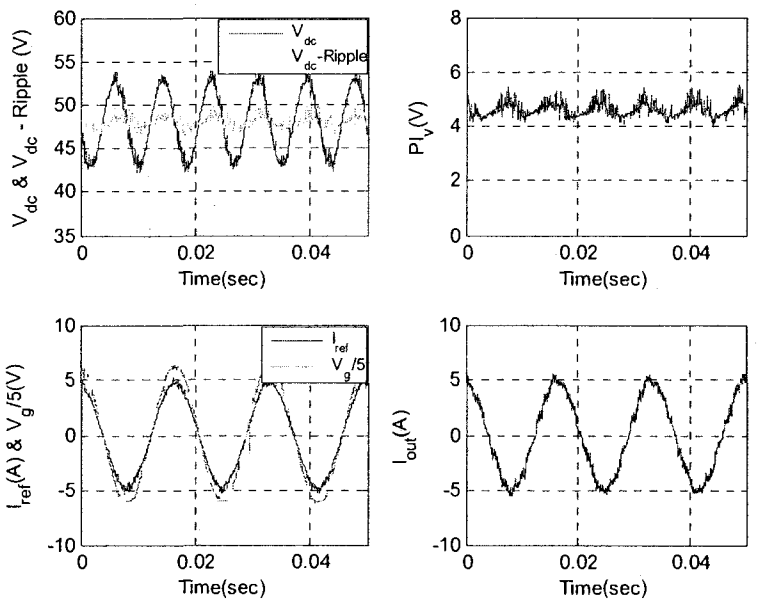
Fig. 4-15 Effect of feedforward ripple compensation on the output ac current. (a) Time domain waveforms, (b) Percentage harmonic components

4.4.4 COMPARISON BETWEEN THE PROPOSED AND THE STANDARD SYSTEMS

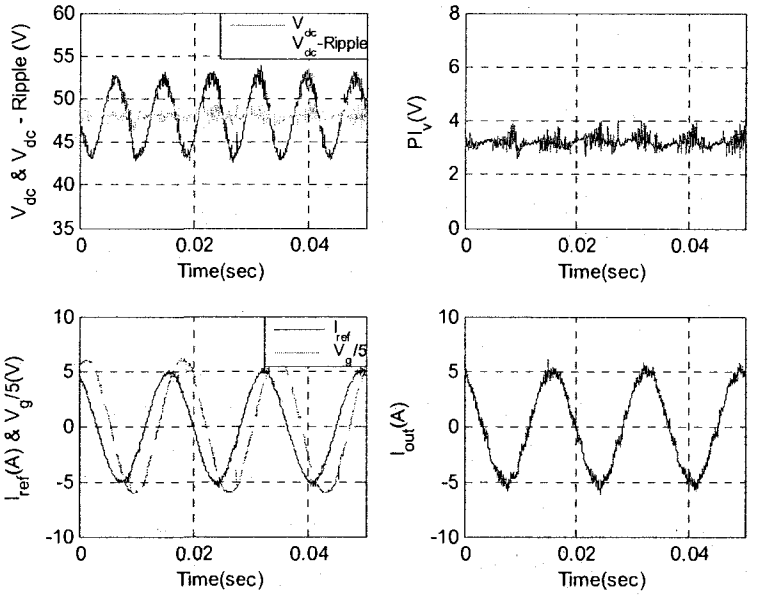
The proposed system with ripple estimator and voltage loop controller designed at a cross-over frequency of 50 Hz is compared with the standard system operating with a large dc capacitor and voltage loop controller designed at low (10 Hz) cross-over frequency. The PR current controller is used for both systems.

4.4.4.1 STEADY STATE

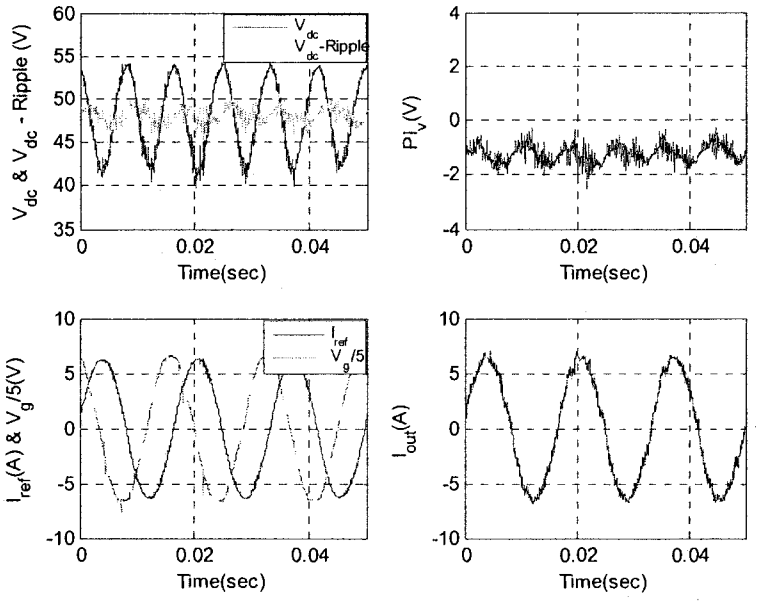
Fig. 4-16 shows some waveforms for the inverter operating with large dc bus voltage ripple and rated apparent power for different values of power factor. The waveforms included in the figures are, dc link voltage (V_{dc}), compensated dc link voltage ($V_{comp} = V_{dc} - Ripple$) for dc link voltage regulation, output of the voltage loop controller (PI_v), reference current (I_{ref}), scaled down grid voltage (V_g) and output current of the inverter (I_{out}). The ripple of the dc bus is estimated and subtracted from the original dc link voltage. The resulting signal V_{comp} is sent to the voltage loop controller for dc bus voltage regulation. Since both V_{comp} and output of voltage controller present low value for the harmonics, so the reference and output current THD are acceptable. When the current supplied from the SAS changes, i.e., the real power changes, then the voltage loop controller output also changes, to provide the appropriate magnitude of the active component of the reference current. When the system operates for only reactive power compensation, then the output of the voltage controller is a negative dc value, indicating that the inverter absorbs real power from the grid to overcome the losses of the inverter and capacitor to regulate the dc bus voltage. Details of the frequency spectrum of the waveforms can be found later in Table 4-1.


V_{dc}
V_{dc}-Ripple
V_{dc} & V_{dc} - Ripple (V)
Time(sec)
PI_v(V)
Time(sec)
I_{ref}
V_g/5
I_{ref}(A) & V_g/5(V)
Time(sec)
I_{out}(A)
Time(sec)

(a)


V_{dc}
V_{dc}-Ripple
V_{dc} & V_{dc} - Ripple (V)
Time(sec)
PI_v(V)
Time(sec)
I_{ref}
V_g/5
I_{ref}(A) & V_g/5(V)
Time(sec)
I_{out}(A)
Time(sec)

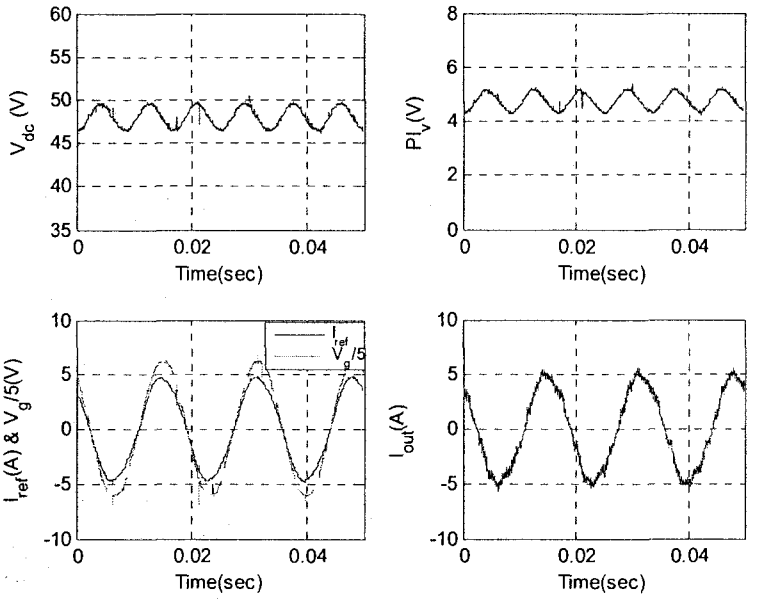
(b)



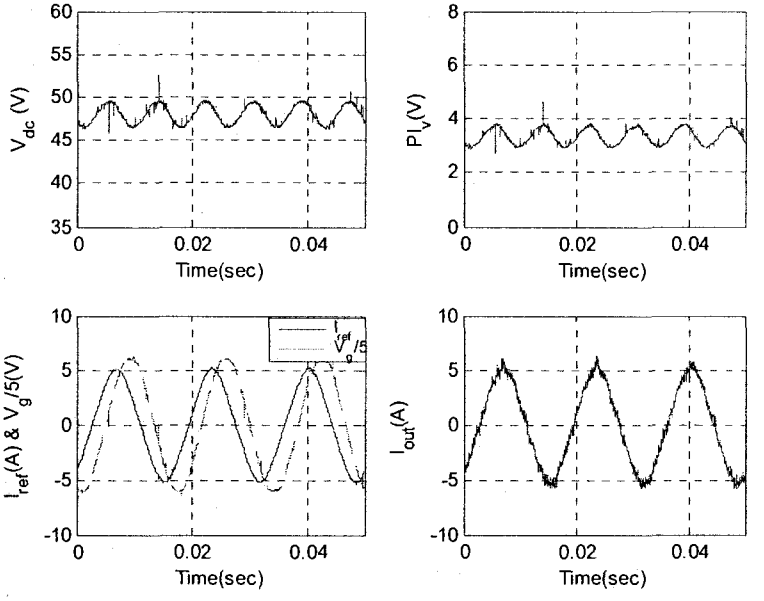
(c)

Fig. 4-16 Waveforms for the inverter operating with large dc bus voltage ripple. (a) P =100 W Q = 0 VAR, (b) P = 80 W Q = 60 VAR, (c) P = 0 W Q = -100 VAR

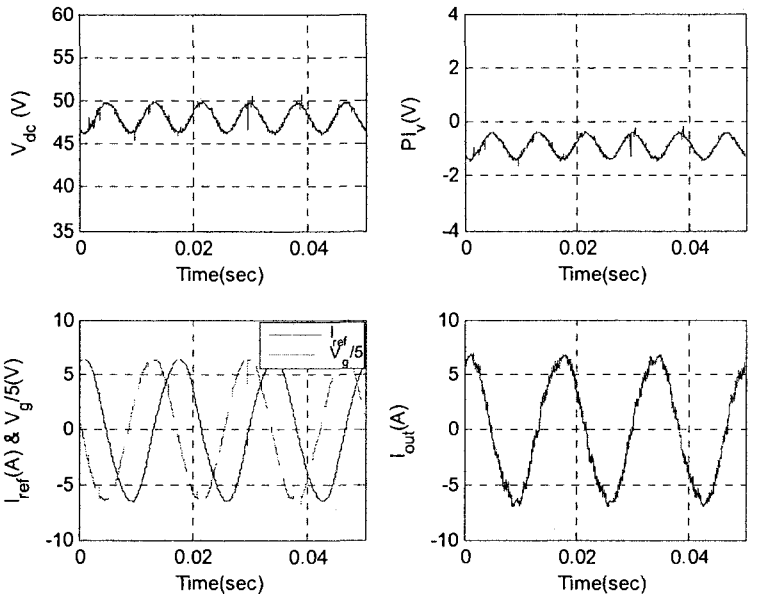
The results for the inverter operating with large dc bus capacitor and small crossover frequency for the dc bus voltage loop with the same operating conditions are presented in Fig. 4-17. The entire control circuit as used for proposed system except the ripple estimator has been used for this purpose. The peak-to-peak value of the ripple in the output voltage of the PI controller is roughly the same for both schemes as shown later in Table 4-1. In case of standard scheme, the 2nd order harmonic at the output of the voltage loop controller is the dominant harmonic component. Therefore the proposed scheme can provide the same steady state performance as the standard one.


V_{dc} (V)
PI_v(V)
I_{ref}(A) & V_g/5(V)
I_{out}(A)
Time(sec)
I_{ref}
V_g/5

(a)


V_{dc} (V)
PI_v(V)
I_{ref}(A) & V_g/5(V)
I_{out}(A)
Time(sec)
I_{ref}
V_g/5

(b)



(c)

Fig. 4-17 Waveforms for the inverter operating with small dc bus voltage ripple. (a) P =100 W Q = 0 VAR, (b) P = 80 W Q = 60 VAR, (c) P = 0 W Q = -100 VAR

The harmonic spectra data of the waveforms for 3 different cases (P = 100 W & Q = 0 VAR, P = 80 W & Q = 60 VAR, and P = 0 W & Q = -100 VAR) are shown in Table 4-1. The percentage odd harmonics and total harmonic distortion for the output current of the proposed system is calculated and it complies with the IEEE standard for distributed generation requirement. The output of the voltage loop controller presents the magnitude of the active component of the current which is multiplied with the sine template to obtain the active component of reference current. Therefore, the larger the 2^{nd} and 4^{th} order component at the output of voltage loop controller, the larger will be the 3^{rd} and 5^{th} order harmonic in the reference current as well as in the output current. When in the standard scheme, the inverter supplies 100 W to the grid, the 2^{nd} and 4^{th} order component at the output of voltage loop controller are 0.41 V and 0.011 V respectively, which results in 0.198 A and 0.013 A of 3^{rd} and 5^{th} harmonics in the reference current. Similarly, for

the proposed scheme, the 2nd and 4th harmonic at the output of voltage loop controller are 0.25 V and 0.01 V respectively which results in smaller 3rd and 5th harmonics in the reference current (0.13 A and 0.014 A respectively).

Table 4-1 Frequency content of the signals for different operating conditions.

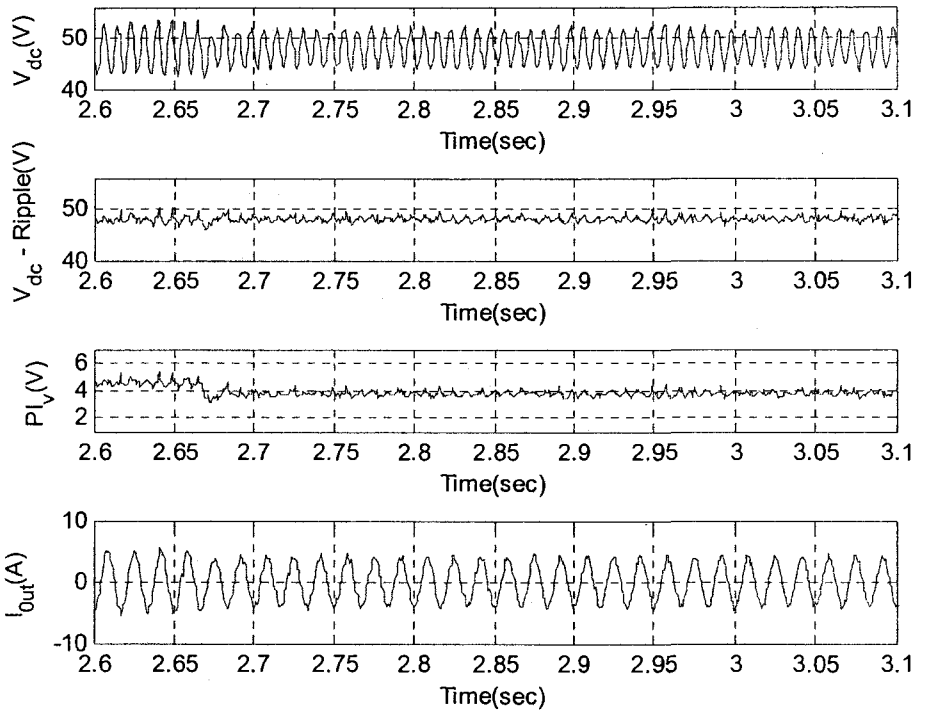
		P = 100 W Q = 0		P = 80 W Q = 60 VAR		P = 0 Q =-100 VAR	
		Large C_{dc}	Small C_{dc}	Large C_{dc}	Small C_{dc}	Large C_{dc}	Small C_{dc}
Dc link Voltage	DC	48	48	48	48	48	48
	120Hz	1.501	4.953	1.45	4.607	1.486	5.82
	240Hz	0.04	0.04	0.046	0.145	0.027	0.162
Output of Voltage Controller	DC	4.736	4.61	3.347	3.209	1.234	1.237
	120Hz	0.41	0.25	0.4	0.117	0.406	0.298
	240Hz	0.011	0.01	0.012	0.05	0.005	0.05
Reference Current	60Hz	4.709	4.7	5.0	4.98	6.45	6.39
	180Hz	0.198	0.13	0.196	0.079	0.208	0.154
	300Hz	0.013	0.014	0.01	0.041	0.002	0.033
	420Hz	0.002	0.004	0.004	0.012	0.003	0.023
	540Hz	0.004	0.01	0.003	0.017	0.004	0.009
Output Current	60Hz	4.914	4.91	5.127	5.09	6.49	6.52
	180Hz	0.228	0.129	0.211	0.071	0.27	0.187
	300Hz	0.102	0.131	0.061	0.129	0.096	0.157
	420Hz	0.06	0.04	0.036	0.078	0.026	0.09
	540Hz	0.057	0.06	0.088	0.04	0.12	0.03
THD of Reference Current	%	4.37	2.82	3.94	1.86	3.24	2.52
THD of Output Current	%	5.75	4.09	4.88	3.46	5.23	4.13

The dominant switching frequency harmonic current was measured with different PF at rated VA and it is always less than 4% of rated fundamental current. It happens because the output filter was designed considering the ideal condition, but in experiment the losses of the system cause the fundamental current to decrease from the rated value, as a result it is little bit more than the theoretical value. Table 4-1 shows that the dc bus

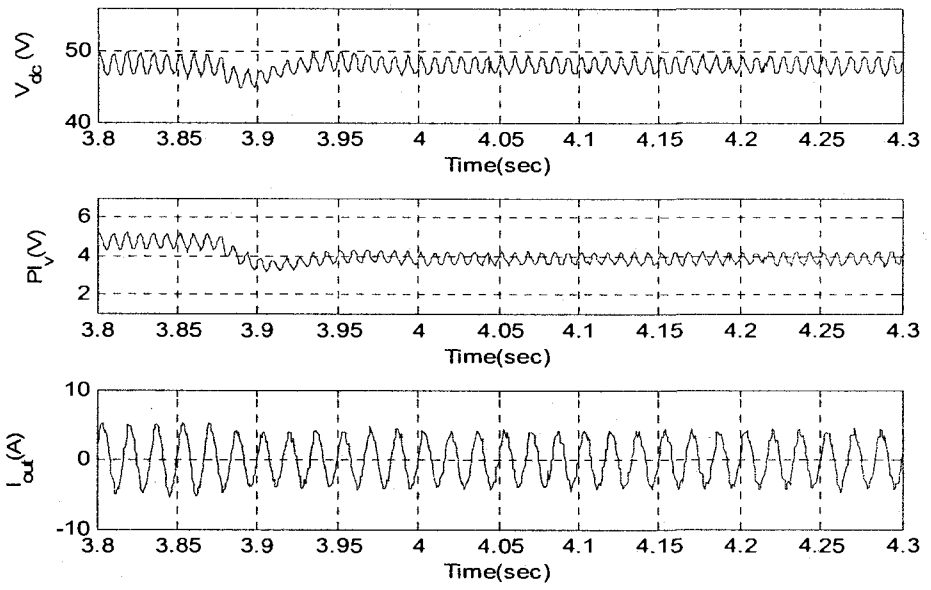
voltage ripple changes with different PF at rated VA. The peak value of 2nd order component value is more for STACOM operation which complies with simulation result.

4.4.4.2 TRANSIENT RESPONSE

The response of the two systems to a step decrease of 20% in the input power (100 W to 80 W while Q = 0 VAR) injected into the dc bus of the inverter is shown in Fig 4-18. The SAS output current changes from 2.083 A to 1.667 A at 2.67 s for the proposed system and at 3.87 s for the standard system in their respective figures. The signal passed to the voltage loop controller for proposed system follows the average value of the dc bus voltage, therefore the proposed system settles down quickly without any undershot. The standard system takes quite a long time to settle down. As the input power from the SAS decreases, the ripple as well as the output dc value of the voltage loop controller decreases. The transient response of the system when operating as a power conditioner is shown in Fig. 4-19. It shows the variation of the dc bus voltage, output of the voltage loop controller and the ac output current of the inverter when the reactive power supplied by the inverter was reduced from 100 VAR to 80 VAR. The transient response of the system with a small capacitor (large ripple) and higher bandwidth is faster than that of the system with large capacitor and lower bandwidth. There was no significant voltage sag (undershoot) in the dc bus of the first unlike in the second one. There is no significant variation in the average value of the dc bus voltage due to variation of the reactive power. As Q reduces, the fundamental component of the ac current and the losses in the inverter reduce as can be seen in the magnitude of the output voltage of the dc bus voltage controller. Finally, dc bus voltage ripple decreases as the magnitude of the reactive component of the output ac current decreases.



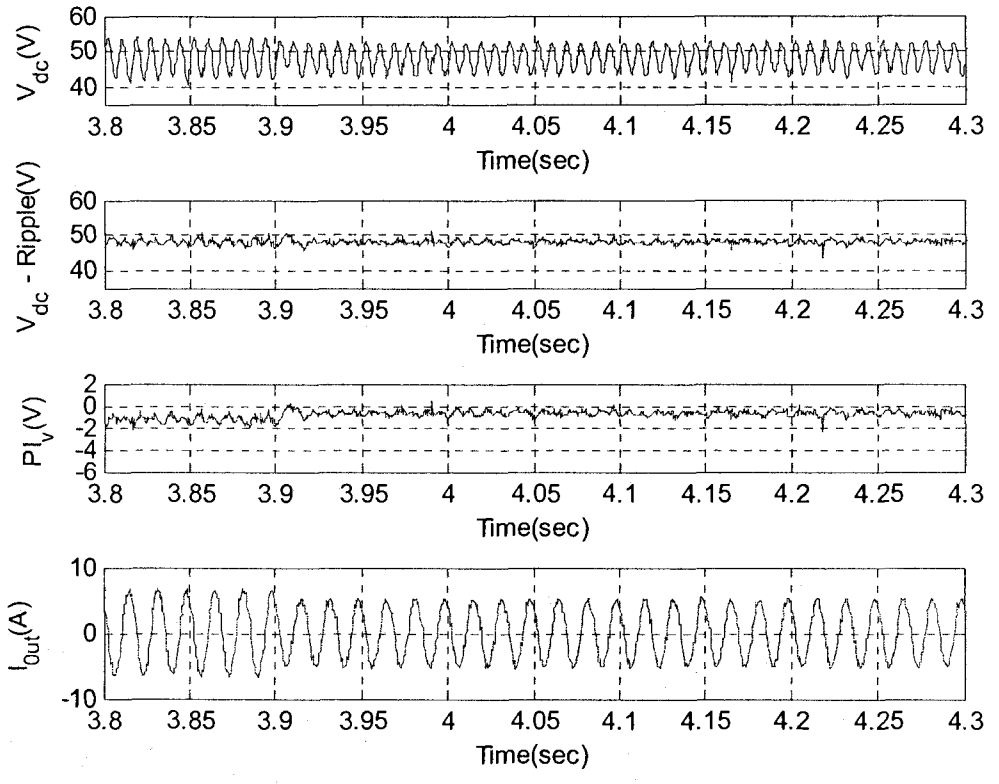
(a)



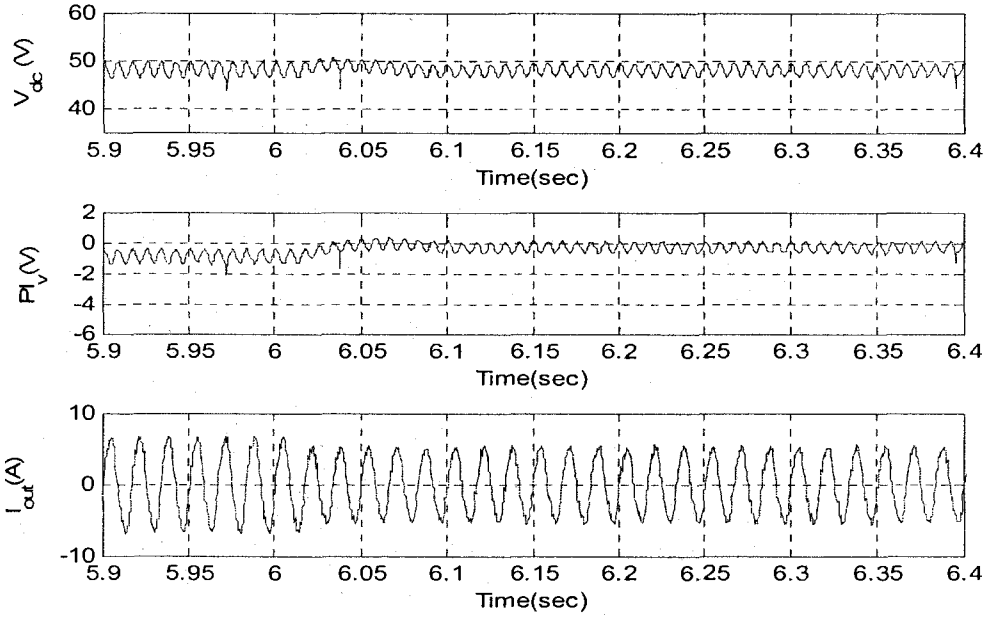
(b)

Fig. 4-18 The response of the inverter system for a step decrease in input power.

(a)Small capacitor system, (b) Large capacitor system



(a)



(b)

Fig. 4-19 The response of the inverter system for a step change in reactive power. (a) Small capacitor system, (b) Large capacitor system

Some additional tests are conducted to verify the performance of the proposed inverter system under transient conditions. In the first case, described by the waveforms shown in Fig. 4-20, the inverter is just connected to the grid. There is no current coming from the SAS and no active power being injected into the grid. The reactive power flow between the inverter and grid is also set at zero. The voltage at the dc bus is regulated at 48 V by the inverter's dc bus voltage control loop. There is virtually no ripple because the active ac current required for compensating the losses in the capacitor and inverter is negligible. The inverter starts supplying 100 W when the SAS starts supplying active power at 1.45 s. The reactive power is still set at 0 VAR. The transient start-up lasts for about 2 ac line cycles.

Fig. 4-21 shows the system's response when the reactive power injected into the grid changes from 0 to 60 VAR at 3.94 s, while it supplies 80 W. The dc bus voltage ripple increases as the total apparent power increases. The output current changes its phase instantaneously following the disturbance. The dc bus average voltage shows a small undershot as it suddenly starts supplying reactive power. The sudden real power turn off from 100 W to 0 W at 2.76 s is shown in Fig. 4-22, while reactive power is set at 0 VAR. The dc bus voltage is regulated at 48 V. Since the losses are negligible so the output of the voltage controller is almost zero. Therefore the output current is also zero.

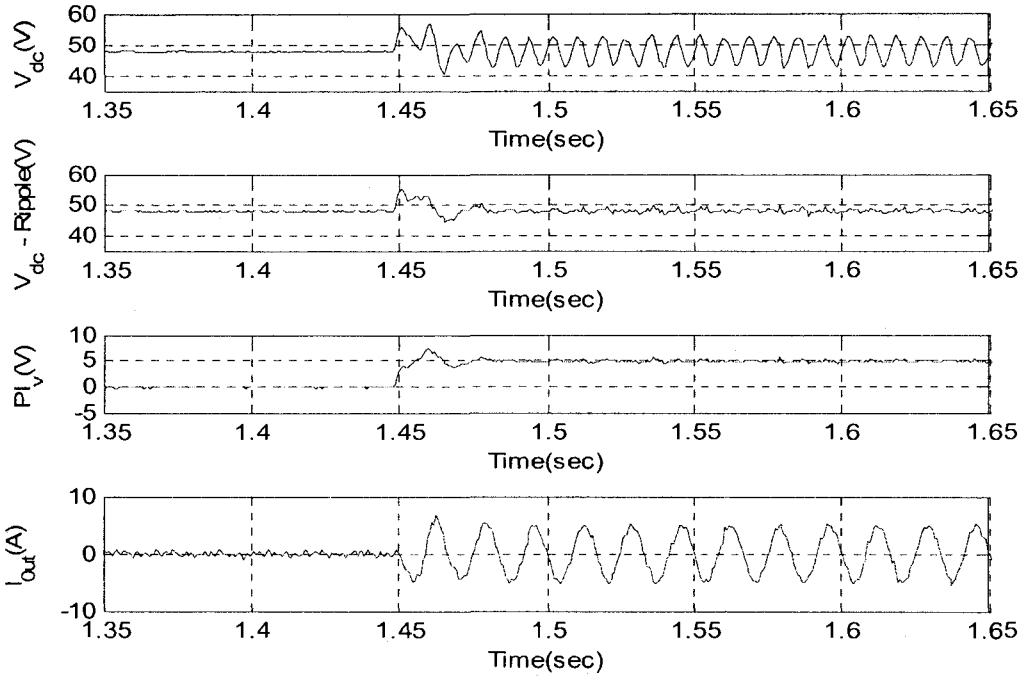


Fig. 4-20 Waveforms showing start-up transient for the PV inverter system

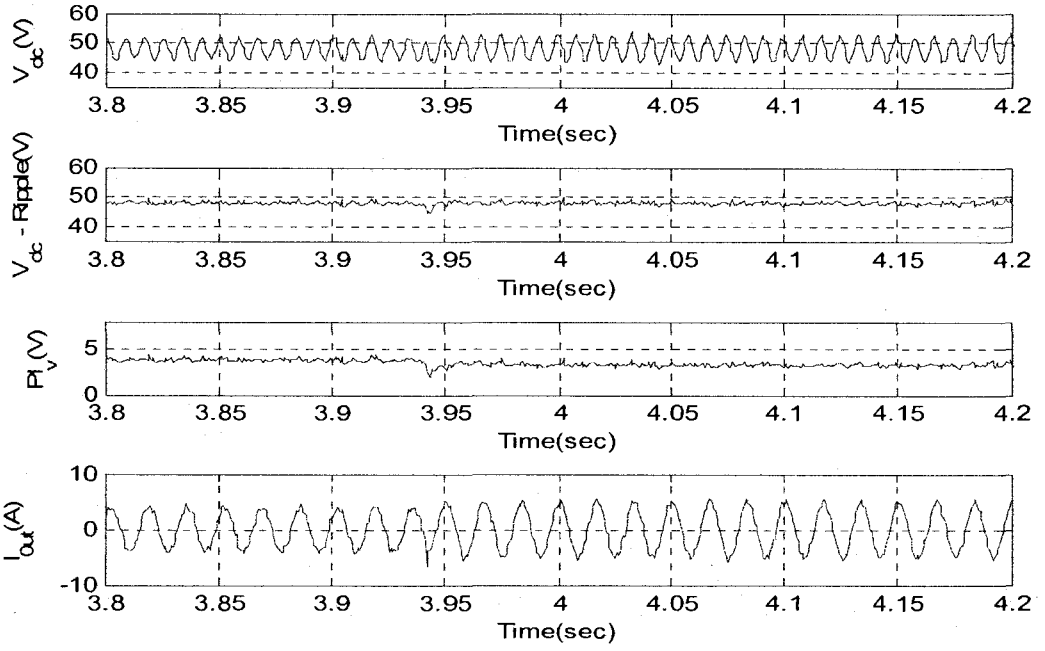


Fig. 4-21 Waveforms showing sudden change of reactive power (real power is the same)

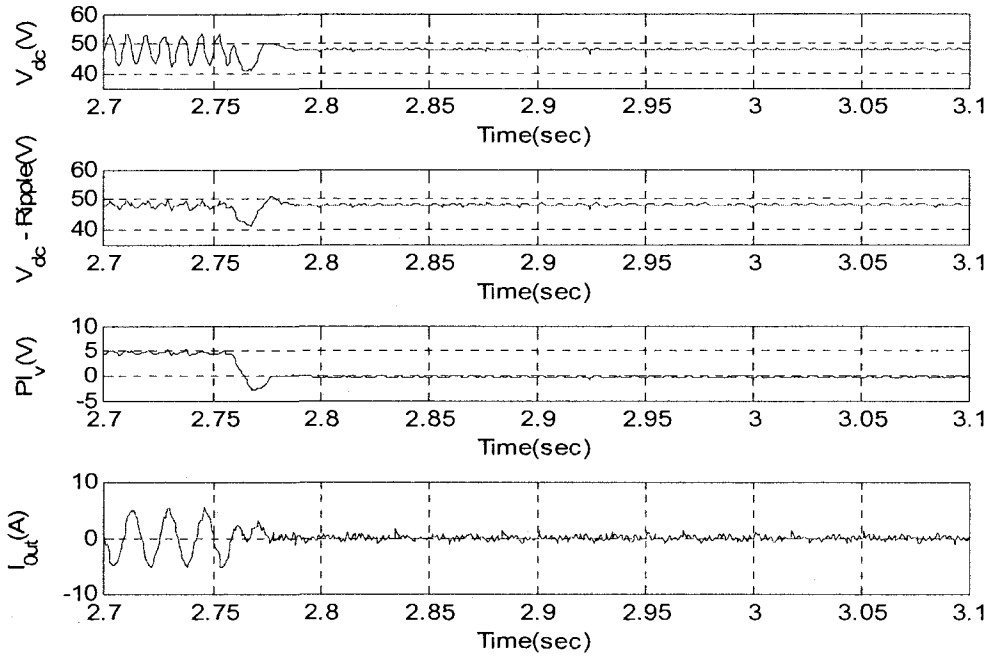


Fig. 4-22 Waveforms showing turn-off transient for the PV inverter system

4.5 CONCLUSION

This Chapter has presented the experimental results to validate the theoretical analysis and simulation results presented in previous Chapters. First, the hardware used to implement the set-up has been described in details. A small-scale laboratory prototype was implemented. The control scheme for the inverter was implemented in a DSP development kit from dSPACE with user interface that allows monitoring and variation of the parameters of the system. It employed the dc bus voltage ripple estimator, dc bus voltage controller, the PLL, output ac current controller, dead-time compensation and feedforward ripple compensation described in previous chapters. The experimental results demonstrate the effectiveness of those circuits. The current controllers (PI with grid voltage feedforward and PR) significantly reduce the steady state error. The dc bus

voltage ripple estimator allowed the use of a larger crossover frequency for the dc bus voltage control loop while reducing the low order harmonic distortion in the reference current. In this way, the transient response of the dc bus voltage loop is faster. It was shown that the variation of the reactive power injected or absorbed by the inverter causes a small transient in the dc bus voltage than a similar variation in the active power supplied by the solar array simulator. Star-up and shut-down tests were also conducted successfully.

CHAPTER 5
CONCLUSION

5.1 SUMMARY

The Thesis describes a control strategy for the inverter of a dual power stage single-phase grid interface for distributed power generation units, suitable for operation with a large intermediate dc bus voltage ripple. In such a case, one can use a small, non-electrolytic capacitor for increased reliability. The main objective of the grid-connected inverter is to transfer active power into the ac side. With an adequate control scheme, the inverter can also provide and absorb reactive power for power factor compensation and ac bus voltage regulation, what adds value to the DG unit.

The dual power stage scheme allows a good degree of decoupling between the 2^{nd} order current harmonic that appears at the dc bus of the inverter and the current in the DG source that is in the input of the dc-dc converter. This facilitates the implementation of maximum power point tracking algorithms for photovoltaic arrays. The inverter is controlled to behave as a current source, presenting an inner current loop and an outer voltage loop for the regulation of the dc bus voltage. The output of the voltage loop controller is the peak value of the reference active current of the current loop and should be ideally a dc signal, with no ripple, to create a sinusoidal reference current. This is hard to achieve when the voltage to be controlled presents a large low frequency ripple. The alternative sought in this Thesis was the use of a dc bus voltage estimator that can minimize the magnitude of the low frequency harmonics at the input of the voltage

controller which then can be designed to have a higher bandwidth for faster transient responses. This has been done before, but not for an inverter that can operate with variable power factor, from unity to zero (reactive power compensator). It was found that the ESR of the dc bus capacitor and the flow of ripple current in the output branch of the dc-dc converter can decrease somewhat the accuracy of the ripple estimator. However, it was still possible to obtain a reference current that is less distorted than that of a conventional large dc capacitor and a small (10 Hz) bandwidth for the voltage loop.

The ripple of the dc link also appears as a time varying envelope in the inverter output voltage waveform and it introduces low order voltage harmonics. Its impact on the output current distortion for the inverter operating in closed loop is relatively small, but it was further reduced using a dc bus voltage ripple feedforward approach. For low voltage application, the relatively large dead-time of the SKHI22IGBT driver affected the output current distortion significantly, requiring a dead-time compensation logic for meeting the stringent THD requirements of the international standard for distributed generation.

Regarding the current control loop, both current controllers (PI current controller with grid voltage feedforward and PR current controller) exhibits almost the same performance for typical design specifications. Steady state error exists for PI current controller. The feedforward of grid voltage minimizes this error significantly, but cannot make it zero, because of the limited gain at concerned (grid) frequency. The PR controller eliminates this problem due to its inherent high gain at the resonant frequency that is selected as the grid frequency.

The performance of the proposed system was compared to that of a standard grid interface operating with a small dc bus voltage ripple and a low bandwidth for the voltage

loop. Simulation was carried out for both systems in PSIM®. The effectiveness of the compensation circuits, voltage ripple estimator, current controllers (PI with grid voltage feedforward and PR) and the dc bus voltage control loop were verified by simulation. The low order harmonic content in the steady state and percentage overshot/undershot or settling time in transient were used as performance index for the two systems. The use of a voltage ripple estimator in the proposed system ensures lower value for individual harmonics and total harmonic distortion of the output current compared to the standard scheme. The compensated signal sent for dc bus voltage regulation presents very low value of harmonics and follows the average value of the dc bus voltage in the transient, and settles down to the steady state value within 1.5 cycles.

Finally a laboratory prototype was built to validate the simulation results. The control circuit for the inverter was implemented with a digital signal processing kit. The details of the experimental setup and experimental procedure have been discussed. A number of tests that demonstrate the superior performance of the proposed system under steady state and transient conditions have been presented.

5.2 SUGGESTIONS FOR FUTURE WORK

(1) Develop a modified version of the dc bus voltage ripple estimator to incorporate harmonic compensation of the local load, i.e., active power filter application.

(2) Determining a harmonic transfer function model of the entire system that can mathematically present the interactions of the harmonics of the dc bus and grid.

(3) Design of a control loop for the regulation of the magnitude of the ac voltage at the point of common coupling of the DG grid interface.

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APPENDIX

A-1. DC-DC BOOST CONVERTER ACTING AS CURRENT SOURCE

This appendix deals with the verification by simulation of the impact of having a dc-dc converter operating with input current control, as for systems with maximum power point tracking (MPPT), on the current injected in the dc bus of the single-phase grid interface discussed in the main body of the thesis. A small signal model is derived for the dc-dc converter to allow the design of the current controller. Then, simulation results are presented for the complete system (dc-dc converter + inverter) operating at rated power.

Fig. A1-1 shows the circuit diagram of a boost converter with average input current control using PWM. The PV panel in the input of the converter is modeled by a dc source for the sake of simplicity. There one sees that the input inductor current of the boost is compared with the reference current. The reference current can come from an MPPT algorithm for a PV panel. The error signal generated from the comparator passes through a linear controller which gives the required control (modulating) signal for the PWM modulator that produces the gating signal for the switch of the boost converter. The small signal model of the converter is derived assuming operation in the continuous conduction mode (CCM), with rated power delivered to a resistive load as follows.

When the switch (S) is 'on',

$$v_{in} = v_L \quad \text{and} \quad i_C + i_R = 0 \tag{A-1}$$

$$dv_{in} = dv_L \quad \text{and} \quad d\,i_C + di_R = 0 \tag{A-2}$$

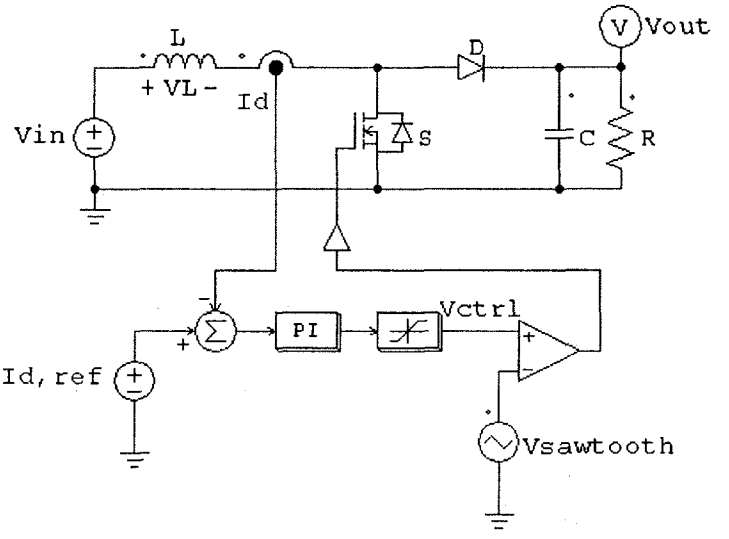


Fig. A1-1 Circuit diagram of boost converter with average current mode control

Where, v_{in}, v_L, i_C and i_R are the input voltage, inductor voltage, capacitor current and the load resistance current respectively. d is the duty cycle of the switch.

Similarly, when the switch is 'off',

$$v_{in} = v_L + v_{out} \quad \text{and} \quad i_C + i_R = i_L \tag{A-3}$$

$$(1-d)v_{in} = (1-d)v_L + (1-d)v_{out} \quad \text{and} \quad (1-d)i_C + (1-d)i_R = (1-d)i_L \tag{A-4}$$

Where v_{out} and i_L are the output voltage and inductor current respectively.

Therefore,

$$v_{in} = v_L + (1-d)v_{out} \quad \text{and} \quad i_C + i_R = di_L \tag{A-5}$$

$$v_{in} = L\frac{di_L}{dt} + (1-d)v_{out} \quad \text{and} \quad C\frac{dv_{out}}{dt} + \frac{v_{out}}{R} = di_L \tag{A-6}$$

Applying small variation around the operating point,

$$v_{in} = V_{in}, \quad i_L = I_L + \tilde{i}_L, \quad v_{out} = V_{out} + \tilde{v}_{out}, \quad d = D + \tilde{d} \tag{A-7}$$

So,

$$V_{in} = L\frac{d\left(I_L + \tilde{i}_L\right)}{dt} + \left(1 - D - \tilde{d}\right)\left(V_{out} + \tilde{v}_{out}\right) \tag{A-8}$$

Neglecting the steady state value and the product of two small variation,

$$0 = L\frac{d\tilde{i}_L}{dt} + \tilde{v}_{out} - D\tilde{v}_{out} - \tilde{d}V_{out} \tag{A-9}$$

Therefore, in Laplace domain,

$$sLI_L(s) + V_{out}(s)(1-D) - D(s)V_{out} = 0$$

$$V_{out}(s) = \frac{1}{(1-D)}\left[D(s)V_{out} - sLI_L(s)\right] \tag{A-10}$$

Again, considering the current equation of A-6 and applying small variation,

$$(1 - D - \tilde{d})(I_L + \tilde{i}_L) = C\frac{d\left(V_{out} + \tilde{v}_{out}\right)}{dt} + \frac{V_{out} + \tilde{v}_{out}}{R}$$

Following the same procedure as stated above,

$$I_L(s)\left(1-D\right) - D(s)I_L = \left(sC + \frac{1}{R}\right)V_{out}(s) \tag{A-11}$$

Therefore, from equation A-10 and equation A-11, the relationship between duty cycle and inductor current can be given as,

$$\frac{I_L(s)}{D(s)} = \frac{\left(1-D\right)I_L + \frac{V_o}{R} + sCV_{out}}{R\left(1-D\right)^2 + s^2LC + s\frac{L}{R}} \tag{A-12}$$

If V_{ctrl} and $\hat{V}_{ST}$ are the control voltage and peak value of sawtooth carrier respectively, then, $D = {V_{ctrl}}/{\hat{V}_{ST}}$.

Since $\frac{V_{out}}{R} = I_R = (1-D)I_L$, the transfer function describing the relationship between control voltage and inductor current is given as,

$$\frac{I_L(s)}{V_{ctrl}(s)} = \frac{1}{\hat{V}_{ST}}\left[\frac{2(1-D)I_L + sCV_{out}}{(1-D)^2 + s^2LC + s\frac{L}{R}}\right] \tag{A-13}$$

The power supplied by the PV array (input voltage source) is assumed constant (100W). The input and output voltages of the converter are 24 V and 48 V respectively. The inductor and capacitor are designed considering the allowable high frequency ripple in the input current (3%) and the output voltage (1%) respectively. The main parameter values for the converter are provided in Table A1-1.

Table A1-1 Parameters of the boost converter

Rated power	100 W
Input Voltage	24 V
Output Voltage	48 V
Nominal duty cycle	0.5
Input Current	4.17 A
Output Current	2.083 A
Inductor	1 mH
Capacitor	5 μF
Equivalent Output Load	23.04 Ω
Switching frequency	100 kHz
Peak value of carrier	10 V

The bode plot of the uncompensated current loop as given by A-13 is obtained as shown in Fig. A1-2.

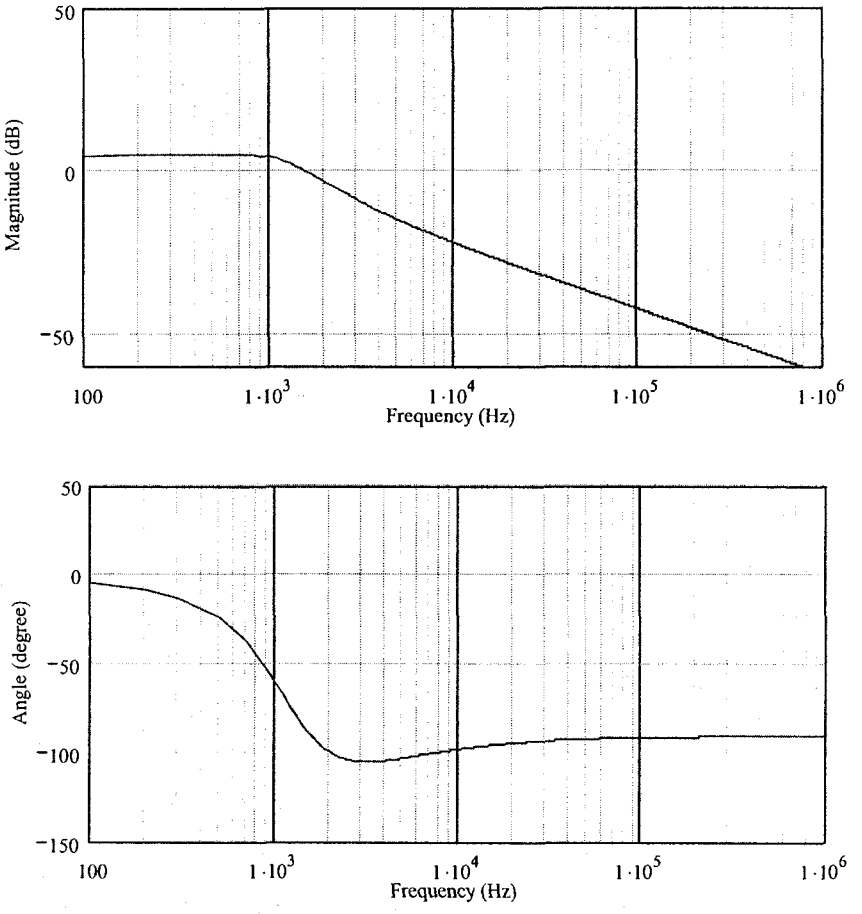


Fig. A1-2 Bode plot of the uncompensated current loop

At the desired cross-over frequency (10 kHz), the system provides a gain of -21.993 dB and an angle of -97.48 degree. A PI type-2 controller is designed for a PM of 55 degree. Fig. A1-3 shows the bode plot of the compensated loop transfer function and the controller. The transfer function of the controller is given by,

$$G_c(s) = \frac{K_{PI}(1+s\tau)}{s\tau(1+sT_P)} = \frac{12.579\left(1+6.5\times10^{-5}s\right)}{6.5\times10^{-5}s\left(1+3.897\times10^{-6}s\right)}$$

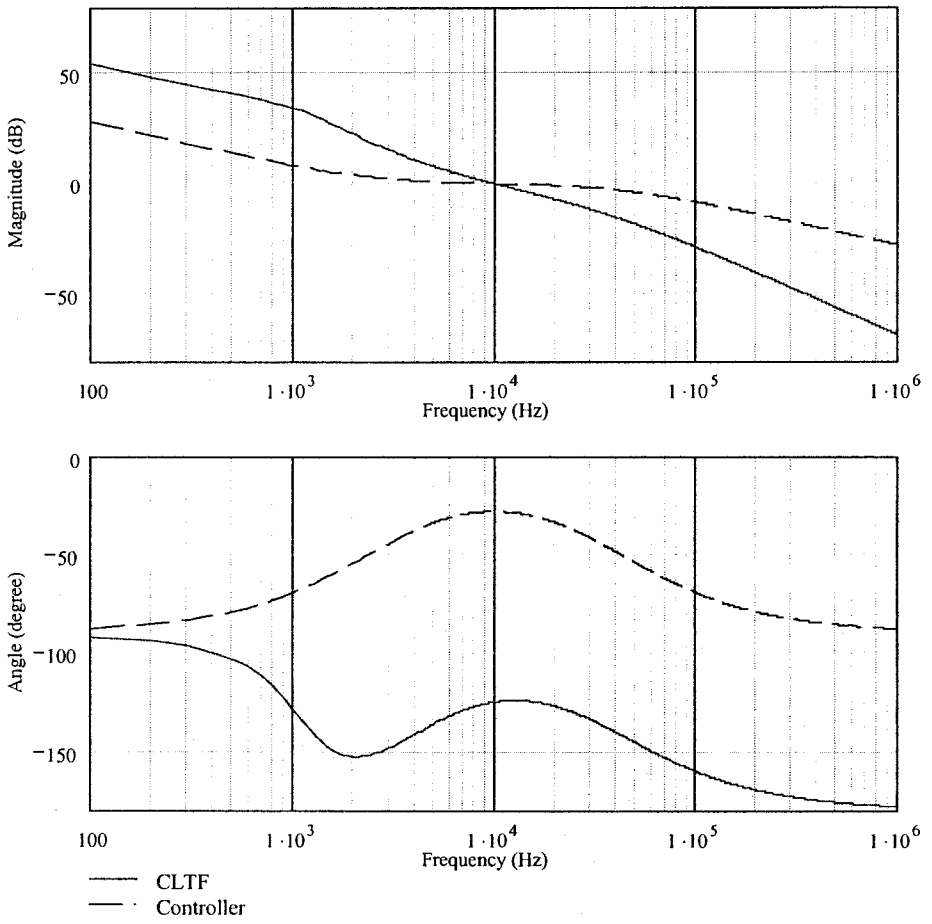


Fig. A1-3 Bode plot of the compensated current loop and controller

To verify the operation of the two cascaded converters, the resistive load of the boost converter is removed and it is connected to the dc bus of the inverter through a small inductor (0.5 mH) is used. The power circuit used for simulation is shown in Fig. A1-4.

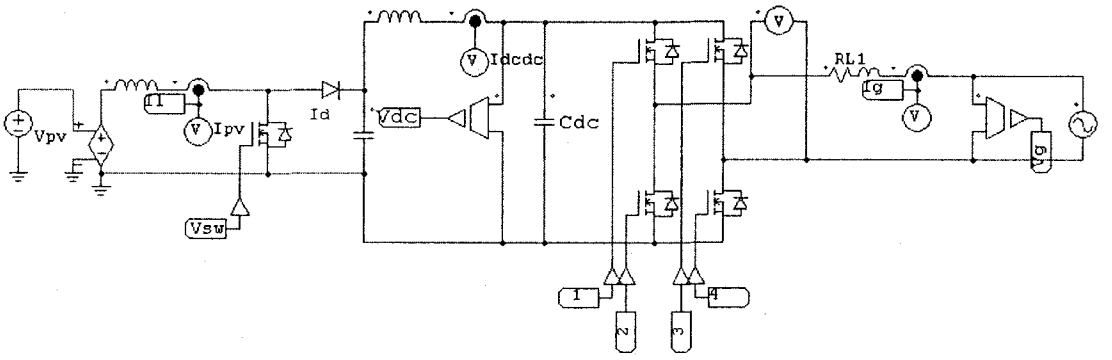
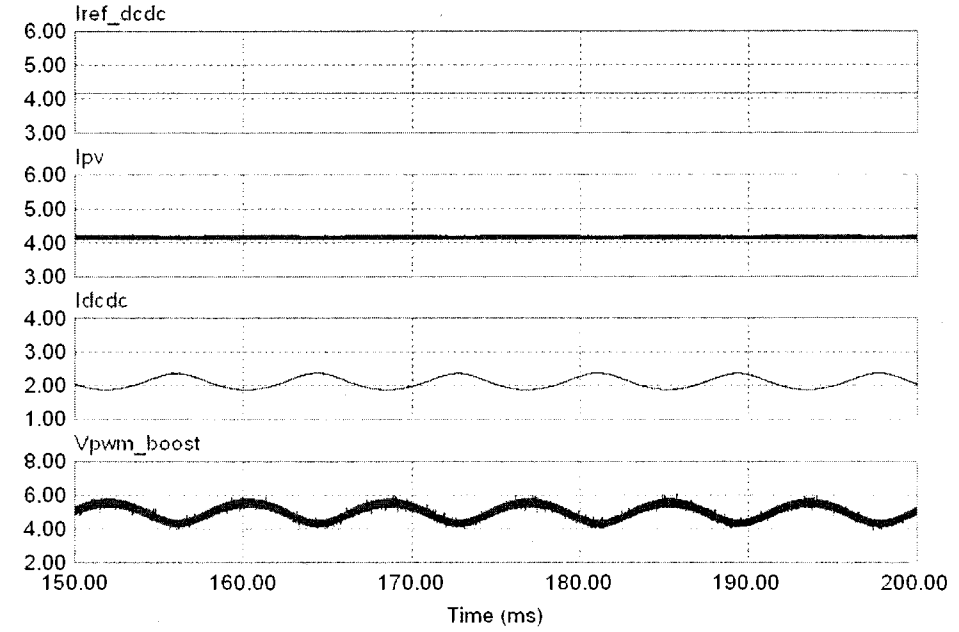
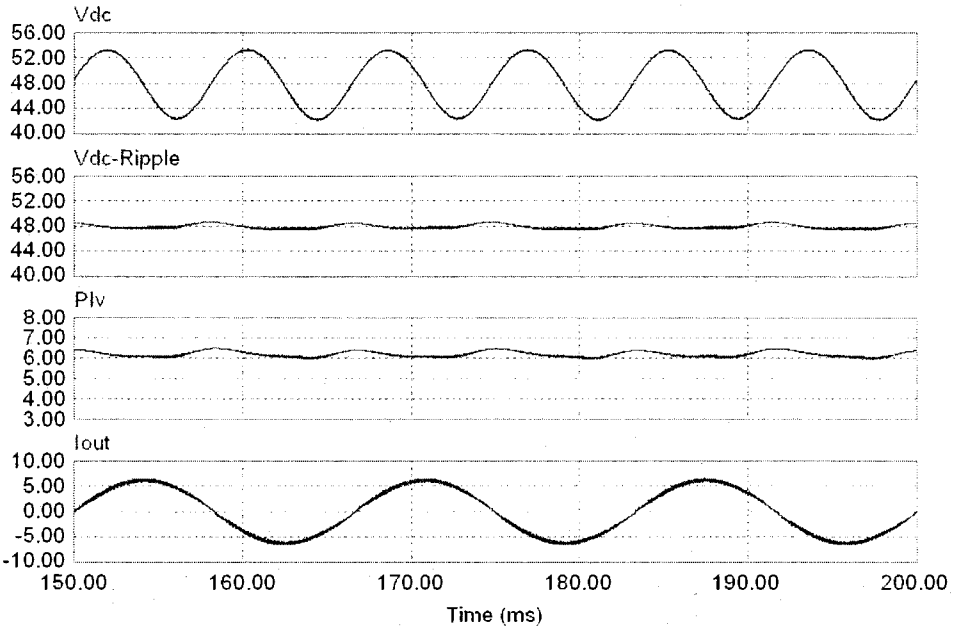


Fig. A1-4 Power circuit of the PV inverter supplied from a boost converter

Fig. A1-5(a) shows the main waveforms of the boost converter. The reference current is 4.167 A and the current extracted from the source is the same and it does not present any 2nd order component in the input (PV) current. The control voltage of the boost varies with a 120 Hz component around the nominal dc value to regulate the input current, due to the ripple present in the dc bus of the inverter. The average value of the output dc current from the boost is 2.083 A but one clearly see the presence of a 2nd order component. This can have an impact on the accuracy of the ripple estimator that assumed that all 2nd order current harmonic at the dc side of the inverter would flow through the capacitor. Fig. A1-5(b) shows the main waveforms of the inverter. The dc bus voltage is regulated at 48 V with a large 2nd order ripple. The estimated ripple is subtracted from the original dc bus voltage and passed through the controller for dc bus voltage regulation. The output of the voltage loop controller presents almost a pure dc signal for reference current generation. This shows that the impact of the 2nd order harmonic that flows through the output branch of the dc-dc converter on the accuracy of the ripple estimator can be neglected and that the low frequency distortion in the ac side current of the inverter is very small.



(a)



(b)

Fig. A1-5 Waveforms of the entire system. (a) Boost converter, (b) Inverter

A-2. ELECTRONIC CIRCUIT FOR THE GATING SIGNALS OF VSI