MODELING, DESIGN, AND IMPLEMENTATION OF A NOVEL BATTERY CELL EQUALIZER FOR ELECTRIC, HYBRID ELECTRIC, AND PLUG-IN HYBRID ELECTRIC VEHICLES

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ABSTRACT

Modeling, Design, and Implementation of a Novel Battery Cell Equalizer for Electric, Hybrid Electric, and Plug-In Hybrid Electric Vehicles

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In order to meet the stringent cost targets for electric, hybrid electric, and plug-in hybrid electric vehicles (EVs, HEVs and PHEVs), a serious improvement in battery cycle-life and safety is undoubtedly essential. More recently, lithium batteries, in the form of lithium-ion, lithium-polymer or lithium iron phosphate have been profoundly explored. Despite critical research initiatives, lithium-based batteries have not yet been able to meet the steep energy demands, long lifetime and low cost, unique to vehicular propulsion applications. One of the most practical techniques of improving overall performance is to use suitable power electronics intensive cell voltage equalizers in conjunction with on-board energy storage devices. There have been some interesting developments in this area during the last few years, but cost constraints and high current specifications have prevented the complete deployment of this versatile technology. The purpose of this thesis is to introduce a novel configuration for a cell voltage equalizer, with the potential of fulfilling the expectations of low cost, high current-capability, and high efficiency.

This thesis consists of six parts: the first part deals with an introduction to the battery problems in electric vehicle applications; the second part deals with a review of the available popular cell equalizer configurations; the third part deals with an economic and feasibility analyses of battery cell equalizers. Thereafter, a detailed analysis of the

proposed novel battery cell equalizer configuration is presented, comparing the theoretical models, modeling and simulation results, and prototype measurements. A separate chapter is discusses from the point of view of power electronic converter control, considering practical issues. Finally, the thesis discusses the major motivating inferences drawn from this work, and suggests possible future directions and trends, based on those conclusions.

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Last, but not least, the author would like to extend his sincere gratitude to his wife, Silvia Campo. Without her steady support and encouragement, the author would not be able to accomplish his project.

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LIST OF ACRONYMS

ADVISOR	Advanced Vehicle Simulator
Ah	Ampere-Hour
EOL	End of Life
ESS	Energy Storage System
EV	(All) Electric Vehicle
HEV	Hybrid Electric Vehicle
ICE	Internal Combustion Engine
Kg	Kilo-gram
L	Liter
Li-Ion	Lithium-ion
$LiFePO_4$	Lithium iron phosphate
mΩ	Milli-Ohm
NiMH	Nickel Metal Hydride
PHEV	Plug-in Hybrid Electric Vehicle
PI	Proportional Integrative
PPT	Peak Power Tracking
SOC	State of Charge
SOH	State of Health
σ	Statistic Dispersion
UDDS	Urban Dynamometer Driving Schedule
UPS	Uninterruptible Power Supply
V	Volt

V_{OC}	Open Circuit Voltage
W	Watt
Wh	Watt-hour

LIST OF PRINCIPAL SYMBOLS

A, B	Linearization constants
C	Capacitance (Farad) – Capacity (Ah or Wh)
C_2	Cell slow dynamic equivalent capacitance, due to error in V_{OC} estimation
C_a	Cell fast dynamic equivalent capacitance
C_b	Cell slow dynamic equivalent capacitance
dt_n	Differential time, per MOSFET number
DT	Dead time
Err	Error signal, to fed the control
I_{Bat}	Total battery pack current
I_{Cn}, IB_x	Cell current
I_{Eqn}	Cell equalizing current
IL_n	Inductor current
k_t	Cell related factor
K_I	Integration factor
K_P	Proportional factor
n	DC/DC converter ratio
N	Amount of cells in series
R_2	Cell slow dynamic internal resistance, due to error in V_{OC} estimation
R_a	Cell fast dynamic internal resistance
R_b	Cell slow dynamic internal resistance
R_{ds}, R_{dsOn}	Resistance from drain to source, on-state (in MOSFETs)
R, R_{int}	Cell steady state internal resistance

RL_n	Inductor equivalent internal resistance
t	Time
T	Total period time
T_n	Time at n seconds from event current step
T_a , T_b	Time constants a and b
T_s	Sampling time
τ	Duty cycle
Vb_n	Cell voltage
V_t	Total battery pack voltage

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

There is little doubt that the current oil based economy is not sustainable. Even considering the drop in oil prices after Sept. 2008, the average gas price at pumps has risen at an average of 15% per year, in the last 5 years [1]. This trend is depicted in Fig 1-1. There is no reason to think that this tendency will change, even when the most recent world recession (2008-2009), has dampened the consumption, as depicted in Fig 1-3. Political instabilities in producer countries and growing demand in developing countries, as shown in Fig 1-2, have added to the growing world population. This will further worsen the overall economic dilemma.

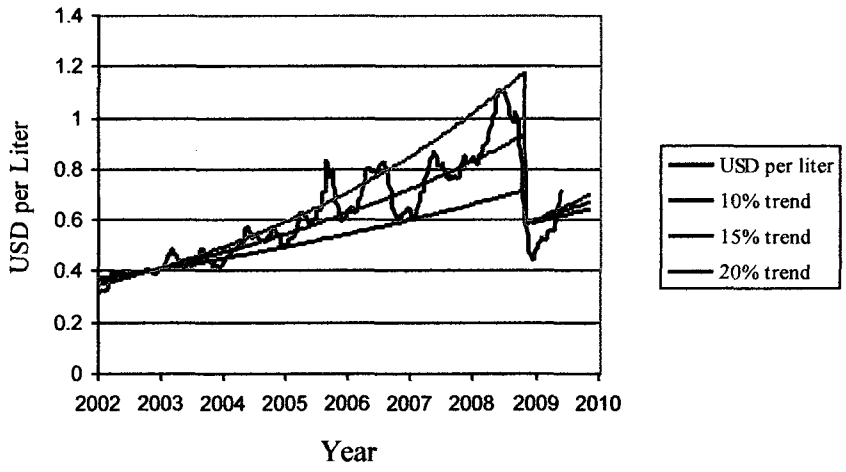


Fig. 1-1 Gas pump price (weekly average), in U.S., all formulations [1].

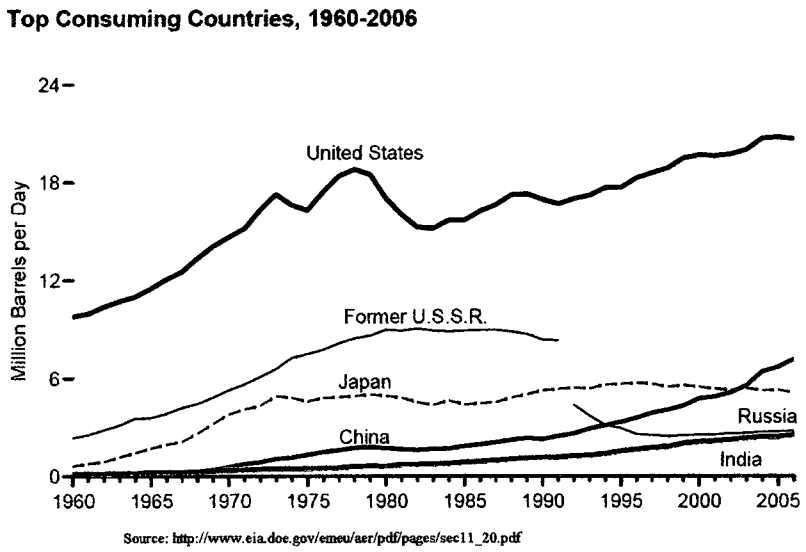


Fig. 1-2 Oil consumption per country (1960-2006), top consuming countries [2].

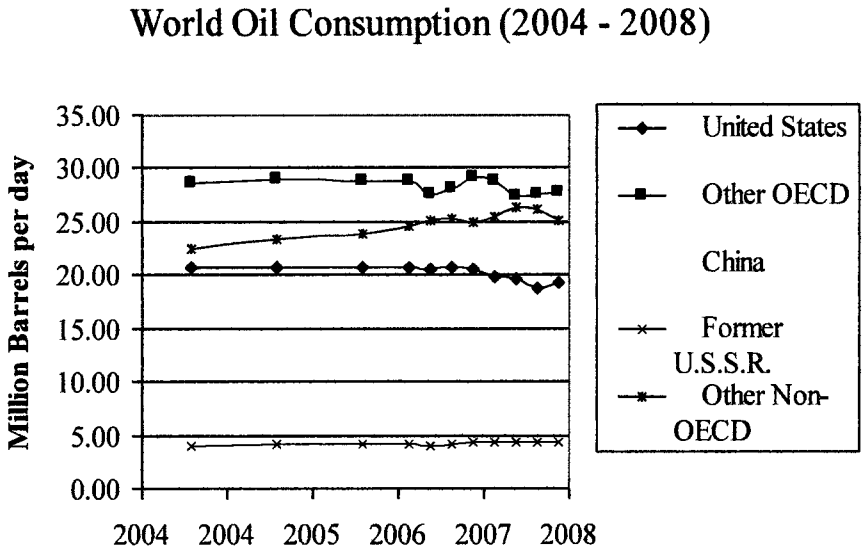


Fig. 1-3 Oil consumption per economic group (2004-1008) [3].

Given the fact that ground transportation represents two thirds of the total oil consumption [4], any alternative to current oil based ICE vehicles will dramatically reduce oil consumption, reserving it to certain uses, where oil is more difficult to replace, such as the petro-chemical industry. The most practical approach to reduce oil

consumption in ground transportation today lies in hybrid electric, plug-in hybrid electric, and all-electric vehicles (HEV, PHEV, and EV).

This thesis will focus on the energy storage issues of PHEVs and EVs, in an effort to make them easy to manufacture and commercialize.

1.2 Energy Storage Issues of PHEVs and EVs

It is well-known today that batteries are indeed the main stumbling block to driving electric vehicles. In fact, the common issues related to lithium rechargeable cells can be summed up by one simple topic: cell equalization. Typically, a battery of a HEV consists of a long string of cells (typically 100 cells, providing a total of about 360 Volts), where each cell is not exactly equal to the others, in terms of capacity and internal resistance, because of normal dispersion during manufacturing. However, the most viable solution for this problem might not originate from mere changes in battery properties. The aim of this chapter is, firstly, to explain the role of power electronics based battery cell voltage equalizers and their role in improving cycle life, calendar life, power, and overall safety of EV/HEV battery energy storage systems.

It is imperative that most studies related to energy storage systems (ESS) for HEV applications must follow a cost-conscious approach. For instance, taking into account that typical lithium batteries cost about $500/kWh [5] (or $250/kWh [6]-[7], if manufactured in high volumes), a typical 16 kWh battery, which provides about 80 km (50 miles) autonomy to a small vehicle (simulated and tested under the Federal Test Procedure, FTP driving pattern). This amounts to a surcharge of about $5,000 over the price of a standard vehicle, exceeding the reasonable budget for an medium consumer.

Moreover, issues related to cycle life and the calendar life issues cannot be ignored. Depending on the intensity of usage, an average cobalt or manganese cathode Li-Ion battery holds about 500 cycles of 80% the capacity, before losing 20% of its initial capacity [1]. If the battery is replaced at that point and the cost of electricity is added, the expenses rise to $0.1/km. Consequently, the existing scheme makes the EV option more expensive than the traditional gasoline based vehicle. Considering newer batteries based on lithium iron phosphate ($LiFePO_4$) chemistries, these numbers are slightly better, withstanding 1000 cycles on current technology, and expecting (but still not proven) 6000-7000 cycles for future PHEV applications. On the other hand, the $LiFePO_4$ chemistry depicts slightly lower energy density (100 Wh/kg) [8]-[9]. Although $LiFePO_4$ seems to be the best fit for EVs, the long term cycle life and volume costs have to be considered seriously. As a reference, current price per unit of $LiFePO_4$ ranges from $1.90-$2.40/Wh, compared to $0.86/Wh, for typical manganese based Li-ion batteries [5]-[9]. Extrapolating the current unit price relationship to high volume applications, the battery pack for a typical medium-sized car would cost in the range of $7,000-$10,000 for a 16kWh pack.

Another critical issue to be considered is overall safety. The key factors that play a vital role in maintaining safety include, usage of high quality materials and safety monitoring at the development process. In addition, continuous monitoring of cell current, cell voltage, temperature, and taking eventual corrective measures, also helps in critically improving the safety of the system.

However, the most viable solution for today's problem might not be originated merely from changes in the battery chemistry. In fact, a much smarter solution relies on a

power electronic battery cell equalizer, which can improve not only the cycle life (the quantity of charge-discharge cycles before the end of life) of batteries, but also their calendar life (the time, fully charged and no cycling, to end of life), power, and safety. In the following chapters the impact of the utilization of a battery cell equalizer is going to be analyzed, in terms of economical as well as safety advantages.

1.3 Characteristics of Lithium Batteries for Vehicular Applications

1.3.1 Introduction to Lithium Batteries

Lithium rechargeable battery technologies, although not mature enough to be used in EV/PHEVs, prove to be the best solution for PHEV applications today. For instance, a 20 kWh lithium-ion battery weighs about 160 kg (100-140 kWh/kg), which is acceptable for PHEV applications. In contrast, current HEV Nickel-Metal Hydride (Ni-MH) batteries weigh between 275-300 kg, for the same application. Moreover, Li-ion batteries also depict excellent power densities (400-800 W/kg) [7], allowing more than 2C discharge rate. "C" represents the discharge of full capacity in 1 hour (at the rate of 40-80 kW peak power, in a 20 kWh pack), and up to 10C for some chemistries [8]-[9]. However, they also suffer from many drawbacks. One of them is the cost (projected at about \$250-\$300/kWh; \$600/kWh for the $LiFePO_4$ chemistry), which is the most expensive of all chemistries [5], [7]. The second drawback is that lithium is a very flammable element, whereby its flame cannot be put off with a normal ABC extinguisher [10]. Finally, Li-ion batteries have a cycle life between 400 to 700 cycles, which does not

satisfy HEV expectations [7]. Therefore, finding a solution to these issues is extremely crucial.

In order to resolve safety issues, few manufacturers have modified the chemistry of the battery [8]-[9]. This is currently the case for Lithium iron phosphate ($LiFePO_4$) batteries, which seem to have handled few issues related to EV applications, such us reducing flammability and obtaining higher cycle life (1000 cycles or more) [8]-[9], but the higher cost and equalization issues are still pending to be resolved.

With reference to cycle life, the battery can suffer significant degradation in its capacity, depending on its usage. Furthermore, the internal resistance also increases with each charge cycle. Also, according to the chemistry and the quality of the cells, a battery typically loses about 20% of its initial capacity after about 200 to 2000 full cycles, also known as the 100% state of charge (SOC) cycles. The cycle life can be greatly increased by reducing SOC, by avoiding complete discharges of the pack between recharging or full charging. Consequently, a significant increase is obtained in the total energy delivered, whereby the battery lasts longer. In addition, over-charging or over-discharging the pack also drastically reduces the battery lifetime [12]-[19].

1.3.2 SOLUTIONS TO KEYS ISSUES

An alternative way to solve the above mentioned problems, which are essentially common to the all lithium rechargeable batteries, is using electronic control, in the form of cell voltage equalizers. Few of the control rationales are briefly listed below.

1. *Over-Voltage Protection*

This functionality cuts charging current when the total voltage is more than 4.3V per cell. This is because, at higher voltages, metallic lithium is formed inside the cell [12], which is highly flammable, as explained earlier [10]. For the sake of simplicity, this protection is sometimes applied to the whole pack of cells, instead of measuring the voltage of each cell.

2. *Under-Voltage Protection*

This functionality cuts discharging current when voltage is under 2.5V per cell. Under this voltage, some capacity fades, and a specific quantity of unwanted copper plating is formed inside the cell [13]. This unwanted copper may generate internal short circuits. Also in this case, for the sake of simplicity, the total voltage might be measured, instead of verifying the voltage of each cell.

3. *Short Circuit or Over-current Protection*

This protection scheme disconnects the charging/discharging current if it is over a certain limit (2C to 50C, depending on the cell technology) [11].

4. *Overheating Protection*

There are 2 reasons as to why it is recommended to avoid working at high temperature: First is safety, because of the lithium flammability [10]. The second is degradation of the capacity increases with higher cell temperature. In this case, current stops flowing, if pack temperature rises over a certain value (about 60 °C) [11].

5. *Cell Voltage Equalizing*

Using a simple cell voltage equalizer, based on heat dissipation (using a resistor), some of the excessive power from the higher voltage cell can be successfully purged. Due to heating problems that this method may involve, the discharging current must be relatively small (about 300mA, depending on the capacity of the pack).

Although these protection functionalities are useful, they prove to be highly insufficient. In fact, the differences in capacity and internal resistance from cell-to-cell, within the same pack, may result in unwanted voltage peaks, especially during the final stages of charge and discharge. For example, during the charge of a battery pack, due to differences among the cells, a smaller capacity cell will finish with a voltage higher than the average. Depending on the protection circuitry, usually controlled by the total pack voltage, this situation may not be detected, and even if detected, the protection will simply cut the charger, reducing the battery capacity and not solving the issue at hand. A resistive equalizer will only reduce the voltage of the overcharged cell gradually, but it will not be able to avoid degradation of the cell.

A similar situation occurs during discharge. The lower capacity cell suffers from over-discharge, which is not detected by the protection circuit. Furthermore, the reduced capacity cell goes into over-charge and over-discharge. Thus, it suffers from additional capacity reduction and the cell rapidly deteriorates, which downgrades the overall capacity of the pack.

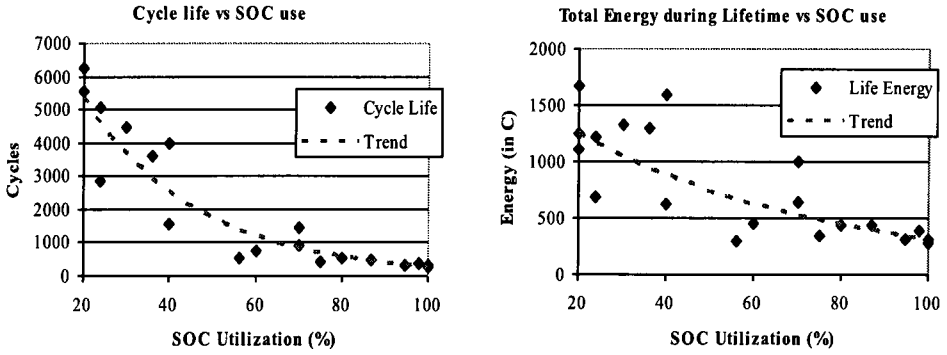
1.3.3 Cycle Life versus SOC

In the context of this chapter, 100% SOC is the state of a cell after being fully charged at 4.2V per cell, and 0% SOC corresponds to the state of a fully discharged cell (3V per cell). The initial Capacity (C) is the capacity during the first few cycles that go

from 100 to 0% SOC, and the cycle life is the amount of cycles after the cell loses 20% of its initial capacity.

If the battery is initially not fully charged, and not fully discharged during the discharge period and before charging again, then the full capacity is not used. Contrary to the Ni-Cd batteries, in lithium batteries this is actually beneficial to the cell. In fact, the cycle life is greatly increased.

In Fig. 1-4a, the cycle life of several available cells in the market are shown, under different SOC during the cycle. It can be appreciated how cycle life increases as SOC utilization is reduced. In this case, SOC utilization is considered to be centered around 50% SOC, or half charge. This is also confirmed by Fig. 1-4b, where the total energy delivered during the cell lifetime is also higher when SOC reduces. The latter is expressed in C units (initial capacity under 100% SOC).

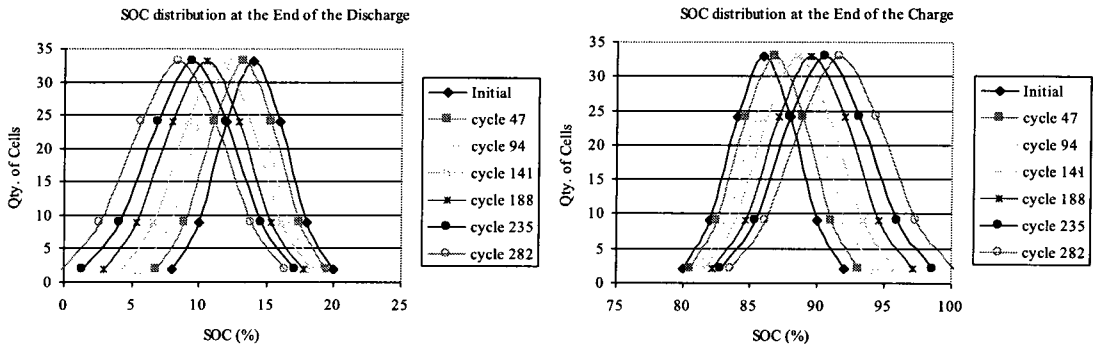


(a) (b)

Fig. 1-4 (a) Cell cycle life versus SOC utilization; (b) Cell total energy delivered during total lifetime versus SOC utilization.

The trend curves are critical for economical analysis. They are estimated based on the tests performed by [12]-[19]. Each point represents the value during a test performed on multiple reference sources, and the dotted line is the calculated trend of all those

values. The plots of Fig. 1-4 can also be the subject matter for further analyses. For example, in 360V HEV batteries, a string of 100 cells is used. In this simulation, a 5% initial dispersion (σ) in the capacity of the cells is considered, charging the pack at 4.1V per cell (86% SOC), and discharging at 72% of the total capacity (up to 14% SOC). An interesting trend can be observed. The smaller capacity cells swing initially from about 92% SOC to 8% SOC, which is 84% of the total capacity, instead of the average 72%. This higher SOC swing can be translated into less cycle life (282 cycles, instead of 600), which is a deeper degradation for the smallest capacity cells. This effect deepens during successive cycles, producing a premature degradation of smallest capacity cells, which brings the whole pack into a premature "out of service." Fig. 1-5a shows the distribution of SOC (quantity of cells versus SOC) at the end of discharge, in steps of 47 cycles. Fig. 1-5b shows the distribution of SOC (quantity of cells versus SOC) at the beginning of discharge, in steps of 47 cycles. The gradually increasing SOC span is an indication of the reduced capacity.



(a) (b)

Fig. 1-5 (a) Cell distribution of SOC in a pack, with initial σ = 5%, at the end of discharge; (b) Cell distribution of SOC in a pack, with initial σ = 5%, at the end of charge.

From Fig. 1-5, it is clear that the end of life arrives faster, because of the initial dispersion in capacity. Another critical inference that can be drawn is that the dispersion increases with cycle life. In this case, 282 operation cycles causes the smallest capacity cell to completely discharge, even if the demanded capacity is 72% of the nominal capacity. The average capacity cell, on the other hand, withstands 602 cycles of 72% nominal capacity, before over-charging or over-discharging. Although, this cycle life is better, it is still not enough from the point of view of PHEV energy storage applications.

Throughout this chapter, several issues related to lithium batteries, for EV/HEV/PHEV applications, have been exposed, particularly the unbalance in SOC among cells. It is clear that there can be considerable improvements in lifetime of a battery pack, if all cell capacities are suitably matched. A practical solution to obtain cell equalization exists in the form of an electronic cell equalizer. In chapter 2, the most common equalizer topologies are reviewed.

1.4 CONTRIBUTION OF THE THESIS

The major contributions of this thesis include:

(a) The quantification of improvement in lifetime (and cost) of a lithium-ion battery, due to the use of a cell equalizer.

(b) The evaluation of overall economic feasibility of PHEVs and EVs, considering lifetime with and without the use of equalization.

(c) The introduction of a novel power electronic cell equalizer configuration, capable of depicting high efficiency and low cost.

(d) The development of suitable control technique for the novel equalizer.

(e) The implementation of the proposed battery cell equalizer on an industry grade board, using commercial components, including overall validation of system cost effectiveness.

(f) Validation of the novel cell equalizer models, as well as the designed control system, using measurements obtained from the prototype.

1.5 THESIS OUTLINE

The contents of this thesis are organized into 6 chapters. Chapter 1 gives a brief introduction to the issues in using lithium rechargeable batteries for PHEV and EV applications. Chapter 1 also summarizes the major contributions of the thesis.

Chapter 2 reviews current cell equalizing techniques, and will compare their functionality, strong points, as well as weaknesses.

Chapter 3 evaluates the economic feasibility of battery cell equalizers, given the fact that the main goal of equalizing is prolonging battery life, thus reducing its maintenance cost. For this analysis, facts such as battery life extension, gas prices, and battery costs have to be carefully weighed.

Chapter 4 presents the novel cell voltage equalizer configuration, analyzes its mathematical model, and compares the results with simulation models and measurements performed on the built prototype.

Chapter 5 focuses on the control algorithm of the novel equalizer, taking in account the dynamic model of the battery. It also considers practical issues established during initial tests on the prototype, such as noise, limited processing power, resolution limitations, and numerical errors.

Chapter 6 summarizes the overall research conducted in the thesis and presents the overall conclusion. Finally, appropriate future research directions are suggested.

CHAPTER 2

INTRODUCTION TO CLASSIC AND ADVANCED PHEV/EV CELL VOLTAGE EQUALIZERS

2.1 INTRODUCTION

A battery cell voltage equalizer is essentially a power electronic controller, which takes active measures to equalize the voltage in each cell. Furthermore, by few additional methods, such as measuring the actual capacity and internal resistance of each cell (followed by instantaneous SOC computation), it is capable of equalizing the SOC of each cell. As a result, each of the cells will have the same SOC during charging and discharging, even in conditions of high dispersion in capacity and internal resistance. If all the cells have the same SOC utilization, they will degrade equally, at the average degradation of the pack. If this condition is accomplished, then all the cells will have the same capacity during the whole lifetime of the battery pack, avoiding premature end of life (EOL), due to the EOL of only one cell. If after SOC equalization, there still exists a case of faster degradation in some cells, the equalizer will further reduce the current demand on those cells, thus reducing the demand and degradation. In the example presented in section 1-3-3, in Fig. 1-5, instead of 282 cycles, the pack would last 602 cycles. For the same application, the requirement of current though the equalizer is 5 Amps of equalizing current from any one cell to another, as will be explored later in section 4.2.

In principle, there exist 3 basic groups of equalizers; resistive, capacitive, and inductive. In the next section their main characteristics are explored.

2.2 RESISTIVE EQUALIZERS

Resistive equalizers simply burn the excess power in higher voltage cells, as depicted in Fig. 2-1. Consequently, they represent the cheapest option, and are widely utilized for laptop batteries.

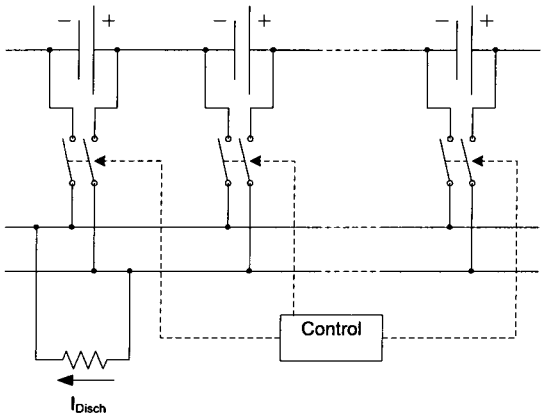


Fig. 2-1 Schematic representation of a typical resistive equalizer.

Obviously, due to inherent heating problems, resistive equalizers tend to have low equalizing currents in the range of 300-500mA, and work only in the final stages of charging and flotation. Due to the virtual non-existence of energy recovery, the efficiency is 0%. Also, because the battery should avoid working at high temperatures (section 1.3.2), and because in this configuration, all the equalizing current is transformed into heat, this equalizer configuration is not recommended for high reliability battery packs [20].

2.3 CAPACITIVE EQUALIZERS

Capacitive based equalizers use switched capacitors, as shown in Fig. 2-2, in order to transfer the energy from the higher voltage cell to the lower voltage cell. It switches the capacitor from cell-to-cell, allowing each cell to physically have the same voltage. Besides, it also depicts higher current capabilities than a resistive equalizer.

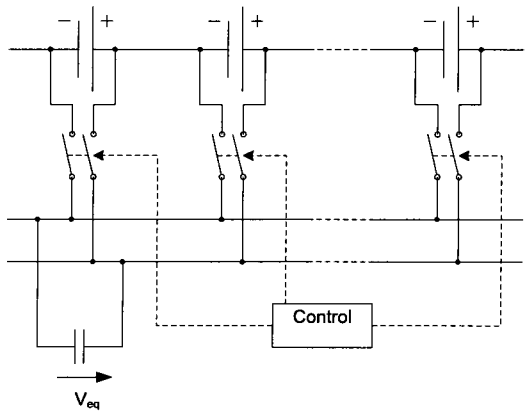


Fig. 2-2 Schematic representation of a typical capacitive equalizer.

In addition, capacitive equalizers are also quite simple to implement, without any control issues [20], [25]. At the same time, the main drawback of capacitive equalizers is the fact that they cannot control inrush currents, in the case of big differences in cell voltages, leading to potentially devastating current ripples flowing into the cells. Furthermore, they do not allow any desired voltage difference, which are especially critical in equalizing SOC.

2.4 INDUCTIVE EQUALIZERS

Inductive or transformer based equalizers use an inductor to transfer energy from the higher voltage cell to the lower voltage cell. In fact, this is the most popular family of high-end equalizers. Due to its capability to fulfill most of the needs for vehicular energy

storage: high equalizing current, high efficiency, and in some configurations, controllability, it is explored in detail in forthcoming sections of this chapter.

2.4.1 BASIC INDUCTIVE EQUALIZER

A basic inductive equalizer is shown in Fig. 2-3. These equalizers are relatively straightforward and can transport a large amount of energy. At the same time, they are also capable of handling more complex control schemes, such as current limitation and voltage difference control [21].

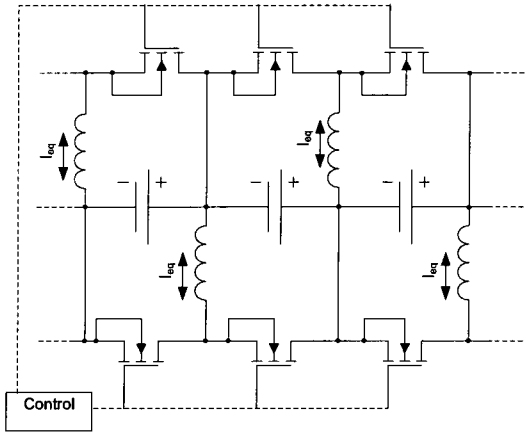


Fig. 2-3 Schematic representation of a typical inductive equalizer.

This allows the controller to compensate for the internal resistance of the cells, and increase equalization current, independent of the cell voltage. On the other hand, it takes some additional components to avoid current ripples from getting into the cell. Typically, this configuration requires 2 switches (plus drivers and controls) per cell. Also, due to switching losses, the distribution of current tends to be highly concentrated in adjacent cells. Hence, a high-voltage cell will distribute the current largely among the adjacent cells, instead of doing it equally in all the cells along the string. In this case, the

typical 50% duty cycle switching scheme could be replaced by a more global scheme, with a slight additional cost of more processing power.

2.4.2 CUK EQUALIZER

As the name indicates, this is an inductive-capacitive type of equalizer, primarily based on the *Cuk* converter topology. It shares almost all the positive characteristics of inductive equalizers, plus a very small cell current ripple. However, it suffers in terms of additional cost of power capacitors and double rated switches (higher voltage and current handling) [22]-[24]. The schematic representation of a typical *Cuk* equalizer is shown in Fig. 2-4.

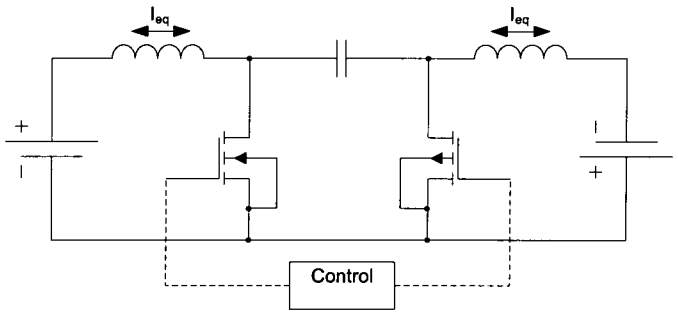


Fig. 2-4 Schematic representation of a typical *Cuk* equalizer.

The *Cuk* equalizer does incur additional losses due to the series capacitor, having slightly less efficiency than typical inductive equalizers. Similar to inductive equalizer, the *Cuk* equalizer also presents some issues while distributing equalizing current among all the cells in the string. This equalizer also possesses high current and complex control capability, at the expense of additional processing power.

2.4.3 TRANSFORMER BASED EQUALIZERS

The solutions provided by transformer-based equalizers theoretically permit the right current distribution along all cells, without any additional losses or control issues. One such popular arrangement is depicted in Fig. 2-5. [20]

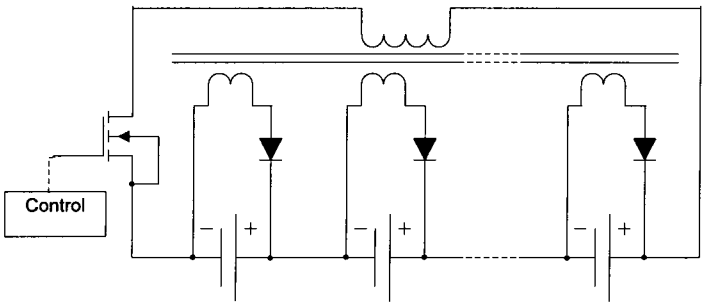


Fig. 2-5 Schematic representation of a multi-winding transformer equalizer.

Such a topology poses an additional problem of using a very complex multi-secondary transformer. This transformer is very difficult to mass produce, because all the secondary windings must have exactly the same voltage and resistance. If not, the differences will be translated into cell voltage difference, failing to perform the equalization accurately. Hence, this option is not a practical solution for high-count HEV cell packs. Moreover, this option also lacks the capability of handling complex control algorithms, such as current and voltage control. An alternative solution is presented in Fig. 2-6, using separate transformers for each cell.

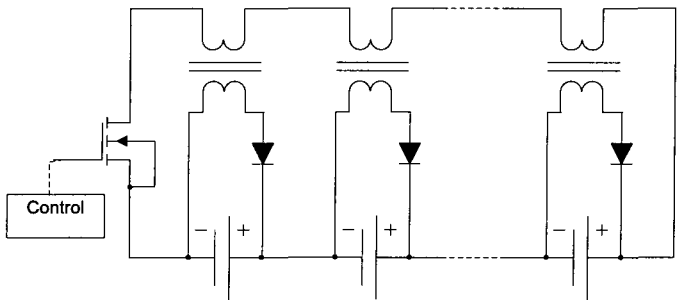


Fig. 2-6 Schematic representation of a multiple transformer equalizer.

This solution is modified here, in order to use 1:1 transformers, which are less difficult to mass produce [20]. Although this topology represents a substantial improvement with respect to multi-secondary transformers, in terms of manufacturability and cost, only a very small dispersion can be accepted in the transformer primary inductance. This is still very difficult to obtain in commercial inductors, with the risk of experiencing current and voltage imbalance.

2.4.4 NOVEL CELL VOLTAGE EQUALIZER

Keeping the various drawbacks of classic cell equalizers in mind, a novel design of a multi-cell equalizer, more specific for PHEV/EV energy storage applications, is presented in this thesis, in chapter 4. A simplified block diagram representation, that primarily highlights the basic principle of operation of a multi-cell equalizer topology, is shown in Fig. 2-7.

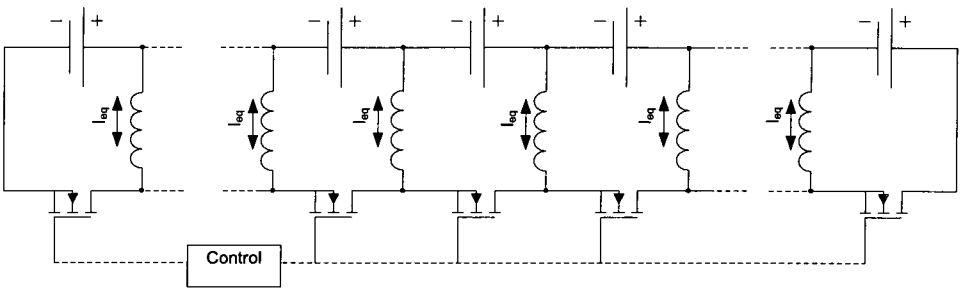


Fig. 2-7 Schematic representation of the proposed cell equalizer.

The proposed novel equalizer circuit has several advantages:

(a) Standard manufacturing requirements: the overall manufacturing process is simple, using low cost commercial components, no calibration required.

(b) Low component count: it only uses one MOSFET per equalized cell (instead of 2, in the typical and *Cuk* configurations), which reduces the component count, and therefore, the cost, as seen later in Table 3.2.

(c) Equal current distribution: It is capable of sharing the equalizing current more efficiently than other popular equalizers, except transformer based equalizers.

(d) Low cell current ripple: The inductors work in continuous conduction mode, thus obtaining minimal current ripple flowing through the cells.

(e) Independent current control: The proposed equalizer is capable of controlling the equalizing current independent of the cell voltage. Thus, it can achieve high equalizing currents independent of both the cell voltage as well as resistance.

The proposed equalizer topology also possesses a few drawbacks:

(a) Need for additional processing power: The current control in this circuit is based on the MOSFET's trigger timing calculation, a process which is highly

multifaceted, which has to be implemented in the on-board microcontroller. If SOC equalizing is desired (instead of cell voltage equalizing), additional processing power is invariably required. On the other hand, the necessary processing power can be easily allocated within the same on-board microcontroller, actually used for monitoring purposes. It is worth mentioning here that current available microcontroller technology allows performing such calculations without much additional cost.

(b) Chain length limitations: Because each MOSFET withstands the total voltage, and very low internal resistance MOSFETs (RdsOn) have usually low voltage (in the order of 30V to 60V) [26], the amount of cells that the equalizer can handle is limited (from 4 to 10 cells). Furthermore, the timing calculation complexity grows exponentially with the amount of cells. Keeping these issues in mind, this thesis explores 4 and 5 cell equalizers, without being necessarily limited to these numbers. In order to overcome this limitation, the cell equalizers can be chain connected, as shown in Fig. 2-8.

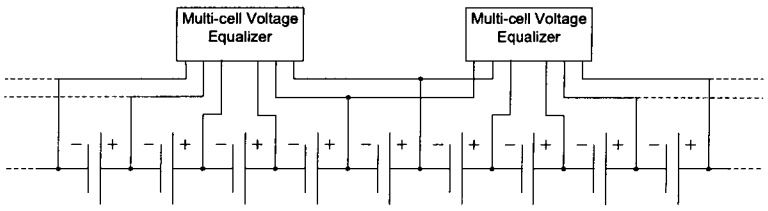


Fig. 2-8 Schematic representation of the proposed cell equalizer chaining method.

2.5 SUMMARY

Table 2-1 summarizes the capabilities of each type of equalizer. They are classified in relation with the main characteristics of each type of equalizer, as previously

reviewed. The ranking scheme considers the positive or negative effect over the equalizer, i.e. higher equalizer current is positive, while higher cost is negative.

Table 2-1 Comparison of cell equalizer characteristics [20]-[25].

Equalizer type	Equalizing current	Current distribution	Current control	Current ripple	Manufacture	Cost	Control
Resistive	--	N.A.	+	+++	+++	+++	+++
Capacitive	-	+	--	--	++	++	++
Basic Inductive	++	+	+	++	+	-	-
Cuk	++	+	+	+++	-	--	-
Transformer	+	+++	--	--	--	--	++
Novel equalizer	++	++	++	++	+	+	--

It can be appreciated, that in general, none of the equalizer configurations are a perfect fit for a particular set of applications. For example, in very low cost, low current applications, such as laptop batteries, the resistive equalizer is practical. For intermediate size batteries, where current or battery string length is limited, the capacitive or transformer based equalizers can be envisaged. In high current applications, especially with high count battery strings, the options are less obvious. In this high current range, the proposed novel cell equalizer configuration outperforms the various other options in terms of average performance, demonstrating positive performance in all characteristics, except in control complexity. The control aspect, though, as described before, does not necessarily imply a higher cost.

In conclusion, the high current carrying capability and the possibility of advanced control, based on instantaneous battery SOC estimation, combined with low cost and simplified manufacturing, makes the novel equalizer configuration a highly attractive and

practical option for EV/HEV/PHEV energy storage applications. In the next chapter the economic feasibility of using a cell equalizer is explored, in general. In particular, the cost impact of the novel cell equalizer is thoroughly reviewed.

CHAPTER 3

ECONOMIC SIGNIFICANCE OF BATTERY CELL EQUALIZATION

3.1 INTRODUCTION

In order to evaluate the economic feasibility of battery cell equalizers, more specifically, the novel cell equalizer configuration presented in this thesis, several critical factors need to be taken into account. Considering the high initial investment of a battery for PHEV applications ($5K-$10K), and the unimpressive cycle life of 500 to 2000 cycles in typical usage (section 1.3.2), at a first glance, the lithium rechargeable battery does not seem to be apt for EV/PHEV applications. Furthermore, certain concerns have been raised about the safety of using lithium rechargeable batteries in mobile applications.

Through the work presented in this chapter, it can be observed that a cell voltage equalizer with certain characteristics can seriously improve the cycle life and safety of lithium batteries. Later, the equalizer cost will also be determined. Finally, the conditions for the economic feasibility of PHEVs will be weighed against the size of the battery pack and the use of a cell equalizer arrangement. Parameters such as, rising price of the gas, capital interests, and calendar lifetime of the cell will also be taken into account.

The characteristics of lithium batteries, particularly its cycle life, have been analyzed in section 1.3.3 "Cycle life versus SOC." It was concluded that deeper discharges as well as a higher charges drastically reduce the cycle life of a cell. In

addition, the continuously degrading effect in cell capacity, followed by charge-discharge cycles on a multiple cell string, with initial small dispersion, was also demonstrated. In the next section, the benefits of the use of the battery cell equalizers will be highlighted.

3.2 IMPORTANCE OF BATTERY CELL EQUALIZERS

The primary characteristic of a battery cell equalizer is that it has the capacity to take energy from a higher SOC cell to a lower SOC cell. Several configurations have been explored in [20]-[25], and in chapter 2 of this thesis. It is worth mentioning here that only a few of them are capable of meeting cost targets and power/efficiency requirements of EVs and PHEVs.

Simulations performed on a battery string composed of 100 cells (360 Volts), with an initial capacity dispersion (σ) of 5%, have proven that an equalizer used in a typical PHEV application must be capable of driving more than 5A from the high voltage cell to the low voltage cell, in order to balance the SOC utilization of each cell, independent of individual cell capacities. In addition, this process should cost a small fraction of the overall battery price. The equalizer cost will be considered as $400, as analyzed later in Table 3.2.

Due to the equalizing characteristics of cell voltage equalizers, the SOC would tend to be equal in all cells; thus, the equalized battery pack will exhibit the cycle life of an average capacity cell, and not the one of the lower capacity cell. As a result, the whole battery pack will withhold 600 cycles, like the average cell, instead of 280 cycles, using 80% of the capacity. In addition, a higher cycle life is obtained using a smaller fraction of the total capacity. Consequently, the battery pack gains cycle life from 50 to 100%,

compared to non-equalized battery packs, as seen on section 1.3.3. The financial impact of this fact will also be analyzed later in this chapter.

As aforementioned, the microcontroller located in each equalizer board performs voltage and temperature monitoring of each cell, in order to maintain safety and health monitoring of the pack. These microcontrollers report the status to a central processor, which assures environmental conditions, such as maximum current and temperature control, and will perform failure detection and prediction. Microcontrollers are also responsible for MOSFET gate timing calculations for their own equalizer, located in the same board.

For comparative purposes, the cost of a typical cell voltage equalizer and the proposed novel cell equalizer, both capable of complying with the aforementioned specifications, will be analyzed in the next section. The transformer based equalizer and the *Cuk* equalizer will not be considered here; the first, because of impractical manufacturing issues, and the latter due to higher costs.

3.2.1 PHEV/EV CELL EQUALIZERS

The typical cell voltage equalizer, as shown in Fig. 3-1, proposed in [21], is a very simple, yet powerful example of an equalizer. It has a high current capacity and common components. In order to meet safety requirements, both temperature as well as voltage monitoring, have been added to the proposed system.

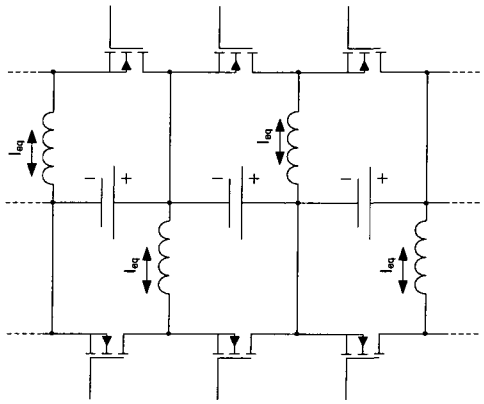


Fig. 3-1 Typical cell voltage equalizer.

Although fundamental benefits exist for the typical configuration, it also presents some weaknesses, i.e. higher cost, due to the double switch per cell and poor current distribution, which includes capability of distributing current equally among all cells. Conversely, the proposed novel cell voltage equalizer, shown in Fig. 3-2, also has the ability to drive high currents, while achieving high efficiency at the same time. Besides, it may also cost less than the typical equalizer, mainly due to the use of only 1 MOSFET (and its driver) per cell, as shown in Table 3.1. Although the control core is more complex than the typical equalizer, a simple implementation is presented in Chapter 5, and it may be implemented in the same microcontroller that performs safety monitoring, with only a small increase in RAM memory (1kB) and calculation time (2ms every sampled second). The additional cost of these requirements is evaluated in Table 3.1.

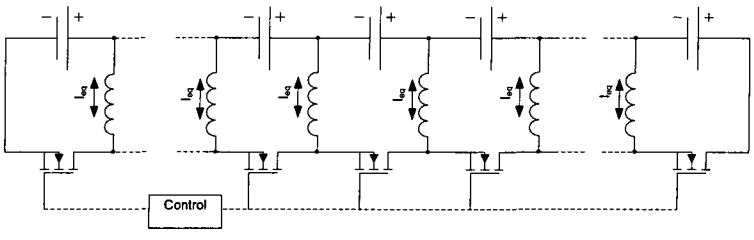


Fig. 3-2 Proposed novel cell voltage equalizer.

It must be pointed out here that both the equalizer arrangements have the potential to comply with the specifications needed for a PHEV application. In the next section their cost implications will be studied in detail.

3.2.2 Cost Analyses of Cell Equalizers

One of the key reasons for using a cell voltage equalizer is to increase lifetime and reduce overall cost of energy storage. Considering the fact that the main benefits of a cell equalizer is to extend lifetime of a battery pack, it is clear that it should not cost more than a small fraction of the battery pack itself. In this cost analysis, factors such as timing calculation, safety-monitoring, and inter-communication will be considered. These tasks will be performed by a microcontroller. Due to factual limitations, such as quantity of Analog-to-Digital inputs as well as PWM output channels, 1 microcontroller per equalizer unit of 5 cells, in the proposed topology, can perform the job satisfactorily. In case of the typical equalizer configuration, 1 microcontroller is dedicated to every 3 equalizer units (6 MOSFETs). This is due to the limitation in the number of PWM output channels, which ranges between 4 and 8 outputs per microcontroller. The constructed prototype uses a 6 PWM channel microcontroller, which provides an excellent balance between functionality and cost.

Even if the voltage ratings of the MOSFETs in the typical and novel equalizer are different, they in fact use the same MOSFETs. This is due to the fact that the novel equalizer uses 30V MOSFETs, which is considered to be the lowest MOSFET voltage. The typical equalizer would be able to use lower voltage rating (20V). However, in reality, those MOSFETs are simply not commercially available.

Table 3-1 shows the cost breakdown (the cost of the parts and the assembly) for

both the novel as well as typical equalizer. The prices are based in quantities of 10K [26], which is a rather small quantity, given the fact that an equalizer for a battery pack would need close to 100-120 MOSFETs. In fact, it is safe to assume improvements in price with higher production volumes.

Table 3-1 Cost breakdown of the mounted equalizer board.

Equalizer Board Items	Quantity per Board		Cost per unit ($)
	New Equalizer	Typ. Equalizer	
Equalizer Units	1	3	
Equalized Cells	4	3	
MOSFETs	5	6	0.4
MOSFET Drivers	5	6	0.6
Inductors	4	3	0.8
Microcontroller	1	1	3
Capacitors	5	4	0.2
Optocouplers	2	2	0.1
Other components	1	1	0.5
PCB	1	1	1.6
Component mounting	40	40	0.03

Consider a 20kWh battery pack, consisting of 100 cells, costing a total of nearly $6,000. The expected aim is for the equalizer not to cost more than 10% of the battery pack. This pushes the equalizer price to $6 per cell and a total of $600 per battery pack. Table 3-2 summarizes the estimated total cost for each equalizer.

Table 3-2 Equalizer total cost estimation.

Eq. Type	$/board	Cells/board	$/Cell	Boards/Pack	$/Pack
New Equalizer	15.84	4	3.96	25	396
Typical Equalizer	15.81	3	5.27	34	537.5

Table 3-2 proves that in both cases, the cost target was met, and that the proposed novel equalizer outperforms the typical equalizer cost by 37%. Moreover, Table 3-2 also proves that the cost target is not only met, but is also improved by 40%. In the next section, the economic feasibility of PHEVs will be analysed.

3.3 PHEV ECONOMIC AND FINANCIAL ANALYSIS

It is obvious that there is an economic impetus in switching from conventional gas based vehicles to advanced EVs/HEVs/PHEVs. Thus, an in-depth economic and financial analysis is mandatory, based on the following critical factors:

(a) Cost of gas: Even considering the fall of gas prices after Sept. 2008, statistically, gas prices have elevated to an average of 15% per year in the last 5 years [1]. Several scenarios will be considered (10%, 15%, and 20% per year), based on 0.6 USD per liter, at the end of 2008, which is a very conservative estimation, considering the latest rise in gas prices (since May 2009). Gas savings, based on this calculation, will be used to pay the surplus of a PHEV system, if possible.

(b) Interest on capital will be estimated as 5%.

(c) Rise in electricity price will be considered as 5%, starting from $0.1/ kWh (2008) [27].

(d) The calculations performed in this chapter are for an average small vehicle (family sedan), considering all-electric driving of 16,000 km (10,000 miles) per year, with one charge per day. Additional mileage, based on gas, is to be considered.

(e) Autonomy of 50 km (30 miles) is considered, which fairly represents the daily driving average. This is equivalent to 7.5kWh per charge, based on simulations performed in the ADVISOR software, under the UDDS test procedure [28].

(f) The overall cost of the equalizer was demonstrated before, and is considered here as $600.

(g) The influence of the cost of a lithium battery will also be evaluated, using 3 types of batteries: low, average, and full-performance.

(h) Low cost batteries are represented by the typical Li-ion chemistry, like the one used in laptops, costing about $300/kWh. The cycle life is shown in Fig. 3-3. The annual degradation, which is independent of cycle degradation, amounts to 3% per year [6]-[7].

(i) Full-performance batteries are essentially top-of-the-line cells, with LiFePO4 chemistry. Although it is a new technology, and complete data is not yet available, it is possible to consider the volume price as $600/kWh. In addition, the cycle life is about 3 times better than typical Li-ion batteries (1000 cycles at 100% SOC [8]), with an annual degradation of 1% [8]-[9].

(j) Average batteries, represented by good quality Li-ion, or some alternate Lithium chemistry, cost about $400/kWh, with cycle life 2 times better than those depicted by low-cost cells, with an annual degradation of 2%.

(k) A fixed cost of $3,000 will be added to the PHEV, to account for additional costs, for all-electric propulsion.

(l) The remaining value of the battery at the end of its lifetime will not be considered, although a battery with half its original capacity would still be useful for other applications, such us UPS systems [7].

In the next few sections, several combinations of battery capacities will be analyzed in order to obtain 50 km (30 miles) autonomy in a PHEV. Using larger batteries for similar requirements will allow smaller discharges with respect to full capacity, and will make cycle life longer, as was seen in the chapter 1. On the other hand, larger batteries point towards higher initial costs, and will affect the payback time, and hence, the Return on Investment (ROI). The ROI will be calculated using the estimated gas saved during the battery utilization, minus the electricity expenses, considered as down-payment per year, leaving the remaining capital exposed to annual interests.

Fig. 3-3a presents a comparison of the battery lifetime and the system payback time as a function of the battery size. Also, the lifetime is expressed as a function of annual degradation (1%, 2%, and 3%), and payback time is expressed as a function of the initial battery cost ($300, $400, and $600/kWh). Fig. 3-3-b represents the same comparison, for a system with a cell equalizer.

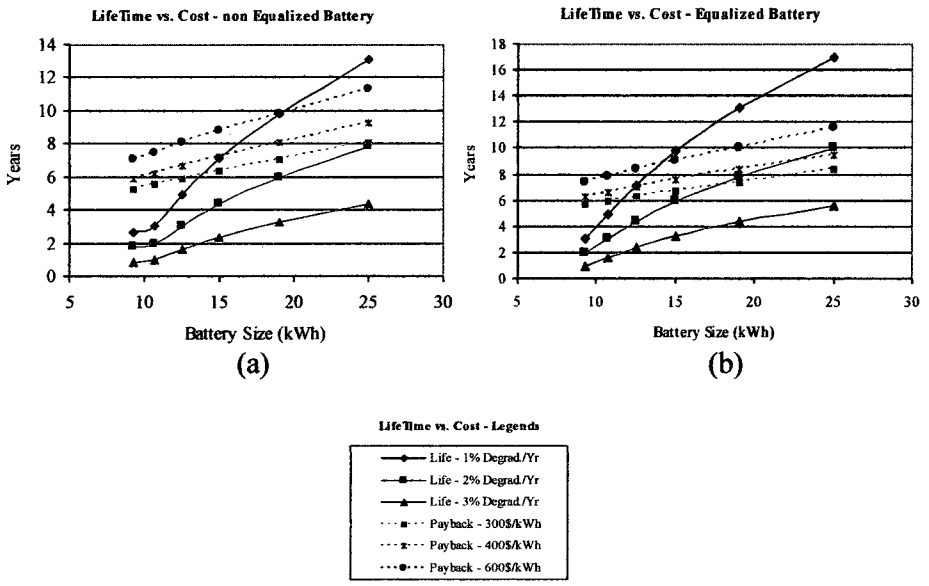


Fig. 3-3 Battery lifetime vs. electric system payback time, (a) non-equalized system; (b) equalized system.

From Fig. 3-3-a, it can be appreciated that a non-equalized system is almost never or marginally paid back. The investment only returns under strict conditions, such as over-sizing the battery to 25 kWh, and having a long life battery with 1% degradation per year. On the other hand, Fig. 3-3-b demonstrates that returns are significant for a system with a suitable cell equalizer. Hence, it can be safely concluded that any battery, lasting more than 10 years, will more than pay back for itself. Not surprisingly, some hybrid manufacturers warrant their hybrid components up to 8 years or 160,000 kilometers.

Figs. 3-4a, 3-4b, and 3-4c depict a comparison of net gains using a PHEV system, compared to a conventional gas vehicle, at the end of the lifetime. This scenario is considered for an equalized system, using the following combinations: a battery with 1% degradation per year and \$600/kWh, 2% and \$400, and 3% and \$500. The plots show the returns on PHEV surcharge investment against the gas costs saved at the end of the life of the battery (ROI), as a function of battery size. Fig. 3-4a depicts the returns, considering the rise in gas prices, at an average of 10% per year, Fig. 3-4b shows this value to be 15% per year, and Fig. 3-4c shows it to be 20% per year. Fig 3-4d again, considers a 15% gas price increase per year, but starting in 2010, at \$0.7/liter, which is the calculated value, using the 5 year tendency in gas price fluctuation trend.

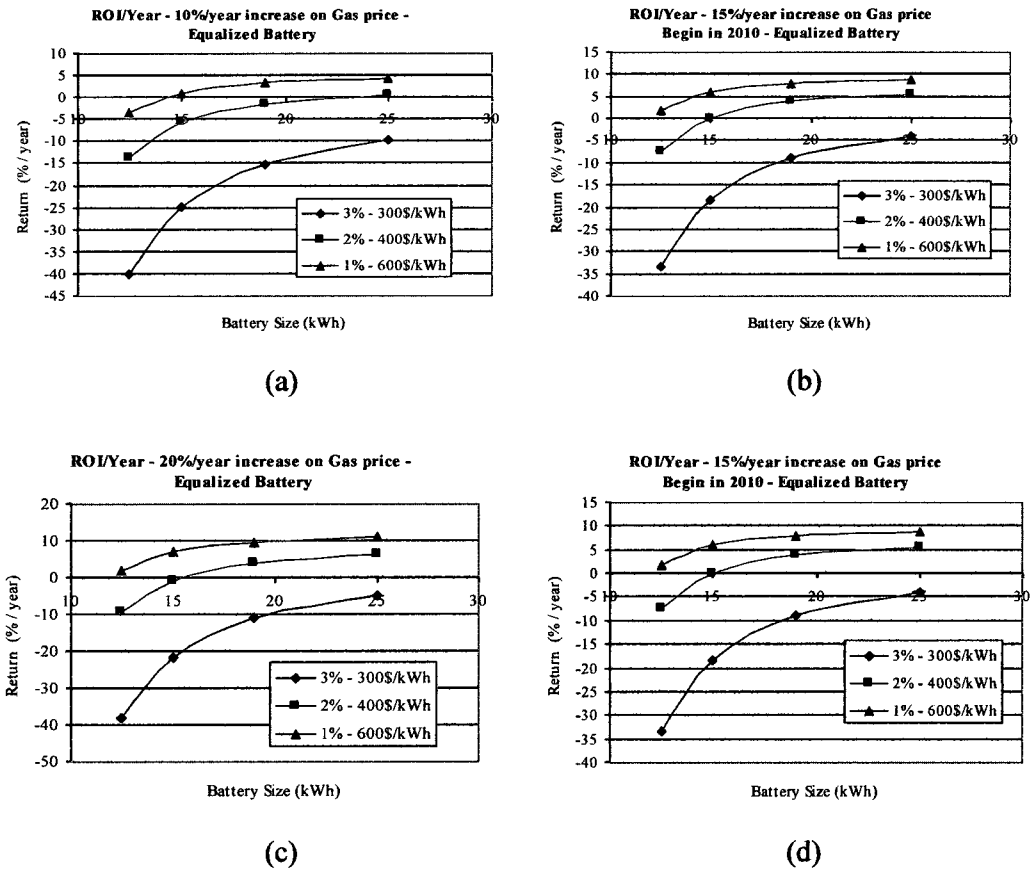


Fig. 3-4 Battery ROI/year for a PHEV system investment, at the end of battery lifetime (a) considering 10% gas price increase/year; (b) considering 15% gas price increase/year; (c) considering 20% gas price increase/year; (d) considering 15% gas price increase/year, starting in 2010.

It is clear that the higher the rise in gas prices, the greater the savings, and thus, higher the benefit of using a PHEV system. The 10% average annual increase of gas price is not likely to happen, considering that gas at the pump station has risen at an average of 15%/year, in the last 5 years. This rate was about 25% in 2007-2008, and it currently seems to be recovering from the price fall from Sept. 2008 to May 2009. It must be noted that these projections have not considered any artificial event, such as political instability or speculation, which will make the PHEV option even more interesting. In any case, the

ROI is higher in all scenarios, for batteries that last more than 10 years. Although the ROI for a 25kWh battery pack (30% SOC discharge) is slightly higher, the difference may not be worth the increase in the initial investment and weight. Furthermore, the predicted returns starting next year (2010) are much more notable.

It is interesting to note that a slight gain in the ROI is experienced by reducing the annual degradation, instead of lowering the cost of the battery. Using a battery with 1% degradation per year and paying 20% more on battery cost makes 1.5% more return per year, in all cases. In other words, it pays more to extend the battery life, rather than producing it slightly cheaper. Also, the impact on the ROI by using different battery technologies is smaller than that when using a suitable cell equalizer. Thus, it is obvious that future research directions and discussions, specifically related to battery lifetime, should be duly channeled towards critical issues, such as cell equalization, monitoring, and sizing, rather than being focused solely on mere battery chemistries.

There are other benefits of using an EV/PHEV system, not considered in this analysis, like government subsidies to green vehicles, tax rebates, carbon taxes, and protection against gas price spikes. They have not been considered here, because the objective of this chapter is to prove the economical feasibility of an equalized PHEV energy storage system, independent of artificial conditions, which in any event, will eventually become additional net gains.

3.4 SUMMARY

In conclusion, it is safe to say that PHEVs are indeed economically viable today, even in a medium-priced oil market, given the following conditions:

(a) The battery should be oversized in order to last longer, and it should never be fully discharged nor fully charged. These conditions are enforced by the on-board hybrid management system (not part of the equalization system), which turns off the utilization of the battery, if the SOC (or the voltage) is outside limits. Of course, this fact will raise the initial investment.

(b) The use of a cell equalizer and monitor is mandatory. Longer lifetime of the battery pack at a very low cost makes a huge difference in the return on investment (ROI). On the other hand, the cell equalizer has to comply with low cost, high-current, and high-efficiency requirements. A novel cell voltage equalizer, capable of accomplishing these expectations, is described in the next chapter.

(c) Battery annual degradation and cycle life are imperative parameters. Currently, the $LiFePO_4$ chemistry seems to comply with these requirements. Nevertheless, the use of battery equalizers double the profits obtained with high-quality batteries, with lower annual degradation.

In summary, in Fig. 3-3 it can be appreciated that any battery lasting more than 10 years is paid-off, and preferably more than 12 years, in order to have interesting returns. This is possible under the aforementioned conditions, with the best battery technology available today. Not surprisingly, current proposed PHEV architectures consider using the smallest battery that would last about 10 years. In this scenario, considering an initial cost of about $10,000, the ROI is expected to be about 10 years.

In addition, there would be much more profits of using PHEVs in the next 2-3 years, due to the continuously rising price of oil. For example, a PHEV produced in 2010

could increase the ROI from 6.5% to 8% per year. Moreover, the work presented in this chapter has not considered surcharges, which may be due to political instability, disruptions in oil production (for natural or artificial causes), speculation in prices, and peak oil theories; all of the events that are highly likely to occur.

Given these conditions, the high initial investment will be fully compensated by savings in gas in the ensuing years. Also, the high returns will most definitely invite investors to support initial costs. As future work, additional experimental verification will be necessary, to add more mathematical precision to the battery cycle life model.

In conclusion, appropriately designed cell equalizers and improved battery dimensioning models will most definitely pave the way towards wider utilization of EVs/PHEVs. A novel cell voltage equalizer is discussed in detail in the next chapter, which is capable of accomplishing the low cost, high current, and high efficiency.

CHAPTER 4

NOVEL BATTERY CELL EQUALIZER TOPOLOGY: PERFORMANCE AND COST ANALYSIS

4.1 INTRODUCTION

It has been proven in the previous chapters that an equalizer to be used in a typical PHEV/EV application should be capable of driving more than 6A from a high-voltage cell to a low-voltage cell, and must cost a small fraction of the battery price (less than 10%). An equalizer, which satisfies these conditions, drastically improves the life cycle of an EV battery, increasing the chances of positive ROI.

In this chapter, the proposed novel battery cell equalizer, as presented in section 2.4.4, is thoroughly evaluated. A schematic representation of the proposed cell equalizer is shown in Fig. 4-1. Thereafter, the common specifications of an equalizer for EV/PHEV ESS applications are evaluated. The capabilities as well as cost issues of the proposed equalizer topology will also be analyzed in detail in this chapter. Finally, a comprehensive comparison between the mathematical model of the novel equalizer, a typical inductive equalizer (as presented in section 2.4.1), and the experimental prototype (Fig. 4-2) of the novel equalizer, is also included.

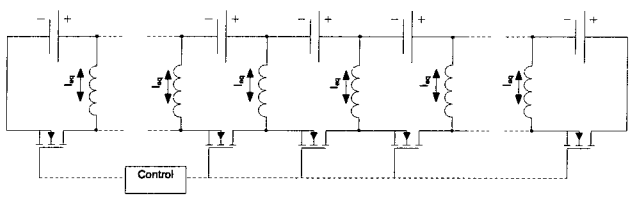


Fig. 4-1 Schematic representation of the proposed cell equalizer.

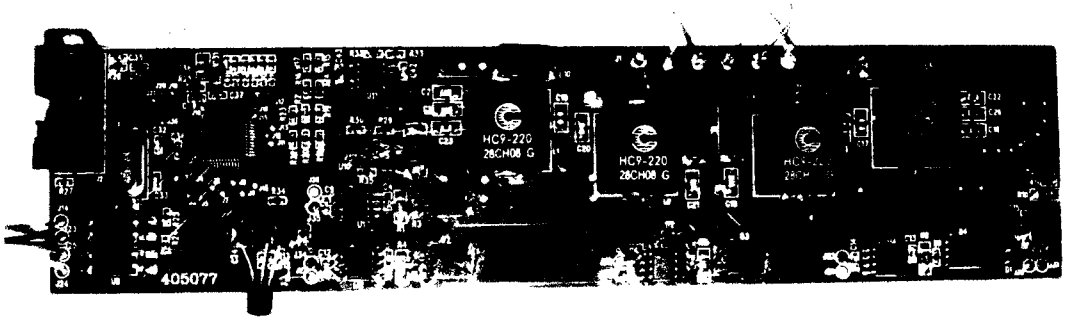


Fig. 4-2 Experimental prototype of the novel cell equalizer.

4.2 DESIGN SPECIFICATIONS

Considering that the main goal of an equalizer is maintaining the same SOC at all times, there are several issues to consider for an equalizer design. First, the equalizer must be capable of transferring the necessary amount of power to maintain the battery cells balanced, not necessarily during high power peak demands, but during the full discharge or charge cycles. A common EV/PHEV battery consists of a string of around 100 cells. Because of normal dispersion, not all cells have the same capacity. In fact, measurements performed in the lab and by [24] demonstrated a dispersion of up to 5% in the capacity of cells. It was determined in the previous chapter that an EV/PHEV battery has to possess energy between 15 kWh to 30 kWh, in order to be paid off. This means that each cell of the battery pack has a capacity ranging between 50Ah and 100Ah. Furthermore, discharging larger batteries by 50%, in 30 minutes, will lead to an average consumption of 100A. In order to compensate for 5% dispersion in the cell capacities, the equalizer should transfer up to 5A from any one of the cells to another.

Secondly, the equalizer has to depict a good efficiency during energy transfer. As a reference, the obtained efficiency from previous literature, starts as low as 60%, using

hard switching [23]-[24], to 80-83%, using soft switching [24] and [29]. In addition, as will be analysed in section 4.4.3, the typical equalizer obtains an average of 70% power transfer efficiency. Although the equalizer presented in this thesis uses hard switching, an improvement in the efficiency is expected, and an initial objective of 75% efficiency will be set.

Thirdly, any equalizer should have a certain precision in the equalization balance. The SOC estimation, used in [30], [32], and [33], obtained about 0.1% precision in V_{OC} estimation. Because the equalizer presented in this chapter equalizes V_{OC}, this difference will be considered as the accepted unbalance in the cells.

Furthermore, as was analysed in Chapter 3, the equalizer should cost a small fraction of the cost of the battery (less than 10% of the total cost, about $6.00/cell), in order to allow the EV/PHEV system to be paid off. The equalizer presented in this thesis easily meets this criterion, as demonstrated in Chapter 3.

Finally, an equalizer has to be capable of reporting status and alarms of the battery condition to a central processor. Table 4-1 summarizes the design specifications of an equalizer for EV/PHEV applications.

Table 4-1 Design specifications of an equalizer for EV/PHEV applications.

Equalizer Specifications	Cost per unit ($)
Peak equalizing current	> 5 Amps
Efficiency	> 75 %
V_{OC} error between cells	> 0.1 %
V_{OC} cell average error	> 0.1 %
Cost	> $6.00/cell

4.3 CIRCUIT ANALYSIS OF THE PROPOSED CELL VOLTAGE EQUALIZER

4.3.1 THE PROPOSED CELL VOLTAGE EQUALIZER

In this example, a 4-cell equalizer will be analyzed in detail, as shown in Fig. 4-3. This analysis may be extended to any *N*-cell equalizer. Fig. 4-3 shows the MOSFET firing sequence.

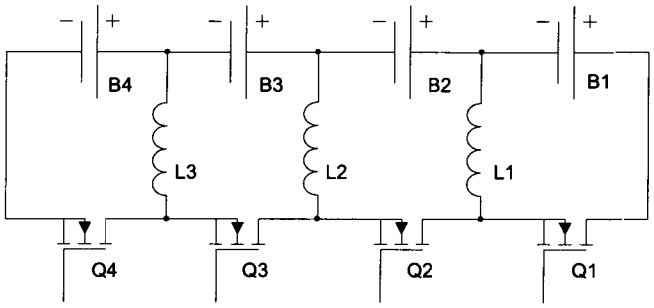


Fig. 4-3 Topological layout of a 4-cell voltage equalizer.

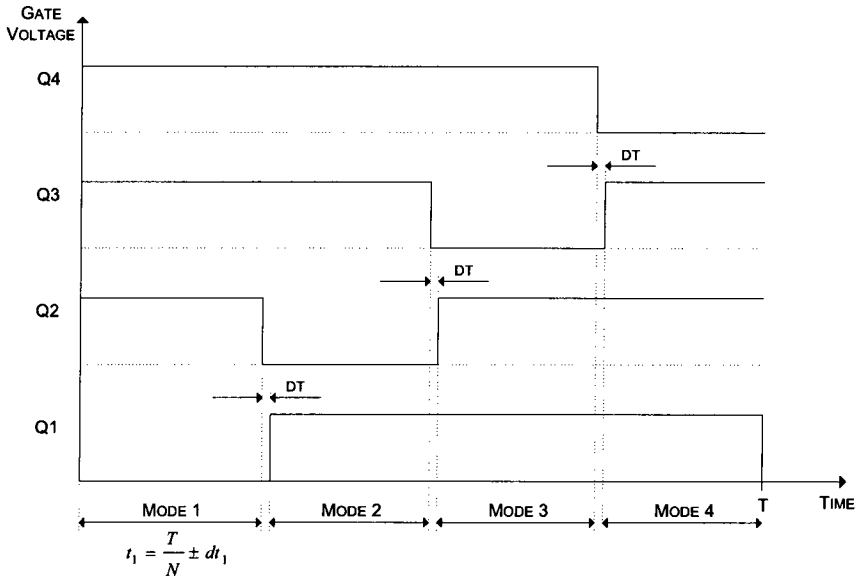


Fig. 4-4 MOSFET firing sequence for the 4-cell topology.

Fig. 4-4 shows that all MOSFETs are triggered together, except one, at all times. In this example, each mode has equal operating time, T (total time), over N number of cells, and is represented by one of the MOSFETs turned off. For example, in a 4-cell equalizer, each MOSFET will be off for about $1/4^{th}$ of the time, plus or minus an adjusting time (dt_n). The duty cycle of each mode will be defined as τ_n, where n is the mode number.

Among the various tasks to be performed by the equalizer, it also sometimes needs to shift current with very little or no voltage difference. At the same time, high current is always desirable, which means that very small parasitic resistances, copper traces, as well as the internal resistance of MOSFETs (R_{dsOn}) may have a strong influence on overall current distribution. In order to correct this effect, small modifications can be made in trigger timing, allowing production of desired distribution of current. The main objective of the small dead-time between modes, as shown in Fig. 4-4 (DT), is to avoid a current shoot-through in the MOSFETs. This is not considered as an operation mode, due to its trivial influence on the overall operational characteristics.

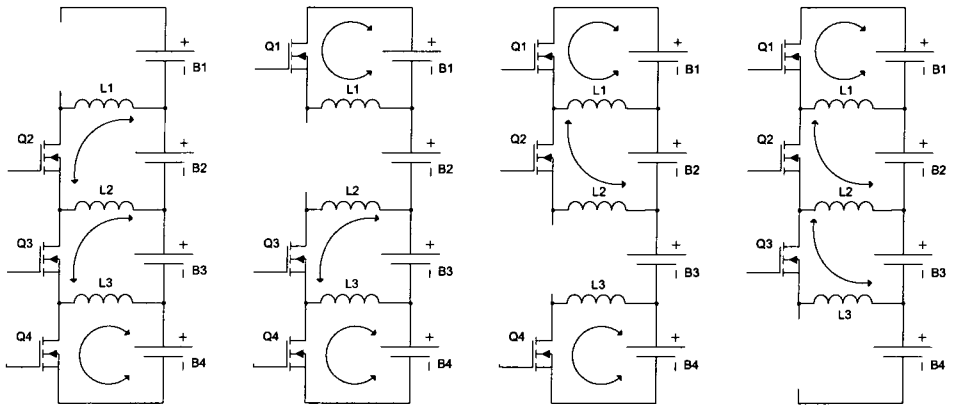


Fig. 4-5 Modes of operation: (a) Q1 off, (b) Q2 off, (c) Q3 off, and (d) Q4 off.

The different modes of operation of the 4-cell equalizer are displayed in Fig. 4-5. Each mode is defined by one of the MOSFETs not in conduction.

The voltages and currents in the circuit are shown in Figs. 4-6 and 4-7. For demonstration purposes, in this example, the circuit is performing a current transfer from the first cell to the second cell, with all the cells having the same voltage, equal to $1/4^{th}$ of the total voltage (V_t). The duty cycle of each mode (τ_n) has been adjusted, in order to force the current transfer in the desired manner. The timing calculation is described in the next section.

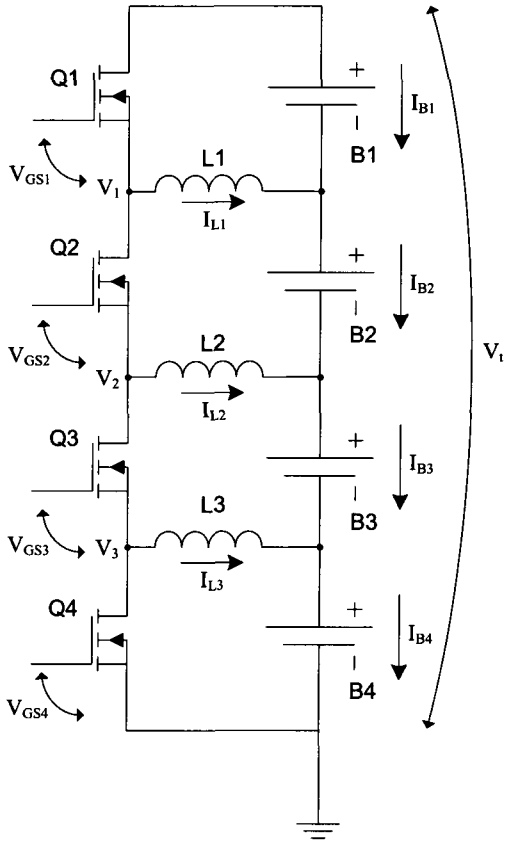


Fig. 4-6 Equalizer voltages and currents.

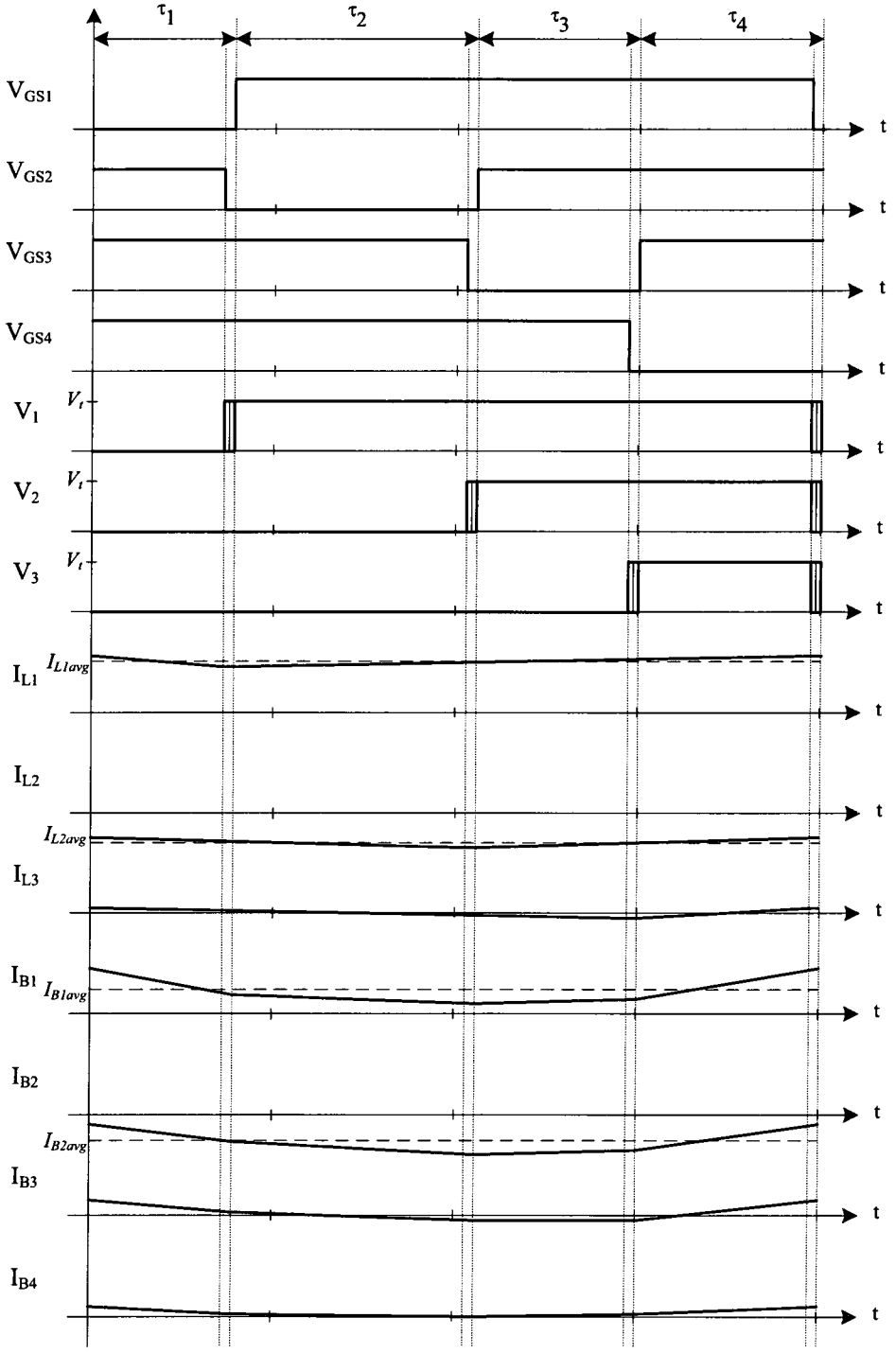


Fig. 4-7 Equalizer voltages and currents.

The minimum τ_n will be set to 0.5 times the typical time, and the maximum τ_n is set to 1.5 times the typical time. This is set to avoid overly fast switching and the possibility of one mode disappearing. The dead time between modes is very small, compared to τ_n (around 50ns, versus 2μs, in the equalizer used in this thesis), and it can be safely ignored from the mathematical model.

The MOSFETs have to be selected to withstand V_t as maximum voltage, plus ringing due to parasitic inductances of the PCB traces. In this prototype, 30V MOSFETs were selected, for a maximum working voltage of 21V, which is the minimum voltage found in commercial MOSFETs. The maximum MOSFET current is the maximum inductor current plus headroom to avoid malfunction in the case of short-circuit in the outputs. Another important parameter is the Rds_{ON} versus the C_{GS} as well as cost. For example, the use of a MOSFET with an Rds_{ON} of 3 mΩ, instead of 7 mΩ, leads to an increase of 5% in the efficiency at high power. However, a 10% higher cost per cell is incurred, and idle losses are doubled, due to a higher C_{GS}. Actually, both types of MOSFETs are good for this application, depending on the trade-off between power and cost.

The inductor sizes are computed so as to operate in continuous conduction mode (CCM) in most cases, as seen in Fig. 4-7 (I_{L1} and I_{L2}). Lower inductance values will increase the current ripple, thus increasing idle losses. The results of this current ripple on the inductors can be observed later, in section 4.4.3. On the other hand, higher inductance values increase the cost and the size of the equalizer. Higher switching frequency will reduce the current ripple (and the idle losses). However, this will increase the switching losses, reducing the efficiency at higher power transfer. A successful design should

balance switching frequency, inductor size, cost, and efficiency, to find the optimal combination for each application. The equalizer designed in this thesis was optimized to work efficiently between 1-5 Amps of current transfer.

Furthermore, as can be appreciated in Fig. 4-7, current is transferred as desired, from cell 1 to cell 2. There is also an undesired current ripple over the cells, which should be filtered, to avoid additional losses in the internal resistances of the cells.

4.3.2 Mathematical Model of the Proposed Cell Voltage Equalizer

In this section, 2 possible mathematical models of the 4-cell equalizer will be analysed and compared to simulations performed in a "closest-to-real" situation. The "first" mathematical model was simplified, in order to fit in the reduced processing power of a microcontroller. Thereafter, a second order model was deduced, in order to validate the modeling technique. Moreover, it is possible to extend the model to 5 or more cells per system.

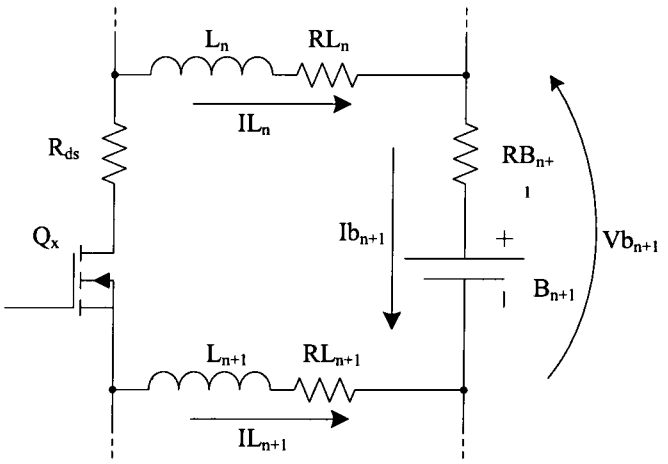


Fig. 4-8 Equalizer currents and voltages.

Defining the currents and voltages in the equalizer, as shown in Fig. 4-8, the current through the inductors (I_{Ln}) is considered constant (as seen in Fig. 4-7). I_{Ln} can be computed as the average voltage applied over the inductors (in all modes) divided by the inductor internal resistance (R_{Ln}). Taking into account the voltage lost in the MOSFET resistance (R_{ds}), which depends on the inductor currents and the timings, and taking into consideration cell voltage (V_{bn}), which is sum of V_{OC} and voltage drop across the internal resistance, and total battery pack voltage (V_t), as well as the duty cycle of each mode τ_n, the equations 4-1, 4-2, and 4-3 describe the voltages and currents in the first, second, and third mode:

$$-Vb_1 + \tau_1 \cdot Vt = \begin{pmatrix} I_{L1} & I_{L2} & I_{L3} \end{pmatrix} \cdot \left[\begin{pmatrix} 3 & 1 & 1 & 1 \\ 2 & 0 & 1 & 1 \\ 1 & 0 & 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} \tau_1 \\ \tau_2 \\ \tau_3 \\ 1-\tau_1-\tau_2-\tau_3 \end{pmatrix} \cdot R_{ds} + \begin{pmatrix} R_L \\ 0 \\ 0 \end{pmatrix} \right] \quad (4\text{-}1)$$

$$-Vb_1 - Vb_2 + \tau_1 \cdot Vt + \tau_2 \cdot Vt = \begin{pmatrix} I_{L1} & I_{L2} & I_{L3} \end{pmatrix} \cdot \left[\begin{pmatrix} 2 & 0 & 1 & 1 \\ 2 & 2 & 2 & 2 \\ 1 & 1 & 0 & 2 \end{pmatrix} \cdot \begin{pmatrix} \tau_1 \\ \tau_2 \\ \tau_3 \\ 1-\tau_1-\tau_2-\tau_3 \end{pmatrix} \cdot R_{ds} + \begin{pmatrix} 0 \\ R_L \\ 0 \end{pmatrix} \right] \quad (4\text{-}2)$$

$$-Vb_1 - Vb_2 - Vb_3 + \tau_1 \cdot Vt + \tau_2 \cdot Vt + \tau_3 \cdot Vt = \begin{pmatrix} I_{L1} & I_{L2} & I_{L3} \end{pmatrix} \cdot \left[\begin{pmatrix} 1 & 0 & 0 & 1 \\ 1 & 1 & 0 & 2 \\ 1 & 1 & 1 & 3 \end{pmatrix} \cdot \begin{pmatrix} \tau_1 \\ \tau_2 \\ \tau_3 \\ 1-\tau_1-\tau_2-\tau_3 \end{pmatrix} \cdot R_{ds} + \begin{pmatrix} 0 \\ 0 \\ R_L \end{pmatrix} \right] \quad (4\text{-}3)$$

The average current through each cell, I_{Bx}, is related not only to I_{Lx}, but also to the timing of each mode. Hence, the equation for the cell currents is:

$$\begin{bmatrix} -(\tau_2+\tau_3+\tau_4) & -(\tau_3+\tau_4) & -\tau_4 \\ \tau_1 & -(\tau_3+\tau_4) & -\tau_4 \\ \tau_1 & \tau_1+\tau_2 & -\tau_4 \\ \tau_1 & \tau_1+\tau_2 & \tau_1+\tau_2+\tau_3 \end{bmatrix} \cdot \begin{pmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \end{pmatrix} = \begin{pmatrix} Ib_1 \\ Ib_2 \\ Ib_3 \\ Ib_4 \end{pmatrix} \quad (4\text{-}4)$$

In order to reduce the complexity of the above equations, the MOSFETs could be considered as ideal switches (R_{ds} = 0Ω). Under these conditions, equations 4-1 to 4-4 can be simplified and combined to form equation 4-5; it depicts the equation of the cell currents as a function of the cell voltages and the timing. In the context of this thesis, this equation will be referred to as the "First Mathematical Model."

$$\begin{bmatrix} -(\tau_2+\tau_3+\tau_4) & -(\tau_3+\tau_4) & -\tau_4 \\ \tau_1 & -(\tau_3+\tau_4) & -\tau_4 \\ \tau_1 & \tau_1+\tau_2 & -\tau_4 \\ \tau_1 & \tau_1+\tau_2 & \tau_1+\tau_2+\tau_3 \end{bmatrix} \cdot \begin{bmatrix} -(\tau_2+\tau_3+\tau_4) & \tau_1 & \tau_1 & \tau_1 \\ -(\tau_3+\tau_4) & -(\tau_3+\tau_4) & \tau_1+\tau_2 & \tau_1+\tau_2 \\ -\tau_4 & -\tau_4 & -\tau_4 & \tau_1+\tau_2+\tau_3 \end{bmatrix} \cdot \begin{pmatrix} Vb_1 \\ Vb_2 \\ Vb_3 \\ Vb_4 \end{pmatrix} \cdot \frac{1}{R_L} = \begin{pmatrix} Ib_1 \\ Ib_2 \\ Ib_3 \\ Ib_4 \end{pmatrix} \quad (4\text{-}5)$$

Combining equations 4-1, 4-2, and 4-3 leads to equation 4-6, which expresses the inductor currents versus cell voltage and timing.

$$\begin{bmatrix} -(\tau_2+\tau_3+\tau_4) & \tau_1 & \tau_1 & \tau_1 \\ -(\tau_3+\tau_4) & -(\tau_3+\tau_4) & \tau_1+\tau_2 & \tau_1+\tau_2 \\ -\tau_4 & -\tau_4 & -\tau_4 & \tau_1+\tau_2+\tau_3 \end{bmatrix} \cdot \begin{pmatrix} Vb_1 \\ Vb_2 \\ Vb_3 \\ Vb_4 \end{pmatrix} \cdot \frac{1}{R_L} = \begin{pmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \end{pmatrix} \quad (4\text{-}6)$$

Also, the inductor currents can be deduced as:

$$\begin{pmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \end{pmatrix} = \begin{pmatrix} Ib_1 - Ib_2 \\ Ib_2 - Ib_3 \\ Ib_3 - Ib_4 \end{pmatrix} \quad (4\text{-}7)$$

Then, consider the following relationships:

$$\tau_4 = 1 - \tau_1 - \tau_2 - \tau_3 \quad (4\text{-}8)$$

$$Vt = Vb_1 + Vb_2 + Vb_3 + Vb_4 \quad (4\text{-}9)$$

Substituting equations 4-8 and 4-9 into 4-6, and upon inverting the resulting equation, the timing as a function of the cell voltages and inductor currents is obtained (equation 4-10). When used in a microcontroller, the inverted equation can help calculate the timing of the

MOSFETs. Chapter 5 (section 5-3) proposes a control system to calculate the inductor currents in closed loop.

$$\begin{pmatrix}\tau_1\\ \tau_2\\ \tau_3\end{pmatrix}=\frac{1}{Vt^3}\cdot\begin{pmatrix}Vt^2 & 0 & 0\\ -Vt^2 & Vt^2 & 0\\ 0 & -Vt^2 & Vt^2\end{pmatrix}\cdot\left(\begin{pmatrix}I_{L1}\\ I_{L2}\\ I_{L3}\end{pmatrix}\cdot R_L+\begin{pmatrix}Vb_1\\ Vb_1+Vb_2\\ Vb_1+Vb_2+Vb_3\end{pmatrix}\right) \tag{4-10}$$

Although it is relatively simple, this mathematical model considers that R_{ds} is much smaller than the inductor resistance. In fact, this is not always true, because high power inductors may have very low resistance, sometimes comparable to that of MOSFET resistance (about 5mΩ). Thus, this supposition makes the "first mathematical model" only an approximate estimation of the real behaviour of the equalizer. In fact, this was the case in the equalizer prototype used in this thesis, where the "first mathematical model" was found to have critical differences with the measurements. In order to obtain a better prediction, R_{ds} has to be considered as non-negligible. Consequently, merging equations 4-1, 4-2, and 4-3 results in equation 4-11, linking the inductor current, I_{Lx}, timing, t_x, and cell voltage, V_{Bx}. Finally, it can be concluded that equations 4-4 and 4-11 represent the "Second Mathematical Model."

$$\begin{bmatrix}\frac{Vt}{R_{ds}}-2I_{L1}-I_{L2} & I_{L2}+I_{L3} & I_{L3}\\ \frac{Vt}{R_{ds}}-I_{L1}+I_{L3} & \frac{Vt}{R_{ds}}+I_{L1}+I_{L3} & 2I_{L3}\\ \frac{Vt}{R_{ds}}+I_{L2}+2I_{L3} & \frac{Vt}{R_{ds}}+I_{L1}+I_{L2}+2I_{L3} & \frac{Vt}{R_{ds}}+I_{L1}+2I_{L2}+2I_{L3}\end{bmatrix}\cdot\begin{pmatrix}\tau_1\\ \tau_2\\ \tau_3\end{pmatrix}=\begin{bmatrix}\frac{Vb_1}{R_{ds}}+I_{L1}+I_{L2}+I_{L3}+I_{L1}\frac{R_L}{R_{ds}}\\ \left(\frac{Vb_1}{R_{ds}}+\frac{Vb_2}{R_{ds}}\right)+I_{L1}+2I_{L2}+2I_{L3}+I_{L2}\frac{R_L}{R_{ds}}\\ \left(\frac{Vb_1}{R_{ds}}+\frac{Vb_2}{R_{ds}}+\frac{Vb_3}{R_{ds}}\right)+I_{L1}+2I_{L2}+3I_{L3}+I_{L3}\frac{R_L}{R_{ds}}\end{bmatrix} \tag{4-11}$$

Upon analyzing equation 4-11, it is clear that the cell current is a complex function of the MOSFETs' gate timing and cell voltages. As aforementioned, this model can be also extended to 5 cells or more, although the mathematical complexity will grow

exponentially. The prototype presented in this thesis uses an implementation of the 5-cell model, in order to calculate timing as a function of cell voltages and desired current.

In the next section, a detailed comparison between the results obtained from the mathematical model, the simulations, and the experimental tests will be presented.

4.4 Comparative Study Between Simulations and Experimental Results

4.4.1 Prototype Evaluation

A prototype of the cell equalizer has been implemented using low-cost, standard components. A 5-cell instead of a 4-cell equalizer prototype has been built, in order to improve the cost effectiveness. The equalizer under test is connected to a pack of 20, 2.2Ah, Li-ion cells (size 18650), in a 4-parallel, 5-series arrangement [5]. The complete pack has 18V, 8.8Ah, and 500 mΩ equivalent series resistance, including current sensing resistors and cables. The objective of the test is to demonstrate the functionality of the equalizer, as well as measuring the efficiency and maximum current capabilities. The test is performed using a simple cell voltage control, much simpler than the SOC equalization, presented in chapter 5.

The functionality and the efficiency have been tested by creating an imbalance in the pack, discharging cell "2" by 6A, during 20 minutes (2Ah imbalance), and activating the equalizer in cell voltage equalizing mode. During run time, the equalizer will tend to make the voltage over each cell equal. The SOC equalizing mode, which has a better

dynamic response, is explored later, in chapter 5. The cell voltages during equalization are shown in Fig. 4-9, and the corresponding cell currents are shown in Fig. 4-10.

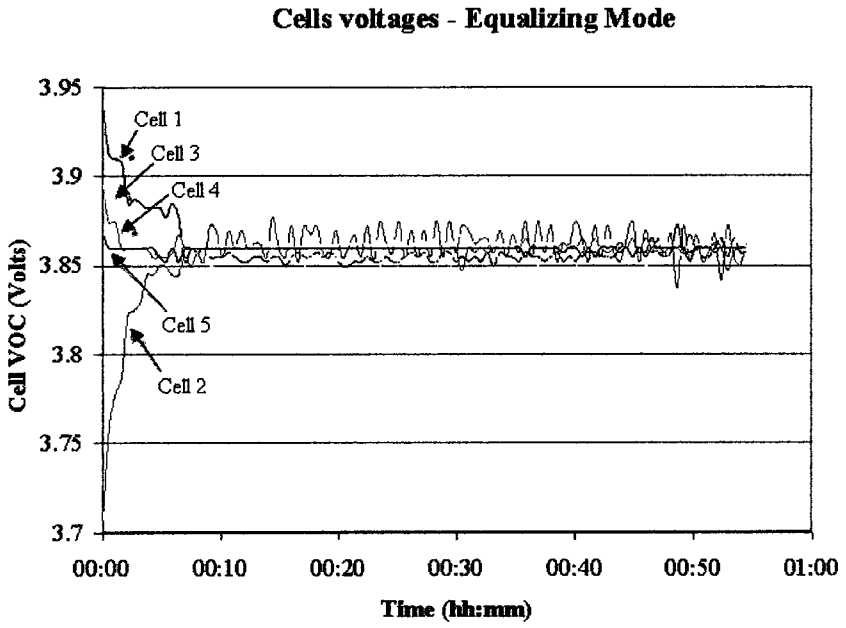


Fig. 4-9 Cell voltages during equalization, with 2Ah initial imbalance in Cell "2".

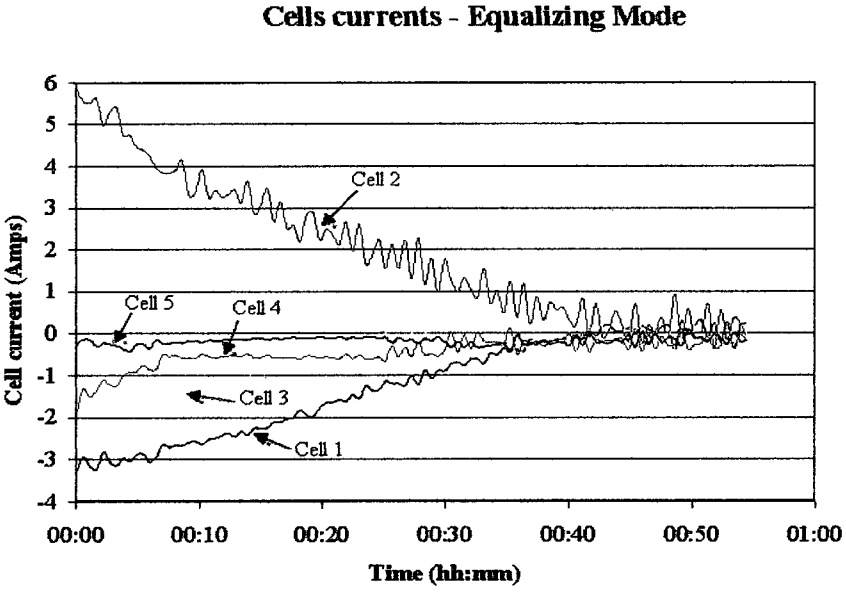


Fig. 4-10 Cell currents during equalization, with 2Ah initial imbalance in Cell "2".

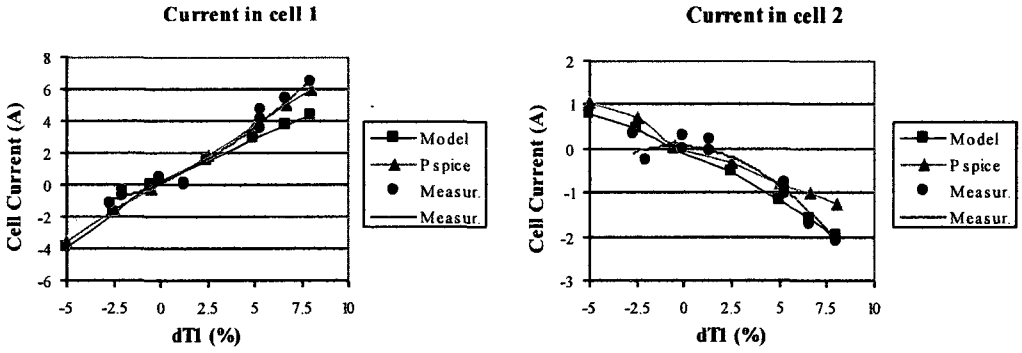
Integrating the current in cell #2, it can be appreciated in Fig. 4-10 that the equalized energy is about 2Ah, exactly the same amount lost during the forced imbalance. It is also notable that the equalizing current is not constant, but rather depicts a linearly decreasing behaviour, taking the equalizing process twice the time to equalize than if the current were constant at 6A. This is improved later, using SOC equalization, explained in chapter 5, where the SOC is equalized, instead of cell voltage. Hence, all the cells will tend to have the same voltage, but not necessarily the same SOC. Referring to Fig. 4-9; it can be appreciated that the voltages equalize particularly fast compared to the current in Fig. 4-10 (proportional to the SOC). In order to equalize the SOC as fast as possible, the equalizer should maintain 6A current for 20 minutes. This objective is not possible because of controller stability issues, and it will be explored in chapter 5. The noise in the cell voltage during this test was rather high (about 0.3%), which is higher than specified (0.1%). This is improved later, using the SOC equalization method.

4.4.2 Mathematical Model and Experimental Comparison

In order to evaluate the effectiveness and limitations of the mathematical model, its results will be compared to a 4-cell system, simulated in PSpice, using the most complete model of a typical low cost MOSFET, incorporating the experimental results at the same time. For this comparison, only the "Second Mathematical Model" will be used (equations 4-4 and 4-11), because, in this prototype, the assumptions considered in "First Mathematical Model" (equation 4-10), are not true (i.e. the MOSFETs R_{ds}, plus the trace impedances and capacitors' equivalent resistances, estimated in 20 mΩ, are not much smaller than the inductance equivalent resistance, about 10 mΩ), leading to critical errors in the "First Mathematical Model." The simulation studies also consider a small dead-

band time between modes, shown in the previous firing sequence (Fig. 4-4), in order to avoid shoot-through in the MOSFETs. The simulations also take in account the dynamic response of the MOSFETs, which, due to high switching frequency (higher than 100 kHz), will exhibit high switching losses. Because these losses are not considered in the mathematical model, some differences between the models and the simulations are expected. The mathematical model and the simulations also take into account the parasitic equivalent series resistances of several other components, such as filter capacitors, PCB traces, and cables. Finally, the measurements performed on the prototype will be compared against both calculations.

The average current through the cells is shown in Fig. 4-11, as a function of delta T1 (difference in timing of MOSFET 1, as a percentage of nominal time, corresponding to the time in Mode 1, as shown in Fig. 4-4), considering equal voltage in all cells. The dots represent the measured working points, and the corresponding lines represent the characteristic trend.



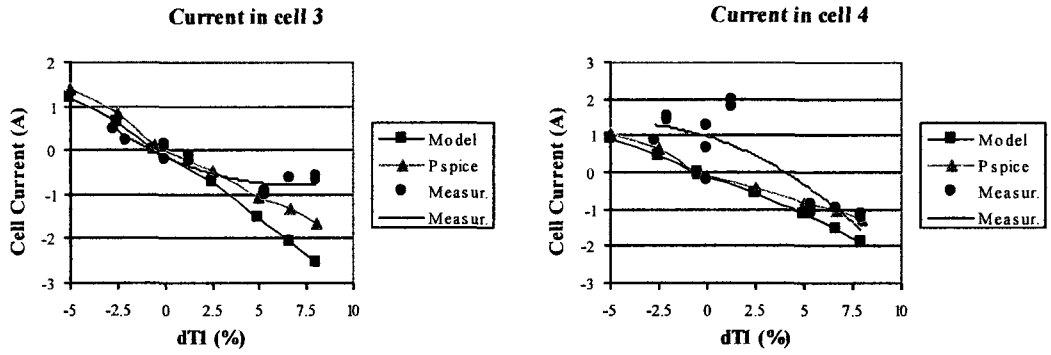


Fig. 4-11 Current through cells, with varying dt_1.

Secondly, the current through the cells are shown in Fig. 4-12 as a function of dt_2 (difference in timing of MOSFET 2, as a percentage of nominal time, corresponding to the time in Mode 2, as shown in Fig. 4-4), considering equal voltage in all cells.

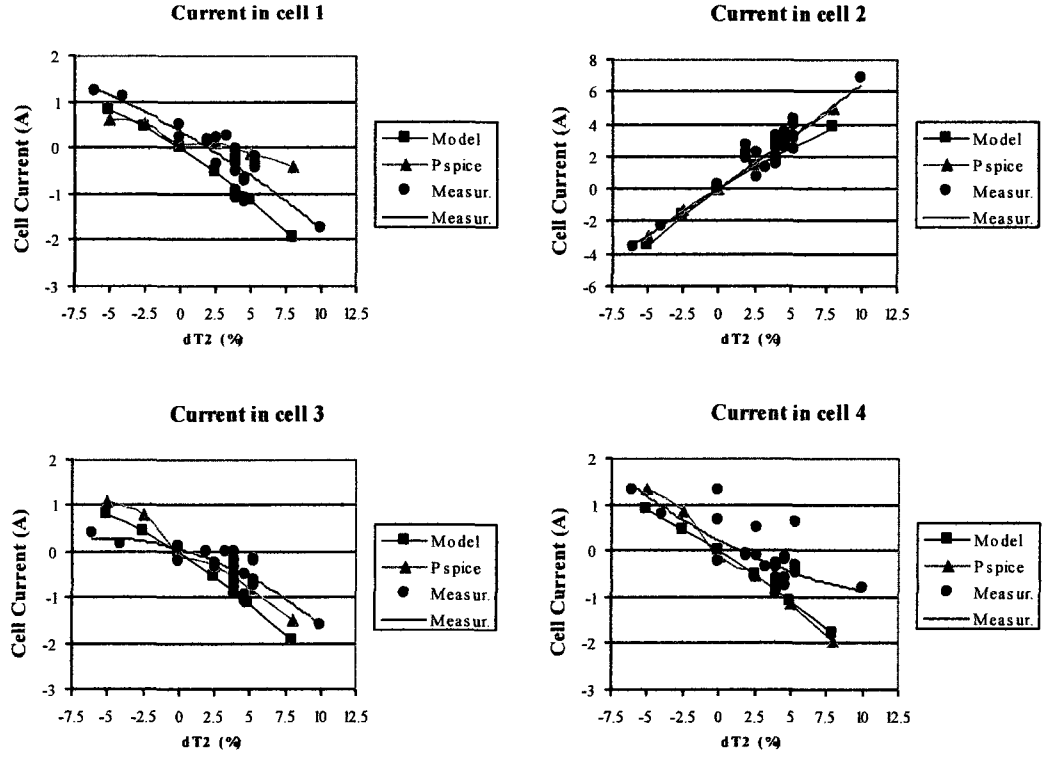


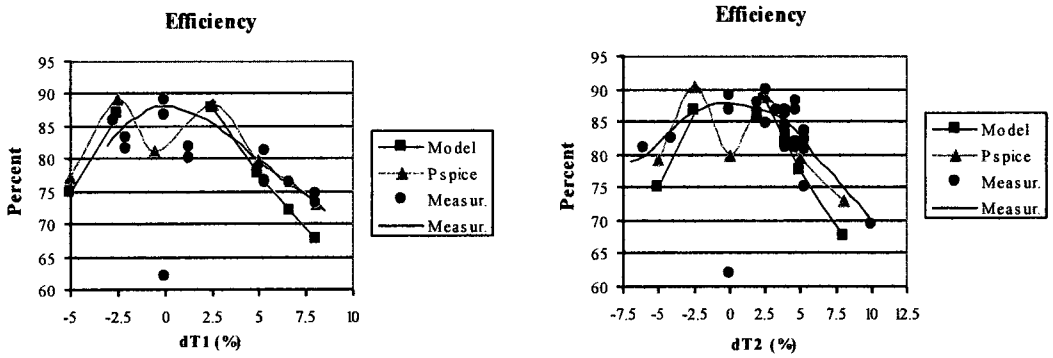
Fig. 4-12 Current through cells, with varying dt_2.

Because of the equalizer symmetry, the results of varying dt_3 and dt_4 (modes III and IV) are similar to dt_2 and dt_1, respectively.

The current through the cells in the prototype matches the mathematical model and the simulations fairly well. In particular, the current prediction of the developed model for a corresponding cell (for example, current through cell #2 by varying dt_2) is very precise, obtaining a mean squared error of less than 5%. The remaining differences between the *PSpice* simulations and the results from the model can be attributed to the fact that the mathematical model does not take into account the dead-time and the dynamic losses (the losses due to the switching) in the MOSFETs. It also does not take into account variation of MOSFET R_{dt} with temperature. In addition, it can be appreciated that a change in the timings of one MOSFET mainly affects the current over the corresponding cell, and to some extent, the currents over the other cells, in a less significant manner.

Because the equalizer works in closed loop, using the controller described in chapter 5 eliminates the relatively small difference between the model and the prototype. Thus, the final precision of the system remains unaffected. These errors are cancelled by the high open loop gain of the controller.

The total efficiency is also predicted with good precision. Fig. 4-13 shows the efficiency, defined as total losses divided by the total transferred power to the cells, as a function of dt_1 and dt_2.



(a) (b)

Fig. 4-13 Total efficiency (a) with varying dt_1, and (b) with varying dt_2.

From Fig. 4-13, it can be appreciated again that, for most parts, the mathematical model and the simulations match the measurements on the prototype. Furthermore, it may also be observed that the efficiency drops, when the timing becomes much different from the nominal timing. As determined previously in the design specifications (section 4.2), equalizing currents are usually lower than 5A (*dt* less than 5%). Thus, the efficiency is higher than 80% in this scenario. This is a rather good performance, considering the MOSFETs are working in hard switching. In fact, this performance is very close to the efficiency obtained by other equalizers using soft switching, such as the ones used in [24] and [29].

On the other hand, a large performance drop (down to 60% efficiency) is found near the neutral timing, when low current is transferred. At this working point, the equalizer fails to meet the specifications of 75% efficiency. This is due to the idle losses generated by the inductor current ripple, as explained in section 4.3.1. These losses are around 1 Watt, which affect the performance of the equalizer when the transferred current is less than 1 Amp (equivalent to 3.6 Watts). There are two ways to solve this issue: by increasing the inductance to reduce the current ripple, which increases the cost, size, and

weight, or by avoiding operation under 1 Amp current transfer, at the cost of allowing a small SOC difference between cells. The later method, called "deadband" method, is the solution used in this thesis, stopping the equalization when the difference of V_{OC} between cells is less than 0.1%, as explained in detail in chapter 5.

4.4.3 Comparison Between Typical Equalizer and Prototype Experimental Results

In order to compare the theoretical performance of both equalizers against the experimental measurements performed on the novel equalizer prototype, given the fact that the efficiency depends on the transferred power, several working points have been simulated to emulate a real scenario. Primarily, the simulations have been separated in 2 groups: transfer current to/from the first cell of the chain, summarized in Fig. 4-14, and to/from the second cell, summarized in Fig. 4-15. These batches of simulations have been discriminated, because they exhibit different performances. These groups of simulations of the novel equalizer have been called "A." The corresponding groups of simulations of the typical equalizer are called "B." Finally, the experimental test results for the proposed equalizer prototype will be called "C."

The "transferred power" is defined as the power provided to one or many cells, and the "total efficiency" is defined as the total equalizer losses over the transferred power from one or many cells (using the same components and switching frequency). Figs. 4-14 and 4-15 summarize the efficiency versus transferred power for the simulations on several working points for both the typical and novel equalizers, as well as the experimental measurements on the novel prototype. Fig. 4-14 shows the results with

varying dt_1, thus generating power transfer mainly in the first cell, while Fig. 4-15 shows the results with varying dt_2, which creates power transfer mainly in the second cell.

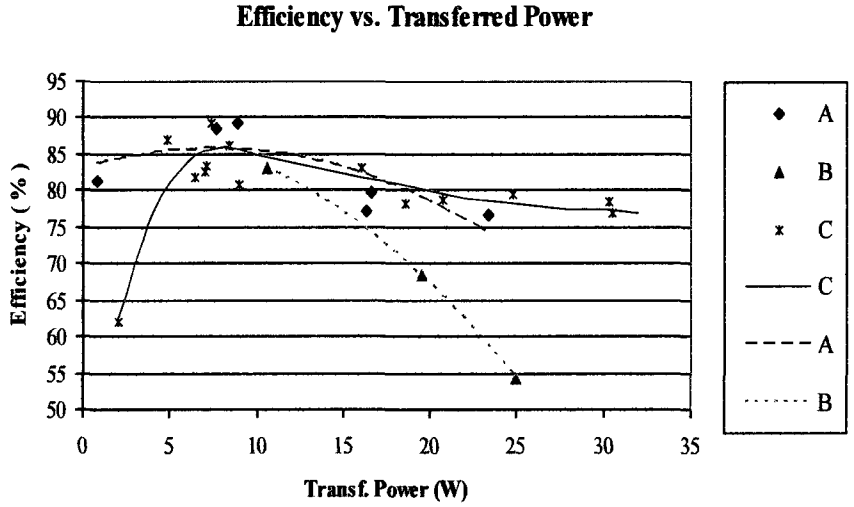


Fig. 4-14 Efficiency versus transferred power on first cell: (A) Simulation Novel EQ., (B) Simulation Typ. EQ., and (C) Experimental Measurements Novel EQ.

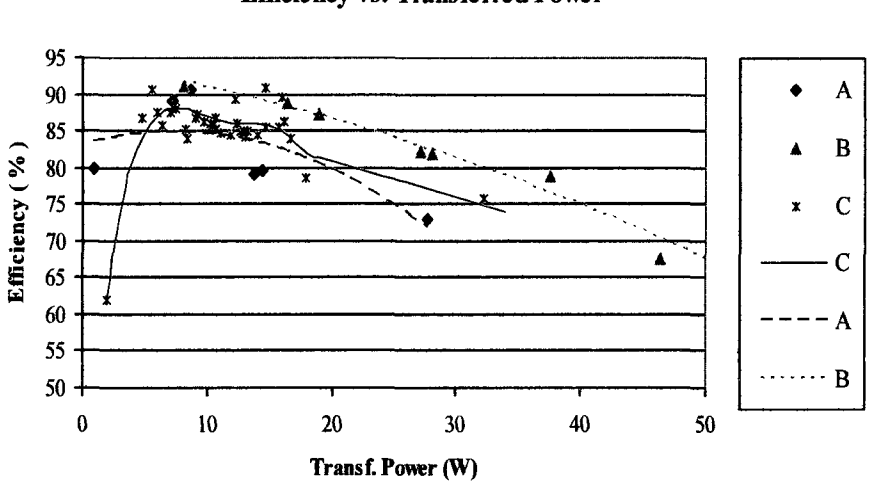


Fig. 4-15 Efficiency versus transferred power on second cell: (A) Simulation Novel EQ., (B) Simulation Typ. EQ., and (C) Experimental Measurements Novel EQ.

From Fig. 4-14, it can be observed that the best performance is achieved by the novel cell equalizer. Fig. 4-14 clearly indicates more than 80% efficiency for a power transfer of 5W-20W (equivalent to 1.4-5.5 Amps). It must be noted that there exist only minor differences between the simulation and experimental measurements in this range of power transfer. The only important difference is at low transferred power (less than 3W), whereby the efficiency falls under the specifications (approximately 60%). As explained before, this is due to the idle consumption of about 1W. This phenomenon was observed in the simulations as well as real measurements, due to the inductor current ripple flowing through the system.

In Fig. 4-15, there is a trivial difference in the performance, with the real measurements actually performing better than those predicted in the simulations. It presents the same worst-case performance (60% efficiency) at low transfer power. Comparing all cases, the worst efficiency (68%, at 20W, and 55%, at 25W) is observed in the case of the typical cell equalizer, draining from the first cell. In fact, this result was predictable, since the current must traverse more equalizer units to flow from the first cell to the last cell, as shown in the configuration of Fig. 2-3. In general, the new equalizer performs better in extreme-to-extreme cell power transfers, contrary to the typical equalizer, which theoretically performs slightly better in adjacent cell power transfers.

4.4.4 EQUALIZER CHAINING METHOD

Higher efficiencies of the equalizer in extreme-to-extreme cell power transfer cases are especially interesting for real EV/PHEV applications, where the utilization of long strings of cells is common. The proposed equalizer, using the chaining method introduced in Fig. 2-8, would be able to transfer power efficiently from one equalizer unit

to another. This is particularly true, given its properties of higher than 80% efficiency during power transfers from extreme-to-extreme cells. This is in contrary to the typical cell equalizer, where the average efficiency is 15% lower than that of the novel equalizer. Thus, the novel equalizer is capable of distributing excess energy among equalizer units in a more efficient manner than the typical equalizer. Fig. 4-16 depicts a possible method to extend the equalization to a long chain of cells. Fig. 4-16 also shows an example of current transfer between equalizers.

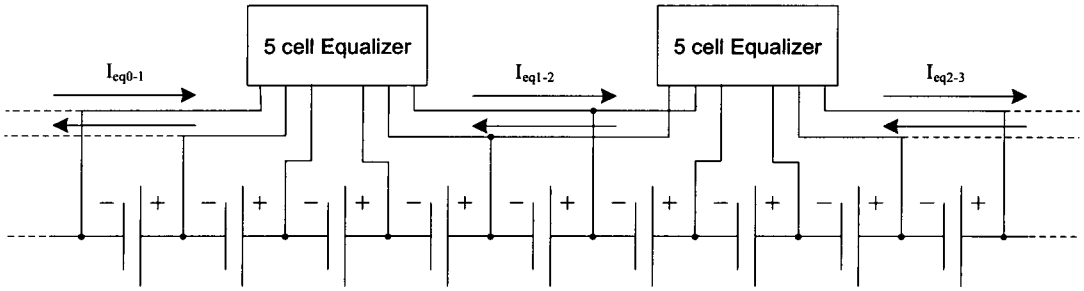


Fig. 4-16 Equalizer chain current transfer.

Basically, each equalizer unit is connected to the next one by sharing the last cell. When one equalizer needs to transfer excess power to the other equalizer, first, it sends it to its last cell, after which the next equalizer takes power from its first cell. A possible way to calculate the amount of current transfer includes each equalizer communicating their average cell SOC to a central controller, which decides the amount of current that the equalizers should transfer between each other.

The total system efficiency is dependant on the amount of equalizer units that the energy must traverse, which is totally dependent on the capacity dispersion of the cells. Supposing a 5% Gaussian distribution in the battery cell capacities, about 20 cells out of 100 cells have more than ± 3% dispersion. That is about one cell with high capacity

dispersion per equalizer unit. Hence, in a typical simulated case, the energy did not have to traverse more than 1 unit. Rather, the energy only traversed partially to the next unit. In this case, depending on the capacity distribution of the cells, the total system efficiency is found to be about 75%, which satisfies minimum original specifications. This is clearly better than the total system efficiency obtained by the typical equalizer, which is found to be about 68%.

4.5 SUMMARY

Overall, it can be safely inferred that the proposed novel cell equalizer prototype performs as predicted, obtaining a 90% peak efficiency at 7W power transfer, and 77% at 30W transfer, as shown in Figs. 4-12 and 4-13. There is a good agreement between the efficiencies observed in the model, simulations, and the experimental results. However, as aforementioned, there exists an exception at low power transfer (less than 3W), where the high losses (about 1W) caused by the inductor current ripples, affect the overall efficiency. This is the only operating point where the efficiency (60%) is worse than the specifications (75%). These losses can be eliminated by turning off the equalizer when the transferred power is so small that it does not justify the losses, as described in chapter 5.

It is worthwhile mentioning here that the maximum equalizer current is higher than the specifications (7 Amps). However, the range of equalizing current, where the efficiency is good, is limited from 1 Amp to 5 Amps, in accordance with the specifications.

The equalization test performed in section 4.3.1 proved not to be up to expectations. This is because the test depicted a long equalizing time (40 minutes, instead

of the ideal 20 minutes). It also depicted a noise of 0.3%, instead of 0.1%. It is worth pointing out that this test used cell voltage equalization instead of SOC equalization. The controller presented in chapter 5 is developed to improve these issues.

The cost targets are met without difficulty, as demonstrated in section 3.2.2. The cost achieved is $4.00/cell, against a maximum of $6.00/cell. This is considered in the economic analysis, in chapter 3. The equalizer includes the communication capabilities demanded in the specifications.

It can be clearly deduced that the novel cell equalizer outperforms the typical cell equalizer, when the power has to be distributed from the first to the last cell of an equalizer module. This is particularly useful in very long battery cell strings, using the method described in section 4.4.4. The difference in extreme-to-extreme cell performance leads to a major difference in total system efficiency of about 75% (for the novel equalizer), against 68% (for the typical equalizer), using a 5% Gaussian dispersion in the battery cell capacities.

CHAPTER 5

CONTROLLER DESIGN FOR THE NOVEL PHEV/EV BATTERY CELL EQUALIZER

5.1 INTRODUCTION

In the previous chapters, the topological layout and design of a novel cell equalizer configuration was presented, which is capable of meeting the performance and cost targets for PHEV/EV applications. As aforementioned, the only practical weakness of this configuration is the complex control algorithm, especially if SOC equalizing is desired. The purpose of this chapter is to introduce a new and simplified control scheme, based on open-circuit voltage estimation, for the novel cell equalizer configuration, fulfilling expectations of low cost, large currents, and high efficiency. Practical issues, such as limitations on maximum and minimum cell voltage, noise, errors in quantization, and modelling, among others, are explored. It is critical to point out that the designed control scheme is not necessarily limited to the novel cell voltage equalizer configuration, but may also be applicable to other equalizer topologies, like those presented in [20]-[25]. Finally, a comprehensive comparison between theoretical test results and practical equalization test results is presented.

5.1.1 CONTROLLER FUNCTIONS

The on-board controller has several responsibilities, some of them exclusively for the proposed novel cell equalizer configuration, such as:

(a) Real-time measurement of cell voltages: The controller measures the voltage of each cell individually, at a certain sampling frequency. In the prototype used in this thesis, this time is set at 1 second.

(b) Computation of the SOC of each cell: Using a method proposed later in this chapter, the controller calculates the SOC based on cell voltages.

(c) Calculation of equalizing current: Considering diverse factors, such as equalizer efficiency and maximum cell ratings, the controller estimates the desired equalizing current.

(d) MOSFET timing calculation: Based on the mathematical models, presented in 4.3.2, the controller calculates the MOSFET gate timings, to obtain desired equalizing current.

(e) Current measurement: Alternatively, the cell equalizer unit may include a cell current measurement option, to improve the equalizing and the SOC estimation precision. This can be replaced with single current measurement per battery pack, and the single cell current can be mathematically estimated using the mathematical model presented in section 4.3.2.

(f) Safety monitoring: In addition, the controller monitors each cell individually, including temperature, investigating voltage and internal resistance anomalies, and may also be responsible for state of health (SOH) monitoring [11], [33]. This provides valuable information that leads to warnings, or eventually a system shut down. Safety monitoring, although overviewed in section 1.3.1, is not covered in the scope of this thesis.

(g) Communication: The controller shares information with all the controllers in each chained equalizer [11] and eventually, with the main controller, in order to allow better current sharing and distribution. The multiple equalizer chain management and current distribution is not part of this thesis, and could be explored as future work.

All the above tasks are performed real-time, in an inexpensive, low-consumption microcontroller through simplified, yet precise methods, as explained in the ensuing sections. These methods include estimating cell open circuit voltage (V_{OC}) and internal resistance. Due to the high interaction between the control block and the battery model, the latter will be explored in detail in the next section.

5.2 LITHIUM-ION CELL ELECTRICAL MODEL

There exist several equivalent models for batteries, with varying complexities [30]-[33]. In [30], the V_{OC} error is about 0.1%, and in [32]-[33], the SOC error is about 5%. All values are consistent with the error obtained by the method described later in this thesis. For the equalizer controller explored in this chapter, the battery cell equivalent electrical model presented in [30] has been chosen, because of its simplicity and high precision in the range of state of charge (SOC) typically used in electric vehicles (from 30% to 80% SOC) (as highlighted in chapter 3). The equivalent model of a battery cell is shown in Fig. 5-1.

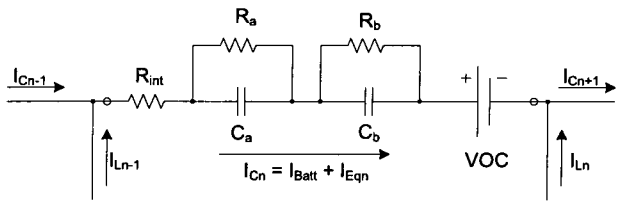


Fig. 5-1 Equivalent electrical model of a battery cell.

In the equivalent model of Fig. 5-1, R_{int} represents the total steady state cell internal resistance, including connections; R_a, R_b, C_a, and C_b model the dynamic response, in the case tested in this thesis with a time response of 3 seconds and 50 seconds; the open circuit voltage (V_{OC}) has a non-linear relationship with SOC, temperature, and age, and represents chemically stored energy. The internal resistance is also dependent on SOC, temperature, and age. Hence, internal resistance cannot be considered as a constant. I_{Cn} is the cell current, which comprises of I_{Bat} (total battery current) and I_{Eqn} (equalizing current). The battery used in this prototype has 4, 2.2Ah lithium-ion (Li-ion) cells connected in parallel, 5 groups of 4 cells in series, totalling 8.8Ah, and 18V nominal voltage. Fig. 5-2 shows the voltage in slow discharge of this Li-ion cell, practically equal to the V_{OC}. Fig. 5-3 plots the variation of internal resistance as a function of the SOC.

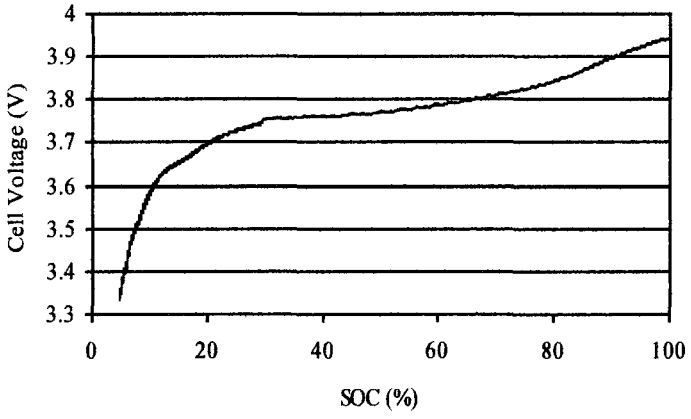


Fig. 5-2 Cell voltage in slow discharge (V_{OC} versus SOC).

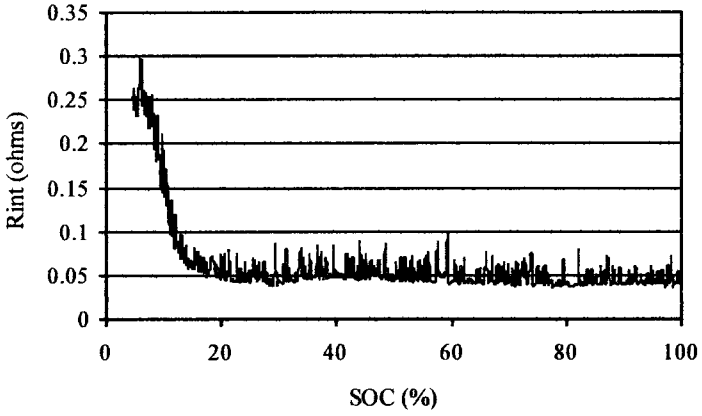


Fig. 5-3 Internal resistance versus SOC.

The dynamic response equivalent capacitors and resistors, R_a, R_b, C_a, and C_b, although not constant, remain stable in a good range of SOC, as can be appreciated through measurements performed in [30]. Fig. 5-3 also provides an estimate of the SOC-region where the equivalent model is valid (from 100% to 15% SOC).

5.2.1 V_{OC} DETERMINATION

The most precise technique, yet not practical, to find the V_{OC} of a battery, is to disconnect the current for a long period of time, in order to pass through the transient response time. In fact, the battery will be loaded according to the user demand. The only controllable load is the equalizer: equalizing current can be stopped for short periods of time, in order to estimate the V_{OC}, after which the equalizing process can be resumed. The remaining issue is settling time necessary to achieve the steady state voltage, which is too long for a feasible battery equalizer (from tens of seconds to several minutes), as shown in Fig. 5-4.

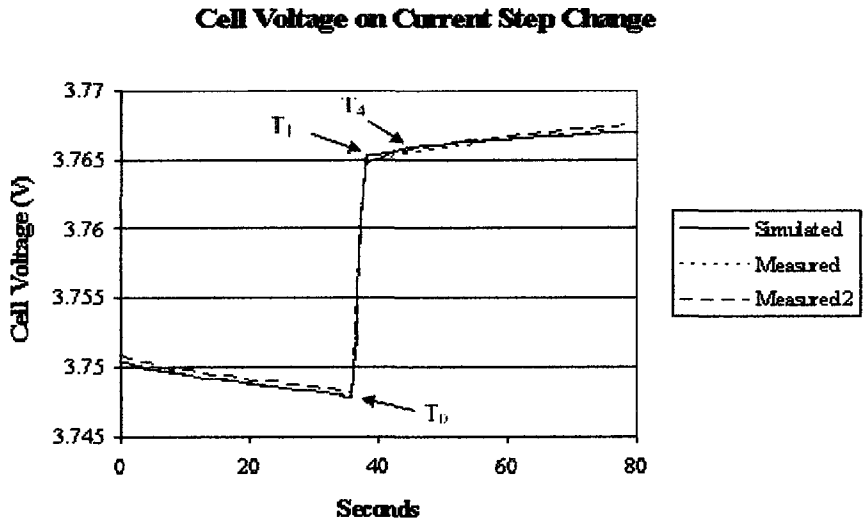


Fig. 5-4 Cell voltage during a step change in current.

To solve this issue, a simple method for estimating the V_{OC}, with only short time periods of no equalizing current, is presented in this chapter. Because of the long settling time of the battery voltage, several seconds are necessary to make an accurate estimation. In this case, only 4 seconds was enough for the equalizer controller to obtain a V_{OC} estimation error of less than 1%. In fact, there are several methods to calculate battery model parameters, even without forcing variations in current, like those presented in [31]-[33]. However, the computation power required for these tasks is extremely demanding for an inexpensive microcontroller, like the one used in this application. Hence, simplified versions of the methods presented in [31]-[33] must be developed, before they can be utilized for low cost applications, such as the one presented in this thesis.

5.2.2 V_{OC} ESTIMATION ALGORITHM

Based on the battery model described in section 5-2, it is possible to mathematically calculate the voltage on a battery cell (V_b) during a forced step change of

current, such as the one generated when the equalizer turns off, using the following equation:

$$V_b = VOC + R_{\text{int}} \cdot (I_{Bat} + I_{Eq} \cdot \delta_0) + R_a \cdot I_{Eq} \cdot e^{-\frac{t}{T_a}} + R_b \cdot I_{Eq} \cdot e^{-\frac{t}{T_b}} \quad (5\text{-}1)$$

Here, V_b is the instantaneous cell voltage, starting at T_0, I_{Eq} is the equalizing current, active only at T_0 and interrupted after T_1, I_{Bat} is the battery pack current, R_{int} is the static internal resistance, R_a, R_b are the dynamic resistances, and T_a, T_b are the dynamic time constants. R_{int}, R_a, and R_b are considered unknown, while T_a and T_b are constants. R_a and R_b are considered to be related and proportional. For example, in calculations made from real measurements, observed from the battery cells used in this prototype, $R_a/R_b \approx 0.1$, T_a = 3 sec, and T_b = 50 sec. The voltage samples (Fig. 5-4) are observed at T_0, (when I_{Eq} is still active), at T_1 (the first second after $I_{Eq} = 0$), and at T_4 (the fourth second after $I_{Eq} = 0$). The cell equalizer current and total battery current are used in the algorithm to determine the estimated V_{OC}. Taking the above points into consideration, V_b can be approximated as:

$$V_b \cong VOC + R_{\text{int}} \cdot (I_{Bat} + I_{Eq} \cdot \delta_0) + R_b \cdot I_{Eq} \cdot k_t \quad (5\text{-}2)$$

$$k_t = \frac{R_a}{R_b} \cdot e^{-\frac{t}{T_a}} + e^{-\frac{t}{T_b}} \quad (5\text{-}3)$$

Knowing I_{Bat}, I_{Eq}, V_b, and using the 3 equations generated from (5-2), by replacing t by T_0, T_1, and T_4, the unknown variables R_b, R_{int} and finally, V_{OC} can be calculated. It must be pointed out that k_t is previously stored in a lookup table, based on values that are

specific for a particular type of battery cell. The resulting 3 system of equations are easy to solve, reducing the computational power demand.

The performance of the V_{OC} estimator has been validated using the following experimental algorithm: The cell is loaded using a known current. Thereafter, the load is interrupted, until the cell voltage reaches a constant value. This value (the actual V_{OC}) is compared with the V_{OC} estimated using the previous method. Fig. 5-5 shows the error between the estimated V_{OC} and the measured V_{OC} as a function of the SOC. As the SOC approaches 0% (discharged cell), the previous assumptions become less accurate.

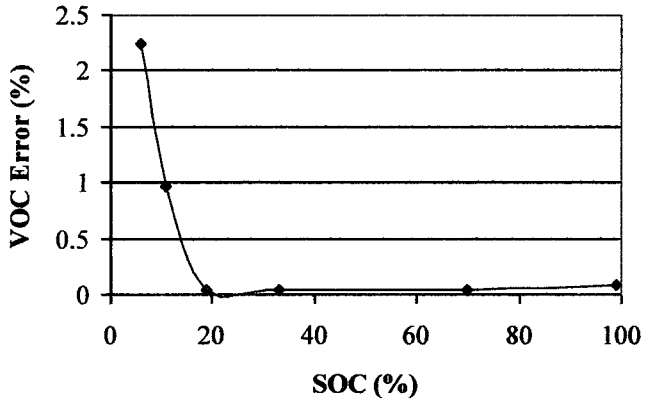


Fig. 5-5 V_{OC} estimation error versus SOC.

Fig. 5-5 points out an obvious limitation of the method, wherein closer to 10% of SOC, the error sharply increases, due to a very significant change in the equivalent dynamic resistances and time constants, nearing the full discharge state of the cell. It may be inferred that the method is accurate to 0.1% in the 20% to 100% SOC range. Outside this SOC range, the method becomes ineffective, due to parameter dependency on the SOC. Nevertheless, for PHEV/EV applications, where the longevity of battery operation is important, this is not considered to be a major issue, because the battery is never discharged under 30% SOC, as explained earlier, in section 3-3. On the other hand, an

error of 0.1% in V_{OC} corresponds to an error of 1% to 3% in SOC (using Fig. 5-2, V_{OC} versus SOC), which corresponds with the error obtained by [32]-[33]. This error generates undesired differences in cell equalization. For EV/PHEV applications, suitable calibration of the equalizer is necessary during the manufacturing process, to avoid additional errors due to voltage measurements (0.1%) and voltage reference (0.05%). Without calibration, the absolute overall error could increase to about 0.25%, corresponding to a maximum error of 7.5% in SOC, which is very high for this application.

In the next section, the V_{OC} estimation method is applied to the novel battery cell equalizer control system.

5.3 PROPOSED CELL EQUALIZER CONTROL STRATEGY

The cell equalizer controller is composed of several blocks: cell V_{OC} estimation, overviewed in the previous section; V_{OC} difference calculation, which is used as an error signal; a proportional-integral block (PI), that will affect the error signal; desired cell current calculation, based on the PI output; cell current and voltage limiter; and finally, the timing calculations for the MOSFETs, calculated using equations 4-4 and 4-6. Fig. 5-6 shows the equalizer controller block diagram, while Fig. 5-7 shows the equalizer controller details.

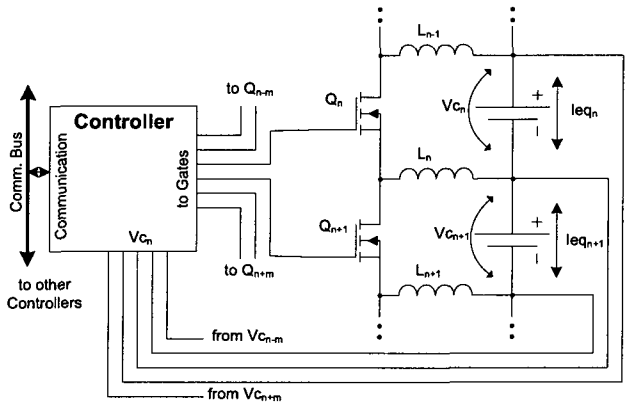


Fig. 5-6 Equalizer controller block diagram.

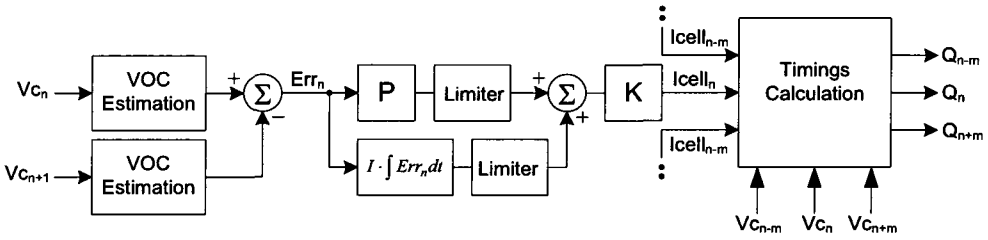


Fig. 5-7 Equalizer controller details.

As mentioned in the previous section, the V_{OC} estimator needs to interrupt the equalizing current for at least 4 seconds, in order to record the necessary measurements of cell voltage. The V_{OC} of each cell is estimated using cell voltage measurements, cell equalizing currents, provided by the equalizer hardware (or from estimations), using the cell voltages and the load current, and finally, using the load current, taken from the system controller. The objective is to equalize the V_{OC} of each cell, so that the difference is used as the error signal, as represented in equation 5-4.

$$Err_n = Vc_{n+1} - Vc_n \tag{5-4}$$

Because these errors are sampled at a very slow rate (from 30 seconds to several minutes), the error signal is passed through a PI block, to avoid stability issues, and to improve the steady state error, as represented in equation 5-5. An optional derivative component in the controller is not used here, because of the inherent noise related to V_{OC} estimation, which would be amplified to unacceptable levels.

$$PIerr_n = Err_n \cdot P + I \cdot \int Err_n dt\Big|_{resetable} \tag{5-5}$$

Once the complete equalization is obtained, i.e. the error signals are very close to zero, the equalizer can be turned off, to reduce consumption, and the error integration is reset. This method can be termed as the "Dead-Band" method. Thereafter, the desired cell currents are calculated based on (5-6) and (5-7).

$$Ic_{n+1} - Ic_n = k * PIerr_n \tag{5-6}$$

$$\sum_n Ic_n = 0 \tag{5-7}$$

Safety is insured by limiting the cell currents to a maximum acceptable level by each cell, and limiting the maximum cell voltage, using the internal resistance obtained from V_{OC} estimation. Additional warnings are issued when the cell voltage is too low or the temperature is too high.

Additional precautions should be taken, such as maximum cell temperature, maximum equalizer current, and balance between equalizing time and efficiency. Fig. 5-8 shows the efficiency of the equalizer versus the transferred power (section 4.4.3). It is clear that a medium range of equalizing current (from 5W to 20W of transferred power,

equivalent to 1.5A to 5A) is desired, when high efficiency is critical. The average efficiency in this range is about 85%.

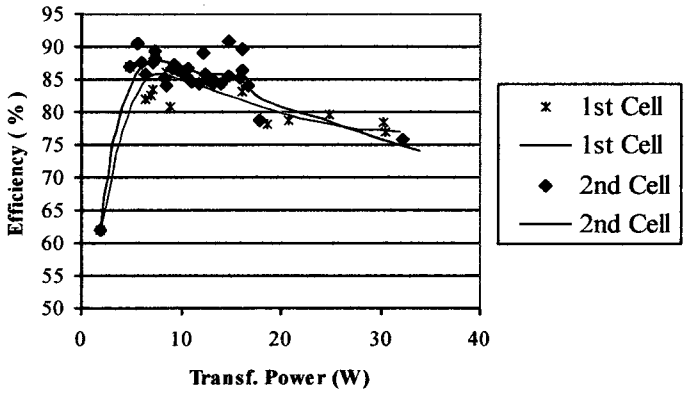


Fig. 5-8 Equalizer efficiency vs. transferred power.

Based on the above considerations, the desired cell current and instantaneous cell voltage values are inserted into equations 4-4 and 4-6, in order to obtain the timings of the MOSFETs. To avoid shoot through in the MOSFET chain, minimum turn-off times (50% of the typical τ_n time), maximum turn-off times (150% of the typical τ_n time), and a guard time (of 50 ns) must be enforced in each MOSFET. If the calculated timing violates these limits, then the desired cell currents are reduced, and the timing is recalculated, until an allowed timing scheme is obtained.

In the next section, an appropriate controller for the proposed novel equalizer will be modelled and the stability of the system will be evaluated, considering the proportional and integral coefficients and sampling time as major parameters.

5.4 PROPOSED CELL EQUALIZER CONTROLLER MODELING

Several simplifications must be applied in order to evaluate the controllability, reduce the amount of variables, as well as linearize the proposed non-linear system. These tasks are explained in detail in the ensuing sections.

5.4.1 CELL EQUALIZER CONTROL SYSTEM SIMPLIFICATION

The first case of simplification is to consider the fact that the equalizer will transfer energy from only one cell to another. The model is exactly that of a basic inductive equalizer, reviewed in 2.4.1. The system will then be simplified to "one input-one output," as shown in Fig. 5-9.

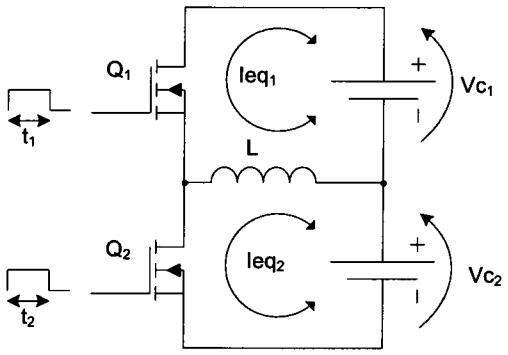


Fig. 5-9 Simplified "one input-one output" equalizer model.

Considering the duty cycle ($\tau_n = t_n/T$) of each MOSFET, which are complementary to each other ($t_1 + t_2 = T$), the equalizer can be seen as a DC/DC converter, satisfying the operating rules of an ideal transformer. This is shown in Fig. 5-10, where the primary is connected to cell #1 and the secondary is connected to cell #2. Voltage ratio (n) is equal to the duty cycle ratio, τ_1/τ_2, as summarized in equation 5-8. Resistor, R, represents the added internal resistance of the cells, cables, PCB traces, and

conduction losses in the DC/DC converter. Considering ideal converter efficiency, the current ratio is expressed as shown in equation 5-9.

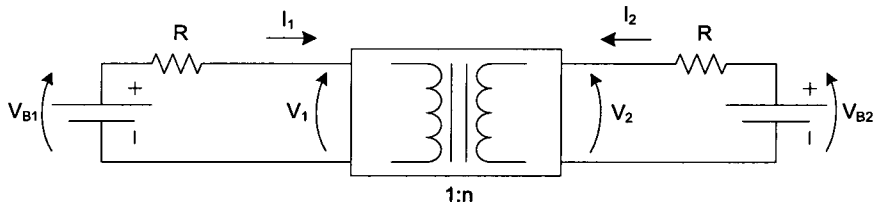


Fig. 5-10 Simplified electrical model of the equalizer.

Voltage ratio can be written as:

$$\frac{V_2}{V_1} = \frac{\tau_1}{\tau_2} = \frac{\tau_1}{1-\tau_1} = n \tag{5-8}$$

Current ratio can be written as:

$$\frac{I_2}{I_1} = -\frac{\tau_2}{\tau_1} = \frac{\tau_1 - 1}{\tau_1} = -\frac{1}{n} \tag{5-9}$$

Considering the fact that V_{OC} sampling frequency is about 1 minute, and the first time constant is about 3 seconds, the dynamic model of the cell, as shown in Fig. 5-1, can be reduced to the model of Fig. 5-11. In the reduced model, the first time constant is ignored. The cell V_{OC} can be considered as linear, particularly from 30% to 70% SOC. R_{int} can be considered as constant, as was depicted in Fig. 5-2. Hence, the battery cell can be modelled as a simple capacitor.

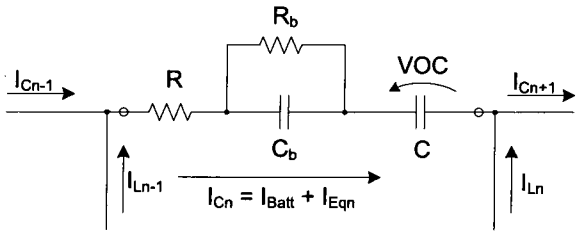


Fig. 5-11 Simplified electrical cell model.

The V_{OC} estimation method, as discussed in section 5.2.2, is theoretically capable of obtaining V_{OC}, independent of the effects caused by R_b and C_b. In fact, there is always a noteworthy V_{OC} estimation error, mainly due to a miscalculation of R_b. This error can be modelled as a capacitor-resistor pair (R_2-C_2), replacing the R_b-C_b pair. Because their time constant (50 seconds) is too close to the sampling frequency, T_S (30 to 120 seconds), it cannot be ignored from the stability analysis.

The controller error signal is obtained from the difference between both the estimated V_{OC} values. Depending on the difference between the R_b-C_b pairs of each cell, 2 possible electrical models can be analysed; one case with a remaining V_{OC} estimation error (R_2-C_2) in series with cell #1, as shown in Fig. 5-12, and another case in series with cell #2, as shown in Fig. 5-13.

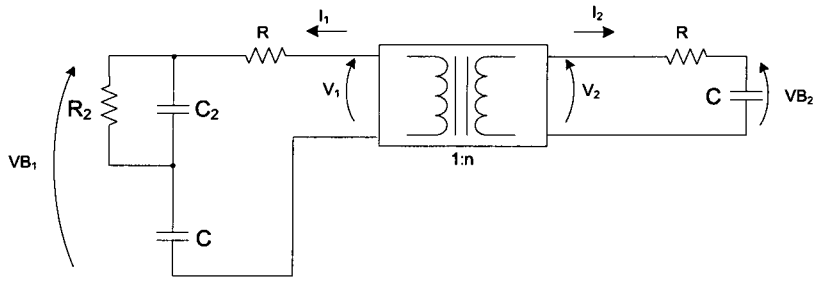


Fig. 5-12 Simplified electrical plant model, with V_{OC} error dominant in cell #1.

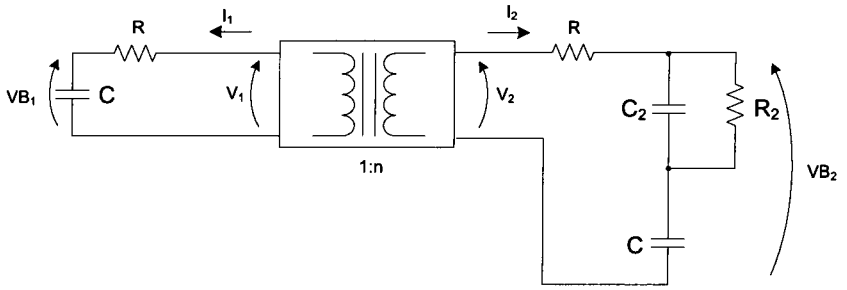


Fig. 5-13 Simplified electrical plant model, with V_{OC} error dominant in cell #2.

VB_1 and VB_2 are the instantaneous V_{OC} estimations. The controller should be stable in both cases, considering the sampling time of the V_{OC}, $R_2 << R$, and $C_2 << C$. In the next section, the mathematical model for both cases will be derived.

5.4.2 Mathematical Derivation of the Cell Equalizer Controller

(a) Plant modelling for first case, shown in Fig. 5-12.

Considering V_{OC} as the initial open circuit voltage, the voltages for the first circuit, using Laplace transform, can be expressed as:

$$V_1 = \frac{VOC_1}{S} + \frac{I_1}{S \cdot C} + I_1 \cdot R + \frac{I_1 \cdot R_2}{(1 + S \cdot R_2 \cdot C_2)} \tag{5-10}$$

$$V_2 = \frac{VOC_2}{S} + \frac{I_2}{S \cdot C} + I_2 \cdot R \tag{5-11}$$

$$VB_1 = \frac{VOC_1}{S} + \frac{I_1}{S \cdot C} + \frac{I_1 \cdot R_2}{(1 + S \cdot R_2 \cdot C_2)} \tag{5-12}$$

$$VB_2 = \frac{VOC_2}{S} + \frac{I_2}{S \cdot C} \tag{5-13}$$

Thereafter, considering the DC/DC transformer ideal equations, as defined in equations 5-8 and 5-9, the following expression can be obtained for computing current through cell #1 (Ic_1):

$$Ic_1 = \frac{(-VOC_1 \cdot n + VOC_2) \cdot C \cdot (1 + SR_2C_2) \cdot n}{(n^2 + n^2 S \cdot R_2C_2 + n^2 S \cdot (R + R_2)C + n^2 S^2 RC \cdot R_2C_2 + 1 + S \cdot R_2C_2 + S \cdot RC + S^2 RC \cdot R_2C)} \tag{5-14}$$

R_2 is much smaller than R, and in the stability analysis of this case, V_{OC1} is considered equal to V_{OC2}, which is the point where the system is nearly equalized. Hence, the following equation can be obtained:

$$Ic_1 = \frac{VOC \cdot (1-n) \cdot C \cdot (1 + SR_2C_2) \cdot n}{(1 + S \cdot R_2 \cdot C_2) \cdot (1 + S \cdot R \cdot C) \cdot (1 + n^2)} \tag{5-15}$$

(b) Plant modelling for second case, shown in Fig. 5-13.

Using Laplace transform, the voltages for the second case, can be expressed as:

$$V_1 = \frac{VOC_1}{S} + \frac{Ic_1}{S \cdot C} + Ic_1 \cdot R \tag{5-16}$$

$$V_2 = \frac{VOC_2}{S} + \frac{Ic_2}{S \cdot C} + Ic_2 \cdot R + \frac{Ic_2 \cdot R_2}{(1 + S \cdot R_2 \cdot C_2)} \tag{5-17}$$

$$VB_1 = \frac{VOC_1}{S} + \frac{Ic_1}{S \cdot C} \tag{5-18}$$

$$VB_2 = \frac{VOC_2}{S} + \frac{Ic_2}{S \cdot C} + \frac{Ic_2 \cdot R_2}{(1 + S \cdot R_2 \cdot C_2)} \tag{5-19}$$

Again, considering the DC/DC transformer ideal equations, as defined in equations 5-8 and 5-9, the following expression can be obtained for computing current through cell #1 (Ic_1):

$$Ic_1 = \frac{(-VOC_1 \cdot n + VOC_2) \cdot C \cdot (1 + SR_2C_2) \cdot n}{(n^2 + n^2S \cdot R_2C_2 + n^2S \cdot RC + n^2S^2RC \cdot R_2C_2 + 1 + S \cdot R_2C_2 + S \cdot (R + R_2)C + S^2RC \cdot R_2C)} \tag{5-20}$$

As R_2 is much smaller than R, and in the stability analysis of this case, V_{OC1} is considered equal to V_{OC2}, which is the point where the system is nearly equalized. Hence, the equation for the second case (5-20) becomes exactly the same as the one for the first case (5-15). This equation represents the response of the overall system.

(c) Controller modelling for first case, shown in Fig. 5-12.

For the purpose of this thesis, n is defined in equation 5-8, as a voltage gain of V_2/V_1, the nominal value of which is 100%.

The error signal is taken from the difference between the 2-cell V_{OC} estimation (equation 5-21). The V_{OC} estimation method inherently possesses a slow first order sample and hold, which is about 1 minute of sampling time (T_s). The gain, n, is kept constant during this sampling time. For the controller model, a simple PI is used, considered here without the limiters, as shown in Fig. 5-14.

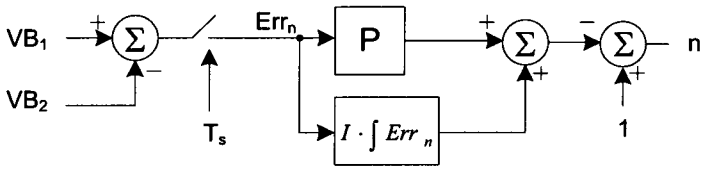


Fig. 5-14 Details of the controller.

The complete block diagram for the control analysis is shown in Fig. 5-15. A δ-signal applied to the input represents the initial error due to an unbalance of the cells. Conceptually, the transfer function represents the response of the error (the difference between the V_{OC} of each cell) to an initial unbalance.

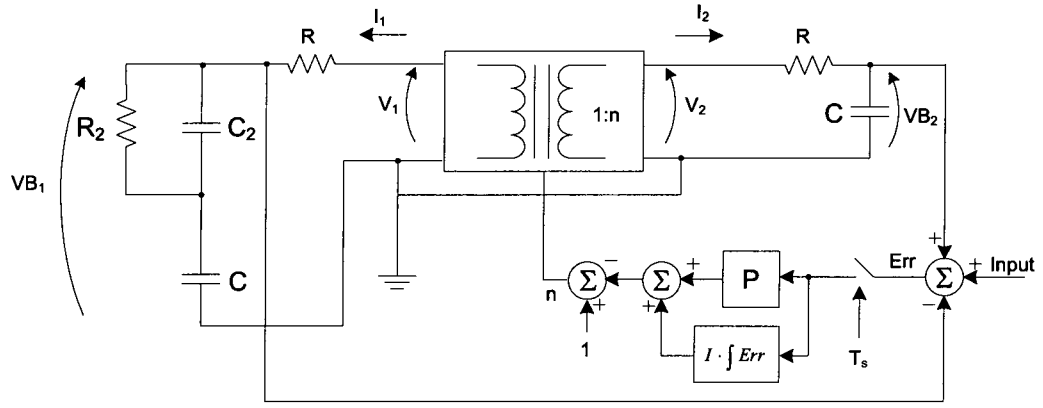


Fig. 5-15 Complete system diagram.

Considering the error signal, before sampling:

$$Err = VB_2 - VB_1 \tag{5-21}$$

Thereafter, substituting VB_1 (using equation 5-12) and VB_2 (using equation 5-13) for the first case, the following error value can be obtained:

$$Err = -Ic_1 \cdot \left[\frac{1+\frac{1}{n}}{SC} + \frac{R_2}{(1+S \cdot R_2 \cdot C_2)} \right] \tag{5-22}$$

Substituting Ic_1, obtained from equation 5-15:

$$Err = \frac{-VOC \cdot C \cdot (1+SR_2C_2)}{(1+S \cdot R_2 \cdot C_2) \cdot (1+S \cdot R \cdot C)} \cdot \left[\frac{(1-n) \cdot (1+n)}{(1+n^2) \cdot SC} + \frac{(1-n) \cdot n \cdot R_2}{(1+n^2) \cdot (1+S \cdot R_2 \cdot C_2)} \right] \tag{5-23}$$

(d) Controller modelling for second case, shown in Fig. 5-13.

Repeating the procedure for the second case, and substituting equation 5-21 with equations 5-18 and 5-19, the following error value can be obtained:

$$Err = -Ic_1 \cdot \left[\frac{1+\frac{1}{n}}{SC} + \frac{\frac{R_2}{n}}{(1+S \cdot R_2 \cdot C_2)} \right] \tag{5-24}$$

Substituting Ic_1 from equation 5-15:

$$Err = \frac{-VOC \cdot C \cdot (1+SR_2C_2)}{(1+S \cdot R_2 \cdot C_2) \cdot (1+S \cdot R \cdot C)} \cdot \left[\frac{(1-n) \cdot (1+n)}{(1+n^2) \cdot SC} + \frac{(1-n) \cdot R_2}{(1+n^2) \cdot (1+S \cdot R_2 \cdot C_2)} \right] \tag{5-25}$$

(e) System modelling for both cases, shown in Figs. 5-12 and 5-13.

Due to the fact that n works in a very limited range (from 0.5 to 1.5), due to timing limitations, it is possible to approximate the following relationships:

$$\frac{(1-n) \cdot (1+n)}{(1+n^2)} \cong 1.7 to 2.3 \cdot \frac{(1-n)}{2} \tag{5-26}$$

$$\frac{(1-n)\cdot n}{(1+n^2)} \cong 1\cdot\frac{(1-n)}{2} \tag{5-27}$$

$$\frac{(1-n)\cdot n}{(1+n^2)} \cong 0.75 to 1.4\cdot\frac{(1-n)}{2} \tag{5-28}$$

Substituting equations 5-26, 5-27, and 5-28 into equation 5-23, for the first case, and into equation 5-25, for the second case, the equation that covers both cases can be summarized as:

$$Err = \frac{-VOC\cdot C\cdot(1+SR_2C_2)\cdot(1-n)}{(1+S\cdot R_2\cdot C_2)\cdot(1+S\cdot R\cdot C)\cdot 2}\cdot\left[\frac{(1.7 to 2.3)}{SC}+\frac{(0.75 to 1.4)\cdot R_2}{(1+S\cdot R_2\cdot C_2)}\right] \tag{5-29}$$

From Fig. 5-14, using Laplace transform, Δn is calculated as:

$$n = \left(K_P+\frac{K_I}{S}\right)\cdot\left(\frac{1-e^{S\cdot T_S}}{S\cdot T_S}\right)\cdot Err - 1 \tag{5-30}$$

Substituting n, from equation 5-21, into equation 5-29, and using equation 5-30, the expression for the complete open loop transfer function is obtained as depicted in equation 5-31. The loop is open at the *Err* signal point, in Fig. 5-14, and considers A as a variable ranging between 1.7 and 2.3, from equation 5-26, and B ranging between 0.75 and 1.4, from equation 5-28.

$$T_{OL} = \frac{Err_{out}}{Err_{in}} = \frac{VOC\cdot\left(K_P+\frac{K_I}{S}\right)\cdot\left(\frac{1-e^{S\cdot T_S}}{S\cdot T_S}\right)}{(1+S\cdot R_2\cdot C_2)\cdot(1+S\cdot R\cdot C)\cdot 2\cdot S}\cdot\left[A\cdot(1+SR_2C_2)+B\cdot SR_2C\right] \tag{5-31}$$

For the open loop transfer function of the complete system, *Err* in equation 5-30 can be considered as input, and the corresponding *Err*, in equation 5-29, can be considered as output. The equation 5-32 depicts the closed loop transfer function:

$$T_{CL} = \frac{VOC \cdot \left(K_P + \frac{K_I}{S}\right) \cdot \left(\frac{1 - e^{S \cdot T_S}}{S \cdot T_S}\right) \cdot [A \cdot (1 + SR_2C_2) + B \cdot SR_2C]}{(1 + S \cdot R_2 \cdot C_2) \cdot (1 + S \cdot R \cdot C) \cdot 2 \cdot S + VOC \cdot \left(K_P + \frac{K_I}{S}\right) \cdot \left(\frac{1 - e^{S \cdot T_S}}{S \cdot T_S}\right) \cdot [A \cdot (1 + SR_2C_2) + B \cdot SR_2C]} \quad (5\text{-}32)$$

5.4.3 CELL EQUALIZER CONTROLLER STABILITY ANALYSIS IN FREQUENCY DOMAIN

Several variables exist in equations 5-31 and 5-32. The closed loop control system must be stable in all possible scenarios, which are specified by the combinations of possible variable values. Table 5-1 summarizes the variable values obtained from measurements:

Table 5-1 Summary of controller variables.

Variable	Value
Battery	
V_{OC}	3 ~ 4.2 Volt
R	100 ~ 150 mΩ
R_2	0 ~ 20% of R
C	20000 ~ 50000 F
$R_2 C_2$	~ 50 sec.
Controller	
T_S	30 sec ~ 2 min
A	1.7 ~ 2.3
B	0.75 ~ 1.4

The goal of the controller design for this application is not to find the optimum equalizing time, but to define a set of K_P - K_I that obtains a robust controller, i.e. the variable variations of Table 5-1 or the noise of the analog measurements do not affect the stability of the system.

Given that the error in V_{OC} (R_2-C_2) estimation has a time constant close to T_S, R_2 will have the greatest influence on the stability of the system. In this analysis, a sampling

time of 1 minute is estimated. For the rest of the variables, which have smaller sensitivity, the worst case is considered, given V_{OC} = 4.2 Volts, R = 100 mΩ, C = 20,000F, A = 2.3, and B = 1.4. For these conditions, the stability requirements in frequency domain (*Barkhausen Stability Criterion*) must comply with a minimum phase margin or gain margin [36]-[37]. The minimum necessary K_I is used, in order to obtain a zero steady-state error (10% of K_P). Fig. 5-16 shows the gain of the open loop system, for different combinations of K_P and R_2.

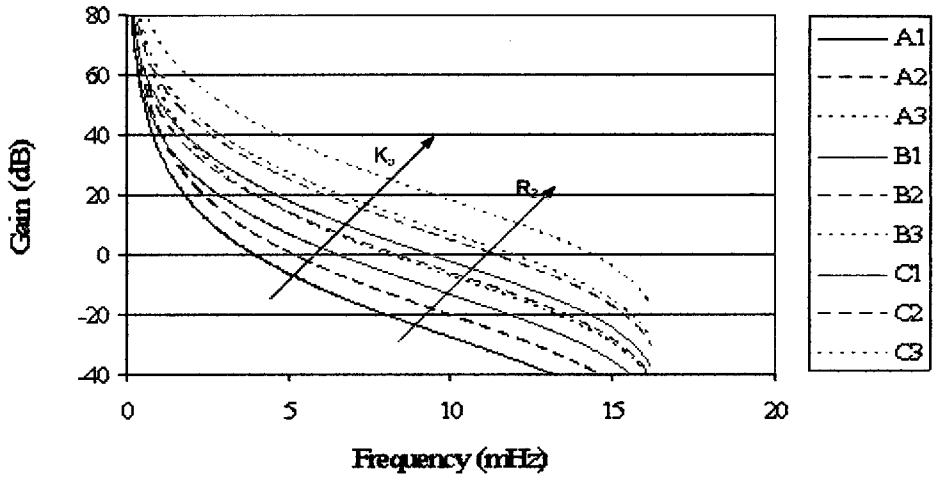


Fig. 5-16 System open loop gain, for different K_P and R_2 values.

In Fig. 5-16, A, B, and C correspond to different values of R_2 (A = 0% of R, B = 20% of R, and C = 80% of R). The numbers 1, 2, and 3 indicate K_P = 10, K_P = 22, and K_P = 100, respectively. Fig. 5-17 shows the phase of the open loop system, for different values of R_2, which is independent of K_P.

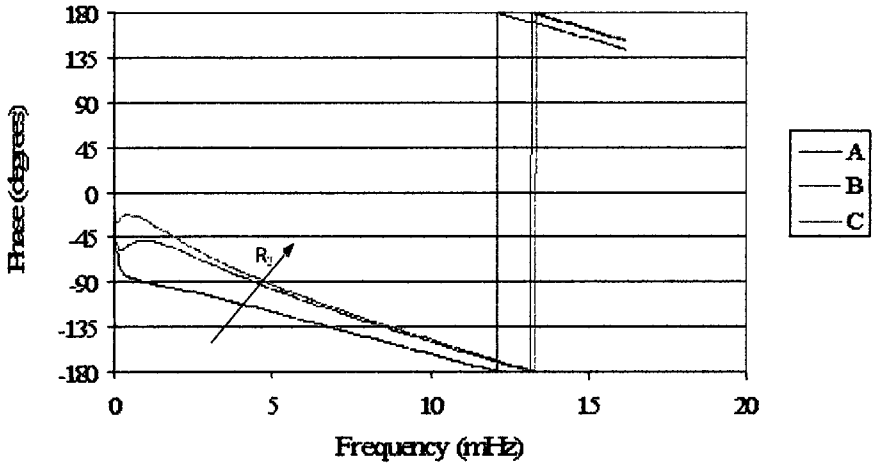


Fig. 5-17 System open loop phase, for different R_2 values.

In Fig. 5-17, A, B, and C correspond to different values of R_2 (A = 0% of R, B = 20% of R, and C = 80% of R). It can be appreciated that the higher the gain or R_2 is, the less stable the system. Table 5-2 summarizes the stability indicators for each K_P-R_2 combination.

Table 5-2 Summary of stability indicators, for different K_P-R_2 combinations.

Combination	R_2 (% R)	K_p	Phase Margin (degrees)	Gain Margin (dB)
A1	0	10	69	+36
A2	0	22	60	+29
A3	0	100	35	+16
B1	20	10	66	+26
B2	20	22	48	+19
B3	20	100	14	+6
C1	80	10	39	+15
C2	80	22	21	+9
C3	80	100	-9	-5

For a maximum acceptable V_{OC} estimation error, represented by the R_2 value, which is 20% of R, the combination B2, having about 50 degrees of phase margin and

almost 20 dB of gain margin, is an excellent starting point. It is worthwhile mentioning here that if the error in V_{OC} estimation (represented by R_2) is not considered ($R_2 = 0$), the system might accept a much bigger K_P; as much as 4 or 5 times higher, as is the case in combination A3. Fig. 5-18 shows the closed loop gain for the same combinations of K_P and R_2, as in Fig. 5-16.

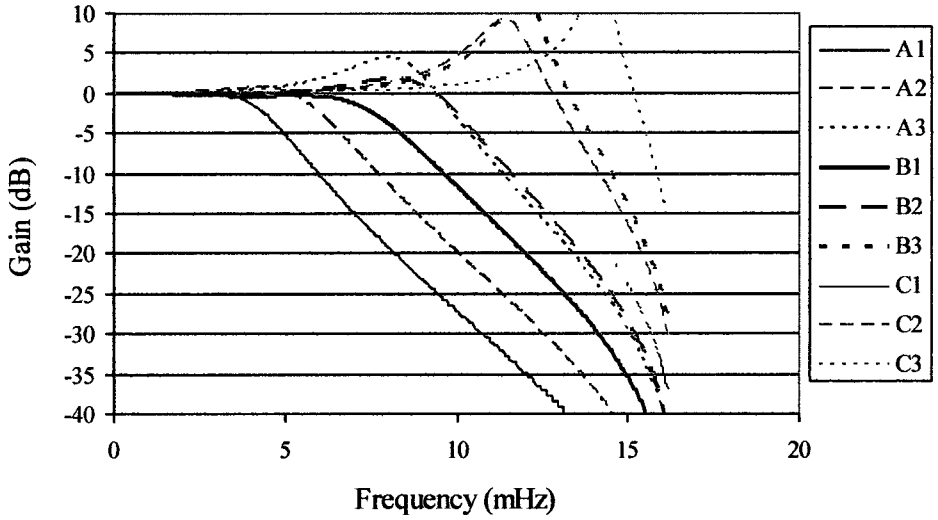


Fig. 5-18 System closed loop gain, for different K_P and R_2 values.

In Fig. 5-18, A, B, and C correspond to different values of R_2 (A = 0% of R, B = 20% of R, and C = 80% of R). The numbers 1, 2, and 3 indicate K_P = 10, K_P = 22, and K_P = 100, respectively. Again, it can be appreciated that the higher the gain or R_2 is, the less stable and faster is the system, which is proven in fig. 5-18 by the higher peak gain and higher bandwidth, respectively. Table 5-3 summarizes the stability indicators for each K_P-R_2 combination.

Table 5-3 Summary of stability indicators for different K_P-R_2 combinations (closed loop).

Combination	R_2 (%R)	K_p	Peak Gain (dB)	Bandwidth (mHz)
A1	0	10	+0.1	4.5
A2	0	22	+0.5	6.2
A3	0	100	+4.3	10
B1	20	10	0	7.8
B2	20	22	+1.8	10.1
B3	20	100	+12.9	13.6
C1	80	10	+3.5	11.4
C2	80	22	+9	13.2
C3	80	100	+17	15.5

As can be appreciated from Table 5-3, the combination B2 (K_P value of 22 and R_2 = 20% of R), presents a very good speed (high bandwidth), while maintaining the stability of the system (relatively low gain peak).

Subsequently, the effect of frequency sampling of V_{OC} estimation is studied. Section 5.2.2 explained a very simple V_{OC} estimation method, the main disadvantage of which includes, turning off the equalizer for several seconds (in this case 4 seconds). This fact forces the reduction in sampling rate, from approximately 30 seconds to several minutes, in order to obtain a reasonable equalizing duty cycle.

Using the previously obtained K_P value of 22 and R_2 = 20% of R, Fig. 5-19 shows the gain of the open loop system. Fig. 5-20 the corresponding phase of the open loop system, with T_S = 30 seconds, 1 minute, and 2 minutes, respectively.

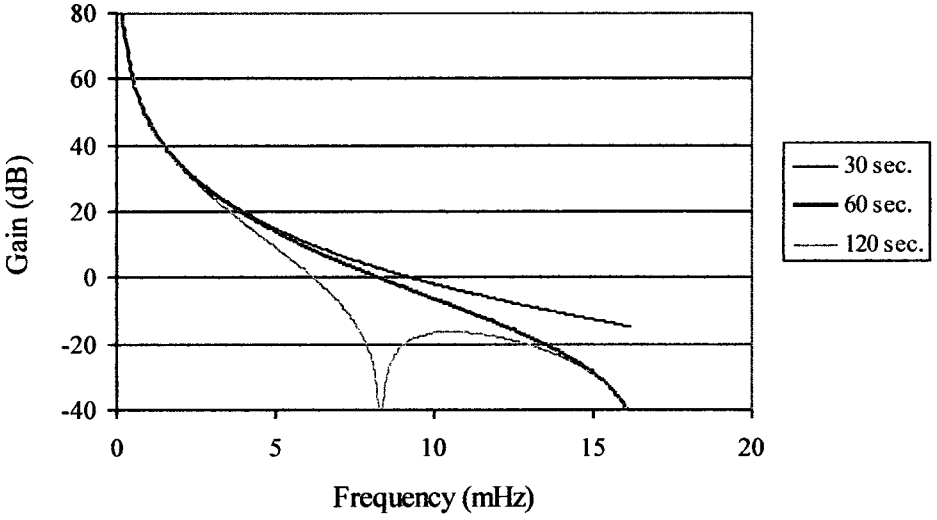


Fig. 5-19 System open loop gain, for different T_S values.

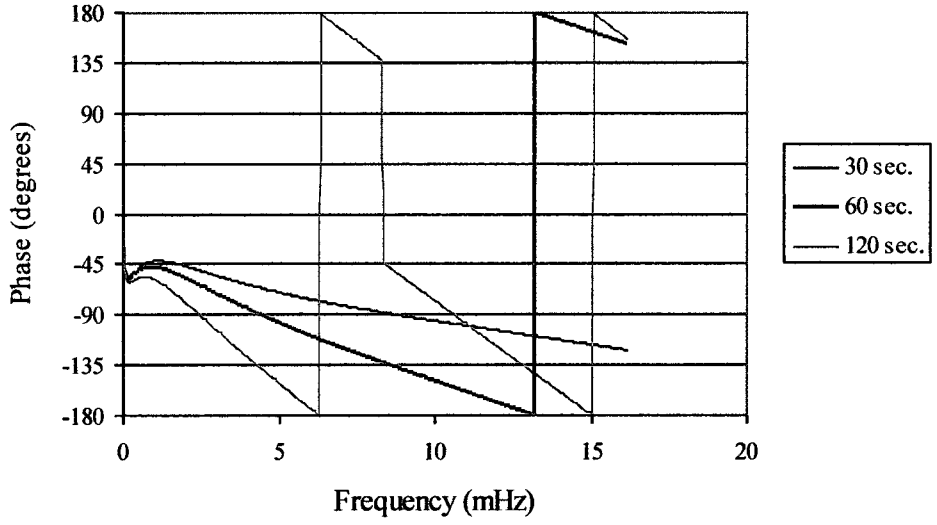


Fig. 5-20 System open loop phase, for different T_S values.

As expected, a faster sampling rate makes the system much more stable. Table 5-4 summarizes the stability indicators for each sampling frequency and the resulting equalizer duty cycle.

Table 5-4 Summary of stability indicators for different sampling rates.

Sampling Rate (seconds)	Phase Margin (degrees)	Gain Margin (dB)	Equalizer duty cycle (%)
30	88	-40	87
60	48	-19	93
120	2	-1	97

From Table 5-4, it is clear that a maximum sampling rate of 1 minute is necessary to obtain stable operating conditions. However, due to the 4 seconds turn-off during V_{OC} measurement, the equalizer duty cycle is negatively affected, as sampling rate tends to increase. As observed in Table 5-4, with a reasonable duty cycle of 93%, a sampling rate of 1 minute was found to perform satisfactorily.

Thus, critical control parameters have been extrapolated, in order to obtain a robust controller. After considering a possible error in V_{OC} estimation, the proportional factor was reduced to 25% of the original value, in order to maintain stability of the system. In the next section, the stability of the system will be verified in time domain, considering non-linear effects and variable limiters.

5.4.4 Cell Equalizer Controller Stability Verification in Time Domain

In order to verify the stability and dynamic performance of the controller, a full time domain simulation is necessary. This is due to the presence of various system non-linearities, such as the ones shown in equations 5-26, 5-27, and 5-28, as well as the ones presented by the limitations of DC/DC ratio, n. It must be pointed out here that n is limited from 0.5 to 1.5, while the equalizer current and cell voltage are limited to 7 Amps and 4.2V, respectively. As explained in section 4.3.1, the maximum DC/DC ratio is

limited, due to minimum and maximum switching times. This limitation is introduced in order to avoid overlapping between modes. The limitation in current is used to avoid saturation in the inductor. Furthermore, the limitation in maximum cell voltage is enforced to improve safety. If none of these limiters is active, then the system is considered to be in linear mode, and it usually occurs in the final stages of equalization.

The proposed novel equalizer is simulated using the dynamic model of the battery cells, reviewed in section 5.2. The control method is explained in section 5.3, using the parameters obtained from section 5.4.3, and the V_{OC} estimation method, presented in section 5.2.2. In order to reduce the complexity of the simulation, a system of 2 cells is used. This simulation represents the response of a bigger system fairly well, as validated later by practical measurements.

As seen in section 5.2.2, V_{OC} estimation involves an equalizing current interruption for 4 seconds. This can be seen in the current plot as a "glitch," witnessing the small impact of the V_{OC} estimation method on the average equalizing current. Fig. 5-21 shows the equalizing current in one of the 2 cells, with an initial unbalance, for 3 cases. The first case involves the original and most common controller, where the error signal is taken directly from the cell voltage, as demonstrated in chapter 4, in Figs. 4-9 and 4-10. Here, the proportional and integral (K_P and K_I) factors are critically damped (this is called "*Method A*").

The second case involves the ideal optimal controller, where the error signal is fed back from the estimated V_{OC}, as analysed in section 5.4.3 (combination A3), where K_P and K_I factors are critically damped (K_P = 100; this is called "*Method B*"). Finally, the third case involves a simulation with a more robust controller, in order to allow some

error in the V_{OC} estimation. As explained earlier, in this scenario, K_P is reduced to 22, in order to maintain stability under all conditions (this is called "*Method C*"). Method C uses the same K_P as the experimental controller. Fig. 5-22 shows the corresponding V_{OC} of each of the 3 systems.

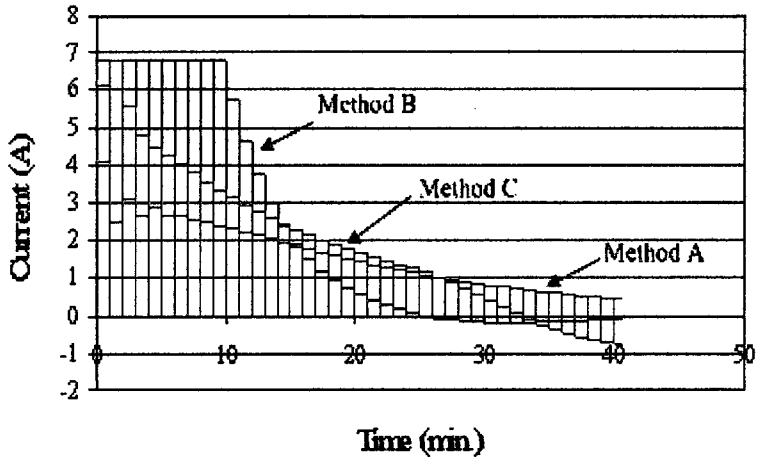


Fig. 5-21 Equalizer current in a cell, using: a) cell voltage control, b) V_{OC} control, and c) reduced K_P factor V_{OC} control.

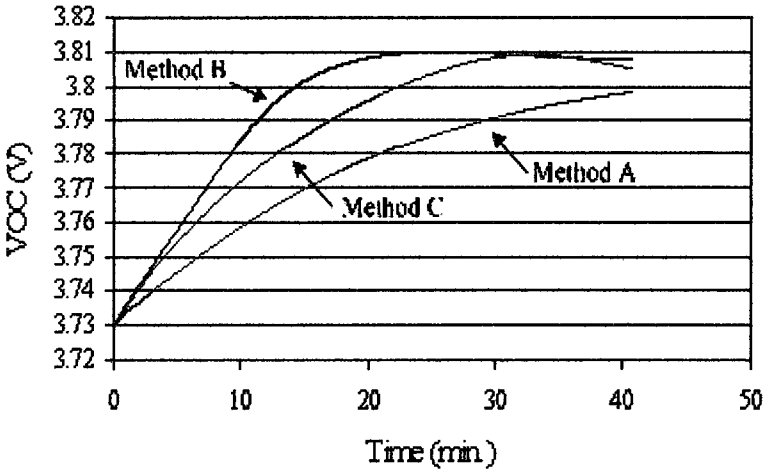


Fig. 5-22 Equalizer V_{OC} in a cell, using: a) cell voltage control, b) V_{OC} control, and c) reduced K_P factor V_{OC} control.

The equalizing time can be seen in Fig. 5-21, when the current reaches zero, and in Fig. 5-22, when the V_{OC} peaks. The improvement in system response is obvious, based on V_{OC} estimation as an error signal ("method B"), in terms of equalizing time (25 min.). On the other hand, "method C" slows down the system, by reducing K_P (33 min.), in order to be stable in all situations. Even with reduction in K_P, the resulting system is much faster than the original one ("Method A," at 60 min.), which effectively reduces the overall equalizing time by nearly 50%. The effect of limitation in equalizing current is critical to note, whereby the current is limited to 7 Amps, for safety, to avoid inductor saturation and for efficiency reasons (since the efficiency drops to less than 75% at higher currents). This is clear in Fig. 5-21, during the first 10 minutes, in "Method B."

In addition, the controller should stop equalizing when the V_{OC} of each cell lies within the defined "deadband," specified to be 0.1% of V_{OC}. This will be shown later, by means of experimental measurements. For example, in Fig. 5-22, the equalizer should have stopped, when the V_{OC} reached the equalizing voltage. In the next section, the experimental measurements performed on the proposed novel equalizer prototype will be presented.

5.5 PROPOSED NOVEL CELL EQUALIZER EXPERIMENTAL RESULTS

The equalizer prototype, on which the measurements were performed, uses the modelled controller of "method C." These measurements validate the previous theoretical models. In order to prove the performance of the equalizer to a full extent, a string of 5 cells were used, where all cells were half charged, except one (cell #2), which was almost

discharged. The charge difference was 2.5Ah. For testing purposes, the total battery voltage was kept constant. This was achieved by using an external power supply, to provide a small current, proportional to the equalizer losses. Fig. 5-23 shows the equalizing current on each cell during the equalization time.

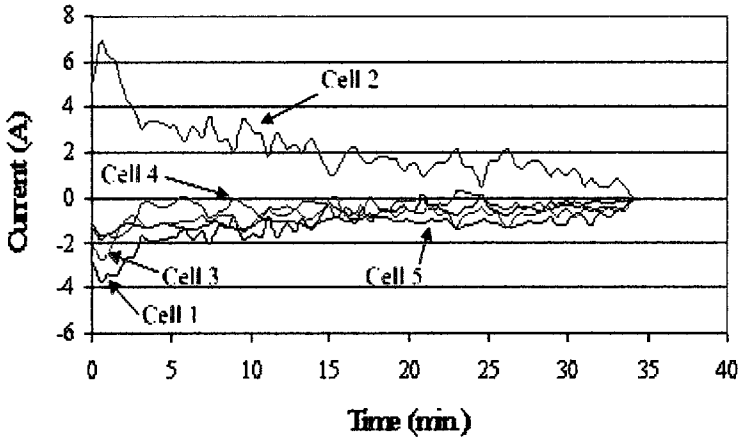


Fig. 5-23 Equalizer current per cell.

In Fig. 5-23, it is clear that the equalizer provides current to cell #2 (positive current), while absorbing current (energy) from rest of the cells (negative current), in an almost equal manner. It is also clear that the equalizer is turned off (zero current) when the discharged cell comes closer to rest of the pack (inside the ±0.1% of V_{OC} difference window), to avoid forcing the equalizer to work in a low power transfer mode. This mode is not necessary in this application, in order to obtain a better efficiency (see Figs. 4-14 and 4-15). On the downside, there exists a certain amount of ripple in the measured current. This is mainly due to 2 sources: one is the error in V_{OC} estimation, as aforementioned, in section 5.4.1, which can also be seen in Fig. 5-23. The second source is the noise generated in the output PWM counter, due to discretization. Fig. 5-24 summarizes the estimated V_{OC} during the equalization time.

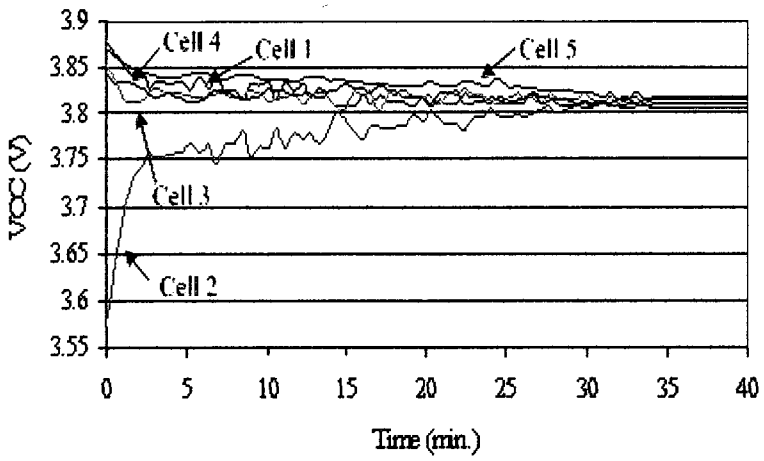


Fig. 5-24 Estimated equalizer V_{OC} per cell.

Fig. 5-24 shows the V_{OC} equalization of cell #2, being completed in about 32 minutes. When the cells reach within a minimum voltage difference, defined by the specifications of 0.1% of the V_{OC}, the equalizer is turned off, as shown in Figs. 5-23 and 5-24, in order to avoid low efficiency working points (Fig. 5-8, lower power transfer). It is clear that there exists a small remaining difference in V_{OC}, which does not justify further equalizing. Furthermore, there also exists some ripple in the estimated V_{OC}, which, as explained before, will affect the calculations. Again, as aforementioned, this is mainly due to small errors in V_{OC} estimation. The value of this error is approximately equal to the maximum error allowed by the specifications, of ±0.1%. Finally, when the cell voltages are within the "deadband," the equalizer is turned off. Hence, there exists no equalizing current, and the cell voltage is equal to the real V_{OC}. After 32 minutes, in Fig. 5-24, it can be appreciated that the change in V_{OC} is inside the allowable error, which perfectly validates the V_{OC} estimation method.

The next section discusses the novel equalizer simulations, using the "method C" control scheme, and will be compared with experimental measurements performed on the practical equalizer.

5.6 COMPARISON BETWEEN THEORETICAL AND EXPERIMENTAL RESULTS

The simulated and measured equalizing currents on cell #2 are shown in Fig. 5-25. The measured equalizing current and V_{OC} per cell are sampled once every 60 seconds, while the simulation is sampled once every second. Logically, this reduces the resolution of the measured current. Fig. 5-26 shows the simulated and experimentally estimated V_{OC} on cell #2.

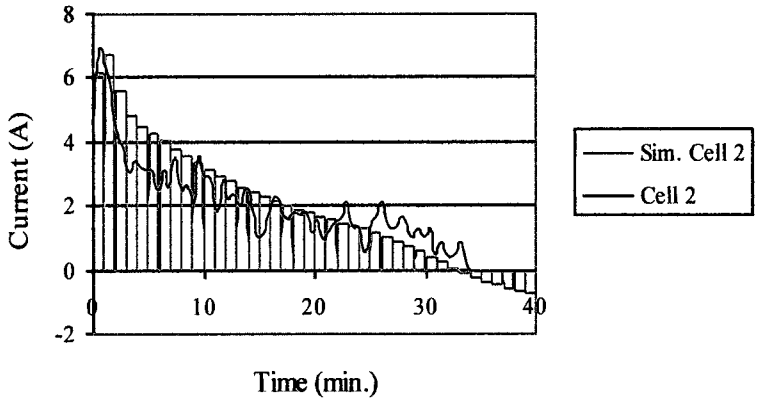


Fig. 5-25 Equalizing current on cell #2; simulated and measured.

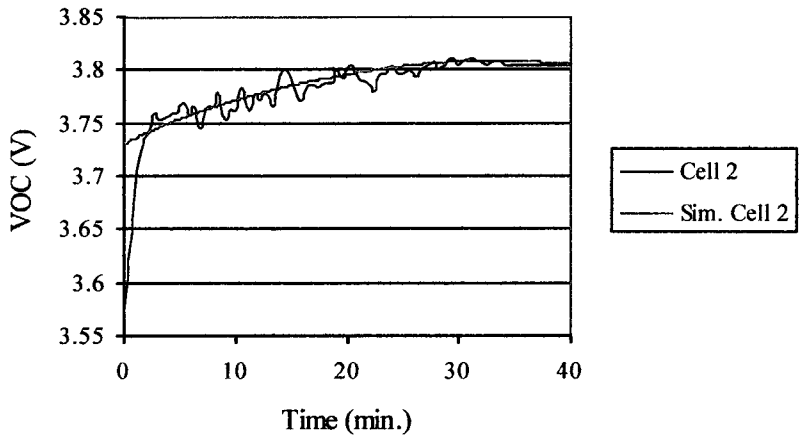


Fig. 5-26 V_{OC} on cell #2; simulated and estimated from measurements.

There also exist some visible differences; for example, there is a significant inaccuracy in the first 2 minutes of equalization. This is because cell #2 was nearly discharged when the equalization began (V_{OC} = 3.5V, equivalent to less than 10% SOC; see Fig. 5-2). In this range of SOC, the electrical equivalent of the battery cell, used for simulation, was no longer valid (Figs. 5-3 and 5-5). Hence, the simulation is quite different from the experimental results, during the first 2 minutes of equalization. Again, it is worth mentioning here that this level of SOC is not generally used in EV/PHEV applications (as described in chapter 3). Thus, making use of a more precise simulation in this range becomes fairly unnecessary.

Another important difference is the presence of relatively high noise in the measurements, which is around the maximum allowable specified noise (RMS value of 0.1% of V_{OC}). Although in physical systems, noise is fairly unavoidable, in this case, there exist additional difficulties. The noise present in this system is generated from 3 primary sources: error in V_{OC} estimation (described in section 5.4.1), the analog sources,

like voltage and current measurements, and from quantization sources, like the resolution of the A/D converter, or the pulse width modulation (PWM) counter.

The noise due to PWM counter resolution, in particular, is critical in this implementation. In order to reduce component costs, the size of the equalizer inductors has been decreased. Because they work in continuous conduction mode (CCM), the way to reduce the inductor sizes, without increasing the current ripple, is to increase the switching frequency. In this case, MOSFETs (and their drivers) are chosen to be fast enough; hence, theoretically there is no problem (except for the losses) in increasing the switching frequency [36]. At the same time, there exists a problem in the microcontroller, the internal oscillator of which is running at a certain speed (in this case, 20 MHz). This frequency is fed to the PWM counters. In order to increase PWM switching frequency, the total count of the PWM counter must be reduced, which in turn reduces PWM resolution. For example, a total count of 200 will provide a 100 kHz switching frequency and a resolution of 40 ticks per PWM channel, in a 5 cell equalizer. This is barely enough resolution for the equalizer, and it is equivalent to a quantization error of $1/40^{th}$ of the total time range, resulting in small noise in the desired current.

Although these noise sources are undesirable, they are not considered a major issue. This is because the equalization will still be performed accurately, but with slight variation in current, as demonstrated in Figs. 5-25 and 5-26. The only downside is the need to overdamp the system, by reducing K_P, in order to smooth the output, with a slight negative effect in equalizing time (section 5.5). Possible techniques to improve equalizing time include: using a faster microcontroller; usually more expensive, bigger

inductors and filter capacitors, which are also expensive, and/or using an additional external PWM modulator, which again increases the component count and total cost.

As in any engineering problem, there exists a trade off. In this case, the current ripple during equalization has to be balanced against the cost of the system. However, in a cost sensitive application, such as EVs/PHEVs, as discussed in chapter 3, the balance is against the current ripple. As observed in chapter 4 (sections 4.3.1 and 4.4.3), the current ripple increases idle losses, reducing the efficiency at lower current transfer levels. There exists a critical trade-off between this efficiency and cost. In the case of the developed prototype, the use of the "deadband" method, as seen in section 5.5, avoided entering into low current equalization. Hence, a good efficiency at lower current transfer levels becomes unnecessary. Finally, the relatively precise prediction of current and V_{OC} in the normal SOC range is worth pointing out, even in the presence of current ripples. Thus, the control model for this application is successfully validated.

5.7 SUMMARY

Based on the comprehensive control analysis and comparison with the experimental measurements, this chapter presented a detailed procedure to control an equalizer system, considering practical issues, such as cost and measurement errors (both numerical and physical). A simple V_{OC} estimation algorithm has been presented and validated. On the downside, the relatively small error of this method negatively affected the controller stability, forcing a slight increase in damping of the system. Thus, there is a slight increase in equalization time; however, this does not seriously affect the performance of the equalizer.

A suitable controller, integrated with the proposed equalizer, has been modeled, simulated, and validated against experimental measurements. Additional issues appeared during experiments, such as analog noise in the voltage and current measurements and quantization noise in PWM timer. These issues are not large enough to justify changing the solution, which would inevitably involve a cost increase.

In this chapter, the objective of designing a low cost, robust equalizer controller has been successfully achieved. As part of potential future work, an implementation of a more precise V_{OC} estimator, based on the methods proposed by [31]-[33] might be undertaken. However, issues such as computational load have to be overcome. The methods proposed in [31]-[33] will help reduce the sampling rate, without sacrificing the duty cycle of the equalizer. This will invariably increase the stability of the controller and improve the precision of V_{OC} estimation.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 SUMMARY

Battery technology is still the main stumbling block for commercialization of electric (EV), hybrid electric (HEV), and plug-in hybrid electric vehicles (PHEV). This thesis focused on discovering a practical power electronics intensive solution to overcome this major obstacle. Given the fact that the main issue is the sensitivity of the economic nature of advanced electric vehicles, the solution proposed in this thesis has been cost optimized, without disregarding features such as performance, efficiency, and safety. More specifically, the following inferences and synopsis can be made.

(a) In general, none of the equalizer configurations are a perfect match for any specific application. Nevertheless, for PHEV and EV applications, the proposed novel cell equalizer displayed exceptional performance in most aspects, except control complexity. This, on the other hand, does not necessarily imply higher costs, as was discussed earlier.

(b) The importance of overall economic analysis for EV applications was emphasized upon in chapter 3. The importance of using a battery equalizer, in terms of cycle life, lifetime, and safety was presented. The influence of using the battery equalizer on the overall cost of the complete PHEV/EV system was evaluated and compared to a normal ICE vehicle. The equalizing system cost, using the novel equalizer, was found to be as low as $4.00/cell, which corresponds to to 5% of the battery cost.

(c) It can be safely concluded that battery chemistries, depicting a long life, and capable of lasting more than 10 years (such as $LiFePO_4$) provide a good option for EV applications. Furthermore, a reduced SOC utilization (50% capacity or less) and the use of a high current, high efficiency, and low cost cell equalizer makes future EVs economically viable, even in low-priced oil markets (2009).

(d) Chapter 4 presented the novel cell equalizer configuration, capable of accomplishing low cost, high-current, and high efficiency requirements. The efficiency of the equalizer was found to be quite good in the required current range (80%, at 1 Amp to 5 Amps). In fact, this is comparable to efficiencies obtained by soft-switching equalizers. Furthermore, the total system efficiency was also satisfactory (about 75%). This fact encompasses the potential of designing an advanced soft-switched version of the proposed topology, whereby efficiencies reaching about 85-90% are definitely possible. A detailed comparison with the best contender, the typical inductive equalizer, has been also performed, demonstrating lower cost (40% less) and slightly higher efficiency.

(e) The proposed equalizer depicts higher efficiency, especially when power is transferred from the first to the last cell of an equalizer module (10% more, on average). This fact is particularly useful in long EV/PHEV battery cell strings. However, the equalizer chaining method and a centralized management system would be required (section 4.4.4).

(f) Chapter 5 presents a complete procedure to control the proposed equalizer system, considering practical issues, such as cost and measurement errors. A simple V_{OC} estimation algorithm has been presented and validated. The errors have been appropriately evaluated and their effects have been minimized. A marginally compliant error in V_{OC} estimation, of $\pm 0.1\%$, has been obtained.

(g) The control method has been integrated within the proposed equalizer system, and modeled, simulated, and validated against experimental measurements, performed on a commercial grade prototype. The issues that appeared during experiments have been thoughtfully weighted against cost. However, the objective of designing a low-cost, robust equalizer controller has been successfully achieved.

In conclusion, this thesis presented a practical and cost-effective solution to key issues of energy storage systems for future EV commercialization, in the form of a power electronics based battery cell equalizer. The proposed novel cell equalizer depicts high current carrying capability, advanced control, based on battery SOC estimation, and high efficiency, combined with low cost and simple manufacturability. These aspects make the proposed novel cell equalizer a highly attractive option for current PHEV and future EV energy storage applications.

6.2 POTENTIAL FUTURE WORK

Due to the novelty of the work presented in this thesis, numerous opportunities exist for future research and development. Few of them include, but are not limited to the following possible approaches.

(a) In relation to lithium battery modeling, additional experiments are undoubtedly essential, to add more data, especially in terms of battery cycle life. Furthermore, additional investigation is necessary for the new $LiFePO_4$ chemistry, the cycle life of which is claimed to be excellent. However, no experimental data is currently available to back up this claim.

(b) The novel cell equalizer presented in this thesis also has scope for improvement. In general, commercial MOSFETs, having lower R_{dsOn}, also present higher C_{GS}, lowering the conduction losses, and increasing idle consumption and cost. The balance between idle power consumption, power capabilities, and cost, by optimizing the MOSFET gate capacity versus conduction losses, could be one of the focus areas of future research. In addition, considerable improvements in efficiency may be obtained by using soft switching instead of hard switching.

(c) The novel cell equalizer also has the potential to increase the output power of the battery pack. This feature requires detailed measurement of internal resistance and open circuit voltage versus SOC. Thereafter, a suitable algorithm could be designed to calculate the peak power tracking (PPT) of each cell.

(d) The management of multiple equalizer modules in one long chain presents another challenge. The overall energy management could be performed in one central processor, which would constantly communicate with the dedicated microcontroller of each equalizer.

(e) The concept of state of health (SOH) and its estimation could be explored in further detail. Reference [33] could be a solid starting point.

(f) For V_{OC} and SOC estimators, the methods proposed by [31]-[33] might possibly be better than the one implemented in this thesis. However, critical issues, such as computational load, have to be overcome. The methods presented in [31]-[33] could help reduce sampling rate, without affecting the duty cycle of the equalizer. Thus, the stability of the controller could be increased and the precision of V_{OC} estimation could be improved.

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