AlGaN/GaN HFETs: Current-drive Scalability, Gate-lag and Frequency-dispersion Studies

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ABSTRACT

AlGaN/GaN HFETs: Current-drive Scalability, Gate-lag and Frequency-dispersion Studies

Md. Jahirul Sikder

AlGaN/GaN Heterostructure Field Effect Transistors (HFETs) are suitable candidates for high-power and high-frequency applications. Although GaN possesses a broad peak in its drift-velocity versus electric-field (i.e., v_d-E) characteristics, with very large peak drift-velocity and a pronounced region of negative differential mobility, oftentimes a purely-saturating approximation of v_d-E characteristics is considered to be adequate for the evaluation of the drain-current characteristics of AlGaN/GaN HFETs. In contradiction to this belief, it was deemed necessary to investigate the accuracy of this purely-saturating transport characteristics in evaluation of the scalability of the current-drive of AlGaN/GaN HFETs with gate-length. This evaluation is carried out by considering both the realistic steady-state drift transport characteristics and the purely-saturating approximation of the drift transport characteristics. Results show that the drain-current of AlGaN/GaN HFET is less scalable, than expected on the basis of the purely-saturating drift transport characteristics. The predictability of this scaling-trend with the improvement in the Ohmic contact technology is also investigated.

In addition, in this study two newly-developed AlGaN/GaN HFETs, known as island-, and fin-isolated, are evaluated from the point of view of gate-lag and frequency-dispersion. These studies are deemed important for further development of these novel device technologies. The studies are carried out over a wide range of temperatures. Variation of the observed gate-lag profiles with temperature provided important signatures linking the fabrication technology of these new device types with reliability concerns. In light of this study, suggestions are made to improve the aforementioned technologies.

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Chapter 1

Introduction

1.1 Advantages of III-nitride Material System

III-nitride material system (i.e., AlN, GaN, InN, and their ternary alloys) has gained significant research interest for high-power, high-frequency, high-temperature, and optoelectronic device applications. This interest is the consequence of a combination of several factors including: high two-dimensional electron-gas (i.e., 2DEG) concentration, large critical electric-field, good thermal-stability, and superb steady-state drift-velocity versus electric-field (i.e., v_d-E) characteristics in specific heterojunctions of this material system [1-4].

Polarization properties are among the most advantageous features of III-nitride semiconductors in comparison to other III-V semiconductors. Made possible by these polarization properties, III-nitride heterostructures can form 2DEG carrier concentrations of at least one order of magnitude larger than other III-V heterostructures. These polarization properties present themselves in two forms: spontaneous and piezoelectric [5-6].

The steady-state drift-velocity versus electric-field characteristics of GaN has been the subject of much interest. Although other III-V semiconductors such as GaAs also exhibit a steady-state peak in their drift transport characteristics, GaN possesses a much broader v_d-E characteristics with a much higher peak drift-velocity. The saturation velocity of GaN is also superior to those other semiconductors.

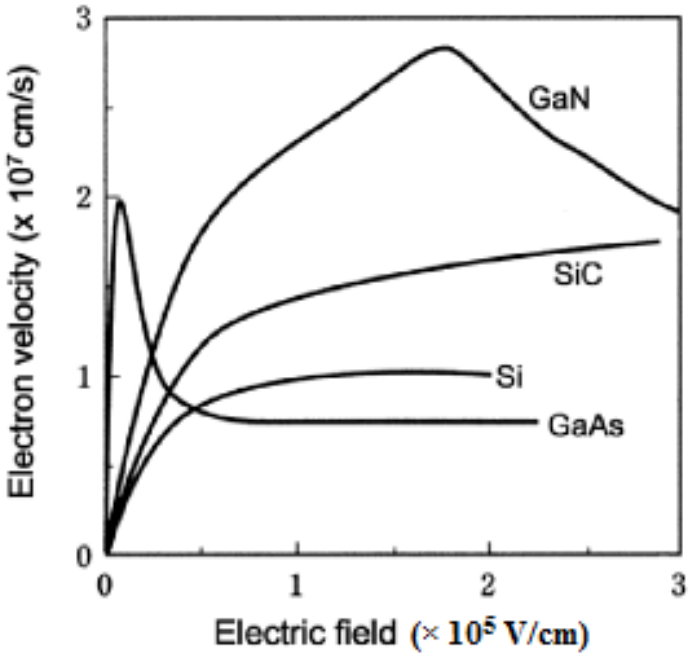


Figure 1.1: Steady-state electron drift-velocity versus electric-field characteristics of GaN, SiC, Si, and GaAs [7].

Figure 1.1 illustrates that GaN offers the broadest peak in v_d-E characteristics among the main contenders of semiconductor market. Presence of this pronounced peak, and the negative differential mobility region attributed to it, poses important consequences on device operation.

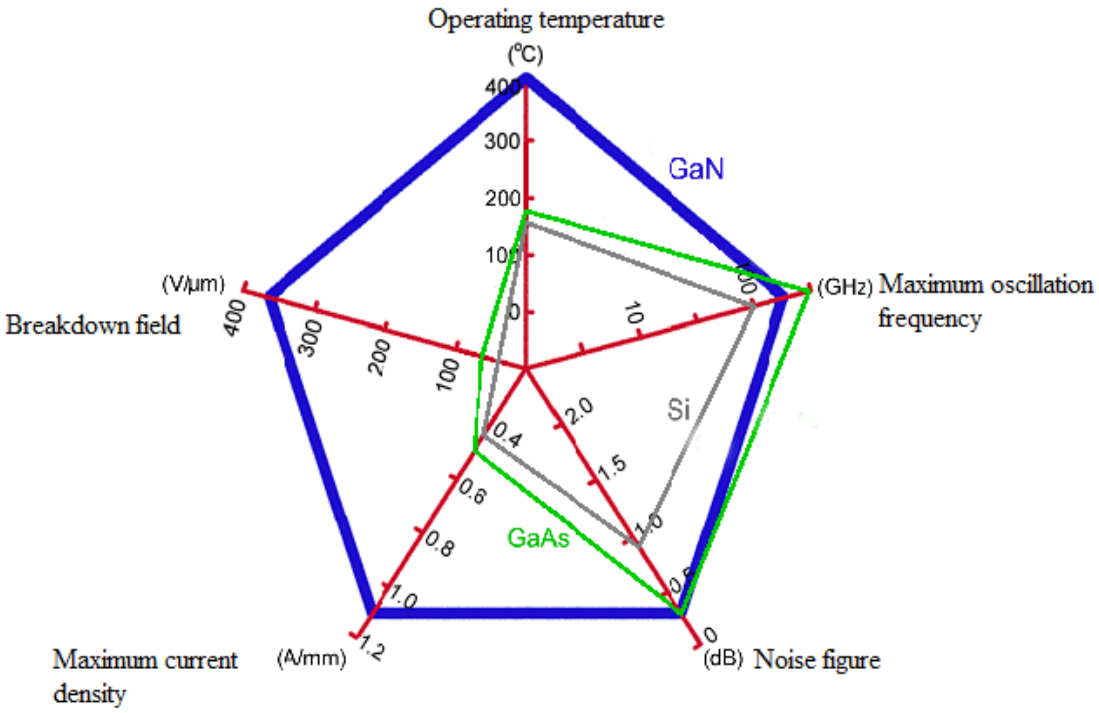


Figure 1.2: Comparison of GaN, GaAs and Si for high-temperature, high-frequency, and high-power applications [8].

Figure 1.2 compares the operating temperature, maximum oscillation frequency, noise figure, breakdown field, and maximum current density of GaN Field-Effect Transistors (i.e., FETs) with FETs from two other major semiconductor technologies (i.e., GaAs and Si). Nowadays, GaN-based devices are commercially available in the market in the form of power electronic systems, LEDs, RF systems and solar cells [9]. The estimated market revenue for GaN semiconductor devices is forecasted to be about $2.6 billion by 2022 [10].

1.2 AlGaN/GaN Heterostructure Field Effect Transistor

AlGaN/GaN Heterostructure Field Effect Transistor (i.e., HFET) is composed of a wide band-gap material (i.e., AlGaN, which is referred to as the barrier layer) grown on top of a narrow band-gap material (i.e., GaN, which is known as the channel layer). Caused by the conduction band discontinuity between the barrier and the channel layer, a triangular quantum well will form on the GaN-side of the heterointerface (Figure 1.3). The wide band-gap barrier layer in an HFET mimics the role of the oxide layer in a MOSFET, in terms of confining the electron concentration in the channel.

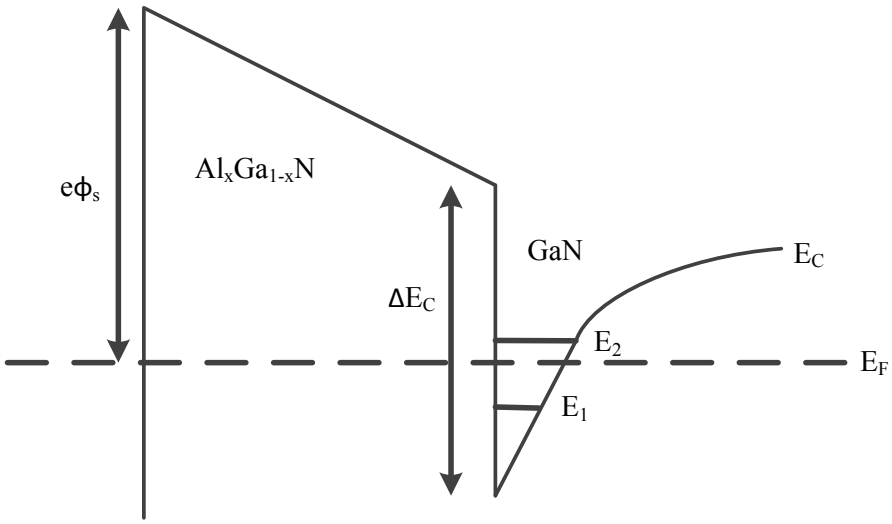


Figure 1.3: Schematic conduction band diagram of AlGaN/GaN HFET. ΔE_C is the conduction band discontinuity at the heterointerface, E_1 and E_2 are the first and second sub-bands of the triangular quantum well, $e\varphi_s$ is the Schottky barrier height, and x is the Al-mole fraction in the AlGaN barrier.

The source of electron concentration in the channel of a non-polar HFET is the highly-doped wide band-gap barrier layer. Band bending at these heterointerfaces results in migration of charge carriers from the barrier (where the parent donors are located) to the triangular quantum well formed in the channel layer. Since 2DEG electrons are

confined in the triangular quantum well (and as a result are spatially separated from the parent ionized impurities), electron mobility will be enhanced in such a structure [11].

III-nitride semiconductors can be grown both in Zinc blende (Zb) and Wurtzite (Wz) crystalline forms. The non-centrosymmetric nature of III-nitride Wurtzite crystals induces a sizeable spontaneous polarization in these crystals. The strength of this spontaneous polarization is in increasing order from GaN to InN, and to AlN [12]. Wurtzite III-nitride crystals can be grown according to two different faces: (i) metallic-face: when the top most atoms are metals and (ii) nitrogen-face: when the top most atoms are Nitrogen [6]. The direction of the spontaneous polarization depends on the face of the crystal (Figure 1.4).

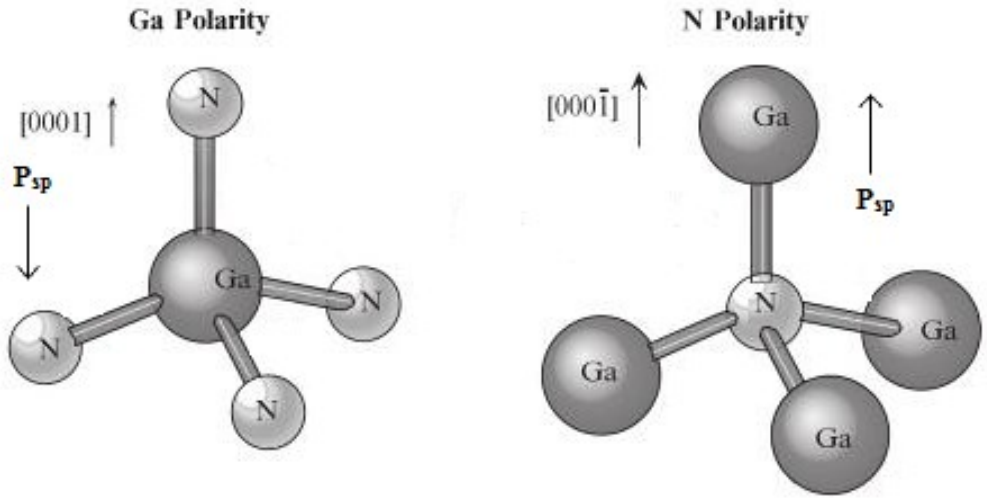


Figure 1.4: Stick and ball configuration of Ga-face and N-face GaN [13]. P_{sp} is the spontaneous polarization.

There exists a sizeable discontinuity between the strength of the unidirectional spontaneous polarization of the AlGaN barrier and the GaN channel layer. As a result of the difference between these spontaneous polarizations, a negative polarization charge concentration is induced at the GaN-side of the metallic-face AlGaN/GaN

heterostructure. This polarization charge is partially responsible for the formation of the 2DEG in AlGaN/GaN HFETs [14].

In addition to the mismatch of spontaneous polarizations between AlGaN and GaN, a piezoelectric polarization also exits at the AlGaN/GaN heterointerface. Due to the lattice mismatch between AlGaN and GaN, in pseudomorphic growth of the AlGaN barrier on top of the GaN channel layer, tensile strain builds up at the heterointerface. Presence of this built-in strain and the large piezoelectric coefficients of III-nitride cause the induction of a sizeable piezoelectric polarization. The direction of this polarization vector in a metallic-face AlGaN/GaN HFET is the same as the spontaneous polarization (Figure 1.5). The formation of high 2DEG carrier concentration at the heterointerface of an unintentionally doped metallic-face AlGaN/GaN HFET is the net result of the discontinuity of spontaneous polarization between AlGaN and GaN, and this large piezoelectric polarization [15].

Figure 1.6 illustrates the basic structure of an AlGaN/GaN HFET. Due to the absence of a commercially viable GaN substrate, AlGaN/GaN HFETs are conventionally fabricated on SiC or Sapphire substrates [16]. During crystal growth on these lattice-mismatched substrates, AlN and GaN nucleation and buffer layers are used to minimize the number of dislocations. The thin AlGaN barrier layer is pseudomorphically grown on top of a relaxed GaN channel layer. As indicated earlier, according to this tensile-strained growth mode, the unidirectional spontaneous and piezoelectric polarizations contribute to the formation of 2DEG at the AlGaN/GaN heterointerface. Due to the presence of these sufficient sources for 2DEG induction, intentional doping is usually absent from the fabrication process of AlGaN/GaN HFETs.

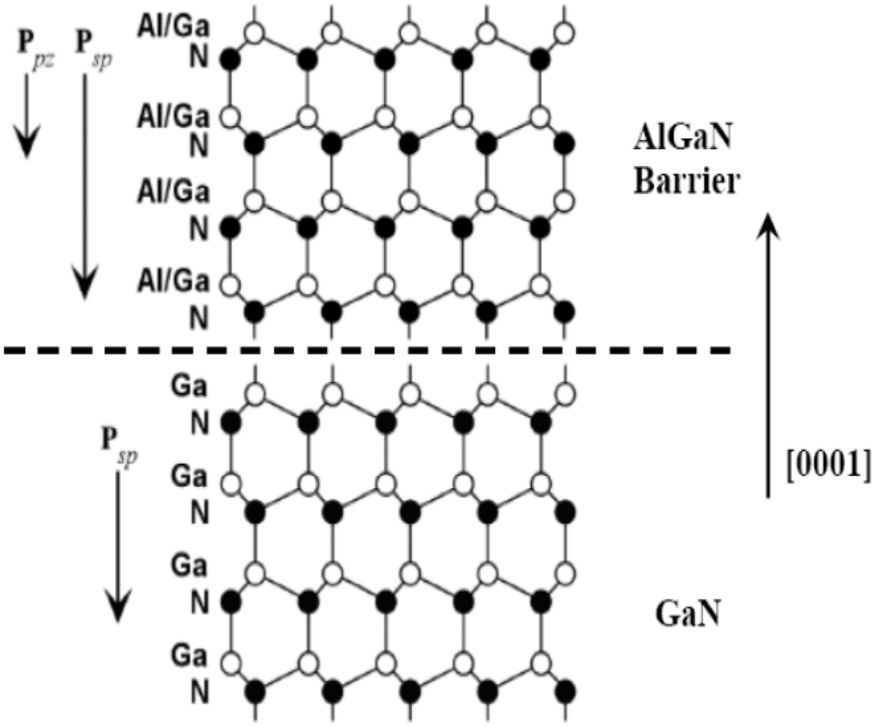


Figure 1.5: Spontaneous and piezoelectric polarization in a metallic-face AlGaN/GaN HFET. P_{sp} represents spontaneous polarization and P_{pz} represents piezoelectric polarization [17].

In the structure illustrated in figure 1.6, the alloyed Ohmic contacts directly connect the source and drain electrodes to the 2DEG. Gate electrode forms a Schottky contact and is situated between the source and drain electrodes. Unlike MOSFETs, AlGaN/GaN HFETs are often realized as nonself-aligned devices. Presence of gate-drain spacing is very important in increasing the breakdown voltage of these transistors. Therefore, the channel of an AlGaN/GaN HFET is composed of source-access region (i.e., spacing between the source-electrode and the gate-electrode), gated channel, and drain-access region (i.e., spacing between the gate-electrode and the drain-electrode).

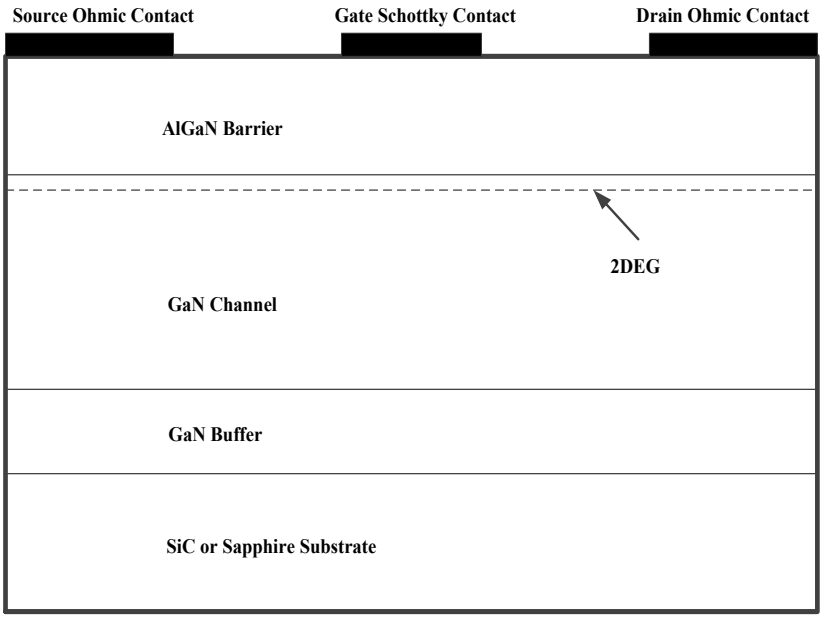


Figure 1.6: Basic schematic of an AlGaN/GaN HFET.

1.3 Significance of v_d-E Characteristics of GaN in Drain-current Scalability of AlGaN/GaN HFET

Over the past five decades gate-length scaling of field-effect transistors has served as the key driver for improving the frequency response and current-drive, and as a result functionality of chips realized in the FET technology. Caused by the major presence of silicon MOSFETs, our understanding of scaling is very much biased to the scaling-trends observed in these devices. In a silicon MOSFET, due to the purely-saturating v_d-E characteristics of silicon, increase in the average electric-field of the channel (caused by the reduction of gate-length), tends to enhance the proportional length of the channel operating under saturation velocity. As the saturation velocity in a purely-saturating v_d-E characteristics (like that of silicon) also is the highest achievable drift-velocity, in this

case the proportional increase in the length of the high field region is translated to higher average electron-velocity. As a result, due to proportionality between drain-current and this average-velocity, scaling is observed to directly contribute to enhancement of current-drive. Whereas enhancement of the maximum electric-field along the channel of a FET is an undisputed outcome of gate-length scaling, the presence of a hump in the v_d-E characteristics (such as the one observed in III-V semiconductors) can result in a degradation of average-velocity if the maximum electric-field is matched with the trailing side of this hump (i.e., region of negative differential mobility).

While in many III-V semiconductors such as InP and GaAs, the small width of the hump in the v_d-E characteristics severely limits the chance of operating under conditions where the maximum electric-field is defined in this negative differential mobility region, the very wide peak of the v_d-E characteristics of GaN (Figure 1.1) predicts otherwise. As a result, in order to properly understand the implications of gate-length scaling on the operation of AlGaN/GaN HFET, it is deemed important to rigorously analyze the behavior of these devices with scaling.

1.4 Characterization of AlGaN/GaN HFET

Although AlGaN/GaN HFETs are popular candidates in high-frequency and high-power electronic systems (Figure 1.8), these devices still suffer from reliability issues. Existence of trap-centers and material defects are the main reliability concerns of AlGaN/GaN HFET technology [18-23]. Introduction of a new device design always requires the evaluation of those concerns. Among the characterization techniques deemed suitable for studying the operation of high-frequency devices, gate-lag and frequency-dispersion

study of the output resistance (i.e., R_{DS}) have a predominant place. In this thesis, these characterization techniques have been applied to two new AlGaN/GaN HFET structures, recently developed at Concordia University.

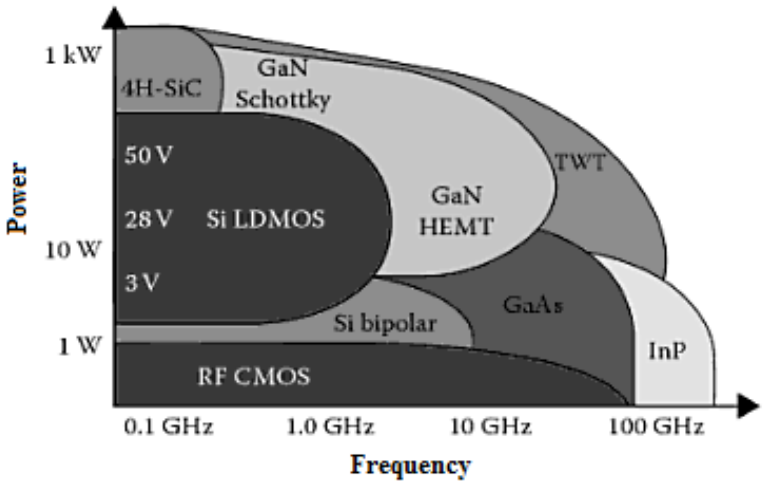


Figure 1.7: Power-frequency diagram of some major semiconductors (i.e., GaN, GaAs, Si, InP, and SiC) for different applications [24].

Gate-lag and frequency-dispersion can have significant effect on the high-frequency performance of these devices. Gate-lag is referred to the transient delay of the drain-current in response to an abrupt change in the gate voltage. R_{DS}-dispersion is known as the variation of device output resistance, with the increment of frequency. These measurements are effective tools for identifying the existence of trap-centers and also limitation on the device high-frequency performance.

1.5 Overview of Thesis

In Chapter 2 of the thesis, the study of the scalability of the current-drive of AlGaN/GaN HFETs with gate-length is carried out by considering both the realistic steady-state drift transport characteristics and the approximate purely-saturating drift transport characteristics. The investigations reveal that the approximate purely-saturating model tends to overestimate the improvement in drain-current drive with gate-length scaling.

In Chapter 3, gate-lag and R_{DS}-dispersion of two newly developed device types (i.e., island-, and fin-isolated) are studied at different temperatures and compared with the conventional mesa-isolated device. Modifications to the fabrication process of these two novel device technologies are proposed in order to improve their gate-lag and high-frequency performance.

Conclusion of this work along with some suggested future works are presented in Chapter 4.

Chapter 2

Scalability of the Drain-current Drive of AlGaN/GaN HFETs with Gate-length

2.1 Abstract

The scaling-trend of the current-drive of AlGaN/GaN Heterostructure Field Effect Transistors (HFETs) with gate-length is studied with the application of a realistic steady-state drift transport characteristics and an approximate purely-saturating drift transport characteristics. Findings show that due to an overwhelming presence of a region of negative differential mobility in the transport characteristics of GaN, a scaling-trend different from the one observed in mainstream silicon MOSFETs should be expected for AlGaN/GaN HFETs. The role of improvement in Ohmic contact technology on this scaling-trend is also investigated.

2.2 Introduction

The last two decades have been witness to a growing interest in the application of AlGaN/GaN Heterostructure Field Effect Transistors (HFETs) to high-power and high-frequency electronic systems [25-27]. This growing interest has been fed by a large number of factors including: large critical electric-field, superior two-dimensional electron-gas (2DEG) density, good thermal-stability and -conductivity, very large peak electron-velocity, and very broad peak in the steady-state drift-velocity versus electric-field characteristics (i.e., v_d-E characteristics) of this material system [28].

The formation of the very high concentration polarization-induced 2DEG at the polar AlGaN/GaN heterointerface, and its particularly broad v_d-E characteristics (with very large peak drift-velocity) fulfill the expectation of large drain-current density in AlGaN/GaN HFETs. As a result of the importance of these particular features in evaluation of the current-drive of these relatively new transistors, a fresh and unbiased perspective, towards the drain-current scalability of mainstream silicon MOSFETs, is needed for better understanding the drain-current scalability of AlGaN/GaN HFETs.

In the present work, particular attention has been given to the v_d-E characteristics. Although oftentimes, a purely-saturating v_d-E characteristic is deemed sufficient for evaluation of drain-current characteristics of AlGaN/GaN HFETs [29], it has been shown that with the improvement in fabrication technology of Ohmic contacts such models underestimate the current-drive [30]. In the present work, both the approximate purely-saturating v_d-E characteristics and the realistic steady-state drift transport characteristics have been used in modeling the drain-current characteristics of AlGaN/GaN HFET and

evaluation of its scalability with gate-length (i.e., L_G) and gate-drain spacing (i.e., L_{GD}). An improved version of the analytical model of Loghmany *et al.* has been employed [31]. The model was validated with the use of experimentally measured drain-current characteristics of a variety of devices with different values of L_G and L_{GD}. Findings show that the broad peak of the v_d-E characteristics can play a tangible role in limiting the gain in average electron-velocity of the 2DEG electrons, and as a result the gain in drain-current, as the gate-length and gate-drain spacing are scaled down. Such degradation in scalability of the drain-current drive with application of the proper v_d-E characteristics, instead of the approximate purely-saturating v_d-E characteristics, proves that a reduced gain in terms of drain-current, with regards to mainstream silicon MOSFETs, should be expected from L_G-scaling of AlGaN/GaN HFETs. It is observed that this reduction increases with expected improvements in Ohmic contact technology.

Since the employed analytical model does not consider the energy relaxation time and temporal overshoot in drift-velocity, the conclusions of this work are not extendable to very small values of L_G and L_{GD}, for which ballistic transport becomes important to consider. As a result, a minimum gate-length of 0.2 μm has been used in evaluations.

In Section 2.3, a brief overview of the analytical model used in evaluation of scaling-trends, and also information about the devices used in experimental validation of the results are presented. Section 2.4 presents the discussions on the observed trends in drain-current and average drift-velocity scaling with gate-length and length of gate-drain spacing. Also in this section the impact of improvement of Ohmic contact technology on these scaling-trends is evaluated. Conclusions are presented in Section 2.5.

2.3 Analytical Model for Evaluation of Drain-current Scalability and Device Information

So far, a variety of analytical and semi-analytical models for evaluation of drain-current characteristics of AlGaN/GaN HFETs have been proposed [29-36]. Some of these models rely on Ridley's mobility model [37], which describes the v_d-E characteristics as a purely-saturating characteristics, without the presence of a peak in the steady-state drift-velocity [29]. Although adoption of this simpler framework of transport simplifies the modeling of drain-current characteristics, Loghmany *et al.* have shown that lack of consideration of steady-state velocity overshoot can result in an inaccurate estimation of the current-drive of AlGaN/GaN HFETs, especially with the expected improvement in Ohmic contact technology [30]. In the present work, the more accurate mobility model used in the work of Loghmany *et al.*, and also Ridley's mobility model were used in evaluation of the prediction power of these two models in forecasting the drain-current scalability of AlGaN/GaN HFETs with L_G and L_{GD}.

According to Ridley's mobility model, the electron-velocity $v(E)$ is described by the following two-section relationship [37]:

$$v(E) = \begin{cases} v_0 E \frac{E+E_1}{E_1(E+E_0)} & E \le E_s \\ v_s & E > E_s \end{cases} \quad \text{where } E_0 = \frac{v_0}{\mu_0} \;\; E_1 = \frac{v_0}{\mu_1} \tag{2.1}$$

Here v_0 is the knee velocity, v_{sat} is the saturation velocity, E_s is the saturation electric-field, μ_0 is the low-field mobility and μ_1 is the high-field mobility, E_0 is referred to as the threshold for the low-electric-field and E_1 is the threshold for the high-electric-

field. μ_0 = 1300 cm^2/(V.s), μ_1 = 50 cm^2/(V.s), v_{sat} = 1.94 × 10^7 cm/s, v_0 = 13.2 × 10^6 cm/s.

The mobility model adopted in the work of Loghmany *et al.*, which was originally proposed by Polyakov *et al.* [38] is formulated as:

$$v(E) = \frac{\mu_0 E + \mu_1 E\left(\frac{E}{E_0}\right)^{\alpha} + v_{sat}\left(\frac{E}{E_1}\right)^{\beta}}{1+\left(\frac{E}{E_0}\right)^{\alpha}+\left(\frac{E}{E_1}\right)^{\beta}} \tag{2.2}$$

Here μ_0 is the low-field mobility, μ_1 is the high-field mobility, E_0 and E_1 are the indicators of low- and high- electric-field, v_{sat} is the saturation velocity, and α and β are power indices.

In the present work, with the exception of low-field mobility, parameters of (2.2) were adopted from the work of AlOtaibi *et al.* [31]. The low-field mobility was provided by the Hall measurements performed on the investigated devices. Table 2.1, tabulates the value of the parameters of (2.2). Figure 2.1 illustrates the velocity versus electric-field characteristics according to the two aforementioned transport models.

Table 2.1: Parameters used in (2.2)

Symbol	Description	Value
μ_0	Low-field mobility	1200 and 1300 cm^2/(V.s) for Al mole-fraction of 0.4 and 0.3
μ_1	High-field mobility	128 cm^2/(V.s)
E_0	Low electric field	2.06 × 10^4 V/cm
E_1	High electric field	12.79 × 10^4 V/cm
v_{sat}	Saturation velocity	1.94 × 10^7 cm/s
α, β	Power Index	1.33, 7.10

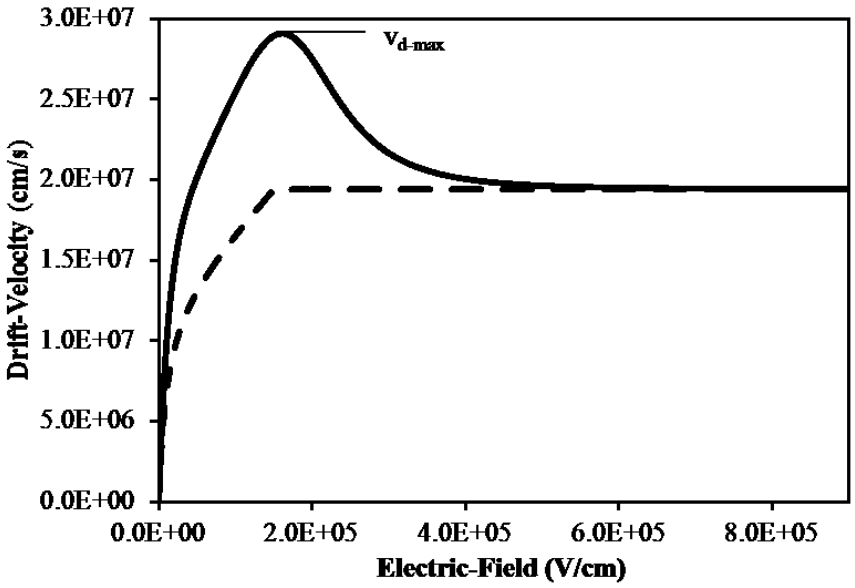


Figure 2.1: Electron drift-velocity versus electric-field characteristics of AlGaN/GaN 2DEG. The solid line represents mobility model represented by (2.2) and the dashed line represents the mobility model of (2.1).

According to the analytical model of Loghmany *et al.* [30], the channel of a nonself-aligned AlGaN/GaN HFET is considered in the form of a tandem connection of one gated HFET (situated under the gate-electrode) and two ungated HFETs in the drain- and source-access regions. Figure 2.2 identifies the aforementioned regions of this model. Whereas normally the source-access region operates under low electric-fields, the gated HFET and the ungated HFET situated in the drain-access region are exposed to high electric-fields, as drain bias increases. As a result, the aforementioned model considers these two parts of the channel in the form of two regions: one operating under low electric-field (which is referred to as "linear") and a second region in which the electric-field has exceeded the saturation electric-field in the case of Ridley's mobility model, and electric-field corresponding to peak electron-velocity (i.e., $v_{d\text{-}max}$) in the case of Polyakov's mobility model (which is referred to as "saturation"). The "saturation"

regions of both the gated HFET and the ungated HFET of drain-access region are formed closer to the drain-edge of the gate.

This analytical model is based on current-continuity, continuity of electric-field, and drift-diffusion transport formalism. As by-products of the calculation of drain-current, the model provides the variation of channel-potential, electric-field, and drift-velocity along the channel. As a result, in evaluation of the scalability of the drain-current characteristics, the resulting profile of the variation of electron drift-velocity under the gate is also used, in order to establish the link between gate-length scaling and average drift-velocity under the gate-electrode as L_G and L_{GD} are changing. The average electron-velocity under the gate-electrode is calculated in terms of the following averaging expression:

$$v_{avg} = \frac{\int_0^{L_G} v(x)\, dx}{L_G} \tag{2.3}$$

Here v_{avg} is the average electron-velocity, $v(x)$ is the electron-velocity under the gate, and L_G is the gate-length. Further details about this model are presented in [30].

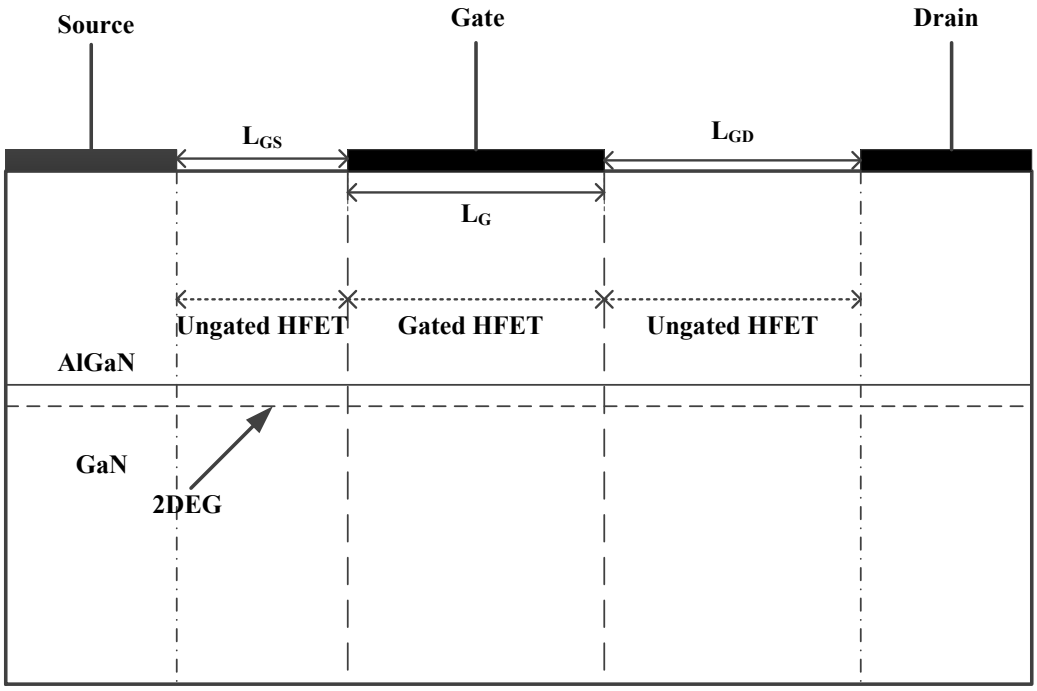


Figure 2.2: Basic schematic diagram of a nonself-aligned AlGaN/GaN HFET. L_{GS}, L_G, and L_{GD} represent the source-access region length, gate-length, and drain-access region length, respectively.

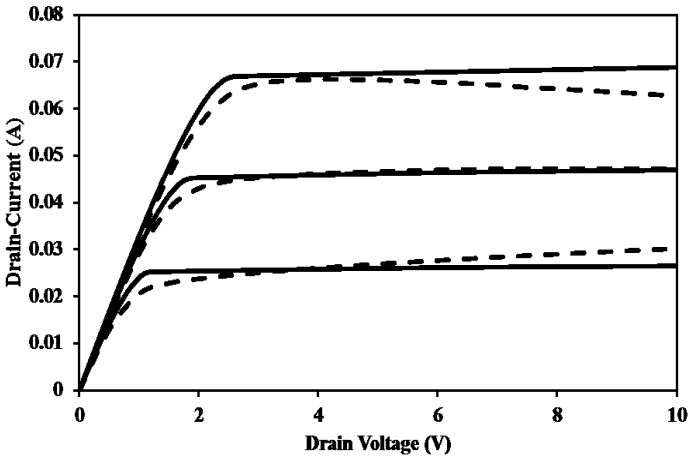
In the present work the experimental drain current-voltage characteristics (i.e., I_D-V_D) of a group of devices with different values of Al-mole fraction, L_G, and L_{GD} were used in validating the model. The devices were fabricated on AlGaN/GaN heterostructure layers grown by metalorganic chemical vapor deposition (i.e., MOCVD) on sapphire substrate. The epitaxial layers of all samples were composed of a 17 nm thick $Al_xGa_{1-x}N$ barrier layer, on top of an unintentionally doped GaN grown on an AlN buffer layer. Al composition "x" in the $Al_xGa_{1-x}N$ barrier was 0.3 and 0.4. Hall measured 2DEG carrier concentration of the samples with Al composition of 0.3 and 0.4 were equal to 1.14 x 10^{13} and 1.5 x 10^{13} cm^{-2}, respectively. The room temperature 2DEG Hall mobilities of the samples with Al composition of 0.3 and 0.4 were approximately equal to 1300 and 1200 $cm^2/V.s$, respectively. The devices had T-type gates with a gate width of 200 μm and

gate-source spacing (i.e., L_{GS}) of 0.7 μm. Devices with variable gate-length (L_G) of 0.6, 0.7, 0.8, and 0.9 μm and gate-drain spacing (L_{GD}) of 0.5, 0.9, 1, 2, and 3 μm were considered. Through plasma-enhanced chemical vapor deposition (i.e., PECVD), SiN films were deposited to passivate the exposed surfaces of all HFETs [39]. The Hall measurement data and structural information of the devices are introduced to the analytical model.

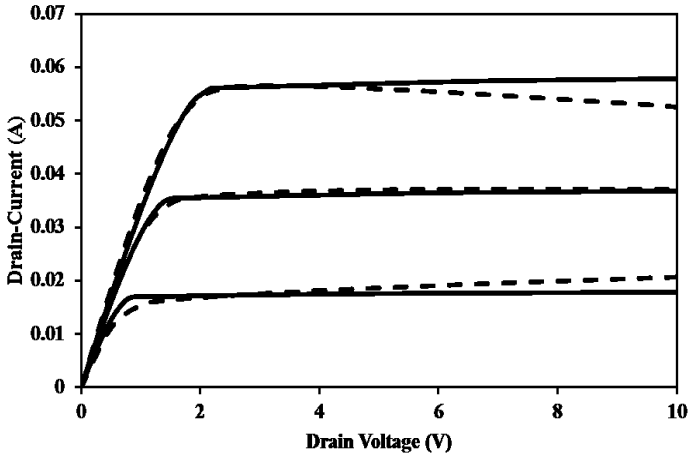
2.4 Results and Discussions

As an evidence for the validity of the analytical model of Loghmany *et al.*, this model was used to reproduce the I_D-V_D characteristics of the devices indicated in section 2.2. Although as indicated in [30], this model lacks the possibility of modeling the self-heating effect (observed at large V_{DS} and V_{GS} values), and also the buffer's leakage current (which is most obvious at V_{GS} values close to threshold, and large V_{DS} values), for a wide range of V_{DS} and V_{GS} values superb match to the experimental I_D-V_D characteristics was obtained. Figure 2.3 illustrates this match for both values of the Al-mole fraction, and a few values of L_G and $L_{GD.}$ In obtaining this match, for "x" of 0.3 and 0.4 source and drain series parasitic contact-resistance (i.e., R_S and R_D) of 11, and 9.5 Ω were introduced to the analytical model, respectively.

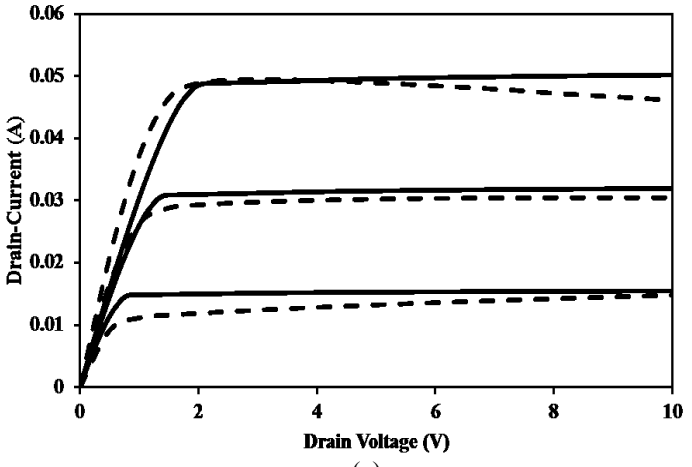
In order to compare the capabilities of the drift transport characteristics expressed in (2.1) and (2.2), (2.1) was also adopted to the analytical model of [30]. In these simulations, same values of parasitic contact-resistance were adopted. As shown by Loghmany *et al.*, adoption of (2.1) results in an underestimation of drain-current in I_D-V_D characteristics.



(a)



(b)



(c)

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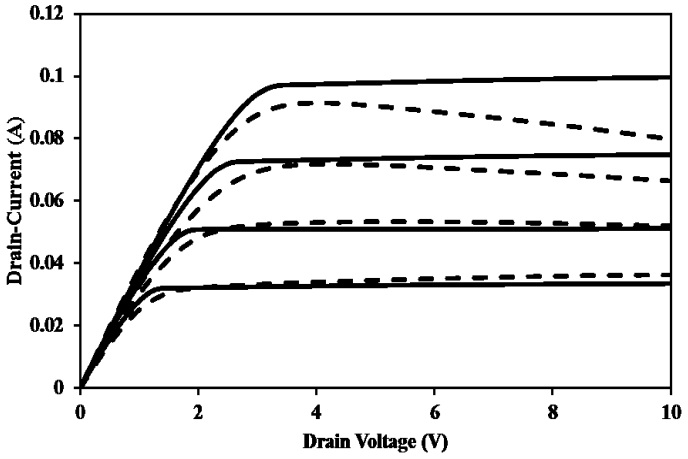

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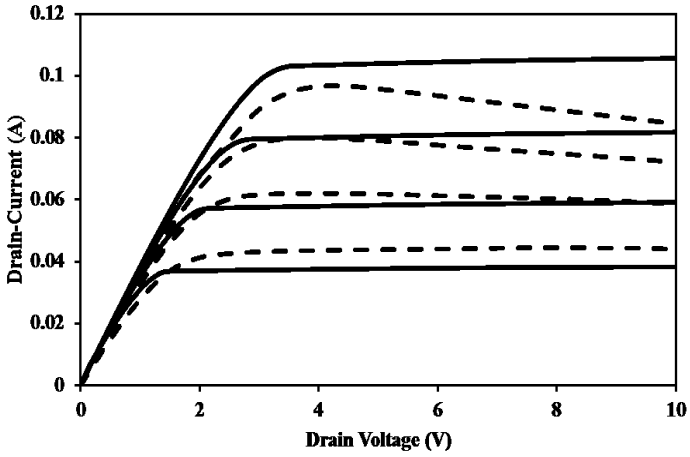
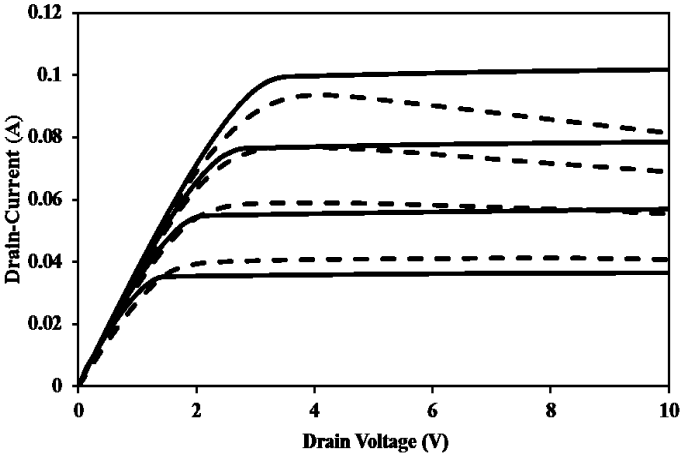


(e)



(f)

Figure 2.3: I_D-V_D characteristics based on the model (solid line) and the experimental results [39] (dashed line) for V_{GS}=0 V to V_{GS} =-1.0 V with -0.5 V steps, Al mole fraction of 0.3 and gate length of 0.7 µm, 0.8 µm, and 0.9 µm in (a), (b), and (c), respectively, and V_{GS}=-0.5 V to V_{GS} =-2.0 V with -0.5 V steps, Al mole fraction of 0.4 and gate length of 0.7 µm, 0.8 µm, and 0.9 µm in (d), (e), and (f), respectively. Gate-drain spacing length is 1 µm in (b), (c), (e), and (f), and 2 µm in (a) and (d).

Figure 2.4 illustrates the variation of electron drift-velocity under the gate-electrode resulting from adoption of the two transport models (i.e., (2.1) and (2.2)), for a variety of V_{DS}'s and V_{GS} equal to zero volt (for "x" of 0.3 and L_G equal to 0.9 μm). As observed in figure 2.4, for V_{DS} values corresponding to the early drain-current saturation, (2.2) predicts a maximum value of drift-velocity much higher than the value predicted by (2.1). This is of course expected from figure 2.1. However, as V_{DS} is further increased (i.e., deep saturation of I_D-V_D), instead of forming an expanding region with highest drift-velocity at the drain-edge of the gate, a region of saturated velocity (which is smaller than $v_{d\text{-}max}$) is going to form in this part of the channel. This is while the high drift-velocity region, instead of expansion is merely pushed towards the source-side of the gate-electrode (Figure 2.4(a)). In contrast to this, adoption of (2.1) (as shown in Figure 2.4 (b)) simply indicates the formation of a region with saturated drift-velocity at the drain-edge of the gate for V_{DS} values corresponding to early saturation of drain-current, whereas larger values of V_{DS} expand this region of highest velocity towards the source-side of the gate-electrode.

The predictions of Ridley's purely-saturating drift transport characteristics are in line with the behavior of silicon MOSFETs. It has been observed that at an identical bias point, in a silicon MOSFET of shorter channel-length along a proportionally longer part of the channel electrons will fly at their saturated drift-velocity [40]. In this case, the drift-velocity along the channel prior to this part is smaller than v_{sat}. As a result, the smaller the gate-length, the larger will be the average electron-velocity. Consequently, it is expected from Ridley's transport model that the average electron drift-velocity and also drain-current will improve as the gate-length is being scaled down. Although adoption of

Ridley's mobility model to AlGaN/GaN HFETs predicts such a scaling-trend, the obvious differences in how the regions of negative differential mobility and velocity-saturation are formed and evolved with V_{DS} (as shown in Figure 2.4), demands a re-evaluation of the scaling-trend of the current-drive of these devices with L_G.

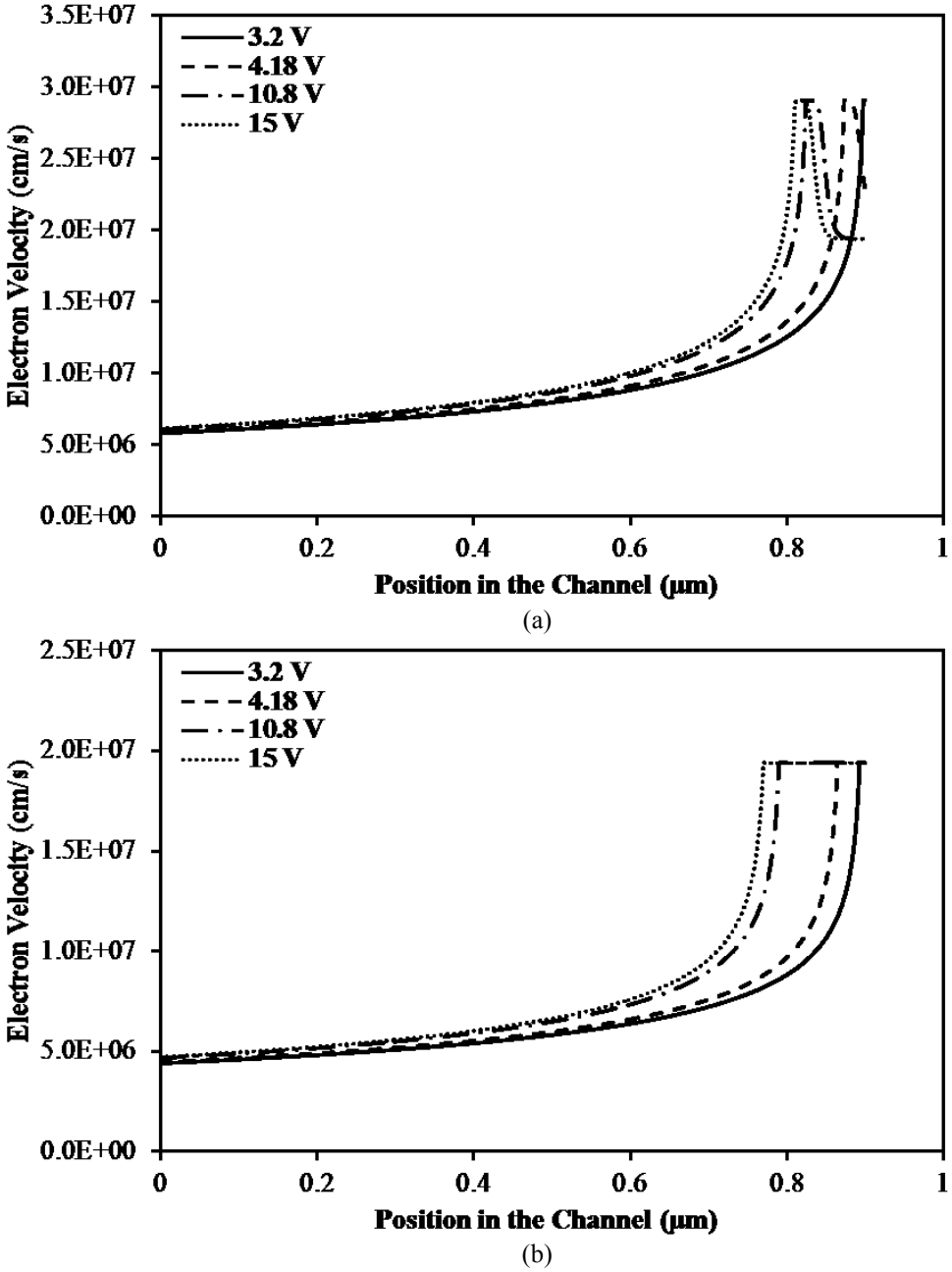
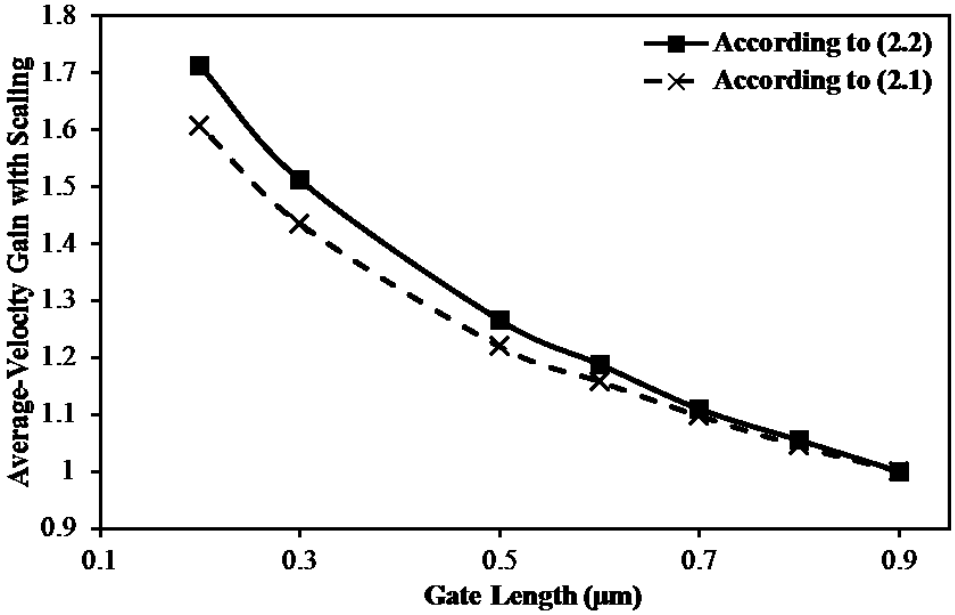


Figure 2.4: Electron drift-velocity under the gate for drain voltages of 3.2 V, 4.18 V, 10.8 V, and 15.0 V, using (2.2) and (2.1) in (a), and (b), respectively. L_G=0.9 µm, V_{GS}=0 V, and Al mole-fraction in barrier is 0.3.

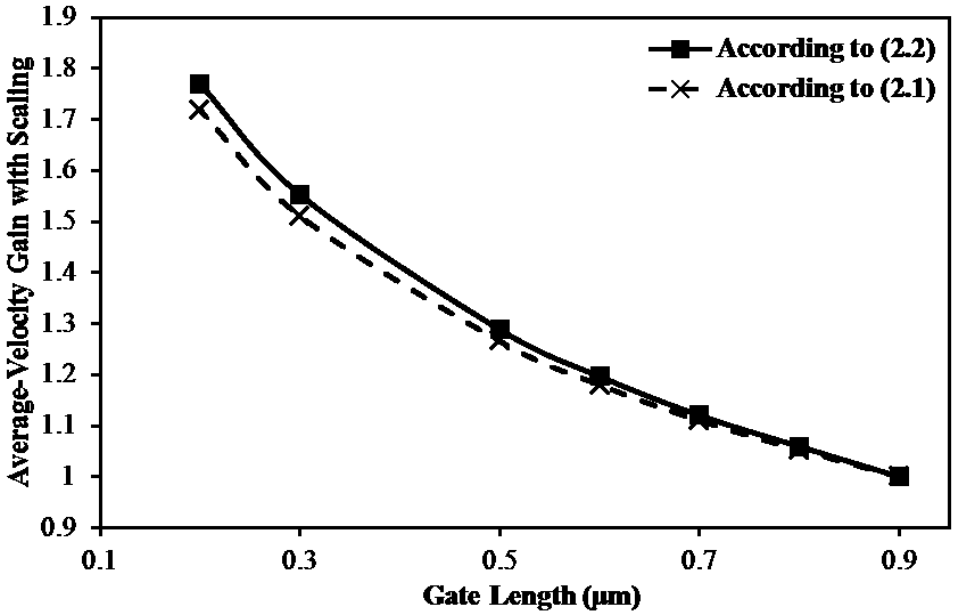
The presence of steady-state peak in drift transport characteristics of a variety of semiconductor technologies such as GaAs and InP, also hint towards the prevalence of a different trend in scaling of the current-drive with L_G in those other semiconductor technologies. However, the overwhelming presence of a much higher peak drift-velocity, which in addition has a much wider v_d-E profile than those other semiconductors, forecasts a much more important outcome in modifying the gate-length scaling-trend of AlGaN/GaN HFETs.

Figure 2.5 illustrates the result of gate-length scaling on the improvement in average electron drift-velocity under the gate-electrode of AlGaN/GaN HFETs, according to the two aforementioned mobility models (for one V_{GS} value and a variety of V_{DS} values). In this figure, L_G is chosen equal to 0.9, 0.8, 0.7, 0.6, 0.5, 0.3, and 0.2 μm, L_{GS} is equal to 0.7 μm, and L_{DS} is equal to 1 μm. Although for the first four larger values of L_G, the presented results according to (2.2) were validated with the experimental data, in evaluation of devices of smaller gate-length and also simulations based on (2.1) same set of parameters, including contact resistance, were simply adopted from the experimentally-validated simulations.

Figure 2.5 shows that with gate-length scaling, the average electron drift-velocity of the 2DEG channel improves. In order to evaluate the amount of improvement in average drift-velocity, the calculated values for each value of L_G are divided by the average drift-velocity calculated for the largest considered value of L_G (i.e., 0.9 μm). This form of presentation facilitates the comparison between the gains in drift-velocity according to the two mobility models.



(a)



(b)

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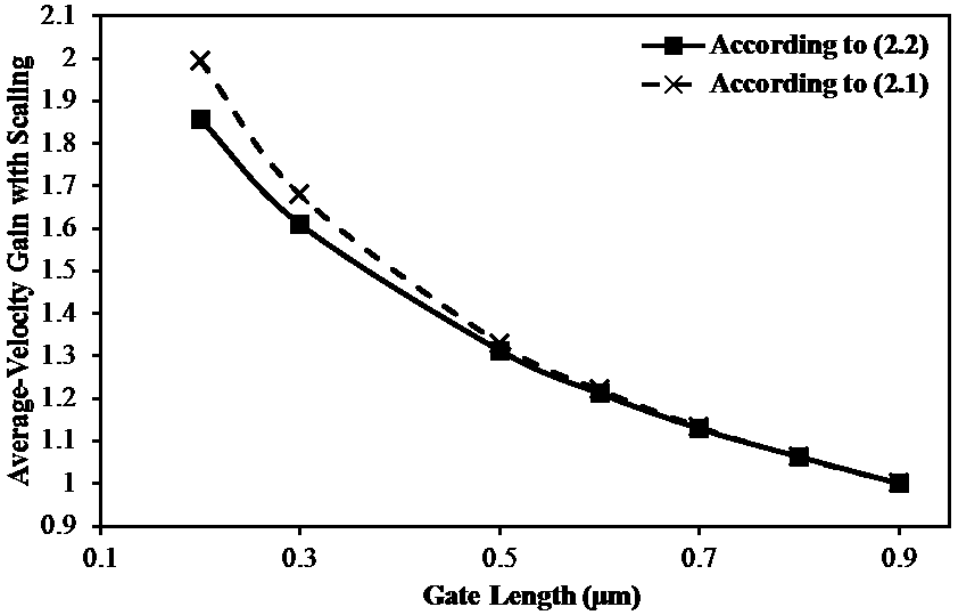

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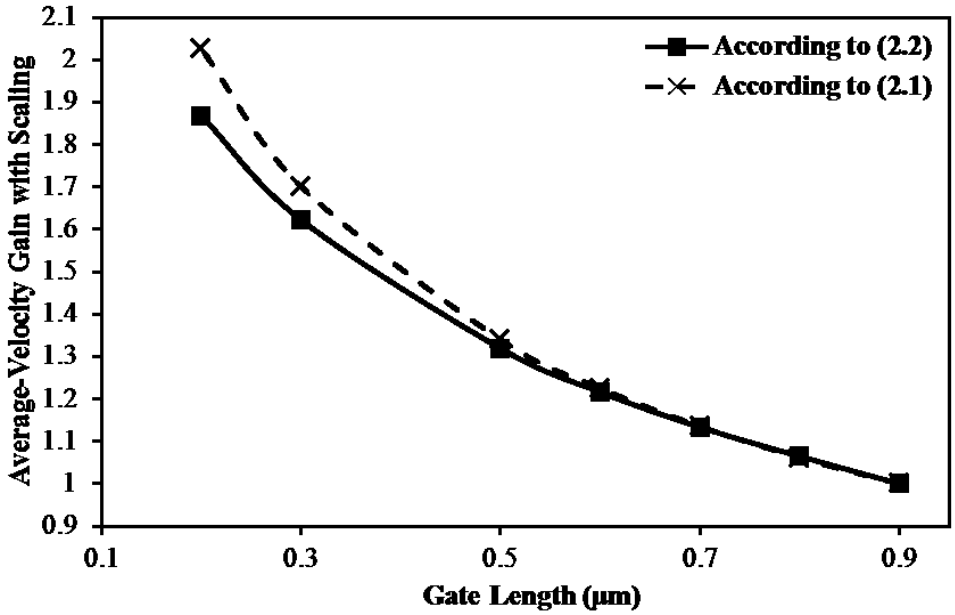


(d)

Figure 2.5: Proportional change in average electron drift-velocity with gate-length scaling using transport model of (2.2) (solid line) and (2.1) (dashed line) for drain voltage V_{DS} of 3.2 V, 4.18 V, 10.8 V, and 15.0 V in (a), (b), (c), and (d), respectively. Al mole-fraction in AlGaN is 0.3 and $V_{GS}–V_T$ = 1.75 V.

As shown in figure 2.5, whereas for V_{DS} values closer to the linear regime of operation of an AlGaN/GaN HFET, (2.1) shows less improvement in average drift-

velocity by the L_G-scaling, deeper into the saturation regime of operation (i.e., higher V_{DS}) this trend reverses. This reversal of trends is caused by the presence of negative differential mobility in (2.2) (Figure 2.1). For low values of a maximum electric-field formed at the drain-edge of the gate (i.e., low V_{DS} values), higher low-field drift-velocity predicted by (2.2), forecasts a further improvement in average electron-velocity as the maximum electric-field is made larger by gate-length scaling (as long as this value is still limited to the electric-field corresponding to $v_{d\text{-}max}$). However, as the maximum electric-field at the drain-edge of the gate becomes larger than this value, according to (2.2), a region of reduced drift-velocity will form at the drain-edge of the gate-electrode (Figure 2.4(a)). Formation and expansion of this region by reducing the L_G, causes a reduction in gain in average drift-velocity as L_G is made smaller. According to figure 2.1, such a negative differential mobility region and its implications on scaling are overlooked in the approximate mobility model of (2.1).

As shown in figure 2.6, the scaling-trends were equally observed for the two considered values of "x". In this figure, due to the difference between the threshold-voltage of the two samples, instead of evaluation at the same value of V_{GS}, the effective threshold voltage (i.e., $V_{GT} = V_{GS}-V_T$) is taken to be the same.

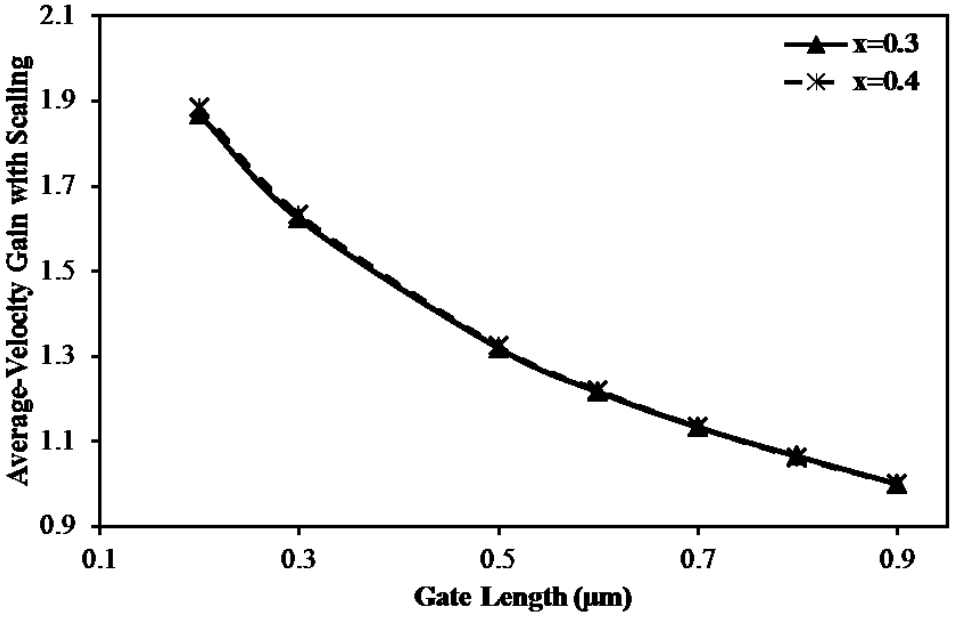


Figure 2.6: Change in average electron drift-velocity with gate length scaling for Al mole-fraction "x" of 0.3 (solid line) and 0.4 (dashed line), for drain voltage V_{DS} of 15.0 V and $V_{GS} - V_T = 1.75$ V.

Figure 2.7 illustrates the variation of the proportional size of the combined regions of saturated velocity (for both mobility models) and negative differential mobility (for mobility model (2.2)) with L_G, for all V_{DS} values indicated in figure 2.5. As illustrated in this figure, at higher V_{DS} values and especially smaller L_G's, the approximate purely-saturating transport model of (2.1), in contrast to (2.2) predicts a drastically larger proportion of the gated channel to be operating under electric-fields larger than the value corresponding to the peak drift-velocity. The combined role of this observed trend and the presence of a region of negative differential mobility in the more accurate transport characteristics of (2.2), support our earlier suggestion that a smaller gain in current-drive of scaled AlGaN/GaN HFETs, than the value predicted by the approximate transport model of (2.1), is realistically achievable.

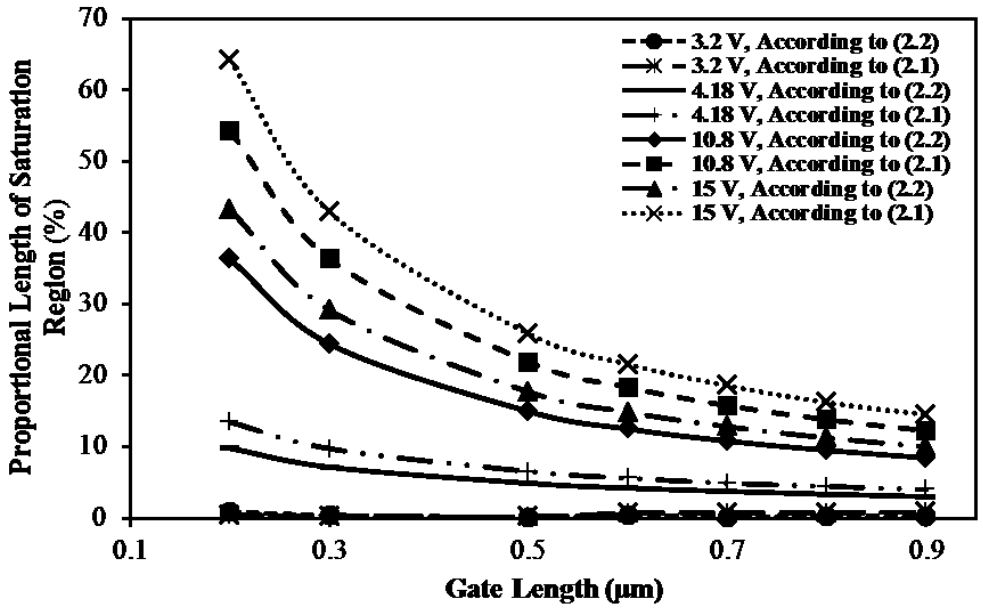


Figure 2.7: Variation of the percentage of gated channel-length operating under "saturation" with gate length according to both mobility models (i.e., (2.1) and (2.2)) and for drain voltage V_{DS} of 3.2, 4.18, 10.8, and 15.0 V, respectively.

Whereas it is expected that a larger parasitic contact resistance has a limiting effect on the maximum electric-field at a given bias point, and as a result average drift-velocity, it is anticipated that the expected improvements in realization of Ohmic contacts to AlGaN/GaN 2DEG [41-44] can be very consequential in determining the gain in drain-current through L_G scaling. Simulations according to the two aforementioned mobility models for two extra values of contact resistance (i.e., 5 and 0 Ω) were performed, while V_{DS} values were chosen for deep saturation of I_D-V_D characteristics. As illustrated in figure 2.8, the expected gain in average electron-velocity forecasted by the two mobility models diverge even further if the contact resistance is reduced below the 11 Ω value, which was determined by the match to the experimental data. Although the 0 Ω contact resistance is not realizable, this value was taken for comparison purposes.

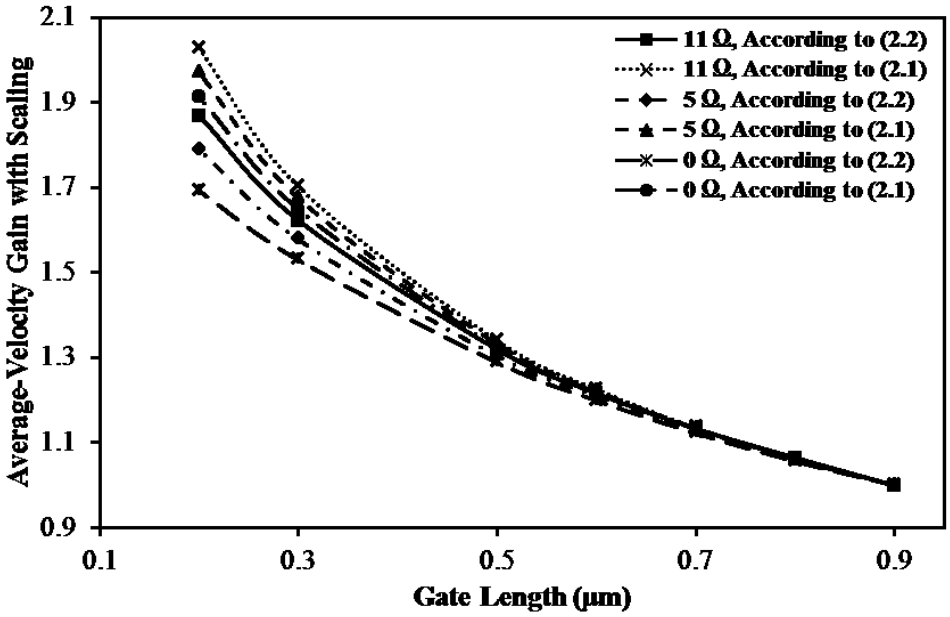


Figure 2.8: Change in average electron drift-velocity with gate-length scaling for both transport models with contact resistances of 11 Ω, 5 Ω, and 0 Ω and for drain voltage V_{DS} of 15.0 V. Al mole-fraction in AlGaN is 0.3 and $V_{GS} - V_T = 1.75$ V.

Figure 2.9 illustrates the effect of reduction in contact resistance on proportional length of negative differential mobility region and saturation region, as gate-length scaling is performed. Comparing this figure and figure 2.7, it is observed that with a reduced value of contact resistance, predictions of (2.1) and (2.2) diverge slightly further. This is in agreement with our earlier observations on the lowering of the predicting power of (2.1), as the contact technology is improved.

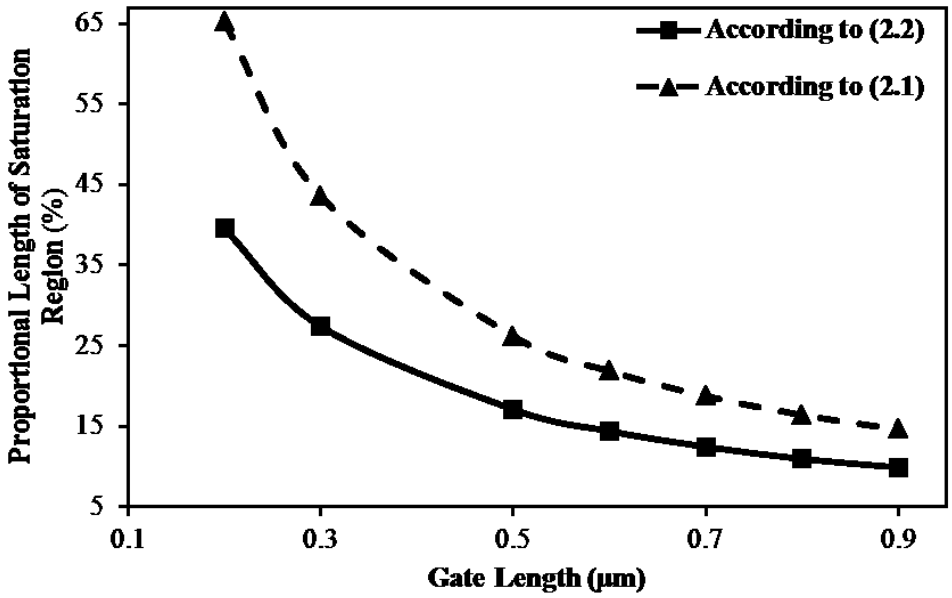
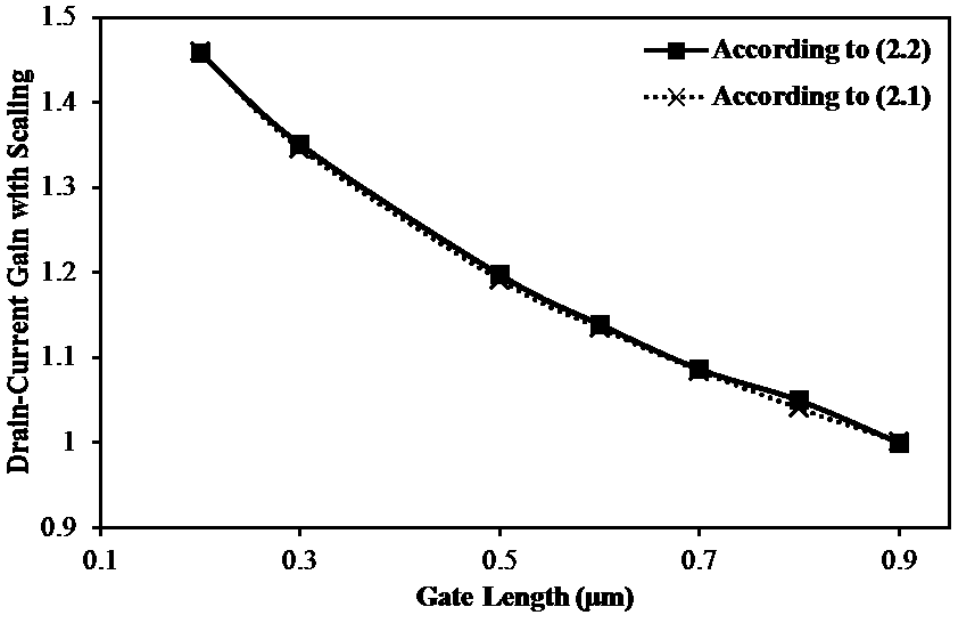
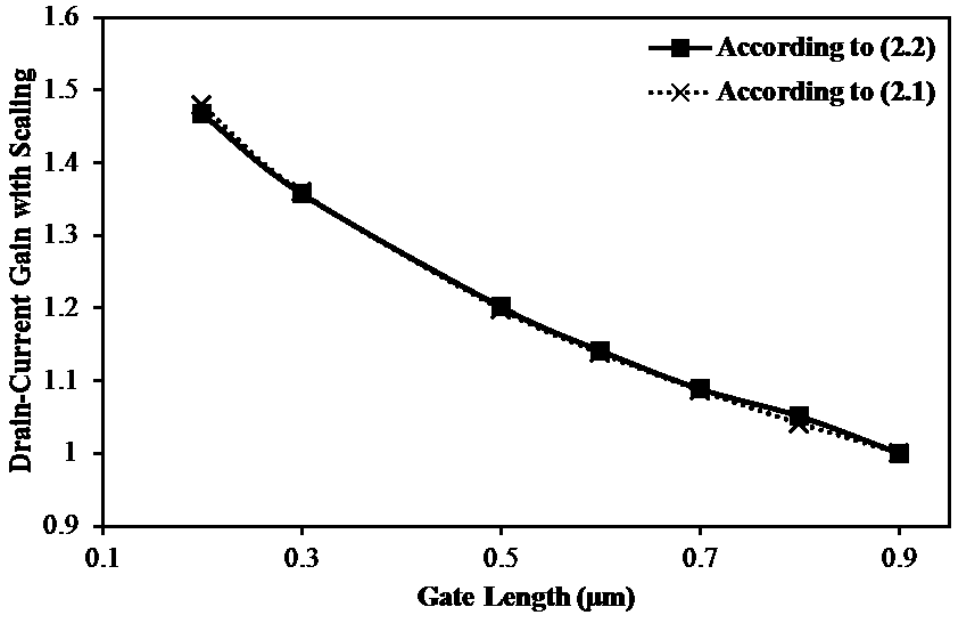


Figure 2.9: Variation of the percentage of gated channel-length operating under "saturation" with gate length according to both mobility models (i.e., (2.1) and (2.2)), for contact resistances of 0 Ω, drain voltage V_{DS} of 15.0 V. Al mole-fraction in AlGaN is 0.3 and $V_{GS} - V_T = 1.75$ V.

Figures 2.5(c) and 2.5(d) support the earlier prediction that the expected gain in average drift-velocity according to (2.1) is an overestimation of what should be expected from L_G-scaling of AlGaN/GaN HFET technology. Whereas so far the discussion is limited to the presentation of gain in average electron-velocity with L_G-scaling, figure 2.10 shows the expected gain in drain-current according to the two aforementioned mobility models. This figure also hints towards the insufficiency of (2.1) in forecasting the scalability of drain-current drive of AlGaN/GaN HFETs. From the diverging predictions of the two mobility models on the proportional length of the saturation region (Figure 2.7) and also average electron-velocity (Figure 2.5), a much bigger difference in terms of drain-current drive is expected. However, presence of a large drain-access region is observed to have a masking effect on these differences. It is expected that in devices of smaller L_{GD}, this difference will be more meaningful. This observation is supported by our investigation of scaling-trend of drain-current drive with L_{GD}.



(a)



(b)

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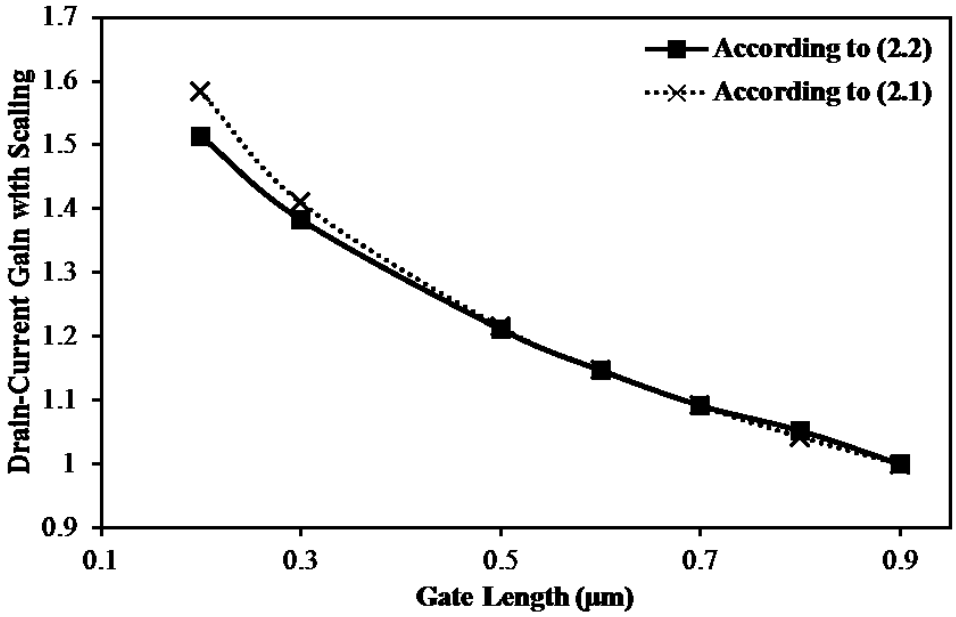

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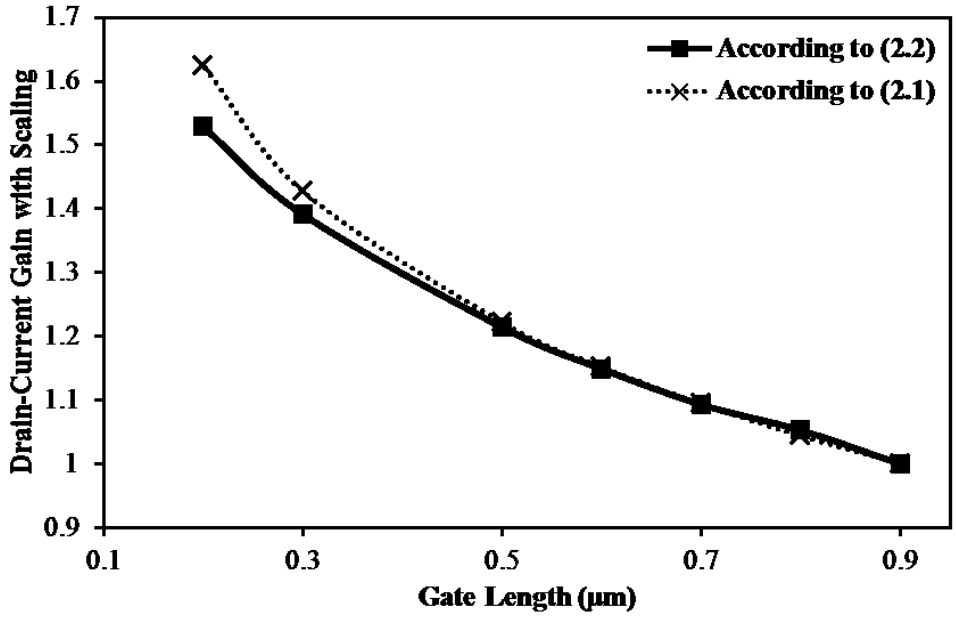


(d)

Figure 2.10: Change in drain current with gate-length scaling for both transport models with contact resistances of 11 Ω and for drain voltage V_{DS} of 3.2 V, 4.18 V, 10.8 V, and 15.0 V in (a), (b), (c), and (d), respectively. Al mole-fraction in AlGaN is 0.3 and $V_{GS} - V_T = 1.75$ V.

The formation of high electric-field region in a nonself-aligned HFET is not merely limited to the gated channel. Such a high electric-field region is also formed in the

vicinity of the gate-electrode in the drain-access region. For that reason, the study was extended into the scaling of L_{GD} for one fixed value of L_G, and it is observed that the predictions of (2.1) overestimate the drain-current drive (Figure 2.11).

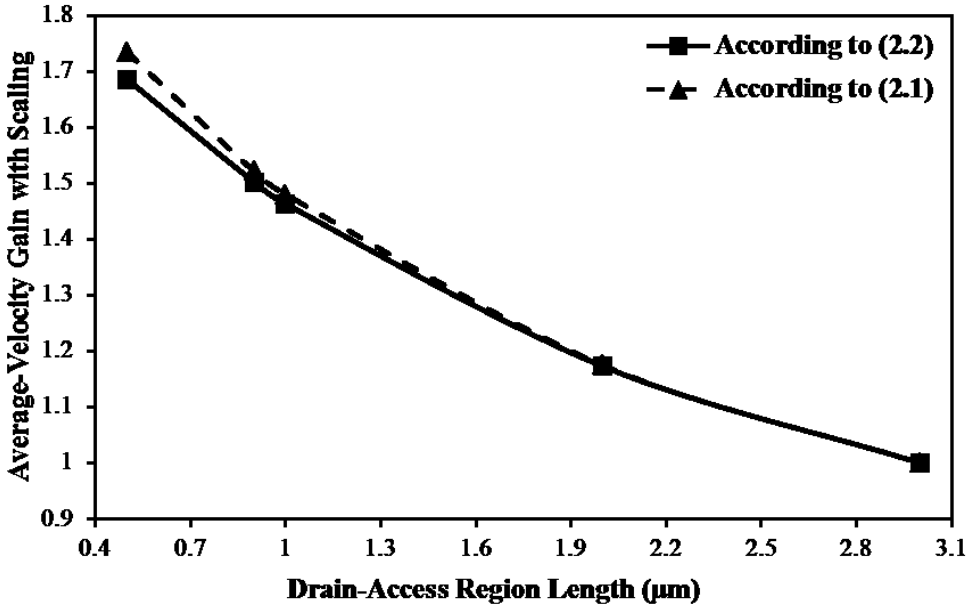


Figure 2.11: Change in average electron drift-velocity (over L_G plus L_{GD}) with drain-access region length scaling using (2.2) (solid line) and (2.1) (dashed line) for drain voltage V_{DS} of 15.0 V, gate length L_G of 0.7 μm and gate-drain spacing length L_{GD} of 0.5, 0.9, 1, 2, and 3 μm, respectively. Al mole-fraction in AlGaN is 0.3 and $V_{GS} - V_T$=1.75 V.

2.5 Conclusion

Scalability of the drain current-drive with gate-length and length of the drain-access region of AlGaN/GaN HFETs has been studied. An approximate purely-saturating transport characteristics and a realistic transport model, with steady-state drift-velocity overshoot, have been considered in this study. It has been observed that the approximate purely-saturating transport model overestimates the gain in average drift-velocity as well as the gain in the drain-current, with gate-length scaling. This gain reduction has been shown to be further increased with expected improvements in Ohmic contact technology.

It has been shown that the pronounced presence of an overshoot in the drift transport characteristics of GaN plays an important role in forecasting the scalability of drain-current-drive of AlGaN/GaN HFETs.

Chapter 3

Temperature-dependent Study of Gate-lag and R_{DS}-dispersion of Island-, Fin-, and Mesa-isolated AlGaN/GaN HFETs

3.1 Abstract

Gate-lag and frequency-dispersion in the output resistance (i.e., R_{DS}) of AlGaN/GaN heterostructure field effect transistors in devices with three different sizes of isolation feature are experimentally investigated at 300, 350, and 400 K. Island-isolated (i.e., devices fabricated on arrays of fourteen islands of size 16 μm × 7 μm), fin-isolated (i.e., devices fabricated on narrow mesas of size 16 μm × 100 μm), and mesa-isolated (i.e., devices fabricated on conventional mesas of size 70 μm × 100 μm) device types are considered. Gate-lag is observed only in island-, and fin-isolated devices and at all measurement temperatures. R_{DS}-dispersion at frequencies above 1 MHz is, however, observed in all three device types. Exposure of the gate and Ohmic contacts to additionally dry-etched sidewalls is deemed responsible for the observed gate-lag in

island-, and fin-isolated devices. Defects in the GaN buffer layer are predicted to be responsible for R_{DS}-dispersion in all three device types.

3.2 Introduction

Large critical electric-field, superior two-dimensional electron-gas (i.e., 2DEG) concentration, very broad peak in the steady-state drift-velocity versus electric-field characteristics in addition to the advancements of material growth have made AlGaN/GaN Heterostructure Field Effect Transistors (i.e., HFETs), suitable candidates for application in high-frequency and high-power electronic systems [25-27], [45-46]. Along with this growing interest, considerable attention has been drawn to reliability of these devices, which is oftentimes proven deficient due to the existence of trap-centers and defects [18-23].

As indicated earlier in chapter 1, the non-centrosymmectric nature of Wurtzite III-nitride crystals in addition to large piezoelectric coefficients and built-in strain in the pseudomorphically grown AlGaN/GaN heterostructures are responsible for induction of an unprecedented 2DEG carrier concentration at the AlGaN/GaN heterointerfaces [5], [15]. While advantageous from the point of view of offering large current-drive, this high 2DEG carrier concentration leads to the depletion-mode operation of AlGaN/GaN HFETs. Although depletion-mode FETs offer proper sources for current, as switches their performance suffers from the presence of standby power.

Due to its polar nature, one of the major challenges of AlGaN/GaN HFET technology is the realization of enhancement-mode devices [47-51]. Valizadeh *et al.* have proposed the method of selective engineering of piezoelectric polarization [51], to control

the 2DEG charge concentration. According to this method, reduction of the size of the isolation mesa contributes to enhancing the chance for development of peel forces and consequently reduction of the built-in strain. This reduction in strain and piezoelectric polarization consequently reduces the 2DEG electron concentration. Valizadeh *et al.*, have experimentally demonstrated supportive evidence in terms of registration of less negative threshold voltage for island-, and fin-isolated AlGaN/GaN HFETs with reduction of the mesa size, while maintaining the values of maximum drain-current density and gate transconductance [51].

Considering the recent development of new device types based on this technology, evaluation of gate-lag and frequency-dispersion characteristics of these devices are deemed necessary. Gate-lag and frequency-dispersion present effective measures for evaluation of high-frequency operation of HFETs. Gate-lag is referred to as the time delay in the drain-current, while a turn-on pulse of nanosecond rise-time is applied to the gate electrode. R_{DS}-dispersion is known as the variation of the small-signal output-resistance (i.e., R_{DS}) of the device, as the frequency is increased. Both gate-lag and R_{DS}-dispersion provide information on trap levels, transient response, and high-frequency performance of the device. Surface related trap-centers and material defects have been reported by several investigators, as the possible reasons for gate-lag and frequency-dispersion [52-56]. The novelty of the fabrication technology of the newly proposed island-, and fin-isolated AlGaN/GaN HFETs, promotes the need for studying the gate-lag and R_{DS}-dispersion characteristics of these device types at different temperatures, and comparing them with the conventional mesa-isolated devices.

In the present work, gate-lag and R_{DS}-dispersion characteristics of island-, fin-, and mesa-isolated devices have been studied at different temperatures (i.e., 300, 350, and 400 K). Gate-lag has been observed in island-, and fin-isolated devices, whereas R_{DS}-dispersion has been observed in all three device types.

In section 3.3, device structures and the details of the experimental setup are described. Experimental results and analysis, including the discussions on the possible reasons for the observed gate-lag in island-, and fin-isolated devices and R_{DS}-dispersion at high-frequencies for all device types are presented in section 3.4. Conclusions are presented in section 3.5.

3.3 Device Structures and Experimental Setup

As indicated in section 3.2, in this study, gate-lag and R_{DS}-dispersion characteristics of AlGaN/GaN HFETs of three different isolation types are investigated. All these three types of devices were realized as two-finger HFETs on the same epilayer. Island-isolated devices were fabricated on array of very small mesas of size 16 μm × 7 μm, fin-isolated devices were fabricated on narrow mesas of size 16 μm × 100 μm, and mesa-isolated devices were fabricated on large mesas of size 70 μm × 100 μm. The total effective gate width of island-isolated devices, composed of fourteen islands of 7 μm width, is 98 μm. All devices have gate-length of 1 μm, gate-drain spacing length of 2 μm, and gate-source spacing length of 1.1 μm. The thickness of AlGaN barrier is 20 nm, GaN channel is 200 nm thick, and Al mole fraction of AlGaN barrier is 0.3 (Figure 3.1). The three device types have the same height of isolation-feature (i.e., 300 nm). Further details about the device structures are presented in [51].

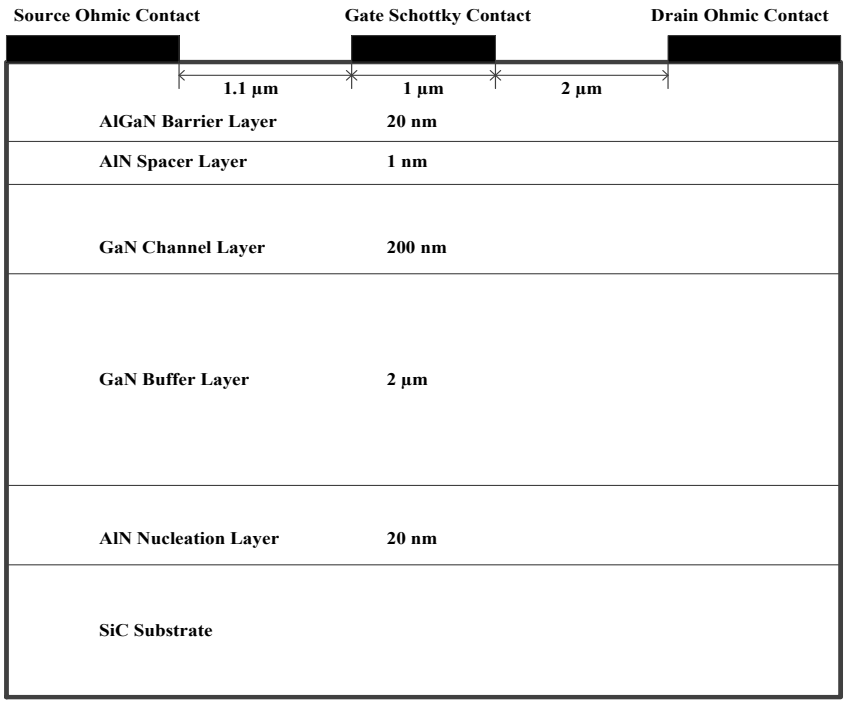
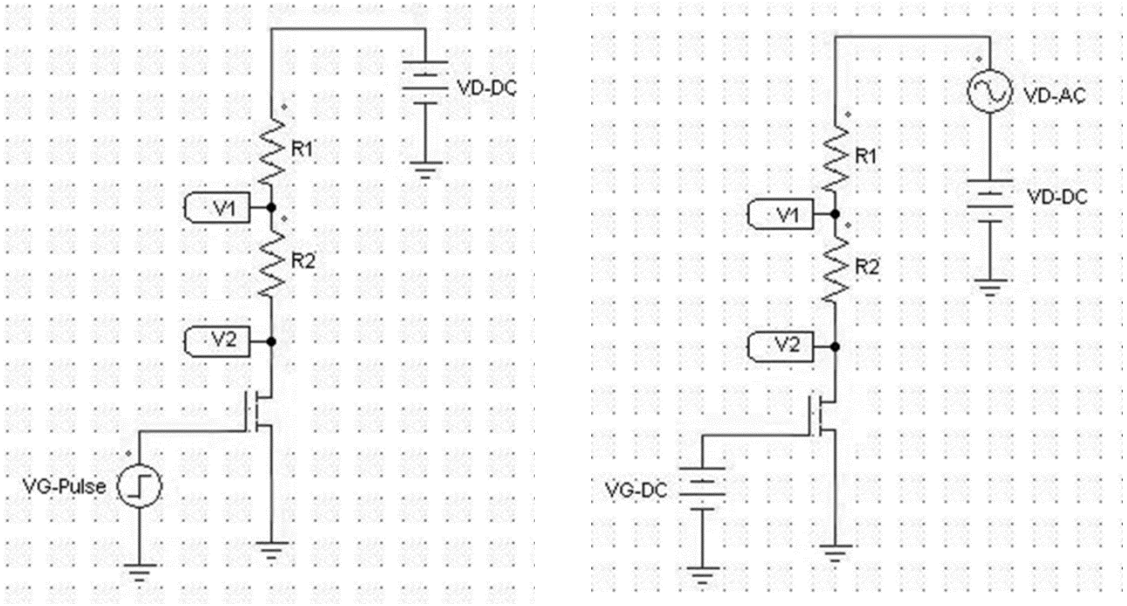


Figure 3.1: Schematic cross-section of the studied AlGaN/GaN HFET. Figure not in scale.

The temperature-controlled chamber of a MMR-LTMP4 probe station was used to perform the measurements. This probe station can reliably maintain the temperature between 80 and 500 K. Coaxial cables were used to prevent the unwanted noise. Figure 3.2 illustrates the measurement setups. For gate-lag measurement, a nanosecond rise-time gate turn-on pulse with low- and high-states of -10 and 0 V, respectively, was applied at a fixed drain bias of 7 V. The low-state of the pulse is chosen well below the threshold voltage to ensure zero drain-current. For R_{DS}-dispersion measurement, the small-signal frequency of the AC signal generator was varied from 20 Hz to 20 MHz, while maintaining a quiescent gate bias of -1 V and drain bias of 10 V. The amplitude of the AC small-signal was 0.1 V.



(a) (b)

Figure 3.2: Gate-lag, and R_{DS}-dispersion measurement setup in (a), and (b), respectively.

For both measurements, the potentials V_1 and V_2 versus time were recorded using a digital oscilloscope. In gate-lag studies, according to figure 3.2 (a), the drain-current (i.e., I_D) is evaluated as:

$$I_D = \frac{\Delta(V_1 - V_2)}{R_2} \tag{3.1}$$

According to figure 3.2 (b), R_{DS} can be calculated, on the basis of the amplitude of small-signal sinusoidals recorded for V_1 and V_2, using the following expression:

$$R_{DS} = \frac{\Delta(V_2) \times R_2}{\Delta(V_1 - V_2)} \tag{3.2}$$

In these measurements, HP 8116A pulse/function generator was used, for generating the gate pulse and the excitation small-signal sinusoid. Tektronix DP04054 digital oscilloscope was used for recording the excitation signals and temporal variation of V_1 and V_2. Keithley 4200-SCS semiconductor characterization system was used to obtain the DC characteristics of the devices. Measurements were conducted in the order

of 300, 350, and 400 K. Unstressed devices were used in performing all the measurements. After each gate-lag and R_{DS}-dispersion measurement, the DC characteristics were verified versus the previously recorded characteristics. No significant degradation was found after each measurement. During measurements, the MMR-LTMP4 probe station was operated under low pressure and the temperature was controlled and monitored by the MMR-K20 temperature controller.

3.4 Experimental Results and Analysis

3.4.1 Gate-lag

There are many reports on observation of gate-lag in AlGaN/GaN HFETs [52-55]. According to many of these reposts, upon pulsing the gate voltage from off-state (i.e., V_{GS} much smaller than threshold voltage) to on-state, the drain-current originally jumps to only a certain proportion of the expected DC drain-current at the on-state value of the gate pulse. Following this jump, it is observed that the pulsed-mode drain-current gradually increases according to a saturating characteristic. This exponentially decaying improvement in drain-current is referred to as gate-lag.

Gate-lag is understood in terms of the difference between the rise-time of the gate pulse and the trapping/de-trapping time constant of trap-sites present in the vicinity of the channel. While electron trapping in the acceptor-type trap-sites in the off-state causes a drop in the channel electron concentration (and drain-current), de-trapping of electrons from these states tends to improve the channel electron concentration (and the drain-current). However, such a process if limited by a time constant longer than the rise-time

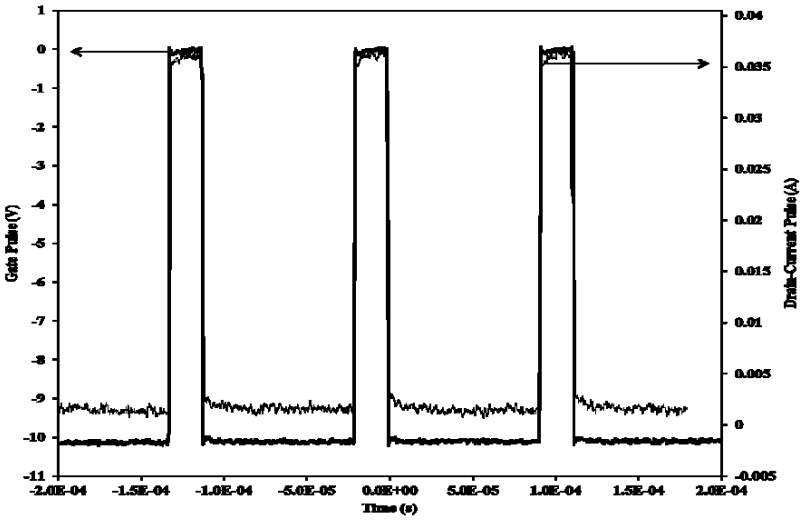
of the gate pulse, results in observation of gate-lag. As a result of this explanation, presence of gate-lag is linked to the role of fabrication process in forming new trap levels.

Across the devices considered in this study, figure 3.3 illustrates that both island-, and fin-isolated devices exhibit gate-lag at all temperatures. All three device types demonstrated a jump in drain-current with the application of the gate pulse. However, as shown in the expanded view presented in figure 3.4 only in island-, and fin-isolated devices, and not the mesa-isolated devices, this jump was followed by a saturating exponential characteristic (which is representative of gate-lag). These values in terms of percentages of DC drain-current are indicated in figure 3.4.

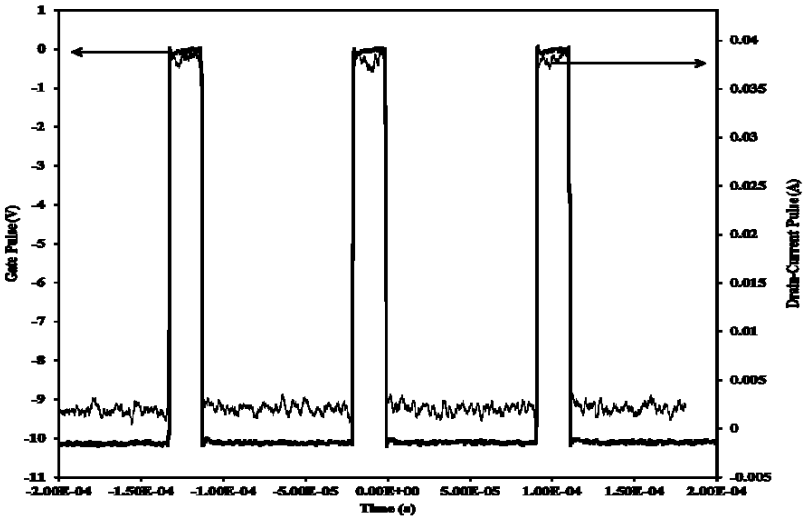
It has been reported by others that the time constant identified in gate-lag profiles follows a modified Arrhenius characteristics. Study of the variation of the time constant of the gate-lag profile with temperature has been shown to be able to identify energy levels of the trap-sites responsible for the observed gate-lag [52-53]. The trapping/de-trapping time constants extracted from figure 3.3, and the temperature-dependent Arrhenius plots are illustrated in figure 3.5. According to the modified Arrhenius characteristics, the temperature dependency of the trapping/de-trapping time constant (i.e., τ) is expressed by:

$$\tau = \frac{\tau_0}{T^2}\, exp\left(\frac{E_A}{K_B T}\right) \tag{3.3}$$

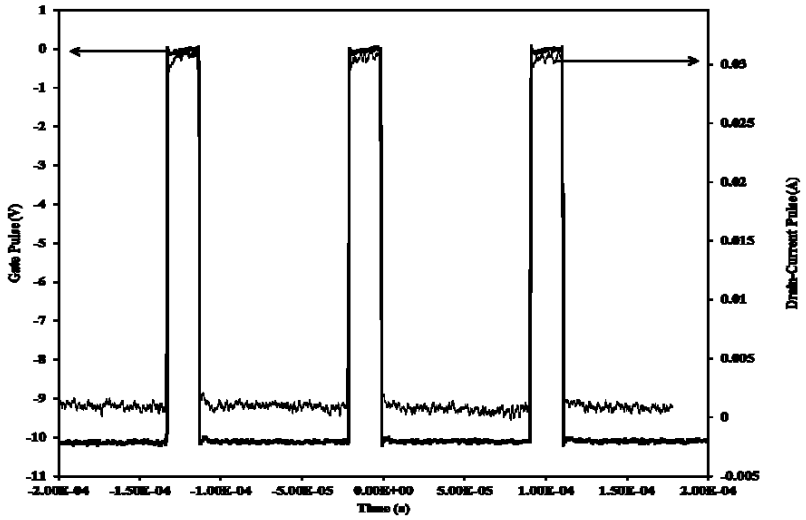
Here, τ_0 is proportionality constant, T is the temperature in Kelvin, E_A is the energy level of the responsible trap-site, and K_B is the Boltzmann constant.



(a)

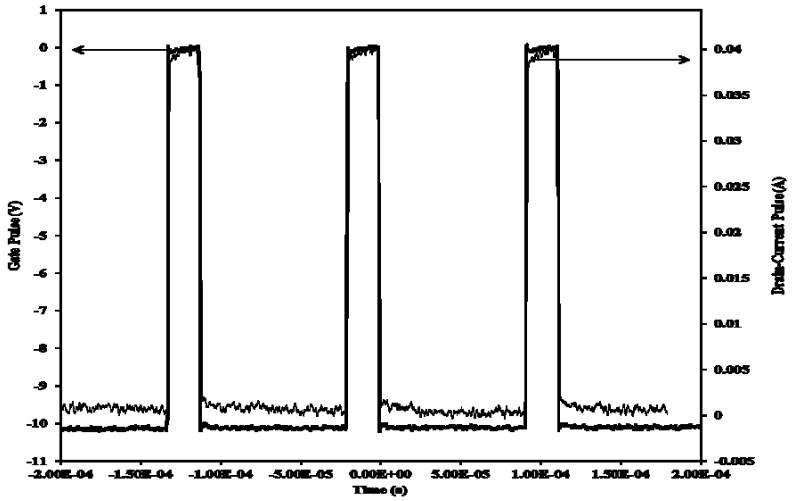


(b)



(c)

Figure 3.3: Continued on the next page.



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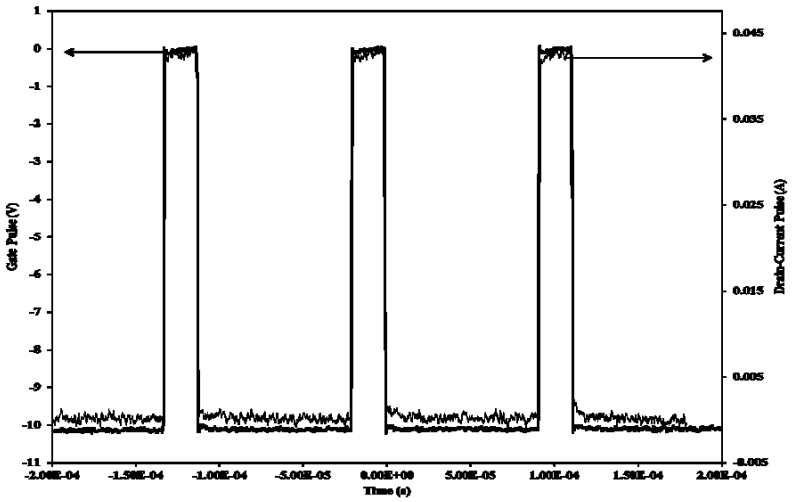

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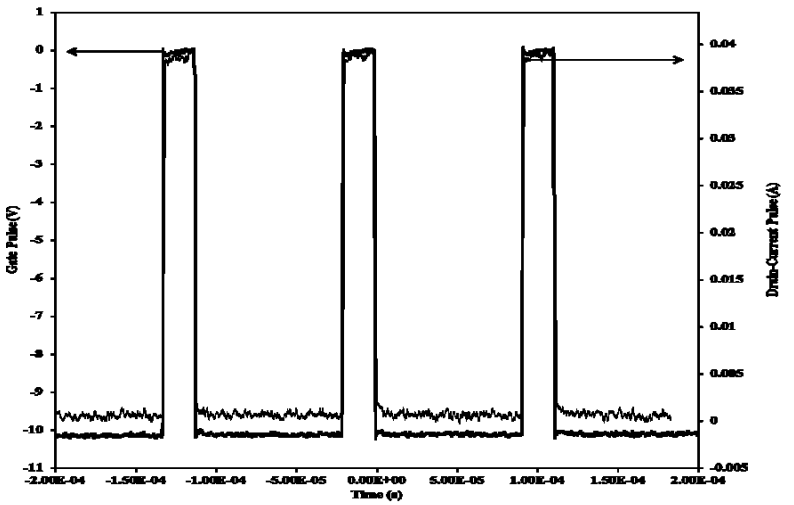


(f)

Figure 3.3: Pulsed-mode drain-current measurements, for island-isolated devices at 300, 350, and 400 K in (a), (b), and (c), respectively. And for fin-isolated devices at 300, 350, and 400 K in (d), (e), and (f), respectively. Darker lines represent the gate-pulse and lighter lines represent the drain-current pulse.

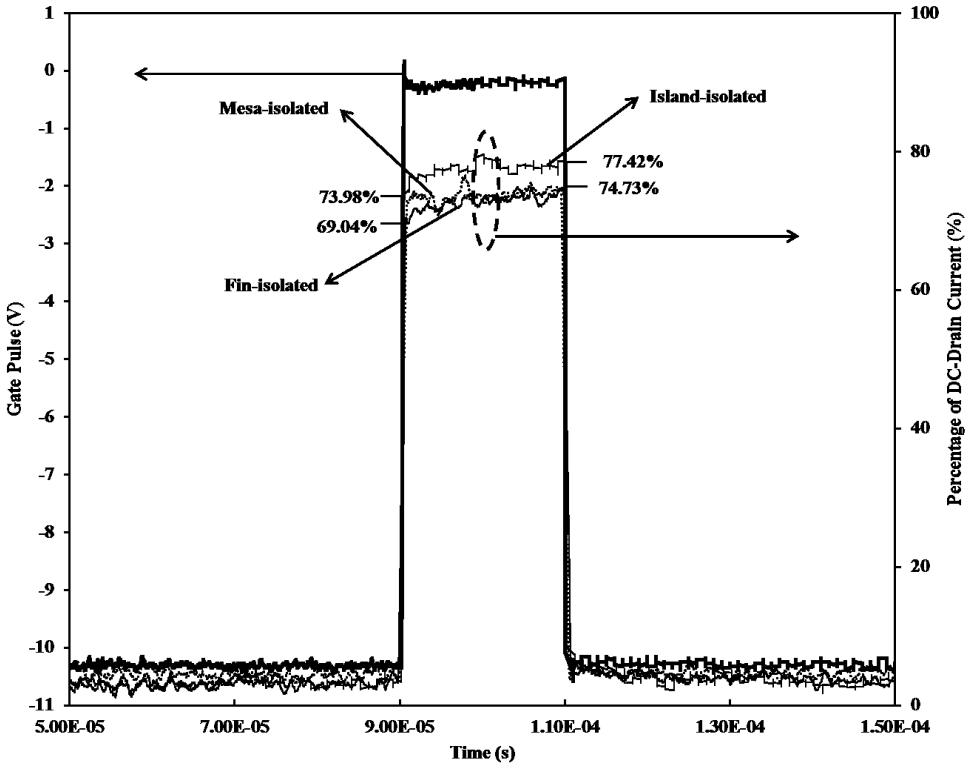
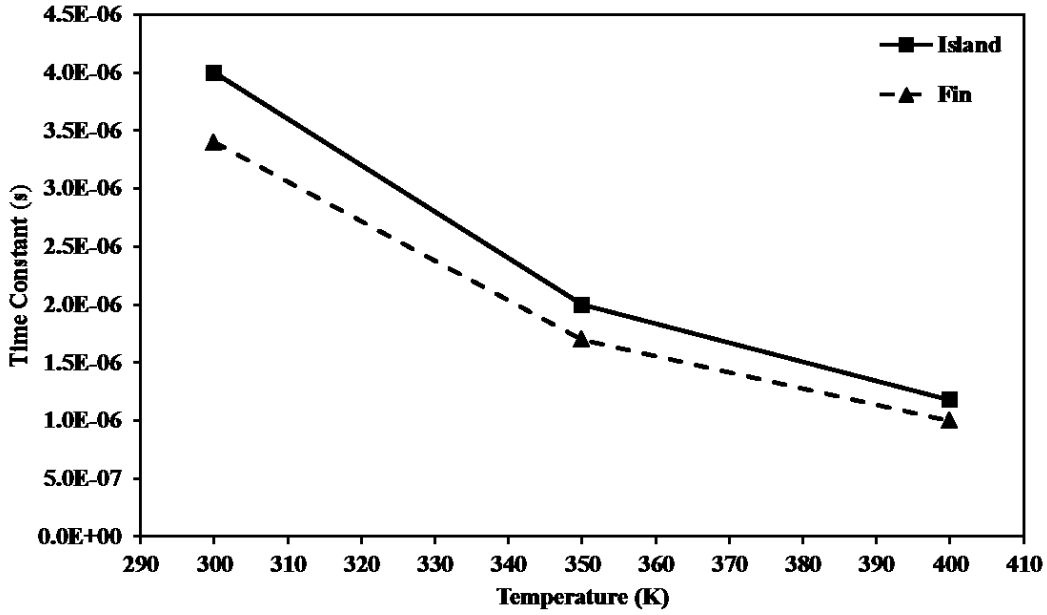


Figure 3.4: Gate voltage pulse versus pulsed drain-current for island-, fin-, and mesa-isolated device at 300 K.

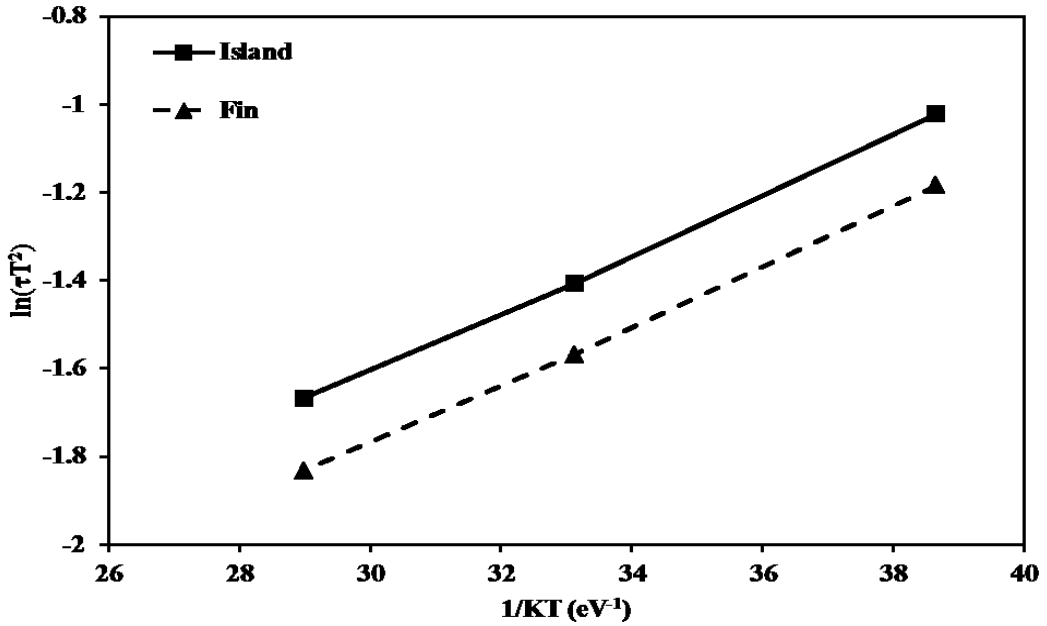
As shown in figure 3.5 (b), the linear variation of $\ln(\tau\, T^2)$ with $1/(KT)$ in island-, and fin-isolated devices clearly indicates an Arrhenius characteristics. According to the modified Arrhenius characteristics of (3.3), using the values of trapping/de-trapping time constants (i.e., τ_1 and τ_2) acquired at two different temperatures (i.e., T_1 and T_2, respectively), the energy level of the responsible trap-site can be calculated as:

$$E_A = \frac{K_B}{\left(\frac{1}{T_2}-\frac{1}{T_1}\right)} \ln\left(\frac{\tau_2/\tau_1}{(T_1/T_2)^2}\right) \tag{3.4}$$

According to (3.4), the trap energy level for island-, and fin-isolated devices are calculated to be equal to 69.7 meV, which is indicative of the existence of a shallow trap level in these device types.



(a)



(b)

Figure 3.5: Calculated time constants (a) according to the gate-lag observed in figure 3.4, and Arrhenius plots (b), at 300, 350, and 400 K for island-isolated device (solid line), and fin-isolated device (dashed line).

The structures of the three device types are presented in figure 3.6. The first step of fabrication was the realization of the isolation features (i.e., island, fin, and mesa) using dry-etching. Inductively-coupled plasma etching (i.e., ICP) was used in fabrication

of the AlGaN/GaN HFETs of this study. Source and drain contacts on these devices were realized using a two-step metallization process. In the first step, the metal layer was deposited on the top surface of the island-, fin-, and mesa-isolation structures. After the first step, rapid thermal annealing was performed for realization of Ohmic contacts to the 2DEG. Connections between the Ohmic contacts and measurement pads were formed in the second metallization step.

Island-isolated devices are composed of an array of fourteen islands. As shown in figure 3.6, implementation of island-isolated devices in this fashion exposes the electrodes to dry-etched sidewalls of islands and also dry-etched GaN surfaces in between the islands. Also in fin-isolated devices shown in this figure, the improved proximity of the dry-etched sidewalls, caused by the reduced width of the fin-isolation in comparison to the mesa-isolation, exposes the channel electrons to a more predominant interaction with the defects created by dry-etching of these sidewalls.

The link between dry-etching of III-nitrides and formation of trap-states has been established in a number of studies [57-60]. Therefore, according to the aforementioned enhanced exposure of 2DEG electrons to dry-etched surfaces in island-, and fin-isolated devices, it is speculated that trap levels introduced by the physical dry-etching is the origin of the observed gate-lag in these device types.

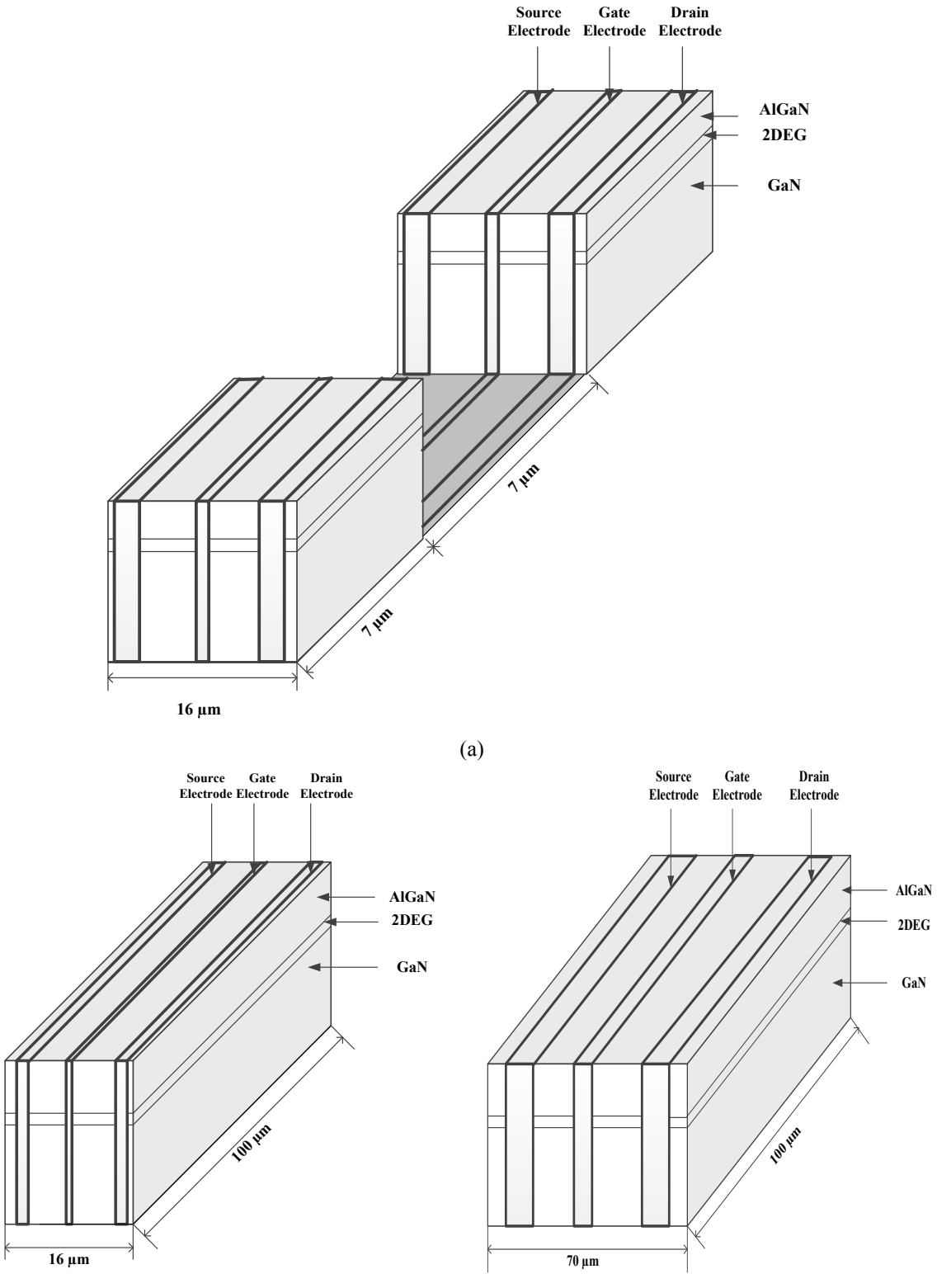
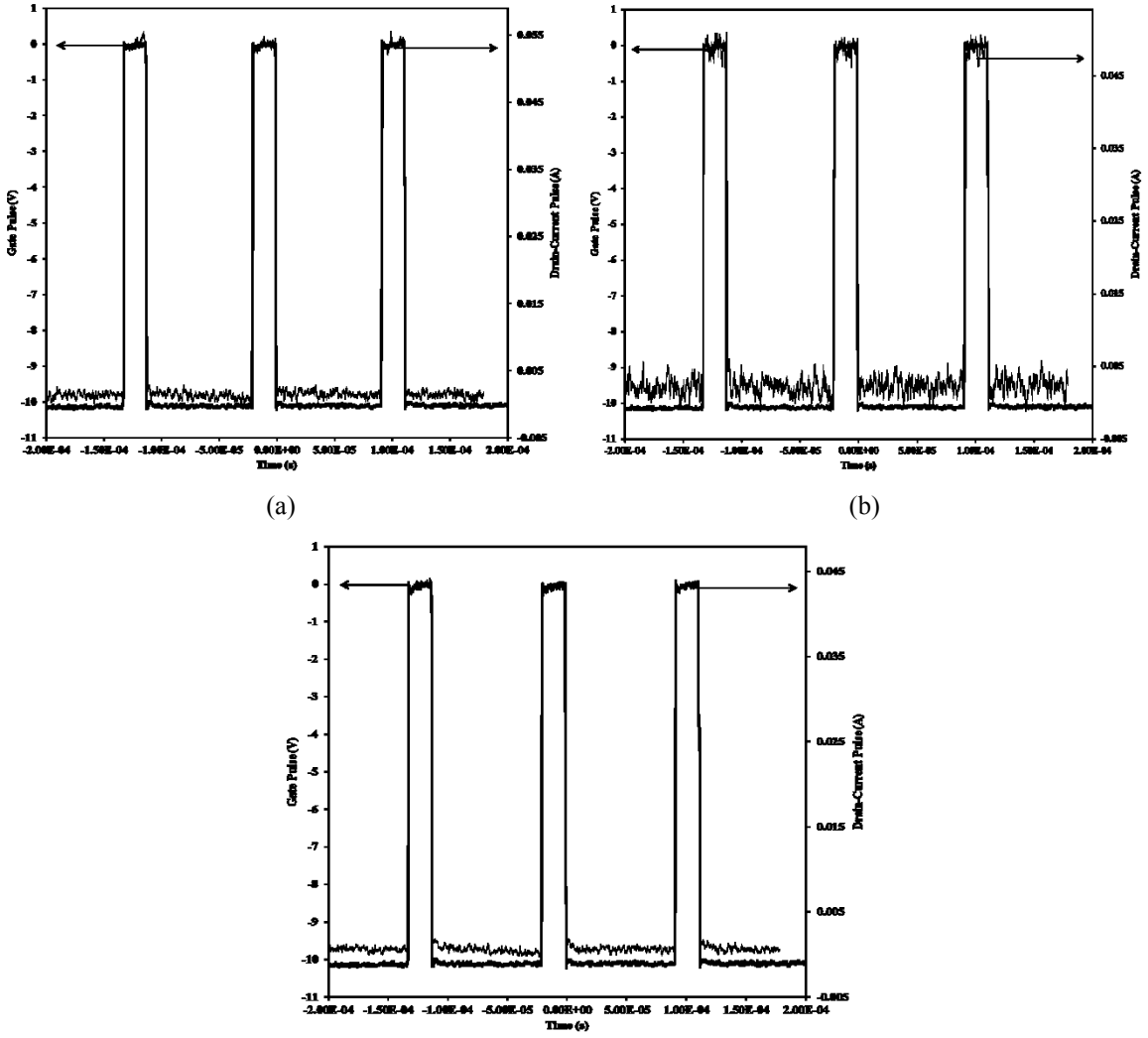


Figure 3.6: Schematics of single-finger island-isolated with two islands, fin-isolated, and mesa-isolated device in (a), (b), and (c), respectively. Source, gate, and drain electrodes overlap proportionally larger dry-etched surfaces in island-isolated device. Figure not in scale.



(a) (b)

(c)

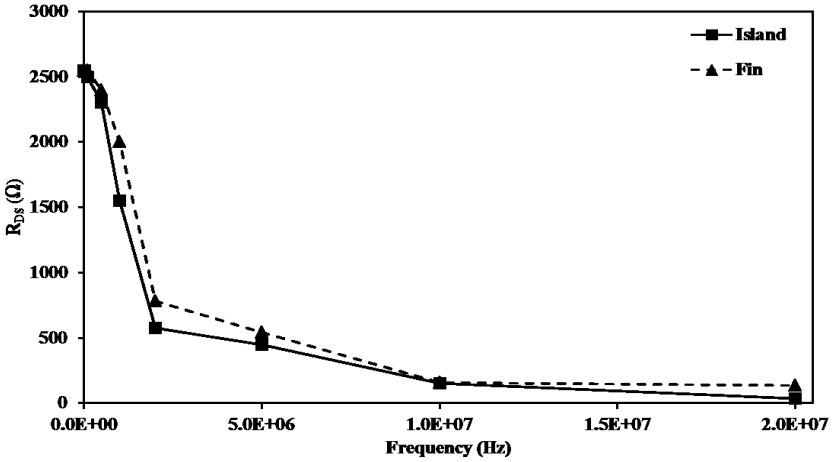
Figure 3.7: Pulsed-mode drain-current measurement, for mesa-isolated devices at 300, 350, and 400 K in (a), (b), and (c), respectively. Darker lines represent the gate-pulse and lighter lines represent the drain-current pulse.

The absence of gate-lag in the pulsed-mode drain-current characteristics of mesa-isolated devices (Figure 3.7) supports the argument that there exists a link between the proximity of the sidewalls to each other and an average position in the channel. Accordingly, while gate-lag was absent in the mesa-isolated devices, in the fin-isolated devices such a behavior was observed.

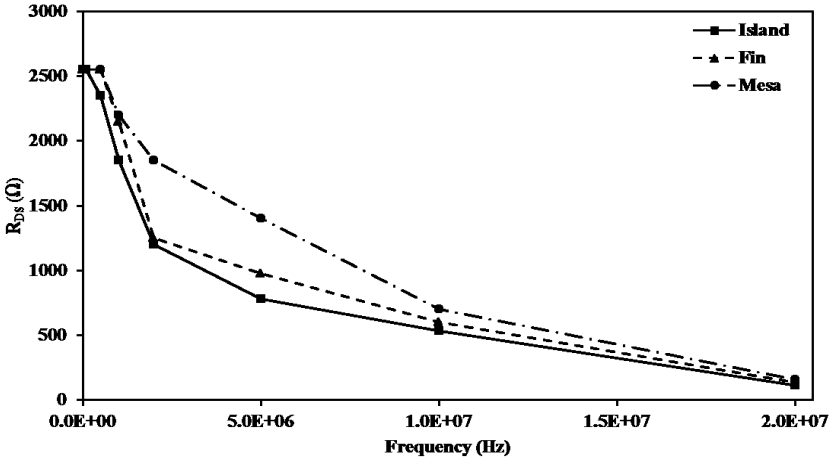
As island-isolated device has larger number of dry-etched sidewalls and surfaces, and proportionally larger interfaces of gate and Ohmic contacts with the etched areas, the trapping/de-trapping time constant in island-isolated device is higher than fin-isolated device for all temperatures (Figure 3.5 (a)). As all three isolation device types were fabricated side by side one another (i.e., on the same epilayer), there can be no link between these observations and pre-existing defects of the epilayer. As a result of these observations, surface passivation before the metallization process is suggested for compensating the trap-centers generated through dry-etching. This is expected to contribute to elimination of the observed gate-lag in the two newly implemented device types (i.e., island-, and fin-isolated).

3.4.2 R_{DS}-dispersion

Figure 3.8 illustrates that at frequencies above 1 MHz, all three device types exhibit R_{DS}-dispersion. It is important to reiterate that usually such an observation is indicative of the presence of very slow deep trap levels. The observed challenge in reaching the value of DC current in pulsed-mode measurements of figure 3.4 and 3.7 is also supportive of this argument. The almost identical presence of R_{DS}-dispersion among these devices of widely varying structures, hint towards a commonality between all devices (i.e., buffer layer).



(a)



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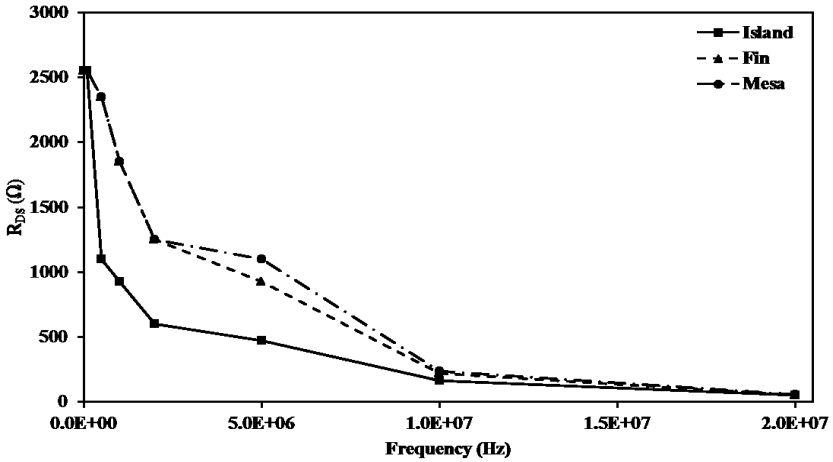

(c)

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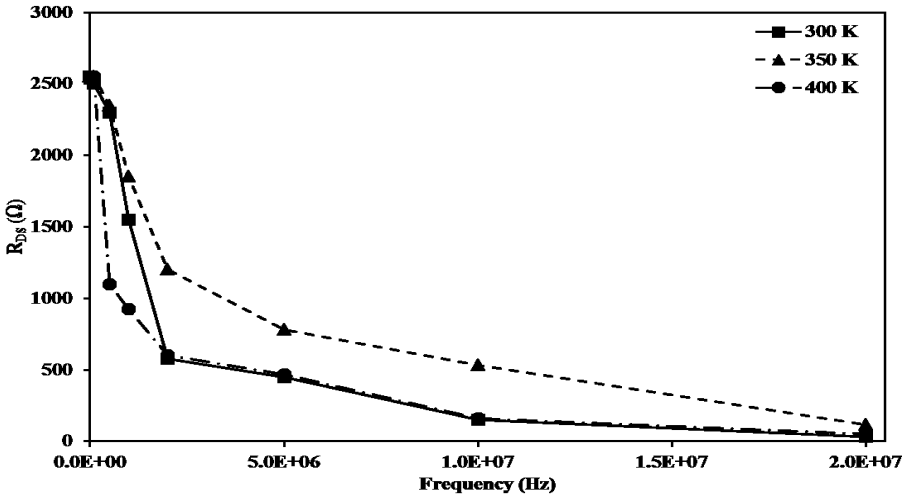

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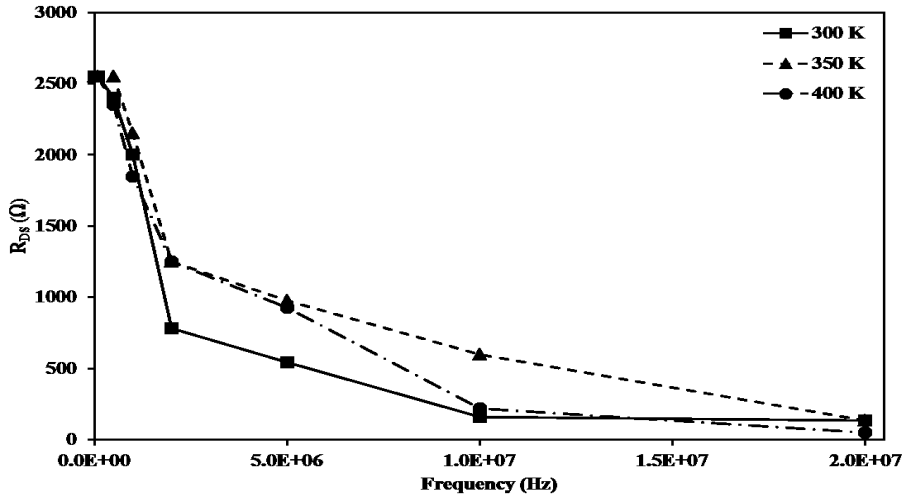

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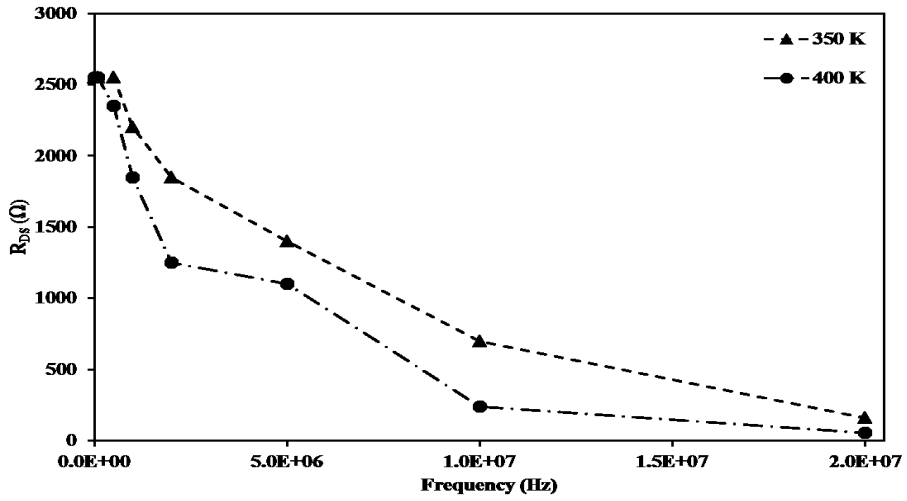

(f)

Figure 3.8: Variation of small-signal output-resistance versus frequency, for island-, fin-, and mesa-isolated devices at 300, 350, and 400 K in (a), (b), and (c), respectively. And at different temperatures for island-, fin-, and mesa-isolated devices in (d), (e), and (f), respectively. Data for mesa-isolated device at 300 K is not present.

All three isolation structures were fabricated on the same epilayer grown on a SiC substrate, following the same process technology. The GaN buffer layer was Carbon-doped [51]. Although incorporation of Carbon-dopants in the GaN buffer layer compensates the unintentionally incorporated donors and reduces leakage through this layer, this introduction of dopants can also create trap-centers. Through the variation of the incorporated Carbon concentration and photoionization spectroscopy, Klein *et al.* have previously reported formation of very deep trap-centers related to Carbon-doping of GaN buffer layer, and have linked that to current collapse in GaN channels [61-62].

Since significant R_{DS}-dispersion is observed in all devices, it is speculated that the observed output-resistance dispersion with frequency might be rooted in the existence of trap-centers formed by the Carbon-doping of the GaN buffer layer. Figure 3.8 demonstrates that island-isolated device shows the highest dispersion among the three device types at all temperatures. In addition to the Carbon-related buffer defects, the existence of dry-etched sidewalls in island-, and fin-isolated devices might be the cause for the observed degradation in their R_{DS}-dispersion characteristics.

By inserting an AlGaN interlayer between the AlN and the GaN layer, Chen *et al*. have demonstrated semi-insulating GaN buffer layer fabricated on SiC substrate. Accordingly, they have reported AlGaN/GaN HFETs with negligible dispersion with the incorporation of the semi-insulating GaN buffer layer [63]. Therefore, the use of AlGaN interlayer between GaN buffer and AlN nucleation layer is suggested to avoid negative outcomes of the Carbon-doping of the buffer. This is expected to improve the high-frequency performance of the studied devices.

3.5 Conclusion

Gate-lag and R_{DS}-dispersion characteristics of newly proposed island-, and fin-isolated and conventional mesa-isolated AlGaN/GaN HFETs were experimentally investigated for three different temperatures. Both island-, and fin-isolated devices exhibited gate-lag with a time constant identified by the Arrhenius characteristics, whereas gate-lag was not observed in mesa-isolated device. Exposure of electrodes to additionally dry-etched sidewalls of the two new device types (i.e., island-, and fin-isolated) are believed to responsible for the observed gate-lag.

R_{DS}-dispersion at high-frequency was observed in all devices. Carbon-related buffer defects are speculated as the causes for the observed R_{DS}-dispersion. Accordingly, deposition of passivation layer before the metallization process is proposed to eliminate the gate-lag, while use of AlGaN interlayer between GaN and AlN layer is proposed to improve the device high-frequency performance.

Chapter 4

Conclusion and Future Work

One of the goals of this thesis was to study the scalability of the current-drive of AlGaN/GaN HFETs with gate-length according to the application of full drift transport characteristics of GaN and also to evaluate the significance of the negative differential mobility region on the scaling-trend. The findings of this work are beneficial in forecasting a more accurate scaling-trend of the drain-current drive of AlGaN/GaN HFETs with gate-length.

In chapter 2, the evaluation of the scalability of the current-drive of AlGaN/GaN HFETs with gate-length was reported by utilizing a realistic steady-state drift transport characteristics and an approximate purely-saturating drift transport characteristics. Results show that the existence of a broad peak along with the negative differential mobility region in the v_d-E characteristics of GaN play a significant role in forecasting the scaling-trend of the current-drive with gate-length. Therefore, it has been observed that the approximate purely-saturating drift transport characteristics overestimates the gain in drain-current of AlGaN/GaN HFETs, with gate-length scaling. The predictability of this scaling-trend through the adoption of the purely-saturating drift transport characteristics is also observed to be worsened with the improvement in the Ohmic

contact technology. Therefore, steady-state drift transport characteristics must be considered in evaluation of the drain-current drive of AlGaN/GaN HFETs with gate-length scaling.

Evaluation of two recently developed island-, and fin-isolated AlGaN/GaN HFETs was the other goal of this thesis. This evaluation was carried out through gate-lag and R_{DS}-dispersion studies at different temperatures and comparison of the same characteristics with that of the conventional mesa-isolated device. Results of these characterizations will be beneficial for further development of these novel fabrication technologies.

In chapter 3, gate-lag and frequency-dispersion of the output-resistance of island-, fin-, and mesa-isolated devices were experimentally studied at three different temperatures. Investigations revealed that presence of additionally dry-etched surfaces, formed in further average proximity with the channel in realization of the two new device types, created difficulties with additionally formed trap-centers. Therefore, gate-lag has been observed in island-, and fin-isolated devices. Accordingly, surface passivation before the metallization process is proposed to eliminate the observed gate-lag. Results also show that defects in the buffer layer, formed by the Carbon-dopants, caused R_{DS}-dispersion at high-frequency in all three device types. Therefore, buffer layer with the incorporation of an AlGaN interlayer is proposed to improve the high-frequency performance of all devices.

The suggested future works in these two areas are following:

- Incorporation of gate-, and substrate-leakage to study the scaling-trend of current-drive with gate-length.

- Incorporation of the energy relaxation time constant and temporal overshoot to determine the average drift-velocity for very small gate-length.
- Fabrication of island-, and fin-isolated devices by considering the proposed design modifications and characterization of those devices.

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