

**Fabrication of Silicon Nanowires and the Effects of Different Parameters on The
Fabrication Results**

Nassim Mashayekh

A Thesis

in

The Department of
Electrical and Computer Engineering

Presented in Partial Fulfillment of Requirements

For the Degree of Master of Applied Science

(Electrical & Computer Engineering) at

Concordia University

Montreal, Quebec, Canada

November 2013

© Nassim Mashayekh

CONCORDIA UNIVERSITY

School of Graduate Studies

This is to certify that the thesis prepared

By: Nassim Mashayekh

Entitled: Fabrication of Silicon Nanowires and the Effects of Different Parameters on The
Fabrication Results

and submitted in partial fulfillment of the requirements for the degree of

Master of Applied Science (Electrical and Computer Engineering)

Complies with the regulations of the University and meets the accepted standards with respect to
originality and quality.

Signed by the final examining committee:

Dr. M. Kabir,	Chair
Dr. J. Dargahi (MIE),	Examiner
Dr. A. J. Al-Khalili,	Examiner
Dr. M. Kahrizi	Supervisor

Approved by _____

Chair of Department or Graduate Program Director

_____ 2013 _____

Dean of Faculty

ABSTRACT

Fabrication of Silicon Nanowires and Effects of Different Parameters on

The Fabrication Results

Nassim Mashayekh

In today's world everything is going toward speed and comfort. This includes different technologies which their improvement leads to an easier life for human beings. One of these technologies is nanotechnology that deals with fabrication and structures of objects in nanometer scale.

Today's technology and science has proved that nanowires are excellent candidates for fabrication of many different devices and their components. These devices take less space while having high performance. Nanowires are one-dimensional structures that have many applications including a variety of sensors, transistors as well as energy-storage devices like solar cells and Li-ion batteries.

Fabrication of nanowires is still under research and many universities and institutes are trying to find methods that are both time- and cost-efficient. This is a challenging subject since there are many parameters involved in the process and each of these parameters affect the final results of fabrication.

The concentration of this work is on fabrication of silicon nanowires. Silicon is the second-most abundant element on the earth and therefore has a more reasonable price compare to other elements.

There are many different techniques to fabricate silicon nanowires but most of these methods are expensive and time consuming.

In this work we have used a top-down method which is time and cost efficient compare to other fabrication methods. There are three main steps in our work; anisotropic etching to texture the surface of the silicon wafer, electrochemical etching to produce the nanowires and a post-etching process in order to clean the surface of the sample. Wafer type, etching duration, temperature, and the applied current are the parameters that are studied during the experiments. The fabricated nanowires are captured and characterized using scanning electron microscopy.

ACKNOWLEDGEMENT

I would like to express my deepest appreciation to my supervisor, Pr. Kahrizi who provided me the possibility to complete this thesis. His continuous contributions, advices, encouragements and supports helped me to accomplish this project.

Furthermore I would like to acknowledge my supervisory committee for their insight reviews, critics and invaluable feedback.

I also express my gratitude to Mr. M. Amouzgar for his kindness, valuable suggestions and assistance during my experiments.

Last but not least, I would like to thank my family. I am thankful to my dear parents, Noushin and Asghar, for having confidence in me and for providing me the opportunity to continue my study. Their supports, kindness and encouragement have always motivated me to take stronger steps in my life. I would also like to thank my beloved sister, Shamim, for being patient and motivating me all these years.

TABLE OF CONTENTS

LIST OF FIGURES	viii
LIST OF TABLES	xi
LIST OF ACRONYMS	xii
LIST OF SYMBOLS	xiv
Chapter 1: Introduction	1
1.1. What is Nanotechnology?	1
1.2. Why Silicon?	1
Chapter 2: Literature Review	3
2.1. Nanowires.....	3
2.1.1. Metallic Nanowires.....	7
2.1.2. Semiconductor Nanowires.....	9
2.2. Silicon Nanowires and Their Applications	10
2.2.1. Lithium-ion Batteries.....	11
2.2.2. Silicon Nanowire Sensors.....	13
2.1. Porous Silicon	15
2.4. Motivation and problem statement.....	18
2.5. Organization of the Thesis	18
Chapter 3: Experimental and characterization facilities	19
3.1. Fabrication Experimental Steps	19
3.1.1 Sample Preparation	19
3.1.2. Anisotropic Etching	20
3.1.3. Metallization and Annealing.....	21
3.1.4. Electrochemical Etching.....	23
3.2. Characterization Equipment.....	26
3.2.1. Scanning Electron Microscope	26
3.2.2. Energy-dispersive X-ray Spectroscopy.....	28
Chapter 4: Experimental and fabrication results.....	31

4.1. Anisotropic Etching Results	31
4.2. Electrochemical Etching results.....	34
4.3. EDX Measurements; Chemical Compositions	41
Chapter 5: Discussion, Conclusion and future work	44
5.1 Discussion	44
5.2. Conclusion and future work.....	45
References.....	48

LIST OF FIGURES

Figure 1.1. Silicon electron configuration [2]

Figure 2.1. Top-down etching method

Figure 2.2. Schematic view of the CVD method [10]

Figure 2.3. a) Vapor Liquid Solid growth method of ZnO nanowires on copper substrate. b) and c) SEM images of nanowires generated on a copper grid [14]

Figure 2.4. Left: SEM images of longer pentagonal faceted silver nanorods with the aspect ratios of (a) 8.7 and (b) 10.2; as well as (c) and (d) longer $2 \mu\text{m}$ pentagonal faceted silver rods regrown from ca. $0.5 \mu\text{m}$ rods. The scale bar is 100 nm for (a) and (b) and $2 \mu\text{m}$ for (c) and (d). Right: Optical properties of synthesized pentagonal faceted silver nanorods. (e) Photographs of aqueous dispersions and (f) UV-vis spectra of pentagonal faceted silver nanorods with thickness of $49.5 \pm 2.5 \text{ nm}$ and length of (1) $62 \pm 3 \text{ nm}$; (2) $75.3 \pm \text{ nm}$; (3) $108 \pm 5 \text{ nm}$; (4) $142.7 \pm \text{ nm}$; (5) $158 \pm 8 \text{ nm}$. [15]

Figure 2.5. Silicon deposition types illustration [33]

Figure 2.6. Response of the sensor to ammonia and incense smoke exposure [4]

Figure 2.7. SEM image of porous silicon [48]

Figure 2.8. SEM image of different pore types: a) and b): branched or tree structure; c) sponge; d) closed; e) pyramidal; f, g, and h) filament or cylindrical pores [49]

Figure 3.1. Schematic view of the oil bath and the etching process. During the process, a cold water flow is available on top of the beaker in order to avoid any change in the solution concentration

Figure 3.2. SEM image of pyramids on the surface of the sample after TMAH wet-etching

Figure 3.3. Metallization machine

Figure 3.4. Annealing machine used during experiments

Figure 3.5. Teflon anodization cell used during electro-chemical etching

Figure 3.6. Schematic view of a scanning electron microscope [51]

Figure 3.7. Hitachi SEM model S-4700

Figure 3.8. Schematic view of a typical EDX [52]

Figure 4.1. Images obtained from the optical microscope. A) High concentration of pyramids; B) Medium concentration of pyramids and C) Low concentration of pyramids

Figure 4.2. SEM images from three different samples with various pyramid concentrations: A) High concentration of pyramids; B) Medium concentration of pyramids and C) Low concentration of pyramids

Figure 4.3. SEM images. A) n-type Si wafer, resistivity of 10-20 Ω cm; B) p-type Si wafer, resistivity of 10-20 Ω cm. Both of these wafers had a high density of pyramids before electrochemical etching. The electrochemical etching conditions are: 30 minutes, HF:Ethanol (1:3), 65mA applied currents

Figure 4.4. SEM image of silicon nanowires. A) No NaOH, top view; B) 30seconds NaOH immersion, top view; C) No NaOH, side view; D) 30 seconds NaOH immersion, side view

Figure 4.5. SEM image of some of the fabricated Si nanowires

Figure 4.6. Porous silicons fabricated during the experiments

Figure 4.7. EDX chemical characterization of the fabricated nanowires

Figure 4.8. Elemental mapping of fabricated Si nanowire

LIST OF TABLES

Table 2.1. Comparison of the capacity of different elements [33]

Table 4.1. The summary of various conditions experiments during the wet-etching step

Table 4.2. Some of the applied conditions during the electro-chemical etching experiments

LIST OF ACRONYMS

AgNO ₃	Silver Nitrate
CdS	Cadmium Sulphide
CVD	Chemical Vapor Deposition
DI Water	De-Ionized Water
EBL	Electron Beam Lithography
EFM	Electrical Force Microscopy
HF	<i>Hydrofluoric acid</i>
KOH	Potassium Hydroxide
LED	Light Emitting Diode
MBE	Molecular Beam Expitaxy
MEMS	Micro-Electro-Mechanical System
NW	Nano-wires
PPS	Pyramidal Porous Silicon
PECVD	Plasma Enhanced Chemical Vapor Deposition
PS	Porous Silicon
RF	Radio Frequency
SSPM	Scanning Surface Potential Microscopy
SEM	Scanning Electron Microscope
Si	Amorphous Silicon
TiO ₂	Titanium Dioxide
TMAH	Tetra-Methyl Ammonium Hydroxide
VLS	Vapor Liquid Solid

VS	Vapor Solid
VSS	Vapor Solid Solid
XRD	X-Ray Diffraction
ZnO	Zinc Oxide
ZnONW	Zinc Oxide Nanowire
2-D	2 Dimensions
3-D	3 Dimensions

LIST OF SYMBOLS

A	Area of the deposition	[cm ²]
D	Density of bulk silicon	[gr.cm ⁻³]
d_{gap}	Electrode distance	[μm]
e	Charge per electron	1.602x10 ⁻¹⁹ [C]
E	Effective electric field	[Vcm ⁻¹]
F	Faraday constant	96485[C.mol ⁻¹]
J	Current density	[A.cm ⁻²]
J_{ep}	Electropolishing current density	[A.cm ⁻²]
n	Number of exchanged charge	-
Na	Avogadro's number	6.02x10 ²³ [mol ⁻¹]
P	Gas pressure	[torr]
$P\%$	Porosity	-
Q	Total charge	[C]
S	Electrochemical etched area	[cm ²]
T	Thickness of the deposited metal	[μm]
t_{dep}	Deposition time	[hr]
V_b	Breakdown voltage	[V]

W	Weight of the deposited metal	[gr]
W_p	Pore thickness	[μm]
γ_l	Liquid surface tension	[dyn.cm ⁻¹]
Δp	Pressure drop	[kPa]
λ	Number of exchanged charge	-
$\lambda_{incident}$	Incident photon wavelength	[μm]
$\lambda_{scattered}$	Scattered photon wavelength	[μm]
ρ_v	Metal density	[gr.cm ⁻³]

Chapter 1: Introduction

1.1. What is Nanotechnology?

As Jack Uldrich and Deb Newberry said, “The next big thing is really small”. [1]

By reducing the size of materials to nano scale, their properties change. This includes their physical, chemical and mechanical properties. Nanotechnology is the technology that deals with fabrication and structures of nanometer dimensional objects in the length scale of approximately 1 -100 nanometer. Research and development at the atomic, molecular or macromolecular level is the objective of this technology. Sciences related to the systems structured by nanotechnology are known as Nanoscience.

Nanotechnology is not a future technology anymore and has already been used in some industries and technologies. Chemistry, physics, biology, material science, and different engineering fields are some fields that are attracted to nanoscience and nanotechnology.

Progresses of this technology plays an important role for those who believe in the golden rules; smaller size, faster speed, larger functionality, less cost, and less heat.

1.2. Why Silicon?

In this work silicon (Si) is chosen as the main material of fabrication and the fabricated nanowires are made from pure Si. Si is the second-most abundant element in our world and builds more than 27% of the chemicals on the Earth.

In the nature silicon which is a semiconductor can be found in form of dioxide (SiO_2) and carbide mostly in sand and can be used in the electronics industry. [2]

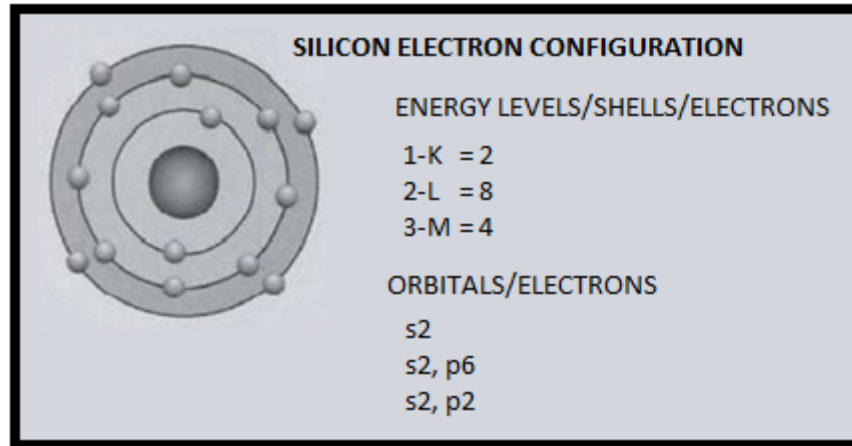


Figure 1.1. Silicon electron configuration [2]

Some properties of this material are its chemical stability, being an indirect semiconductor, the small mobility of electrons/holes, and small electronic band gaps. Also it can grow easily in high temperatures in the form of crystal structures (used in most micro/optoelectronic devices). [3]

Considering the above explanations, scientists have been searching the benefits and consumption of Si in other forms like porous silicon (PS) and silicon nanowires.

Chapter 2: Literature Review

2.1. Nanowires

Nanowires, also known as quantum wires, are structures that are extremely thin, and their diameters can be as little as only a few nanometers or less. These tiny structures can be made of different materials, including metals, insulators and semiconductors. Nanowires are considered as one- dimensional (1-D) nanostructures with diameters in the range of 1-100nanometers. This new technology will bring many new opportunities to the future of the world of devices and their components.

There are many different methods for the fabrication of different nanowires. It is important to choose the best method that result in nanowires with those characteristics we are looking for.

The production of nanostructures including nanowires can be divided into two methods. One is the top-down method and the other is the bottom-up. In the top-down method, bulk material will be used, and the desired nanostructure will be obtained using lithographic techniques.

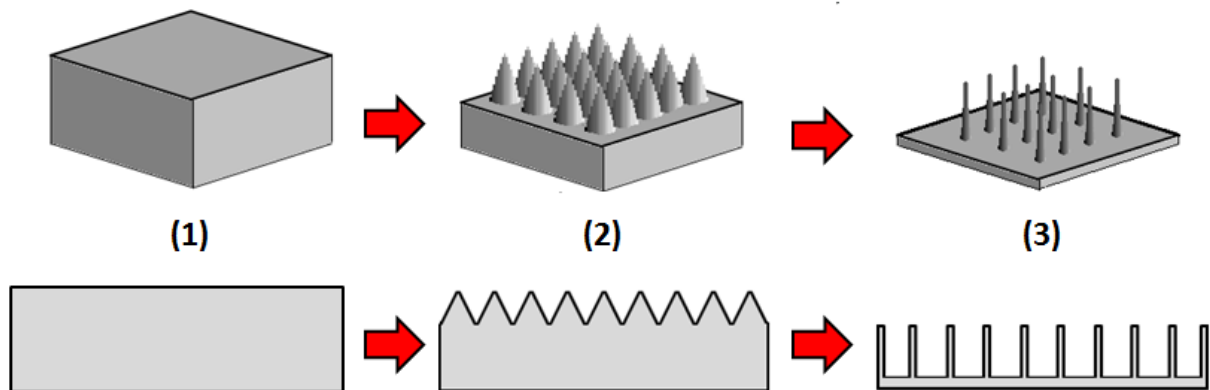


Figure 2.1. Top-down etching method

Figure 2.1 illustrate both two-dimensional and three-dimensional schematic view of the top down process used in this work to fabricate silicon nanowires. As it can be seen, the fabrication process starts with bulk material and by passing through two etching processes we obtain the nanowires.

The main purpose of this method, which has been used for many years, is to fabricate nano scale structures from the bulk materials. However, using bulk materials to reach the nano size structure might result in lots of waste and difficulty of structure and uniformity control. [4, 5]

In the bottom-up method, the atoms will be self-assembled and at the end they will form a larger but still nanosize structure. This is a controllable method that results in a uniform structure. The structures will be formed from a controllable crystallization of material available in a liquid or vapor. Although there will be less wasted material, the fabrication cost is higher than top-down method. [4, 6]

In general, the growth process of nanowires, especially silicon nanowires, have two parts: The growth technique and the growth mechanism. The growth technique is related to the material transportation or production in the defined area. The Chemical Vapor Deposition (CVD), the Molecular Beam Epitaxy (MBE), and Plasma Enhanced CVD (PECVD) are three growth techniques. As growth mechanisms, Vapor Liquid Solid (VLS) and Vapor Solid Solid (VSS) can be mentioned. [7] In this chapter the CVD technique and VLS mechanism will be explained.

The CVD technique is usually used in fabrication of high purity or solid materials, as well as in the production of micro-size devices made from carbon fiber, such as silicon, tungsten, and filaments [8].

There are different types of CVD techniques, such as atmospheric pressure CVD, ultrahigh vacuum CVD, and low pressure CVD, and each of them are suitable for different aims and materials. Each of these techniques can be preferable depending on the experiment condition and specifications we are looking for. Figure 2.3 is an example of CVD technique in fabrication of carbon nanotubes [9].

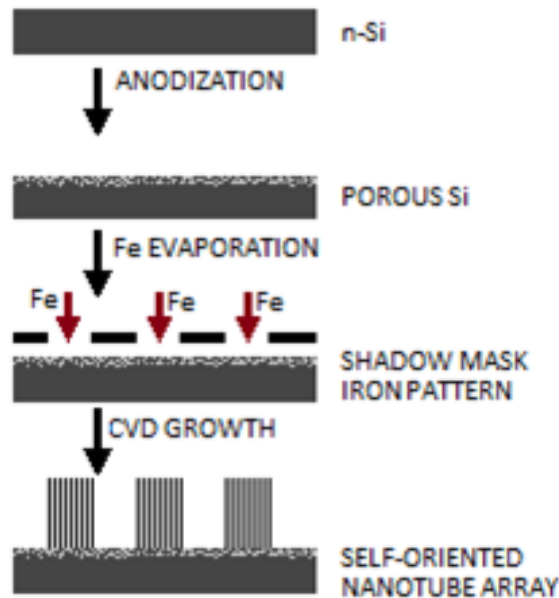


Figure 2.2. Schematic view of the CVD method [10]

VLS is a mechanism to fabricate one-dimensional structures including nanowire. A catalyst is required for this method and the suitable catalyst for nanowires fabrication is liquid metal. The process starts simply when the saturation begins by turning on the source, and it ends when the source is disconnected [11-13]. In this method the growth area and size of the wires are controllable. However, the catalyst should have some required conditions for the best results. As an example, the catalyst should consist of crystalline material and it should not react to the

reaction products while the growth is in process [12, 13]. Figure 2.3 illustrates the ZnO nanowire growth using the VLS mechanism.

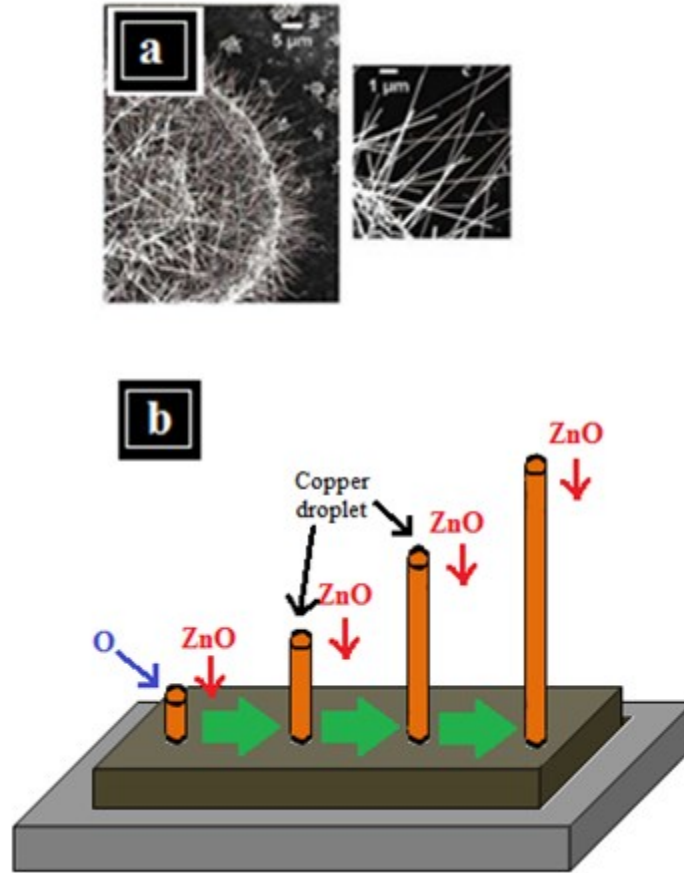


Figure 2.3. a) Vapor Liquid Solid growth method of ZnO nanowires on copper substrate. b) and c) SEM images of nanowires generated on a copper grid [14]

The method used in this project in order to fabricate silicon nanowires is known as anodization. This method includes electrochemical etching of a silicon wafer in the presence of a current source, an electrode, and the etching solution. The fabrication steps are explained with more detail in the next chapters.

Nanowires are divided into different types including metallic nanowires, non-metallic nanowires, and semiconductor nanowires. In this chapter metallic and semiconductor nanowires are explained.

2.1.1. Metallic Nanowires

Metallic nanowires have unique mechanical, catalytic, and electronic properties. One method to fabricate metal nanowires is seed-mediated approach developed by Murphy's group on 2001. [15] On 2003, scientists from Zurich Laboratory fabricated metal nanowires using a micro contract printing method. As per their results, this method is applicable for gold, silver, copper, and palladium nanowires. [16] Another method developed by Xia et al. [15] is the wispily synthesis method which has resulted in uniformity of shape and size of the gold nanowires.

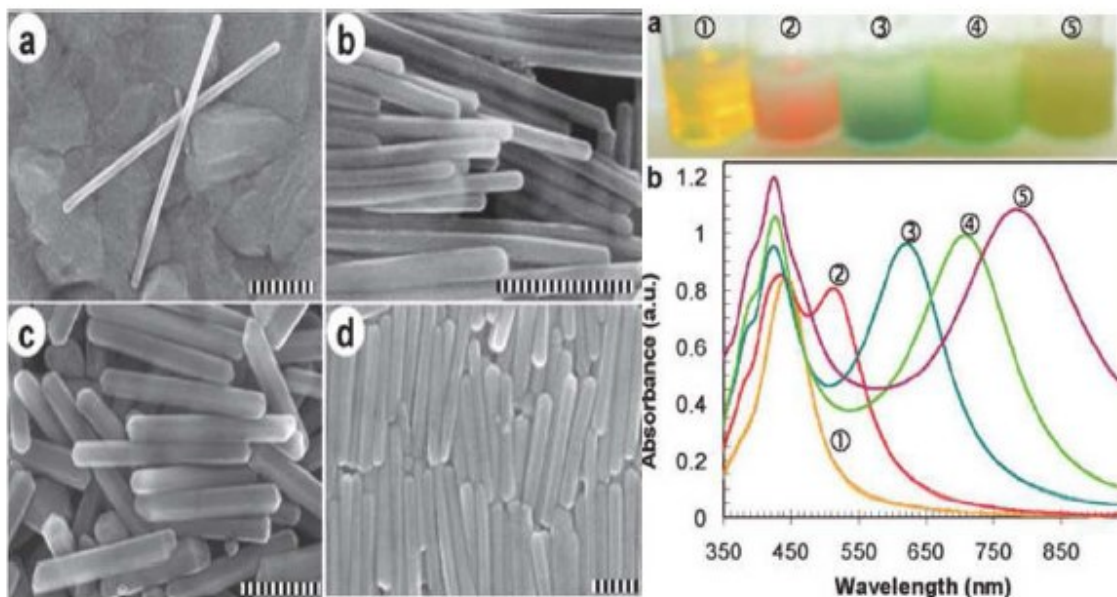


Figure 2.4. Left: SEM images of longer pentagonal faceted silver nanorods with the aspect ratios of (a) 8.7 and (b) 10.2; as well as (c) and (d) longer 2 μ m pentagonal faceted silver rods regrown from ca. 0.5 μ m rods. The scale bar is 100 nm for (a) and (b) and 2 μ m for (c) and

(d). Right: Optical properties of synthesized pentagonal faceted silver nanorods. (e) Photographs of aqueous dispersions and (f) UV-vis spectra of pentagonal faceted silver nanorods with thickness of 49.5 ± 2.5 nm and length of (1) 62 ± 3 nm; (2) $75.3 \pm$ nm; (3) 108 ± 5 nm; (4) $142.7 \pm$ nm; (5) 158 ± 8 nm. From Ref (Pietrobon et al 2009) [15]

In general there are few basic techniques in order to develop metal nanowires. However there is always a possibility of a new method of development by making any changes to these basic techniques. Each technique will cause specific properties and characteristics. Therefore different methods are suitable for different tasks and targets. Lithographic techniques, templating, and chemistry and self-assembly methods are at the base of most of metal nanowire fabrication techniques [17].

The application of metal nanowires application is a wide topic. One application for the metal nanowires is the perpendicular magnetic data storage media. The one-dimensional structure of metal nanowires facilitates the magnetization to saturation by longitudinal field [18]. Another example from metal nanowires applications is high resolution scanning probe microscopy tips. As we know the resolution and accuracy of these kinds of microscopes depends on the sharpness and geometry of their tips. The metal nanowires are used as the metal tip in microscopes such as electrical force microscopy (EFM) and scanning surface potential microscopy (SSPM) [19].

Some other applications of metal nanowires are biological tags, meta-materials, field emission electron emitters, and gas sensors. [18- 20]

2.1.2. Semiconductor Nanowires

The functionality and performance of micro and nano-size device can be increased by using semiconductors in their fabrications. Among all existed materials, semiconductors are the most searched nanostructures. This includes controllable conductivity, doping, and morphology over large areas. Chemical vapor deposition and Molecular Beam Epitaxy are two out of the many methods for fabrication of semiconductor nanowires [21]. As an example of semiconductor nanowires silicon nanowires, indium phosphide nanowires, and gallium nitride nanowires can be mentioned. In the next section Si nanowires and its applications will be discussed.

2.2. Silicon Nanowires and Their Applications

As mentioned before, Silicon nanowires (Si NW) like other nanowires are one-dimensional structures in the scales of nano. They have attracted the attention of many researchers due to their specific characteristic including their strong broadband optical absorption as well as their high compatible structures among all semiconductors. [4, 22]

On 2003 the Electrical Engineering and Computer Sciences and the Chemistry departments of the University of California at Berkeley used the photolithography-based method in order to fabricate a sub-10-nm silicon nanowires arrays. [23]

On 2004 G. Zheng et al. studied fabrication of n-type silicon nanowires. In their work they synthesized a single crystal n-type silicon nanowire that had controlled phosphorus dopant concentrations. Their result was later used in the fabrication of field effect transistor (FET) devices. [24] Later on in 2006, F. Patolsky et al. used silicon nanowires to make an ultra-sensitive, label-free sensor for real-time detection of biological and chemical species including proteins, small molecules, viruses and nucleic acids. [25]

In 2007, Z. Huang et al. published a paper about controlled fabrication of silicon nanowire arrays. During their experiments they developed a template catalytic etching process in order to have a large area of silicon nanowire arrays with controlled density and diameter. [26]

In 2009, researchers demonstrated a novel method using molecular beam epitaxy technique in order to fabricate silicon nanowire p-n junctions. [27]

Later on another group of researcher used one-step etching method in order to fabricate n-type mesoporous silicon nanowires. [28] In this work, they explained the possibility of n-type

mesoporous silicon nanowires production using one-step metal-assisted chemical etching in HF and AgNO₃ method.

In 2012, a group of scientists from National Sun Yat-sen University of Taiwan performed an experiment to produce p-type silicon nanowires that were suitable for biosensor applications. They used a silver assisted chemical etching method. Study of their method proves that this is a very time consuming method since their etching time was 3 hours. [29]

There are various applications for silicon nanowires such as solar cells, memories, Li-ion batteries, and in biological and chemical sensors. [30, 31] in the next two sections two of these applications are discussed.

2.2.1. Lithium-ion Batteries

Silicon nanowires are a candidate for the improvement of battery technologies. As said by Amprius, a lithium-ion battery development company, they developed a battery in 2010 that is made from nanostructure silicon and is capable of storing twice the energy compared to the regular batteries available in the market.

Table 2.1 shows a comparison between the capacities of different elements that can be used in battery fabrication. [32, 33]

According to Amprius, vertical arrays of silicon nanowires are used to fabricate this battery. These nanowires, which are flexible and tapered, are used to play the anode role in the battery. [33]

Elements	Capacity (mAh/g)
Carbon	370
Antimony	660
Aluminum	990
Tin	994
Germanium	1600
Silicon	4200

Table 2.1. Comparison of the capacity of different elements [33]

Figure 2.6 illustrates the results of cycling on the anode part of the battery.

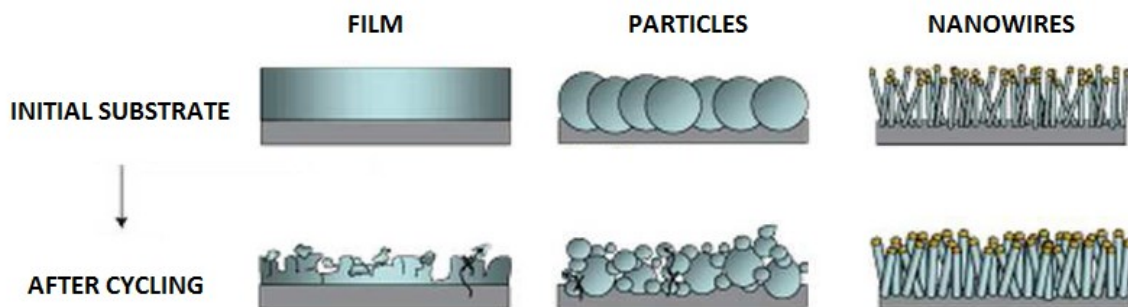


Figure 2.5. Silicon deposition types illustration [33]

2.2.2. Silicon Nanowire Sensors

As the name indicates, gas sensors are devices which are used to detect the presence of gas, especially toxic and combustible gases. The main concentration in gas sensor researches is to manufacture smaller, lighter, and more accurate devices with longer life time and performance. Different types of gas sensor have different life time. There are four major types of gas sensor known as “Electrochemical,” “Semiconductor,” “Catalytic,” and “Infrared (IR).” [34]

Electrochemical gas sensors have two, three, or maximum four electrodes, and measure the gas concentration by gas oxidization or by verifying the current resulting from gas reduction at the electrode. [35, 36]

The semiconductor gas detectors operate by chemical reactions upon presence of gas. The most common material is Tin dioxide. [37]

The catalytic and infrared sensors gas sensors are mostly used to detect the combustible gases and oxygen level. This device was invented in the mid-1960s. [34, 38]

The traditional infrared gas sensors are complicated, expensive, and heavy devices, however they do not need to be placed directly in contact with the gas. The new developed versions of IR sensors are simpler and more reliable compared to the old ones. [39]

Studies show that high surface-to-volume ratio in one-dimensional nanostructures such as carbon nanotubes and metal oxide nanowires make them suitable for catalytic gas sensor applications. Although these devices are dominant because of their sensitivity, they have selectivity and reversibility weaknesses due to the similar changes in device when the gas is present. [40]

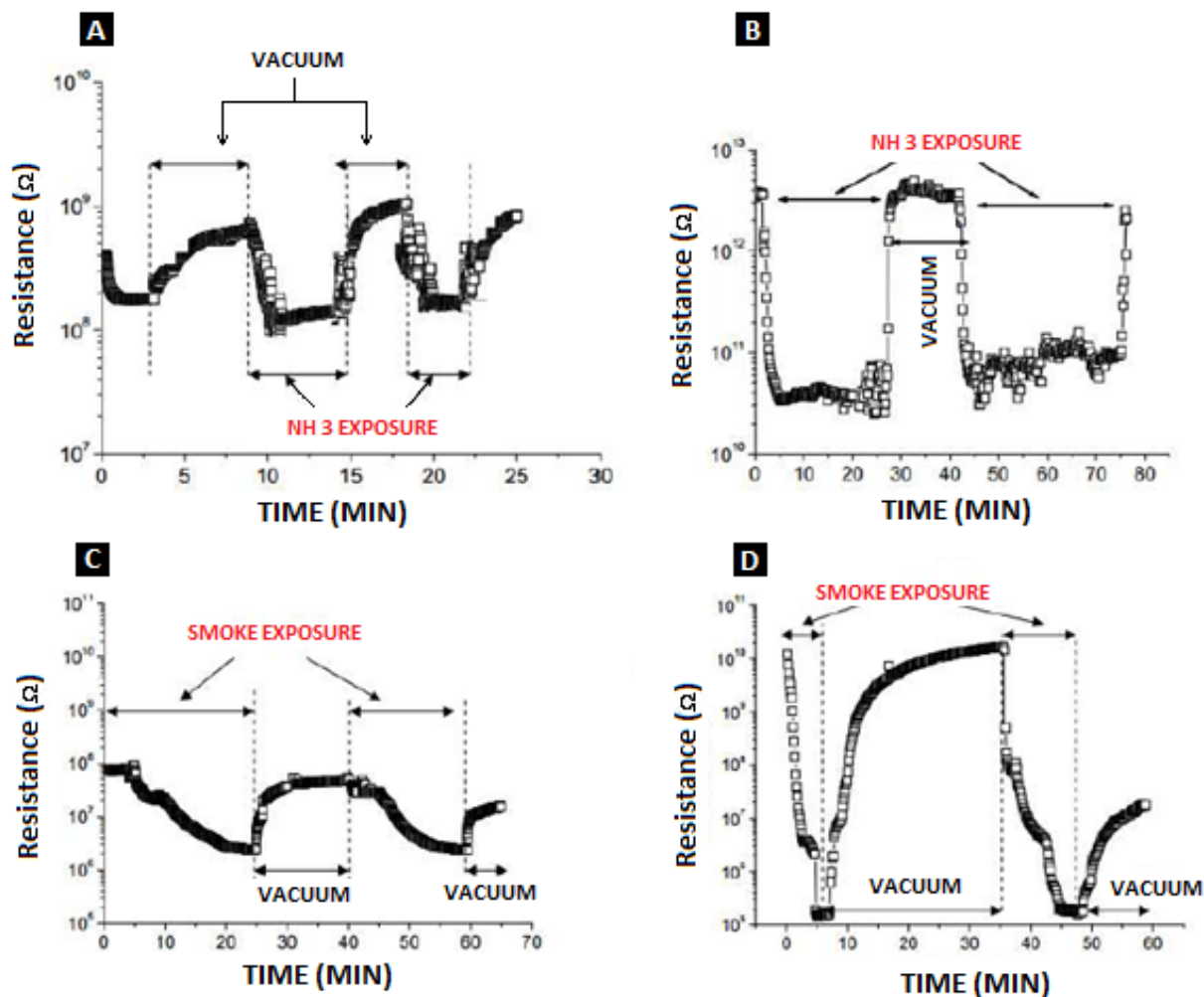


Figure 2.6. Response of the sensor to ammonia and incense smoke exposure [42]

The first chemical and biological application of silicon nanowires in gas sensors was discovered in 2001 by Leiber's group. [41, 42] One kind of these gas sensors are silicon nanowire-based resistors. These sensors have a low manufacturing cost. As shown in figure 2.7, in the presence of ammonia or smoke the resistivity of the silicon nanowires decreases while in a vacuum situation it increases. In this situation, the atoms of the ammonia and smoke acts as a donor of electrons, also known as reducing agents. [42]

2.1. Porous Silicon

Porous silicon (PS) is a form of silicon crystal that has a network of nano voids or nanoporous holes on its surface. The word “porous” in this context refer to billions of nano-holes in a single silicon crystal substrate. The structure size of the pores on the silicon substrate varies between 1-100nm. [3, 43]

PS was accidentally discovered in 1956 by Arthur Uhlir and Ingeborg Uhlir while they were performing the Si electro-polishing process. The experiments showed that during the process when the applied current is above certain value, Si rather than get polished will be etched and produced a structure called PS. [44]

During the 1980s and 1990s, PS attracted more attention due to its excellent properties such as light emission and large surface-area-to-volume ratio. Leigh Canham, who was working in England’s Defence Research Agency, discovered that PS might display quantum confinement effects. Later, he published his red luminescence experiment results from PS, which illustrates that if a Si wafer is subjected to electrochemical and chemical dissolution, light emission can be obtained. [45, 46]

Knowing that PS can behave as a visible light emitter has led to the idea of creating Si-based optoelectronic devices, such as LEDs, optical memories, lasers, switches, and displays. On the other hand, unlike bulk Si, PS is biocompatible and is suitable for biomedical applications in both vivo (external) and vitro (internal) experiments. As the example of the biomedical applications the biological sensing devices, electronic sensing devices such as hearing, viewing, checking body chemistry in order to monitor pain, disease, or drug dosage, as well as the replacement of damaged tissue in the ear, eye and skin can be mentioned. [46- 48]

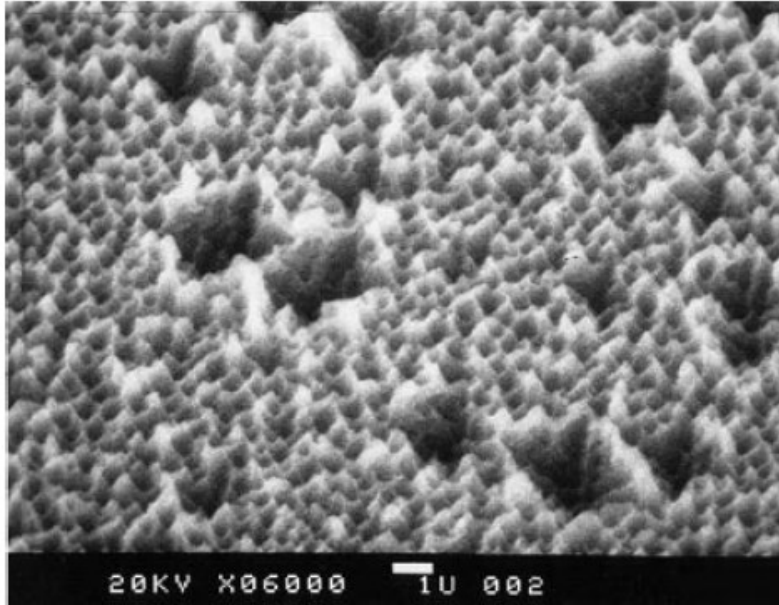


Figure 2.7. SEM image of porous silicon [49]

PS fabrication is a simple and easy process. However, the fact that PS is a disordered material causes difficulty in having a controlled structure. The main concern of researchers in PS production is having the maximum possible control on their thickness, porosity, as well as the reproducibility. [46] There are different techniques to produce PS, such as stain-etching methods or anodization.

In this work, solution of HF acid and ethanol is used to create porosity on the silicon surface. This process will be explained in details in the next chapters.

According to pore sizes, PS is divided into three groups. If the pore size exceeds 50nm, it will be microporous. PS with a pore size between 5nm and 50nm are mesoporous, and those with pores smaller than 5nm are nanoporous.

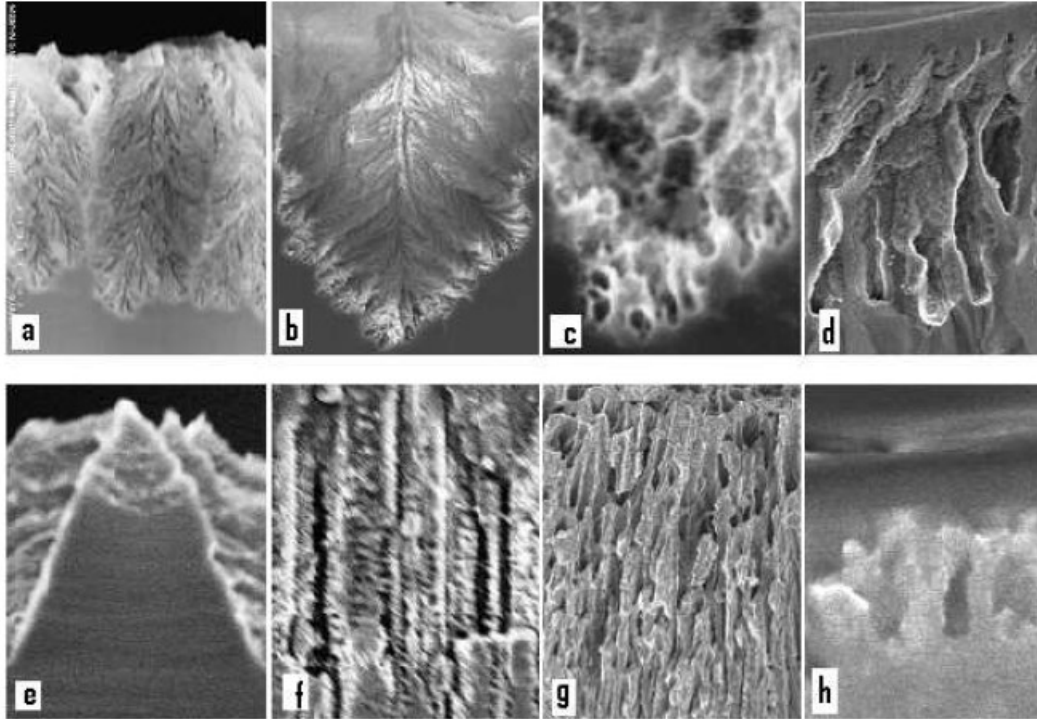


Figure 2.8. SEM image of different pore types: a) and b): branched or tree structure; c) sponge; d) closed; e) pyramidal; f, g, and h) filament or cylindrical pores [50]

The porosity of materials can be determined by measuring their weight in different steps of the experiment, and is defined as the ratio of the volume of pores over the total or bulk volume. Knowing the porosity will help us to calculate the thickness of the porous layer. [50]

Toxicity of a material is an important and serious topic that needs to be discussed depending on the type of experiments. Although different sources report that PS can be used in most biological applications since it does not have fatal toxic property, scientists are still quantifying the results in order to confirm the nontoxicity property of PS. [46]

In our study, we have used PS as a part of the process in order to fabricate nanowires.

2.4. Motivation and problem statement

Applications of silicon nanowires are still an understudy subject. The most importantly we are looking to find suitable methods to fabricate these nanowires. There are still lots of weaknesses in production of silicon nanowires in case of time and cost efficiency. Most of the techniques are described above are either very expensive and/or very time consuming, (in most cases we need to use photolithography step, masking). In this work we are introducing a new method of fabrication using simple silicon etching/electrochemical etching techniques.

The whole process includes three fundamental steps: Anisotropic etching, electrochemical etching and the final step which is cleaning the surface of the sample.

In this thesis, we have fabricated silicon nanowires and porous silicon while using the methods that are more time and cost-efficient.

2.5. Organization of the Thesis

The third chapter of this thesis concentrates on experimental and characterization facilities that are used during this work as well as the detail of our fabrication method and the processes.

In the fourth chapter, the results of the fabrication process are explained in detail and finally chapter five includes the results discussion, the conclusion of the work as well as the possible future works.

Chapter 3: Experimental and characterization facilities

There are different steps performed in order to obtain the preferable results.

3.1. Fabrication Experimental Steps

3.1.1 Sample Preparation

The first step in order to start the fabrication process is to prepare the samples. Although this stage is basic, it is very important and affects the whole experiment and the obtained results.

After the silicon wafers were cut into small pieces, the cleaning process should be performed. The process that is chosen for this work is the RCA method. RCA stands for Radio Corporation of America, and the process was developed by W. Kern in 1965. The RCA method includes three steps. The first step is the removal of organic contaminants, then the oxide layer is removed, and finally the ionic contaminants are removed. During all these steps DI water should be available in order to rinse the sample. [51]

In order to perform organic contaminants removal, the wafers were placed in an 80°C solution that contains of $\text{NH}_4\text{OH}+\text{H}_2\text{O}_2+\text{H}_2\text{O}$ (1:1:5) for 10 to 15 minutes and then were rinsed using DI water. In the next step we remove the oxide layer from the surface of the sample. The solution used in this step contains $\text{HF}:\text{H}_2\text{O}$ (1:50) and the samples are immersed in the solution for 1 to 2 minutes. The third step is to place the sample in an 80°C solution of $\text{HCl}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (1:1:6) for another 10 to 15 minutes followed by rinsing them with DI water to remove the ionic

contaminants. Although in this step the solution is placed on the hot plate, it should not reach the boiling point. [51]

3.1.2. Anisotropic Etching

In this step we textured the surface of the sample in order to improve the result of the experiments. We have used an oil bath that is heated between 90°C to 100°C. The <100> plane prepared silicon samples are located in a solution made from TMAH 25% and DI water. During the experiments, different density of the solution, different process timings, and different temperatures were examined in order to get the most uniform results.

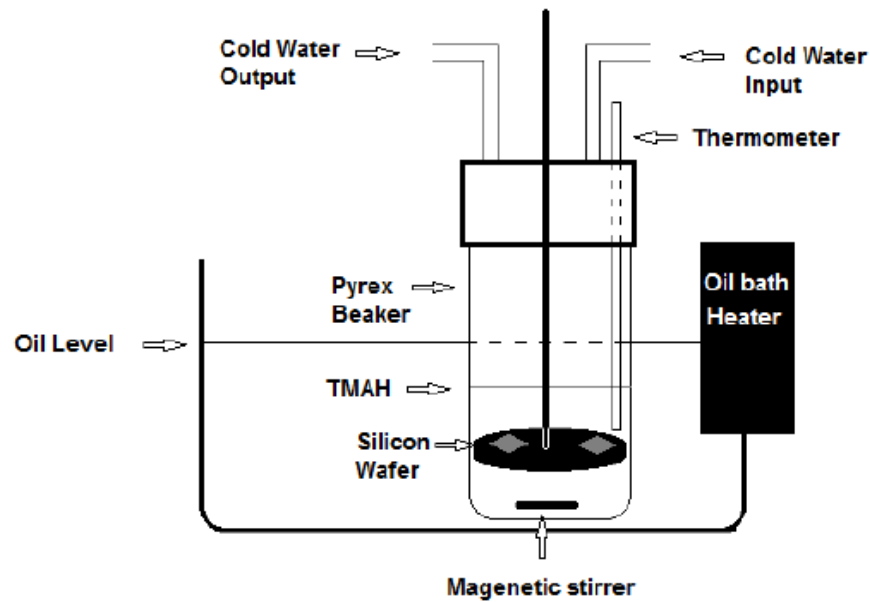


Figure 3.1. Schematic view of the oil bath and the etching process. During the process, a cold water flow is available on top of the beaker in order to avoid any change in the solution concentration

When we put the <100> plane silicon wafer in the heated TMAH-DI water solution, the anisotropic wet-etching process will start. The wafer will be etched in different directions, which leads to the pyramid-shaped textures on the surface. The etching speed and the size of pyramids depend on the TMAH solution concentration and the duration of etching.

As illustrated in Figure 3.1, during the experiments the samples were placed horizontally in order to have a unique condition for the whole surface. This is to prevent the damage that will be caused by air bubbles that are released during the etching process.

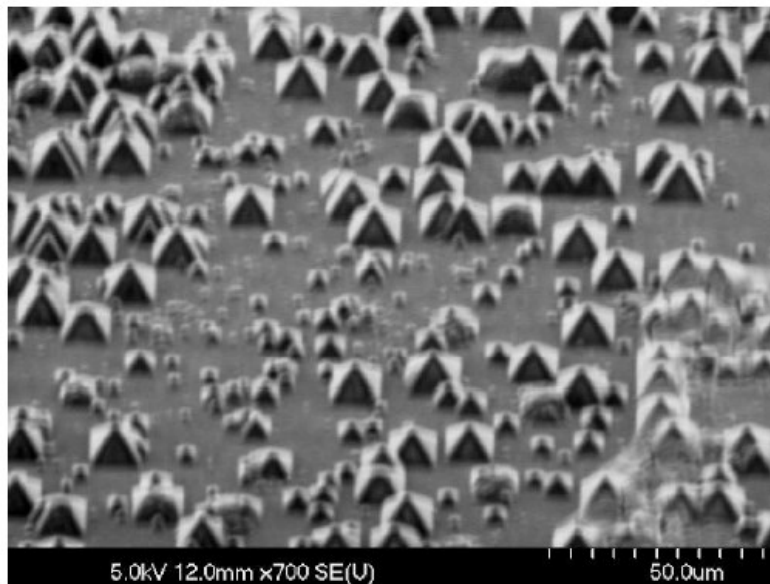


Figure 3.2. SEM image of pyramids on the surface of the sample after TMAH wet-etching

3.1.3. Metallization and Annealing

Metallization is the process of covering any non-metal surface with metal. In order to have accurate results close to our expectations, a good ohmic contact is required. The ohmic contact is defined as the contact between semiconductor and the metal, which allows for an easier flow of electronic carriers from and into the semiconductor. Gold, silver and many other metals can be

used for metallization, but aluminum is an excellent candidate due to its high conductivity, low melting point, and reasonable price.

Figure 3.3 demonstrates the instrument that is used in the laboratory to perform metallization. The metallization technique used in this project is known as Filament Evaporation. A disposable tungsten basket is located in the vacuum container that will be filled with the required amount of aluminum. Each side of this basket is contacted to electrodes. The aluminum will be heated and start boiling due to the high current flow through the basket. When the evaporation happens, the container cap and all silicon wafers that are attached to the cap will be covered by aluminum atoms.



Figure 3.3. Metallization machine

It is important to remember that in our technique, metallization should be performed after wet-etching (section 3.1.2) since TMAH will etch the aluminum that has covered the samples.

The metallization by itself will not provide a good ohmic contact due to the existence of tiny spaces between silicon and aluminum surface. In order to avoid this space, a furnace is used to heat the samples up to 500°C. During the process, hydrogen and nitrogen gases are circulating in the container. The combination of interface free atoms with hydrogen will reduce the sample's resistance. This process is known as annealing.

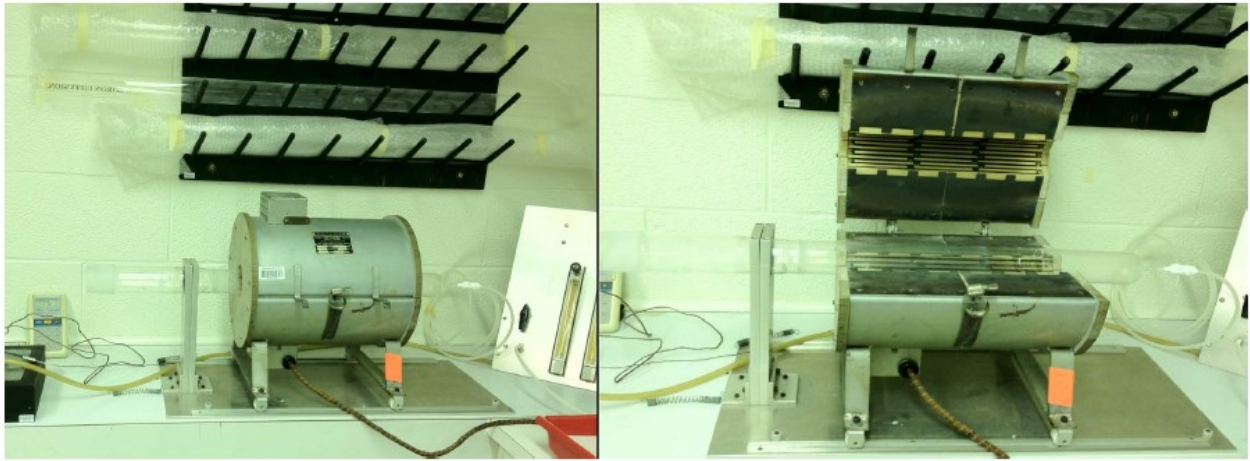


Figure 3.4. Annealing machine used during experiments

3.1.4. Electrochemical Etching

After texturing the surface of the samples, they will be electrochemically etched. This process is performed in the presence of an anodic current. The solution used is Hydrofluoric (HF) acid mixed with Ethanol 95%. Hydrogen bubbles will be produced during the electrochemical etching. Ethanol will remove these bubbles from the surface of the wafer. Fewer bubbles during the chemical etching will lead to a more homogeneous and a uniform structure.

The concentration of HF solution, time duration, and the current passing through the sample are the parameters that affect the result of the experiments. As per experiment results, the applied

current above 80mA will result in silicon electro-polishing. Therefore the current range during the experiments varied between 30mA to 80mA. Figure 3.5 illustrates one part of the facilities used for the electrochemical etching.

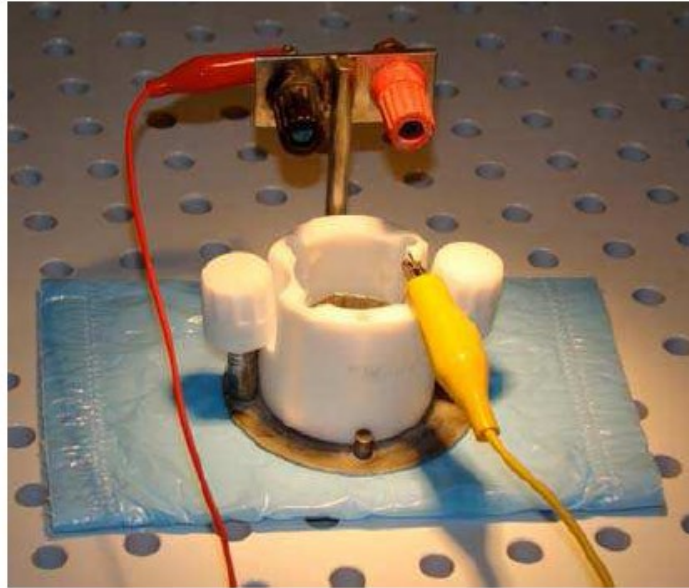


Figure 3.5. Teflon anodization cell used during electro-chemical etching

The current source used during the experiments is a Keithley series 2400 Digital Source Meter. The aluminized side of silicon wafers is used as the anode and a platinum basket is placed into the HF solution as the cathode.

Silicon can be etched only in presence of F⁻. Therefore, positive carriers, also known as holes, are required during the experiment. P-type silicon does not require any extra action since it has more positive carrier than negative. However, if n-type silicon wafers are used, a source of white light will be required in order to excite the electrons. The n-type silicon positive carrier (holes) is less than the negative carriers. The light source we used for n-type samples in this work is 120v and 35W.

After electrochemical etching, a post processing was performed to remove the walls and particulates generated during the fabrications. These particulates could be silicon/silicon oxide particles, and or other impurities. This step helps to remove any extra element in between silicon nanowires.

To do this, the samples were immersed in a 0.2molar NaOH solution in room temperature. This experiment is done on different samples in different time periods.

3.2. Characterization Equipment

3.2.1. Scanning Electron Microscope

Scanning electron microscope (SEM) is a kind of microscope that uses electron beams in order to form the image. Compared to other microscopes, SEM has a higher resolution, higher magnification and since the picture obtained from SEM is captured by electromagnets instead of lenses, SEM has a better controllability. [52]

As illustrated in figure 3.6, SEM has an electron gun that produces a beam of electrons. During the scanning process, the sample chamber is vacuumed. The beam of electrons passes through the electromagnetic field and the lenses, and hits the sample. The vertical contact of the electron beam with the sample will reflect x-rays, primary backscattered electrons, secondary electrons, and auger electrons. The image will be produced by the detectors that convert x-rays and the electrons to the appropriate signal for the screen. [52]

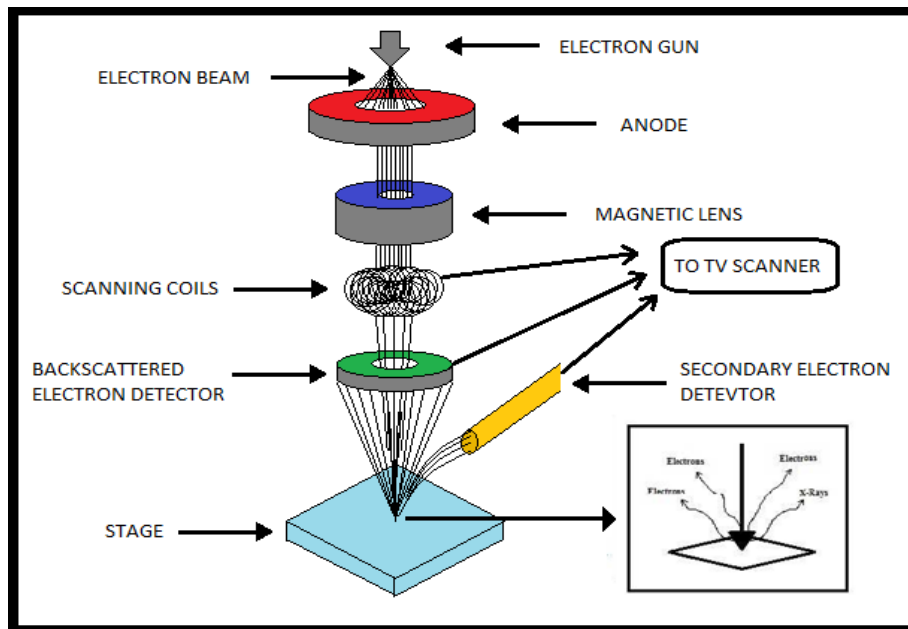


Figure 3.6. Schematic view of a scanning electron microscope [52]

It is important to dry and remove all the moisture from the samples before placing them in the chamber. If the samples are metal and therefore conductive, they can be placed in the vacuum chamber directly. However, if the sample is non-metal, a layer of a conductive material should be applied. [52] In our case, a small piece of carbon double-sided adhesive tape is attached to the back of the sample.

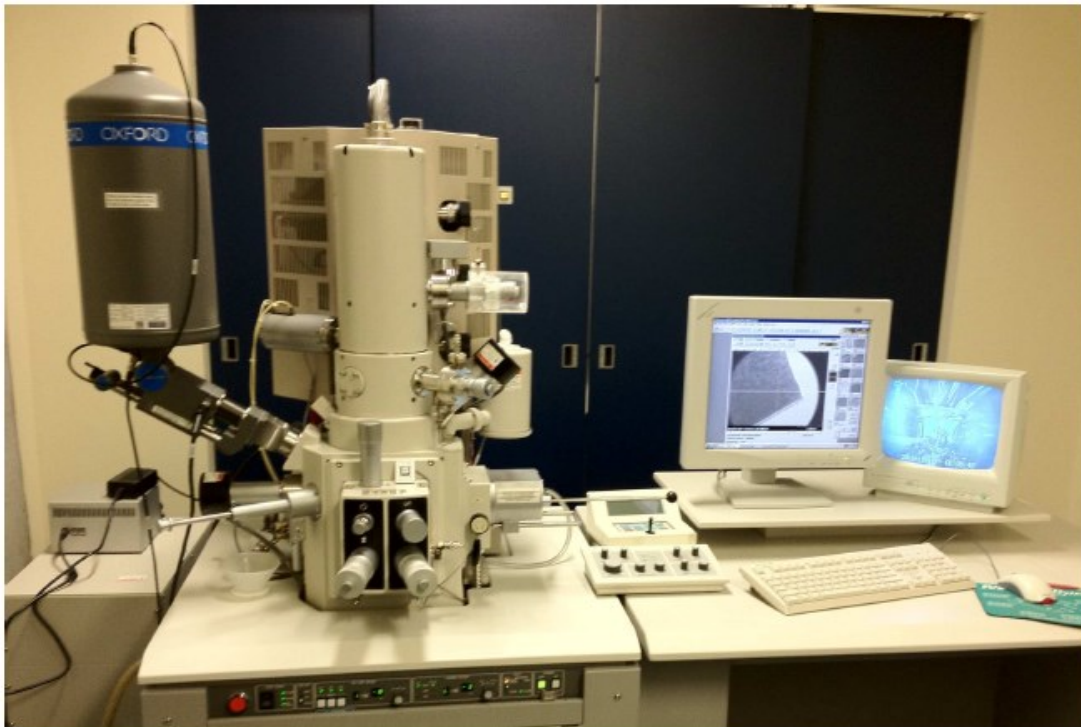


Figure 3.7. Hitachi SEM model S-4700

A sputter coater is a machine that covers the samples with a thin layer of conductors. When the sample is placed in the vacuum chamber of the sputter coater, the argon gas will be realized in presence of an electric field and a gold foil. Due to the electric field, electrons leave argon, therefore the atoms will be charged positively and the negatively charged gold attracts the ions from argon gas. The gold foil knocked atoms will create a thin layer of gold on the surface of the sample. [52]

We should always make a mark or consider a point on the sample in order to have accurate results and to work with any SEM system. This mark or point can be a corner of the sample or the conductive tape. Clean plastic gloves are always necessary. Any extra particles, hand oil, and dust affect the vacuum condition and the accuracy of the scans. The SEM machine cannot be used to scan the pulverized ferromagnetic samples due to their strong magnetic fields. Setting the proper height, voltage, and magnification are the few points that affect the accuracy of the captured images. SEM pictures of this work are illustrated in the next chapter.

3.2.2. Energy-dispersive X-ray Spectroscopy

Energy-dispersive X-ray spectroscopy (EDX) is used to characterize the elements available in the fabricated nanowires.

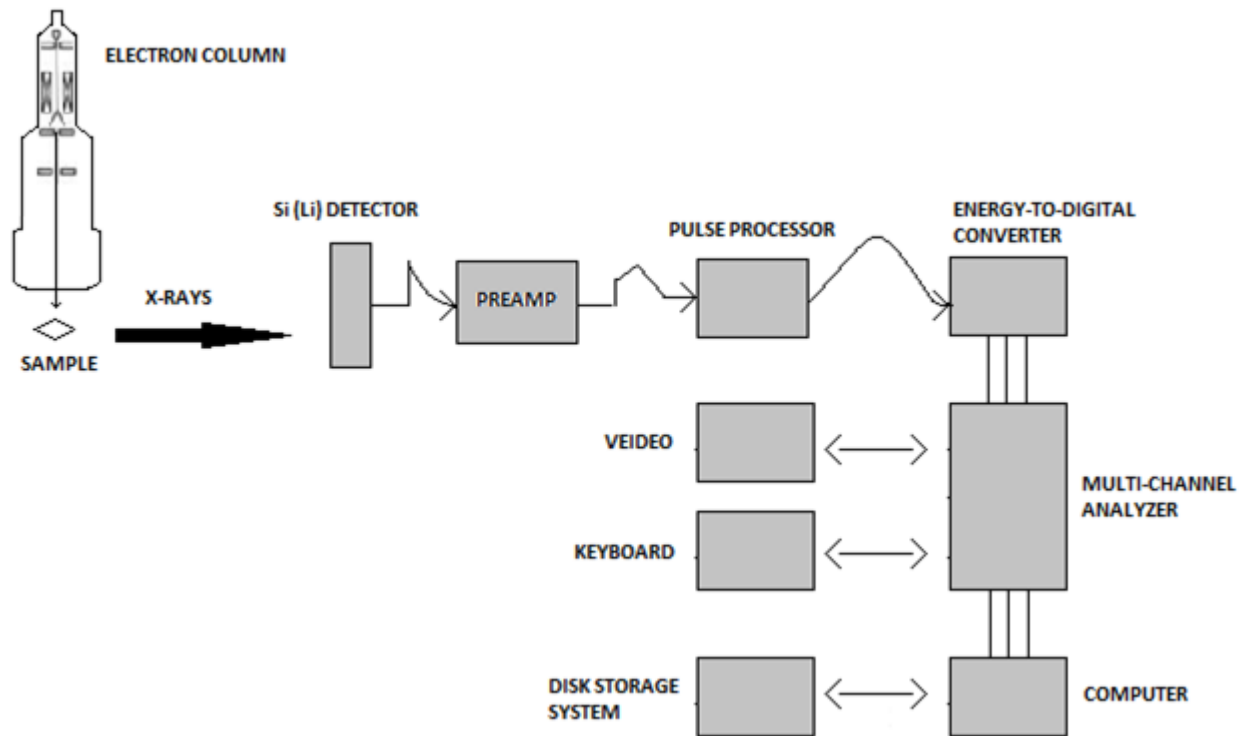


Figure 3.8. Schematic view of a typical EDX [53]

EDX is a chemical micro-analytical method that is used in order to study the chemical and structural characterizations of a sample. Some typical applications for the DEX techniques are rapid material alloy identification, foreign material, coating composition and small component material analysis, corrosion evaluation, phase identification and distribution. This technique is used as a conjunction with SEM. The technique is based on the interaction between the x-ray sources and the sample. Each element has a specific atomic structure. Therefore, under x-ray spectrum or electron bombardment of the sample, each element reaches a unique peak of excitation which will be detected by the EDX technique. The main components in this system are the X-ray source and detector, a pulse processor and an analyzer. [54]

The detectable range of energy for an EDX system is defined by the comparison between the values of the samples' x-ray energy and the known characteristics of x-ray energy. The x-ray energy value of different elements can be found in most of the periodic tables of elements. The EDX has the capability to detect all the elements with an atomic number between beryllium (4) and uranium (92).

Another ability of EDX technique is element mapping. The intensities of the reflected X-ray are measured considering the literal position on the surface of the sample and the difference among these intensities, as well as the characteristic energy values defined by the concentration of each element on the surface of the samples. [54]

There are also some sample requirements that should be considered in order to have more accurate results. The samples placed in the vacuum chamber must be compatible with pressures under 2Torr which is a moderate vacuum atmosphere. The sample size is also a parameter that affects the accuracy of the images. It is preferable not to place samples with a diameter larger

than 200mm in the vacuum chamber, since samples with larger diameters have less movement flexibility and might also damage the SEM lenses. Also the maximum permitted height for a sample is 50mm. [54]

Chapter 4: Experimental and fabrication results

4.1. Anisotropic Etching Results

Silicon wafers that are used in this project can be divided into n-type and p-type groups. In the texturing stage the temperature, TMAH solution density, and etching time are the three parameters that they affect the results of the experiments.

A short summary of some of different conditions experienced in this step are illustrated in table 4.1.

Sample #	Sample Type	Etching Time	Solution Concentration	Uniformity
1	<100> p-type	15 min	3%	High Uniformity(*)
1	<100> p-type	45 min	4%	Low Uniformity
1	<100> p-type	45 min	5%	Low Uniformity
1	<100> p-type	5 min	2%	Medium Uniformity
1	<100> p-type	25 min	2%	Medium Uniformity
1	<100> p-type	15 min	1%	Medium Uniformity
1	<100> p-type	60 min	4%	Medium Uniformity
2	<100> n-type	45 min	2%	High Uniformity
3	<100> p-type	5 min	2%	High Uniformity
3	<100> p-type	30 min	5%	Low Uniformity
3	<100> p-type	30 min	1%	Medium Uniformity
4	<100> p-type	15 min	3%	High Uniformity(*)
4	<100> p-type	25 min	2%	Medium Uniformity
4	<100> p-type	60 min	3%	Medium Uniformity
5	<100> n-type	15 min	3%	High Uniformity
6D2	<100> p-type	20 min	2%	High Uniformity

6	<100> p-type	15 min	1%	High Uniformity(*)
6	<100> p-type	60 min	2%	Medium Uniformity
7	<100> p-type	60 min	3%	Medium Uniformity
9	<100> n-type	5 min	2%	High Uniformity(*)
9	<100> n-type	15 min	3%	High Uniformity
9	<100> n-type	45 min	5%	High Uniformity
10	<100> p-type	55 min	2%	High Uniformity
10	<100> p-type	15 min	3%	High Uniformity
10	<100> p-type	30 min	2%	Medium Uniformity
11	<100> n-type	40 min	2%	High Uniformity
12	<100> p-type	5 min	2%	Low Uniformity(*)

Table 4.1. The summary of various conditions experiments during the wet-etching step

In order to study the effect of the TMAH etching on the nanowire fabrication, the samples obtained from the texturing process were divided into three groups with different pyramid concentrations: Low concentration, medium concentration, and high concentration. Three different sample concentrations are shown in in Figure 4.1.

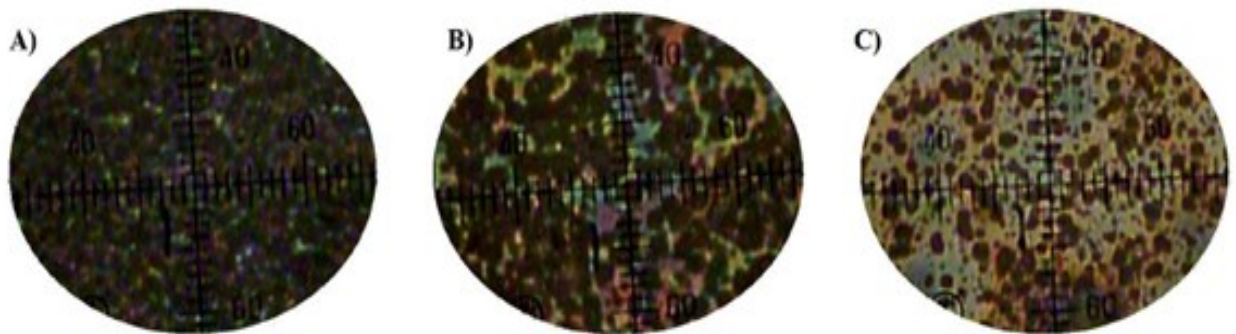


Figure 4.1. Images obtained from the optical microscope. A) High concentration of pyramids; B) Medium concentration of pyramid,s and C) Low concentration of pyramids

From each group few samples that have the most uniformity, smaller pyramids and shorter etching time are chosen for the next steps of the experiments.

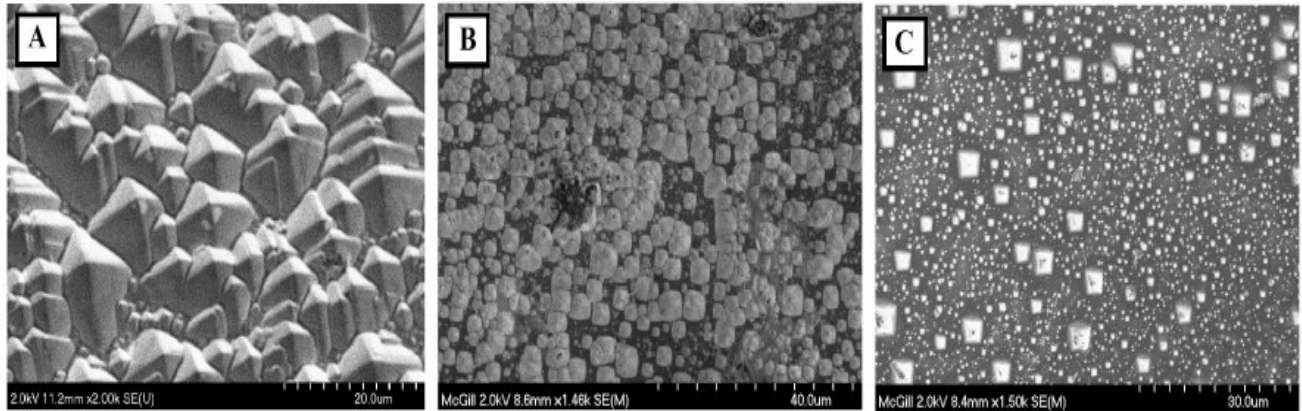


Figure 4.2. SEM images from three different samples with various pyramid concentrations: A) High concentration of pyramids; B) Medium concentration of pyramids and C) Low concentration of pyramids

4.2. Electrochemical Etching results

Table 4.2 illustrates a summary of electrochemical etching experiments.

Sample #	Sample Type and Resistivity	HF:ethanol	Etching Time	Current Density
W1	p-type<100>	1:3	30 min	70 mA
W1	p-type<100>	1:3	45 min	70 mA
W1	p-type<100>	1:3	30 min	65 mA
W3	p-type<100>	1:3	30 min	40 mA
W3	p-type<100>	1:3	60 min	65 mA
W3	p-type<100>	1:3	30 min	40 mA
W3	p-type<100>	1:3	60 min	65 mA
W4	p-type<100>	1:3	30 min	40 mA
W4	p-type<100>	1:3	60 min	65 mA
W4	p-type<100>	1:3	30 min	40 mA
W4	p-type<100>	1:3	60 min	65 mA
W6	p-type<100>	1:3	30 min	40 mA
W6	p-type<100>	1:3	60 min	65 mA
W6	p-type<100>	1:3	30 min	40 mA
W6	p-type<100>	1:3	60 min	65 mA
W9	n-type<100>	1:3	30 min	40 mA
W9	n-type<100>	1:3	60 min	40 mA
W9	n-type<100>	1:3	30 min	65 mA
W9	n-type<100>	1:3	60 min	65 mA
W12	p-type<100>	1:3	30 min	40 mA
W12	p-type<100>	1:3	15 min	70 mA
W12	p-type<100>	1:3	30 min	70 mA
W12	p-type<100>	1:3	45 min	70 mA
W12	p-type<100>	1:3	60	70 mA

Table 4.2. Some of the applied conditions during the electro-chemical etching experiments

As illustrated in Figure 4.3, using p-type or n-type silicon wafers will strongly affect the result of the experiments. N-type silicon is mostly suitable for PS fabrication while p-type silicon have much better results in fabrication of nanowires.

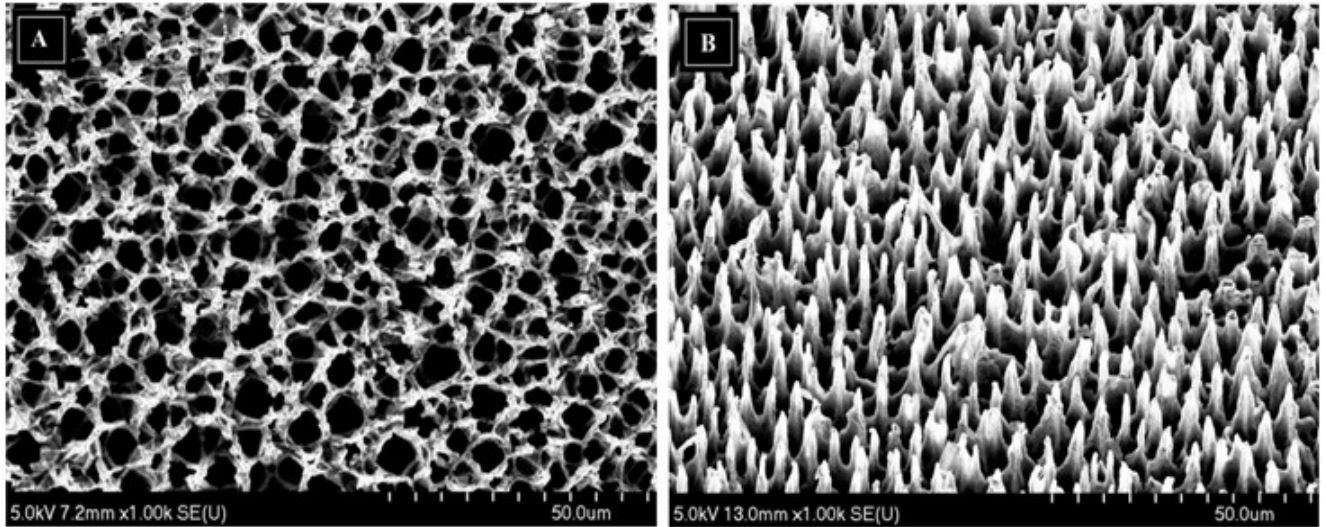


Figure 4.3. SEM images. A) n-type Si wafer, resistivity of 10-20 Ω cm; B) p-type Si wafer, resistivity of 10-20 Ω cm. Both of these wafers had a high density of pyramids before electrochemical etching. The electrochemical etching conditions are: 30 minutes, HF:Ethanol (1:3), 65mA applied currents

As it is explained in section 3.1.4, after the electro-chemical etching, samples are immersed in 0.2molar NaOH at room temperature. The NaOH solution removes the yellow layers from the surface of the wafer. However the duration of immersion is important since it can damage the fabricated nanowires. Figure 4.4 illustrates the SEM image of a sample before and after the NaOH experiment.

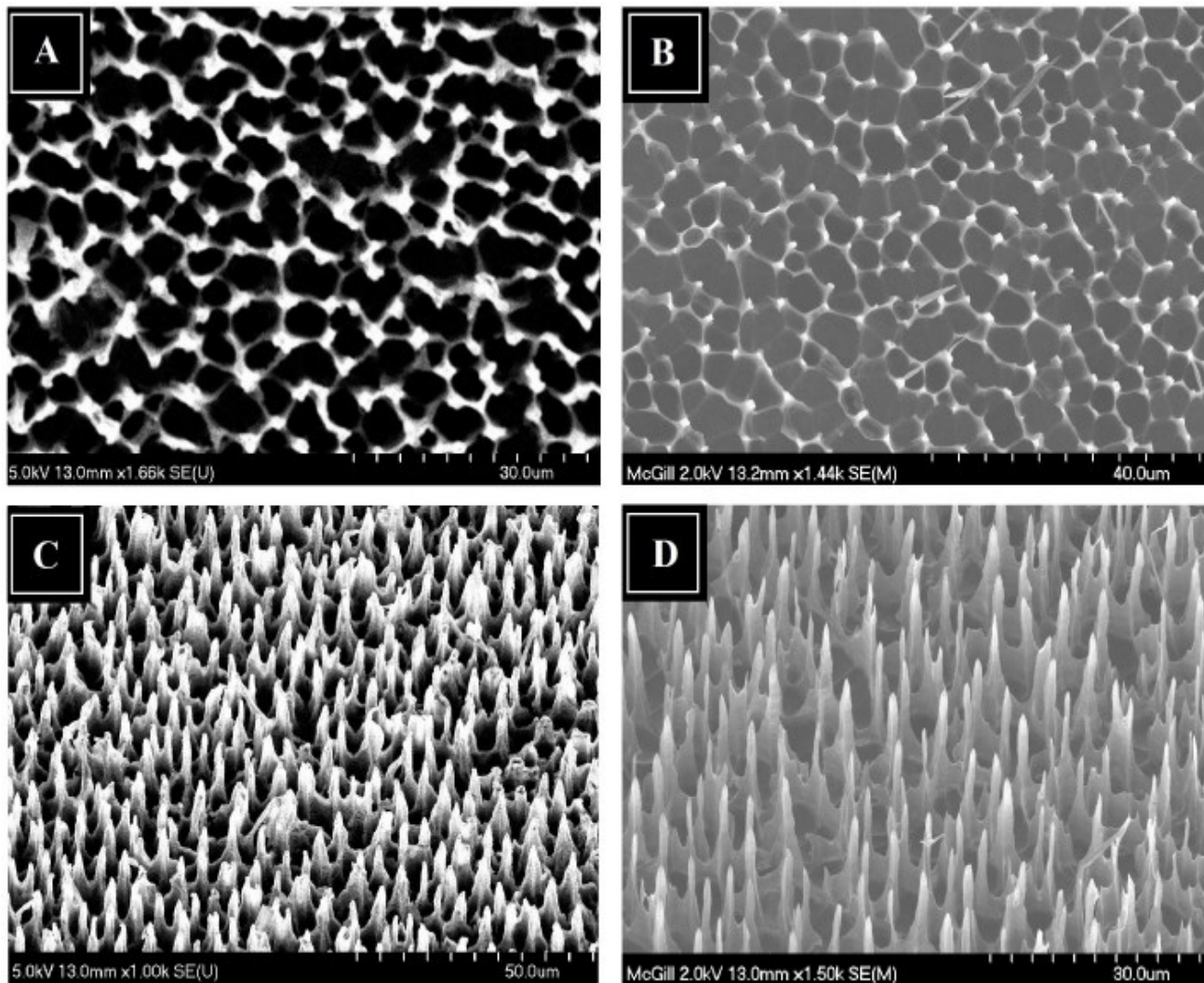


Figure 4.4. SEM image of silicon nanowires. A) No NaOH, top view; B) 30seconds NaOH immersion, top view; C) No NaOH, side view; D) 30 seconds NaOH immersion, side view

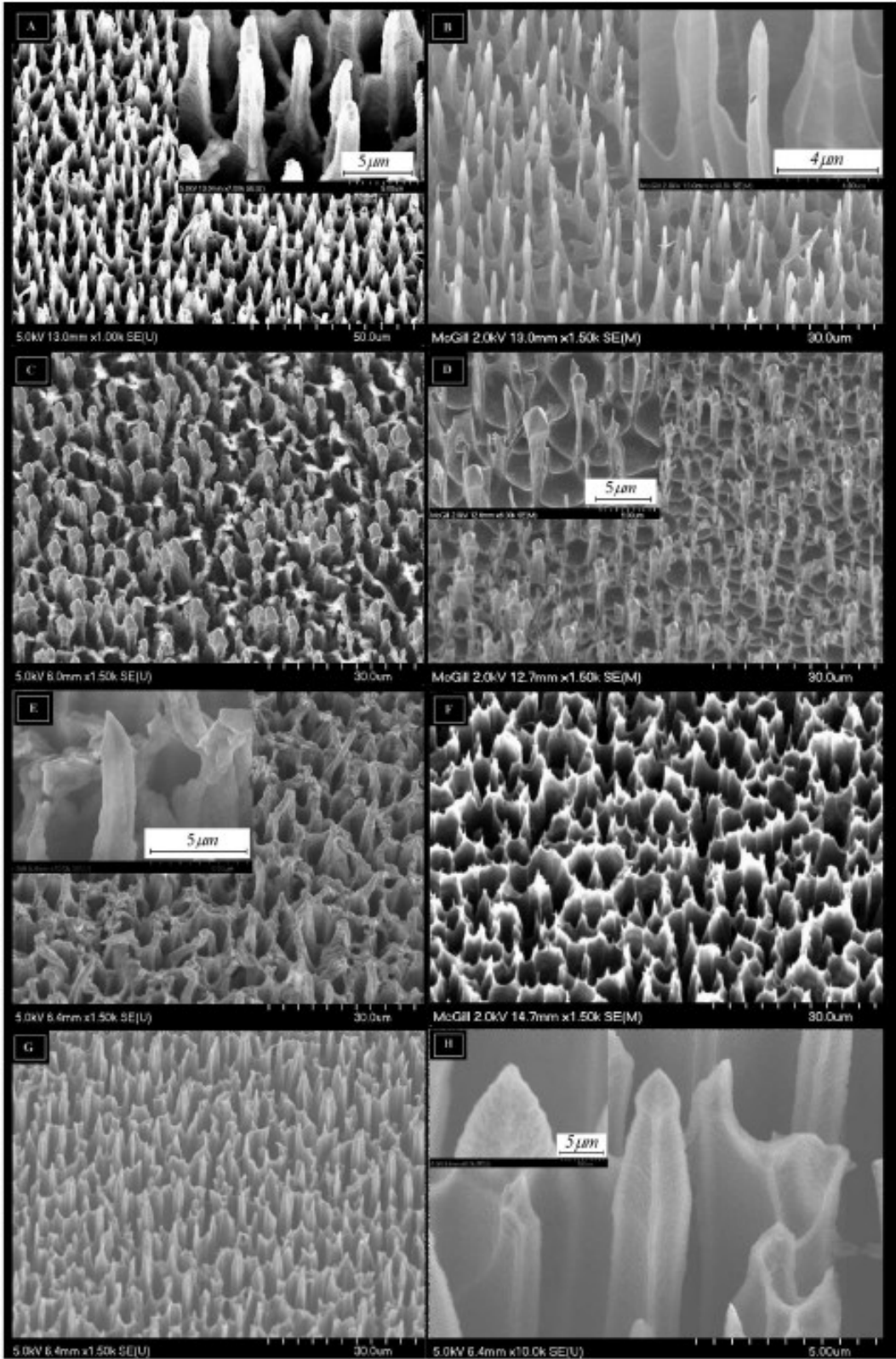


Figure 4.5. SEM image of some of the fabricated Si nanowires

Figure 4.5 illustrates some of the silicon nanowires that are fabricated in this work.

Each of the samples illustrated in this figure is fabricated under different fabrication parameters. The effect of different parameters on the fabrication results will be explained in chapter 5.

Figure 4.5.A presents silicon nanowires with no NaOH immersion. This sample is textured in a 3% TMAH solution for 15 minutes and it is electrochemically etched for 45 Minutes, in a (1:3) HF:ethanol solution with an applied current of 70mA. Since this is a p-type silicon wafer, the electrochemical etching is performed without presence of white light. Figure 4.5.B illustrates the nanowires in figure 4.5.A after being immersed in a 0.2molar NaOH solution for 30 seconds. As it is shown in the figure, these nanowires are thinner than the ones in the previous image.

For fabrication of the nanowires represented in figure 4.5.C, p-type silicon wafer is used. The texturing parameters in this process are again 3% TMAH solution and 15 minutes duration. The anodization parameters are 70mA applied current, no light as this is a p-type silicon wafer and (1:3) HF:ethanol solution for 30 minutes. Figure 4.5.D is showing nanowires fabricated in the same condition as nanowires illustrated in figure 4.5.C, however they have been placed in NaOH for 2mins.

For nanowires in figure 4.5.E, the texturing is 25 minutes in a 2% TMAH solution. This sample is then electro-chemically etched for 30 minutes in (1:3) HF:ethanol solution while an applied current of 65mA is passing through the sample. This wafer is a p-type sample. During the electro-chemical etching no light is available. Figure 4.5.F presents the result of 1 minute immersion of the sample in figure 4.5.E in NaOH.

Finally, figure 4.5.G and H illustrates a p-type that is textured in a 2%TMAH solution for 30 minutes. Later, this sample is etched in a (1:3) HF:ethanol solution with a 65mA applied current for 60 minutes. No light is applied due to the type of the silicon wafer.

The main objective of this work is to fabricate silicon nanowires. However during the experiments, due to the parameters and condition, some samples resulted in porous silicon. These results are shown in figure 4.6.

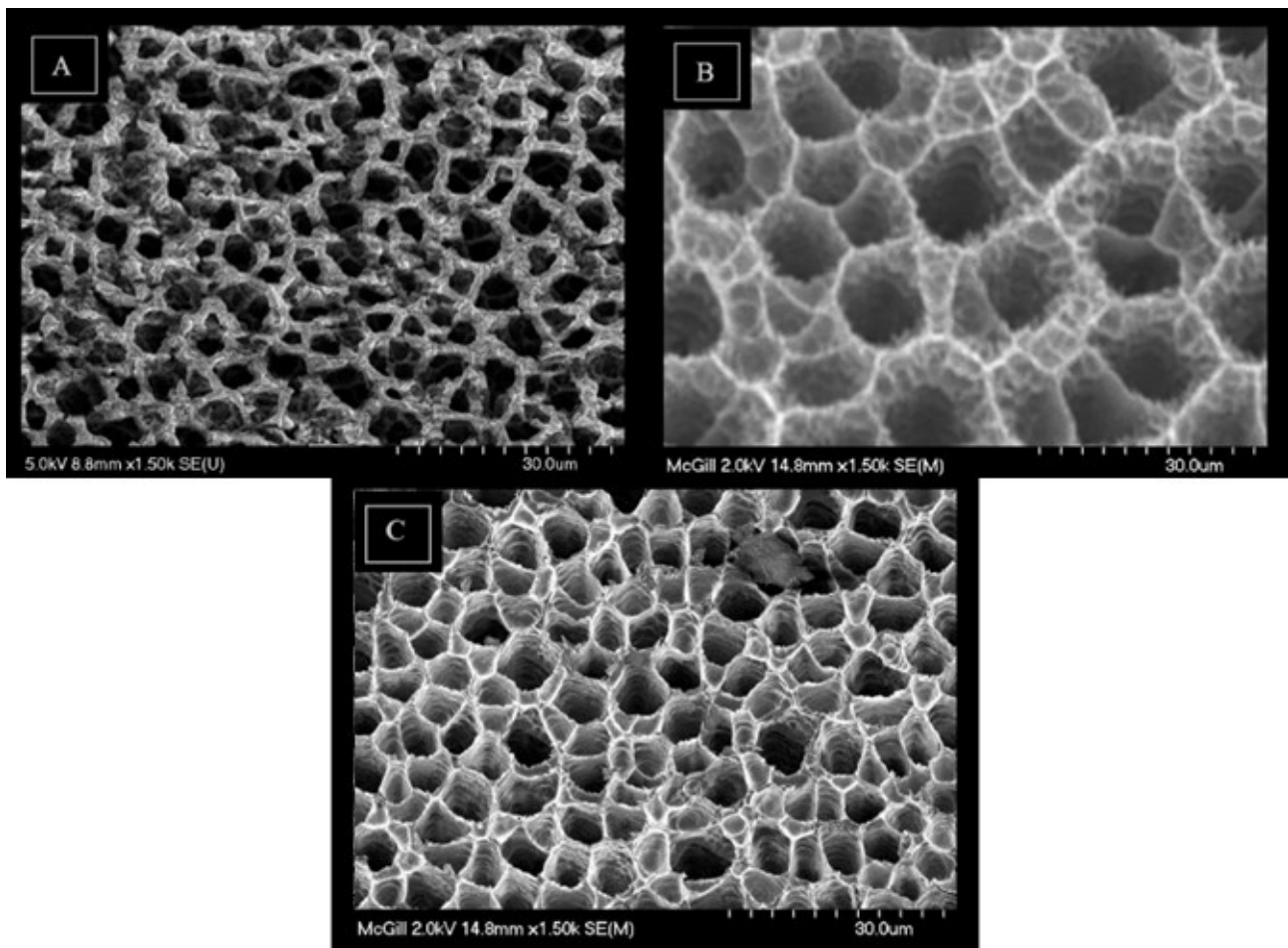


Figure 4.6. Porous silicons fabricated during the experiments

Figure 4.6.A illustrates the <100> n-type sample that is etched in an 2% TMAH solution for 15 minutes and then electro-chemically etched for 60 minutes in the (1:3) HF:ethanol solution with an applied current of 40mA. This process is done under a white light source of 120v and 35W. Figure 4.6.B illustrates the <100> n-type wafer etched in a 2%TMAH solution for 15-minute. The electro-chemical etching is performed with (1:3) HF:ethanol solution for 30 minutes and the applied current is 65mA. A white light source of 120v and 35W is available during the process. This sample is then immersed in 0.2molar NaOH solution for 1 minute.

Figure 4.6.C is <100> n-type sample that is etched in 2% TMAH solution for 15 minutes. Then it is electrochemically etched in presence of the same light source, in the (1:3) HF:ethanol solution for 60 minutes and 65mA current is applied. This sample is also immersed in 0.2molar NaOH solution for 1 minute.

4.3. EDX Measurements; Chemical Compositions

The EDX chemical characterization is performed on the fabricated silicon nanowires. Figure 4.7 shows the result of EDX measurement on the sample illustrated in Figure 4.5.B.

This measurement is performed on different samples. As it can be seen in the picture the only recognised element in the sample is Si. The study of the result of EDX shows that by performing all the fabrication steps explained in this work, the final sample will be made of only one material which is Si and no SiO₂ or other impurities exist on the surface and inside of the sample.

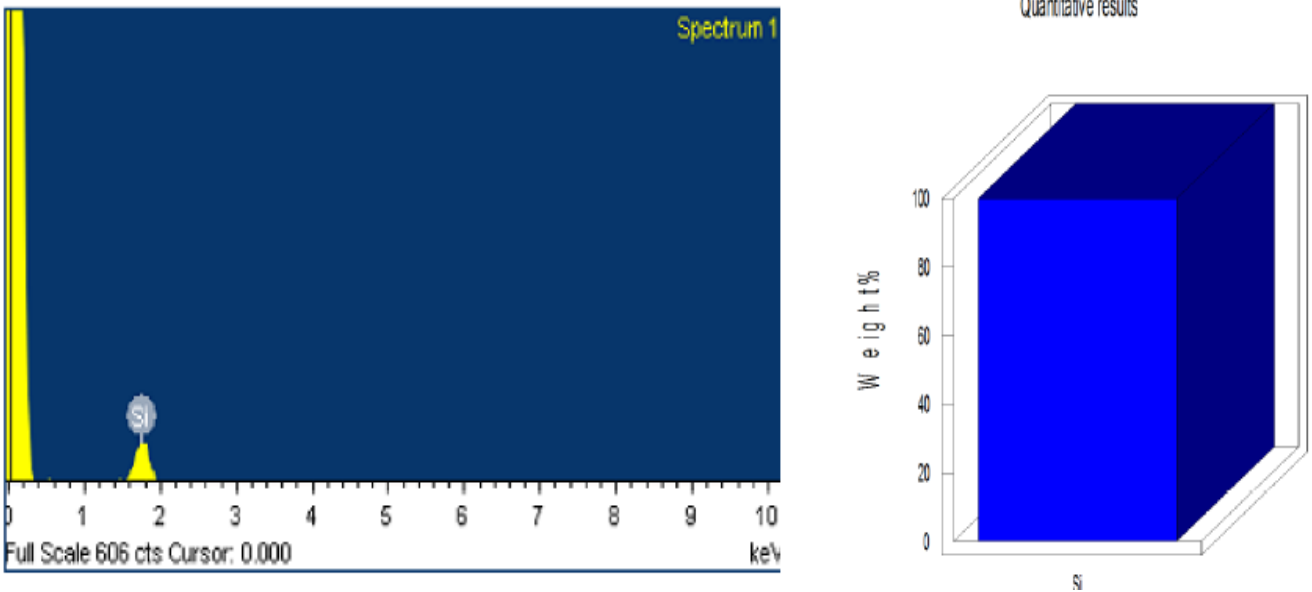


Figure 4.7. EDX chemical characterization of the fabricated nanowires

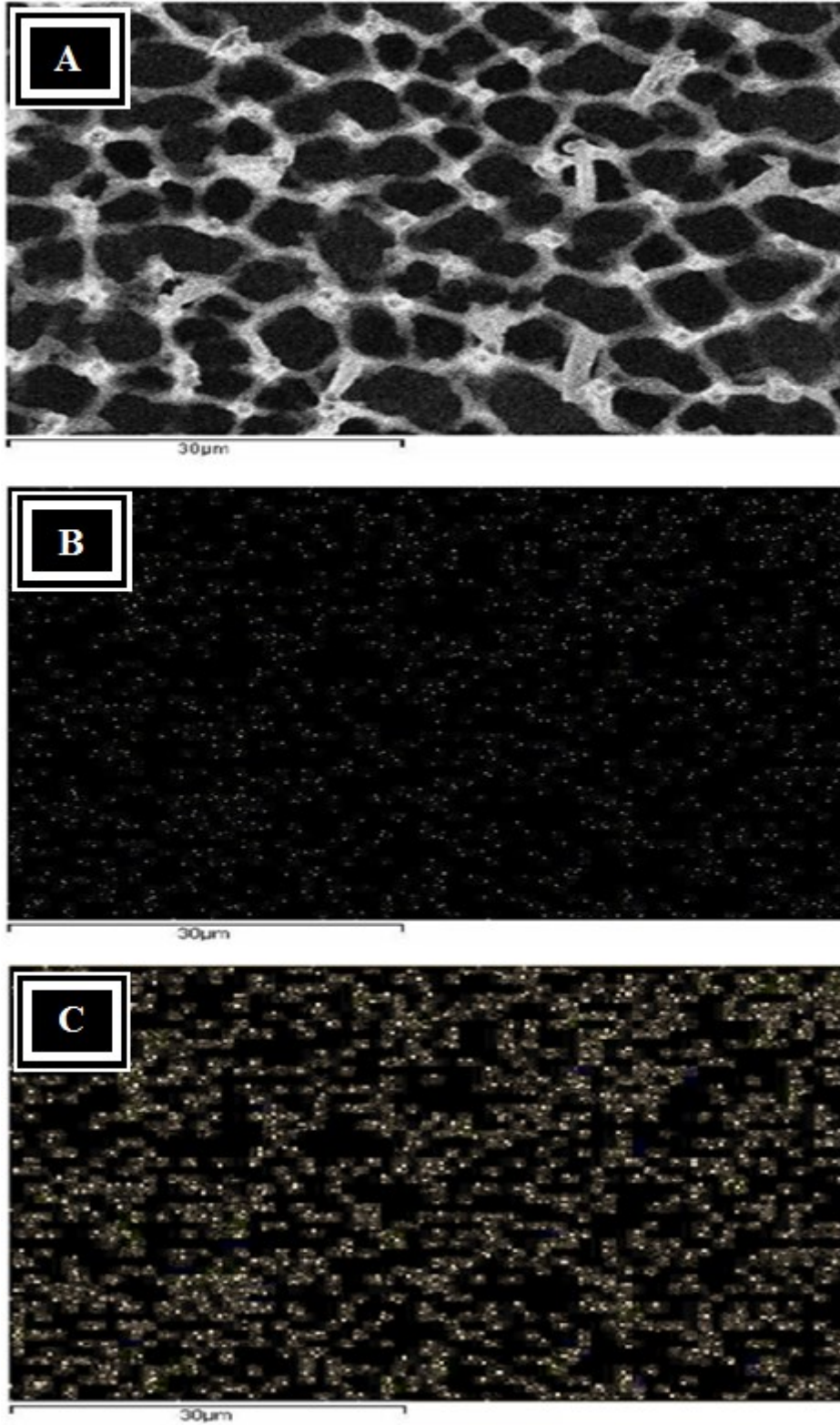


Figure 4.8. Elemental mapping of fabricated Si nanowire

In the next stage, the elemental mapping is performed on the sample illustrated in figure 4.5.B. The yellow dots map the location of silicon nanowires. This helps us to know the materials that exist inside and on the surface of the sample. Also it illustrates the location of each of these elements with different colors. As it is illustrated in figure 4.8, the only element available in this sample is Si. Figure 4.8. A illustrates a top view x-ray image from the sample and figure B is the location mapping of Si. Since this image is not clear enough, in figure C we have increased the color contrast of picture B. The lighter and whiter the dots are, they have a longer and they are higher than the surface of the sample.

Chapter 5: Discussion, Conclusion and future work

5.1 Discussion

In this section we will study the effects of different parameters on the experiments.

As per experiments during the anisotropic etching, by increasing the temperature the etching rate will be increased; however a boiling solution reduces the uniformity of pyramids. During the texturing, the solution temperature is 85°C.

Reducing the amount of TMAH and therefore the density of the solution increases the number of pyramids on the surface. The preferred solution density in this work is 1%, 2%, and 3% TMAH solution.

On the other hand, each time we had a longer etching time, the experiment resulted in bigger hillocks on the surface of the sample.

The textured samples from the anisotropic etching are divided into three categories depending on their uniformity and the density of the pyramids on their surfaces. In each of these category those samples that had the most uniformity with high, medium, and low densities are chosen for the next steps.

As the results shows, by increasing the HF concentration, the etching rate and porosity decrease. However, if the current density gets increased, both etching rate and porosity will increase. As mentioned before, applying the current density of 80mA and more leads to a polished wafer.

Applied current, duration of etching and silicon wafer types are three parameters that affect the fabrication process. If we increase the duration of etching, the etching rate will increase and this will result in deeper etching. Also, by increasing the current density we can increase the etching rate. Different wafers with different resistivity have different electro-polishing densities. The lower the wafer's resistivity, the lower the electro-polishing current density will be.

P-type silicon wafers are suitable for fabrication of Si nanowires, while n-type silicon wafer are good candidates for porous silicon fabrications.

5.2. Conclusion and future work

In this work, we have fabricated silicon nanowires. The technique used for fabrication is electrochemical etching. Prior to this step, samples are textured using TMAH solution. A solution of hydrofluoric acid (HF) and ethanol is used during the fabrication. Different parameters that can affect the result of fabrications are studied. Similar experiments with different parameters are performed for each sample. To texture the samples, the TMAH solution is used to perform anisotropic etching. The solution concentration and etching time are parameters that are studied. In the electro-chemical etching process etching time, HF:ethanol solution concentration, light illumination, silicon wafer type, and the applied current density are studied.

EDX is used to characterize the elements available on the samples. Considering all the fabricated structures, <100> p-type silicon wafers with resistivity of 10-20Ωcm are the most suitable option for the fabrication of silicon nanowires since they require shorter etching time, low solution concentration, and result in longer and thinner silicon nanowires. On the other hand, the

experiments illustrate that n-type <100> silicon wafers are a suitable candidate for fabrication of porous silicon.

- To create textures on the surface of silicon wafers, anisotropic etching is performed. Temperature, solution concentration, and etching time are three parameters that were varied and their effect studied.
- The electro-chemical etching is performed on the prepared samples. In this stage the effects of etching time and the applied current density are studied.
- Increasing the duration of the anisotropic etching results in more large pyramids on the surface.
- By increasing the TMAH solution concentration, smaller pyramids can be obtained.
- Higher temperature during the anisotropic etching increases the speed of the etching rate.
- If the uniformity of pyramids on the surface increases, the uniformity of silicon nanowires will increase.
- Increasing the duration of electrochemical etching and reducing the solution concentration results in longer and thinner silicon nanowires.
- By increasing the applied current density the etching rate increases, however passing the electro-polishing peak result in a smooth surface.
- The electro-polishing peak varies in wafers with different resistance. Wafers with higher resistivity have a higher electro-polishing peak.

Obviously, the initial growth of pyramids and porous silicon has large effect on nanowires. It is important to understand the growth mechanism. The study of the growth mechanism as well as

more detail on the effect of resistivity of the wafer in fabrication process and fabricated nanowires are two subjects that can be introduced as the future work.

References

- [1] J. Uldrich and D. Newberry, "The Next Big Thing Is Really Small: How Nanotechnology Will Change the Future of Your Business", Publisher: Crown Publishing Group, First edition, 2003.
- [2] R. E. Krebs, "The History and Use of our Earth's Chemical Elements", Greenwood Publishing Group, Second Edition, 2006.
- [3] A. Halimaoui, "Porous silicon formation by anodization", Canham, LT, Institution of Engineering and Technology, London, 1997.
- [4] Zh. Huang, H. Fang, and J. Zhu, "Fabrication of Silicon Nanowire Arrays with Controlled Diameter, Length, and Density", *Advanced Materials*, Vol. 19, pp744-748, 2007.
- [5] T. Ito, S. Okazaki, "Pushing the limits of lithography", *NATURE*, Vol. 406, pp. 1027-1031, 2000.
- [6] I. V. Markov, "Crystal growth for beginners: fundamentals of nucleation, crystal growth and epitaxy", World Scientific Publishing Co. Pte. Ltd., Second Edition , 2003.
- [7] J. Ramanujam, Daryoush Shiri, A. Verma, "Silicon Nanowires Growth and Properties: A Review", *Materials Express*, Publisher: American Scientific Publishers, Vol. 1, Number 2, pp. 105-126, 2011.
- [8] J. R. Creighton and P. Ho, "Chemical Vapor Deposition", ASM International, Chapter 1, 2001.

- [9] “LPCVD. Technology and Equipment”, Koyo Thermo Systems Co., Ltd., Available on: <https://www.crystec.com/klllpcvde.htm> , 27/11/2013, 12:18 PM.
- [10] Sh. Fan, M. G. Chapline, N. R. Franklin, T. W. Tomblor, A. M. Cassell, H. Dai, “Self-Oriented Regular Arrays of Carbon Nanotubes and Their Field Emission Properties”, *Science*, Vol. 283, pp. 512-514, 1999.
- [11] P. Cheyssac, M. Sacilotti, and G. Patriarche, “Vapor-Liquid-Solid Mechanisms: Challenges for nanosized quantum cluster/dot/wire materials”, *Journal of Applied Physics*, Vol. 100, Issue 4, p. 044315, 2006.
- [12] H. Choi, “Chapter 1: Vapor–Liquid–Solid Growth of Semiconductor Nanowires from Semiconductor Nanostructures for Optoelectronic Devices”, Springer-Verlag Berlin Heidelberg, 2012.
- [13] R. S. Wagner and W. C. Ellis, “VAPOR-LIQUID-SOLID MECHANISM OF SINGLE CRYSTAL GROWTH”. *Applied Physics Letters*, Volume 4, Issue 5, pp. 89 1964.
- [14] S. Buntin, Staff: S. Eustis (NRC), M. Beversluis (NRC), D. Meier, B. Nikoobakht, “Analysis of Copper Incorporation into Zinc Oxide Nanowires”, National institute of Standards and technology, Materials Measurement Science Division, pp. 368-376, 2008.
- [15] A. Hashim, “Nanowires - Fundamental Research”, InTech, pp. 317-319, 2011.
- [16] M. Geissler, H. Wolf, R. Stutz, E. Delamarche, U. Grummt, B. Michel and A. Beitsch, “Fabrication of Metal Nanowires Using Microcontact Printing”, American Chemical Society, pp 6301–6311, 2003.
- [17] D. Natelson, “Fabrication of metal nanowires”, INIST-CNRS, pp. 157-183, 2003.

- [18] E. C. Walter, R. M. Penner, H. Liu, K. H. Ng, M. P. Zach and F. Favier, “Sensors from electrodeposited metal nanowires”, *Surf. Interface Anal.*, pp. 409–412, 2002.
- [19] G. Kartopu and O. Yalçın, “Fabrication and Applications of Metal Nanowire Arrays Electrodeposited in Ordered Porous Templates” from “Electrodeposited Nanowires and their Applications”, InTech, pp114-140, 2010.
- [20] C. A. Stafford, “Metal Nanowires: Quantum Transport, Cohesion, and Stability”, *phys. stat. sol. (b)* 230, No. 2, pp. 481–489, 2002.
- [21] Sh. A. Dayeh, A Ph.D. thesis on “Semiconductor Nanowires for Future Electronics: Growth, Characterization, Device Fabrication, and Integration”, University of California, San Diego, Available online: <http://escholarship.org/uc/item/8rq81617>, 27/11/2013, 3:32PM.
- [22] Th. Stelzner, M. Pietsch, G. Andrä, F. Falk, E. Ose and S. Christiansen, “Silicon nanowire-based solar cells”, *Nanotechnology*, Volume 19, Number 29, 4pp., 2008.
- [23] Y. Choi, J. Zhu, J. Grunes, J. Bokor and G. A. Somorjai, “Fabrication of Sub-10-nm Silicon Nanowire Arrays by Size Reduction Lithography”, *J. Phys. Chem. B*, 107, pp. 3340–3343, 2003.
- [24] G. Zheng, W. Lu, S. Jin and Lieber, “Synthesis and Fabrication of High-Performance n-Type Silicon Nanowire Transistors”, *Advanced Material*, Volume 16, Issue 21, pp. 1890–1893, 2004.
- [25] F. Patolsky, G. Zheng, C. M. Lieber, “Fabrication of silicon nanowire devices for ultrasensitive, label-free, real-time detection of biological and chemical species”, *Methods in Molecular Biology*, Volume 790, pp. 223-237, 2011.

- [26] Z. Huang, H. Fang and J. Zhu, “Fabrication of Silicon Nanowire Arrays with Controlled Diameter, Length, and Density”, *Advanced Materials*, Volume 19, Issue 5, pp. 744–748, 2007.
- [27] P. D. Kanungo, R. Kögler, P. Werner, U. Gösele, W. Skorupa, “A Novel Method to Fabricate Silicon Nanowire p-n Junctions by Combination of Ion Implantation and in-situ Doping”, *Nanoscale Research Letters*, 5, pp. 243-246, 2009.
- [28] W. To, Ch. Tsang, H.Li and Zh. Huang , “Fabrication of n-Type Mesoporous Silicon Nanowires by one-step Etching”, *Nano Lett.*, 11 (12), pp. 5252–5258, 2011.
- [29] Sh. Hsu, Ch. Tsai, W. Hsu, F. Lu, J. He, K. Cheng, Sh.Hsieh, H.Wang, Y. Sun, L. Tu, “Fabrication of Silicon Nanowires Field Effect Transistors for Biosensor Applications”, *IEEE*, 2012.
- [30] X. Zhu, H. D Xiong, S. Koo, D E Ioannou, J. Kopanski, J S Suehle, and C. A Richter, “Silicon nanowires on oxide/nitride/oxide for memory application”, *Nanotechnology*, Volume 18, Number 23, 2007.
- [31] M. Shao, D. Ma, Sh. Lee, “Silicon Nanoewires - Synthesis, Properties and Applications”, *European Journal of Inorganic Chemistry*, Volume 2010, Issue 27, pp. 4264–4278, 2010.
- [32] D. Stober, “Nanowire battery can hold 10 times the charge of existing lithium-ion battery”, *Stanford Report*, December 18, 2007, Available on: <http://news.stanford.edu/news/2008/january9/nanowire-010908.html> , 27/11/2013, 8:52PM.
- [33] “Silicon Nanowires In Lithium Batteries”, Available on: <http://newenergyandfuel.com/http://newenergyandfuel.com/2010/09/22/silicon-nanowires-in-lithium-batteries-gets-closer/>, 27/11/2013, 8:54PM.

- [34] “Gas Sensors Market - An Overview”, 2007, Available on: <http://www.frost.com/prod/servlet/market-insight-top.pag?docid=104185353>, 27/11/2013, 8:57PM.
- [35] P.R. Warburton, M.P. Pagano, R. Hoover, M. Logman, and K. Crytzer, Yi.J. Warburton, Anal. Chem, “Amperometric Gas Sensor Response Times”, Anal. Chem.,70 (5), pp. 998 -1006, 1998.
- [36] D. Pletcher, J. Evans, P.R. Warburton, T.K. Gibbs, “Acidic Gas Sensors and Method of Using the Same”, US Patent 5,071,526, 1991.
- [37] General information for TGS sensors, Figaro Sensor. Available on: <http://www.figarosensor.com/products/general.pdf> , 27/11/2013, 9:07PM.
- [38] “Technical Note: Pellistor Gas Sensors and Poisoning”, Available on: <http://www.nemoto.eu/poisoning.pdf> , 27/11/2013, 9:08PM.
- [39] “Hazardous Gas Monitors, Chapter 5: Infrared Gas Sensors”, Available on: <http://www.intlsensor.com/pdf/infrared.pdf> , 27/11/2013, 9:10PM.
- [40] R.B. Sadeghian,. M. Kahrizi, “A low voltage gas ionazation sensor based on sparse gold nanorods”, Sensors and Actuators A: Physical, Volume 137, Issue 2, pp. 248–255, 2007.
- [41] F. Demami, L. Ni, R. Rogel, A. C. Salaun, L. Pichon, “Silicon nanowires synthesis for chemical sensor applications”, Procedia Engineering, Volume 5, pp. 351–354, 2010.
- [42] F. Demami, L. Ni, R. Rogel, A. C. Salaun, L. Pichon, “Silicon nanowires based resistors as gas sensors”, Sensors and Actuators B: Chemical, Volume 170, pp. 158–162, 2012.

- [43] J. Boor, N. Geyer, J. V Wittemann, U. Gosele and V. Schmidt “Sub-100 nm silicon nanowires by laser interference lithography and metal-assisted etching”, *Nanotechnology*, Volume 21 Number 9, 2010.
- [44] U. Gosele and V. Lehmann, in Z. C. Feng and R. Tsu (eds.), “Porous Silicon Quantum Sponge Structures: Formation Mechanism, Preparation Methods and Some Properties”, *Porous silicon*, World Scientific, Singapore, p.17, 1994.
- [45] Sailor Research Group, “Introduction to Porous Si”, 2003, Available on: http://sailorgroup.ucsd.edu/research/porous_Si_intro.html, 27/11/2013, 9:58PM.
- [46] L. Buckberry and S. Bayliss, “Porous Silicon as a Biomaterial”, *Materials World*. Vol. 7 no. 4, 1999.
- [47] E. X. Pérez, “Thesis on FABRICATION AND CHARACTERIZATION OF POROUS SILICON MULTILAYER OPTICAL DEVICES”, 2007, Available on: <http://www.scribd.com/doc/96943146/Thesis-Porous-Silicon-Perez> , 27/11/2013, 10:03PM.
- [48] K. Grigoras and V. Pačebutas, “Porous silicon fabrication technique for large area devices”, *IEEE*, Volume:67 Issue:6, pp. 2337 – 2338, 2009.
- [49] R. L. Smith and S. D. Collins, “Porous Silicon”, Available on: <http://www.ece.ucdavis.edu/misl/Web/Pages/Projects/poroussi.htm> , 27/11/2013, 10:17PM.
- [50] M. Esfahani Fard , A thesis on “effects of Fabrication Parameters on Porous Silicon Structure with some Potential Applications”, The department of Electronic and Electrical Engineering of Concordia University, August 2009.

[51] “RCA Clean”, School of Electrical and Computer Engineering of Georgia Tech, Available on: <http://www.ee.gatech.edu/research/labs/vc/processes/rcaClean.html>, 27/11/2013, 10:19PM.

[52] “Scanning Electron Microscope”, Purdue University, Available on: <http://www.purdue.edu/rem/rs/sem.htm> , 27/11/2013, 10:19PM.

[53] “Technical Notes; Energy Dispersive X-ray Micoanalysis An Introduction”, Available on: <https://static.thermoscientific.com/images/D17000~.pdf> , 27/11/2013, 10:21PM.

[54] “Handbook of Analytical Methods for Materials; ENERGY DISPERSIVE X-RAY SPECTROSCOPY”, Available on: <http://mee-inc.com/eds.html> , 27/11/2013, 10:21PM.