# A LABVIEW BASED POWER CONVERTER DESIGN FOR TIME DOMAIN ELECTROMAGNETIC SYSTEM

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Complies with the regulations of this University and meets the accepted standards with respect to originality and quality.

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# ABSTRACT

## A LabVIEW based Power Converter design for Time Domain Electromagnetic System

**Harjot Singh Saini**

In geophysical survey industry, helicopter time domain electromagnetic systems (HTEM) are used widely due to their better spatial resolution and ability to conduct surveys in difficult geographical areas. However, these systems are limited in terms of the exploration depths achieved due to the constraints on the overall weight of the system that a helicopter can safely tow. There is a scope to develop a compact yet high power system that is light in weight, fast in response and able to control high current pulses to achieve deeper exploration depths. In this thesis, a new LabVIEW based power converter is proposed and implemented to achieve *flexible and faster* control of the TEM system. The current control is implemented with hysteresis current control logic and a constant ON-Time current control logic. Proposed topology and current control helps to achieve the targeted fall-time (100 μs) at the end of current pulse. An optimized LabVIEW code and constant ON-Time current control scheme is implemented to achieve sampling times as low as 2 μs. The comparison of experimental results with MATLAB simulation results validates the effectiveness of the control scheme. To reduce the switching power loss in the converter, the same hard switching power converter, working with constant ON-Time current control is modified to simulate a zero current switching scheme by designing the required resonant elements.

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*Dedicated to my parents Sardar Mohinder Singh and Sardarni*

*Surinder Kaur*

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| | |
|---|---|
| TEM | Time Domain Electromagnetic |
| FEM | Frequency domain electromagnetic |
| AEM | Airborne Electromagnetic |
| HTEM | Helicopter Time domain Electromagnetic |
| Tx- coil | Transmitter coil |
| Rx- coil | Receiver coil |
| GPS | Global Positioning System |
| ZCS | Zero current switching |
| ZVS | Zero voltage switching |
| DC | Direct current |
| AC | Alternating current |
| IGBT | Insulated Gate Bipolar Transistor |
| NI | National Instruments |
| LabVIEW | Laboratory Virtual Instrument Engineering Workbench |
| FPGA | Field-Programmable Gate Array |
| VI | Virtual Instrument |
| AISC | Application-Specific Integrated Circuit |
| G- Programming | Graphical Programming |
| GUI | Graphical user interface |
| DMA | Direct memory access |
| FIFO | First in, first out |
| cRIO | CompactRIO |

# LIST OF PRINCIPAL SYMBOLS

| | |
|---|---|
| $i_{coil}$ | Tx- coil instantaneous current |
| $L_{coil}$ | Tx- coil inductance |
| $R_{coil}$ | Tx-coil resistance |
| $V_{dc}$ | DC link capacitor voltage |
| $C_{dc}$ | DC Link Capacitor rating |
| $I_{x1}$ | Tx-coil current at the beginning of Mode 2 |
| $I_{x2}$ | Tx-coil current at the beginning of Mode 3 |
| $\sigma$ | Neper frequency |
| $\omega$ | Damped natural frequency |
| M | Dipole Moment |
| N | Number of turns of Tx –coil |
| $P_{peak}$ | Power Source peak power |
| $V_{ps}$ | Output voltage rating of power source |
| $T_c$ | Capacitor Charging Time |
| $C_s$ | Snubber capacitance |
| $I_{band}$ | Hysteresis current band |
| $L_{stray}$ | DC loop stray inductance |
| $R_s$ | Snubber resistance |
| $P_{RS}$ | Snubber resistor power rating |
| $I_{ref}$ | Tx –coil reference current |
| $V_{pk}$ | Peak voltage allowed across switches |
| $f_{sw}$ | Switching frequency |
| $f'_{sw}$ | Effective switching frequency |
| $T_{sim}$ | Simulation time step |
| $T_{ctr}$ | Controller sampling time |
| $T_{ON}$ | Constant ON-Time for the switch |
| $L_r$ | Resonant Inductor |
| $C_r$ | Resonant Capacitor |
| $Z_r$ | Resonant Impedance |
| $\omega_r$ | Resonant angular frequency |

| | |
|---|---|
| $i_{Lr}$ | Instantaneous resonant inductor current |
| $v_{Cr}$ | Instantaneous resonant capacitor voltage |
| $I_{Lr,peak}$ | Resonant inductor peak current |
| $V_{Cr,peak}$ | Resonant capacitor peak current |

# CHAPTER 1. INTRODUCTION

## 1.1 AIRBORNE ELECTROMAGNETIC SYSTEMS

Airborne Electromagnetic (AEM) systems were built initially for the use in mining industry to explore new mineral land areas. However over the years, AEM systems find extensive use in natural resource management activities such as ground water salinity or water quality investigations. Also these survey techniques are used to explore new freshwater reserves in various countries. The ever increasing application of AEM systems has led to the need for better and efficient systems that are more powerful with deeper exploration depths and at the same time are lighter to carry by an aircraft or a helicopter. The available literature [1, 2] consolidates the journey of evolution of the Airborne Electromagnetic survey systems over the past 50-60 years.

AEM surveys are generally conducted by putting the equipment onboard an aircraft or a helicopter. Time domain electromagnetic (TEM) is the widely used technique in these survey applications [3]. Based on the architecture, the TEM systems are further divided into two categories - Fixed – Wing TEM system and Helicopter TEM system. Due to better spatial resolution and ability to conduct survey in severe terrains, helicopter based systems known as HTEM are preferred over their fixed wing aircraft counterparts. Fig. 1.1 shows a Fixed Wing TEM System and Fig. 1.2 shows a Helicopter TEM system.

Fig. 1.1 Fixed Wing TEM System[1]

Fig. 1.2 Helicopter Time Domain Electromagnetic (HTEM) system[2]

***Image Source:*** *1. Earth & Space Sciences Publication Highlights,*
*web link- http://ees.lanl.gov/images/Cap_Review/Earth%20Science%20Publications%20Highlights.pdf*

*2. The SkyTEM method for mapping groundwater resources,*
*web link - http://danishresponsibility.dk/skytem-method-mapping-groundwater-resources*

## 1.2 TEM SYSTEM AND PRINCIPLE

TEM system mainly consists of following three major subparts [1]:

- Power source (which can be a replaceable battery bank) and power converter with the current control loop
- Transmitter coil (Tx-coil)
- Receiver coil (Rx-coil) and the associated recording electronics.

The operating principles of a TEM can be described as follows. First, a sequence of high current pulse (square, triangular or cosine waveform) is made to flow through the Tx-coil at sub harmonic of the power line frequency (50 Hz/60 Hz). At the end of current pulse, current is abruptly turned OFF. This fast changing current results in the induction of eddy currents in the conductive bodies under earth's top layer which in turn results in a secondary magnetic field. This secondary magnetic field is sensed by the receiver coil and is recorded in the data recording system on board. A GPS signature is recorded to relate the recorded magnetic field data with actual map of the land area. Fig. 1.3 shows a graphical representation of the TEM principle.

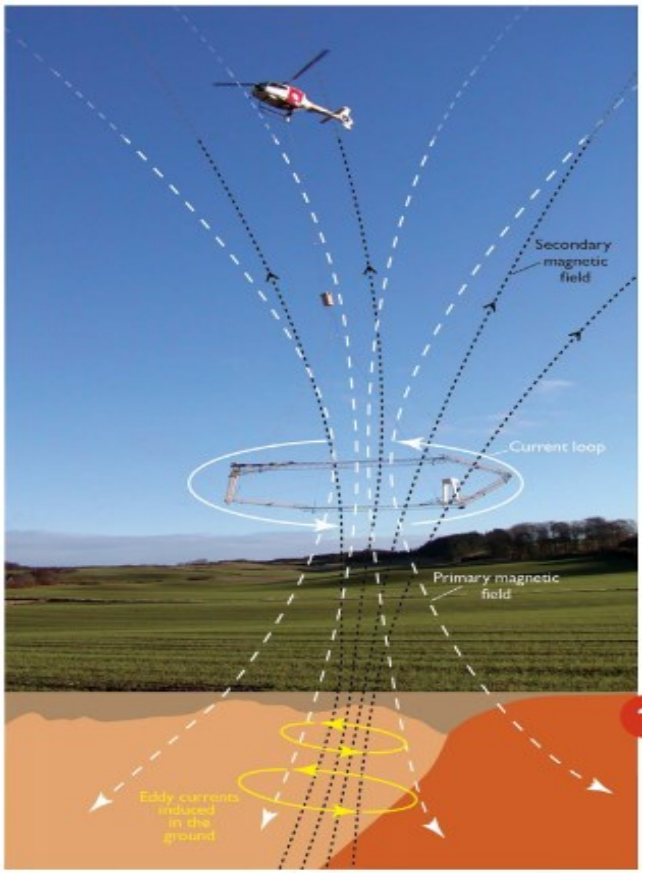



Fig. 1.3 TEM Principle [4]

Fig. 1.4 shows the ideal waveforms for Tx- coil current, voltage and secondary field response as recorded by the receiver in TEM systems [5]. It can be seen that the current through the transmitter coil goes from zero to the peak reference value by applying a high DC voltage. This peak reference current is maintained near its reference value by applying current control techniques. After predefined ON period, the current through the coil is made to fall sharply to zero. This sudden fall induces eddy current in the mineral target which in turn produces secondary magnetic field. The secondary field response, as sensed by the receiver is recorded once the OFF period starts. The secondary field due to conductive mineral is highest just after the coil current goes to zero and it decays

exponentially and goes to zero before start of the next pulse sequence. The reason for recording the response during OFF period is to avoid the effect of the primary field on the total field sensed by the receiver coil. In commercially available TEM systems, there are various types of the primary current waveforms implemented along with different settings for ON period (1 ms – 10 ms) and Fundamental Time period (10 Hz, 30 Hz etc.). However, no single system is reported, providing a complete flexibility to control or change system waveform or to alter the ON period or OFF period of the current waveform.

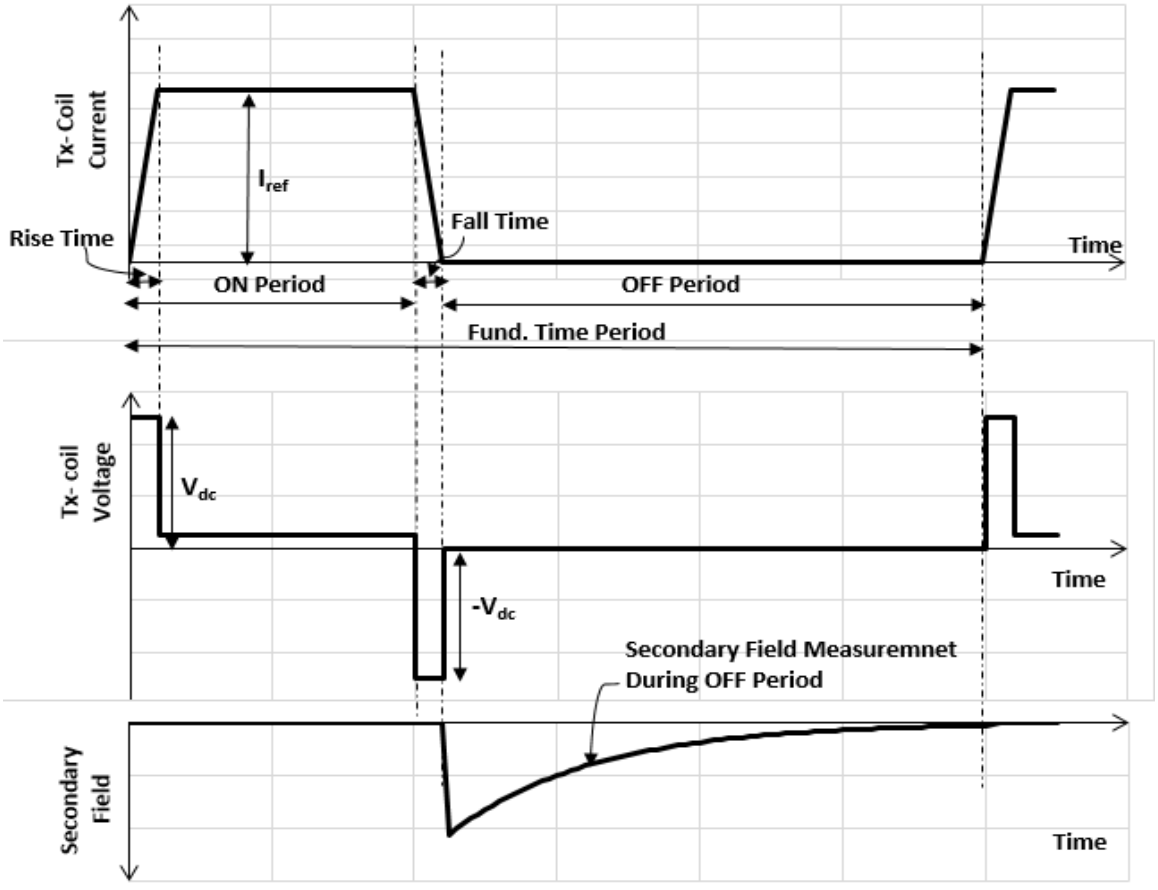



Fig. 1.4 TEM Waveforms

## 1.3 THESIS OBJECTIVE AND CHALLENGES

This thesis deals with the following objectives

- To design the power converter and control scheme to inject trapezoidal, unipolar current pulses into transmitter coil of the TEM system.
- Minimum current fall times (< 100 μs) for high reference current (200 A) shall be achieved to generate better secondary response from mineral targets.
- The converter control and data acquisition system shall be fast, providing a sampling time in the range of 2 μs – 4 μs to provide better data resolution and better current regulation.
- The overall weight and size of the system are limited by the helicopter towing capacity and hence the weight and size of the system shall be kept to minimum (< 200 kg).
- The power losses in the converter shall be minimized.

## 1.4 THESIS CONTRIBUTIONS

- Design of a power converter and associated control to establish high current trapezoidal pulses in the transmitter coil with current fall time less than 100 μs at high current (200 A) with resultant di/dt of 2000 kA/s.
- Maintaining a predefined constant current magnitude for the duration of predefined pulse width using constant ON-Time control.
- Implementation of LabVIEW based CompactRIO system to perform the data acquisition and current control at a fast sampling rate (500 kHz).

- Balancing the thermal stress in the IGBT switches by interchanging the gating signals in alternate cycles.
- Proposal of zero current switching technique to reduce the switching losses.

## 1.5 THESIS OUTLINE

The content of this thesis is organized into 5 Chapters.

Chapter 1 presents basic introduction to the AEM methods used in airborne survey systems along with brief explanation of the TEM system components and working principle.

Chapter 2 presents the review of the present power converter topologies used in airborne electromagnetic survey systems along with the advantages and shortcomings of these systems. A brief introduction is presented on the selection of the type of current waveform for the transmitter coil.

Chapter 3 presents the simulation analysis of proposed converter topology with hysteresis current control and constant ON-time control. Different modes of the converter and the associated equations, governing the current waveform are discussed. MATLAB simulation results are presented at low current and high current levels to simulate the converter operation. Design procedure are presented to select DC link capacitor, DC power source and RCD snubber components.

Chapter 4 presents the details about the implementation of the converter control scheme by introducing various subsystems of NI CompactRIO architecture. LabVIEW programming approach is presented for the proposed system in detail. Code optimization is discussed

to show the improvement steps followed during implementation stage to reduce the sampling time. A problem of switch turn OFF delay is discussed along with the solution, implemented using pull down resistors. The test results obtained from the system tests, carried out at low power (125V, 60 A) and high power (500V, 200 A) are presented to show the effectiveness of the designed system.

Chapter 5 presents the selection of the soft switching scheme to reduce the switching power loss in the converter. The operation of soft switching converter topology is discussed using state plane trajectory and design calculations are presented to select the resonant elements considering the design criteria. MATLAB simulation results are presented to verify the zero current switching design.

Chapter 6 summarizes the overall research conducted in this thesis and presents the final conclusions. Suggestions for future work on this topic are presented.

# CHAPTER 2. REVIEW OF POWER CONVERTER TOPOLOGIES IN AEM SYSTEMS

## 2.1 INTRODUCTION

The AEM applications need a particular attention to the power converter design, to control the excitation of current pulses in the transmitter coil (Tx-coil). Although AEM systems are used for geophysical surveys for a long time and there is great amount of work published and reported in the design optimization and configuration of transmitter coil (Tx-coil) and receiver coil (Rx-coil) but there is very limited work published and reported on the design of the power stage of these systems .However an attempt was made to collect presently available literature pertaining to design of power converters for TEM applications.

## 2.2 SELECTION OF CURRENT WAVEFORM

One of the starting point to design a TEM survey system is to select a current waveform that results in the maximum response from the mineral target. Different type of current waveforms (Triangular, Trapezoidal, Square, Cosine, Half – sine) are historically used in airborne TEM methods. The previous work by [6] investigates the effect of different transmitter coil waveforms on the system response recorded from the mineral deposit and concludes that for the current pulses of same amplitude and width, the maximum response is generated by a square current waveform. However due to the load time constant, a perfect square waveform cannot be achieved in reality. Therefore in this work the power stage is designed to provide a trapezoidal current pulse.

## 2.3 PRESENT CURRENT CONTROL TOPOLOGIES

In [7] a converter topology is proposed for TEM application. This paper discusses the requirements of a HTEM system in detail along with its working modes, analysis, control and performance. This topology is only tested for a laboratory scale model (Current = 30A, supply voltage =12V, fall time =200us). A leading edge modulation technique is presented for capacitor voltage control. Fig. 2.1 shows the converter topology used in [7] and Fig. 2.2 shows the experimental load current and the capacitor voltage waveforms.

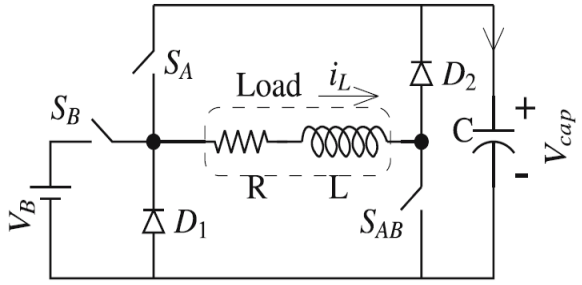



Fig. 2.1 TEM Converter Topology using two energy storage elements [7]

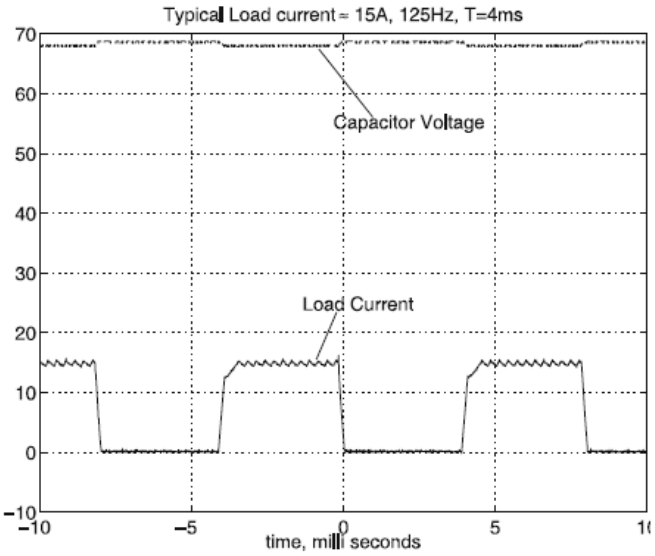



Fig. 2.2 Load Current and capacitor voltage waveforms [7]

**Advantages:**

1. Use of two energy storage elements reduces the current overshoot irrespective of the sampling rate of the control system.
2. Good capacitor voltage regulation at different load current values (low current).
3. The topology presents low power loss due to recycling of the coil energy at the end of pulse.

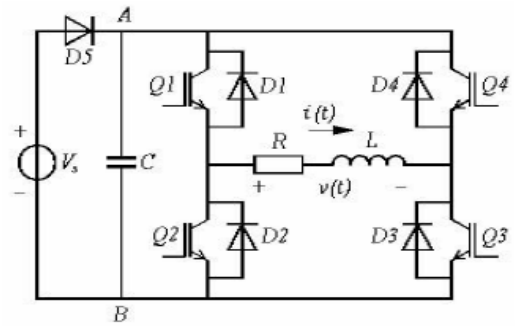
The information on the sampling rate of data acquisition and rate of the control system is not presented.

**Disadvantages:**

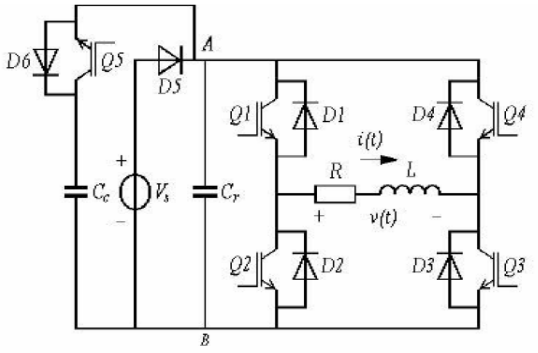
1. The voltage of the capacitor is regulated to a reference value through energy recovery from load to the capacitor during fall time. At high current levels the capacitor voltage cannot be regulated at the reference value due to losses in the circuit.
2. Absence of snubber circuits and implementation with hard switching technique risks system safety.
3. The performance at high current levels is highly uncertain with this topology.
4. Data is not presented on the use of any special technique for data acquisition and control and an important factor of sampling rate is not considered.

In [8], an inverter topology with clamped and unclamped circuit is presented for airborne surveying systems. The main feature of the proposed topology is the fast reversal of the

current through the transmitter coil. Fig. 2.3 shows the circuit layout of the unclamped and clamped converter topology used in airborne electromagnetic surveying system [8]




(a)




(b)

Fig. 2.3 Converter Topologies for fast current reversal (a) unclamped topology (b) clamped Topology [8]

Fig. 2.4 shows the load current and capacitor voltage waveforms for the unclamped converter topology. It can be observed that during the polarity reversal, a larger capacitor voltage is achieved due to resonance between the capacitor and load inductor.

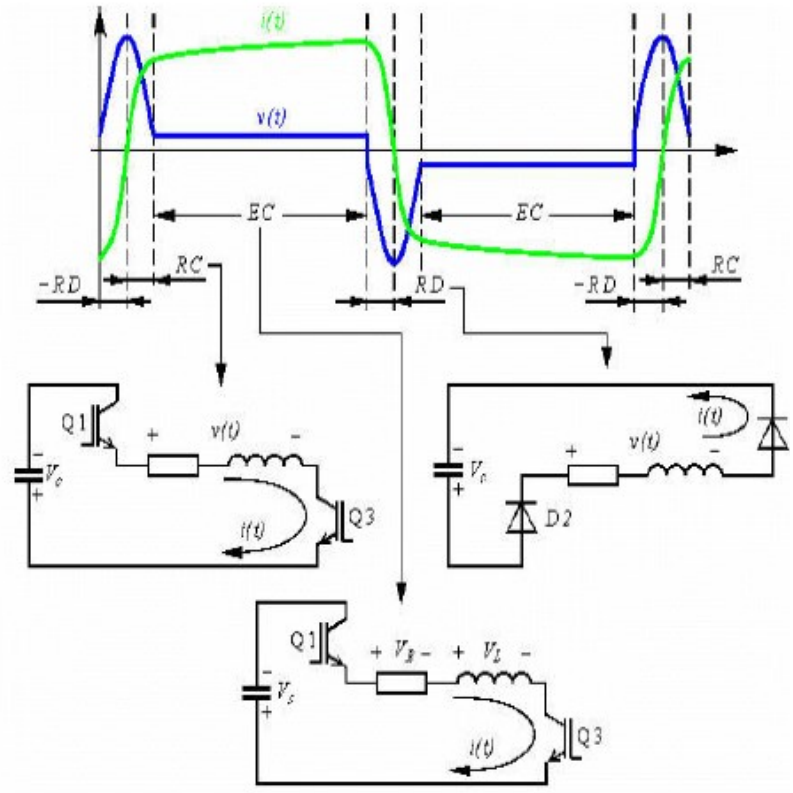



Fig. 2.4 Voltage and current waveforms- Unclamped Topology [8]

The advantages and disadvantage of the proposed system are as follows

**Advantages:**

1. The voltage used for current reversal can be made much larger than the source voltage due to resonance phenomenon. This means that a smaller voltage source can be used while achieving larger voltage magnitudes at current reversal.
2. A current reversal time of 200 µs was achieved.

**Disadvantages**:

1. An OFF period is preferred in between the subsequent current pulses because in this case the distortion produced by primary field is negligible on the recorded

secondary field. However in the present work there is no provision for the OFF period between the subsequent current pulses.

2. Clamped topology requires an additional capacitor and controlled switch that adds to the cost, weight and additional losses in the system.
3. Bad switch utilization, no snubber protection, no soft switching mechanism available.

## 2.4 CONCLUSION

Observing the work discussed in literature review it can be summarized that there is a scope to design a new system that comprise a power source, converter topology, transmission coil, receiver coil and data acquisition system that is efficient , utilizes less number of system components, provides better control and performance. With the improvement in semiconductor technology along with wider use of control and acquisition tools such as LabVIEW, a new high power yet lighter and efficient system is proposed. For implementation of the converter control scheme, a trapezoidal current waveform is selected as the desired current waveform.

# CHAPTER 3. THE PROPOSED POWER CONVERTER – DESIGN AND SIMULATIONS

## 3.1 INTRODUCTION

This chapter presents the detailed design and simulation analysis of the power circuit and the control scheme for controlling the current waveform in the transmitter coil. MATLAB Simulink is used to simulate the performance of the proposed converter and associated control before implementing the system. An attempt is made to provide the information on important starting points defining the scope or the final output. The power converter (Type – D chopper) topology modes are presented along with two current control strategies. First, the current control is achieved by implementing widely used hysteresis current control. However to limit the current overshoots caused by high di/dt and to implement soft switching techniques later in the project work it is very important to have a precise timing control over Turn - ON duration of the switch, which cannot be controlled precisely by hysteresis current control. To achieve better switch timing control, a novel constant ON-time control logic is developed and simulated in MATLAB Simulink and successfully implemented during implementation phase. In the end of this chapter concluding remarks are provided based on the simulation results.

## 3.2 IMPORTANT CONSIDERATIONS

The following points are considered at the start of the design procedure to define the targeted performance from the system.

- The transmitter coil is designed and optimized in different work. Already known resistance value (55 mΩ) and inductance value (200 μH) are used for simulation purposes.
- Although a bipolar (positive and negative) current pulse waveform is a preferred choice to cancel out the noise in the secondary field recorded by the receiver, unipolar current sequences are considered in this work due to design simplicity and cost effectiveness of the converter.
- To avoid interference with the power line frequency, the fundamental time period of the current waveform is selected as sub harmonic of the power line frequency (50 Hz/60 Hz) [9]. To implement unipolar current waveforms in this work, the fundamental time period is selected as 50 Hz/60 Hz. In next stage of development, system will be modified to generate bipolar current pulses at 25 Hz/30 Hz fundamental frequency.
- Ideally a square current waveform, to achieve maximum secondary field response from the mineral target would be used [10].However due to presence of high coil inductance, a trapezoidal pulse waveform with sharp rise and fall times is a practically feasible choice.
- The time for which the current is maintained near the peak reference value is referenced as pulse width and is fixed to 2 ms [11].
- As the final system implementation is based on CompactRIO Platform from NI hence the simulation time step and the controller time step (same as sampling

time) are selected considering the FPGA clock rate of 25 ns and analogue Input module rate of 500 KS/s/channel respectively.

- The final target for the fall time is fixed at 100 µs based on other available system studies [13].
- The ideal Simulink models are considered for the IGBTs, diodes and other passive elements.

## 3.3 PROPOSED CONVERTER TOPOLOGY

Fig. 3.1(a) shows the proposed converter topology. Here the transmitter coil is represented by a RL-load and is supplied by a high voltage capacitor. A DC source is used to charge the capacitor to a predefined voltage before the start of the pulse.

### 3.3.1 MODES OF OPERATION (HARD SWITCHING)

The proposed converter topology has 4 modes of operation which are shown in Fig. 3.1 (b) to 3.1 (f).

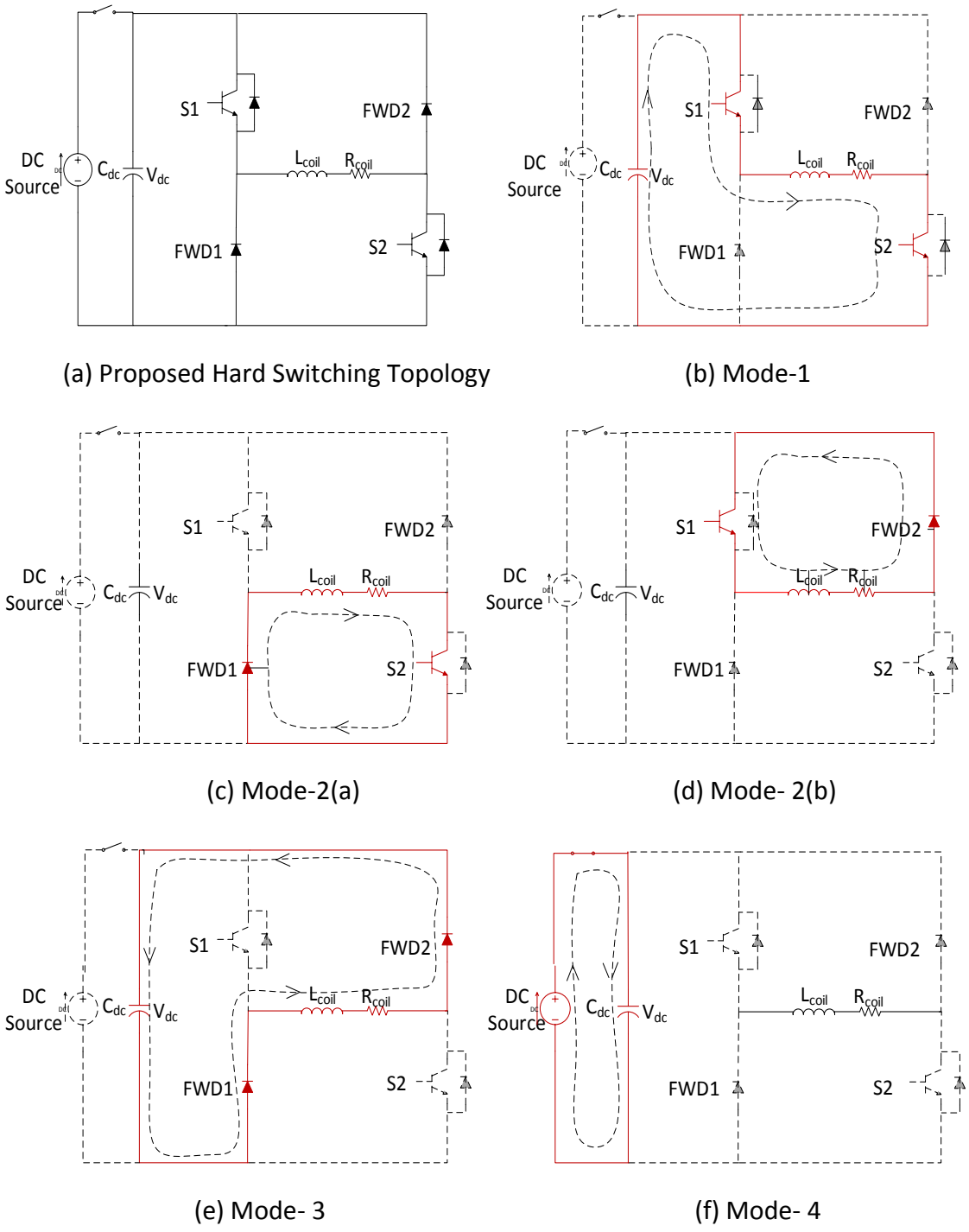
**Mode1:** The first mode in the cycle of operation starts with turning switches S1 and S2 ON as shown in Fig. 3.1(b). In this mode, full capacitor voltage is applied across the Tx-coil and the coil current ($i_{coil}$) increases. The diodes FWD1 and FWD2 remain OFF. The current through the coil rises from 0A to the upper limit set by the reference current.

**Mode2.** Mode 2 corresponds to a free-wheeling period and is initiated when one of the switches is turned off when the current reaches a reference current value set by current control. In this mode current start freewheeling through one of the switches and freewheeling diode. This mode can be implemented in two ways as shown by Fig. 3.1(c)

and Fig. 3.1(d). In first case, switch S2 is kept ON and switch S1 is commutated to maintain the current near the reference value for the required duration of pulse width. In second case, switch S1 is kept ON and switch S2 is commutated to achieve current control. Case 1 and case 2 are applied in alternate pulse cycles to share the switching losses and thermal stress among the two IGBTs.

**Mode 3:** Once the desired pulse width is reached, both the switches S1 and S2 are turned OFF (Fig. 2(e)). Due to inductive nature of the circuit, diode FWD1 and FWD2 are turned ON at this instant and a negative DC link voltage is applied across the coil. This results in sharp decay in current from reference value to zero. During this mode, part of the energy stored in the coil is fed back to the DC link capacitor. As the current reaches 0A, the diodes are naturally commutated to OFF state and this marks the end of Mode 3.

**Mode 4:** In the next mode, Mode 4 , the coil remains isolated form the DC link capacitor hence there is no transfer of energy from the capacitor to coil or vice versa. During this mode the response from the mineral deposit is sensed by the receiver coil and is recorded for post processing. Also at the end of Mode 3, due to energy losses in circuit elements the capacitor voltage is not fully recovered back to the initial value. Hence the power supply is enabled to bring the DC link capacitor voltage back to the reference value. The circuit for this condition is shown in Fig. 3.1 (f). The end of fundamental time cycle marks the end of Mode 4 and initiates next cycle of operation.




(a) Proposed Hard Switching Topology

(b) Mode-1

(c) Mode-2(a)

(d) Mode- 2(b)

(e) Mode- 3

(f) Mode- 4

Fig. 3.1 Proposed Topology & Modes of Operation (Hard Switching)

### 3.3.2 CURRENT GOVERNING EQUATIONS

Before starting the simulation of the proposed converter topology, it is important to model the governing equations and then design and select the system components based on the system requirements. First of all as shown in Mode-1 (Fig. 3.1 (b)), the switches S1 and S2 are closed and the circuit becomes a series RLC resonant circuit. The equations governing the series RLC resonance circuit defines the current flow through the load (Tx-coil). The series RLC resonance circuit can be designed to act as over damped, critically damped or underdamped state by selecting the value of circuit elements. However for a given capacitor voltage, the system developed for underdamped conditions will result in least current rise and fall times.

The current through the circuit in Mode-1 can be represented by following exponential rise equation [14] [15]

$$i_{coil} = \frac{V_{dc}}{\omega L_{coil}} e^{-\sigma t} \, sin(\omega t) \tag{3.1}$$

Where

$$\omega = \sqrt{\frac{1}{L_{coil} C_{dc}} - \left(\frac{R_{coil}}{2L_{coil}}\right)^2} \tag{3.2}$$

$$\sigma = \frac{R_{coil}}{2L_{coil}} \tag{3.3}$$

$i_{coil}$ = Instantaneous current through Tx- coil

$V_{dc}$ = DC link capacitor voltage

$L_{coil}$= Tx-coil inductance = 200 µH

$R_{coil}$ = Tx-coil resistance = 55 mΩ

$C_{dc}$ = DC link capacitor rating

During Mode-2, the coil current freewheels and the zero voltage is applied across the coil, the stored energy is dissipated mainly in the coil resistance. However the resistance of the IGBT switches and the diodes also contribute to some energy loss but for this equation modeling, the small contribution of these factors is not comparable and hence neglected. The current in the Tx-coil during Mode2 is given by following equation [16]

$$i_{coil} = I_{x1}\, e^{-\sigma' t} \tag{3.4}$$

Where $I_{x1}$= Tx- coil current at the beginning of Mode 2

And

$$\sigma' = \frac{R_{coil}}{L_{coil}} \tag{3.5}$$

Similarly, in Mode-3, when both the switches are turned OFF and the diodes FWD1 and FWD2 conducts , the stored energy of the coil is fed back to the DC link capacitor and coil current decays from its peak value to zero.

The current in this phase is governed by following equation [16]

$$i_{coil} = I_{x2} e^{-\sigma t} \left( (\cos(\omega t) - \frac{\sigma}{\omega} \sin(\omega t) \right) \tag{3.6}$$

Where $I_{x2}$ = Tx-coil current at the beginning of Mode 3.

During Mode 4, the coil remains isolated from the power source and the DC link capacitor. Hence no current flows through the Tx-coil for this period until the two switches are turned ON at the start of next current cycle.

### 3.3.3 SELECTION OF DC LINK CAPACITOR

The Tx- coil fabricated for this work is a circular coil (stranded copper cable) with 4 turns and diameter of 5m (Area = 19.6 $m^2$). The dipole moment is fixed to 15000 N-$m^2$ after studying the present TEM systems [2]

So the required current can be calculated as

$$\text{Dipole moment, } M = N * I_{ref} * A \quad (3.7)$$

Where N = No. of turns of Tx-coil

$I_{ref}$ = Reference Tx- coil current

A = Area of Tx- coil

By using equation 3.7, the peak DC current is fixed at 200 A.

For driving this current to the coil, the DC link capacitor voltage is fixed to 500 V.

From equation (3.2), ω can be represented in terms of $C_{dc}$.

From equation (3.5) σ = 137.5 Nepers/s

Putting t= 100 µs, $I_{x2}$= 200 A, $I_{coil}$ = 0 and solving for $C_{dc}$, the required value of $C_{dc}$ is calculated and the closest standard capacitor rating selected is 1000 µF.

The capacitor voltage rating is selected considering the future implementations with higher current ratings.

The final capacitor ratings selected is, voltage rating =1500 VDC, Capacitance =1000 µF.

### 3.3.4 SELECTION OF DC POWER SOURCE

The next step is to select the DC power source that can efficiently charge the capacitor in available time, in-between the current pulses. One of the important point is to select a DC power supply with the provision of remote control i.e. to have a flexibility to control the output voltage of the DC power supply through a user interface. The other important factors to be considered are the output voltage rating and the output current. For this purpose, high power capacitor charging power supplies from TDK Lambda Americas Inc. are found suitable. The equations given in application note [17] are used to select the power source rating for a given charging time of the capacitor.

As per the application note [17], the peak power required from the power source is given by the following equation

$$P_{peak} = \frac{0.5 * C_{dc} * V_{ps} * V_{dc}}{T_c} \quad (3.8)$$

Where $C_{dc}$ = DC link capacitor rating

$V_{ps}$ = Output voltage rating of power source

$V_{dc}$ = DC link Capacitor voltage

$T_c$ = Capacitor Charging Time

As pulse width and fundamental time period for the current pulse is fixed to 2ms and 16.67ms respectively. Therefore the capacitor charging time cannot be more than 16.67ms, if the power supply is always kept connected to the DC capacitor. However it's preferred to connect the power supply only during current OFF period as the power

supply can provide limited amount of current and if it is kept connected to the load all the time the overload protection may cause inhibit action. Effectively maximum value for Tc can be considered equal to 14 ms. Here, $V_{dc}$ is the difference in the voltage that power supply has to provide in between the current pulses. From the simulation results of next section it can be seen that the drop in the voltage for 500V, 200A operation is around 15V but a part of it is recovered by the energy recovery from the coil. Hence to calculate the power rating of the power supply, $V_{dc}$ can be considered around 12V. Using the earlier calculated capacitance of DC link capacitor along with $V_{dc}$=12 V, and $T_c$ = 14 ms, in equation (3.8), a value of peak power was calculated for the power source. The power supply finalized was 1KW, 3KV (102-3kV-POS-5V-LP) from TDK Lambda. A 15 pin D-type female connector located on the power source provides the access to connect the remote interface cable from manual control interface to the power source.

### 3.3.5 SELECTION OF IGBTS

As in all converter applications to select the IGBT switches, the important aspect is to calculate or fix the current and voltage specifications as per the application needs. However in this application additional constraints are put by weight and size of the power converter and hence attention is given to choose the modular, light yet powerful switch modules. Although there are various IGBT product families available from manufacturers such as Infineon, Powerex and On Semiconductors, but for this application, Semix IGBT modules from Semikron are selected due to their modular and compact design, Cost effectiveness and superior performance at high power levels.

The other advantages of Semix modules are [18]

- Single housing contains the IGBT and free-wheeling diode, and needs only one switch assembly for each converter leg resulting in compact size and lower cost of the converter.
- The modular design of Semix IGBT modules result in low – inductance design as the DC link connections can be short, resulting in reduced voltage overshoot.
- Due to directly mounted driver board optimum gate drive performance can be achieved (with minimum noise)
- The reduced solder joints or the connections result in better system reliability.

Considering the future scope of testing at higher power levels, 1200V, 600A IGBT modules are selected. These modules can handle switching frequencies up to 10 KHz with 100% duty cycle. More details on implementation of these IGBT modules is provided in Chapter 4.

### 3.3.6 SIMULATION RESULTS

The simulation analysis was conducted using MATLAB Simulink. Table 3-1 shows the major parameter values considered for the simulation with hysteresis current control

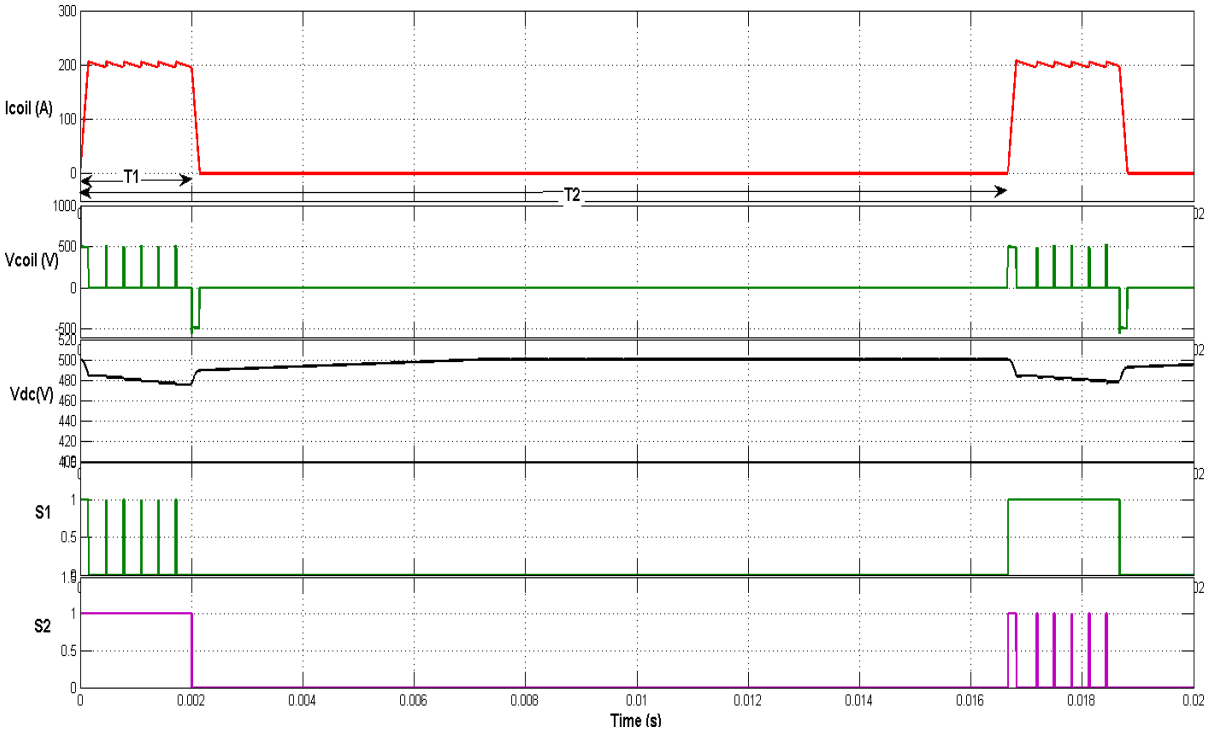
Table 3-1 Simulation Parameters

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Reference Tx- coil current | $I_{ref}$ | 200 | A |
| Initial DC link capacitor voltage | $V_{dc}$ | 500 | V |
| DC Link capacitor rating | $C_{dc}$ | 1000 | µF |
| DC power source peak charging rate | $P_{peak}$ | 1100 | J/s |
| DC power source output voltage rating | $V_{rated}$ | 3 | KV |
| Tx-coil inductance | $L_{coil}$ | 200 | µH |
| Bus bar stray inductance | $L_{stray}$ | 200 | nH |
| Current pulse width | $T_1$ | 2 | ms |
| Fundamental time period | $T_2$ | 16.67 | ms |
| Simulation time step | $T_{sim}$ | 25 | ns |
| Controller sampling time | $T_{ctr}$ | 2 | µs |
| Hysteresis band | $I_{band}$ | ±5 | A |

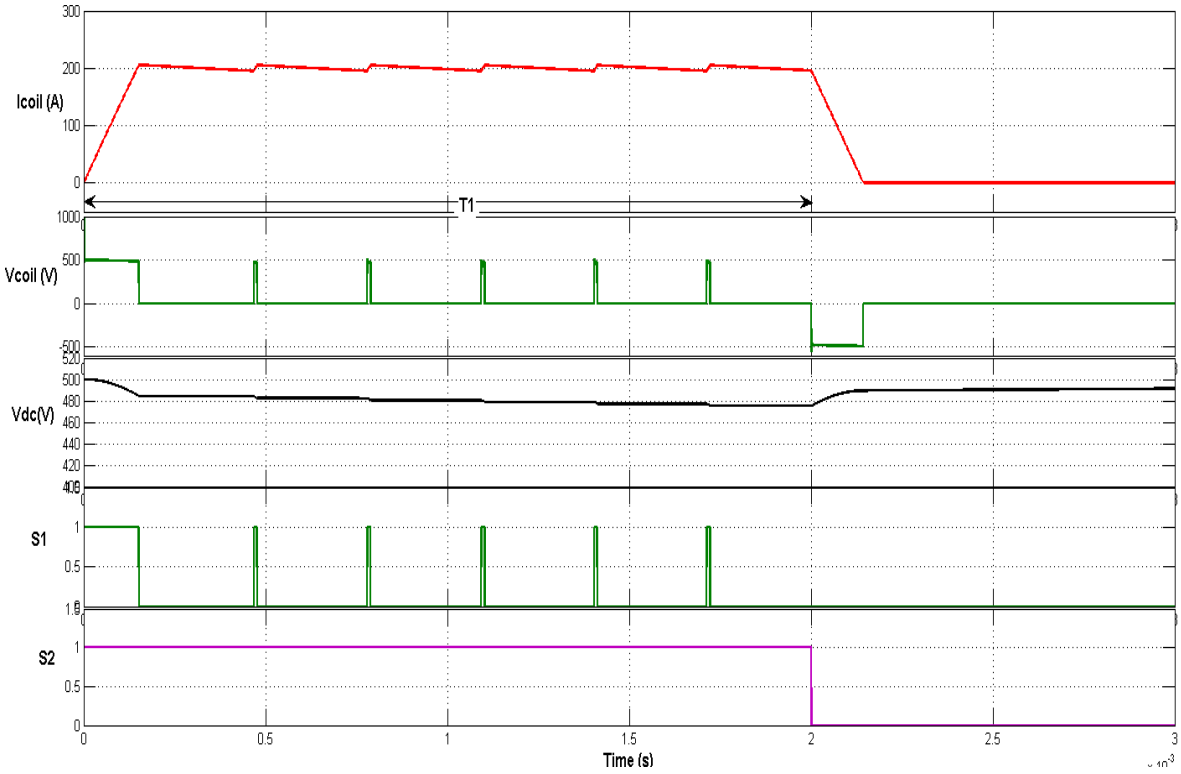
Fig. 3.2 shows the simulated waveforms for the proposed topology with hysteresis current control. Fig. 3.2(a) shows the coil current, coil voltage, DC link capacitor voltage and gating signals for switches S1 and S2. It can be seen that the pulse ON period (T1) is kept to 2ms and fundamental time period of the pulse (T2) is around 16.67ms (for f = 60 Hz). At the beginning of the pulse current rises almost linearly to the preset load value and at the end of pulse ON period current drops sharply to zero. As discussed earlier this sharp decrease in current is important to get an improved field response from the mineral

deposit. Also it is clear from Fig. 3.2(a) that during 1st cycle, switch S2 is kept closed for the duration T1 and Switch S2 commutates to implement hysteresis control. For 2nd cycle, switch S1 is kept closed for the duration T1 and switch S2 commutates.

It is important to note that the DC link capacitor voltage, $V_{dc}$ is depreciated from its initial value of 500V to 480 V at the end of first pulse. However due to energy recovery from the Tx-coil to the DC capacitor, the voltage is recovered from 480V to around 490 V. Hence almost half of the voltage drop has been recovered back due to energy recovery. The remaining 10V charging can be achieved by enabling the DC power source. It is clear that the DC capacitor is charged back to 500V in 5ms which is quite less than the available zero current period of 14.67ms. Fig. 3.2(b) shows the waveforms with changed resolution to observe the waveforms during the pulse width.




(a)




(b)

Fig. 3.2 Simulation waveforms with hysteresis current control

(a) Two pulse cycles (b) One pulse cycle *(Simulation parameters shown in Table-3-1)*

## 3.4 CONSTANT ON - TIME CURRENT CONTROL SCHEME

As discussed in earlier sections one of the important requirements of the TEM system is to inject a trapezoidal current pulse through the Tx-coil. The current can be maintained near the reference value by applying widely used digital hysteresis current control. A digital hysteresis current control was implemented using standard *Relay* function of LabVIEW and alternatively by using S-R flip-flop logic. However in each case the minimum achievable sampling time was 6 µs. This leads to current overshoot beyond the values set by control input (a common problem associated with hysteresis current control) [19]. Also high sampling times will result in low data resolution of the secondary field survey data

as same system is to be used for recording the secondary field response. The high sampling time is contributed to the more processing power utilized by the control code implementation using flip-flops and Relay function. This condition is also not favorable to design a soft switching scheme for the converter, as the ON- time or OFF time cannot be controlled effectively by employing hysteresis current control.

To avoid these problems, a time based control strategy is needed where the switch is allowed to stay ON for a predefined time interval. To achieve this, a novel control strategy referred as Constant ON time control was conceptualized and implemented.

The main attributes of this new technique are

- Results in a better control where the ON- Time for the IGBT switch is directly controlled by passing a numerical control on the host screen.
- Constant ON- Time logic can be implemented in the LabVIEW using case structure architecture which uses less processing power of the controller and is fast to execute as compared to sequential logic control (Hysteresis control using relay VI or SR flip Flops).

A MATLAB Simulink standard function block was used to write a function to perform this control logic. Fig. 3.3 shows the flow chart explaining the logic of constant ON-time current control scheme.

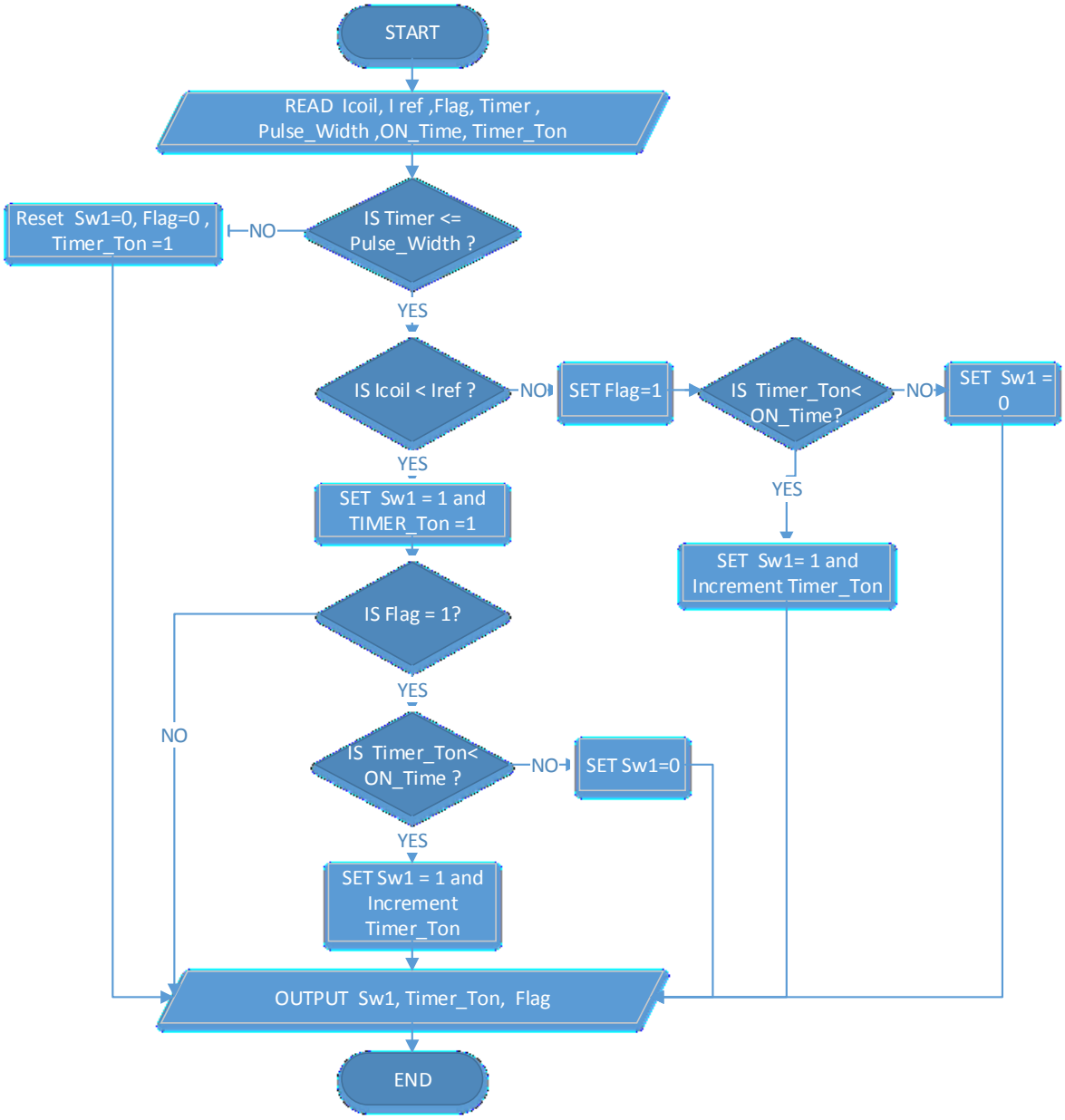



Fig. 3.3 Flow Chart for Constant ON Time Current Control

Following is brief description of the variables used in the flow chart.

“ON _Time” is the variable that stores the fixed number of count corresponding to the pre - defined ON Time.

“Timer_Ton” is the variable that stores the iteration count while the switch is ON.

“Timer” is the counter that counts the number of iterations for the fundamental time period.

“Pulse_Width” represents the fixed time for which the square current waveform is present.

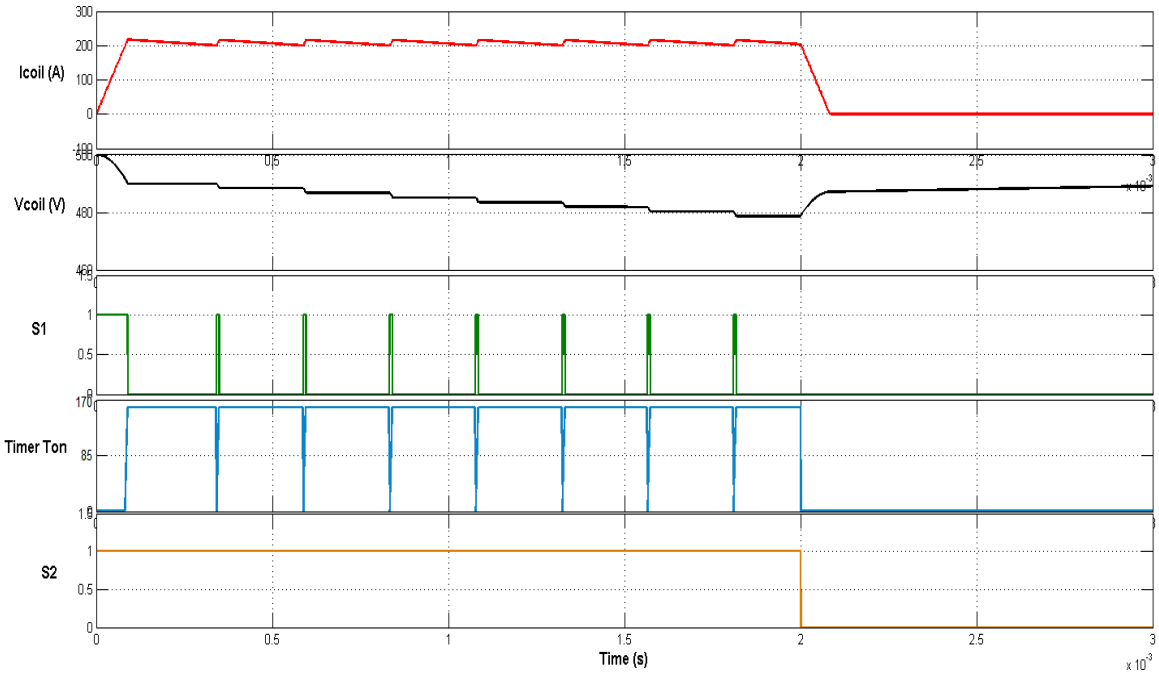
“Flag” is used as a memory element to store the information when the coil current exceeds the reference current first time. It is activated whenever the coil current crosses the value of reference peak current first time. Variable “Flag” is reset when the end of the desired current pulse is reached.

The operation of the TEM with the constant ON-time current control scheme was simulated in MATLAB Simulink. At the start, the parameters such as coil current, reference peak current, pulse width, flag status and timer values are read from the MATLAB workspace and are passed to the function block containing the constant ON-Time program logic. In the initial phase, when the coil current is less than the reference current, the switch stays ON.

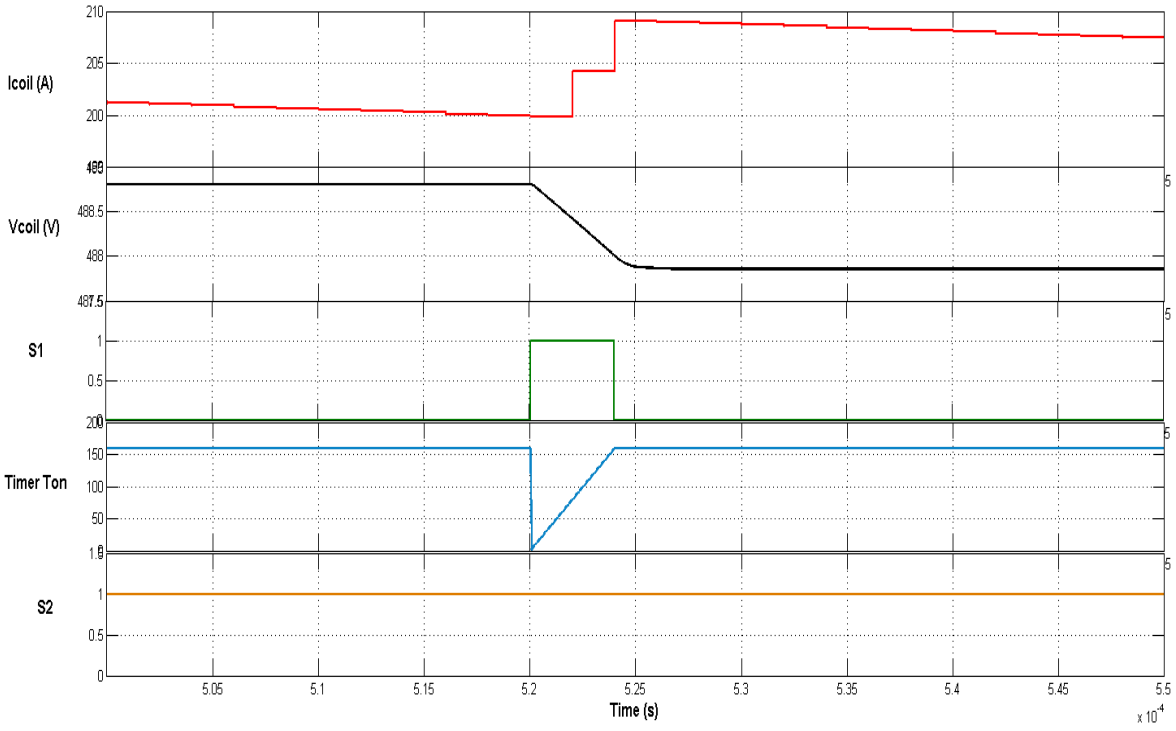
After the initial rise of the current, whenever coil current crosses the reference peak current, “Timer _Ton” is incremented and is compared with “ON_Time” for each loop iteration. Switch S1 remains ON until “Timer_Ton” is less than “ON_Time”, resulting in current rise and “Timer_Ton” keep on updating. Switch S1 is turned-OFF when “Timer_Ton” becomes equal to “ON_Time”, resulting in freewheeling of coil current through freewheeling diode and Switch S2. The coil current is decayed slowly and when it reaches a value less than reference peak current the “Timer_Ton” is reset, Switch S1 is

turned - ON again and value of “Timer_Ton” is incremented in subsequent Iterations for the defined duration of “ON_Time”.

To balance the thermal stress of the IGBT modules, the alternate switch operation (used with hysteresis current control) is retained in constant ON – Time control technique. Fig. 3.4 (a) shows the overall waveforms for one pulse width period. The coil current and DC capacitor voltage waveforms are similar to the one achieved with hysteresis current control. From Fig. 3.4 (b), it can be observed that as soon as the coil current falls below the reference current, the value of “Timer_Ton” start increasing and Switch S1 is turned ON resulting in increase in coil current. After a time of 4 µs the value of “Timer_Ton” becomes equal to 160 (i.e. 4 µs/ 25 ns) and the switch S1 is turned-OFF, and “Timer_Ton” keeps its value until the coil current falls below reference current. The converter was simulated with different values of ON_Time and corresponding effect was observed in the simulation results.




(a)




(b)

Fig. 3.4 Simulation waveforms with Constant ON –Time

(a) One Pulse Period (b) One switching commutation

(Simulation Parameters – $V_{dc}$ = 500V $I_{ref}$ =200A, $T_{sim}$ = 25ns, $T_{ctr}$=2µs, ON_Time = 4µs)

## 3.5 DESIGN OF SNUBBER CIRCUIT

During the discussion of operating modes of the converter in section 3.3.1 the stray inductance due to DC bus was neglected. However in practice, there is always a DC loop stray inductance associated with the DC bus and whenever the IGBT switch is turned OFF, the trapped energy in the stray inductance results in voltage overshoot. In high power applications similar to the case under consideration, this voltage overshoot can reach to a magnitude that can possibly damage the switch and other circuitry. One of the ways to keep the stray inductance to minimum is to keep the DC link conductor lengths to minimum and to carefully design the DC link conductors with minimum overlap lengths.

But these design considerations can't completely eliminate the stray inductance and hence a solution is required to suppress the voltage overshoot at the IGBT terminals. To protect the circuit elements from switching transients the solution proposed in literature [20] [21] is to use a snubber circuit.

### 3.5.1 ADVANTAGES OF RCD SNUBBER

There are various type of snubber circuits that can be used in different applications and their advantages and disadvantages are discussed in detail in [20]. For this application, RCD snubber is used due to following advantages:

1. Suitable for medium and high power applications
2. Suitable for high frequency operation.
3. Can be implemented by using direct mount snubber modules with minimum circuit length and hence minimum parasitic and stray inductance.

4. The snubber diode prevents any oscillations between snubber capacitor and DC capacitor. These oscillations are otherwise present in the case of Decoupling Capacitor.[21]

   The circuit diagram with RCD snubber is shown in Fig.3.5

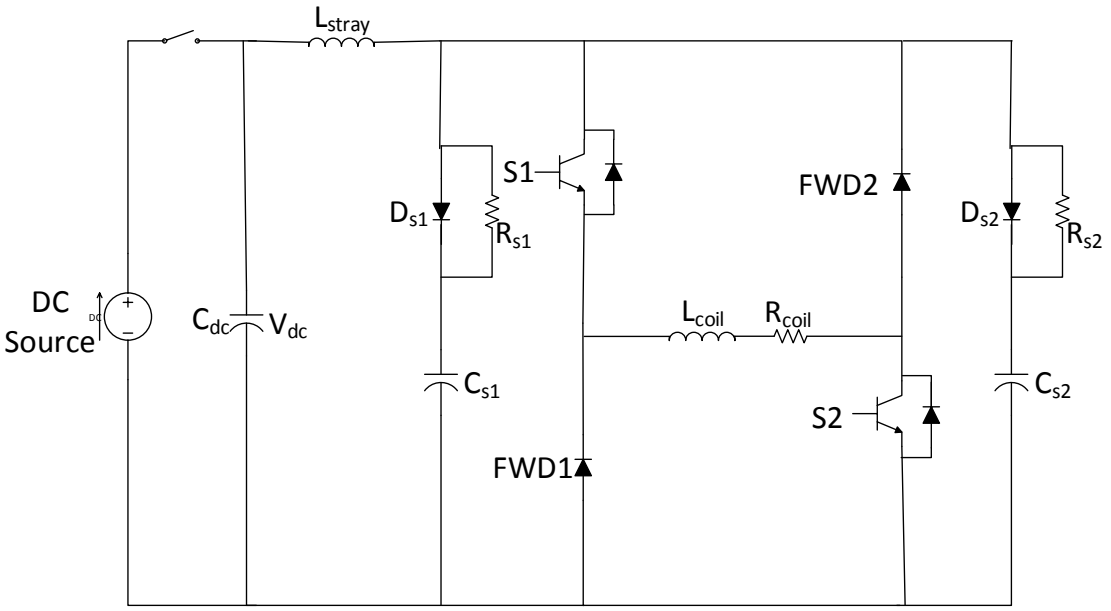



Fig. 3.5 Converter circuit with RCD snubber

### 3.5.2 CALCULATION OF SNUBBER CAPACITANCE

The snubber capacitor is given by the following formula [20]

$$C_s = \frac{L_{stray} {I_0}^2}{(V_{pk} - V_{dc})^2} \quad (3.9)$$

Here $L_{stray}$= DC loop stray inductance =200 nH

$I_0$ =Maximum coil current to be supplied = 200 A

$V_{pk}$= Peak voltage allowed =650 V

$V_{dc}$= DC bus voltage =500 V

Putting these values in equation (3.9)

Cs = 0.35μF

A near standard capacitor rating available is 0.47 μF and the voltage rating of the capacitor selected is 1200 V

### 3.5.3 CALCULATION OF SNUBBER RESISTOR

The snubber resistor can be calculated by formula [21]

$$R_s = \frac{1}{6\, C_s f_{sw}} \tag{3.10}$$

Where $C_s$ = snubber capacitor (calculated above)

$f_{sw}$= switching frequency of Switch S1

Here the switch S1 is commutating for a period of 2 ms and then remains in OFF state till the end of fundamental time period. For a pulse ON period of 2ms and fundamental time period of 16.67ms the switch S1 behavior during switching is observed in the MATLAB simulation. It is seen that for a load current of 200A , DC capacitor voltage 500V and ON-Time of 4 μs, the switching period of switch S1 is 200 μs giving a switching frequency, $f_{sw}$= 5000 Hz. Using this value in equation (3.10) snubber resistor value of 71 ohm is calculated.

Power rating of the snubber resistor is given by

$$P_{Rs} = 0.5 C_s ({V_{pk}}^2 - {V_{dc}}^2) {f'}_{sw} \tag{3.11}$$

Here the effective frequency $\mathrm{f'}_{sw} = \mathrm{f}_{sw} * \frac{T_1}{T_2}$ (3.12)

Where T1 = Pulse ON Time = 2ms

And T2 = Fundamental Time Period = 16.67ms

Hence from equation (3.12), $f'_{sw}$ = 588 Hz

Substituting these values in equation (3.11) yield

$$P_{Rs} = 61 \text{ W}$$

A standard resistor with ratings 75ohm, 100W (non- inductive design) with product no. "MP9100-75.0F-ND" from Caddock Electronics Inc. was selected.

While implementing the snubber design, it is always advantageous to keep the parasitic inductance of the snubber circuit layout to minimum. With individual element R, C and diode there will be unavoidable inductance associated with the circuit layout. To effectively implement the snubber design, the direct mount IGBT capacitor module "SCM474K122H8N24-F" from Cornell Dubillier was used .The direct mounting results in minimum parasitic inductance resulting in a better snubber implementation. It is a direct mount module containing snubber capacitor and snubber diode in a single housing and having an external connection to install the snubber resistor. The module's DC voltage rating is 1200V.

## 3.6 CONCLUSION

In this chapter, based on predefined scope the operating modes are discussed for the class -D converter along with the equations defining the current waveform during these modes. A detailed design approach is described to select the system components. MATLAB Simulink analysis is presented to evaluate the performance of the power

converter. A constant ON –time control technique is explained to achieve better timing control. In the end, to protect the IGBT and the converter circuitry from switching voltage overshoots, a RCD snubber design is presented. The verification of the snubber design cannot be performed in MATLAB simulation due to ideal component behavior. However the effect of snubber circuit is evaluated in experimental tests presented in Chapter 4.

# CHAPTER 4. HARDWARE IMPLEMENTATION AND EXPERIMENTAL RESULTS

## 4.1 INTRODUCTION

This chapter presents the implementation of the proposed converter scheme along with the associated digital control and data acquisition hardware. The LabVIEW programming logic implemented to control the current waveform is presented in detail. The experiment results are presented to display the performance of the entire system at different development stages. An attempt is made to describe the process of LabVIEW code optimization to achieve least possible sampling rates as per the installed hardware capabilities. A problem of switch turn OFF delay was observed and a solution was implemented using pull down resistances. In the end the conclusions are stated.

**NOTE:** The experimental setup was developed and tested at Laval facility of Geo Data Solutions GDS Inc. Canada.

## 4.2 INTRODUCTION TO LABVIEW

LabVIEW (Laboratory Virtual Instrumentation Engineering Workbench) is a graphical programming environment that, with help from logic blocks and other components, makes it possible to test, simulate and control flowchart-type model [23]. It is easily integrated with hardware devices such as the FPGA. Mostly the block diagram (where the logic circuit is drawn) and the front panel (the input/output data and the programmatic interface) is used when dealing with this program. Except the fact that a graphical

programming language is more user-friendly, the LabVIEW software has benefits considering the following two big differences from other programming languages:

- Graphical programming is realized with help from graphical icons, combined in a diagram and is then directly compiled to machine code, so that the processor can understand and execute the orders created in the diagram.
- Data flow is transmitted in form of data (not lines of text). This makes it easier to control different executions done separately and consecutively

## 4.3 INTRODUCTION TO FPGA

Field-programmable gate arrays (FPGAs) are reprogrammable silicon chips. In contrast to processors in a PC, programming an FPGA rewires the chip itself to implement the functionality rather than run a software application.

**Benefits of Using FPGAs:**

- Faster I/O response times and specialized functionality
- Exceeding the computing power of digital signal processors
- Implementing custom functionality with the reliability of dedicated deterministic hardware
- Rapid prototyping and verification without the fabrication process of custom ASIC design
- Field-upgradable eliminating the expense of custom ASIC re-design and maintenance

## 4.4 COMPACTRIO SYSTEM ARCHITECTURE

To implement the digital control of the proposed converter and to acquire the current and voltage signals, National Instrument's CompctRIO platform was selected.

CompactRIO is a reconfigurable embedded control and acquisition system and is vastly used in modern control applications. The CompactRIO system's hardware architecture includes I/O modules, a reconfigurable FPGA chassis, and an embedded real time controller [24]. CompactRIO is programmed with NI LabVIEW graphical programming tools also known as G- Programming.

Due to faster control and data acquisition possible with embedded controller and the modular design approach and the option to expand the cRIO architecture at any time by adding additional input output modules with the same platform, CompactRIO was selected to perform the control and acquisition tasks for this application.

The standard CompactRIO system selected for this application consists of following sub parts [24]:

### 4.4.1 REAL TIME CONTROLLER (NI CRIO 9014):

It's an embedded controller that runs the application code in the FPGA target and interfaces FPGA target with C series I/O modules. It has 400 MHz processor, 2GB non volatile storage and 128 MB DRAM. It supports RS 232 serial port for connection to the peripherals. Alternatively an Ethernet port is used in this application for communication between the real time controller and the host Computer. Also a USB slot can be used to attach an external memory.


Fig. 4.1 NI cRIO-9014 RT controller

### 4.4.2 RECONFIGURABLE FPGA CHASSIS (NI CRIO 9111 -4 SLOT)

A four slot reconfigurable chassis is used to provide rugged modular housing to the Real time controller and the C –series I/O modules. A backplane in the chassis contains the FPGA target, and system's data, timing and triggering buses. The FPGA chassis with internal clock frequency of 40MHz is used in this application. In other words, FPGA internal clock runs at a time step of 25ns that correspond to the FPGA tick rate and is used as a unit to check the execution speed of the FPGA code. The application code is written on the host computer and is compiled and downloaded to the reconfigurable FPGA target. Xilinx Virtex-5 LX30 is the type of FPGA used in this chassis. The chassis comes with Din-Rail Mounting or Panel Mounting options. In this application Din-Rail Mounting is selected due to ease of mounting.

Fig. 4.2 NI cRIO-9111 four –slot, reconfigurable embedded chassis

### 4.4.3 ANALOG INPUT MODULE (NI 9222)

To acquire the Tx- coil current and DC capacitor voltage signals, a C- series 4- channel, 16 bit simultaneous analogue input module is selected. It has a sampling rate of 500 KS/s/ch which translates to a sampling time of 2us per channel. The input voltage range for this module is ± 10V and comes with screw terminal connectivity.

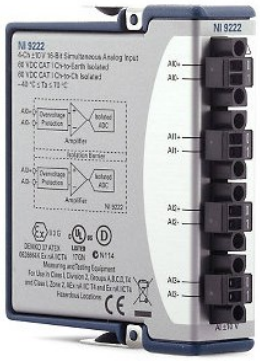



Fig. 4.3 NI-9222 Analogue Input Module (4- Channel)

### 4.4.4 DIGITAL OUTPUT MODULE (NI 9474)

After acquiring the data from input channels the program code is executed in the FPGA target and the output signals are generated for the IGBT switches and the Power Supply Control. A C series, 8 channel, 1 us high speed digital output module is used for this purpose. It has an output voltage range of 5 -30V.


Fig. 4.4 NI-9474 Digital Output Module (8- Channel)

### 4.4.5 CONTROLLER POWER SUPPLY (NI PS –15 POWER SUPPLY)

The function of this power supply is to power the CompactRIO controller and associated hardware devices. The nominal input of this power supply is 115/230V AC and the output is regulated 24VDC at 5A.

Fig. 4.5 NI PS-15 Power Supply

Fig. 4.6 shows the example of CompactRIO system assembly

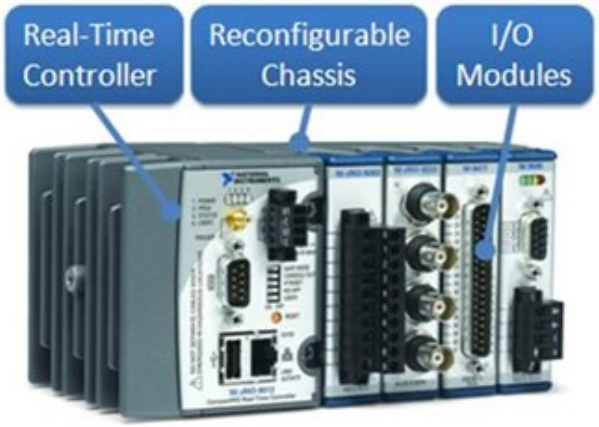



Fig. 4.6 CompactRIO System

### 4.4.6 COMPACTRIO SYSTEM BLOCK DIAGRAM

Fig. 4.7 shows the overall block diagram of the entire system. The arrows shows the direction of data communication between various components of the system.

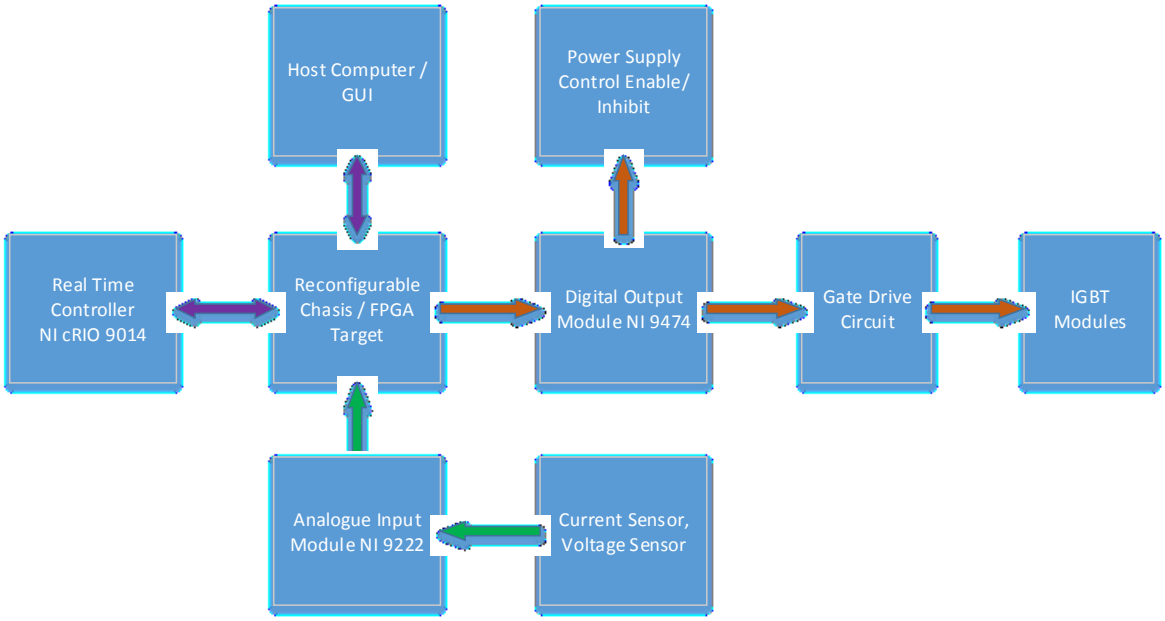



Fig. 4.7 System Block Diagram

Fig. 4.8 shows the circuit diagram for the experimental setup, the RCD snubbers are omitted in this representation for better visualization of circuit components. As shown in

Fig. 4.8, NI 9222 input module is connected to two sensors i.e. current sensor sensing the Tx-coil current and voltage sensor sensing the DC capacitor voltage the same module can be used to connect the input from the Rx-coil sensing the EM response from the target. This input data is passed to the cRIO 9014 digital controller which is connected to the host computer for two way data communication. CRIO9014 executes the control logic in the FPGA target on reconfigurable chassis (FPGA code compiled in the host computer and downloaded to the FPGA memory).Based on the real time input and the control logic, the output control signals are sent to NI 9474 digital output module. There are three output channels used, two to provide the gating pulses to the IGBTs gate drive circuits based on the current control logic and one to enable or inhibit the DC Power Source based on the capacitor voltage level.

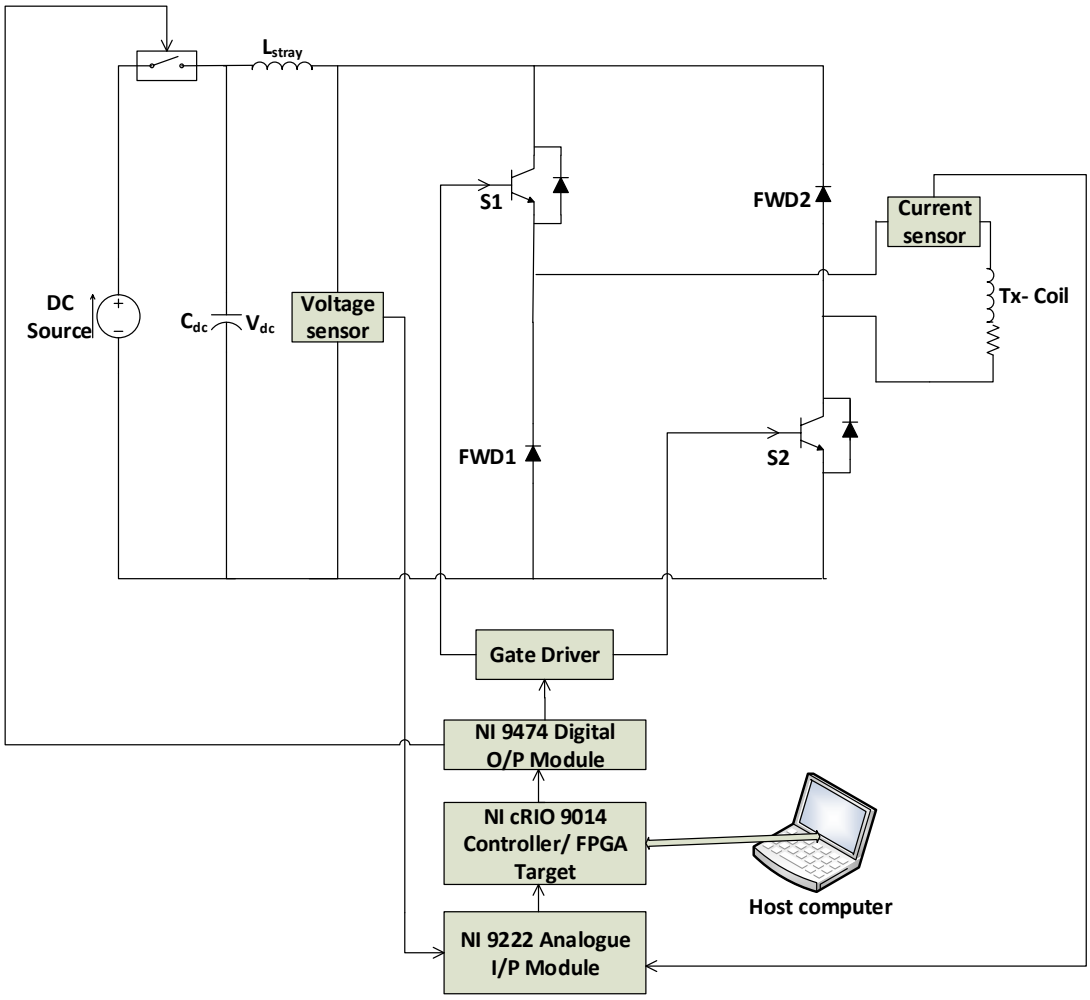



Fig. 4.8 Circuit Diagram- Experimental Setup

## 4.5 PROGRAMMING LOGIC IN LABVIEW

As mentioned earlier, the programming in LabVIEW environment mainly consist of two parts, the front panel and the block diagram. The front panel contains the indicators, control inputs and graphs associated with a block diagram code. A block diagram contains the code based on LabVIEW inbuilt functions blocks or nodes. Virtual Instruments (VIs) are the LabVIEW programs that are used for writing the application control logic. Each VI

has three main subparts – the front panel window, the block diagram and the icon/ connector pane. The front panel window acts as the user interface for the VI. The front panel window may contains controls and indicators that interact with the VI to pass or receive the data. Block Diagram window is used to write the application code using graphical representation of functions to control the front panel objects. The block diagram window contains the graphical source code for an application. Front panel objects appear as terminals on the block diagram. The connector pane allows to use and view a VI in another VI as a sub –VI.

The LabVIEW program code for this application contains 2 main virtual instruments (VIs)

1. GUI.vi 2.FPGA.vi

### 4.5.1 GUI.VI

In this work, a separate GUI as shown in Figure 4.9, is created on the host computer to pass the user defined control parameters to the FPGA code (hysteresis current control). GUI shown in Fig. 4.10 is used for the application using constant ON-Time control. The parameters controlled through GUI are reference current, DC bus voltage, ON-time (Band timer), Pulse Width, Sampling Rate and No of channels read by DMA FIFO. Graphical user interface, GUI is also used to display the DC bus voltage, FPGA loop tick rate and actual sampling rate achieved during run time. Three buttons are created with individual function to start the firing of the converter switches , reset the power supply in case the Power Supply goes into inhibit state and to give a stop command to the data acquisition loop . A data file path selection window is provided to select the path where a data file

containing the acquired input data is saved for post processing. The waveform windows are used to show the current and voltage sensor run time waveforms. This data is passed from FPGA target to the host computer by using DMA FIFO as discussed in next section on data acquisition.

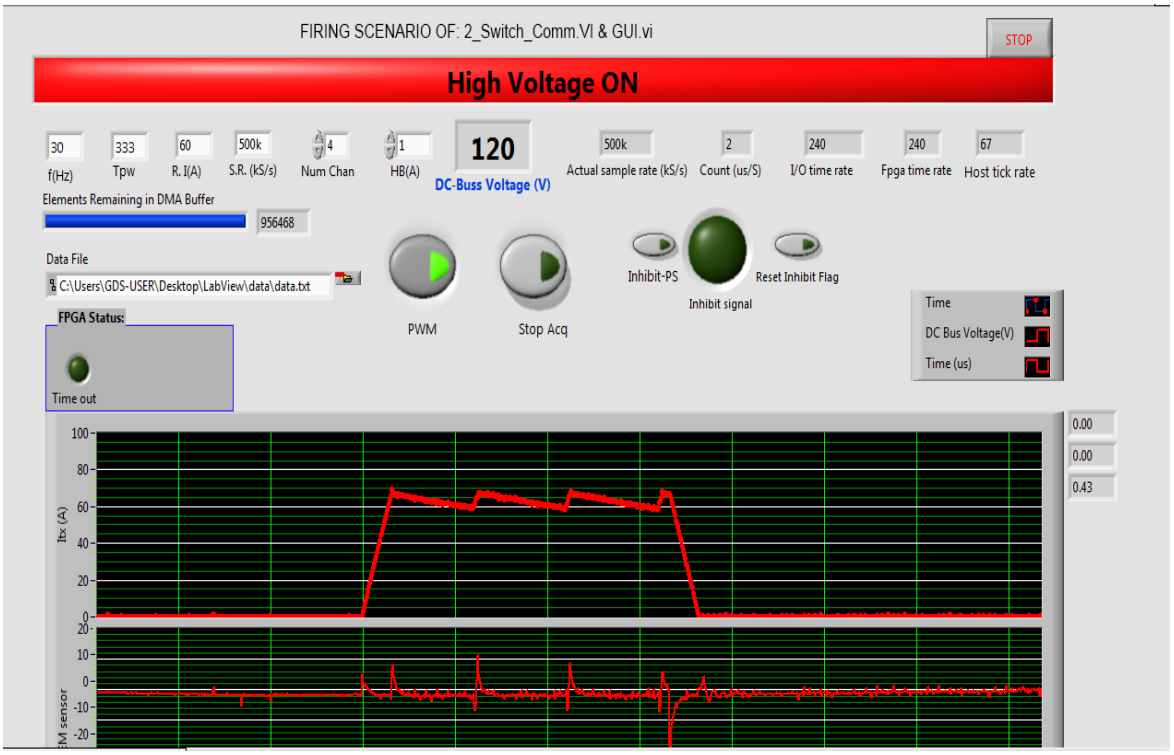



Fig. 4.9 GUI.vi Front Panel (Hysteresis Current Control)

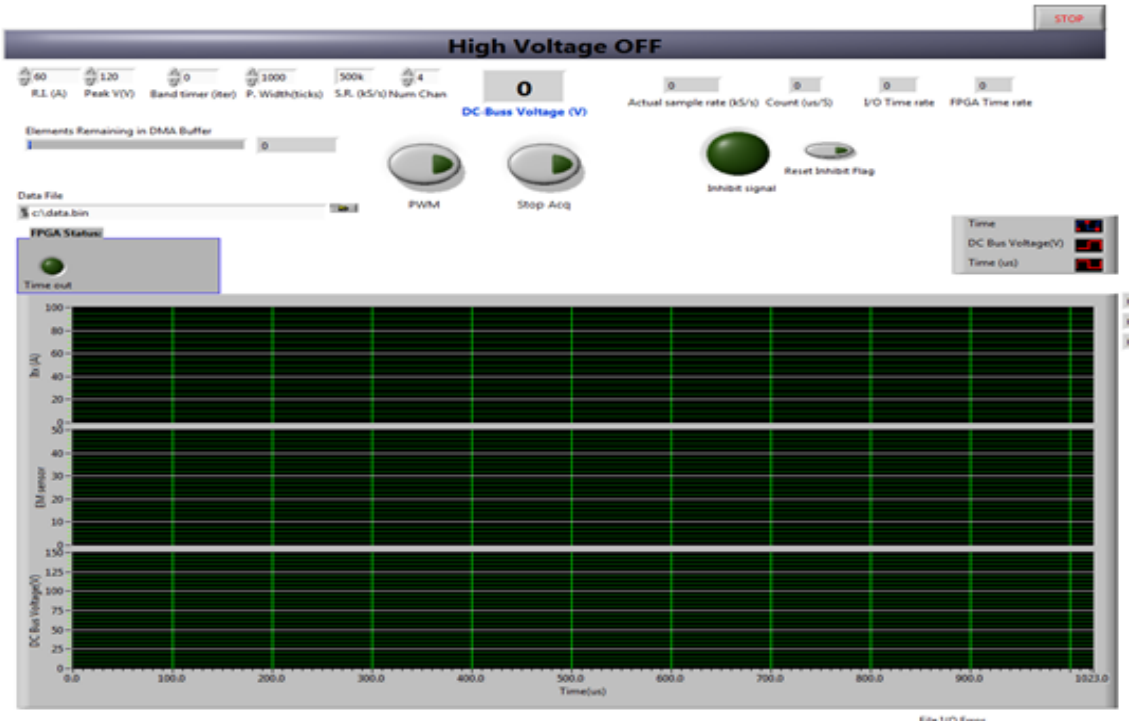



Fig. 4.10 GUI.vi Front Panel (Constant ON-Time Control)

Fig. 4.11 shows the first part of the GUI block diagram that updates the indicators on the GUI front panel by reading their status from the FPGA Target.

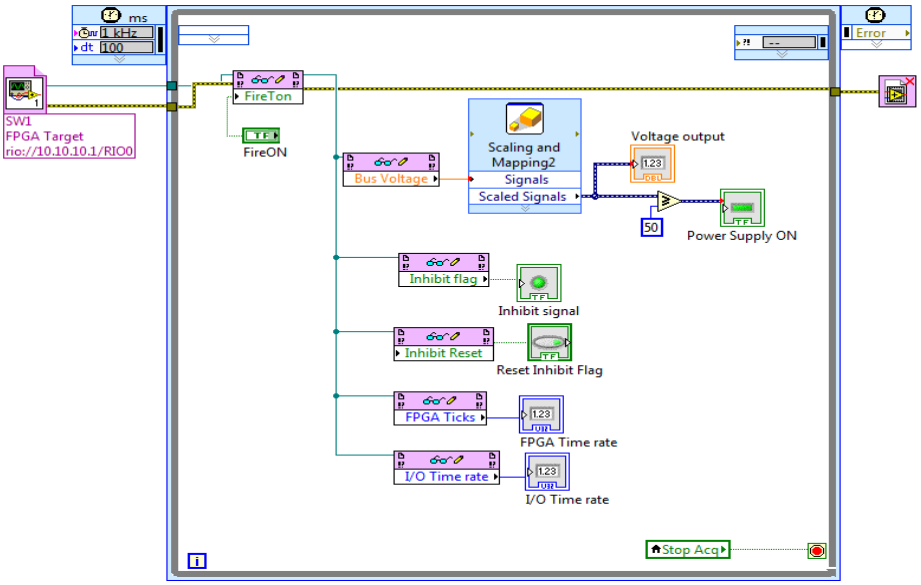



Fig. 4.11 GUI.vi Block diagram (Indicators)

Fig. 4.12 shows the second part of the GUI block diagram where various control parameters are passed to the FPGA and also it contains the host side architecture for DMA FIFO to read the sampled data from analogue input module. The details of data transfer from FPGA to host are discussed in section 4.5.2

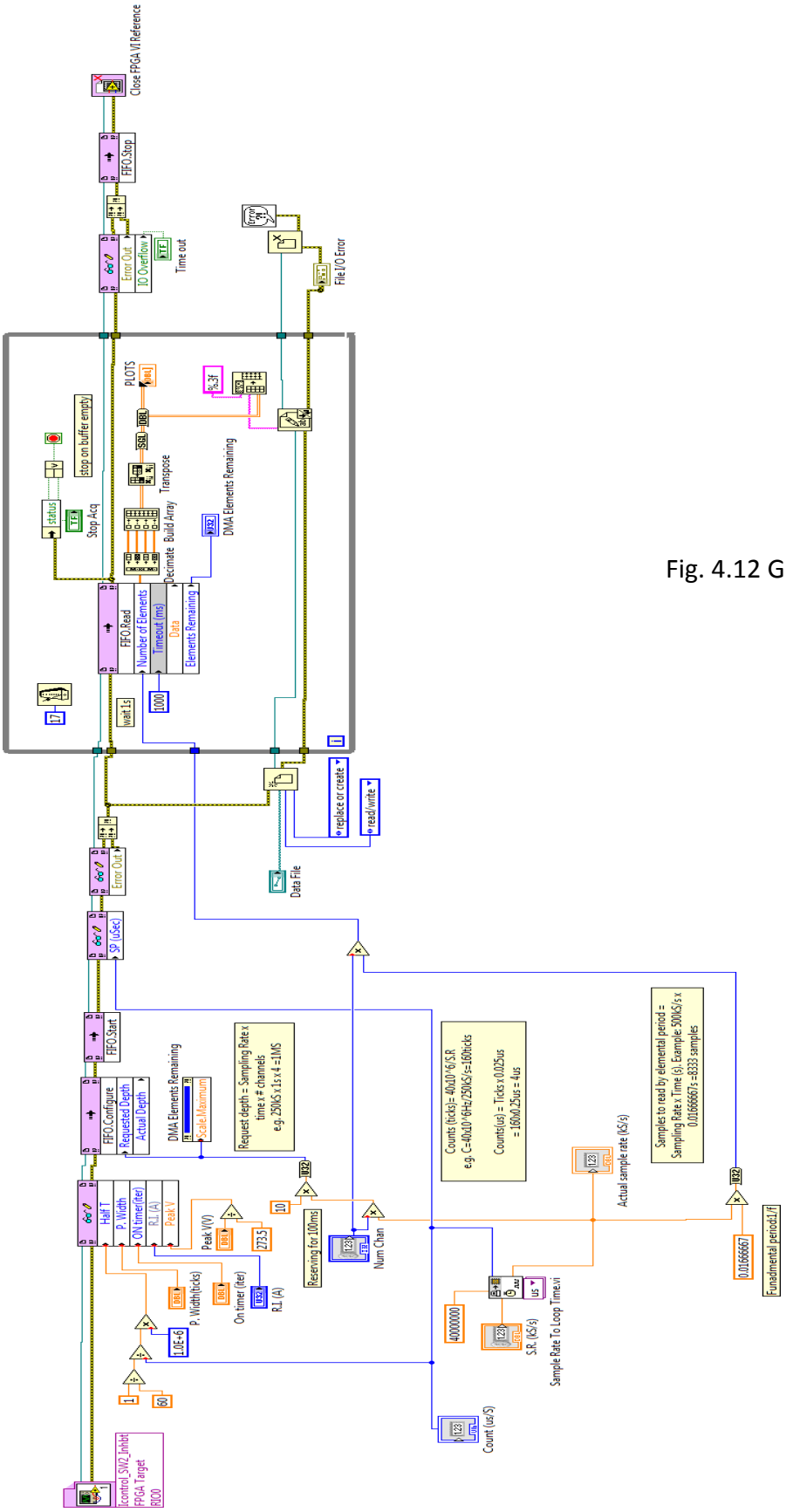



Fig. 4.12 GUI block Diagram (DMA- FIFO)

### 4.5.2 FPGA.VI (FPGA TARGET)

FPGA target contains the main code that controls the functioning of power converter. FPGA code is written in LabVIEW graphical language and is compiled and downloaded to the FPGA target on the reconfigurable chassis. The FPGA code for this application contains two major sub parts in terms of two while loops.

**Data Acquisition Loop**: The first loop as shown in Fig. 4.13 is the Data Acquisition Loop or DMA FIFO loop where the input data from NI 9222 analogue input module is transferred to the host machine. There are various ways to read the data from an input module. However to have a deterministic data reading and transfer from the input module , user-defined I/O sampling method is described as the best method .By using this method the maximum sampling rate as high as 500 KS/s can be achieved from an analogue input module (NI 9222 in this case). Other methods such as using FPGA I/O node results in a maximum sampling rate of 300 KS/s which results in underutilization of the hardware components. Fig. 4.14 and Fig. 4.15 shows the general architecture for FPGA I/O node and user- controlled I/O sampling to read the input module data.

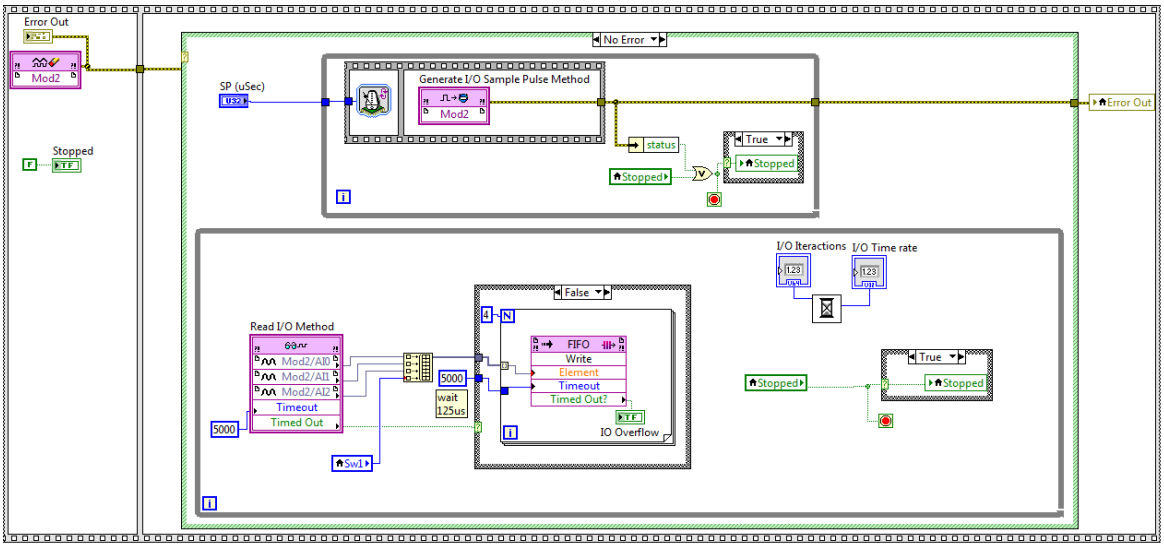



Fig. 4.13 Data Acquisition using User Controlled I/O sampling on the FPGA target side

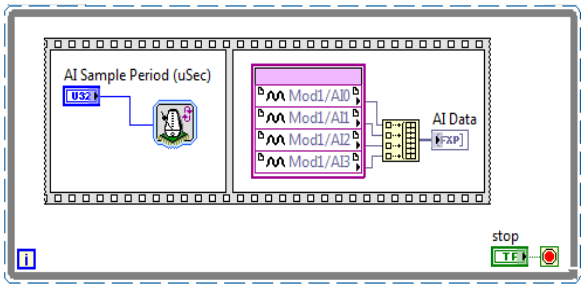



Fig. 4.14 Reading Input channels with FPGA I/O node

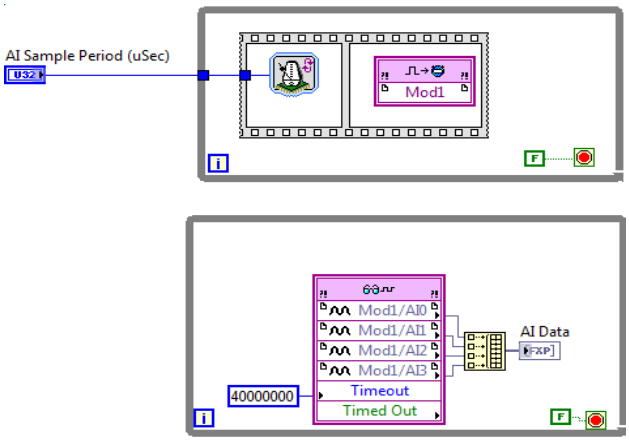



Fig. 4.15 User-Controlled I/O sampling

The acquired data is transferred from FPGA to the host computer using DMA FIFO (Direct Memory Access FIFO). This is a special function architecture defined in LabVIEW for deterministic data transfer between FPGA target and the host computer VI. It consists of two parts. The first part of this FIFO is on the FPGA target. It uses block RAM on the FPGA device and is used to read the data from input module. The second part of the DMA FIFO is on the host machine. This portion of the FIFO uses the host machine memory resources. Fig. 4.15 shows the data acquisition on the FPGA target side by using user controlled I/O sampling and DMA FIFO. The analogue input channel data from 3 input channels and a local variable (containing switch 1 gating signal status) is combined into a single array and is passed to the FIFO by using “For loop” indexing. The For Loop indexes through each element of the array and passes the data into a DMA FIFO sequentially with a timeout of specified ticks (5000 in this case). The second part of the DMA FIFO is on the host side and is shown in Fig.4.12 in previous section. In Fig. 4.12 the reference to the FPGA is provided by configuring an open FPGA VI reference function and connecting it to various blocks in GUI block diagram. The DMA FIFO data is read by starting the DMA FIFO and configuring a DMA FIFO read node. The read data is in the form of indexed array. A decimate array, Build array and transpose function is used to make four separate arrays for the read data. A plot function is used to plot the waveforms on GUI front panel. A write to text file function is used to write the acquired data into a file on the host computer.

**Control Loop:** The second loop in the block diagram is the control loop as shown in Fig. 4.16.The input channel data can be passed from the acquisition loop to the control loop using different methods such as Local Variable or Real Time FIFOs. However it was

found that use of these methods result in the slower execution rates for both the acquisition and control loops. To avoid any delays in loop execution another User-Defined I/O node is used in the control loop to read the input channel data. The control loop was first developed by implementing the digital hysteresis current control by using an inbuilt LabVIEW function “Relay VI”. It resulted in a loop cycle time of 18 us which is quite high for current regulation. The loop cycle time is measured in terms of the ticks that a particular loop takes to execute. For this purpose a sub VI “Timer” was used. The block diagram for this VI is shown in Fig. 4.17. To measure the execution rate of data acquisition loop and the control loop this Sub VI is placed separately in these two loops. FPGA ticks for the data acquisition loop and control loop are passed to the GUI interface as shown in Fig. 4.11. For a case ,if the FPGA rate shown in the block on GUI displays 240 , it means the FPGA control loop is taking 240*0.025 =6us per loop cycle. This loop cycle time defines the actual time step for the control logic. For faster response from the controller it is very important to keep this time step to minimum which is 2 μs as per the used hardware capability.

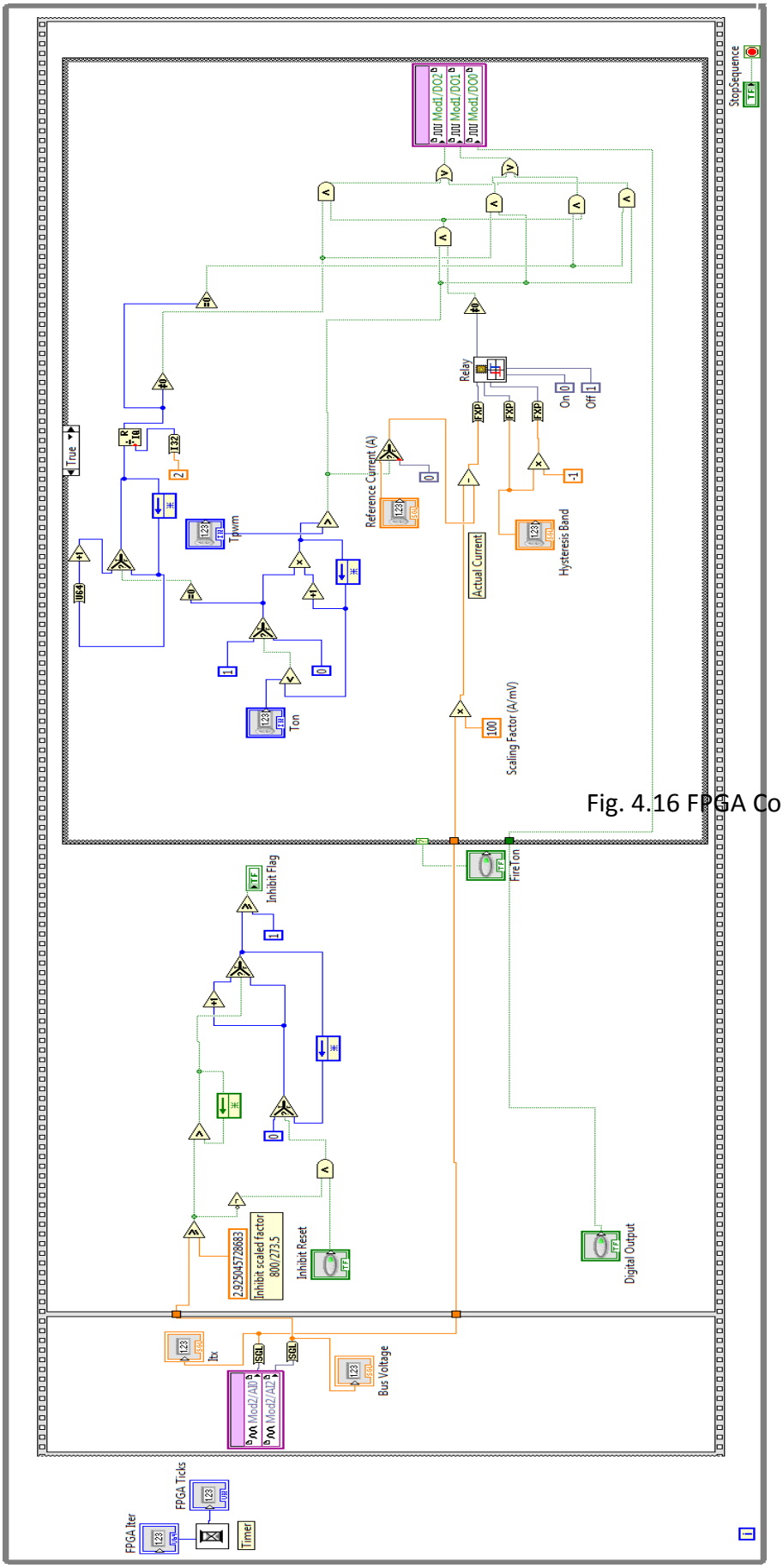



Fig. 4.16 FPGA Control loop (Hysteresis Current Cor

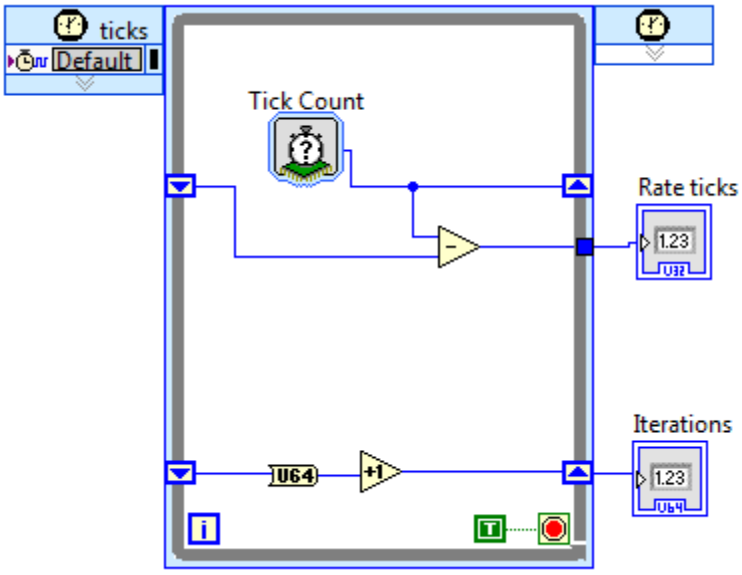



Fig. 4.17 Block Diagram for Timer sub VI

## 4.6 CODE OPTIMIZATION

The execution time of the control loop and data acquisition loop is very sensitive to the coding practices used in developing the application. One function such as reading the input from input module or writing the output signal to the digital output module can be achieved in many different ways. In this particular application, the target was to achieve least possible cycle time of 2µs. The code development has gone through following improvement stages to reach to the final results of 2µs.

**Stage 1**: In initial stage the sensor data was read from analogue input channels using individual FPGA I/O nodes and the output data from control logic was passed to the digital output module NI 9474 using individual FPGA I/O nodes as shown in Fig. 4.18. This called

for more utilization of memory resources on FPGA target and resulted in a loop cycle time of 18µs.

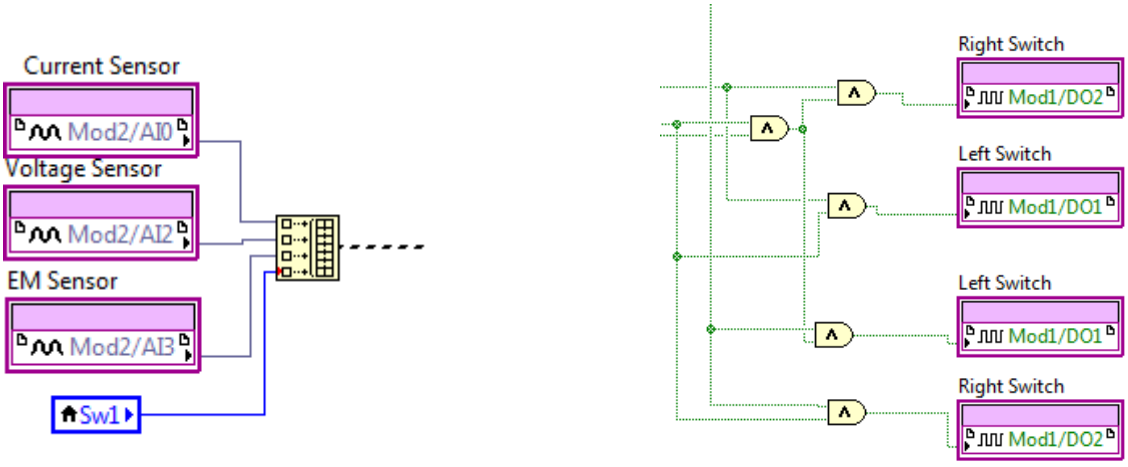



Fig. 4.18 Reading and writing data using individual FPGA I/ O nodes

**Stage 2:** In next stage the reading and writing functions were performed by using an inbuilt "Read I/O method" block as shown in Fig. 4.19. This is a single block containing the group of all input or output channels and since it reads and writes all the channels at once. This change reduced the sampling time from 18 µs to 6 µs.

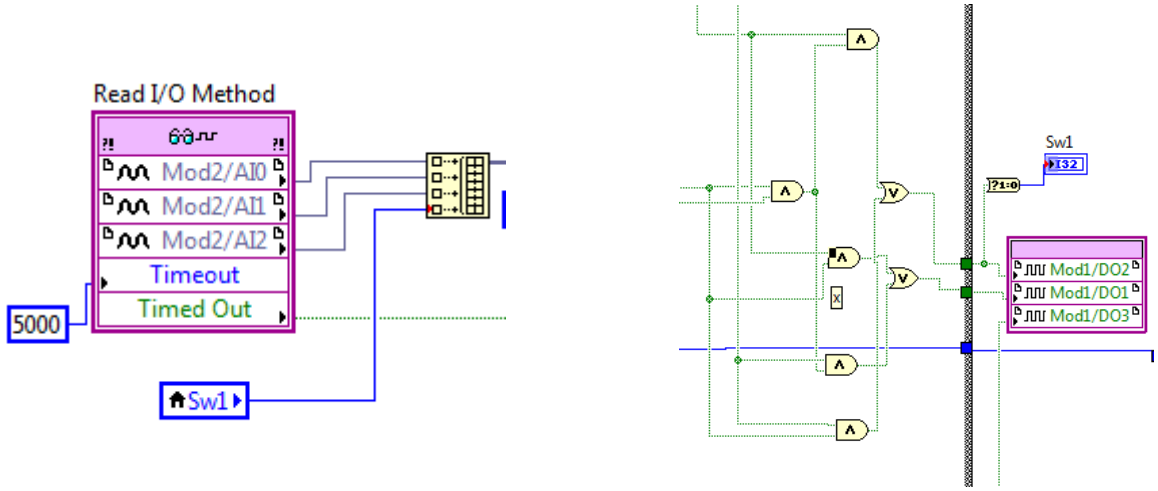
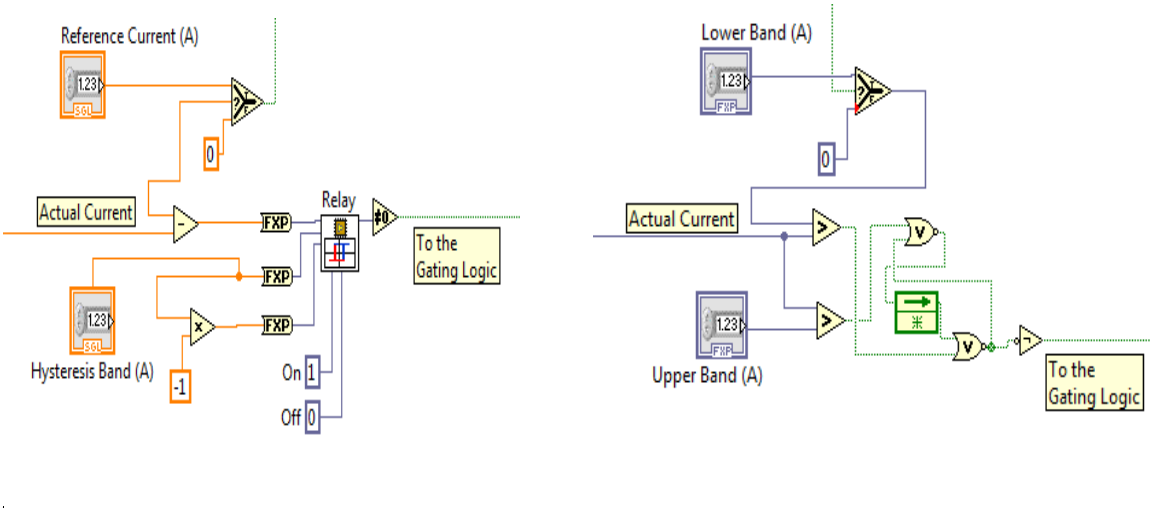



Fig. 4.19 Reading and Writing data using Single I/O node

**Stage 3:** Till this stage the hysteresis logic was implemented by using inbuilt Relay VI function as shown in Fig.4.20 (a). Next, the hysteresis logic was implemented using S-R flip flops as shown in Fig. 4.20 (b). This did not improve the sampling time and it remained to 6 µs.




(a) (b)

Fig. 4.20 Implementation of hysteresis current control using (a) Relay VI (b) S-R flip flop

**Stage 4:** At this stage, the new control technique, constant ON-Time control (as discussed in section 3.4 of Chapter 3) was implemented. This logic is implemented with case structures which is similar to if-else condition in text based programing. This code needs less memory resources on the FPGA chip, as at a time only one case executes. Also at this stage the input data acquisition was implemented by using user –controlled I/O method for both the acquisition and control loop. These improvements resulted in reduction of sampling time from 6 µs to 2µs. However the implementation of double switch operation, as per Fig. 4.21 needs additional code to capture the even and odd cycles and also

requires number of logic gates. All these functional blocks slows down the code execution. To get rid of these additional functions, interchange of the gating signals was implemented using State machine approach (Fig. 4.22). State machine approach is developed by using case structures and shift registers. Implementation of this code architecture resulted in loop cycle time of 2µs (with interchanging of switch signals).

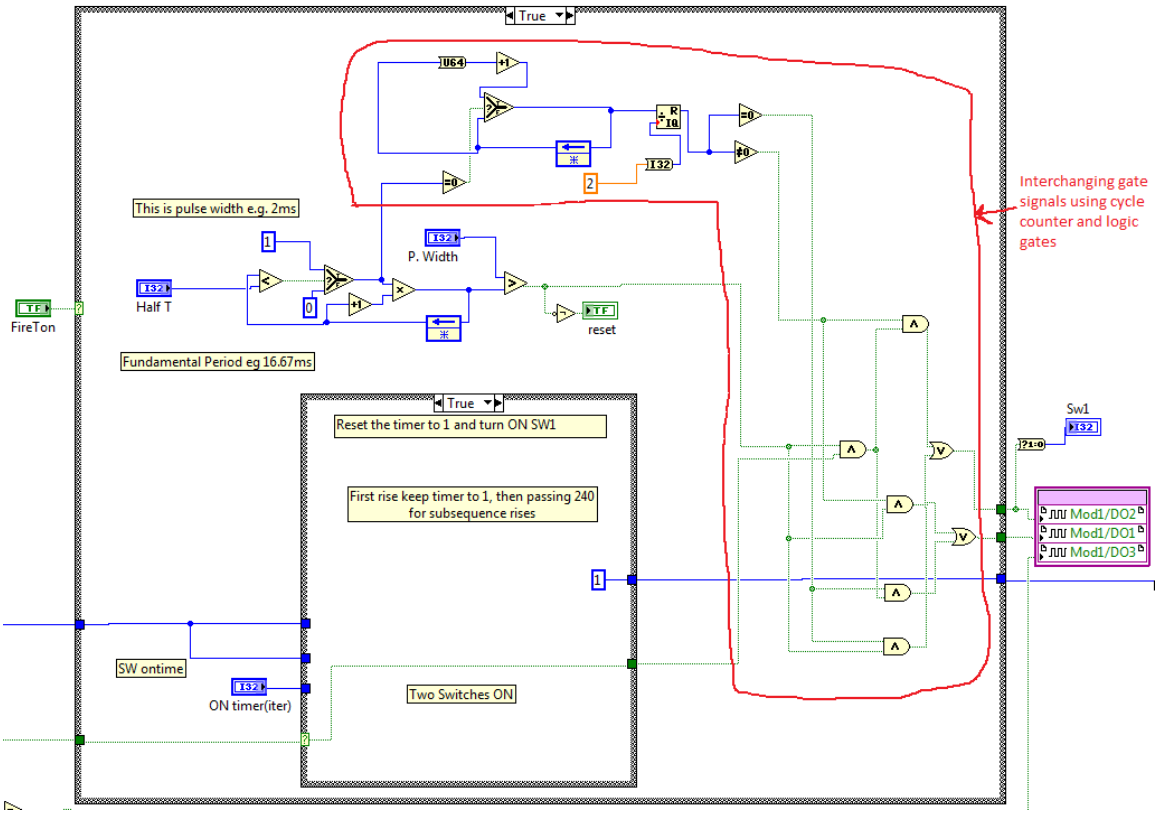



Fig. 4.21 Interchanging switch gate signals using cycle counter and logic gates

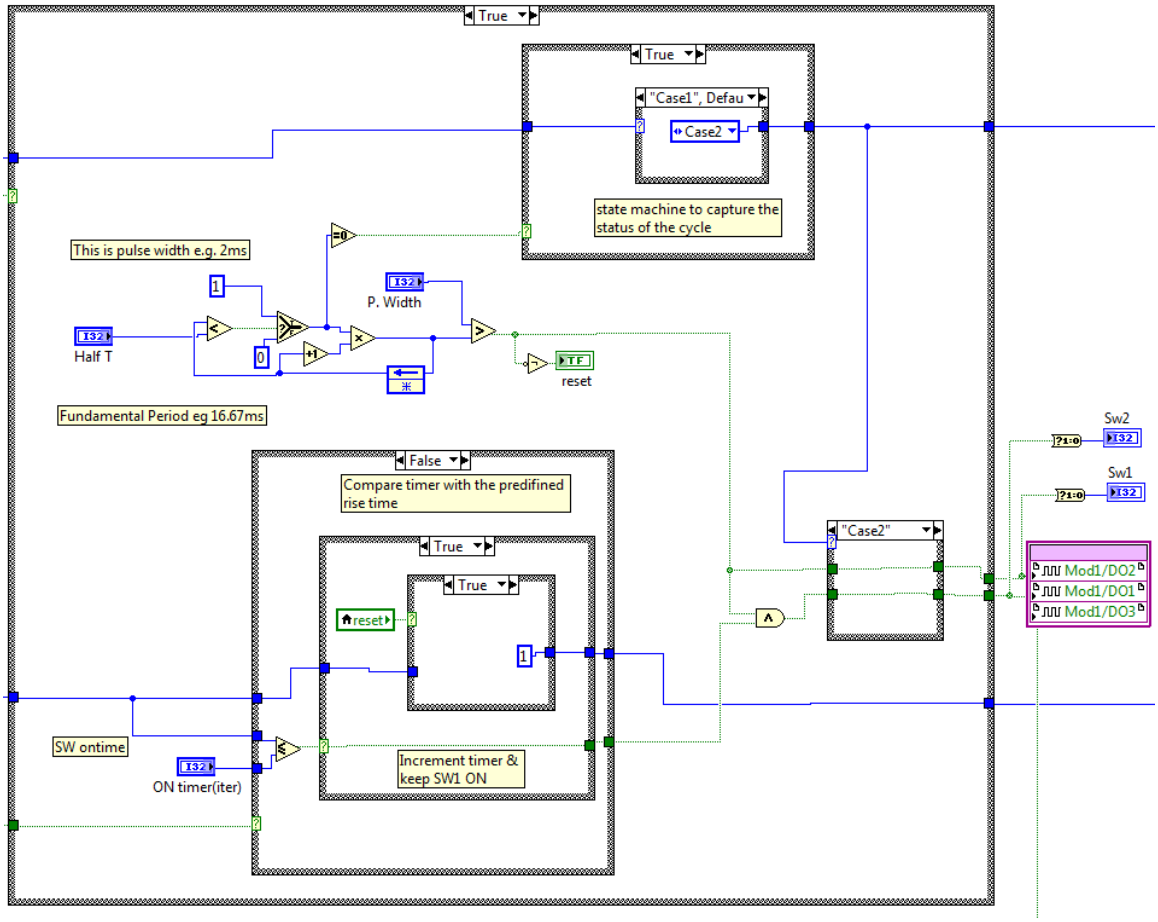


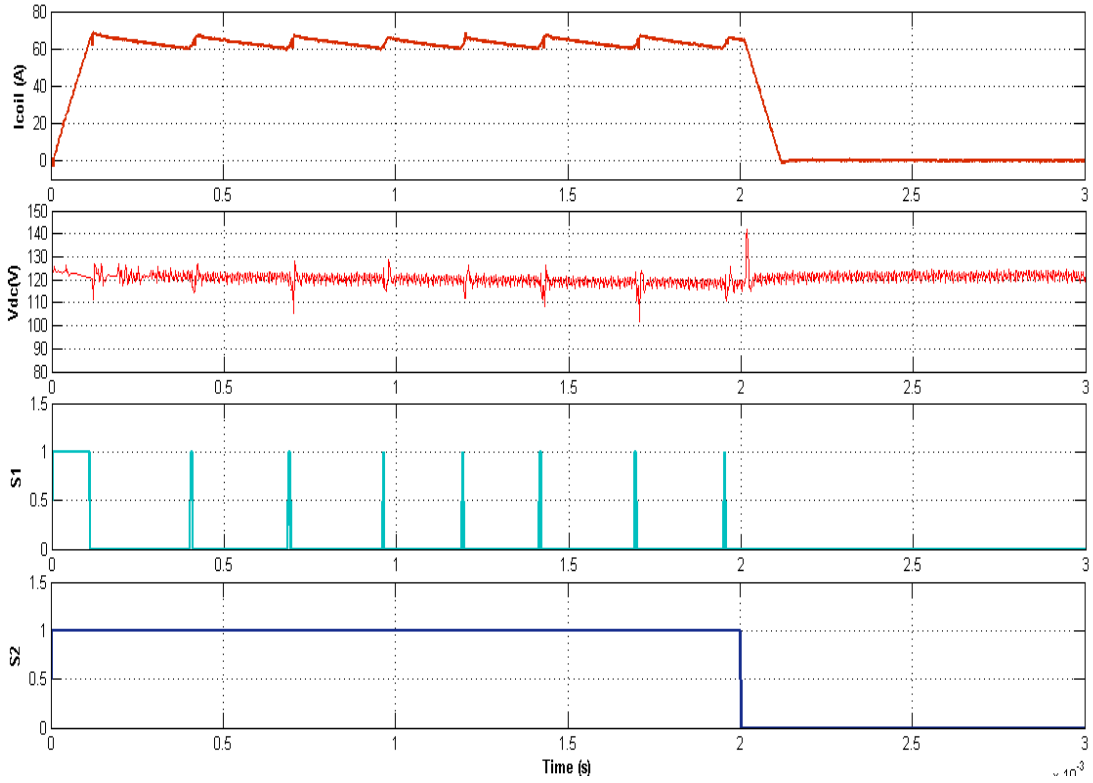

Fig. 4.22 Interchanging gate signals using case structures

It was observed that by code optimization the loop cycle time was reduced from 18 µs to 2 µs i.e. with improved code, the entire cycle containing input current reading from analogue input module and execution of control logic is completed in a time period of 2 µs. This shows that the implementation of the converter control with LabVIEW resulted in control speed way higher than the conventional DSP controllers.

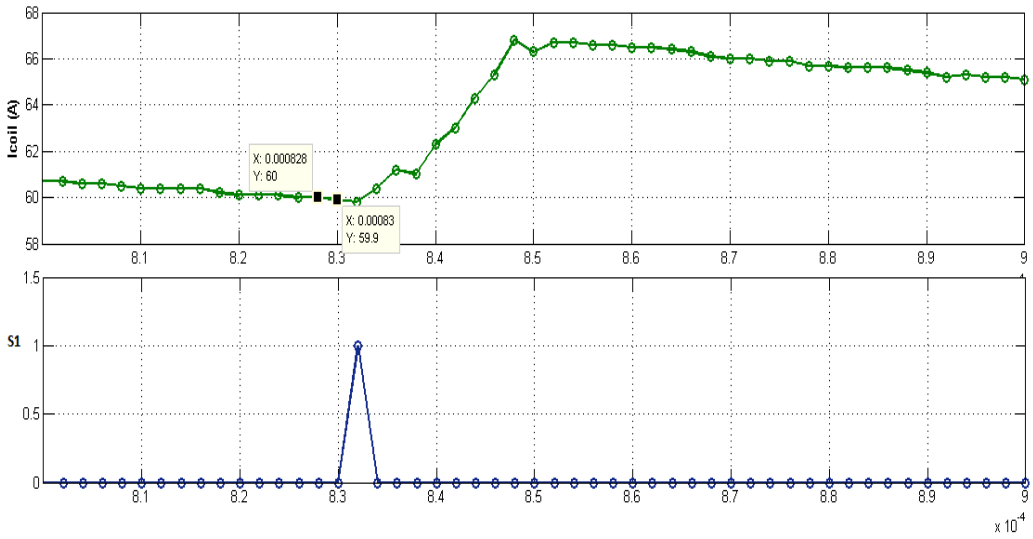
Also reducing the timing further will not improve the performance as the maximum sampling rate per channel for NI 9222 analogue input module is 2 µs.

## 4.7 SWITCH TURN-OFF DELAY

A problem observed during the system implementation and testing was related to the delay in switch Turn-OFF. From Fig. 4.8, it can be observed that NI 9474 output module provides high and low digital signals to the IGBT gate driver to Turn ON and Turn OFF the switches respectively. However during actual testing a delay was observed between the instant the NI 9474 output channel goes from high to low state and the instant switch actually turns OFF (Fig. 4.23 (b) and Fig. 4.24). This delay in turning the switch OFF resulted in higher switch ON periods than the value set using GUI input. Also the higher peak currents (72A) are seen in Fig. 4.23 for low power (125V, 60A) tests.




(a)




(b)

Fig. 4.23 Experimental waveforms ($V_{dc}$= 125V, $I_{ref}$ =60A, ON-Time= 4 µs)

(a) One pulse cycle (b) One switching operation

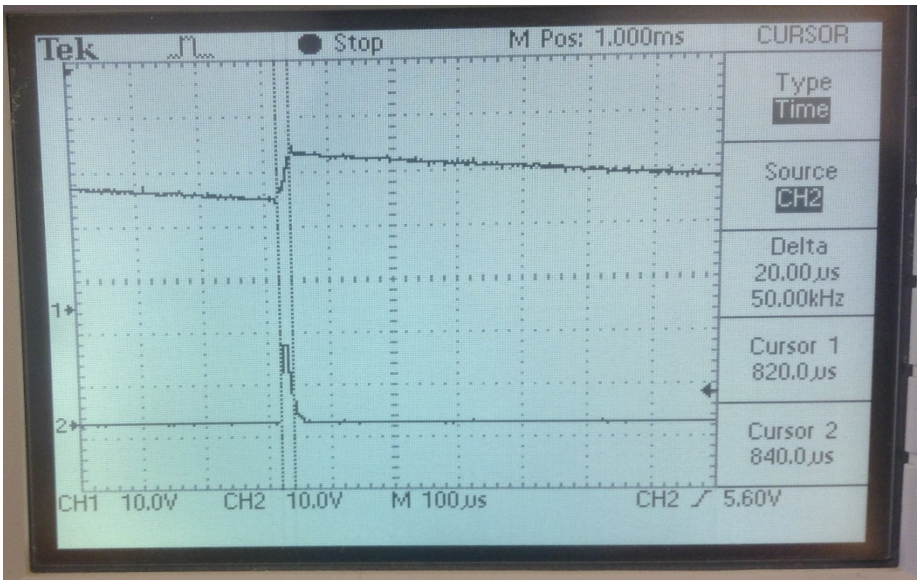



Fig. 4.24 Experimental waveforms without pull down resistor

($V_{dc}$= 125V, $I_{ref}$ =60A, ON-Time= 4 µs (Ch1 – Coil Current, Ch2- S1 gating signal)

The delay in turn OFF is due to the impedance mismatch between the digital output module and the IGBT driver board. Due to this reason the transition from high to low on the output of digital module is delayed. This is a well-known problem in the field of digital electronics and generally pull down resistors are placed between the output channel and ground (as shown in Fig. 4.25) to bring the digital signal from high to low [25]. As per National Instruments knowledgebase [26], placing a 10 kΩ resistor can solve this problem in most of the applications. However in this case, different pull down resistor were used (20 kΩ, 10 kΩ, 3 kΩ and 1 kΩ) and the effect was observed on the gating pulse. It was found that with decrease in resistor value, the delay in transition is reduced. Finally 1 kΩ was used as the final pull down resistors giving nearly square gating pulse.

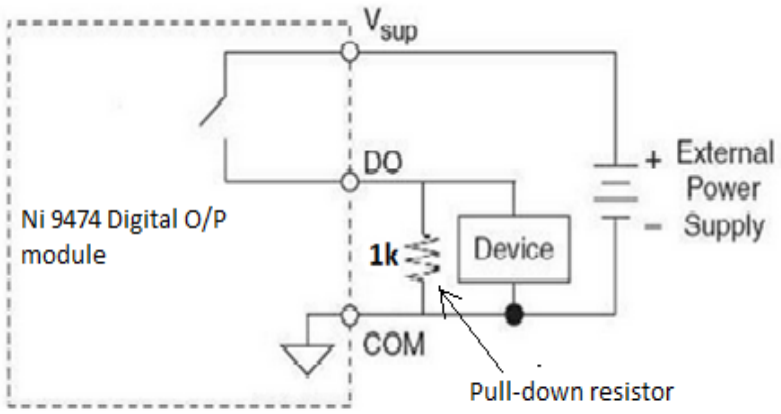
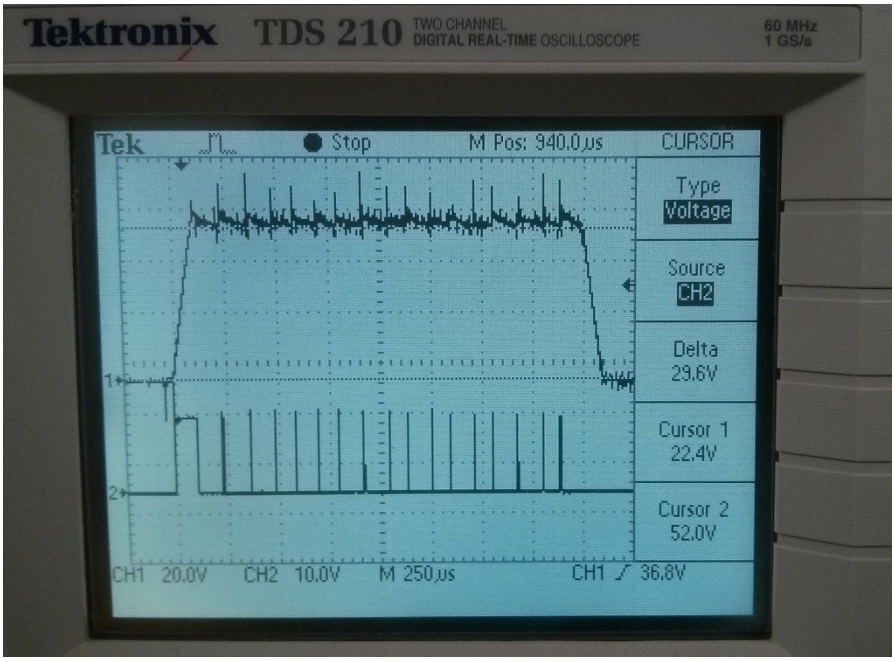


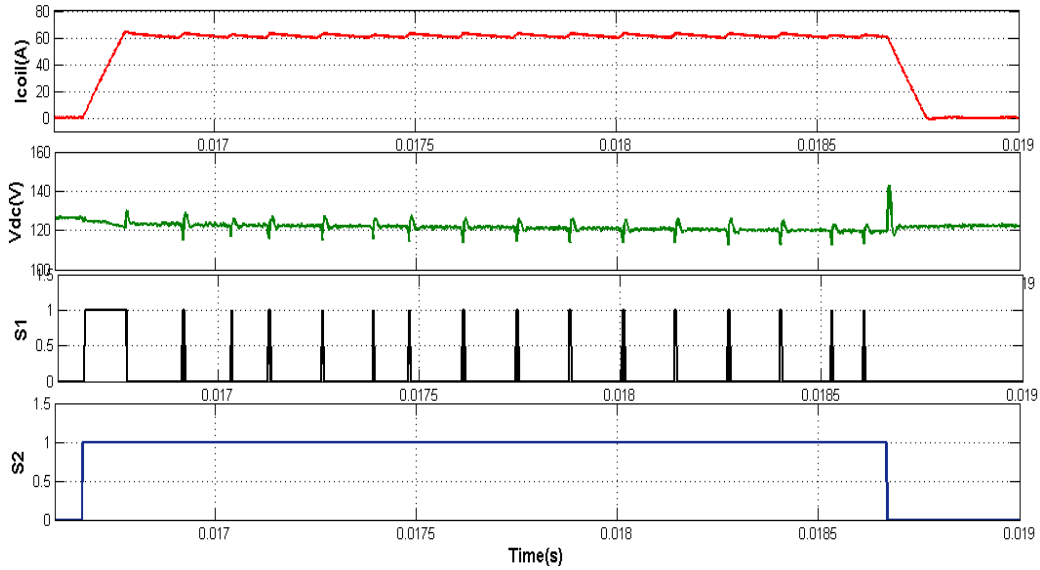

Fig. 4.25 Pull down Resistor and Ni 9474 digital output module

Fig. 4.26 shows the experimental waveforms after placing the pull down resistors between each output of digital output module and ground. It can be seen from Fig. 4.26

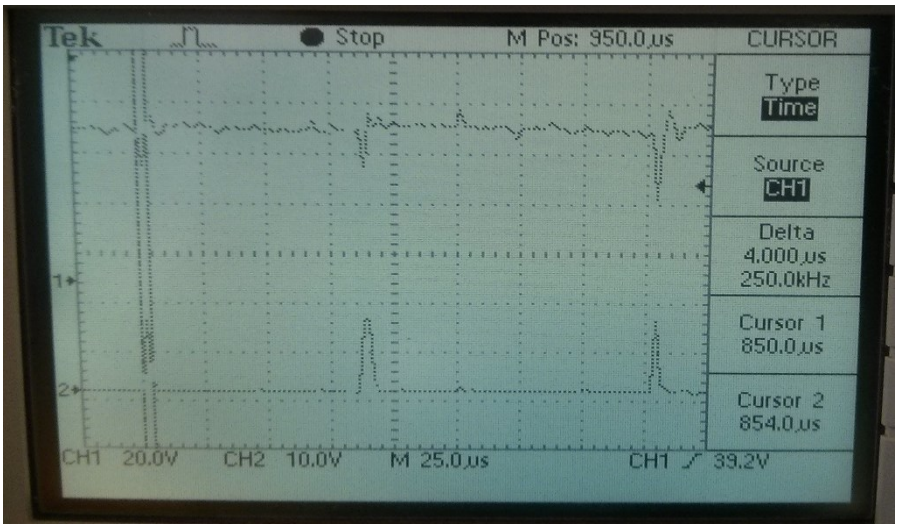
that due to use of the pull down resistors for same pulse width (2 ms) more switch commutations are observed, which indicates less current overshoot keeping the current magnitude closer to the reference value. Fig. 4.26 (c) shows the enlarged waveforms capturing the ON Time of 4 µs which is the value set from the GUI.




(a)




(b)




(c)

Fig. 4.26 Experimental waveforms (with pull down resistor of 1kΩ)

($V_{dc}$= 125V, $I_{ref}$ =60A, ON-Time= 4 µs)

(a) One pulse cycle measured on Oscilloscope (b) Recorded data plot from cRIO (c) Magnified oscilloscope waveform showing switch ON-Time

Table 4-1 presents the description of system hardware components used in the implementation.

Table 4-1 Hardware Description

| Component | Rating | Part No | Manufacturer |
|---|---|---|---|
| DC Power Source | 3kV, 1kW | 102-3kV-POS-5V-LP | TDK -Lambda |
| DC Capacitor | 1000uF, 1500V | SBE 772D100 | SB Electronics |
| IGBT Modules | 1200V, 600A | SEMIX604GAL12E4<br>SEMIX604GAR12E4 | Semikron |
| IGBT Gate Driver | 16V,50mA, 50kHz | Skyper 32 PRO R UL | Semikron |
| Driver Power Supply | ±15VDC ,1.5A | HBB15-1.5-AG | Power-One |
| IGBT Evaluation Board | 16V,50mA, 50kHz | Skyper 32 PRO R | Semikron |
| Digital Controller | 400 MHz processor, 2 GB storage, 128 MB DRAM memory | NI cRIO 9014 | National Instruments |
| Controller Chassis | 4 slot, Virtex-5 LX30, 25ns Resolution | NI cRIO 9111 | National Instruments |
| Analogue Input Module | 4-Channel, 500 kS/s, 16-Bit, ±10 V | NI 9222 | National Instruments |
| Digital Output Module | 8 channel,1µs,5-30V | NI 9474 | National Instruments |
| Controller Power Supply | 24VDC -5A | PS-15 Power Supply | National Instruments |
| Voltage Sensor | 1000V/ 25mA | LV 25-1000 (713122) | LEM |
| Current Sensor | ±400A / ±4V | HAL- 400-S (412107) | LEM |
| Snubber C-D module | 0.47 uF,1200V DC | SCM474K122H8N24-F | Cornell Dubillier |
| Snubber Resistor | 75Ω, 100W | MP9100-75.0F-ND | Caddock Electronics |

Fig. 4.27 shows the overall assembly of the experimental setup developed using above listed hardware.

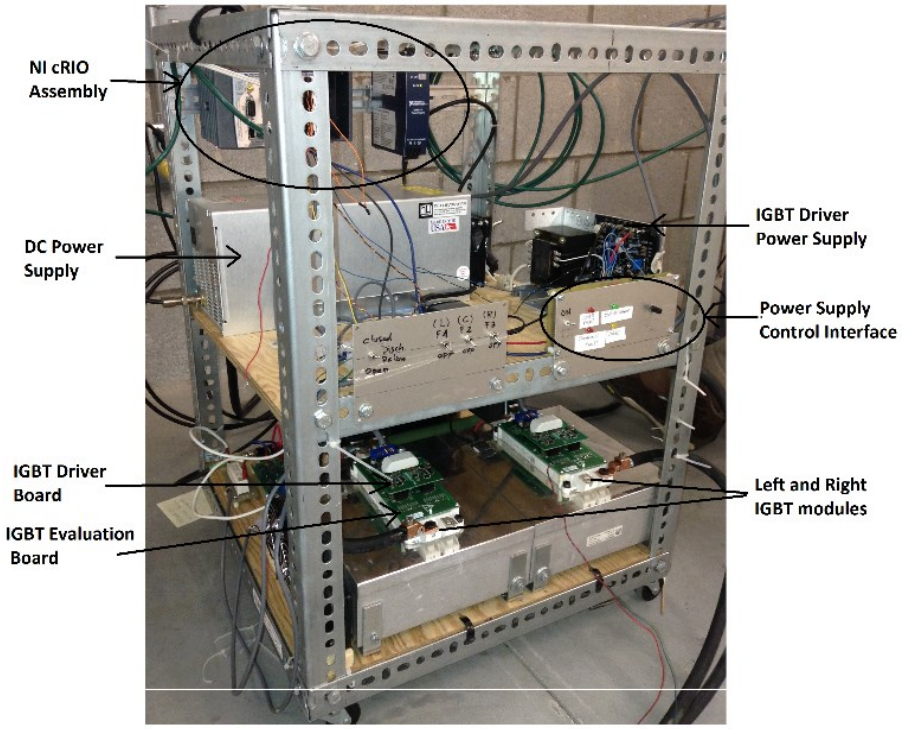



Fig. 4.27 Experimental Setup

Fig. 4.28 shows the din-rail mounted CompactRIO assembly.

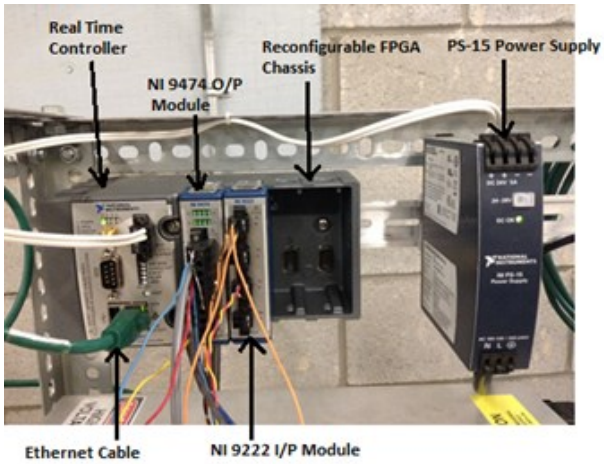



Fig. 4.28 CompactRIO Assembly

Fig. 4.29 shows IGBT module assemblies for left and right leg of the DC -DC converter.

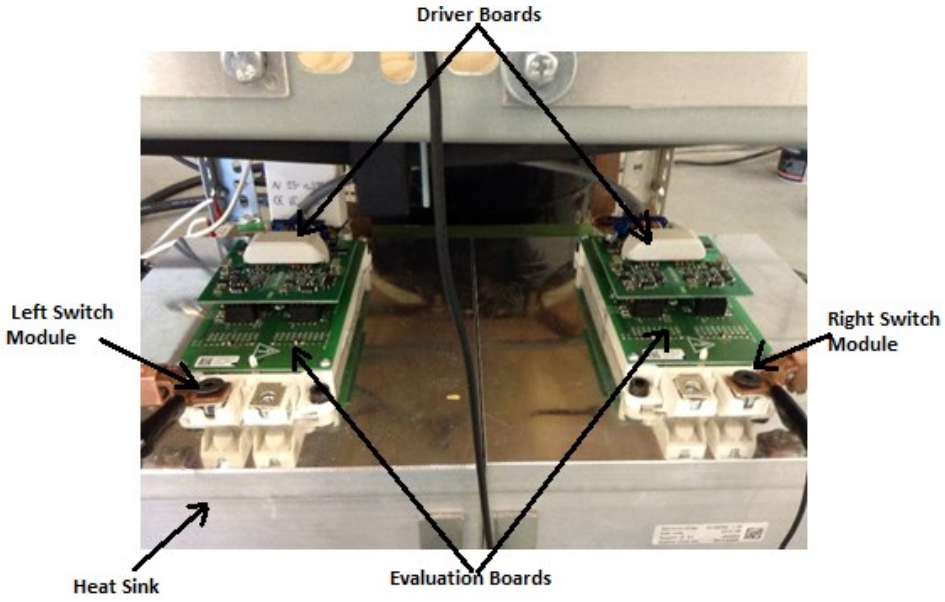



Fig. 4.29 IGBT Modules

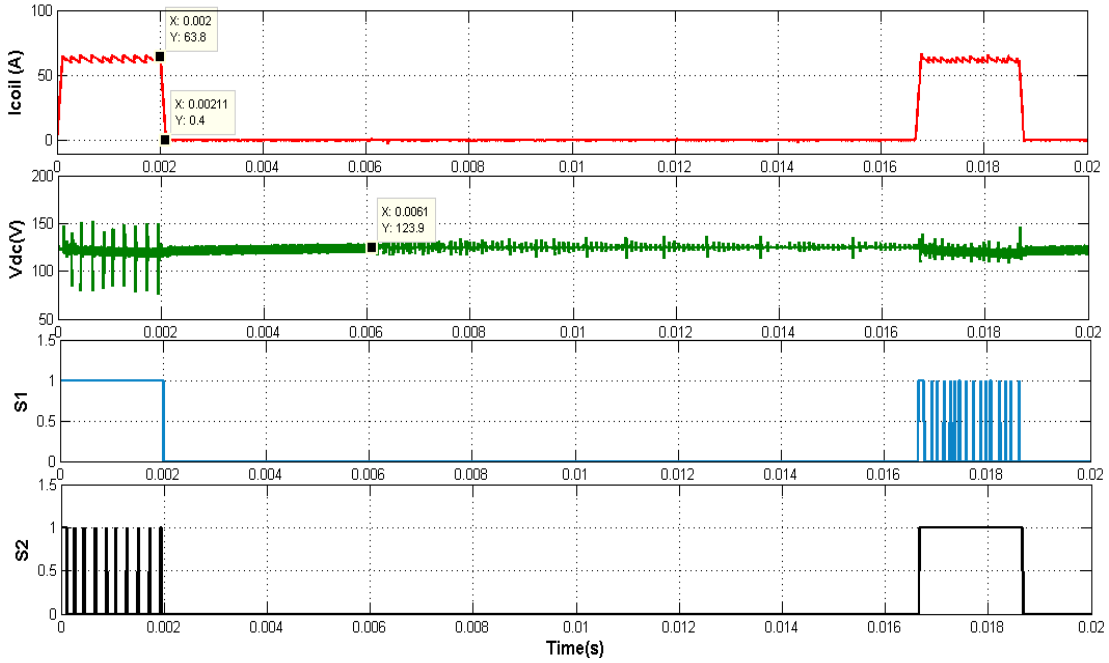
Fig. 4.30 shows the power supply control interface with the turn ON/OFF switch and a control knob for the power supply output voltage control. Indicators are provided to show power supply status signals.


Fig. 4.30 Power supply control interface

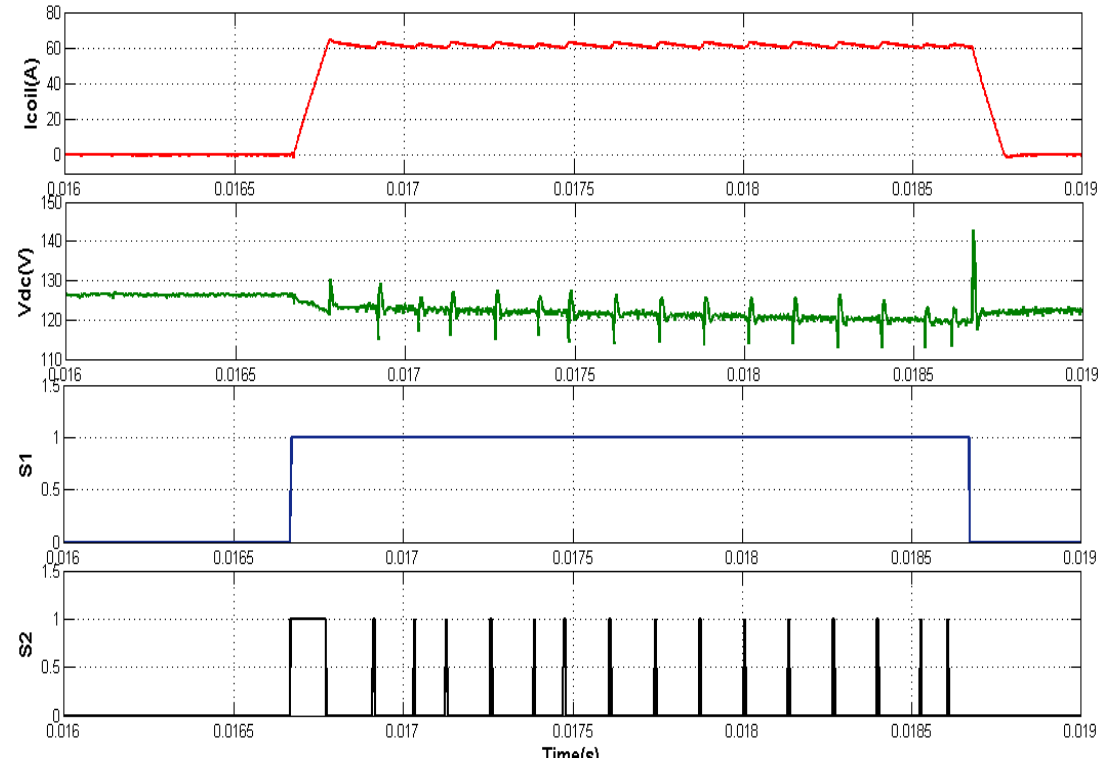
## 4.8 EXPERIMENTAL RESULTS

This section discusses the experimental results obtained from the experimental setup at desired voltage and current levels. The system waveform data is saved on the host computer for each test and was plotted in MATLAB Simulink for better representation.

First the system is tested for low DC bus voltage (125 V) and low current (60 A) and setting the ON-Time to 4 µs. Results with these settings are shown in Fig. 4.31. From Fig. 4.31(a) it can observed that exact times are achieved for the pulse width (2 ms) and fundamental period (16.67 ms). The fall time achieved is 110 µs. Switch gating signals interchange during consecutive cycle is also visible. DC link capacitor voltage is reduced from 125V to 119V by the end of current pulse. The power source supplies the dc current to recharge the capacitor back to reference voltage in approximately 4.1 ms after the end of the current pulse. From Fig. 4.31(b) it can be observed that due to low value selected for the ON-Time, almost constant current is achieved at the top of the current pulse. However this results in more switch commutations per pulse cycle and hence causes more switching power loss. The voltage transients are limited effectively by the RCD snubber modules.




(a)

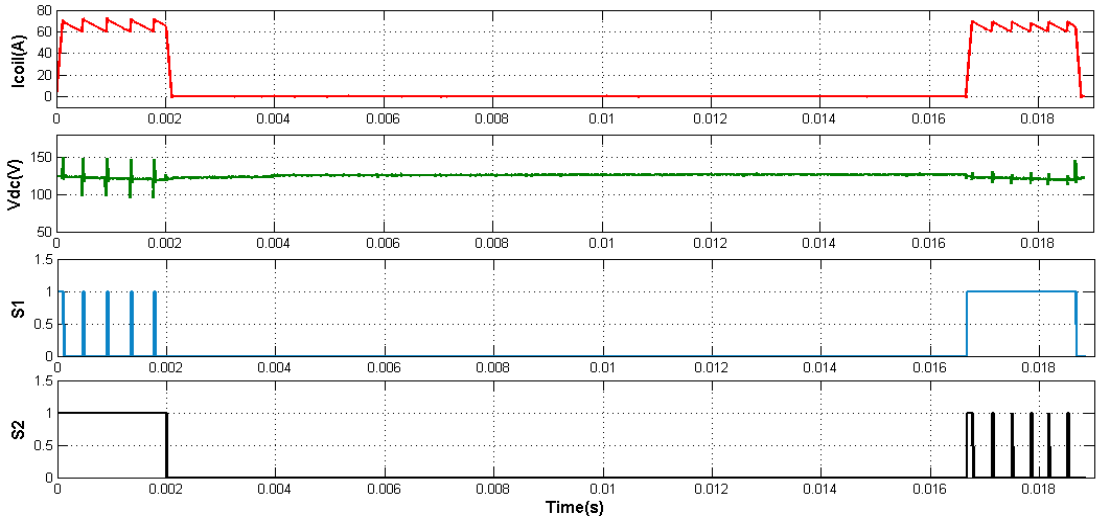



(b)

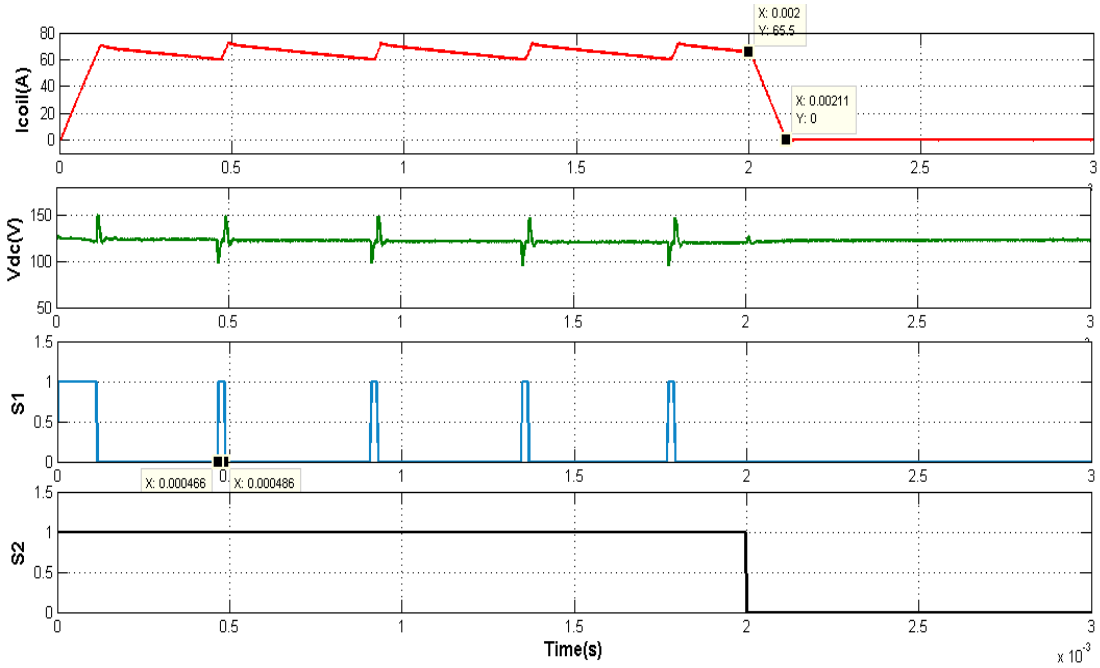
Fig. 4.31 Experimental waveforms- (Vdc= 125V, Iref =60A, ON-Time= 4 µs)

(a) Two pulse cycles (b) One pulse cycle

To reduce the number of commutations, ON –Time is set to 16 µs. Fig. 4.32 (a) and (b) shows the achieved results. It can be seen that the gate pulse has widened in response to higher ON-Time setting. The peak current is around 68 A and reference current is 60 A.




(a)

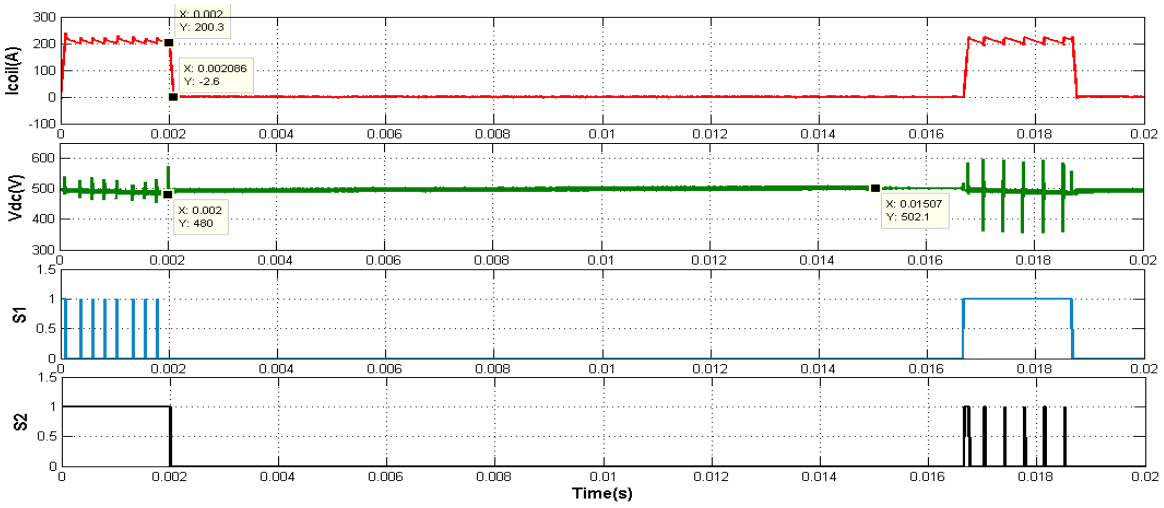



(b)

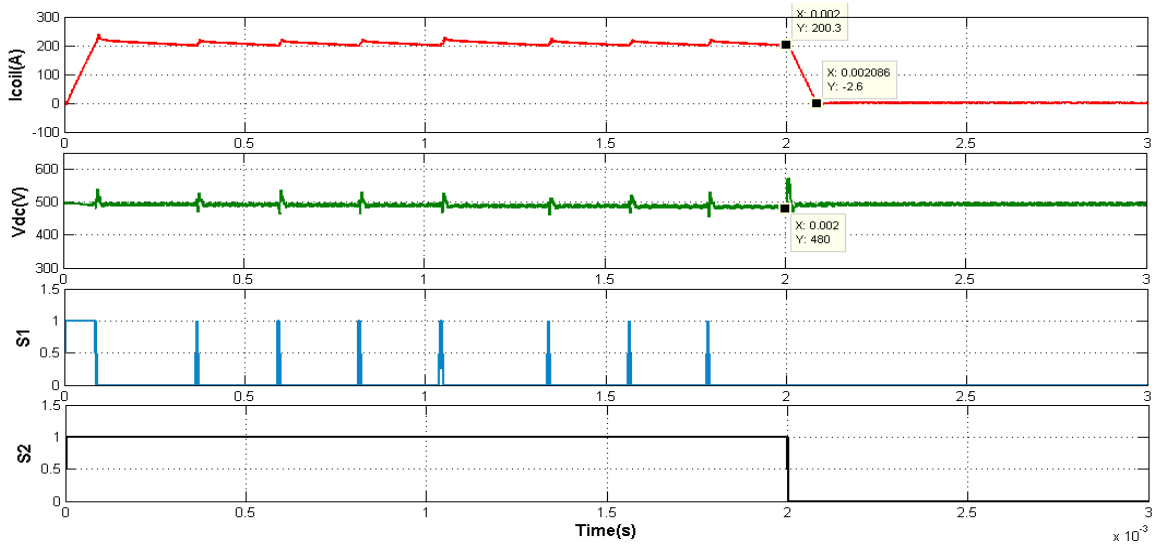
Fig. 4.32 Experimental waveforms- ($V_{dc}$= 125V, $I_{ref}$ =60A, ON-Time= 16µs)

(a) Two pulse cycles (b) one pulse cycle

Fig. 4.33 shows the testing results at high voltage (500V) and high current (200A). The ON-Time achieved is 4 µs. The fall-time achieved in this case is 86 µs (<100µs). Capacitor voltage drops from 500V to 480V at the end of current pulse and is recharged back to 500 V in about 13 ms. With these settings there are around 8 switch commutations per pulse width which are reduced by increasing the preset ON-Time.




(a)

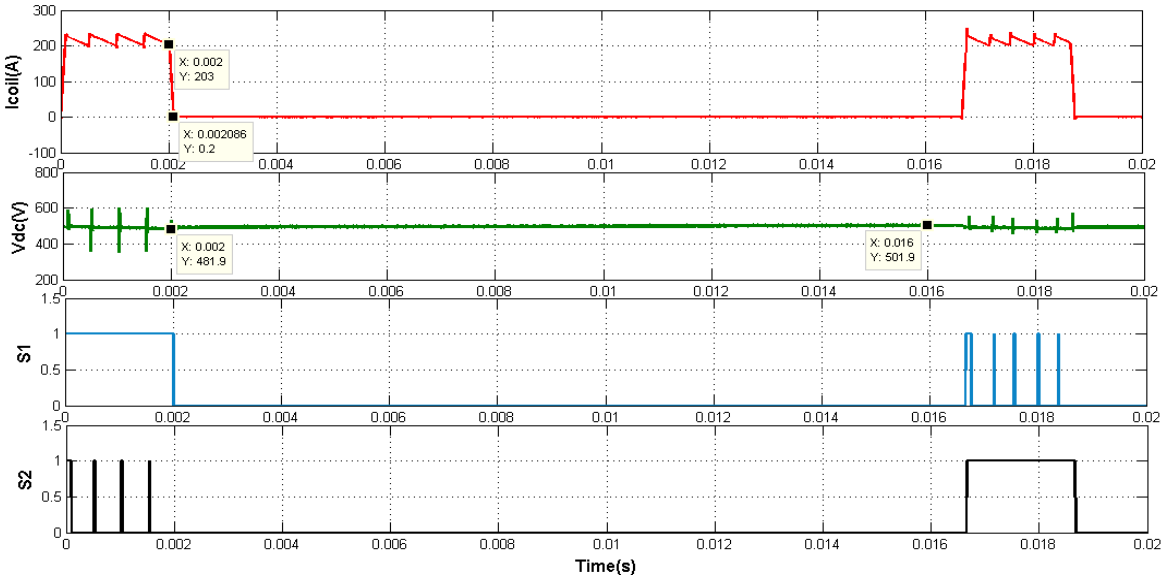



(b)

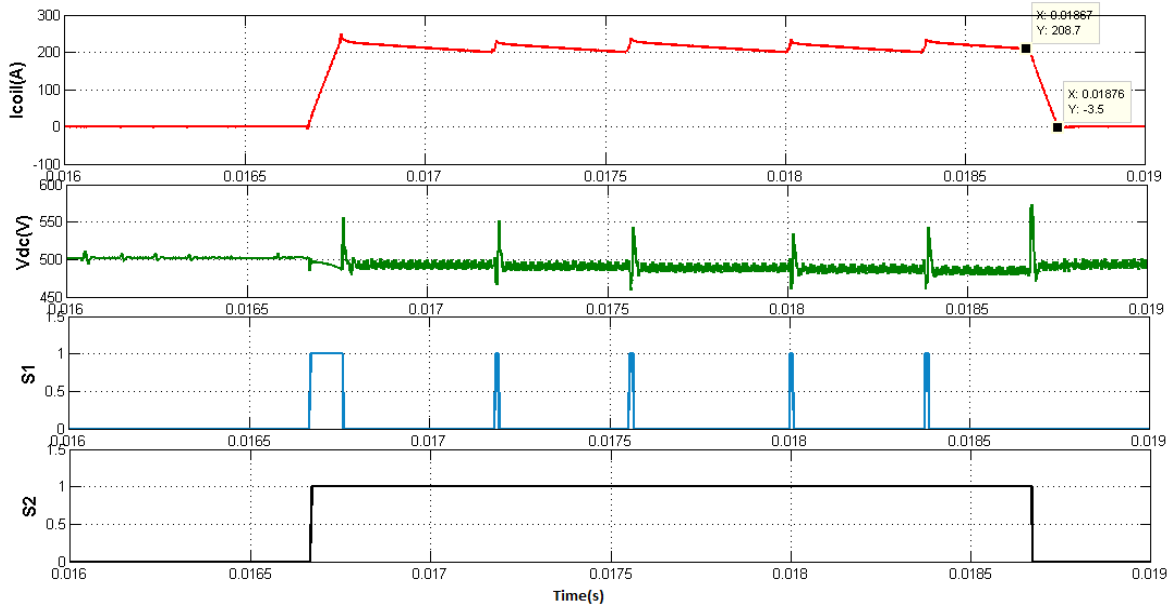
Fig. 4.33 Experimental waveforms ($V_{dc}$= 500 V, $I_{ref}$ =200 A, ON-Time= 4 µs)

(a) Two pulse cycles (b) one pulse cycles

Fig. 4.34 shows the results with ON-Time set to 12 µs. In this case 4 to 5 commutations per pulse cycle were achieved. The fall –Time remains 86 µs. In this case, peak current is around 235 A and reference current is 200 A.




(a)




(b)

Fig. 4.34 Experimental waveforms- (Vdc= 500V, Iref =200A, ON-Time= 12µs)

(a) Two pulse cycles (b) One pulse cycle

The other important feature of developed system is the flexibility to alter the fundamental time period. To test this, the experiment was conducted with DC bus voltage 500 V, and reference current of 200 A. Fig. 4.35 and Fig. 4.36 show the result waveforms for fundamental period 30 Hz and 10 Hz respectively.

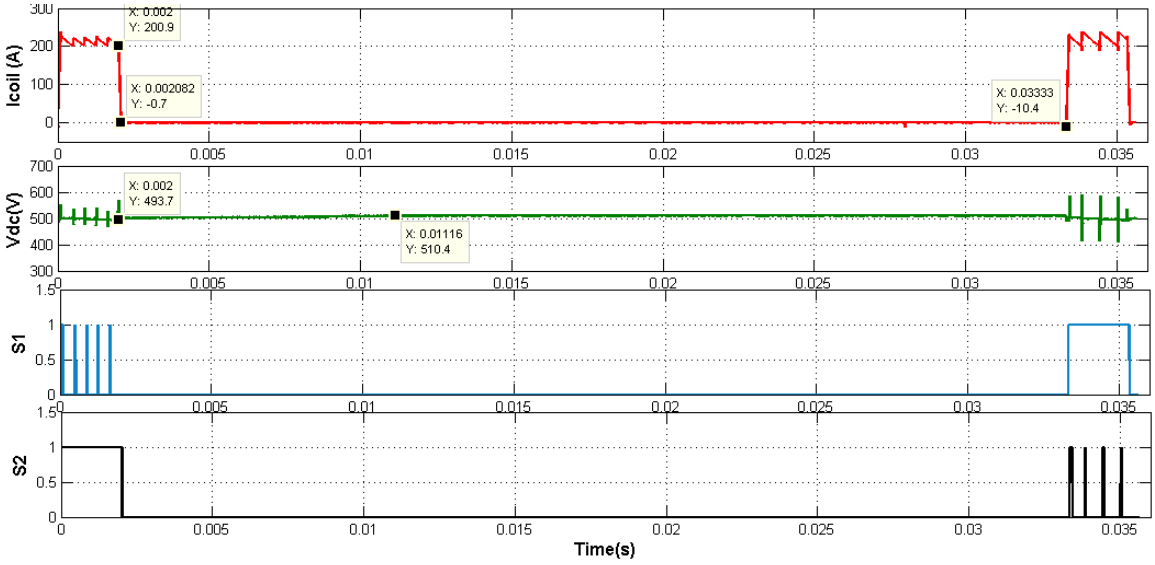



Fig. 4.35 Experimental waveforms- ($V_{dc}$= 500 V, $I_{ref}$ =200 A, ON-Time= 12 µs, Fund. Period = 30 Hz)

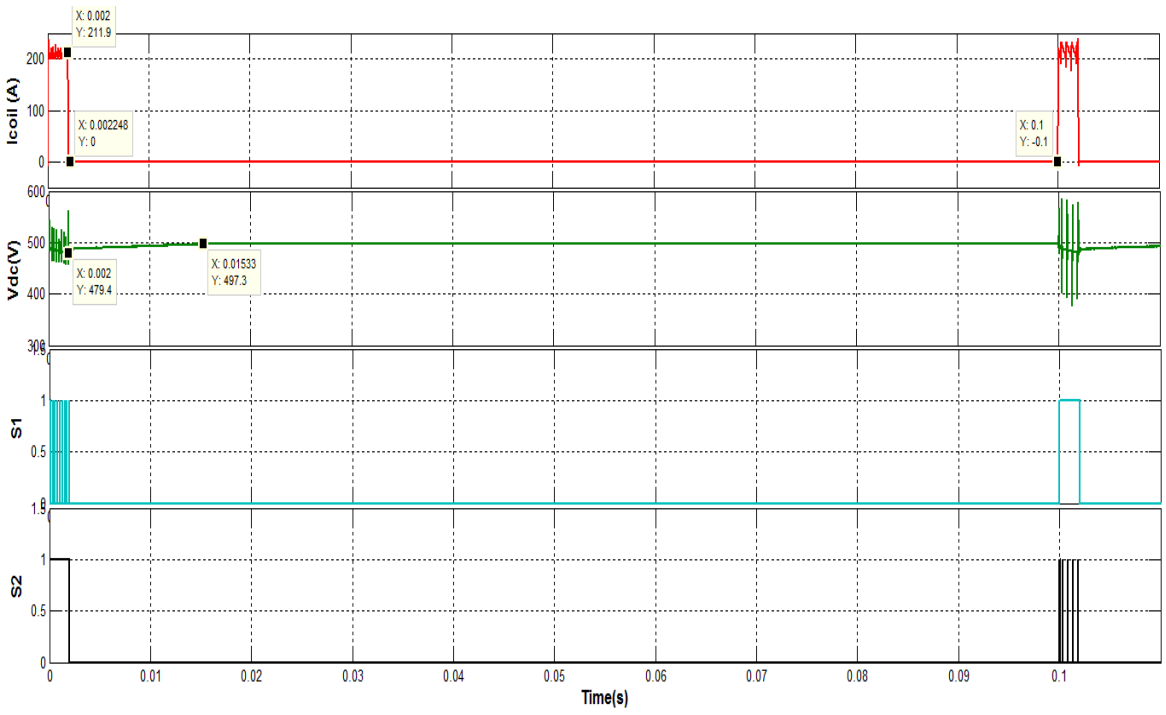
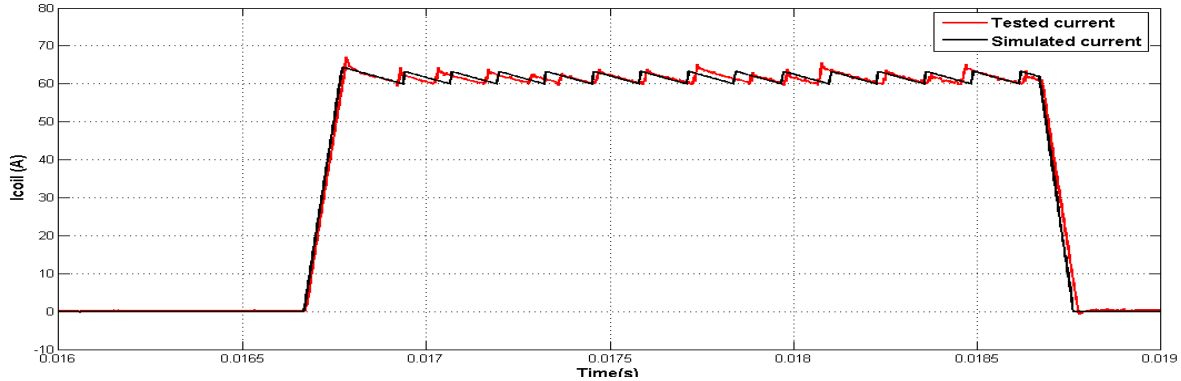



Fig. 4.36 Experimental waveforms- ($V_{dc}$= 500 V, $I_{ref}$ =200 A, ON-Time= 12 µs, Fund. Period = 10Hz)

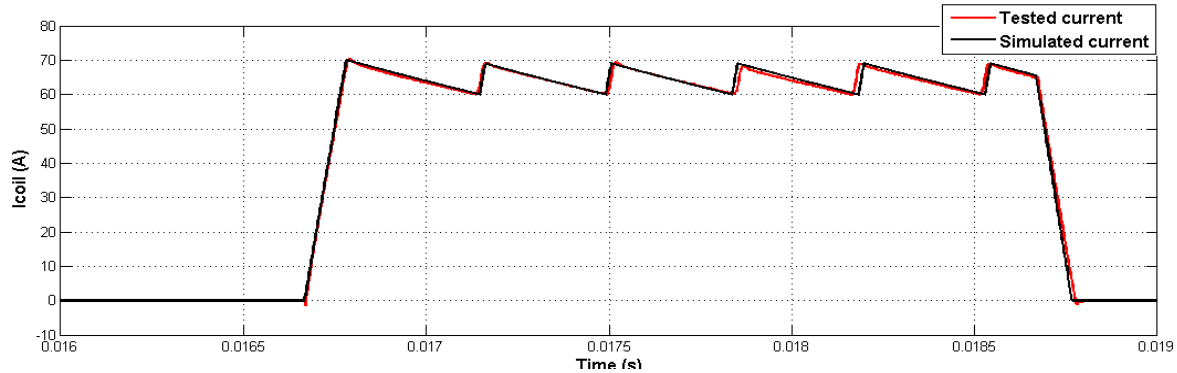
## 4.9 COMPARISON BETWEEN SIMAULTION AND TEST RESULTS

Fig. 4.37 (c) shows the comparison of T-x coil current waveform obtained from MATLAB simulation and the current waveform recorded from actual testing with the experimental setup. There is good agreement between simulation and actual testing results. However there is minor deviation observed in Fig. 4.37(a). The explanation for this deviation can be derived from the fact that in simulation the IGBT and other elements are considered ideal and exactly same current peak is achieved during each switch commutation. However during actual testing with the experimental setup, the current peaks achieved can be slightly different due to discretization error. This error is due to the conversion of input signals from analogue to digital form. By improving the sampling frequency this

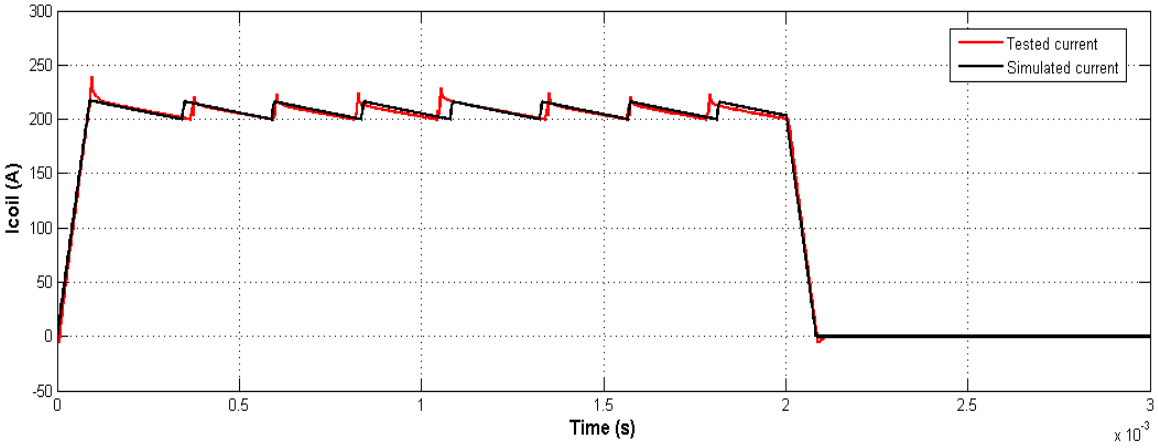
error can be reduced. The offset between actual and tested waveforms is more evident in case of Fig.4.37 (a) due to large number of switch commutations.



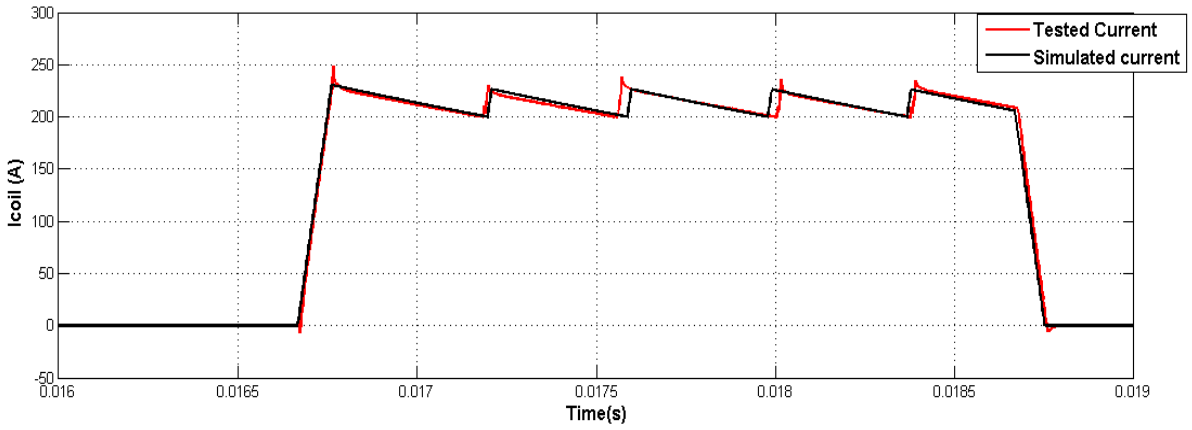

(a)




(b)




(c)




(d)

Fig. 4.37 Comparison of simulation and test current waveforms

(a) $V_{dc}$ =125 V,$I_{ref}$ = 60 A ,ON-Time = 4 µs, (b) $V_{dc}$ =125 V,$I_{ref}$ = 60A ,ON-Time = 16 µs

(c) $V_{dc}$ =500 V, $I_{ref}$ = 200 A, ON-Time = 4 µs, (d) $V_{dc}$ =500 V, $I_{ref}$ = 200A, ON-Time = 12 µs

## 4.10 CONCLUSION

In this chapter, an introduction is presented for the hardware and software components used to implement the converter and current control scheme. CompactRIO architecture is discussed in detail, providing insight to its subsystems. Code optimization steps were instrumental in achieving the lowest possible sampling time. The pull-down resistors were used as an effective solution to achieve fast transition from high to low logic output for digital output module. The experimental results presented in last section are in good agreement with the simulation results, reinforcing the effectiveness of the system design.

# CHAPTER 5. ZERO CURRENT SWITCHING CONVERTER DESIGN

## 5.1 INTRODUCTION

All IGBT based converter topologies involve two basic types of power losses i.e. conduction losses and the switching losses. Conduction losses mainly depend on the current passing through a switch, ON state voltage drop and the conduction time. Switching losses are the losses incurred due to the current and voltage transitions across the IGBT at the time of turn ON and turn OFF process. The switching losses mainly depend on the current and voltage magnitude, the turn ON and turn OFF speed of the IGBT and the switching frequency. At high switching frequencies the switching losses are generally higher than the conduction losses. In order to reduce the overall power loss in the IGBTs, soft switching techniques are widely used [27]. Although there are variety of configurations used in soft switching techniques, but most basic techniques are Zero Current Switching (ZCS) and Zero Voltage Switching (ZVS).

## 5.2 NEED FOR SOFT SWITCHING

Soft switching is basically used in power converters to reduce the switching losses in power converters. Before selecting a soft switching technique for the hard switching converter, it is important to calculate the conduction and switching losses in the hard switching converter. The power loss is mainly calculated for the switches and the diodes. Power loss in other components remain essentially constant and is not considered in these calculations. Previous literature [28] [29] show the method for calculation of IGBT power loss using datasheet parameters.

Turn-ON and Turn –OFF gate resistors have great effect on the switching speed of the IGBT. Hence it is important to calculate the accurate Turn-ON and Turn –OFF resistor values. The calculation of gate resistor is shown in Appendix A-1.The detailed power loss calculations for the hard switching are shown in Appendix A -2. It can be observed that by switch S1 switching power loss is 37% of the total power loss and an effective soft switching scheme can minimize these losses. Hence, the implementation of soft switching converter will help in reduction in power loss and the size of heat sinks can be reduced.

## 5.3 SELECTION BETWEEN ZCS AND ZVS

Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) techniques reduce the switching power loss by bringing the voltage and/ or current across the switch to zero at the time of commutation from ON to OFF state and vice versa. The basic requirement for ZVS is that the switch OFF period should correspond to the resonant half cycle time period of the circuit. On the other hand, in the case of ZCS, switch ON period should correspond to the resonant half cycle time period of the circuit. In the proposed topology due to sharp rise in current during ON period and slow decay of current during OFF period, a relatively shorter ON time period than OFF time period is expected. Also the resonance half period is given by

$$Tr = \frac{\sqrt{Lr*Cr}}{2} \tag{5.1}$$

Where $L_r$= Resonance Inductor and $C_r$ = Resonance Capacitor

As per equation (5.1), use of ZVS needs bigger resonance elements in order to meet the soft switching requirements, however on other side ZCS can be implemented with smaller

resonance elements as resonance half period correspond to the ON time period. Hence in this work, ZCS is preferred choice for soft switching operation of the proposed converter.

## 5.4 ZCS SOFT SWITCHING CONVERTER TOPOLOGY

The current control for the converter operation is achieved by keeping one of the switch ON for the period of current pulse and the other switch commutates at high frequency. The circuit behavior during these modes is similar to a buck converter operation. Hence the zero current switching techniques developed for buck converters [31] can be utilized. To achieve zero current switching, an inductor is placed in series with the switch and a capacitor is placed in parallel with the freewheeling diode FWD1 as shown in Fig. 5.1.

To implement the soft switching, only one switch operation is considered where switch S1 operates at high frequency and switch S2 remains closed for the time of Pulse Width (2ms). Also if the ZCS is implemented, the need for alternate switch operation is eliminated as the thermal stress on the switches will come down.

Fig. 5.1 (a) shows the proposed converter with zero current switching. In a simple zero current switching topology, a resonant inductor is placed in series with the switch and a resonant capacitor is placed in parallel to the freewheeling diode (as shown in Fig.5.1 (a))

### 5.4.1 MODES OF OPERATION (SOFT SWITCHING)

With soft switching (ZCS), the converter modes of operation during constant ON -Time control is shown in Figure 5.1(b) to 5.1(f) and the corresponding waveforms are shown in Fig. 5.2. To discuss the following modes of operations it is considered that the current

through the coil is already established to the reference peak value. Also to explain the soft switching operation, case 1 is considered where switch S1 commutates at high frequency. Before start of the Mode-1, it is considered that the current through the coil is already established to the reference peak value, and the coil current is freewheeling through freewheeling diode FWD1 and switch S2.

**Mode-1 (t1< t ≤ t2):** This mode starts with the closing of switch S1 at time t1. And corresponding circuit state is shown in Fig. 5.1 (b). The current through the inductor current starts increasing from 0 to reference coil current. Till t2, the inductor current is less than the coil current and due to current conduction by the freewheeling diode FWD1, the voltage across resonant capacitor $C_r$ is clamped to zero.

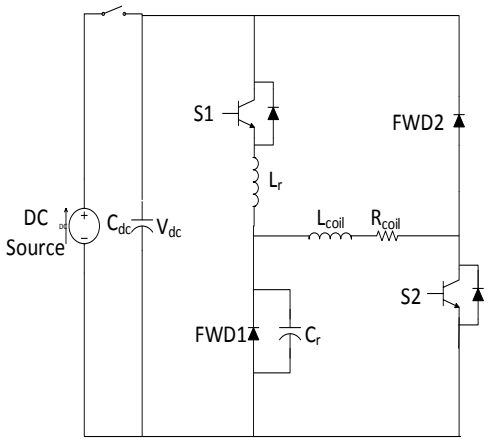
**Mode-2(t2< t ≤ t3):** At t2, the resonant inductor current becomes equal to the reference coil current and at this point freewheeling diode FWD1 opens. This marks the beginning of resonance between the inductor $L_r$ and capacitor $C_r$. By considering the design criteria in the following section, it can be assured that the inductor current swings back to zero at time t3.

**Mode- 3(t3< t ≤ t5)**: At t3, inductor current reverses the direction and this reverse current starts flowing through the antiparallel diode of switch S1. At time t3, switch S1 is naturally commutated and gating signal can be removed from the switch anywhere between time t3 to time t5. For the period t3 to t5, the current through the resonant inductor is in reverse direction. During this period, the current through the switch S1 is zero and the voltage across the switch is clamped to zero. A zero current and zero voltage condition is

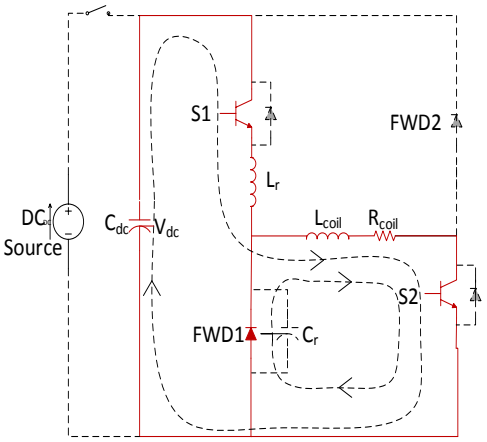
created at the turn OFF of the switch S1. At t5, the current through diode goes to zero and cannot reverse direction as the gating signal for switch S1 is already removed. This marks the end of mode 3.

**Mode - 4(t5< t ≤ t6):** At time t5 inductor current is zero but there is still some positive voltage across resonant capacitor $C_r$. The coil current flows through the capacitor discharging it linearly to zero voltage at time t6.

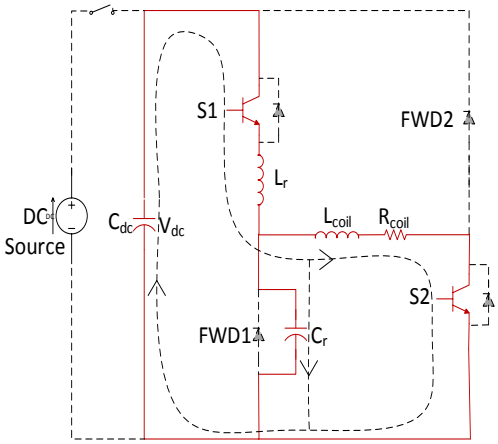
**Mode- 5(t > t6):** Beyond t6, the freewheeling diode FWD1, is forward biased and starts carrying the coil current. In this phase zero voltage is applied across the transmitter coil. So the current starts decreasing due to the resistance of the elements in the current path until the reference coil current is reached. At this point, the switch S1 is closed at zero current and the mode -1 through mode -5 are repeated.



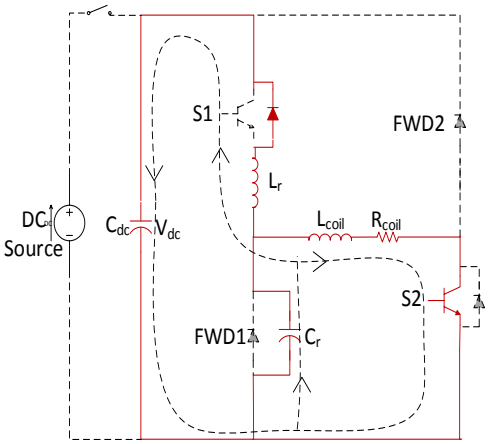

(a) Proposed Soft Switching Topology



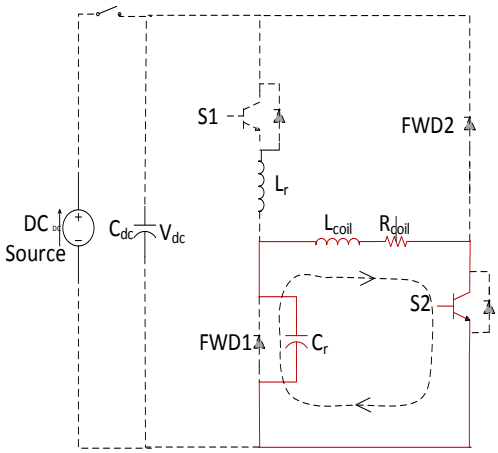

(b) Mode-1



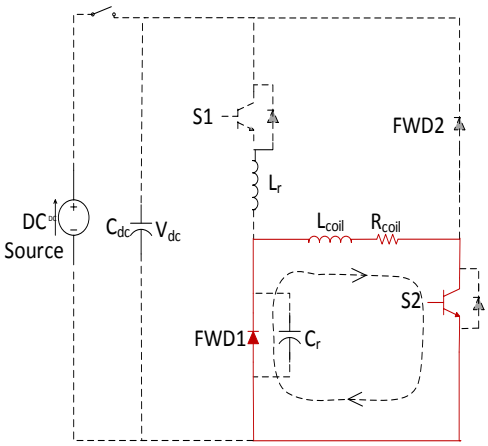

(c) Mode-2




(d) Mode-3




(e) Mode-4




(f) Mode-5

Fig. 5.1 Proposed Topology & Modes of Operation (Soft Switching)

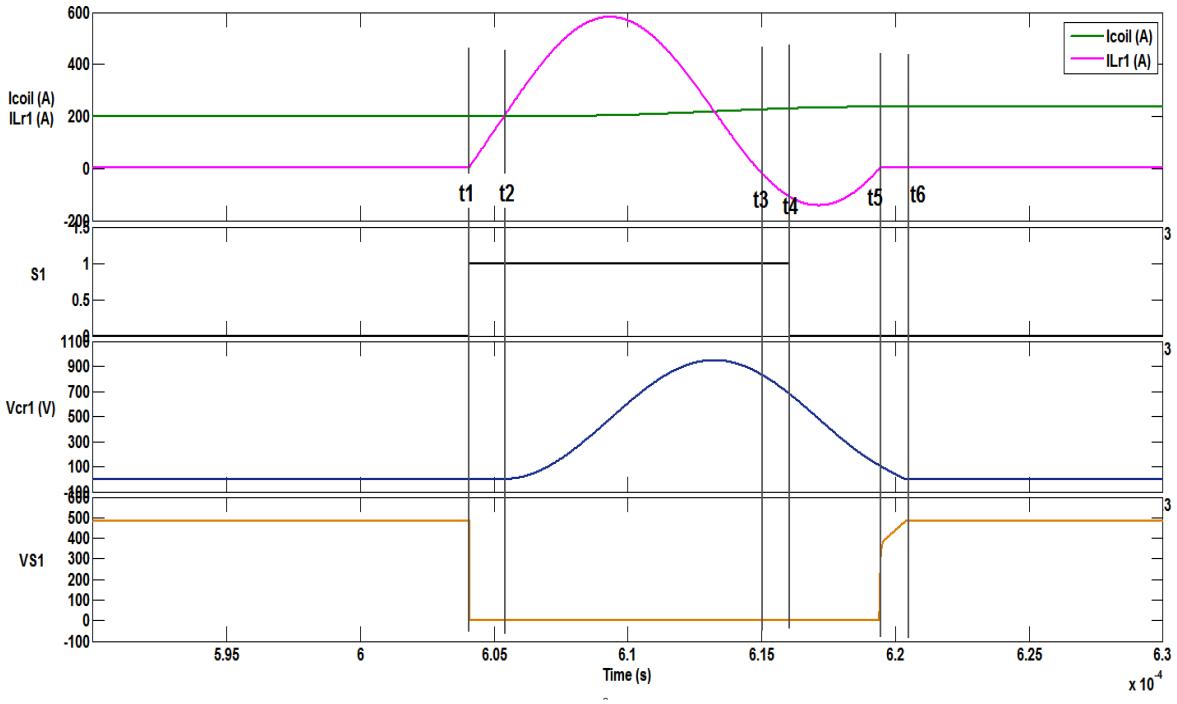



Fig. 5.2 Soft Switching waveforms with zero current switching

### 5.4.2 STATE PLANE TRAJECTORY AND DESIGN CRITERIA FOR ZCS

Prior to determining the value of the resonant elements for the soft switching operation, there is a need to define the design criteria to select the resonant elements. The operation of the converter is analyzed by using the state plane diagram shown in Fig. 5.3 [30].

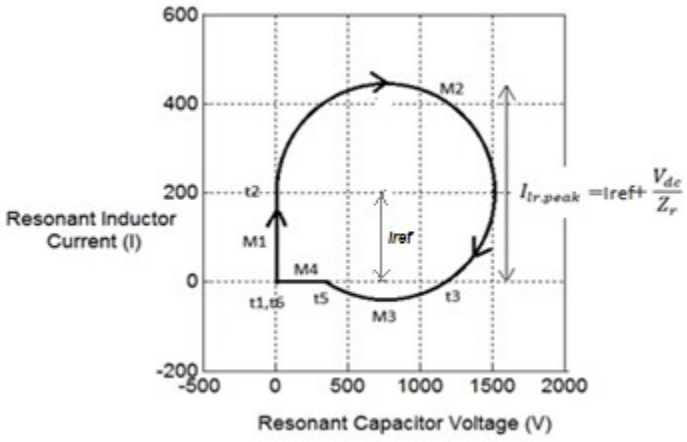



Fig. 5.3 State Plane Trajectory

The equations for inductor voltage and capacitor current for various modes are given as

**Mode1:** In this mode, Inductor current increases linearly from zero to the reference coil current value. Following relationship relates the DC bus voltage with the rate of change of current through the resonant inductor [31].

$$V_{dc} = L_r \frac{I_{ref}}{t_2 - t_1} \tag{5.2}$$

Rearranging equation (5.2),

$$T_a = t_2 - t_1 = L_r \frac{I_{ref}}{V_{dc}} \tag{5.3}$$

$T_a$ represents the initial rise time for the current through the resonant inductor

**Mode2:** In mode 2, inductor $L_r$ and capacitor $C_r$ resonates. During resonance, The Instantaneous resonant inductor current is given by [31]

$$i_{Lr} = I_{ref} + \frac{V_{dc}}{Z_r} \sin(\omega_r t) \tag{5.4}$$

Where $I_{ref}$ = Reference coil current

$V_{dc}$ = DC bus Capacitor voltage

$$Z_r = \sqrt{\frac{L_r}{C_r}}$$

$$\omega_r = \frac{1}{\sqrt{L_r C_r}}$$

And instantaneous capacitor voltage is given by [31]

$$v_{cr} = V_{dc} \left(1 - \cos(\omega_r t)\right) \tag{5.5}$$

From Fig. 5.3 it can be seen that the mode2 ends when the inductor current reaches 0A. Putting $i_{Lr}$=0, in equation (5.4), [31]

$$T_b = t_3 - t_2 = \frac{\pi + \sin^{-1}\left(\frac{I_{ref} Z_r}{V_{dc}}\right)}{\omega_r} \tag{5.6}$$

**Mode3:** In mode 3, the inductor current flows through antiparallel diode and time $t_5$-$t_2$ is given by [31]

$$T_c = t_5 - t_2 = \frac{2\pi - \sin^{-1}\left(\frac{I_{ref} Z_r}{V_{dc}}\right)}{\omega_r} \tag{5.7}$$

**Mode 4:** In this mode, the resonant capacitor discharges linearly and the time for this mode $t_6$ –$t_5$ is given by [31]

$$T_d = t_6 - t_5 = C_r \frac{V_{dc}\left(1 - \cos\left(\sin^{-1}\left(\frac{I_{ref} Z_r}{V_{dc}}\right)\right)\right)}{I_{ref}} \tag{5.8}$$

The major design criteria that should be met for an optimized design is as follows

1. The resonant inductor $L_r$ and resonant capacitor $C_r$ shall be selected in a way that the instant at which the gating signal is removed from the switch, occurs when the antiparallel diode is conducting the reverse current.
2. The average value of coil current $I_{ref}$ must be less than the state space circle radius i.e. $\frac{V_{dc}}{\mathrm{Zr}}$.

   In other words, the condition $Z_r < \frac{V_{dc}}{I_{\mathrm{ref}}}$ shall be satisfied to bring the switch current to zero during each cycle.

   Here $Z_r = \sqrt{\frac{L_r}{C_r}}$,

$L_r$ = Resonant Inductor and $C_r$ = Resonant Capacitor

3. The peak value of current through the resonant inductor and switch is given by

$$I_{Lr,peak} = I_{ref} + \frac{V_{dc}}{Z_r} \quad (5.9)$$

Here in order to keep the $I_{Lr,peak}$ to a minimum value, the resonant impedance $Z_r$ shall be kept maximum possible (in accordance with criteria 2)

### 5.4.3 DESIGN CALCULATIONS

To design $L_r$ and $C_r$, high voltage ($V_{dc}$ =500V) and high current ($I_{coil}$=200A) was considered.

The ON period for the switch is selected as 12µs.

As per the design criteria discussed in previous section,

$$T_a + T_b \leq 12\ \mu s \leq T_a + T_c \quad (5.10)$$

Also, within one pulse operation, the DC bus voltage is subject to decrease due to losses in the circuit. In case of hysteresis current control, with decrease in DC bus voltage the rate of rise of coil current is effected resulting in variable ON time for the switch. However in case of Constant ON- Time control, ON –Time for the switch is independent of the DC bus voltage magnitude. Hence the designed value of resonant elements $L_r$ and $C_r$ provides effective soft switching. To select the rating for $L_r$ and $C_r$, one of the element rating is fixed and then the value of other element is calculated using the above stated equations so that the design criteria is fulfilled. An iterative approach was followed to reach at the final values of $L_r$ and $C_r$, while adhering to the design criteria.

Now as per design criteria for ZCS, $Z_r < \frac{V_{dc}}{I_{ref}}$ = 2.5

$Z_r$ equal to 2.5 is a boundary condition and it implies that $T_b = T_c$. There will be only one instant at which current through the switch is zero. On the other hand if $Z_r$ is less than 2.5 a time period "$T_c$-$T_b$" is achieved where the current through the switch is zero. Also, $Z_r$ can't be too low as it will result in very high current peaks through the switch and resonant inductor as per equation (5.9).

Hence a $Z_r$ = 1.8 was considered to be a reasonably good value for this design.

To start $C_r$ =1.2 µF was considered and by putting value of $C_r$ in following expression, $L_r$ is calculated

$$\sqrt{\frac{L_r}{C_r}} = 1.8$$

$L_r$ = 3.9 µF

Putting $L_r$ =3.9 µH, $C_r$ = 1.2 µF, $Z_r$ =1.8, $\omega_r$ = 4.62x$10^5$ rad/s, in Equation (5.3), (5.6), (5.7), (5.8) and (5.9) Ta = 1.56 µs, $T_b$= 8.54 µs, $T_c$ = 11.9 µs

$T_a + T_b$ = 10.1 µs and $T_a + T_c$ = 13.46 µs

The complete design summary is given in Table 5-1

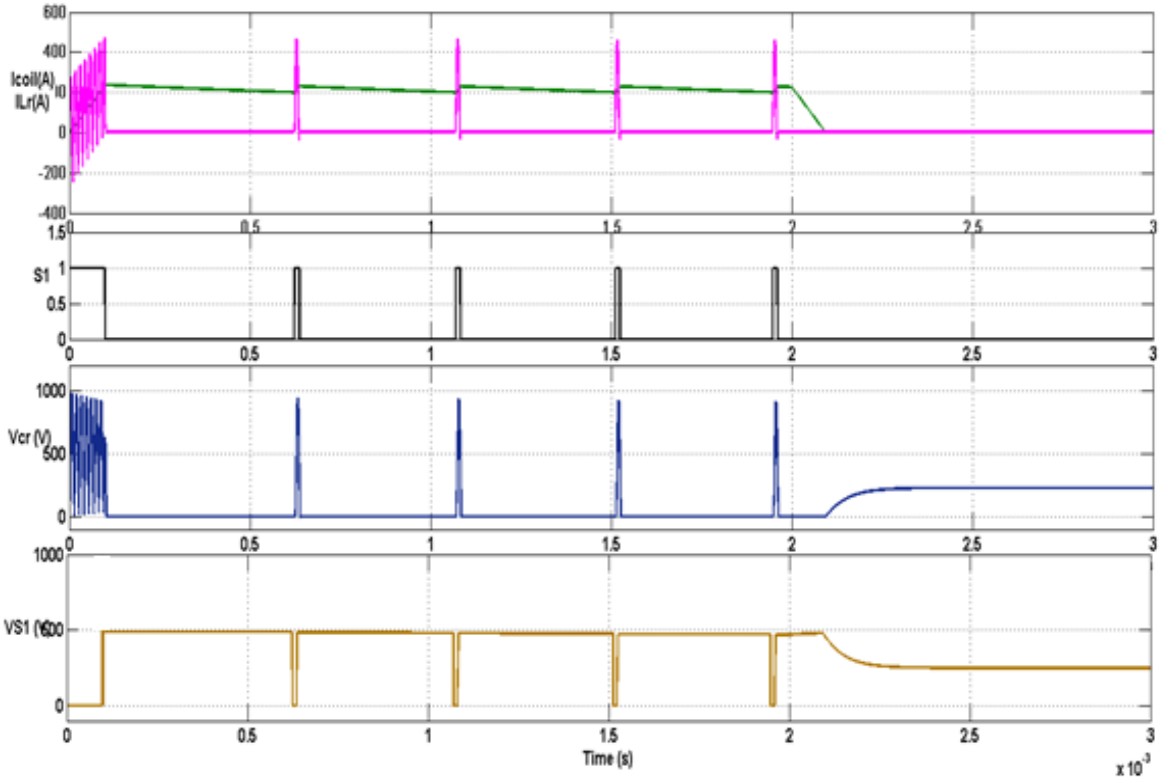
Table 5-1 ZCS Design Summary

| Parameter | Value |
|---|---|
| $V_{dc}$ | 500 V |
| $I_{ref}$ | 200 A |
| $T_{ON}$ | 12 µs |
| $L_r$ | 3.9 µH |
| $C_r$ | 1.2 µF |
| $Z_r$ | 1.8 |
| $T_a + T_b$ | 10.1 µs |
| $T_a + T_c$ | 13.46 µs |
| $I_{Lr,peak}$ | 481A |
| $V_{Cr,peak}$ | 1000V |

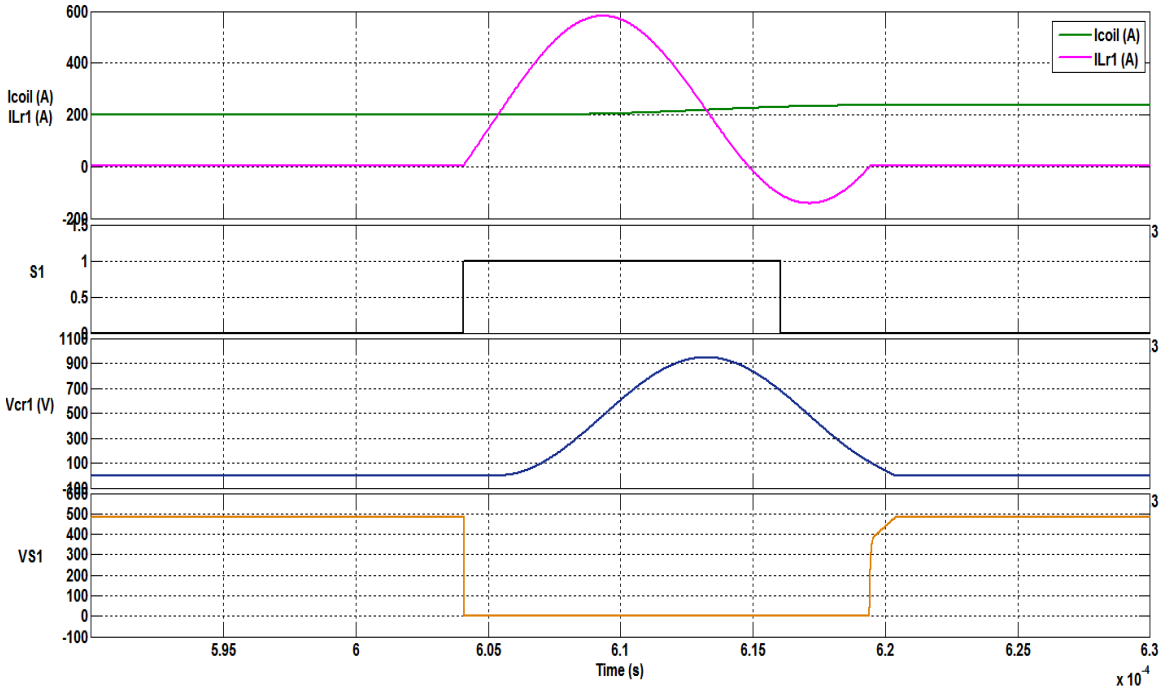
### 5.4.4 SIMULATION RESULTS

To validate the design for zero current switching scheme, converter operation was simulated in MATLAB Simulink. Fig. 5.4 shows the voltage and current waveforms for the soft switching converter. Fig. 5.4 (a) presents the current and voltage waveforms for one current pulse cycle. Here $I_{Lr}$ is the current through resonant inductor, $V_{cr}$ is the voltage across resonant capacitor and $V_{s1}$ is the voltage across switch S1. Fig. 5.4 (b) presents a magnified view for switching cycle of switch S1. It can be clearly observed that the gating signal of switch S1 goes from low state to high state when zero current is passing through the switch. Resonant inductor current rises linearly from 0A to 200A and rises beyond 200A due to resonance between resonant inductor and resonant capacitor. Peak

resonant inductor current is around 480A which is in accordance with the design calculations presented in section 5.3.2. Gate pulse for switch S1 goes from high to low after preset ON Time of 12 µs .At this moment, the negative inductor current is carried by IGBT antiparallel diode and IGBT is turned ON at zero current. Hence zero current switching is achieved for switch S1 resulting in lower power loss.




(a)




(b)

Fig. 5.4 Simulation waveforms with ZCS (Vdc= 500V, Iref =200A, ON-Time= 12µs)

(a) One pulse cycle (b) One switching commutation

## 5.5 CONCLUSION

A zero current switching topology is proposed for reducing the switching power loss in the proposed hard switching converter presented in chapter 3 and chapter 4. The soft switching converter operation is discussed in detail by describing the operating modes. The current, voltage and timing governing equations are described based on state plane diagram. The procedure followed to design the resonant elements while complying with the design criteria is presented in detail. The simulation analysis performed in MATLAB Simulink confirmed the effectiveness of the soft switching design scheme.

# CHAPTER 6. CONCLUSION AND FUTURE WORK

## 6.1 SUMMARY

The thesis describes the design and implementation of a high power converter topology to provide high current pulses in a time domain electromagnetic system. The proposed system is designed with an objective to develop a compact yet high power system, capable of controlling the current pulse through the transmitter coil (Tx- coil).

A LabVIEW based CompactRIO hardware platform was implemented to achieve a faster digital current control. A constant ON-Time current control concept is devised and implemented to achieve better control on switch ON times and to have better current regulation. Current fall time less than 100 µs was achieved with a sampling frequency of 500 kHz. The short fall times and high current magnitude achieved are important to achieve higher secondary field response from the mineral target.

Code optimization techniques, are described in detail which were instrumental in reducing the sampling time to 2 µs. Also high sampling frequency achieved helps to improve the accuracy and resolution of the survey data, providing more data points per fundamental period. The development of graphical user interface on the host computer provides the user with the flexibility to control various parameters such as pulse width and fundamental frequency of the current pulse.

The simulation and experimental results proved the effectiveness of the proposed system and the current control scheme. In the end, a zero current switching scheme is proposed to reduce the switching power loss in the power converter. The design approach for

selecting the resonant elements was presented in detail. The simulated results proved the effectiveness of the proposed soft switching scheme and verified the design of resonant elements.

## 6.2 SUGGESTED FUTURE WORK

1. In this work only unipolar current pulses were implemented. In the next level of development, bipolar current pulses can be implemented using full bridge converter. Bipolar current pulses provides the benefit of automatic noise cancellation during the post processing of the recorded secondary signal.
2. Extension of the control logic in LabVIEW to capture receiver (Rx-coil) response along with survey GPS data with a provision to capture data in selected time windows.
3. Implementation of zero current switching and practical efficiency comparison for hard switching and soft switching operation.
4. The presented system was tested on ground with power supply from the utility source. However final implementation on a helicopter demands a use of battery source or a diesel generator. Instead, a boost power supply can be designed to step up the helicopter power supply voltage (28 VDC) to feed the power converter.
5. Different survey applications in future may need different current waveforms. The converter control logic can be developed to provide the selection of different current waveforms of triangular, trapezoidal, cosine and half sine wave shape within the scope of same hardware.

6. In this work the DC power supply output voltage magnitude was controlled using a manual interface. The control logic in LabVIEW can be extended to achieve a digital control of the DC power supply.

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# APPENDIX

## A-1 CALCULATION OF TURN ON AND TURN OFF GATE RESISTORS

From Semix IGBT module technical explanation document [18], Fig. A.1, represents the gate resistor connections for the Semix IGBT module.

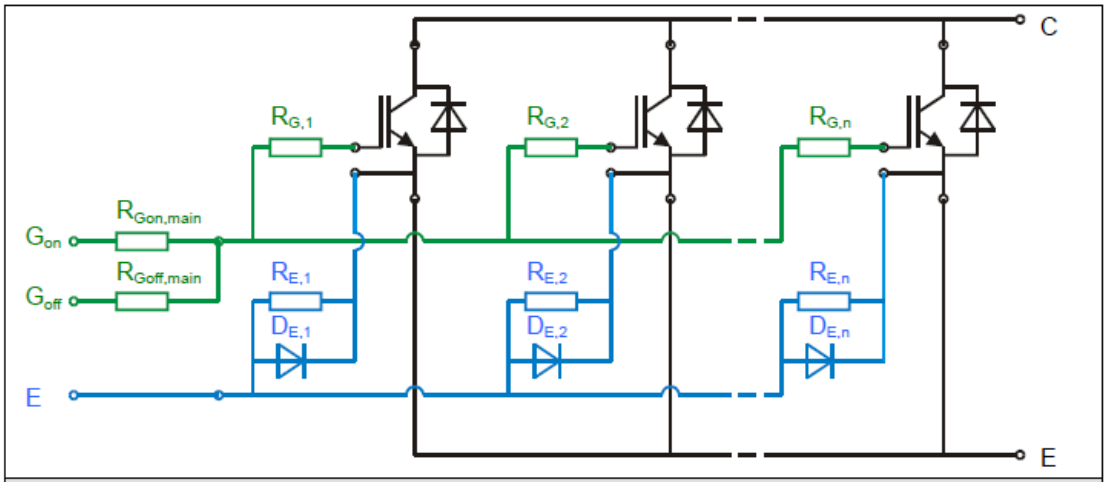


Fig. A.1 Semix IGBT module gating circuit

There are 4 parallel IGBT switches in high current Semix IGBT module and gate turn- ON and turn- OFF resistance is calculated as

$$R_{G,on} = R_{Gon,main} + \frac{1}{\frac{1}{R_{G,1}+R_{E,1}} + \frac{1}{R_{G,2}+R_{E,2}} + \frac{1}{R_{G,3}+R_{E,3}} + \frac{1}{R_{G,4}+R_{E,4}}} \quad \text{(A.1)}$$

$$R_{G,off} = R_{Goff,main} + \frac{1}{\frac{1}{R_{G,1}+R_{E,1}} + \frac{1}{R_{G,2}+R_{E,2}} + \frac{1}{R_{G,3}+R_{E,3}} + \frac{1}{R_{G,4}+R_{E,4}}} \quad \text{(A.2)}$$

Here as per datasheet values , $R_{G,on,main}$ = 1.3Ω, $R_{G,off,main}$ = 6.5Ω, $R_G$= 2.4Ω and $R_E$= 0.5 Ω

Putting these values in equation (A.1) and (A.2)

**$R_{G,on}$ = 2.025 Ω and $R_{G,off}$ = 7.225 Ω**

## A-2 POWER LOSS CALCULATION

**SWITCHING POWER LOSS:** Manufacturer datasheet parameters are used to evaluate the switching loss of the IGBT and the diodes [28] [29]

**Switching power loss in the IGBT:**

The switching power loss of the IGBT is given by

$$P_{switch} = \left(E_{on} + E_{off}\right) * f_{sw} \quad \text{(A-3)}$$

Where $E_{on}$ = the switch turn ON energy loss

$E_{off}$ = switch turn OFF energy loss

$f_{sw}$ = switching frequency (switch S1)

From the plot of switching loss vs collector current, the turn on and turn off energy loss can be found at particular collector current. To measure the losses accurately the plots were reproduced in the Microsoft Excel and the energy loss corresponding to particular current was measured using curve fitting feature of Microsoft excel.

Fig A.2 Shows the $E_{on}$ and $E_{off}$ curves vs $I_c$ at Tmax for the Semix604GAL12E4s IGBT module.

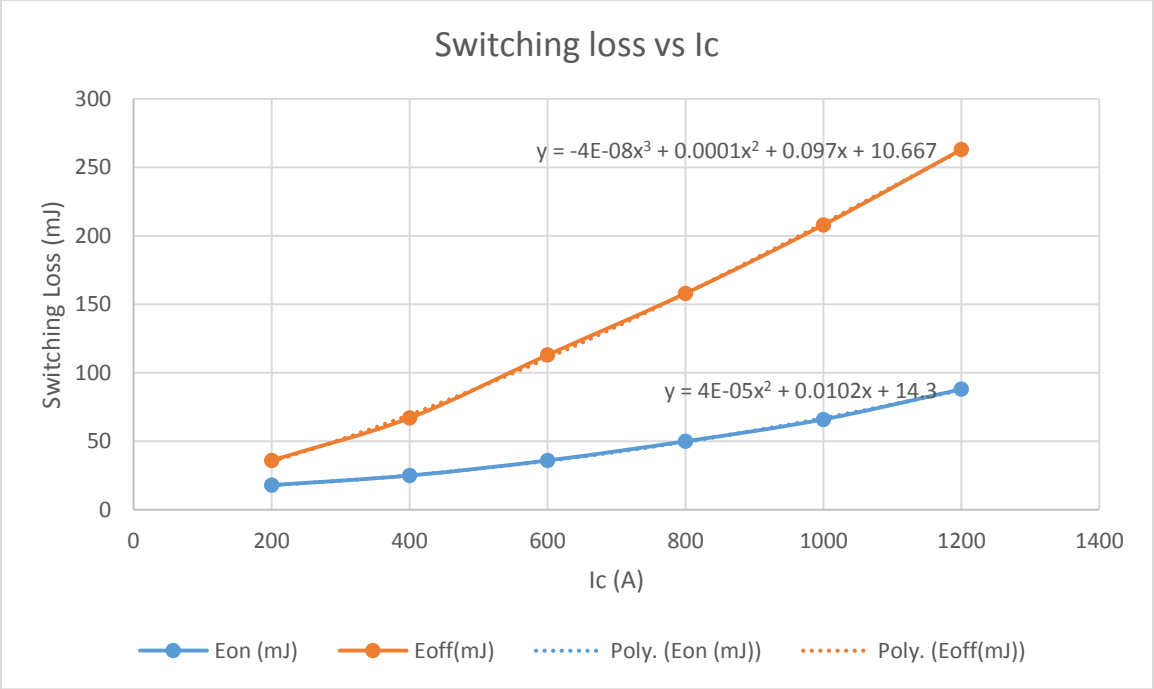


Fig. A.2 Switching loss versus collector current

Table A-1 Test Parameters - Switching loss versus collector current

| Fixed Test Parameters | | | | |
|---|---|---|---|---|
| $T_j$ (C) | $V_{cc}$(V) | $V_{GE}$ (V) | $R_{Gon}$ (Ω) | $R_{Goff}$ (Ω) |
| 150 | 600 | ±15 | 1.7 | 6.9 |

If the gate resistor of the user gate drive resistor is different than the one used to obtain the above energy loss plot (Table A-1), a correction factor must be used. In Fig A.3.

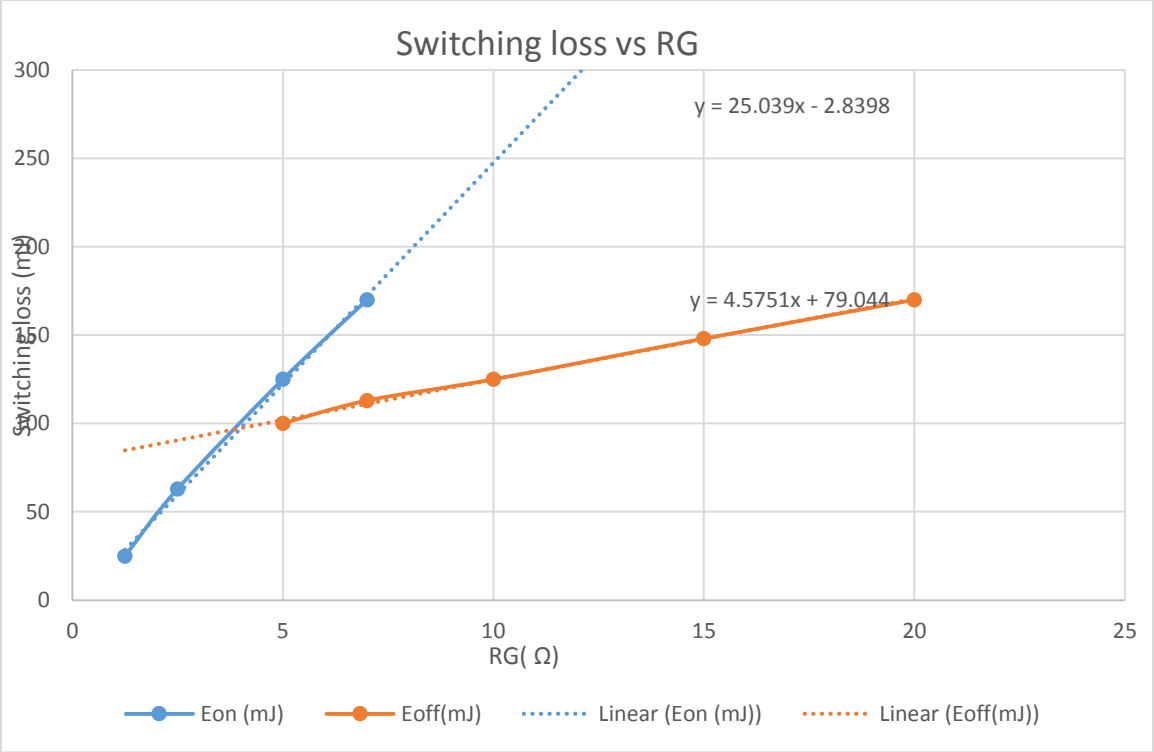


Fig. A.3 Switching loss versus Gate resistor

Table A-2 Test Parameters- Switching loss versus Gate resistor

| Fixed Test Parameters | | | |
|---|---|---|---|
| $T_j$ (C) | $V_{cc}$(V) | $V_{GE}$ (V) | $I_c$ (A) |
| 150 | 600 | ±15 | 600A |

Since the switching energy is proportional to voltage, the result is scaled by ratio of the actual circuit voltage to the test voltage in the datasheet.

$$\mathrm{E_{on}} = \left(A_{on}.{I_c}^3 + B_{on}.{I_c}^2 + C_{on}.I_c + D_{on}\right).\frac{E_{on\ (R_{G,user\ specific})}}{E_{on\ (R_{G,datasheet})}}.\frac{V_{dc,user\ specific}}{V_{dc,datasheet}} \quad \text{(A.4)}$$

$$\mathrm{E_{off}} = \left(A_{off}.{I_c}^2 + B_{off}.I_c + C_{off}\right).\frac{E_{off\ (R_{G,user\ specific})}}{E_{off\ (R_{G,datasheet})}}.\frac{V_{dc,user\ specific}}{V_{dc,datasheet}} \qquad \text{(A.5)}$$

Here constants A,B,C and D for turn ON and turn OFF cases are shown in Fig A.2.

Also $R_{Gon,\ user\ specific}$ = 2.025 Ω, $R_{Gon,\ datasheet}$ = 1.7 Ω, $R_{Goff,\ user\ specific}$ = 7.225 Ω

$R_{Goff,\ datasheet}$ = 6.9 Ω, $V_{dc,\ user\ specific}$ = 500V and $V_{dc\ datasheet}$ = 600V

For switch S1, $V_{dc}$= 500V and $I_c$ = 200A, $f_{sw}$ = 5000

But in the actual waveform implementation the pulse width is 2ms followed by an off period or zero current recording period of 15ms such that the overall current waveform frequency is 60Hz.

So the total power loss is multiplied by the duty cycle of the current waveform which is

$$\mathrm{D} = \frac{\mathrm{Ton}}{\mathrm{Ts}} = \frac{2\mathrm{ms}}{16.67\mathrm{ms}}$$

$$\mathrm{P_{switch}} = (\mathrm{E_{on}} + \mathrm{E_{off}}) * \mathrm{f_{sw}} * \mathrm{D} \qquad \text{(A.6)}$$

For switch 2 the switching frequency is 60Hz. Also for switch S2, D=1.

Putting above calculated parameters for Switch S1 and Switch S2,

$P_{ssw1}$ = 27.9 W and $P_{ssw2}$= 2.8 W

**Switching power loss in antiparallel diodes:** In hard switching the diodes in antiparallel to the IGBTs does not conduct the current at any time of the fundamental period

therefore there are no switching or conduction losses associated with the antiparallel diodes.

**Switching power loss in freewheeling diode:**

Turn on energy of the diode is given by, $E_{on} = \frac{1}{4} * Q_{rr} * U_{dr}$ (A.7)

Where $U_{dr} = V_{dc} = 500$

And $Q_{rr}$ = Diode reverse recovery charge (from datasheet) = 100 µC

And Power loss = $P_{on} = E_{on} * f_{sw} * D = 0.0125*5000*0.12 = 7.5$ W

The turn off losses in the diode are generally small and is neglected

Therefore diode switching power loss = $P_{sfwd1} = 7.5$ W

Switching loss for the 2nd freewheeling diode = $P_{sfwd2} = 0.0125*60 = 0.75$W

**CONDUCTION LOSS:**

**Conduction loss in the IGBT:** Fig A.4 represents the collector current versus collector-emitter voltage characteristics for the Semix IGBT.

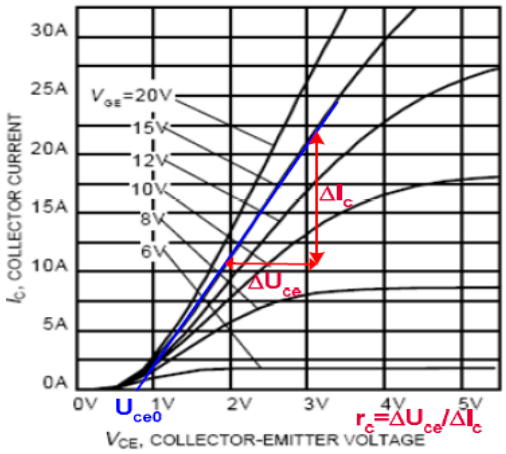


Fig. A.4 Measurement of $U_{ceo}$ and $r_c$

The voltage across the IGBT is given by

$$U_{ce}(I_c) = U_{ce0} + I_c * r_c \tag{A.8}$$

Where $U_{ceo}$ and $r_c$ can be measured from the IGBT datasheet as shown in Fig. A.4

$$U_{ceo} = 0.8\ V \text{ and } r_c = 2.67e\text{-}3\ \Omega$$

Average power is given by

$$P_{csw} = U_{ceo}.I_{av} + r_c.I^2_{rms} \tag{A.9}$$

In case of switch S1, the average collector current is given by.

$$I_{av} = \frac{D * I_0 * P\_width}{T_s} \tag{A.10}$$

Where D = duty cycle of switch S1 = 0.039

$I_o$ is constant load current =200 A

P_width is the pulse width of current waveform =2ms

Ts = Fundamental time period =16.67ms

Therefore by using these values in equation (A.10), $I_{av}$= 0.98 A

$$I_{rms}{}^2 = \frac{D * I_0{}^2 * P\_width^2}{T_s{}^2} \qquad (A.11)$$

$I_{rms}{}^2 = 22.45$

From Fig A.5, $U_{ceo}$= 0.8 V and $r_c$= 2.67e-3 Ω. By putting these values in Equation (A.9)

Pcsw1 = 0.84 W

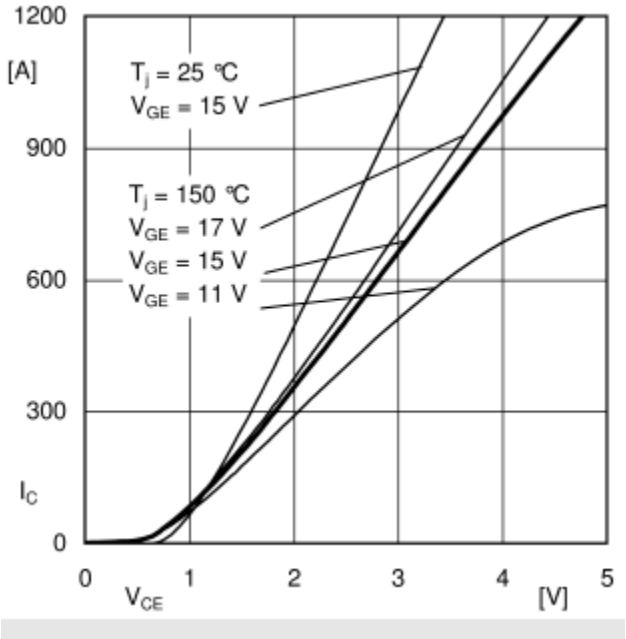


Fig. A.5 $I_c$ versus $V_{ce}$ for Semix IGBT

For switch S2,

$$I_{av} = \frac{I_0 * P\_width}{T_s} \qquad \text{And } I_{rms}{}^2 = \frac{I_0{}^2 * P\_width^2}{T_s{}^2}$$

$I_{av}$ = 23.99 A and $I_{rms}{}^2$ = 575 A

And $P_{csw2}$ = 20.72 W

**Conduction loss in antiparallel diodes:** For antiparallel diodes the conduction loss is zero as they don't conduct in hard switching operation

**Conduction loss in freewheeling diodes:**

The calculation is similar to the conduction loss calculation of IGBTs.

The output characteristics of diode are used to find $U_{ce0}$ and $r_c$

$$I_{av} = \frac{(1 - D) * I_0 * P\_width}{T_s} = 23\ A$$

$${I_{rms}}^2 = \frac{(1 - D) * {I_0}^2 * P\_width^2}{{T_s}^2} = 553.3\ A$$

From Fig. $U_{ceo}$= 0.6 V and $r_c$ =2.65e-3 Ω

Using these values, $P_{cfwd1}$ = 15.26 W

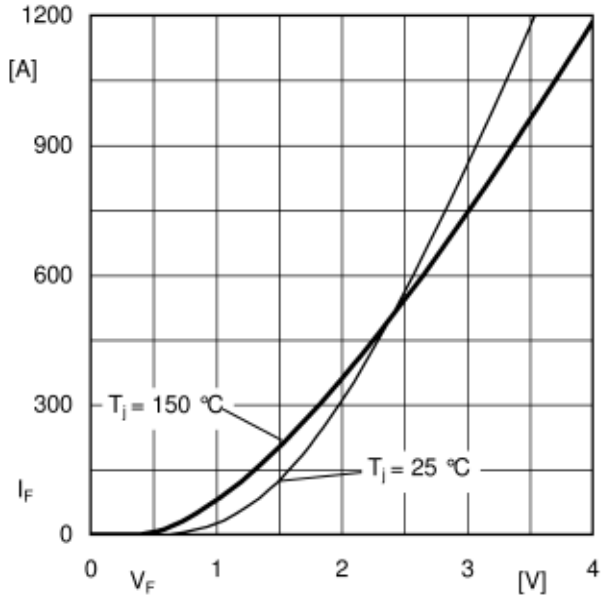


Fig. A.6 $I_c$ versus $V_{ce}$ for Semix Diode

Freewheeling diode 2 conducts the current for very small interval so the conduction power loss of freewheeling diode 2 can be neglected.

Total power loss during hard switching

Table A-3 Summary - Hard Switching Power loss

| Circuit Element | Type of Loss | Value (W) |
|---|---|---|
| Switch S1 | Switching loss | 27.9 |
| | Conduction loss | 0.84 |
| Switch S2 | Switching loss | 2.8 |
| | Conduction loss | 20.72 |
| Antiparallel Diode 1 | Switching loss | 0 |
| | Conduction loss | 0 |
| Antiparallel Diode2 | Switching loss | 0 |
| | Conduction loss | 0 |
| FWD1 | Switching loss | 7.5 |
| | Conduction loss | 15.26 |
| FWD2 | Switching loss | 0.75 |
| | Conduction loss | 0 |
| | **Total Power Loss** | **76** |

Therefore switching power loss of switch S1 makes 37 % of the total converter power loss during hard switching.