THREE-LEVEL NEUTRAL POINT CLAMPED (NPC) TRACTION INVERTER DRIVE FOR ELECTRIC VEHICLES

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ABSTRACT

Three-Level Neutral Point-Clamped (NPC) Traction Inverter Drive for Electric Vehicles

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The motivation of this project was to develop a three level neutral point clamped (NPC) traction inverter for a permanent magnet synchronous machine drive. The three-level inverter helps to reduce the total inverter losses at higher switching frequencies, compared to a two-level inverter for electric vehicle applications. The three-level inverter has also more power switches compared to the two-level inverter. This helps to reduce the voltage stress across the switches and the machine winding. In addition, it also allows an increase in the DC-link voltage, which in turn helps to reduce the DC-link current, phase conductor size and the associated losses. Moreover, at higher DC-bus voltages the power switches will have lower thermal stress when compared to the 2-level. However, the NPC inverter topologies have an inherent problem of DC-link voltage balancing.

In the initial part of this thesis, a novel space vector based DC-link voltage balancing strategy is proposed. This strategy can keep the two DC-link capacitor voltages balanced during transient changes in both speed and torque. The performance of the three-level inverter system is then compared with a two-level inverter based drive to validate its performance improvement. The results showed a significant reduction in total voltage and current harmonic distortions, reduced total inverter losses (by $2/3^{rd}$) and was even was able to keep the neutral point fluctuation low at all operating load power factor conditions.

The second motivation of this thesis was to reduce the computational time in the real-time implementation of the control logic. For this purpose, a modified carrier and hybrid-carrier based PWM strategy was proposed, which also kept the DC-link capacitor voltages balanced. The modified carrier based strategy was able to reduce the switching losses compared to the conventional strategies, while the hybrid-carrier based strategy kept the advantages of both carrier and the space vector techniques.

Finally, a performance comparison study was carried out to compare the total harmonic distortion, switching loss distribution, and total inverter loss of all the four proposed strategies.

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AC	Alternating Current
DC	Direct Current
EV	Electric Vehicle
PWM	Pulse Width Modulation
CPWM	Continuous Pulse Width Modulation
DPWM	Discontinuous Pulse Width Modulation
SPMSM	Surface Permanent Magnet Synchronous Machine
SPWM	Sine Pulse Width Modulation
SV-PWM	Space-Vector Pulse Width Modulation
EMI	Electromagnetic Interference
THD	Total Harmonic Distortion
NPC	Neutral Point Clamp
NPP	Neutral Point Potential
SHE	Selective Harmonic Elimination
CB-PWM	Carrier Based Pulse Width Modulation
NTV/N3V	Nearest Three Vector
SVM	Space Vector Modulation
VSVS	Virtual Space Vector Scheme
NTV^2	Nearest Three Virtual Vector
IPMSM	Interior Permanent Magnet Synchronous Machine
PI	Proportional Integral
M.I.	Modulation Index

IGBT	Insulated Gate Bipolar Transistor
RMS	Root Mean Square
DS-PWM	Double Single Pulse Width Modulation
MTPA	Maximum Torque Per Ampere
NP	Neutral Point
HPWM	Hybrid Pulse Width Modulation
RPM	Revolution Per Minute
CMV	Common Mode Voltage

NOMENCLATURE

v_d, v_q	*d-*, *q-* axis voltages
i_d, i_q	*d-*, *q-* axis currents
φ_d, φ_q	*d-*, *q-* axis flux linkages
ω_e	Electrical speed (rad/sec)
λ	Rotor magnet flux (V.s)
E_{ph}	Back EMF
v_{ph}	Phase voltage
L_d, L_q	*d-*, *q-* axis inductance
P	Machine pole
r_s	Stator resistance
T_e	Electromagnetic torque
I_{inv_avg}	Average inverter current
I_{inv_cap}	DC-link capacitor current
I_{inv_rms}	Inverter RMS current
V_{ref}	Reference phase voltage
m	Modulation index
V_m	Phase voltage peak
V_{dc}	DC-link voltage
T_a, T_b, T_c	Active vector conduction time
T_s	Total switching time
δ	Duty cycle
k	Sharing factor between +ve and –ve redundant vectors

φ	Power factor angle
I_a, I_b, I_c	A, B, C phase currents
φ_{cr}	Critical angle
V_{dc1}, V_{dc2}	Two DC-link capacitor voltages
I_{caprms}	RMS value of capacitor current
I_m	Phase current peak
$V_{capdiff}$	Average capacitor voltage difference
$V_{capupper}$, $V_{caplowerr}$	Two DC-link capacitor voltages
v_{a,b,c_ref}	A, B, C phase reference modulating signals
v_z	Zero sequence voltage
v_{ip}, v_{in}	Modulating signal for three-level inverter switches
i_{np}	Neutral point current
i_a, i_b, i_c	Instantaneous phase currents
δ_{a,b,c_ref}	Duty cycle for three phases
v_o	DC-offset voltage
θ_{re}	Rotor position
P_{c_avg}	Average conduction loss
$P_c(t)$	Instantaneous conduction loss
$P_{sw\_avg\_IGBT/diode}$	Average switching loss for IGBT or Diode
$E_{on/off}$	Turn on or off loss
E	Total switching loss
E_{rr}	Reverse recovery loss for diode
$V_{capdiff}$	Difference between two capacitor voltages

Chapter 1. Introduction

Due to continuous increase in fuel price, reduction in oil reserves and to reduce the air pollution, electric vehicles have become viable solutions. Due to advancement in power electronics and battery technology it is possible to design much advanced electric and hybrid electric vehicles, with improved performance. Also, it is now possible to drive an EV with a range of 480 Km on a single charge [1], [2]. In the past, DC machines were widely used for traction applications, due to simple speed control techniques [3], [4]. However, compared to the AC machines, DC machines have major drawbacks of high rotor inertia, cost, and maintenance issues related to brushes. Due to these disadvantages, modern day traction drives are designed with AC machines. These types of machines have simple mechanical construction and low maintenance cost. However, speed controls for AC machines are not as simple as DC machines. They need special power electronic converters to drive them [5]-[14]. Switch reluctance machines are also attractive solution for electric vehicle applications due to their simple, rugged construction and fault tolerant design of power electronics convectors. However, due to their higher torque ripple and acoustic noise, they are not still preferred for EV applications. However, for high power mining tracks where noise and torque ripple are not of great concern, they could be useful. Fig. 1.1 shows the classification of different types of electric machines available for traction applications.

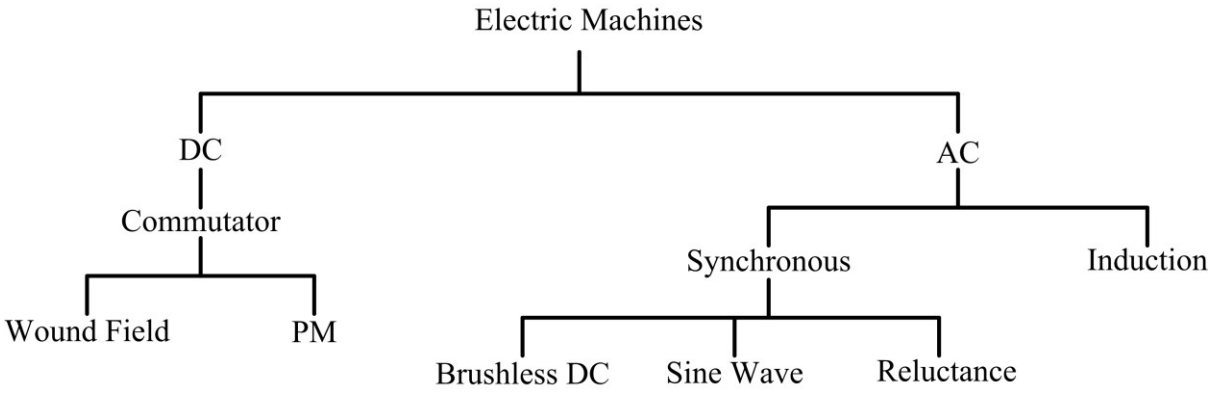


Figure 1.1 Electric machines used for traction applications.

Among all AC machines, both induction and synchronous machines are generally widely used for traction applications. However, permanent magnet synchronous machines (PMSM) are most favourable, due to their high power density magnets, which helps reduce the machine size and weight, compared to the induction machines of the same peak power rating (kW). Due to the presence of permanent magnets in the rotor, PMSMs can produce higher

torque and depict faster dynamic response. However, to operate these machines for different speeds and load torques, controlled DC/AC inverters are required. Moreover, these types of converters need to be designed to produce high efficiency. Due to the development of adjustable DC/AC drives, the performances of AC machines have increased tremendously. A typical structure of an adjustable speed drive system is shown in Fig. 1.2.

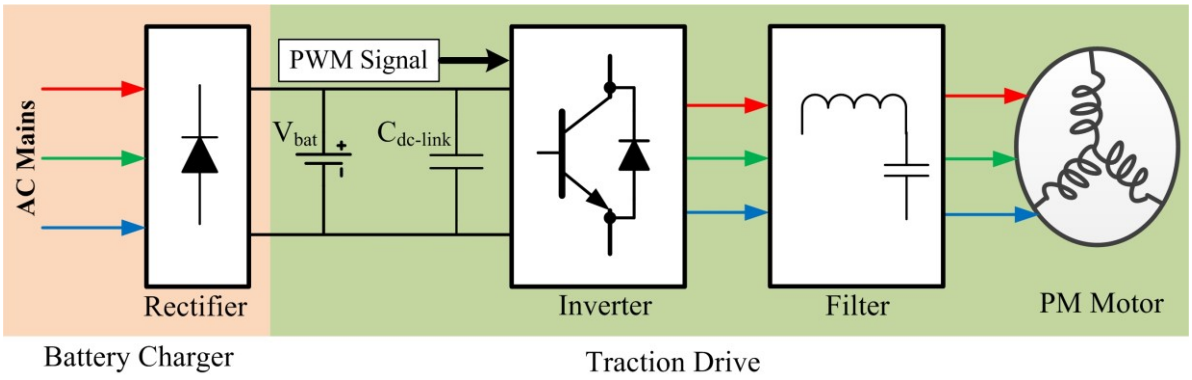


Figure 1.2 AC/DC/AC power converter stage for traction application.

The battery charging state includes a three phase rectifier which converts the three phase AC voltage to DC voltage to charge the high voltage battery pack. Different types of DC-DC converters are generally being used to match the voltage levels of rectified output voltage and the voltage of the high voltage battery pack. The DC-link capacitor is generally being used to filter out the high frequency switching ripples from the battery. Different types of PWM techniques are then used to trigger the three phase inverter to drive the traction machine. Furthermore, *LC*-filters are generally used at the output of the DC/AC inverter, to make the voltage as close as possible to sinusoidal for effective motor operation. When cable lengths are long, *LC*-filter is essential [15], to reduce the stress applied on the machine windings. Fig. 1.3 shows the different available DC/AC converters used for medium power traction.

Voltage source inverters (VSIs) are generally preferred in adjustable traction speed drives to control the output voltage and frequency. VSIs depict faster dynamic response compared to current source converters (CSIs), since there exists no line inductor in the DC link. VSIs can be divided into two configurations; typical 2-level and multilevel inverters. For future high-power electric traction applications, such as EV transit bus or railway propulsion applications, the battery DC-link voltage needs to be increased to about 600 V (compared to 300 V, as is the case in the commercially available Nissan Leaf ®). For a 2-level inverter scenario, with higher blocking voltage and frequency, losses (conduction and switching) would be extremely high. These losses are usually dissipated by a heat sink. To dissipate this

large amount of power, the heat sink size and cooling system needs to be increased, which will increase the space requirements. Hence, multilevel inverters are suggested as a solution, mainly because it portrays a lower blocking voltage per device, which reduces the devise losses compared to 2-level inverters [16]-[19].

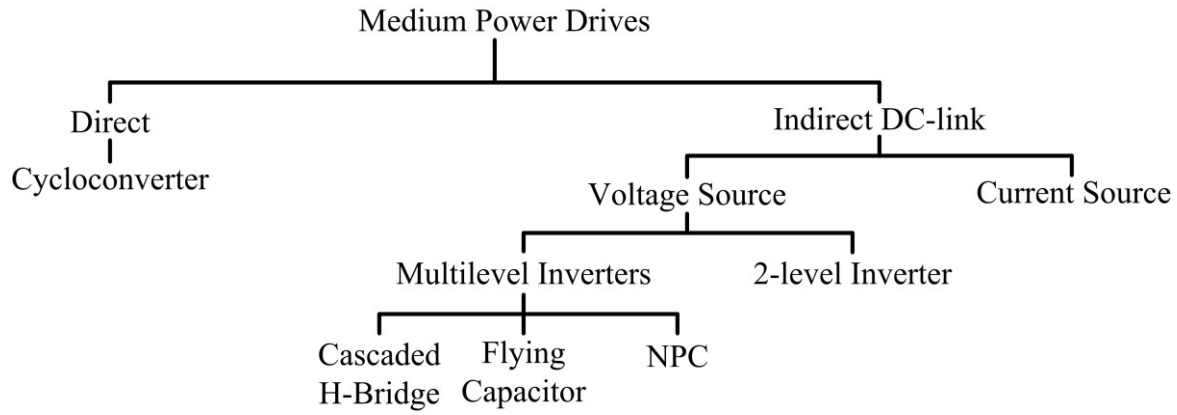


Figure 1.3 Different DC/AC power converters use for motor drives applications.

Fundamentally, the 2-level inverter based vector control of PMSM can be divided into two categories; current control and voltage control. In the current control strategy, a hysteresis band is generally used, to keep the phase current within a predetermined limit, depending on a specified current reference value [20]-[24]. However, due to the presence of this hysteresis band, it is not possible to keep switching frequency constant. Switching frequency keeps on changing, depending on the current reference and hysteresis band. Hence, as far as possible, this type of control scheme is not used for adjustable speed drives.

On the other hand, voltage controlled PWM strategies are generally widely used for adjustable speed drives, because they can provide a fairly constant switching frequency. Voltage controlled PWM schemes can be divided into two strategies; continuous and discontinuous conduction (CPWM, DPWM). Both the continuous and discontinuous conduction mode can be further subdivided into the Sine PWM (SPWM) and Space-vector PWM (SV-PWM) techniques. The maximum phase voltage peak, which can be achieved by SV-PWM is 57.77% of the total DC-link voltage. It is around 15% more compared to the sine-PWM technique [25]. SPWM is the simplest constant switching frequency PWM scheme used in adjustable speed drives. However, it results in reduced DC-link voltage utilization compared to the SV-PWM scheme. Hence, SV-PWM techniques are the most widely used for generating switching pulses for DC/AC traction inverters [26]-[31]. However, sine-triangle PWM with third harmonic injection shows the same DC-bus voltage utilization as SVPWM based strategy discussed in [32]-[34].

To improve inverter efficiency by reducing the switching losses at peak load currents, a control strategy was introduced by researchers in late 1990s. It is known as the discontinuous pulse width modulation scheme [36]-[39]. In this strategy, when the inverter phase current goes higher than a specified limit, one of the phases is forced to be clamped to either the positive or the negative DC voltage. As one of the inverter phases stops switching for certain time duration (120°), it reduces the switching losses to around 33%, compared to the conventional PWM technique [35].

In EVs the main bottle neck is the battery pack, because it is the main source of power to the motor and other control circuits which drives the vehicle. The battery pack takes a significant amount of the space for vehicles, which directly impacts on the vehicle weight and performance. One way to approach this problem is to develop a more advanced battery technology to increase the power density of the battery module or to increase the power density of the inverter drives module. The main space utilized by the inverter drive system is by the heat sink, DC-link capacitor and the other passive components. So by reducing the size of those components, it will be possible to reduce the total size of the system. The size of the passive components is designed by the operating frequency and size of the heat sink is designed by the power switches losses. So increase in the switching frequency of the conventional two-level inverter will reduce the passive component size. However, it will increase the switching losses which will directly have an effect on the size of the cooling system and heat sink size. Presently at higher machine speeds above base speed the switching frequency is generally 12.0 kHz depending on load torque requirement and DC-link voltage generally 450.0 V to keep the switch losses low. However, it introduces more current for the same amount of output power compared to the higher DC bus voltage. Fig. 1.4 shows the general schematic of electric vehicle drive train.

To overcome these problems, a 3-level inverter could be a potential solution. It has reduced switching losses and voltage ratings per device are also half for same DC-link voltage level. Multilevel inverters have attracted special attention in high power applications for the last three decades, after its introduction in 1981 [40]. Due to low power ratings of the switches used for multilevel inverters compared to two-level inverters for same DC-bus voltages, switching losses reduces as the switching frequency increases [19].

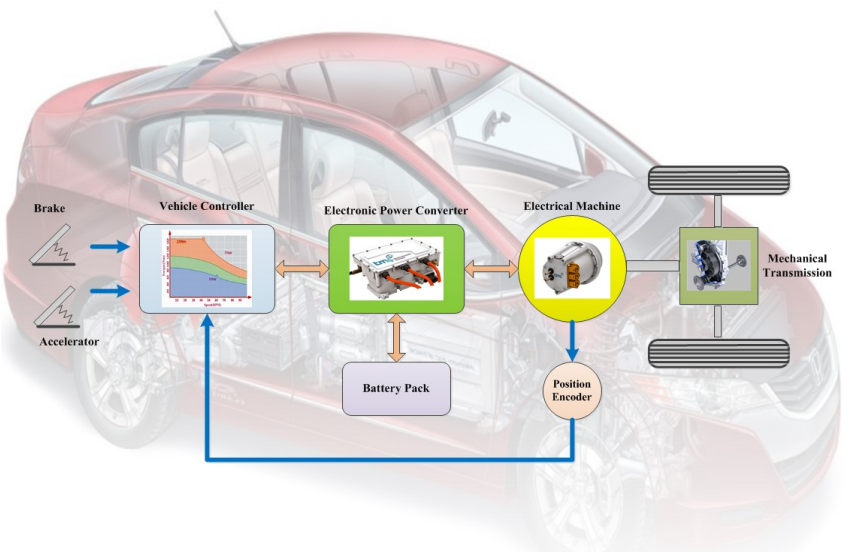


Figure 1.4 Schematic of a pure electric vehicle control.

There are other additional advantages like a reduction in total harmonic distortion (THD) due to an increase in the number of voltage steps, which then reduces EMI emission and high dv/dt stress across semiconductor switches. Other typical problems associated with two-level inverters like stator winding insulation break down and bearing failures can also be significantly reduced in three-level inverters [41].

1.1. Different Multi-Level Inverter Control Strategies

As shown in fig. 1.3, multilevel inverters can be divided into three categories. A detailed study on the different multilevel inverter strategies are explained as follows.

1.1.1. H-Bridge Inverter

Fig. 1.5 shows the block diagram of a cascaded H-bridge inverter [42]-[47]. In this topology, each power unit, which is composed of four power switches, is supplied by separate DC voltage units. Hence, the number of voltage steps in the output voltage will be ($2n$+1), where n is the total number of separate DC-power supply units. Hence, in applications requiring separate DC power sources, H-bridge inverters present an attractive solution. However, for EV applications, where the source of DC power supply is a high-voltage battery pack, it would be very difficult to extract separate connections out of each battery cell or battery module. Moreover, extra control circuits may also be required to balance the cells, which will add extra complexity to the system. Thus, an H-bridge multilevel inverter may not be an optimal solution for EV drives.

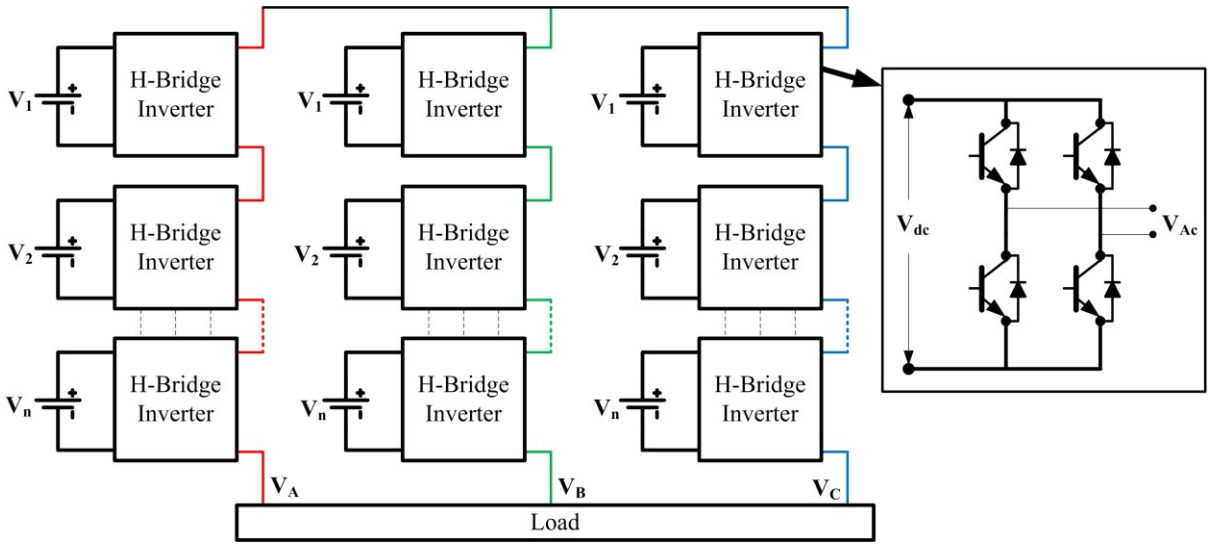


Figure 1.5 Three-phase n-level cascaded H-bridge inverter.

However, in applications where small, discrete DC power sources are available, such as fuel cells, wind power, and solar power, the H-bridge multilevel topology could provide enormous benefit.

1.1.2. Flying Capacitor Inverter

Fig. 1.6 shows the topology of a capacitor-clamped (flying capacitor) multilevel DC/AC inverter. It was first introduced by Meynard and Foch in 1992 [48]. In this topology, for *n* number of output voltage levels, (*n*-1) numbers of capacitors are generally required. The capacitors are connected in a ladder structure, whereby each capacitor voltage is different from the nearest one. One of the advantages of this topology is that, it has redundancies for inner voltage levels. In other words, two or more valid switching combinations can produce a desired output voltage. Moreover, the phase redundancy of clamped capacitors helps balance the capacitor voltages [49]-[54]. However, due to the large number of capacitors required in this topology, serious space implications exist, which negatively influences the power density of the inverter. Hence, this topology may not be the best choice for EV traction, where space and passive component size reduction is of primary importance.

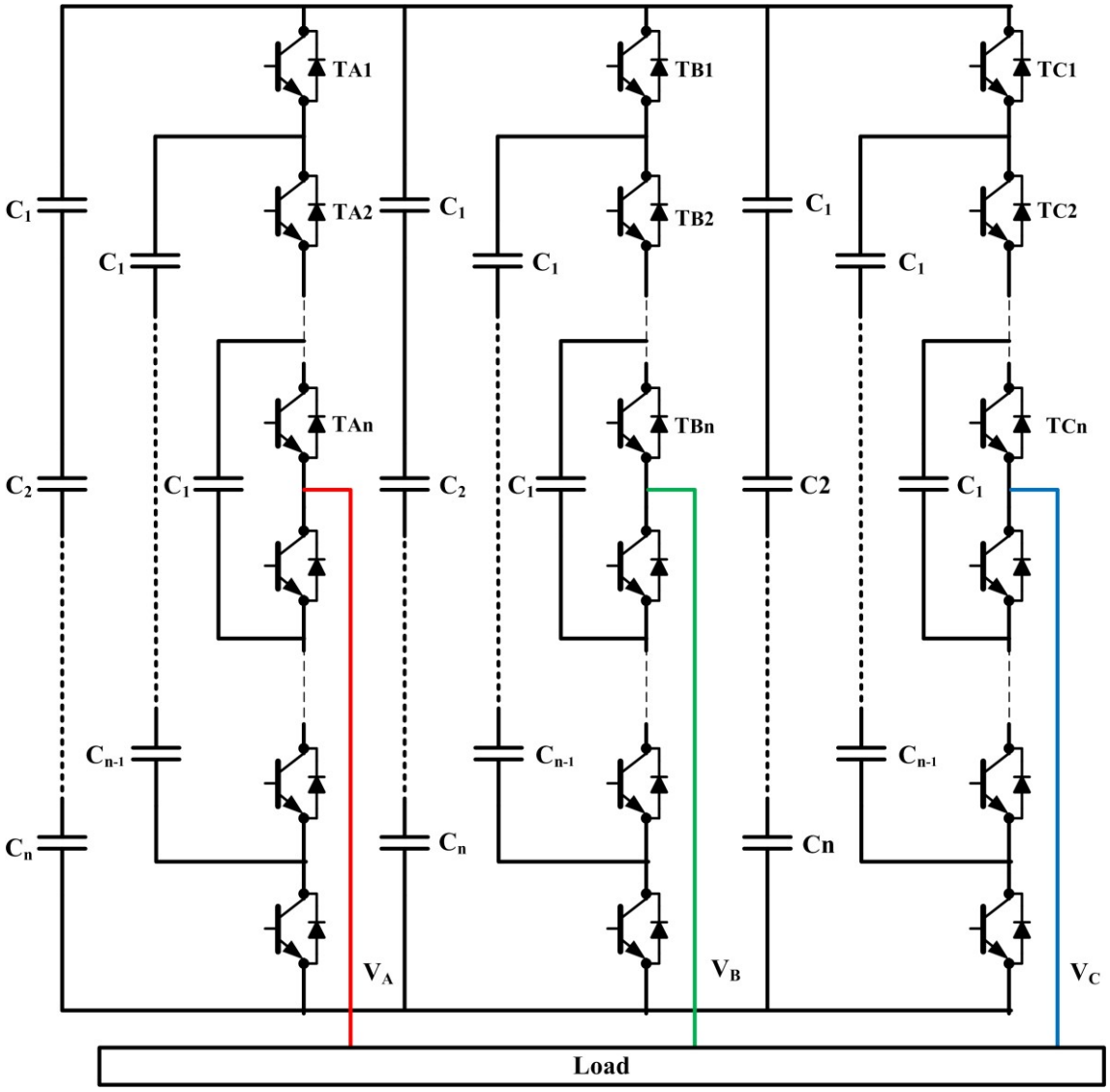


Figure 1.6 Three-phase, *n*-level, clamped capacitor inverter.

1.1.3. N-Level Neutral-Point-Clamped (NPC) Inverter

Fig. 1.7 shows the schematic diagram for a neutral point diode-clamped (NPC) multilevel inverter, introduced by Nabae, Takahashi, and Akagi, in 1981 [40]. Compared to the flying capacitor topology, in NPC inverters, capacitors are replaced by diodes, and the common points are connected to the DC link capacitor neutral point. For an *n*-level NPC inverter, required numbers of capacitors would be (*n*-1). Hence, the total number of capacitors used is reduced drastically, which helps reduce use of passive components. This also reduces the overall space and weight. Therefore, comparing space, weight, and complexity of control strategy, as well as to reduce the number of passive components, NPC multilevel inverters are found to be the prime choice among the three multilevel inverter topological options.

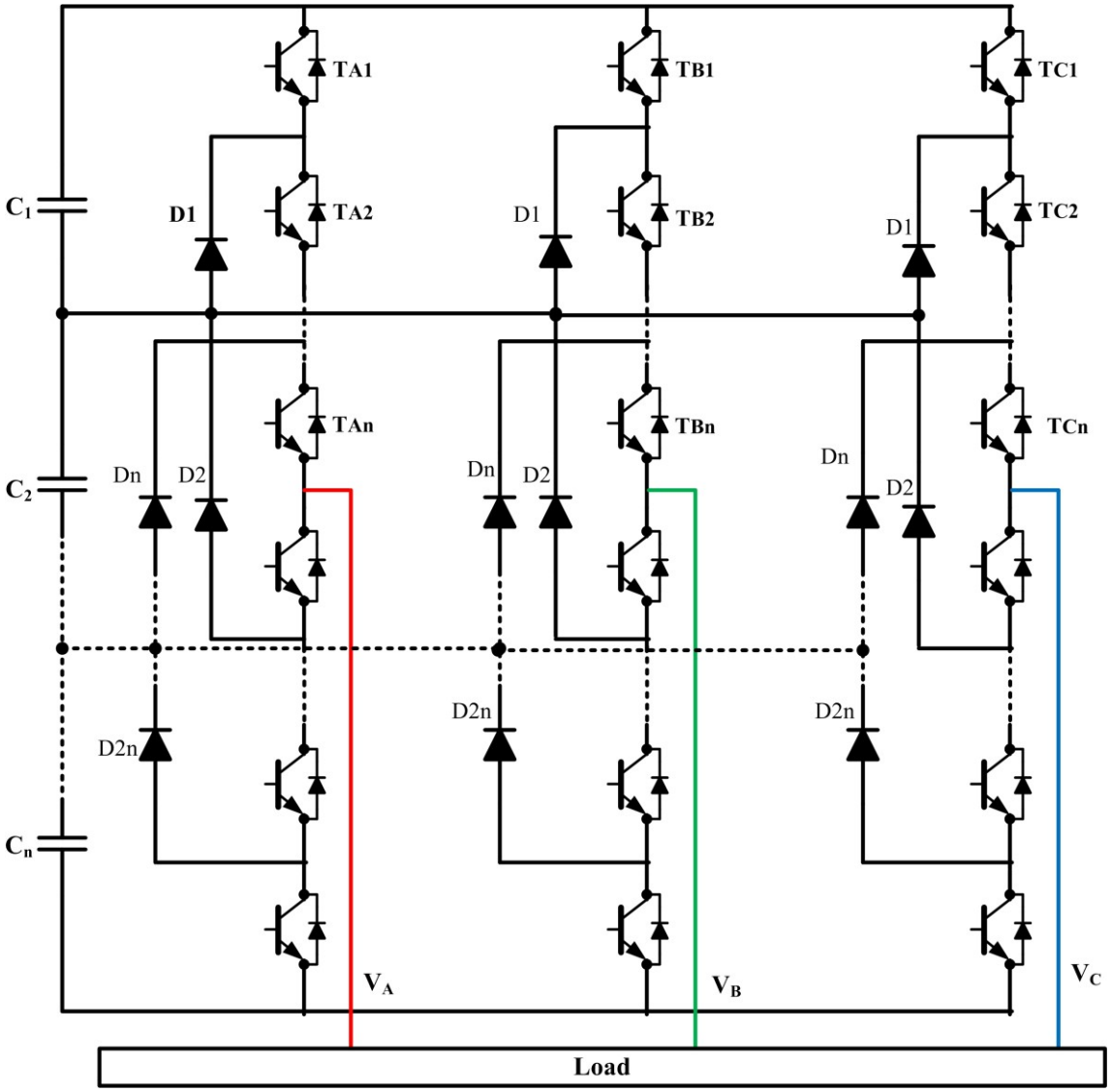


Figure 1.7 Three-phase n-level neutral point clamped inverter.

1.2. Different Available PWM Strategies for Multi-Level Inverters

Although, 3-level neutral point clamped inverters (NPC) have been studied quite widely recently, the DC-link voltage balancing algorithm is still a major concern [55] and considered a disadvantage from a control standpoint. When the two DC-link capacitor voltages are unbalanced, the DC-link neutral point potential (NPP) can significantly fluctuate, which may cause failure of the switches due to over voltage stress. Increasing the DC link capacitance may solve this problem to some extent; however, this scenario will increase the overall cost of the system. There exist numerous topologies for balancing the two DC-bus capacitor voltages, depending on application requirements. In general, there exist two types of DC-link capacitor voltage balancing schemes in literature; Hardware and PWM based control techniques. In the hardware based technique, two capacitor voltages are kept constant by

using two separate rectifiers [56], whereby they need two transformers with isolated secondary windings, which in turn, increases the total system cost. Moreover, they are large, less efficient, and add more cost to the system. This type of transformer can be replaced by connecting two back-to-back NPC converters [57]-[59].

Again, PWM based control strategies for 3-level inverters can be divided into three categories [60]: 1. Selective-harmonic-elimination (SHE), 2. Carrier-based PWM (CB-PWM), and 3. Space vector PWM (SV-PWM). A detailed study of the available and most widely used available DC-bus balancing topologies are presented below.

1.2.1. Selective-Harmonic-Elimination (SHE) Based PWM Strategy

Selective harmonic elimination strategy provides certain advantages over other PWM based control strategies [61]-[64]; such as reducing the switching losses by reduced switching, better utilization of the DC-link voltage and higher power quality by reducing the lower order harmonic components. However, all the SHE strategies proposed so far are based on the generation of commutation angle (α_1, $\alpha_{2...}$ α_n). These angles are generated by equating the equation of the harmonic components to zero, that are required to eliminate. Solutions of these equations are computationally cumbersome and take a lot of processor memory and processing time. Hence, most of the SHE strategies are generally used for high and medium power applications, where switching frequencies are in the range of 200-800 Hz and power frequency of 0-50 Hz. Moreover, no DC-link voltage balancing strategy is shown with the SHE strategy, which will make the system more complicated for multilevel inverters. The DC-link of these inverters is generally supplied by separate three-phase rectifiers across each capacitor for NPC inverters. Hence, for electric vehicle applications where, machine speed goes as high as 800.0 Hz and the DC-link balancing strategy will also be incorporated with the PWM strategy, SHE technique could not be of great interest.

1.2.2. Carrier PWM Based Strategy

Based on the SPWM control strategy, a switching frequency optimized PWM control (SFO-PWM) was introduced for NPC inverters, with DC-link voltage balancing [65]. In this strategy, depending on the DC-link capacitor voltage deviation, offsets were used in addition to the reference three-phase voltage signals. Because of SPWM, this strategy is not easily able to utilize DC-link capacitor voltage efficiency, compared to SV-PWM strategy. Large values of DC-link capacitors are used, which helps reduce the DC-link capacitor voltage deviation. On the other hand, the proposed strategy has not been tested for a wide range of speed and torque variation, to show performance efficiency.

Based on average neutral point current flowing in to or out of the DC-link capacitor, a capacitor voltage balancing strategy is also proposed in [66], [67]. In this strategy, the neutral point current is integrated, which generates the neutral point voltage deviation. Based on this value, a zero sequence voltage (v_o) is added or subtracted from the reference voltage signal, to generate the switching pulses. Because of neutral point current integration, the procedure has a certain time delay associated with it. Hence, for high speed operation, this strategy may introduce larger voltage deviation in the DC-link capacitor voltages. Moreover, capacitor values selected is also high, and no transient or steady state performances are shown to validate the proposed scheme.

A hysteresis controller for capacitor voltage balancing is presented in [68], which keeps the two DC-link capacitor voltages within a certain tolerance band. Unfortunately, this technique has no restriction on the choice of switching state, and simultaneous switching may occur. Instantaneously switching an output through more than one level can result in significant voltage stressing of devices. Also, test results show that the neutral point rapidly diverges, when the control signal is removed. However, without sharing the redundant states, the PWM controller itself becomes unbalanced, and neutral point divergence is unavoidable.

Another DC-link voltage balancing scheme is also proposed based on integration of neutral point capacitor current in [69]. In this study, the effect of a regenerative condition on capacitor balancing is also considered.

An improved carrier based PWM (CB-PWM) is proposed in [70], based on NTV-SVM strategy. In this strategy, a zero-sequence component of voltage, based on capacitor voltage unbalance, is added to the reference voltage signal. Performance comparison with SPWM strategy, based on NP voltage oscillation, is also studied. However, applications of the proposed system with system transients are not shown. Moreover, addition of zero-sequence voltage components with the reference voltages could lead to a modulation value, which can clamp one of the phase voltages. This situation can create further unbalance at the neutral point.

A carrier-based PWM strategy is introduced in [80], which is capable of eliminating low order harmonics. However, it increases the switching frequency by one-third compared to conventional SV-PWM techniques. In this control strategy, DC-link voltage deviation is reduced by shifting the modified modulation signals in accordance with the capacitor voltage differences. However, no transient results are shown to demonstrate the DC-link voltage balancing ability of the scheme and the system takes a considerable time before converging.

A PI controller is proposed in [72]-[75], to calculate the NPP fluctuation with a carrier based PWM technique. In this strategy, neutral point current is integrated for one switching cycle, and then it is subtracts from zero, and passes through a PI controller, to generate the duty for redundant voltage vectors. Although experimental results show that the proposed control strategy is capable of keeping the neutral point voltage stable, the system is highly dependent on the PI gain.

A carrier based neutral point potential regulator is proposed in [76], with continuous change in variable offset voltage components, to keep the capacitor voltage deviation constant. The offset is generated, by comparing the difference between the capacitor voltages, with zero- and pass-through PI control block. As a PI controller has its own settling time and overshoot, for motor drive applications, it may lead to asymmetrical switching of NPC inverter.

Based on the sensed motor phase currents and power factor, an analytical equation is derived to calculate the DC-offset voltage to remove the PI controller and the two DC-link voltage sensors in [77]. For this analysis a balanced system is considered, and it is assumed that all the machine parameter will remain constant. However, in practical system machine parameters varies with temperature and other factors, which can leads to an inaccurate value of the DC-offset voltage. An inaccurate DC-offset value could lead to a more unstable system. Moreover, no experimental studies are performed to show the effectiveness of the proposed system.

A carrier-based DC-link voltage balancing topology, with injection of third harmonic component in the fundamental, is presented in [78]. The 3^{rd} harmonic is added with both the carrier and the reference modulation signal and the NPP variation is studied. Although results showed a stable operation of the NPP in steady state, at transients it may clamp one of the phases and introduce over modulation.

DC-link capacitor balancing by injecting a neutral point current is proposed in [79]. The main shortcoming of this strategy is the additional hardware and complexity of the control system. Another method, by connecting the neutral point of inverter and the corresponding AC-side system, is presented in [80]. The drawback of this method is the existence of zero-sequence current on the AC side, which may not be acceptable, due to heating or magnetic saturation of transformer.

Another carrier based strategy with offset addition is proposed in [81]. Simulation and experimental results are shown to validate the strategy. Results showed required steady state stability, however no transient performances are demonstrated.

In [82], [83] a modified carrier signal is proposed, based on the min-max control. It divided the main carrier signal in two parts for upper and lower carrier signals. It also proposed an analytical calculation of the duty ratio that is required to add with the main modulating signal to keep the DC-link capacitors balanced. However, it has a common problem with the calculation of the proper DC-offset value. If this generated DC-offset goes out of limit, it could unbalance the capacitors. A modified carrier based PWM scheme, which uses one carrier frequency instead of two is shown in [84]. However, DC-link capacitor balancing capability is not shown.

In [85], authors showed three different type of carrier-based-modulation for NPC inverter depending on the phase shift between the two carrier signals. Simulation studies are performed to show the total voltage and current harmonic distortion. However, no results are shown to balance the two DC-link capacitor voltages.

1.2.3. Space-Vector Based PWM (SV-PWM) Strategy

A generalized, fast SVM algorithm for multilevel inverters is proposed in [86] for *n* number of levels, to reduce implementation complexity. However, no simulation and experimental results are shown to prove the system performance.

A control strategy based on small voltage vector redundancy is presented and experimentally verified in [87]-[89]. In this topology, a redundancy factor "α" is introduced to utilize the positive and negative small voltage vectors, which produce the same output voltage, but affects the two capacitor voltages differently. However, to compute the value of "α" online, it produces 1.0 m-sec of computation delay time. This is an iterative process which may introduce higher capacitor voltage deviation for application like motor drives with high load transients. Experimental results are shown only at steady state and it shows large computational delay time to reduce capacitor voltage deviation. DC-link voltage balancing for over modulation regions are also studied and implemented by researches in [90]. In this strategy conventional nearest three vector (N3V) scheme is used at modulation indices below 1 and above that the proposed strategy is used.

Based on the distribution of redundant small voltage vectors, another control strategy is introduced in [91], [92]. In this topology, 4 sub-sectors are further divided in to 6, to make the number of switching sequences symmetrical. Although experimental results show reduced capacitor voltage variation, system transient studies are not performed. Moreover, derivation of distribution factor "α" is not shown and system computational complexity also increased due to increased number of sub-sectors.

Based on the two capacitor voltage deviation, calculated from individual capacitor currents, a capacitor voltage balancing algorithm is also proposed in [93]. Switching sequences are generally altered depending on the instantaneous states of capacitor voltages. As capacitor voltages are calculated by integration, additional computation delay time is introduced in the system. Moreover, in this strategy, both the positive and negative redundant states are used in the same switching sequence, which may influence the capacitor voltage deviation in transients.

A virtual space-vector scheme (VSVS) – an advanced PWM scheme – capable of controlling the neutral point voltage over entire range of output voltage is presented in [94]. According to this topology, the virtual point, based on the small and medium voltage vectors, is added in each sector, which helps to keep the capacitor voltage deviation at a predetermined level. However, the inclusion of an additional vector, which keeps neutral point current zero, creates a more complicated system in terms of real-time implementation and increases the switching frequency. Moreover, experimental results show only steady-state results, without any transients and rapid load variations.

A more complicated system is proposed based on dividing the space vector area into more sectors by calculation of position and length of the boundary vectors in [95]. Redundant voltage vectors time duration are calculated using dc-link voltage unbalance, neutral point current and DC-link capacitance.

A SV-PWM technique which can operate at deep modulation indices and at low power factor is proposed in [96]. The proposed strategy claims to reduce the effect of third harmonics in the neutral. The modulation indexes are obtained directly from the unbalanced SV diagram. Experimental results show significant amounts of deviation in capacitor voltages. Also, low frequency NP voltage oscillation still persists.

A number of modified NTV control strategies are proposed in [97], [98] wherein the capacitor voltage deviation is kept under a certain band, by sensing the 3-phase currents. Based on the 3-phase currents, the neutral point current is calculated, and duty ratios of the nearest three vectors are changed, to keep current in a particular tolerance level. The control action is set to take place at the zero crossing of neutral current. Although this topology is capable of keeping the neutral point voltage at a desired level, it needs a lot of computation as well as zero neutral point current detection, and still it produces significant amount of capacitor voltage deviation.

An iterative technique to solve the DC-link capacitor voltage balancing is proposed in [99], depending on the neutral point current. In this strategy, the zero-sequence voltage is

added at each sampling time, and neutral point potential is observed, to keep the voltage deviation within a particular band. Although capacitor voltage deviation was maintained within a particular band, system computation time is very large, and hence, makes this strategy non-suitable for fast transient systems.

An alternative DC-link voltage balancing strategy, based on two-capacitor voltage sensing, is proposed in [100] and [101]. In this strategy, the duty time of the redundant voltage vectors are changed between each switching cycle, based on the capacitor voltage unbalance. Although the proposed controller showed fairly good performance, the system may suffer from asymmetrical switching, due to the change in duty in between switching cycles. Moreover, due to the switching vector change in between switching cycle, could lead to more switching losses. Furthermore, a SV-PWM based 3-level invert control strategy is also developed without considering the problem with capacitor voltage balancing in [102], [103].

A detailed study of the effect of linear and nonlinear loads on DC-link capacitor voltages is presented in [104]. However, no neutral point balancing strategy is proposed. Based on the symmetry between 2-level inverter space vector diagram and the 3-level inverter, a modified DC-link capacitor voltage balancing topology is developed in [105]. Although, the control strategy developed is fairly novel, it makes the system too complicated. A hybrid controller, using SV-PWM and SHE-PWM, is proposed in [63]. However, the problem associated with capacitor voltage deviation is not presented.

A new space vector modulation scheme, to eliminate even order harmonics in the inverter output voltages, is proposed in [106]. However, DC-link voltage balancing capability is not proven with the proposed scheme. A modified control strategy, by calculating the time offset, based on phase current, and the dwell time of the small and medium voltage vectors, is proposed in [107]. Simulation and experimental results are presented to support the control scheme. However, effects of the control strategy on the phase voltage harmonic distortion are not presented.

A hybrid control strategy based on NTV and NTV^2 is proposed in [108], [109]. The proposed strategy uses nearest three vector (NTV) modulation scheme for each fundamental cycle and uses NTV^2, when NTV scheme is not sufficient enough to keep the DC-link capacitor voltage stable. Although experimental results show required performance with balanced load, dynamic performance of the system is not validated.

Another capacitor voltage balancing strategy based on the redundant voltage vectors is proposed in [110]. In this strategy both the positive and negative voltage vectors are used in

each switching sequence which increases switching losses by introducing more switching states. Moreover, the redundant vectors use time sharing between the positive and negative voltage vectors, to keep the DC-link capacitor voltages balanced. However, if the time sharing is not optimized, it would create additional voltage deviation at neutral point. In [111] authors presented direct torque control of induction machine with three-level NPC inverter. However, no DC-link capacitor voltage balancing issue is discussed.

1.2.4. Other Available Neutral Point Clamped Control Schemes

Another critical issue with adjustable speed drives is that they inherently produce common-mode voltages, which generate common-mode currents. These currents flow though stray capacitances of electric machines very easily. Hence, these currents directly affect machine bearings and generate electro-magnetic interference (EMI) with neighbouring electronic devices. Multilevel inverters produce lower EMI than a corresponding 2-level inverter of same size (kW output power rating). However, to reduce the EMI effect further, a carrier-based PWM control strategy is proposed in [112]. In [113] a DC-link voltage balancing strategy is proposed with reduced common mode voltage. However, no transient results are shown to demonstrate the controllability of the proposed scheme.

A self-neutral point balancing topology is proposed in [114], [115] whereby the switching sequence related to the upper and lower capacitors are used alternatively. Although, this configuration is suitable for systems with slow dynamics, for adjustable speed drives, it may cause tremendous amount of issues. Moreover, if the capacitor voltages have some initial unbalance, it can produce further deviation, if it is not stabilized quickly.

A hysteresis current control based 3-level NPC inverter with DC-link capacitor voltage balancing is also proposed in [116]-[121]. In this control strategy, like 2-level hysteresis current control, reference and load currents are compared and passed through a hysteresis block to generate the PWM control signals for the switches. Although, it is a fast control strategy, it suffers from the fundamental problem of variable switching frequency, which keeps changing with load variations and the hysteresis band. The problem associated with pure reactive power compensation for 3-level inverter used in Flexible AC Transmission systems (FACTS) and balancing DC-link capacitor voltages under those conditions are proposed in [122].

Different fault tolerant operations of neutral point clamped inverter with active NPC is also proposed in [123], [124]. In these strategies the NPC diodes are replaced with switches, which can enable the system to operate for both single and multiple device open and short

circuit conditions, which intern increases the system reliability. However, with higher numbers of IGBT switches instead of power diodes will make the system cost and total inverter losses comparatively higher than the conventional NPC structure.

1.3. Discontinuous-PWM Scheme for Three-level Inverter

In case of continuous PWM strategies, phase voltages are continuously switched between positive, negative, or zero switching states. When the inverter load current is high, this switching contributes considerable amount of switching losses in the converter, which lowers the inverter efficiency considerably. In case of a discontinuous PWM strategy, depending on load current, one of the phase stops switching for 120°, so that switching losses are reduced. With this strategy, the inverter switching loss can be reduced to one-third, compared to the conventional SV-PWM strategy. In case of 2-level inverters, since there exists no issue related to capacitor voltage unbalance, it is widely used in adjustable speed drives. However, in case of a 3-level inverter, it produces challenges, because of capacitor voltage unbalance. Few research studies show possible switching schemes, which allow DC-link capacitor voltage balance even in a discontinuous zone [125]-[128]. However, results are not still convincing for adjustable speed drives, with dynamic changes in load.

A detailed comparative study is performed in [129]-[132], to show the performance comparison between carrier-based and SV-PWM. Results show that, when carrier-based PWM is used, computation time reduces by 50%, compared to when SV-PWM is used. It must be noted, however, that total harmonic distortion (THD) for both control strategies are identical.

Compared to a Surface PMSM (SPMSM), Interior PMSM (IPMSM) has a broader range of speed variation, because of larger stator inductance. Moreover, because of the presence of reluctance torque, which exists due to the difference between the two inductances, L_d and L_q, torque produced by IPMSMs is slightly higher compared to SPMSMs for the similar per-unit stator current [133]-[145]. Hence, the performance of an IPMSM will also be studied, with a 3-level inverter, and its effect on DC-link capacitor voltage balancing will be analysed.

1.4. Research Goals and Objectives

The main focus of this project is to:

1. Develop a PWM control strategy for three-level neutral point clamped inverter (NPC) which takes care of the DC-link voltage balancing with the modulation technique, without any external voltage balancing hardware circuit.

2. Detailed performance comparison study between two- and three-level inverter considering, total voltage harmonic distortion (THD), capacitor current ripple ($I_{capripp}$), torque ripple (T_{rip}) and total inverter loss (Switching and conduction).
3. Performance analysis of three-level inverter with SVPWM, carrier based PWM and discontinuous pulse width modulation (DPWM) schemes.
4. Performance analysis of the proposed three-level inverter controller with interior permanent magnet machine (IPMSM) for wide range of speed variations.

1.5. Research Contributions

Following are the key contributions of this research:

1. A novel reduced switching loss based SVPWM strategy is proposed for both the SPMSM and IPMSM including field weakening operation. The developed controller is also capable of sustaining the difference between the DC-link capacitor voltages within a tolerance level.
2. Detailed simulation, experimental and validation studies are carried out, to depict the performance improvement using the proposed control strategy of the 3-level over the 2-level inverter. Comparative analyses of the results are also presented.
3. A hybrid carrier based PWM strategy for both continuous and discontinuous conduction mode is proposed, which uses both the carrier based and space vector strategy to keep the DC-link capacitor voltages balanced (Hybrid PWM).
4. Detailed comparison studies of conduction and switching loss distribution for IGBTs, IGBT anti parallel diodes, and NPC diodes are carried out with change in modulation index for conventional and the different proposed control strategies. Total inverter losses, torque ripple, neutral point voltage fluctuation comparison with change in switching frequencies is also carried out.

The following journal papers as well as international conference papers have been published as a direct result of the research conducted during my Doctoral Program.

Journal:

Published:

1. **A. Choudhury**, P. Pillay, and S. S. Williamson, "Comparative analysis between two-level and three-level DC/AC electric vehicle traction inverters using a novel DC-link voltage balancing algorithm," *IEEE Journal of Emerging and Selected Topic in Power Electronics*, vol. 2, no. 3, pp. 529-540, Sept. 2014.

2. **A. Choudhury**, P. Pillay, and S. S. Williamson, "DC-link voltage balancing for a 3-level electric vehicle traction inverter using an innovative switching sequence control scheme," *IEEE Journal of Emerging and Selected Topic in Power Electronics*, vol. 2, no. 2, pp. 296-307, June 2014.

Under Review:

1. **A. Choudhury**, P. Pillay, and S. S. Williamson, "Modified DC-bus voltage balancing algorithm based three-level neutral point clamped IPMSM drive for electric vehicle applications," Submitted for review in *IEEE trans. on Industrial Electronics*.
2. **A. Choudhury**, P. Pillay, and S. S. Williamson, "Modified DC-bus voltage balancing algorithm for three-level neutral point clamped PMSM traction inverter drive with low power factor," Submitted for review in *IEEE trans. on Industry Applications*.
3. **A. Choudhury**, P. Pillay, and S. S. Williamson, "A hybrid-PWM based DC-link voltage balancing algorithm for a 3-level neutral-point-clamped (NPC) DC/AC traction inverter drive," Submitted for review in *IEEE Journal of Emerging and Selected Topics in Power Electronics*.
4. **A. Choudhury**, P. Pillay, and S. S. Williamson, "A Modified Discontinuous-PWM three-level neutral point clamped (NPC) traction inverter drive for electric vehicle propulsion applications," Submitted for review in *IEEE trans. on Power Electronics*.

Conference:

1. **A. Choudhury**, P. Pillay, and S. S. Williamson, "A Hybrid-PWM Technique Based DC-Link Voltage Balancing Algorithm for a 3-Level Neutral-Point-Clamped (NPC) DC/AC Traction Inverter Drive," Accepted for presentation in *Proc. on IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, Mar. 2015.
2. **A. Choudhury**, P. Pillay, and Sheldon. S. Williamson, "A Performance Comparison Study of Space-Vector and Carrier-Based PWM Techniques for a 3-Level Neutral Point Clamped (NPC) Traction Inverter Drive," Presented in *Proc. on IEEE Power Electronics, Drives, and Energy Systems (PEDES)*, IIT Bombay, Mumbai, India, Dec. 2014.
3. **A. Choudhury**, P. Pillay and Sheldon. S. Williamson, "Modified DC-bus Voltage Balancing Algorithm Based Three-Level Neutral Point Clamped (NPC) IPMSM Drive for Electric Vehicle Application," Presented at *IEEE Industrial Electronics Society Annual Conf.*, Dallas, TX, USA, Nov. 2014.
4. **A. Choudhury**, P. Pillay and Sheldon. S. Williamson, "A Novel DC-link Voltage Balancing Algorithm for a 3-Level Neutral Point Clamped (NPC) Traction Inverter for an

Electric Vehicle IPMSM drive," Presented at *IEEE Industrial Electronics Society Annual Conf.*, Dallas, TX, USA, Nov. 2014.

5. **A. Choudhury**, P. Pillay, M. Amar and Sheldon. S. Williamson, "Reduced switching loss based DC-bus voltage balancing algorithm for three-level neutral point clamped (NPC) inverter for electric vehicle application," in *Proc. on IEEE Energy Conversion Congress and Exposition*, Pittsburgh, USA, Sept. 2014, pp. 3767-3773.
6. **A. Choudhury**, P. Pillay and Sheldon. S. Williamson, "Modified DC-bus voltage balancing algorithm based three-level neutral point clamped PMSM drive with low power factor," in *Proc. on IEEE XXIth International Conf. on Electrical Machines (ICEM)*, Berlin, Germany, Sept. 2014, pp. 2448-2453.
7. **A. Choudhury**, P. Pillay, M. Amar and S. S. Williamson, "Performance comparison study of two and three-level inverter for electric vehicle application," in *Proc. IEEE Transportation Electrification Conf. and Expo.*, Dearborn, MI, June 2014, pp. 1-6.
8. **A. Choudhury**, P. Pillay, and S. S. Williamson, "Modified DC-link voltage balancing algorithm for a 3-level neutral point clamped (NPC) traction inverter based electric vehicle PMSM drive," in *Proc. Annual Conf. of the IEEE Industrial Electronics Society*, Vienna, Austria, Nov. 2013, pp. 4660-4665.
9. L. Masisi, **A. Choudhury**, P. Pillay, and S. S. Williamson, "Performance comparison of a two-level and three-level inverter permanent magnet synchronous machine drives for HEV application," in *Proc. Annual Conf. of the IEEE Industrial Electronics Society*, Vienna, Austria, Nov. 2013, pp. 7262-7266.
10. **A. Choudhury**, P. Pillay and Sheldon. S. Williamson, "Real time operating system based online rotor position error minimization technique (RPEM) for permanent magnet synchronous machines," in *Proc. on IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, Mar. 2013, pp. 805-810.
11. **A. Choudhury**, P. Pillay and Sheldon. S. Williamson, "Advanced drives for low cost permanent magnet synchronous machines used for hev- a review," in *Proc. on IEEE Industrial Electronics Society Annual Conf.*, Montreal, CA, Oct. 2012, pp. 2895-2900.
12. **A. Choudhury**, P. Pillay and Sheldon. S. Williamson, "Modified stator flux estimation based direct torque controlled PMSM drive for hybrid electric vehicle," in *Proc. on IEEE Industrial Electronics Society Annual Conf.*, Montreal, CA, Oct. 2012, pp. 2965-2970.

1.6. Organization of the proposal

This proposal is organized as follows:

Chapter 1: Presents detail literature survey on the types of inverter used for electric vehicle drive application, their drawbacks and requirement for three-level inverter. Also different existing DC-link voltage balancing topologies are described and their associated problems for electric vehicle drives applications are also highlighted.

Chapter 2: Investigate the root cause for DC-link voltage unbalance and proposed a reduced switching loss based control strategy, which keeps the two DC-link voltages balanced in a particular tolerance level of (5%) the total DC-link voltage. The proposed scheme also able to use lower number of switching states compared to the conventional one. Detail simulation and experimental studies are carried out to proof the controllability of the proposed system. Furthermore, the strategy is modified to take care of the lower power factor condition.

Chapter 3: Presents a details simulation and experimental study of two-level inverter with SPMSM machine. The results are then compared with the three-level inverter based drive. An analytical expression of capacitor current is also derived. Results show a considerable improvement in total voltage harmonic distortion for three-level inverter with the proposed scheme and also considerable amount of reduction in total inverter losses as well.

Chapter 4: A modified carrier based PWM is proposed, which reduced the number of carrier signals to one and also simplifies the expression of duty cycle to trigger the IGBT switches. Moreover, a hybrid PWM strategy is proposed which uses the carrier based approach to generate the duty cycle with reduced computational time and complexity associated with the SVPWM based strategy and uses the redundant vector approach to keep the DC-link capacitor voltages balanced. It helps eliminate the DC-offset addition associated with the carrier based approaches. The proposed strategy is further extended for discontinuous PWM based control.

Chapter 5: The performance comparison studies of different proposed PWM strategies with change in modulation index and switching frequency is studied. Total voltage and current harmonic distortions are also considered.

Chapter 6: Space vector PWM strategy developed in chapter-2 is applied to a IPMSM and performance of the system is observed with change in machine speed and torque. A modified strategy is proposed in field weakening region where system power factor goes leading.

Chapter 7: Describe the conclusions and future work.

1.7. Summary of Chapter 1

This chapter provides a detailed literature survey on the existing inverter topologies and requirement of using three-level inverter for electric vehicle applications. Different available DC-link voltage balancing algorithms are analysed and problem of applying those topologies to electric vehicles are also analysed. Research goals and objective, organization of the thesis are explained and research contributions are also added as well.

Chapter 2. Three-Level Traction Inverter Drive

In permanent magnet synchronous motors (PMSMs) no field winding exists in the rotor; hence, no slip ring is required as in a synchronous machine. It makes the machine rotor inertia low. Also, as high power density permanent magnets are used in the rotor, machine volume is also significantly low compared to an induction machine of same size (kW rating). Moreover, due to the absence of rotor winding or copper conductors in the rotor, machine efficiency is quite high. All these features make permanent magnet machine the best choice for electric vehicle (EV) applications. There exist primarily two types of PMSMs; surface and interior type, depending on the location of the permanent magnets. Fig. 2.1 shows the surface PMSM rotor geometry. As can be observed in surface PMSM (SPMSM), magnets are placed on top of rotor, so the *d*- and *q*- axis inductances are same. However, for interior PMSM (IPMSM), magnets are buried in the rotor, which leads to difference in the *d*- and *q*- axis inductances. In EV industry both the surface and interior PMSM are generally being used, depending on application specific requirement. Interior or inset PMSM has a wider speed range compared to the surface PMSM, due to its difference in L_d and L_q value, which leads to provide reluctance torque. In this chapter, we are going to develop machine model equations and control topology for surface PMSM (SPMSM).

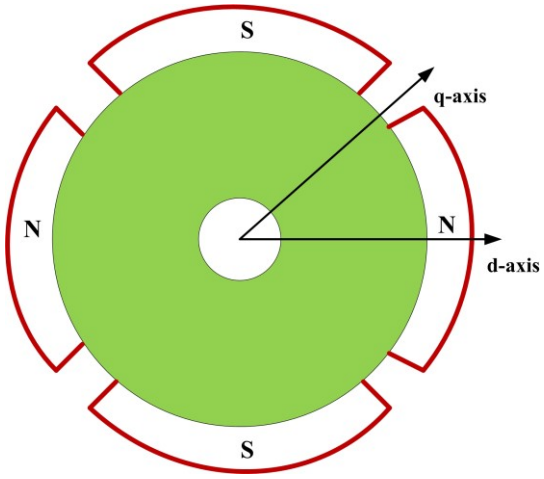


Figure 2.1 Surface PMSM rotor.

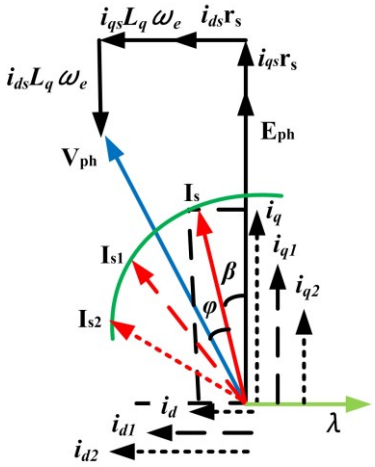


Figure 2.2 Phasor diagram of PMSM.

2.1. Machine Modelling

The machine model equations can be represented as follows:

$$v_{\mathrm{d}} = r_s \cdot i_{\mathrm{d}} + \mathrm{p} \cdot \varphi_d - \omega_{\mathrm{e}} \varphi_q \tag{2.1}$$

$$v_{\mathrm{q}} = r_s \cdot i_{\mathrm{q}} + \mathrm{p}\varphi_{\mathrm{q}} + \omega_e \left(\varphi_d + \lambda\right) \tag{2.2}$$

$$E_{\mathrm{ph}} = k_{\mathrm{b}} \cdot \omega_{\mathrm{e}} \tag{2.3}$$

$$V_{ph}^2 = \left(E_{ph} + r_s \cdot i_q + i_d \cdot X\right)^2 + \left(i_q \cdot X + i_d \cdot r_s\right)^2 \tag{2.4}$$

$$\varphi_{\mathrm{d}} = L_{\mathrm{d}} \cdot i_{\mathrm{d}} \tag{2.5}$$

$$\varphi_q = L_{\mathrm{q}} \cdot i_{\mathrm{q}} \tag{2.6}$$

$$T_e = (3\mathrm{P}/2) \cdot \left[\lambda \cdot i_q - (L_q - L_d) \cdot i_d \cdot i_q\right] \tag{2.7}$$

Here, P is the total number of machine pole, p is the dv/dt, v_d and v_q are the *d*- and *q*- axes components of the stator voltage, respectively, i_d and i_q are the *d*- and *q*- axes components of stator current, respectively, r_s is the stator resistance, ϕ_d and ϕ_q are the stator flux linkages in the *d*- and *q*-axes, respectively, L_d and L_q are the *d*- and *q*- axis inductances, λ is the rotor magnet flux linkage, due to the permanent magnet on the rotor side, E_{ph} is the induced back EMF, due to rotor magnet flux linkage, k_b is the back EMF constant, X is the winding reactance of the machine, P is the machine pole pair, I_s is the reference current vector shown in the phasor diagram, ϕ is the power factor angle between v_{ph} and I_s, and ω_e is the reference field speed. The steady-state phasor diagram of the PMSM is shown in Fig. 2.2. As for surface PMSM (SPMSM) *d*- and *q*-axis inductances are same (L_d = L_q), (2.7) can be expressed like (2.8).

$$T_e = (3\mathrm{P}/2) \cdot \left[\lambda \cdot i_q\right] \tag{2.8}$$

2.2. PMSM Control Strategy

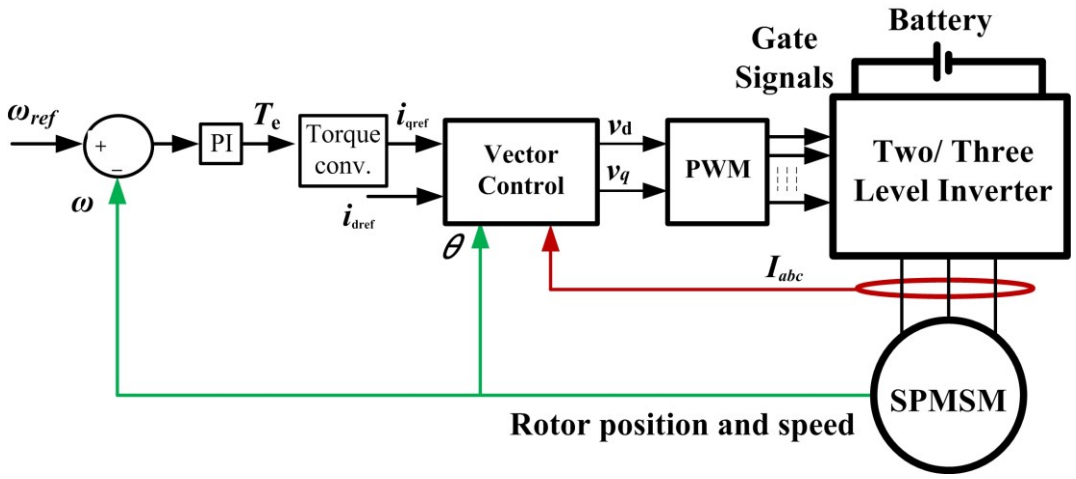


Figure 2.3 Vector control of PMSM.

Fig. 2.3 shows the control circuit diagram of PMSM. To control the machine, conventional vector control strategy is used. To implement the control strategy, we need three current sensors, for 3-phase currents measurement and a position encoder. Both the signals are feed back to the control board. From the position information speed of the machine can be

estimated, as shown in (2.9). Where, θ_n and $\theta_{(n+1)}$ are instantaneous position of rotor and t is the sample time. So based on these two variables and depending on the reference speed command ω_{ref}, d- and q- axis reference voltages are generated, as shown in (2.1) and (2.2). These reference voltage vectors are common for both two and three-level inverters. Depending on the reference voltage vectors and available DC-link voltages, PWM pulses are being generated for inverter.

$$\omega = (\theta_{(n+1)} - \theta_n)/t \tag{2.9}$$

For two-level inverter total number of gate pulse will be six and for three-level inverter it will be twelve.

2.3. Space-Vector PWM (SV-PWM) for Three-Level Inverter

As can be seen from the three-level NPC inverter in Fig. 2.4, the inverter has four switches for each leg. There exist two diodes in each leg, whose common points are connected to the common neutral point of the two DC-link capacitors. Hence, there exist a total 27 switching combinations, out of which three are null or zero vectors and 24 are active vectors, as shown in the vector diagram of Fig. 2.5.

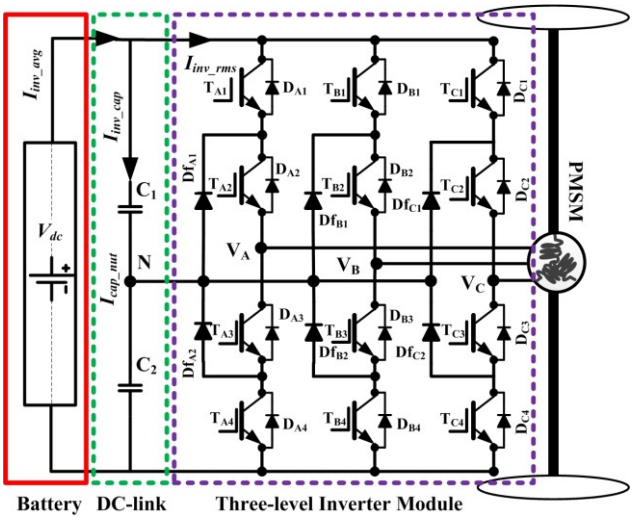


Figure 2.4 Three-level NPC inverter.

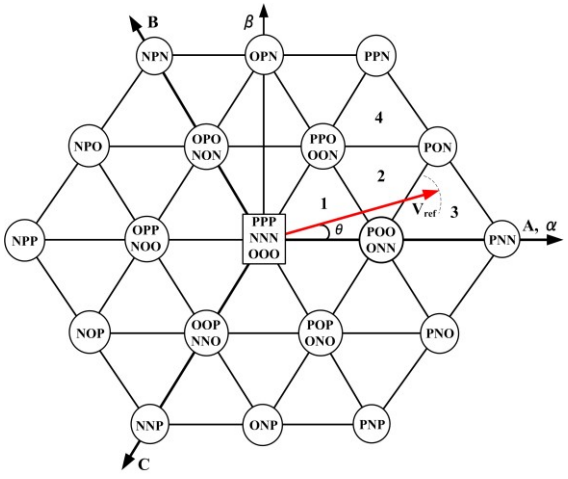


Figure 2.5 Space vector diagram for three-level NPC inverter.

Out of the 24 active vectors, 12 are small, which gives $V_{dc}/3$, 6 are medium of $V_{dc}/\sqrt{3}$, and 6 are large voltage vectors of 2Vdc/3 each. Table I shows the different switching combinations and output pole voltages. Table II shows the list of different null, small, medium, and large voltage vectors.

Table I: DIFFERENT SWITCHING STATES

Switching State	Switch Status, Phase *x* (A/B/C)				Pole Voltage (V_{xN})
	S_{x1}	S_{x2}	S_{x3}	S_{x4}	
P	1	1	0	0	$V_{dc}/2$
O	0	1	1	0	0
N	0	0	1	1	$-V_{dc}/2$

Table II: DIFFERENT SWITCHING COMBINATIONS

Switching vector combination	Voltage level
PPP,NNN,OOO	0 (Null)
PPO,OON,POO,ONN,POP,ONO,OOP, NNO,OPP,NOO,OPO,NON	$V_{dc}/3$ (Small)
PON,OPN,NPO,NOP,ONP,PNO	$V_{dc}/\sqrt{3}$ (Medium)
PNN,PPN,NPN,NPP,NNP,PNP	$2V_{dc}/3$ (Large)

Similar to the two-level SV-PWM, in a three-level inverter, the reference voltage vector is generated with a combination of the available switching states of that sector.

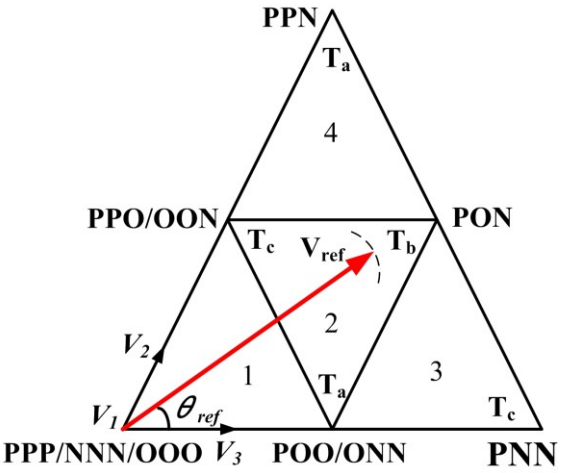


Figure 2.6 First sextant of three-level space vector.

From Fig. 2.6, it can be seen that, when the reference voltage vector is placed in subsector two, it can be represented by the available three voltage vectors; POO/ONN (V_1), PON (V_2), and PPO/OON (V_3). Hence, V_{ref} can be represented as:

$$V_{\text{ref}} \cdot T_{\text{s}} = T_{\text{a}} \cdot V_1 + T_{\text{b}} \cdot V_2 + T_{\text{c}} \cdot V_3 \tag{2.10}$$

Here, $T_{\text{s}} = T_{\text{a}} + T_{\text{b}} + T_c$

In Table III, $m = \sqrt{3}V_{\text{m}}/V_{\text{dc}}$ and $V_{\text{m}} = \sqrt{V_{\text{d}}^2 + V_{\text{q}}^2}$. In a similar manner, when the reference voltage vector moves to the other sub-sectors, it can be represented by the other three voltage

vectors, which are available there. As shown in Fig. 2.6 the time duration for those voltage vectors based on the reference vector trajectory is shown in Table III. Due to the repetitive sequence of all other sectors from 0 to 360° duration, similar equations can be derived.

Table III: SWITCHING VECTOR TIME FOR THREE-LEVEL INVERTER IN SECTOR ONE

Sub-sector	T_a	T_b	T_c
1	$T_s(2\sin(\pi/3-\theta))$	$T_s(1-2\sin(\pi/3+\theta))$	$T_s(2\sin(\theta))$
2	$T_s(1-2\sin(\theta))$	$T_s(2\sin(\pi/3+\theta)-1)$	$T_s(1-2\sin(\pi/3-\theta))$
3	$T_s(2-2\sin(\pi/3+\theta))$	$T_s(2\sin(\theta))$	$T_s(2\sin(\pi/3-\theta)-1)$
4	$T_s(2\sin(\theta)-1)$	$T_s(2\sin(\pi/3-\theta))$	$T_s(2-2\sin(\pi/3+\theta))$

2.4. Conventional DC-Link Voltage Balancing Algorithm and Associated Problems

As can be seen from Fig. 2.6 and Table II, in each sextant, there exists four types of vector combinations. They have different effects on the DC link capacitor voltage distribution.

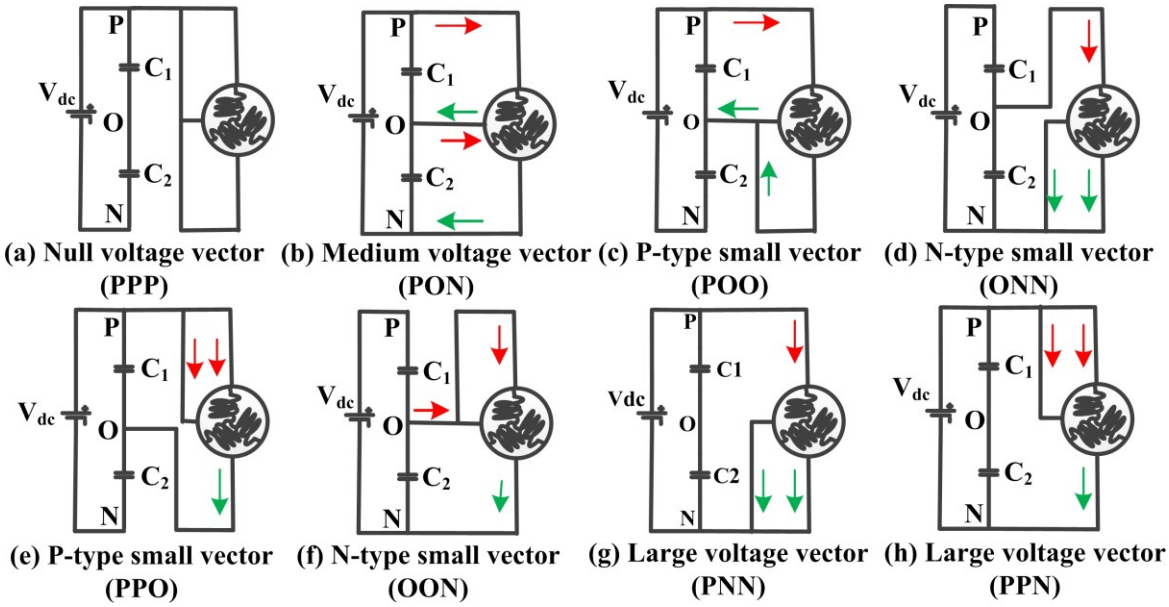


Figure 2.7 Effects of different voltage vectors on dc-link capacitor voltage.

Fig. 2.7 shows the effect of those vectors on the two capacitor voltages. Fig. 2.7(a), (b), (g) and (h) are the null, medium, and large voltage vectors, while (c), (d), (e), (f) are the small voltage vectors. Small and medium voltage vectors are mostly responsible for voltage unbalance, as they differently affect the DC link capacitors. For assumed phase current directions the positive small voltage vectors, like POO/PPO, helps discharge the upper capacitor (c, e) and the negative voltage vectors, such as ONN/OON (d, f) helps to discharge the lower capacitor. In a conventional N3V techniques based on the current direction measured from the machine terminal, a decision has to made, as to which capacitor needs to

be charged and which one needs to discharge. Eq. (2.11) shows the variation in capacitor voltage as a function of duty cycle, switching frequency, capacitance value and the output power level.

$$
\begin{aligned}
&E_1 - E_2 = P \cdot \delta \cdot T_s \\
&\therefore E_2 = E_1 - P \cdot \delta \cdot T_s \\
&\left(\frac{1}{2} \cdot C \cdot V_2^2\right) = \left(\frac{1}{2} \cdot C \cdot V_1^2\right) - P \cdot \delta \cdot T_s \\
&\therefore V_2 = \sqrt{V_1^2 - \left(\frac{2 \cdot P \cdot \delta}{C \cdot f_s}\right)} \\
&\Delta V = V_1 - V_2
\end{aligned}
\tag{2.11}
$$

Where, E_1 and E_2 are the energy stored in the capacitor before and after the discharge. V_1 and V_2 are the corresponding voltages. P is the total load power and δ is the switch on time duty. Fig. 2.8 shows the variation in capacitor voltage (ΔV) with switching frequency and capacitance value variation while load power was kept constant at 1.25 kW and duty at 0.42.

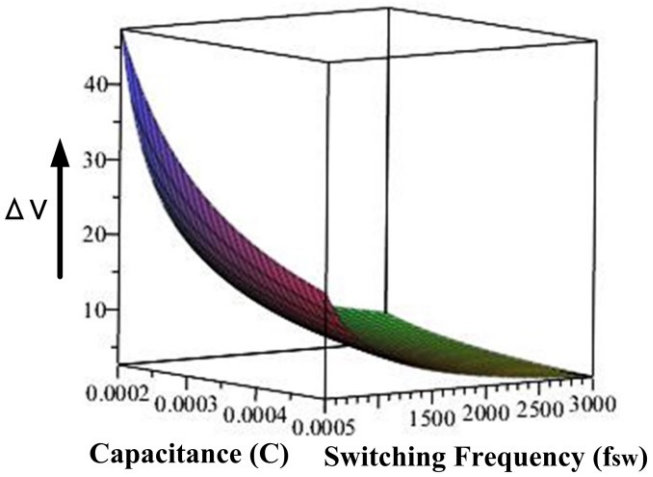


Figure 2.8 Capacitor voltage variation.

From (2.11) and fig. 2.8, it can be conclude that, with higher capacitance and switching frequency, capacitor voltage difference goes down. Moreover, it should be taking into consideration that, voltage variation also depends on the output power level and the duty ratio. So with increase in power this difference goes higher. Here, at 3.0 kHz switching frequency and with 500.0 μF capacitor the maximum capacitor voltage deviation is around 2.6 V.

To overcome the voltage unbalancing issue, there are many control strategies available as discussed in the introduction. In this chapter, the performances of the proposed scheme with the PI-based controller as well as hysteresis type controller are compared.

2.4.1. PI Controller Algorithm

As shown in Fig. 2.9, in a typical PI controller, the difference between the capacitor voltages are passed through a PI controller instead of the conditional block and output of the PI controller generates the redundant voltage vector sharing factor "*k*" [87]. The switching sequences for all sectors are shown in Table IV.

For subsector I, in 1st sector there are four redundant voltage vectors, out of which two discharge the upper capacitor C_1 (POO, PPO) and two discharge the lower capacitor C_2 (ONN, OON). So, T_1 and T_3 can be distributed into two parts: T_{1P}, T_{3P} and T_{1N}, T_{3N}, as shown in (2.12). The PI controller will generate the value of *k*. At stable condition, value of k will be around 0.5, when both the capacitor voltages are equal. However, in practical scenarios, "*k"* cannot be constant, and it keeps on varying with motor speed and load torque variation. Because of this variation, the ON-time for the switches for each cycle keeps varying, which leads to unsymmetrical switching and increased total harmonic distortion in the generated voltage. This effect is more visible in low speed regions, which is proved experimentally later in this thesis. Also, due to the difference in availability of the switching vectors, the switching sequence is different for different sub-sectors, which also leads to variable switching frequency.

$$T_1 = kT_{1P} + (1-k)T_{1N} \qquad (2.12)$$
$$T_3 = kT_{3P} + (1-k)T_{3N}$$

Table IV: VECTOR SEQUENCE FOR PI CONTROLLER BASED DC-LINK VOLTAGE BALANCING

Sector	Sub-sector	Switching Sequence
1	1	NNN-ONN-OON-OOO-POO-PPO-PPP-PPO-POO-OOO-OON-ONN-NNN
	2	ONN-OON-PON-POO-PPO-POO-PON-OON-ONN
	3	ONN-PNN-PON-POO-PON-PNN-ONN
	4	PPO-PPN-PON-OON-PON-PPN-PPO

2.4.2. Hysteresis Controller Algorithm

Two similar approaches are proposed in [97], [110] and the switching sequence of them are shown in Table V. It can be seen that all the subsectors have same number of sequences, compared to the earlier PI controller based scheme, which makes the duty ratio constant.

However, in sector three and four, both positive and negative sequence vectors are used, so that the average currents drown from the capacitors are balanced.

Table V: HYSTERESIS CONTROLLER BASED DC-LINK VOLTAGE BALANCING

Sector	Sub-sector	Balancing Ability	Switching Sequence
1	1	ONN/POO>OON/PPO	ONN-OON-OOO-POO-OOO-OON-ONN
		OON/PPO>ONN/POO	OON-OOO-POO-PPO-POO-OOO-OON
	2	ONN/POO>OON/PPO	ONN-OON-PON-POO-PON-OON-ONN
		OON/PPO>ONN/POO	OON-PON-POO-PPO-POO-PON-OON
	3		ONN-PNN-PON-POO-PON-PNN-ONN
	4		OON-PON-PPN-PPO-PPN-PON-OON

Furthermore, the appropriate sequence is selected for subsector one and two, depending on the capacitor voltage difference. This type of technique may be preferable for low transient system operation. However, for EV traction applications, due to high dynamic performance, the capacitor voltage may change differently. Moreover, due to the change in switching sequence in between switching cycle will increase the inverter switching losses.

2.4.3. Proposed DC-link Voltage Balancing Algorithm

To overcome the problem with variable switching frequency for different sub-sectors in Table V and to increase the controllability of the DC-link capacitors for wide speed and torque range with reduced switching losses, an innovative switching sequence is proposed, as shown in Table VI. The total number of switching in each subsector is five, which is less than the other switching schemes. It helps to reduce the addition switching sequence corresponding losses. Also, since switching sequences are selected depending on the difference in the two capacitor voltages at each time period T_s, this scheme is more useful and robust for PMSM drive applications in transient as well as in steady state conditions. It can also be observed that, in each sequence, one of the switching combinations does not change (for instance, in sector one subsector one, 3rd voltage vector O is constant), which reduces the switching losses further.

However, according to this strategy once the duty cycle is specified, due to the change in the capacitor voltages, the switching sequence may change in between the total switching time period T_s, which may lead to asymmetrical switching.

To overcome this problem, the change in switching state is allowed only at the starting of each switching cycle (T_s). It makes the generated PWM more symmetrical. As shown in Fig. 2.9, the control logic block takes the difference in two capacitor voltages and the carrier

signal of the SV-PWM as inputs. When the capacitor voltage difference is positive ($V_1 > V_2$) or negative ($V_2 > V_1$), the output of the control logic block will give one or zero. This will choose the appropriate voltage vector from Table VI.

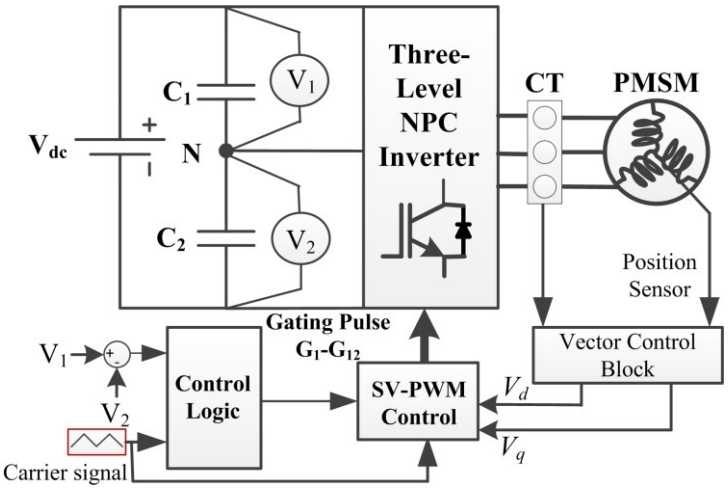


Figure 2.9 Three-level inverter and control strategy model.

Table VI: PROPOSED DC-LINK VOLTAGE BALANCING SEQUENCE

Sector	Sub-sector	Balancing Ability	Switching Sequence
1	1	$V_{dc1}>V_{dc2}$	OOO-POO-PPO-POO-OOO
		$V_{dc2}>V_{dc1}$	NNN-ONN-OON-ONN-NNN
	2	$V_{dc1}>V_{dc2}$	PON-POO-PPO-POO-PON
		$V_{dc2}>V_{dc1}$	ONN-OON-PON-OON-ONN
	3	$V_{dc1}>V_{dc2}$	POO-PON-PNN-PON-POO
		$V_{dc2}>V_{dc1}$	ONN-PNN-PON-PNN-ONN
	4	$V_{dc1}>V_{dc2}$	PPO-PPN-PON-PPN-PPO
		$V_{dc2}>V_{dc1}$	OON-PON-PPN-PON-OON

2.5. Simulation Results

All the simulation studies are carried out in Matlab/ Simulink® Platform, the DC-link capacitor voltage was kept constant at 270.0 V and the capacitor values are 500.0 μF each. All the machine parameters are provided in the appendix A. Figs. 2.10, 2.11 and 2.12 shows the performance of PI controller based algorithm, the proposed control strategy, and the proposed control strategy with the reduction in harmonic distortion. In the simulation setup machine speed, phase voltage, DC-link capacitor voltage difference, and the stator currents are compared. Speed is increased from 150.0 rpm to 800.0 rpm, and the variations in other waveforms are observed. From the phase voltage waveform, it can be observed that, number

of steps or level has increased for all the three strategies with change in speed, which makes the phase voltage more sinusoidal. From the difference of the capacitor voltages, it can be observed that the PI controller based algorithm is good for a system with low transients. The PI controller has a specific settling time in terms of dynamic machine performance, which may be lead to switch damage due to overvoltage.

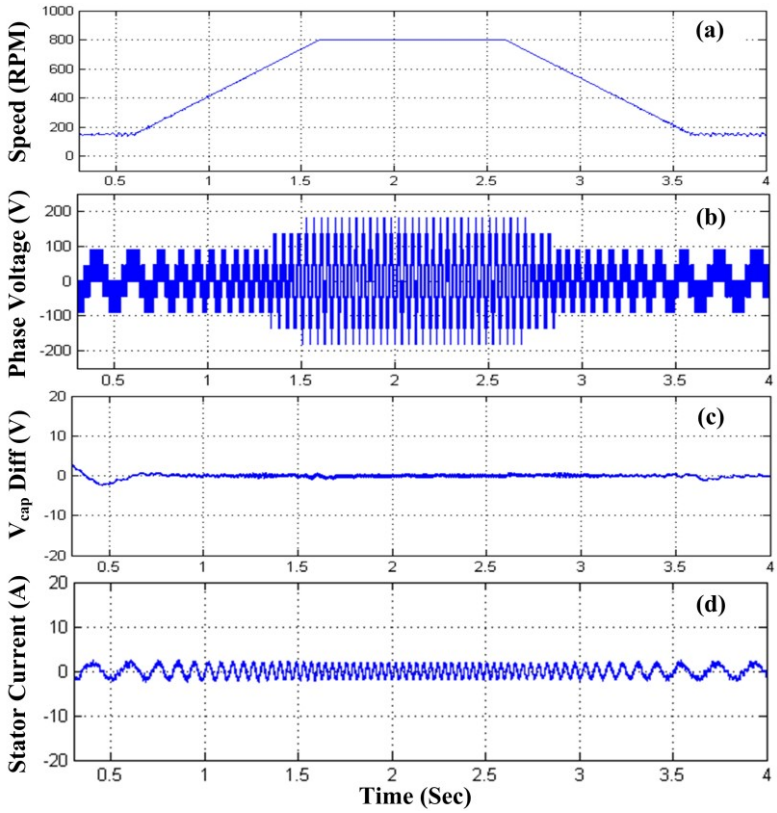


Figure 2.10 Simulation results for PI controller based algorithm, with change in speed from 150.0 rpm to 800.0 rpm; (a) Motor speed; (b) Phase voltage; (c) Difference in two capacitor voltages; (d) Stator current.

From the comparison study of the DC-link capacitor voltage variation, it can be observed that the variation is (NPP) 1.0 V for PI controller based strategy, 0.3 V for the proposed control strategy and 1.4 V for the proposed control strategy with low order harmonic reduction based strategy. Moreover, an initial difference in capacitor voltages for PI controller based algorithm below 0.7 seconds can also be observed, which is not present for the other two control algorithms. This initial offset is present, due to the settling time of the PI based controller. There is not much difference in steady state currents for all the control strategies.

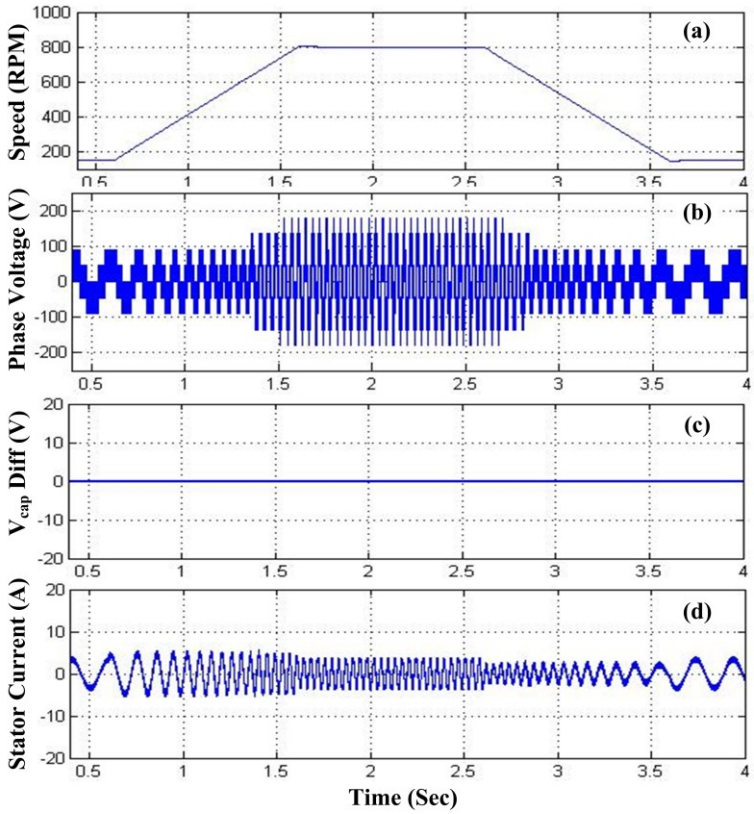


Figure 2.11 Simulation results for proposed DC-link voltage balancing algorithm, with change in speed from 150.0 rpm to 800.0 rpm; (a) Motor speed; (b) Phase voltage; (c) Difference in two capacitor voltages; (d) Stator current.

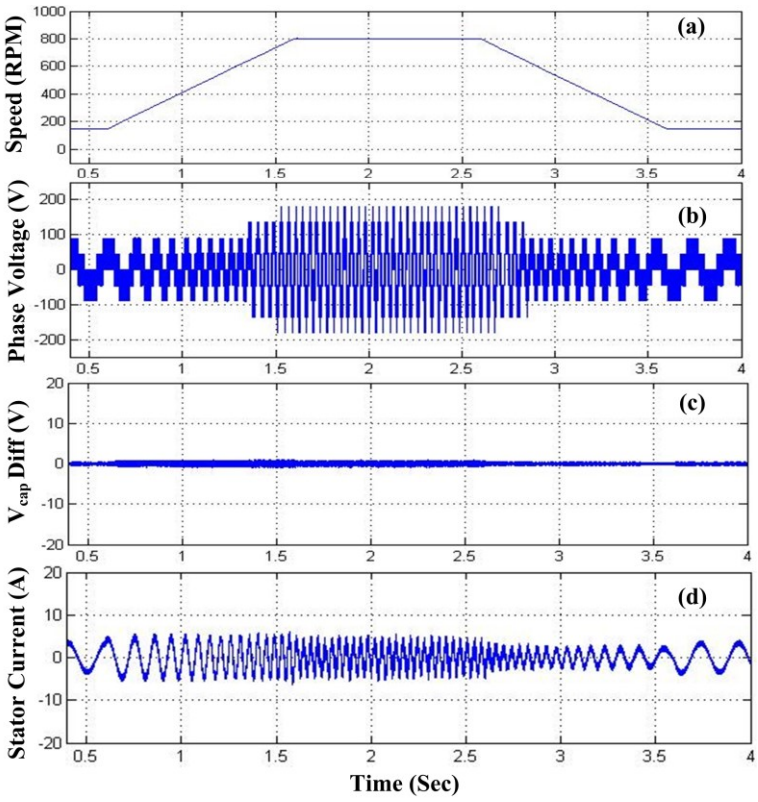


Figure 2.12 Simulation results for proposed DC-link voltage balancing algorithm, with reduced low harmonic distortion while change in speed from 150.0 rpm to 800.0 rpm; (a) Motor speed; (b) Phase voltage; (c) Difference in two capacitor voltages; (d) Stator current.

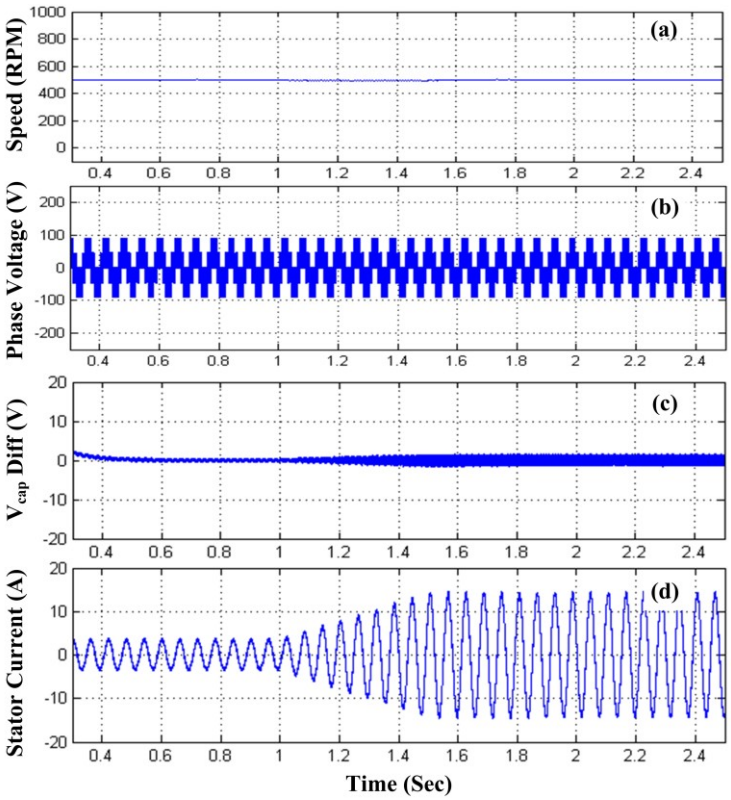


Figure 2.13 Simulation results for PI controller based algorithm, with change in load torque from 6.0 N-m to 24.0 N-m; (a) Motor speed; (b) Phase voltage; (c) Difference in two capacitor voltages; (d) Stator current.

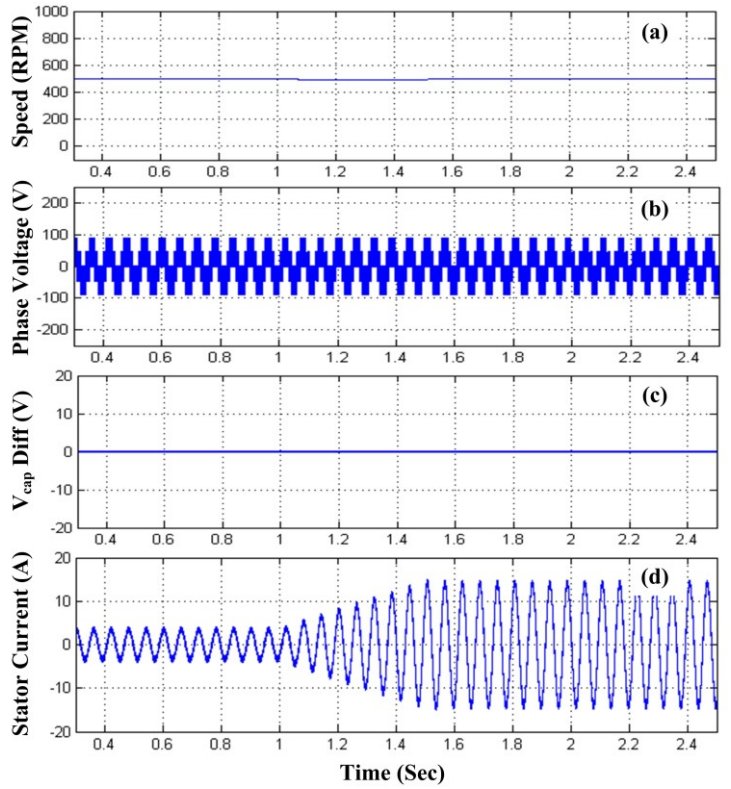


Figure 2.14 Simulation results for proposed DC-link voltage balancing algorithm, with change in load torque from 6.0 N-m to 24.0 N-m; (a) Motor speed; (b) Phase voltage; (c) Difference in two capacitor voltages; (d) Stator current.

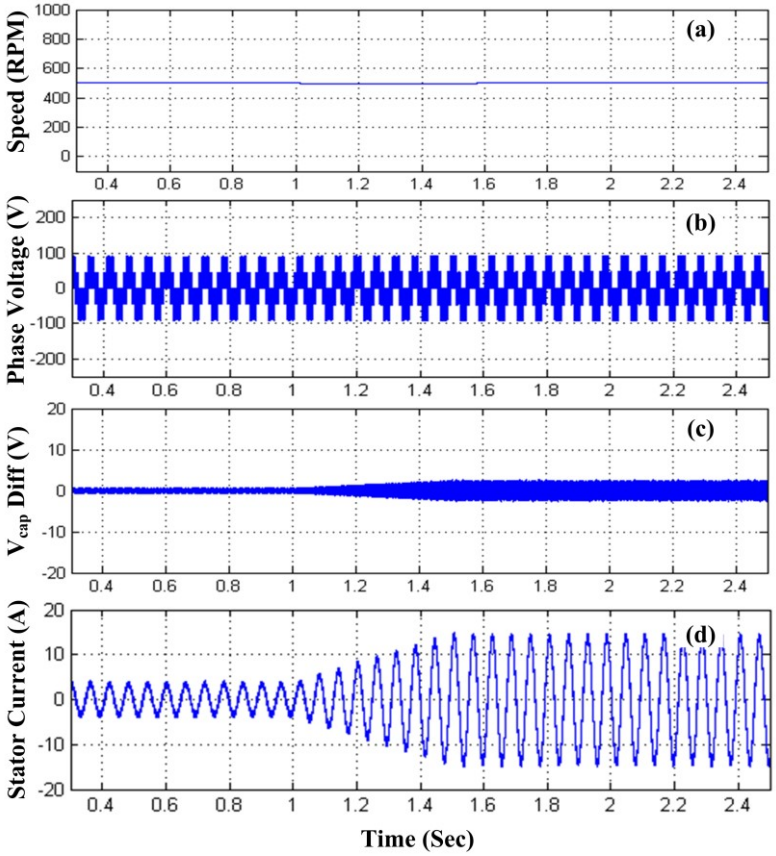


Figure 2.15 Simulation results for proposed DC-link voltage balancing algorithm with reduced low harmonic distortion, with change in load torque from 6.0 N-m to 24.0 N-m; (a) Motor speed; (b) Phase voltage; (c) Difference in two capacitor voltages; (d) Stator current.

In Figs. 2.13, 2.14, and 2.15, the load torque is changed from 6.0 N.m. to 24.0 N.m., while speed was kept constant at 500.0 rpm; and changes in capacitor voltages are observed.

As is clear from the results, the capacitor voltages are balanced and the differences for the three control strategies are as follows: for the PI controller based topology, it is 4.0 V, for the proposed control strategy, it is 0.4 V, and for the proposed control strategy with low order harmonic reduction, it is 4.0 V. It can be observed that capacitor voltage difference of the proposed control strategy is 10% of the PI control based topology. Though, low order harmonic reduction based technique has almost the similar voltage difference as of PI based strategy, proposed strategy has lower low order harmonics and batter controllability of the DC-link capacitor voltages, compared to the PI based topology. The difference in the capacitor voltages between the two new control strategies exists, due to the fact that the second strategy uses less number of switching modes, compared to the other one. The phase voltage waveforms and steady-state armature currents are almost similar, with good controllability of machine speed, during change in load torque.

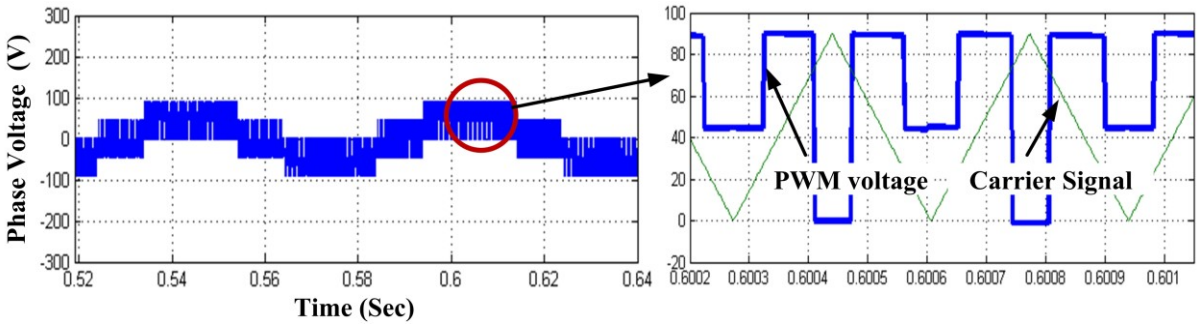


Figure 2.16 Phase voltage at a mdulation index (M.I.) of 0.33 with carrier signal.

Fig. 2.16 shows the phase voltage waveform with the proposed control strategy at a modulation index of 0.33. Two switching cycles of the phase voltage are shown, with the carrier waveform proving that the proposed control strategy works with symmetrical switching frequency. It can be observed that phase voltage is symmetrical on both sides of the middle of carrier signal.

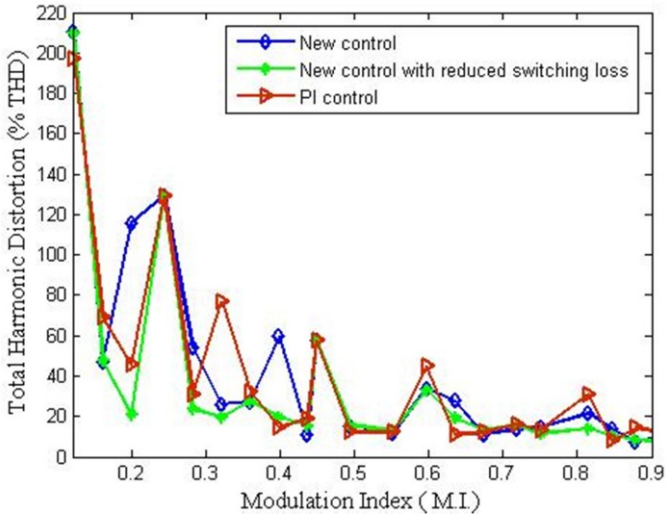


Figure 2.17 Total harmonic distortion (%THD) comparison of phase voltages.

Fig. 2.17 shows the comparison of the phase voltage %THD of the three control strategies for different modulation indices. The new control strategies depict almost the same THD as the PI based controller for low modulation indices and have better performance for high modulation indices.

2.6. Experimental Setup and Test Results

Detailed experimental studies are carried out to show the performance of the proposed system. The control strategies are implemented using dspace® based real time implementation tool, the DC-link capacitor voltage was kept constant at 270.0 V and the capacitor values are 500.0 µF each. Simulation step time was kept at 25µsec. The switching frequency of the carrier was kept constant at 3.0 kHz. During the experimental procedure, the DC-link voltage

was kept constant at 270.0 V. Fig. 2.18 shows the experimental setup for a three-level inverter, which feeds a surface PMSM. A DC dynamometer was used to load the machine.

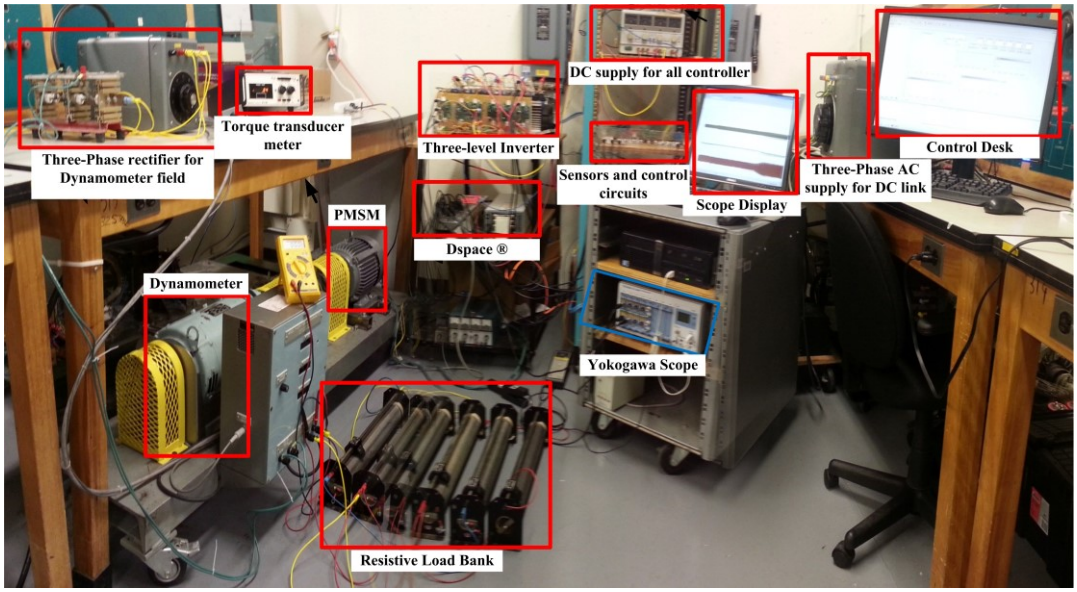


Figure 2.18 Experimental setup for the three-level inverter.

Figs. 2.19 to 2.21 show the experimental test results for speed change from 150.0 rpm to 800.0 rpm using PI and the two new proposed control strategies. From the experimental results of the PI controller based algorithm, it can be observed that the DC-link voltage variation is almost 30.0 V at low speed and at high speed it is about 8.0 V. Hence, as a result, a large voltage deviation occurs, which may increase the dv/dt value, and damage the switches.

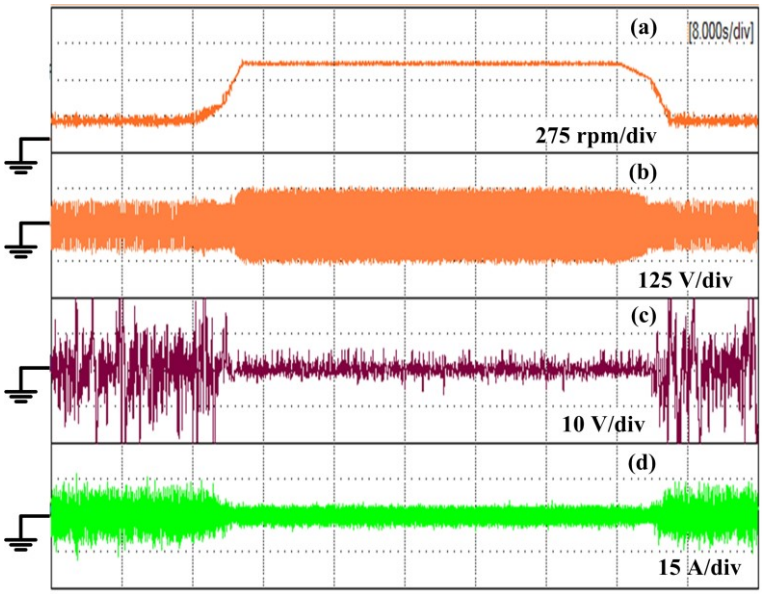


Figure 2.19 Experimental results for PI controller based algorithm, with change in speed from 150.0 rpm to 800.0 rpm; (a) Motor speed; (b) Phase voltage; (c) Difference in two capacitor voltages; (d) Stator current.

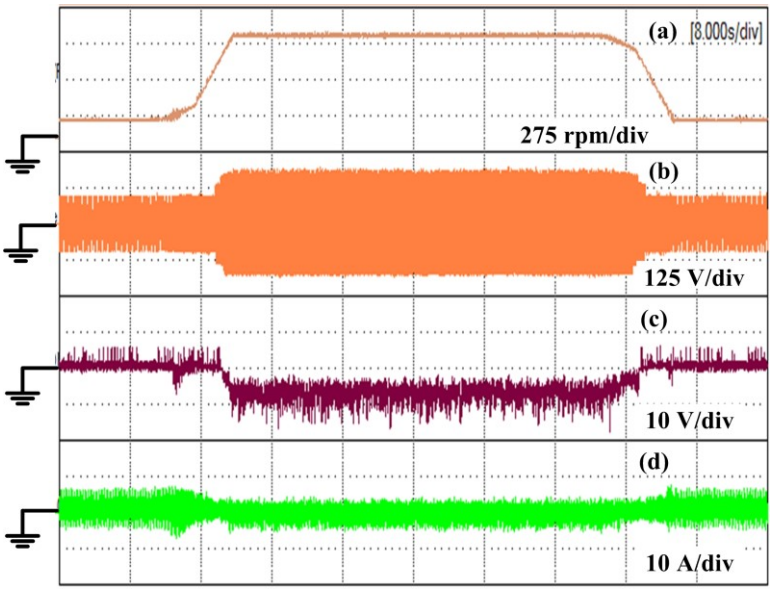


Figure 2.20 Experimental results for proposed DC-link voltage balancing algorithm, with change in speed from 150.0 rpm to 800.0 rpm; (a) Motor speed; (b) Phase voltage; (c) Difference in two capacitor voltages; (d) Stator current.

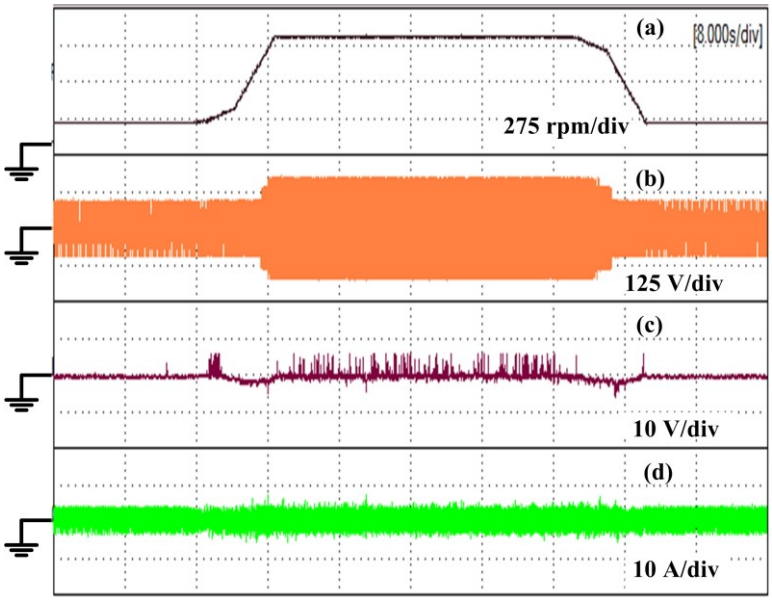


Figure 2.21 Experimental results for new DC-link voltage balancing algorithm, with reduced low harmonic distortion, with change in speed from 150.0 rpm to 800.0 rpm; (a) Motor speed; (b) Phase voltage; (c) Difference in two capacitor voltages; (d) Stator current.

On the other hand, the voltage deviation between the two capacitor voltages for the proposed balancing strategies is about 5.0 V. This is much lower than the PI based control strategy, which saves the switches from high voltage breakdown. The proposed control strategy with reduced low order harmonic has a much lower DC-link voltage difference compared to the second control strategy.

Also the capacitor voltage differences are at a steady DC-level. Phase voltage wave shapes are almost similar, with increased in number of voltage levels, with change in speed. With the PI based controller, the stator current has more spikes and transients, compared to the other controller, which is due to the poor controllability of the capacitor voltages.

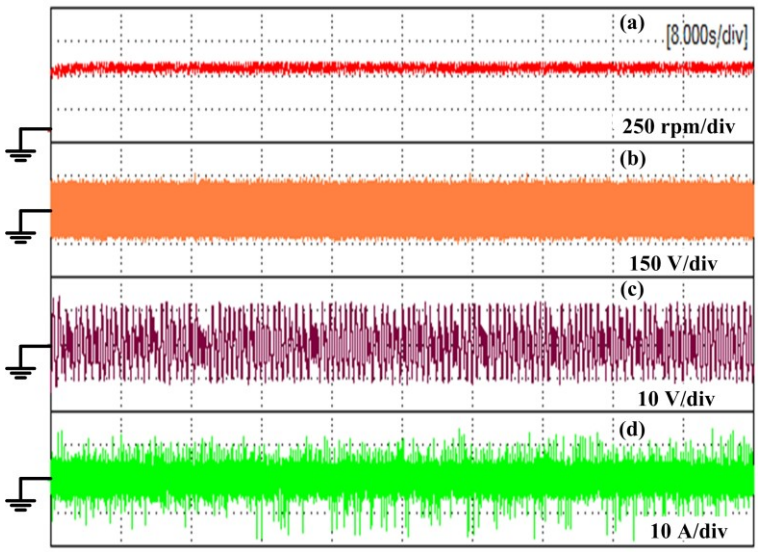


Figure 2.22 Experimental results for the PI control algorithm, with 6.0 N-m load torque (a) Motor speed; (b) Phase voltage; (c) Difference in two capacitor voltages; (d) Stator current

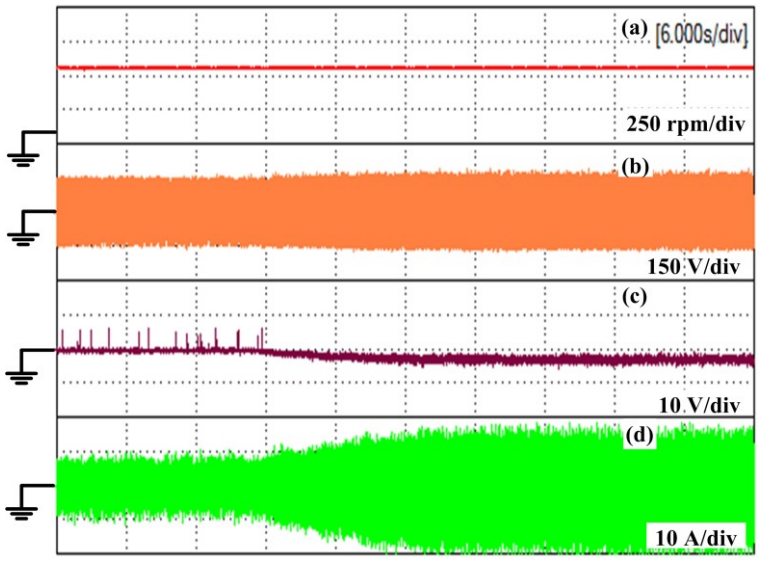


Figure 2.23 Experimental results for proposed DC-link voltage balancing algorithm, with change in load torque from 6.0 N-m to 24.0 N-m; (a) Motor speed; (b) Phase voltage; (c) Difference in two capacitor voltages; (d) Stator current.

Figs. 2.22 to 2.24 show the performance of the system during change in load torque from 6.0 N.m. to 24.0 N.m. Speed of the motor was kept fixed at 500.0 rpm. It can be observed that the capacitor voltage variation is now 30.0 V even at no load, and due to this large voltage variation, load change was not possible to be performed for the PI control strategy.

This increase in voltage difference occurs, because of the voltage fluctuation in the low speed region.

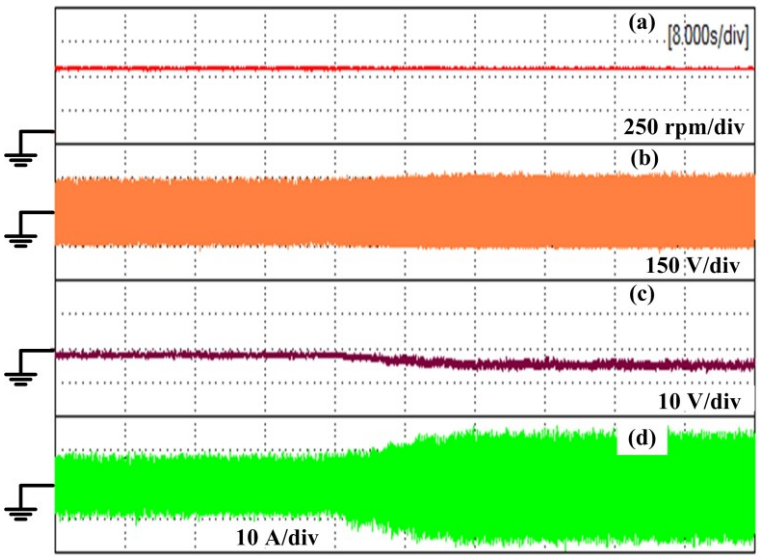


Figure 2.24 Experimental results for new DC-link voltage balancing algorithm, with reduced low harmonic distortion, with change in load torque from 6.0 N-m to 24.0 N-m; (a) Motor speed; (b) Phase voltage; (c) Difference in two capacitor voltages; (d) Stator current.

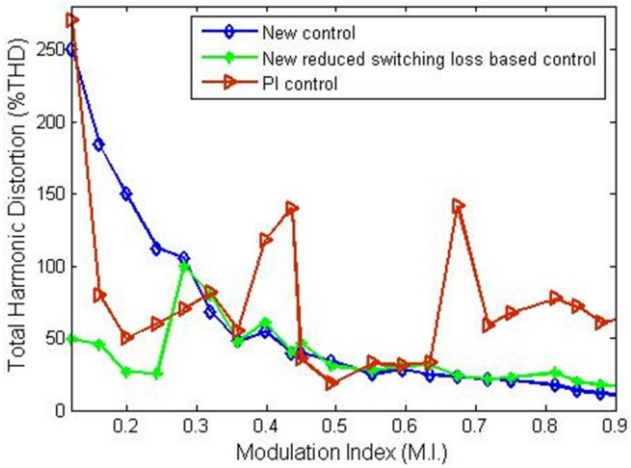


Figure 2.25 Total harmonic distortion (%THD) comparison of phase voltages.

Due to the large voltage fluctuation in positive and negative direction in PI controller at low speeds, compared to the proposed controller, a large amount of clockwise and counter clockwise forces are inflicted on the machine shaft. This loosens the coupling, which in turn, creates large voltage deviations even in the high-speed range. The capacitor voltage deviation for the two new proposed control strategies are around 4.0 V, which is about 1.48% of the total DC link voltage. For the similar stator current, the PI controller has high phase current transients, compared to the other strategies, even at lower torque values, because of the

reason stated above. All the other control strategies have better phase current shapes; moreover, the capacitor voltage difference is also steady.

Fig. 2.25 shows the total harmonic distortion (%THD) comparison for the three schemes. It can be observed that the PI based topology has much more distortion compared to the proposed strategies, as predicted. This is due to the variation of sharing factor "k", in transient condition and change in duty in between switching cycles. The new proposed control strategy with lower low order harmonic distortion strategy has reduced voltage distortion compared to the basic one.

2.7. Effects of Lagging Power Factor on DC-link Capacitor Voltages

Fig. 2.26 shows the states of the two capacitors while phase current changes its direction. For positive phase current direction (a, e), vectors associated with upper capacitor in sector-I (POO/PPO) is going to discharge and for reverse current direction it will be going to charge (b, f). Same is true for the redundant voltage vectors associated with the lower capacitor (c, d, g, h). Hence, if the system power factor gets below a certain level, the DC-link capacitor is going to charge, when they requires to discharge and may get discharge, when they needs to charge to keep the two capacitor voltages balanced. In earlier proposed work, system power factor was assumed to be high enough, so that this situation does not occur. However, a system with lower power factor like as in the case for induction machine or synchronous reluctance machine, it might be essential to take current direction into consideration.

Fig. 2.27 shows the change in phase current direction with change in power factor angle (0° to 90°) for sector I, II and III. Fig. 2.27 (a), (b) shows the current directions associated with the redundant voltage vectors POO and PPO for sector I. Phase A current I_a associated with POO is positive for the entire range of power factor. However, I_c associated with PPO has gone positive after certain power factor, which will affect the DC-link capacitor voltage deviation, if proper switching states are not taken into consideration. Sector II and III has the same trend, where the first set of redundant voltage vectors showed in c, e (PPO, OPO) do not change their direction with power factor angle, and only the second set of vectors d, f (OPO, OPP) changes its direction. Hence, the switching sequences associated with 1, 2 and 4 sub-sectors only needs to be changed instead of the entire subsectors as generally proposed by researchers. Moreover, there is a maximum power factor angle, below which power factor correction need not to be considered. Hence, for applications where power factor angle is below that critical value (φ_{cr}), the current direction is independent of the capacitor voltage balancing capability.

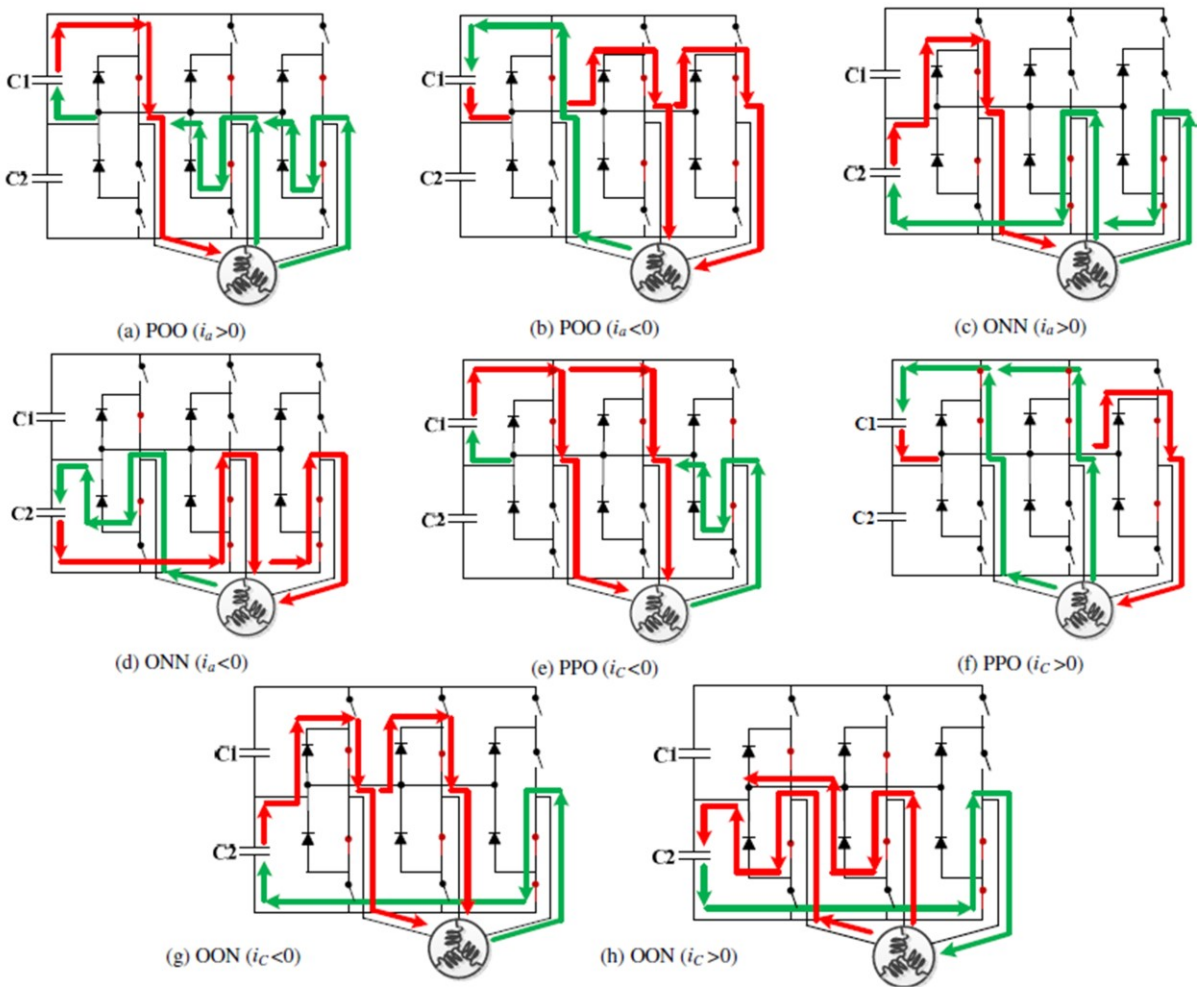


Figure 2.26 Different vector combination and their effects on DC-link capacitor voltage based on current direction.

Equation (2.13) shows the analytical derivation of the critical value the power factor angle (φ_{cr}). In sector I, as shown in Fig. 2.27 (b) phase C current I_c changes its direction and goes positive after certain power factor angle. Let's consider it as φ_{cr} when I_c is zero.

$$I_m \cdot \sin(\theta - \varphi_{cr} - 4 \cdot \Pi/3) = \sin(n \cdot \Pi) \tag{2.13}$$

Here, $\theta = \Pi/2$, as θ is in sector-I and $I_m \neq 0$

$$\therefore \varphi_{cr} = \Pi/6$$

Hence, it can be concluded that if, the system power factor is below 30° it will not affect the capacitor voltage balancing capability of the 3-level inverter. Henceforth, as permanent magnet machines operate at high power factor, it will not affect the capacitor voltage ability of DC-link. A modified control strategy is presented in the following section and detailed simulation and experimental studies are carried out.

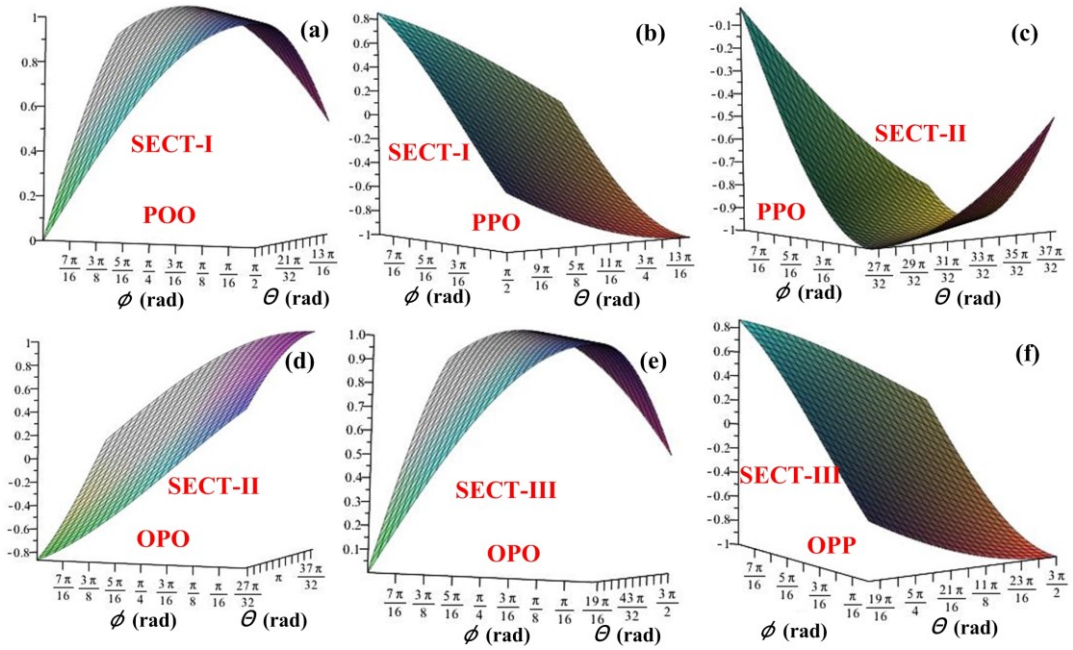


Figure 2.27 Change in current direction with power factor angle.

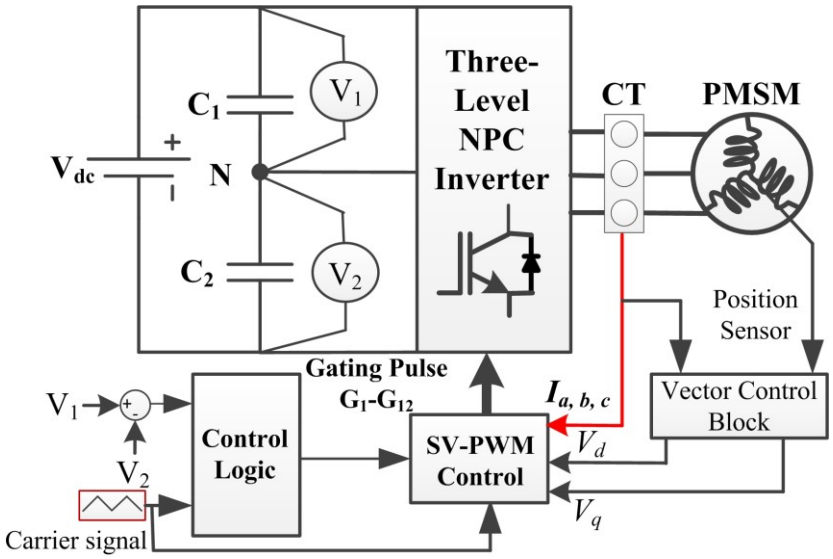


Figure 2.28 Three-level inverter and control strategy model.

2.8. Modified DC-link voltage balancing algorithm

Fig. 2.28 shows the control circuit diagram of the proposed balancing scheme with stator three phase currents taken into consideration. The difference between the two capacitor voltages is passed through a control logic block, which gives the command signal for the SV-PWM. The command signal changes its state only at the start of each switching cycle to reduce the possibility of asymmetrical switching, as already explained in the earlier proposed SV-PWM strategy.

The difference between the previously proposed strategy and the modified strategy is the presence of the current sensing block which is used in the SV-PWM controller. The vector sequence for the earlier scheme is shown in Table VI for sector I, and the modified strategy corresponding switching sequences for sector I is shown in Table VII.

Table VII: MODIFIED DC-LINK VOLTAGE BALANCING ALGORITHM

Sector	Sub-Sector	Balancing Ability	Current Direction	Switching Sequence
1	1	$V_{dc1}>V_{dc2}$	$I_c<0$	OOO-POO-PPO-POO-OOO
			$I_c>0$	OOO-POO-OON-POO-OOO
		$V_{dc2}>V_{dc1}$	$I_c<0$	NNN-ONN-OON-ONN-NNN
			$I_c>0$	NNN-ONN-PPO-ONN-NNN
	2	$V_{dc1}>V_{dc2}$	$I_c<0$	POO-PPO-PON-PPO-POO
			$I_c>0$	POO-OON-PON-OON-POO
		$V_{dc2}>V_{dc1}$	$I_c<0$	ONN-OON-PON-OON-ONN
			$I_c>0$	ONN-PPO-PON-PPO-ONN
	3	$V_{dc1}>V_{dc2}$	$I_a>0$	POO-PON-PNN-PON-POO
		$V_{dc2}>V_{dc1}$	$I_a>0$	ONN-PNN-PON-PNN-ONN
	4	$V_{dc1}>V_{dc2}$	$I_c<0$	PPO-PPN-PON-PPN-PPO
			$I_c>0$	OON-PON-PPN-PON-OON
		$V_{dc2}>V_{dc1}$	$I_c<0$	OON-PON-PPN-PON-OON
			$I_c>0$	PPO-PPN-PON-PPN-PPO

2.9. Simulation Results

All the simulation parameters are kept as its previously set values. Fig. 2.29 shows the simulation results for change in speed from 150.0 rpm to 800.0 rpm, while load torque was kept constant at 6.0 N.m. Fig. 2.30 shows the performance of the system with change in load torque from 6.0 N.m. to 24.0 N.m. During the change in load torque, speed was kept constant at 500.0 rpm. From the simulation results it can be observed that, with the proposed control strategy the DC-link capacitor voltage was kept well below 2.5 % of the total DC-link capacitor voltage. Moreover, modified control strategy shows almost the similar results as the earlier proposed strategy. This is because of the high power factor operation of the surface PMSM, which is below 30° and hence, lagging power factor does not affect the DC-link voltage balancing capability to a large extent.

Fig. 2.31 shows the total harmonic distortion comparison for the both proposed control strategies. Although, both of them follows the same trend, the modified control strategy shows a reduced order harmonic distortion compared to the earlier proposed control strategy.

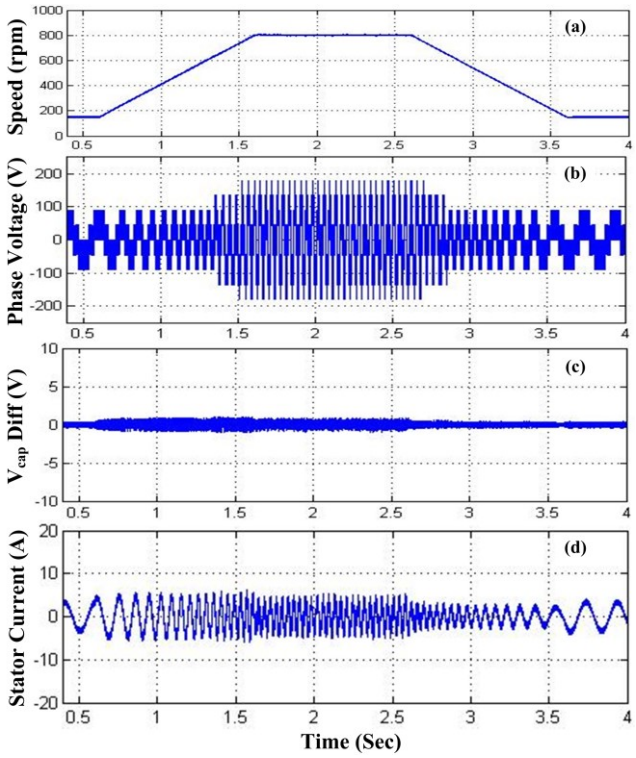


Figure 2.29 Performance results for the three-level inverter with the modified control strategy during change in speed from 150.0 rpm to 800.0 rpm; (a) Change in machine speed; (b) Phase voltage; (c) Difference between the two DC-link capacitor voltages; (d) Stator current.

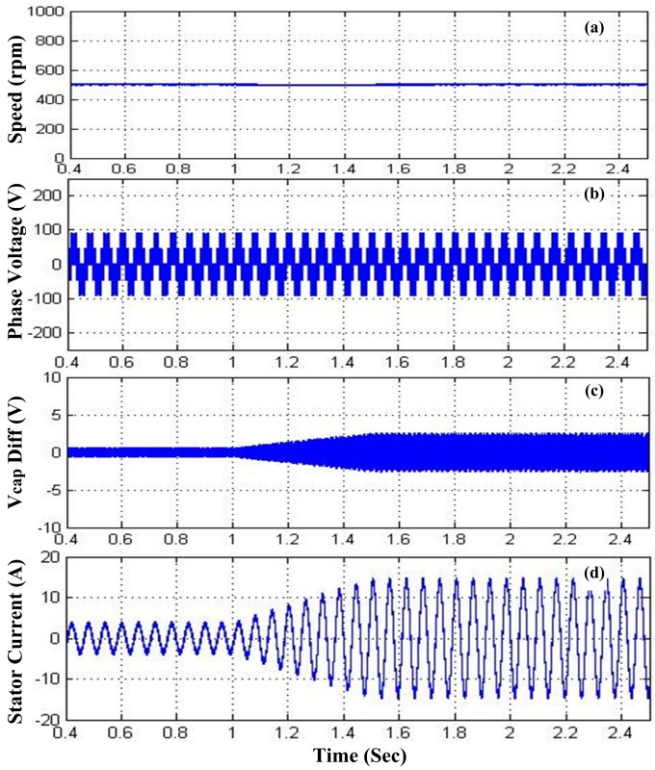


Figure 2.30 Performance results for the three-level inverter with the modified control strategy during change in load torque from 6.0 N.m. to 24.0 N.m. at 500.0 rpm; (a) Change in machine speed; (b) Phase voltage; (c) Difference between the two DC-link capacitor voltage; (d) Stator current.

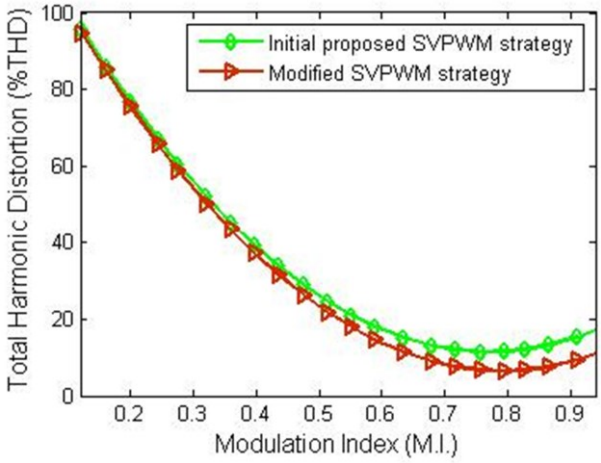


Figure 2.31 Total harmonic distortion comparison for both control strategies.

2.10. Experimental Verification

Hardware testing is done with the same 6.0 kW surface PMSM as mentioned before. Fig. 2.32 shows the result with change in machine speed from 150.0 rpm to 800.0 rpm, at 6.0 N.m. of load torque and Fig. 2.33 shows the result with the change load torque from 6.0 N.m. to 24.0 N.m., while machine speed kept constant at 500.0 rpm. From both the control strategy results, it can be concluded that the controller is able to keep the DC-link capacitor voltages at the desired tolerance level. Results are quite similar with the earlier proposed SV-PWM strategy, as also verified by the simulation studies.

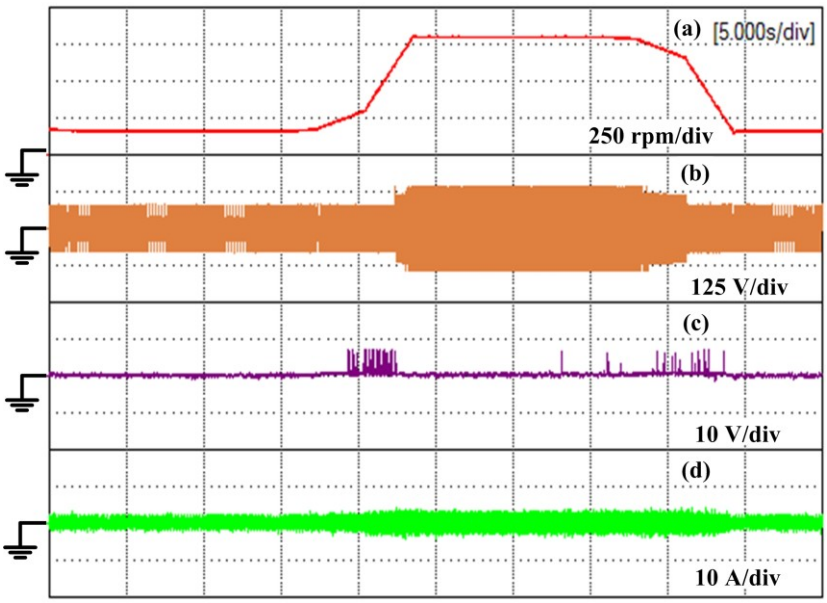


Figure 2.32 Experimental results for the three-level inverter with the modified control strategy during change in speed from 150.0 rpm to 800.0 rpm; (a) Change in machine speed; (b) Phase voltage; (c) Difference between two DC-link capacitor voltages; (d) Stator current.

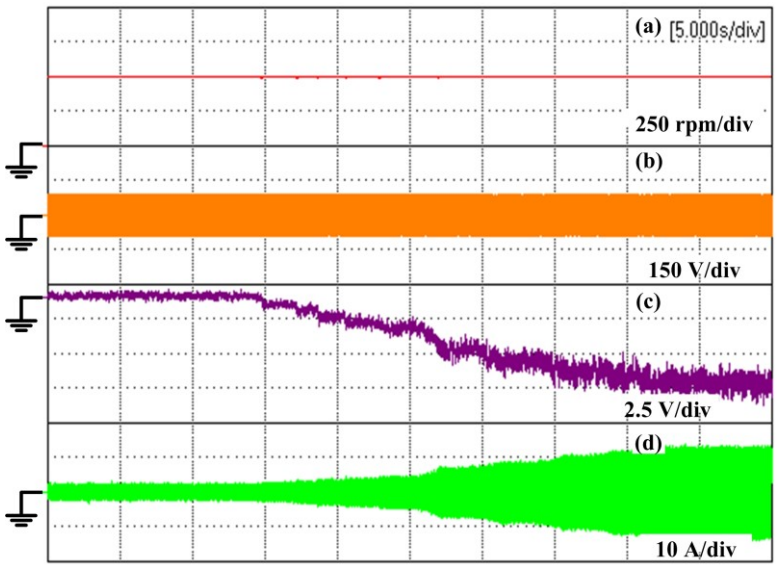


Figure 2.33 Experimental results for the three-level inverter with the modified control strategy during change in the load torque from 6.0 N.m. to 24.0 N.m. at 500.0 rpm; (a) Change in machine speed; (b) Phase voltage; (c) Difference between the two DC-link capacitor; (d) Stator current.

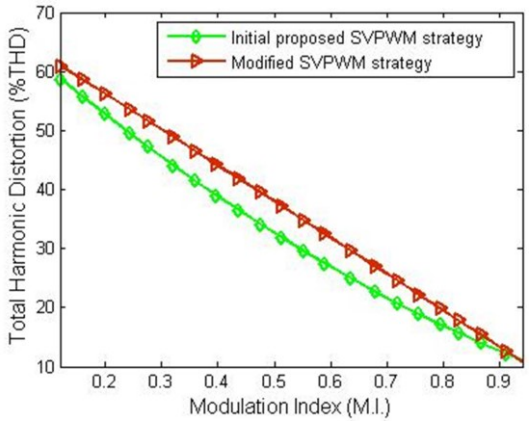


Figure 2.34 Experimental results for total voltage harmonic distortion comparison for both control strategies.

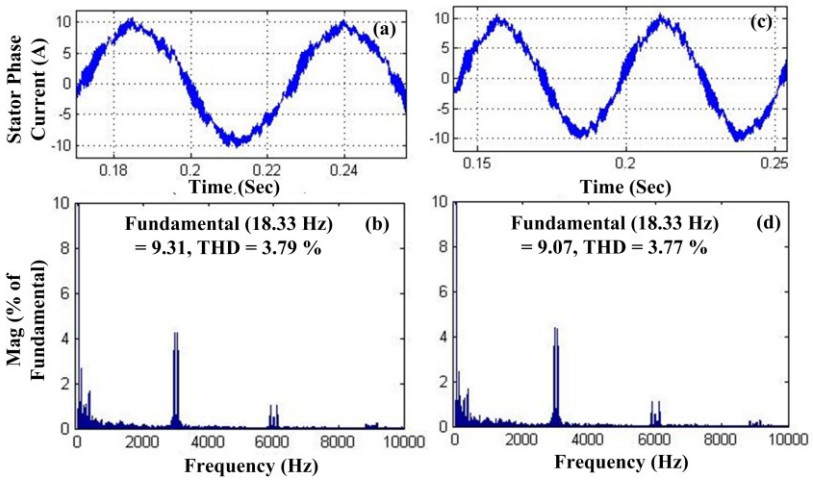


Figure 2.35 Experimental results for total current harmonic distortion comparison for both control strategies; (a, b) Corresponds to the initially proposed SV-PWM strategy, (c, d) for the modified SV-PWM strategy.

Figs. 2.34, 2.35 show the total voltage and current harmonic distortion comparison for both the control strategies. Both of them follows the similar strand as already been seen from the simulation studies. During the current harmonic distortion calculation, the system was run at 18.33 Hz and 0.44 modulation index.

2.11. Performance Comparison between Simulation and Experimental Results

2.11.1. PI based control algorithm

There is a significant difference observed between the simulation and experimental results for the PI-based control algorithm. Due to the mechanical bend in the motor shaft, DC-link voltage fluctuations as well as the PI controller settling-time, a cumulative action occurs. Hence, the DC-link capacitor voltage variation is larger in experiments, compared to the simulation studies. This phenomenon also reflects in the motor armature current.

2.11.2. Novel, reduced harmonic DC-link voltage balancing strategy

In this case, the simulation and experimental results follow almost the similar pattern. However, hardware experimental results have much more transients than the simulation results. This is because, in case of the experiments, there exists a time delay between two complementary switches, to prevent shoot through faults; this introduces additional harmonics. This occurrence can also be observed from the %THD comparison between the simulation and experimental results. Moreover, the DC-link capacitor voltage variation observed in the experimental results is slightly higher than those observed in the simulation results. Since it is challenging to get the actual value of motor inertia and other mechanical parameters, an additional load factor is superimposed on the practical setup, which in turn, affects the DC-link capacitor voltage deviation. Same argument hols for the modified SV-PWM control strategy for lagging power factor operation as well.

2.12. Summary of Chapter 2

This chapter introduced different permanent magnet synchronous machines (PMSM) available and their application for electric vehicle (EV). Mathematical modelling of PMSM is also carried out. It is then followed by space-vector PWM (SV-PWM) technique of three-level inverter and their duty cycle calculation. Available DC-link voltage balancing topology is described and a new reduced switching loss based DC-link voltage balancing topology is proposed. The proposed strategy is than further extended to reduce the effect of lagging power factor. Detail simulation and experimental studies have been carried out to verify the performance of the proposed system. Results show satisfactory transient and steady state

performance of the proposed system with improved total voltage and current harmonics distortion (THD).

Chapter 3. Performance Comparison Study of Two and Three-Level Inverter Drives for the Surface PMSM

To perform a comparison study between two- and three-level inverter based PMSM drive, a two-level inverter is implemented. Both the simulation and experimental studies are carried out to compare the total harmonic distortion (THD), capacitor current ripple with a 6 kW SPMSM and 300.0 V DC-link voltage. To compare the switch losses (Conduction and switching), total inverter losses, torque ripple and capacitor voltage differences a 54.0 kW SPMSM, generally being used for electric vehicle (EV) applications is considered with 600.0 V of DC-link voltage.

3.1. Space Vector Pulse Width Modulation (SV-PWM) for Two-level Inverter

Fig. 3.1 shows the two-level inverter based PMSM traction drives connected with a car wheel. I_{invrms}, I_{invavg}, I_{caprms} are the RMS value of total inverter current supplied to the load, average current supplied by battery and the RMS ripple current supplied by the DC-link capacitor. Total RMS capacitor current and average value of currents supplied by the battery can be represented by equations (3.1) and (3.2).

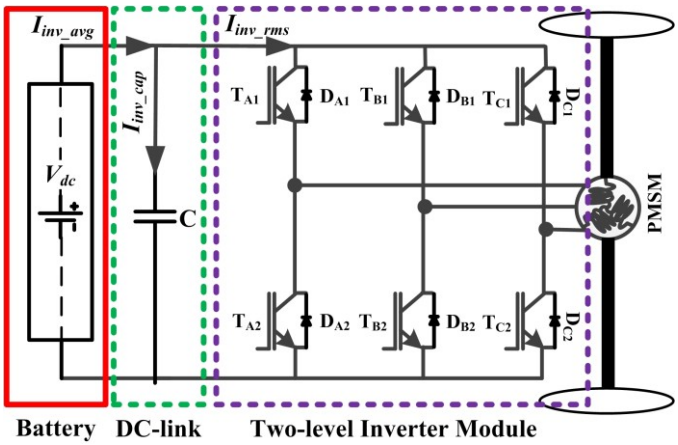


Figure 3.1 Two-level inverter.

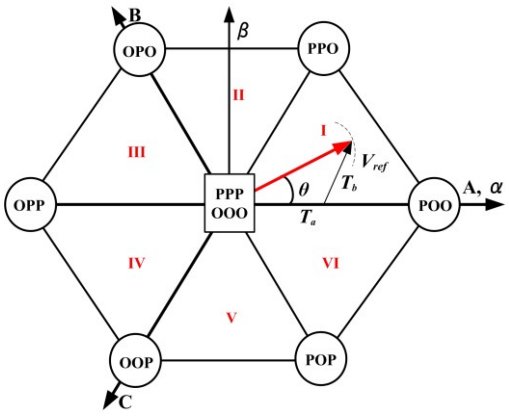


Figure 3.2 Space-vector diagram for two-level inverter.

Fig. 3.2 shows the space-vector diagram for two-level inverter. As shown in the diagram, reference voltage vector V_{ref} in sector one can be constructed by using the three available voltages on that sector. Equation (3.1) shows the representation of the reference voltage vector as a summation of other three voltage vectors.

$$V_{\text{ref}} \cdot T_{\text{S}} = V_1 T_{\text{a}} + V_2 T_{\text{b}} + V_0 T_{\text{z}} \tag{3.1}$$

Where, $T_{\text{s}} = T_{\text{a}} + T_{\text{b}} + T_z$

V_1, V_2 are the two nearest voltage vectors and V_0 is the zero voltage vector.

T_a, T_b and T_z are the respective time duration for those voltage vectors applied, as shown in (3.2).

$$T_a = (m \cdot T_s)\sin\left(\frac{\pi}{3} - \theta\right) \Big/ \sin(\frac{\pi}{3})$$
$$T_b = (m \cdot T_s)\sin(\theta) \Big/ \sin(\frac{\pi}{3}) \quad (3.2)$$
$$T_z = T_s - (T_a + T_b)$$

Where, $\mathrm{m} = \sqrt{3}V_{\mathrm{ref}} / V_{\mathrm{dc}}$ and T_s is the total switching time duration.

3.2. Analytical Calculation of Capacitor current

3.2.1. Two-Level Inverter Capacitor Current

According to the analytical calculations shown for capacitor current in [146], an analytical expression for the capacitor current is derived from the inverter positive bus current. Average value to the inverter current, which is mainly supplied by battery, can be computed by finding out the average value of total inverter current ($I_{inv,avg}$), as shown in (3.3).

$$I_{\mathrm{invavg}} = (\frac{3}{\pi})\int_0^{\frac{\pi}{3}} (I_{\mathrm{poo}} \cdot T_{\mathrm{a}} + I_{\mathrm{ppo}} \cdot T_{\mathrm{b}})\mathrm{d}\theta$$
$$\therefore \; I_{\mathrm{invavg}} = \frac{\sqrt{3}}{2} \cdot \mathrm{m} \cdot I_{\mathrm{m}} \cos(\varphi) \quad (3.3)$$

Where, $I_{poo} = I_{\mathrm{m}}\cos(\theta\text{-}\varphi)$, $I_{ppo} = -I_{\mathrm{m}}\cos(\theta - \varphi\text{-}4\Pi/3)$, are the phase currents associated with the active voltage vectors POO and PPO, I_m is the peak value of per phase load current, $\theta=\omega t$, and φ is the power factor angle. In a similar manner, the total RMS inverter current ($I_{inv,rms}$) can be calculated, as shown in (3.4).

$$I_{\mathrm{invrms}} = I_{\mathrm{m}} \sqrt{(\frac{3}{\pi})\int_0^{\frac{\pi}{3}} (I_{\mathrm{poo}}{}^2 \cdot T_{\mathrm{a}} + I_{\mathrm{ppo}}{}^2 \cdot T_{\mathrm{b}})\mathrm{d}\theta}$$
$$I_{\mathrm{invrms}} = I_{\mathrm{m}} \cdot \sqrt{\frac{\mathrm{m} \cdot (4 \cdot \cos^2(\varphi) + 1)}{2 \cdot \pi}} \quad (3.4)$$

Now, as the total inverter current is composed of the average load current, supplied by battery, and RMS value of ripple current, which is supplied by capacitor, the RMS capacitor current (I_{caprms}) can be calculated as shown in (3.5).

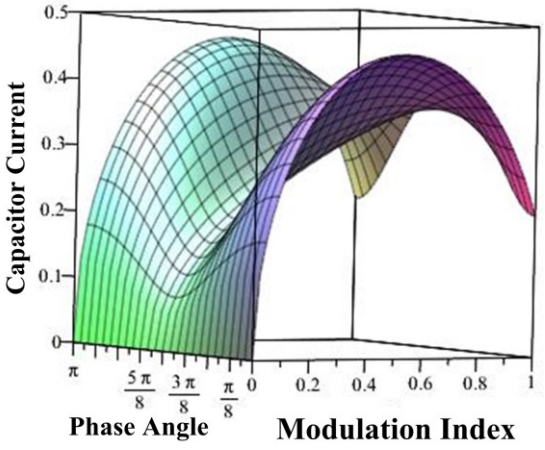


Figure 3.3 DC-link capacitor current ripple (I_{caprms}).

$$I_{\text{caprms}} = \sqrt{I_{invrms}{}^{2} - I_{invavg}{}^{2}}$$

$$I_{\text{caprms}} = \frac{I_{\text{m}}}{2}\sqrt{-3 \cdot m^{2}\cos^{2}(\varphi) + \frac{2 \cdot m(4 \cdot \cos^{2}(\varphi)+1)}{\pi}} \tag{3.5}$$

As is clear from (3.5), RMS value of capacitor current is a function of modulation index, m, and the power factor angle, φ. Fig. 3.3 shows the variation in RMS ripple current, due to the change in m and φ, while keeping the peak load current (I_m) at unity. It can be observed that capacitor current reaches its peak value, when m reaches approximately 0.5.

3.2.2. Three-level Inverter Capacitor Current

Fig. 3.4 shows the vector diagram of sector I, with four sub-sectors. When m is in between 0 and ~ 0.54, the reference vector lays in sub-sector one; and above that value, it will use sub-sector 2, 3, or 4. As seen in subsector I, there exist four small voltage vectors, which are redundant. Either the positive one can be used, which utilizes the upper capacitor, or the negative one could be used, which uses the lower capacitor. In a switching cycle, in order to keep the voltage in the two capacitors balanced both the voltage vectors are used equally, which is valid for other subsectors as well. To calculate the capacitor current, sector I is divided into two regions. Region I includes sub-sector 1 and region II includes sub-sectors 2, 3, and 4. For this analysis, the 1st capacitor current is considered. As in the balanced condition, both the capacitor voltages should be equal; the two capacitor currents will be symmetrical as well.

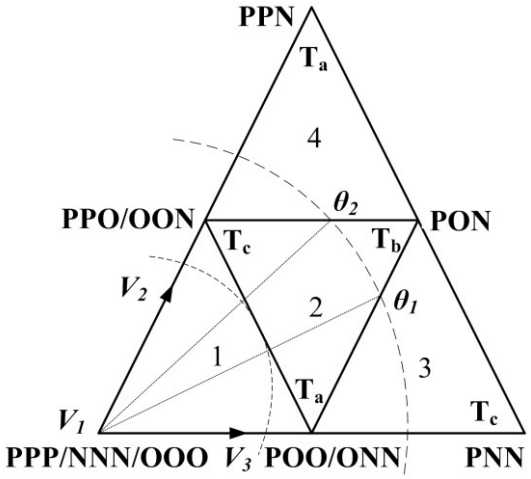


Figure 3.4 Sector-I, with four subsectors for three-level inverter.

Region I

As shown in Fig. 3.4 sub-sector 1, in order to keep the two capacitor voltages balanced, POO/OON and PPO/OON vectors have to be used equally. As ONN and OON vectors are using only the lower capacitor, to calculate the upper capacitor RMS current, only the POO and PPO vectors are considered. The average and RMS inverter current calculation is shown in (3.6) and (3.7), with the same procedure followed, as that for the two-level inverter. The time period for which redundant voltage vectors (POO/ PPO) will be applied can be calculated by their corresponding time period shown in Table III, chapter I and multiply them with 0.5, to equally distribute the time period between the upper and lower capacitors. For null, medium and large voltage vectors, full time period will be considered, because only one voltage vector is available.

$$I_{\text{invavg}} = (\frac{3}{\pi}) \int_0^{\frac{\pi}{3}} \left((I_{\text{poo}} \cdot T_{\text{a}} \cdot 0.5) + (I_{\text{ppo}} \cdot T_{\text{c}} \cdot 0.5) + (0 \cdot T_{\text{b}})\right) \text{d}\alpha$$

$$\therefore I_{\text{invavg}} = \frac{2.7206 \cdot I_{\text{m}} \cdot m \cdot \cos(\varphi)}{\pi} \tag{3.6}$$

$$I_{\text{invrms}} = \sqrt{(\frac{3}{\pi}) \int_0^{\frac{\pi}{3}} \left((I_{\text{poo}}{}^2 \cdot T_{\text{a}} \cdot 0.5) + (I_{\text{ppo}}{}^2 \cdot T_{\text{c}} \cdot 0.5) + (0 \cdot T_{\text{b}})\right) \text{d}\alpha}$$

$$\therefore I_{\text{invrms}} = I_{\text{m}} \sqrt{0.31830 \cdot m \cdot (2 \cdot \cos^2(\varphi) + 0.5)} \tag{3.7}$$

From (3.6) and (3.7), RMS capacitor current can be calculated as:

$$I_{\text{caprms}} = I_{\text{m}} \left(\sqrt{-m \cdot (0.7499 \cdot m \cdot \cos^2(\varphi) - 0.6366 \cdot \cos^2(\varphi) - 0.1591)}\right) \tag{3.8}$$

All the parameters are already explained during two-level inverter current calculation.

Region II

When the reference vector is in region-II, the trajectory will cross the three sub-sectors 2, 3, and 4. Let's assume the reference voltage vector will cross the subsectors at θ_1 and θ_2; hence, the calculation for total average and RMS current of the inverter positive DC-bus can be shown in (3.9) and (3.10). The total RMS ripple current supplied by capacitor is shown in (3.11). Fig. 3.5 shows the variation in capacitor currents during change in modulation index (m). It can be observed that the peak capacitor current is same as two-level capacitor current value. Hence, during the design of capacitor current rating for the three-level inverter, the RMS current rating will be considered the same as that of the two-level inverter. However, the voltage will be half of the two-level inverter corresponding DC-link voltage.

$$I_{\text{invavg}} = (\frac{3}{\pi})\begin{pmatrix} \int_0^{\theta_1}(I_{\text{poo}}\cdot T_{\text{a}}\cdot 0.5 + I_{\text{pnn}}\cdot T_{\text{c}} + I_{\text{pon}}\cdot T_{\text{b}})\,\text{d}\alpha + \int_{\theta_1}^{\theta_2}(I_{\text{poo}}\cdot T_{\text{a}}\cdot 0.5 + I_{\text{pon}}\cdot T_{\text{b}} + I_{\text{ppo}}\cdot T_{\text{c}}\cdot 0.5)\,\text{d}\alpha \\ + \int_{\theta_2}^{\frac{\pi}{3}}(I_{\text{ppo}}\cdot T_{\text{c}}\cdot 0.5 + I_{\text{pon}}\cdot T_{\text{b}} + I_{\text{ppn}}\cdot T_{\text{a}})\,\text{d}\alpha \end{pmatrix}$$

$$\therefore I_{\text{invavg}} = \frac{I_{\text{m}}}{\text{m}}\begin{pmatrix} m^2\cdot(0.866\cdot\cos(\varphi) + \arcsin(\frac{0.5}{m})\cdot(0.477\cdot\sin(\varphi) - 6.36e^{-10}\cos(\varphi))) \\ + m\cdot 0.119\cdot\sin(\varphi)\cdot\sqrt{4\cdot m^2 - 1} - 0.2067\cdot\sin(\varphi) \end{pmatrix} \quad (3.9)$$

$$I_{\text{invrms}} = \sqrt{(\frac{3}{\pi})\begin{pmatrix} \int_0^{\theta_1}(I^2_{\text{poo}}\cdot T_{\text{a}}\cdot 0.5 + I^2_{\text{pnn}}\cdot T_{\text{c}} + I^2_{\text{pon}}\cdot T_{\text{b}})\,\text{d}\alpha + \int_{\theta_1}^{\theta_2}(I^2_{\text{poo}}\cdot T_{\text{a}}\cdot 0.5 + I^2_{\text{pon}}\cdot T_{\text{b}} + I^2_{\text{ppo}}\cdot T_{\text{c}}\cdot 0.5)\,\text{d}\alpha \\ + \int_{\theta_2}^{\frac{\pi}{3}}(I^2_{\text{ppo}}\cdot T_{\text{c}}\cdot 0.5 + I^2_{\text{pon}}\cdot T_{\text{b}} + I^2_{\text{ppn}}\cdot T_{\text{a}})\,\text{d}\alpha \end{pmatrix}} \quad (3.10)$$

$$\therefore I_{\text{invrms}} = \frac{I_{\text{m}}}{m}\cdot\sqrt{\begin{pmatrix} m^3(0.159 - 0.275\cdot\sin(2\cdot\varphi) + 0.636\cdot\cos^2(\varphi)) + m^2(\sqrt{4\cdot m^2 - 1}\cdot(-3.18\cdot e^{-11}\cdot\cos^2(\varphi) \\ + 0.318\cdot\sin(2\cdot\varphi) + 0.358\cdot\sin(2\cdot\varphi))) + \sqrt{4\cdot m^2 - 1}\cdot(-3.18\cdot e^{-11}\cdot\cos^2(\varphi) - 3.18\cdot e^{-12} \\ - 0.034\cdot\sin(2\cdot\varphi)) - 0.059\cdot\sin(2\cdot\varphi) \end{pmatrix}}$$

From (3.9) and (3.10), RMS capacitor current can be calculated as:

$$I_{\text{caprms}} = \frac{I_m}{m}\cdot\sqrt{\begin{pmatrix} m^4\cdot(\arcsin(\frac{0.5}{\text{m}})^2\cdot(-0.227 + 0.227\cdot\cos^2(\varphi) + 3.039\cdot\text{e}^{-10}\cdot\sin(2\cdot\varphi)) + \arcsin(\frac{0.5}{\text{m}})\cdot(-0.416\cdot\sin(2\cdot\varphi) \\ + 1.102\cdot\text{e}^{-9}\cdot\cos^2(\varphi)) - 0.75\cdot\cos^2(\varphi)) + m^3\cdot(0.159 - 0.275\cdot\sin(2\cdot\varphi) + 0.636\cdot\cos^2(\varphi)) \\ + m^2\cdot(\sqrt{4\cdot m^2 - 1}\cdot(-3.18\cdot e^{-11}\cdot\cos^2(\varphi) + 0.113\cdot\cos^2(\varphi)\cdot\arcsin(\frac{0.5}{\text{m}}) - 0.113\cdot\arcsin(\frac{0.5}{\text{m}}) \\ + 0.759\cdot\text{e}^{-10}\cdot\sin(2\cdot\varphi)\cdot\arcsin(\frac{0.5}{\text{m}}) + 0.034\cdot\sin(2\cdot\varphi)) + \arcsin(\frac{0.5}{\text{m}})\cdot(-1.316\cdot\text{e}^{-10}\cdot\sin(2\cdot\varphi) \\ - 0.197\cdot\cos^2(\varphi) + 0.197) + 0.056\cdot\cos^2(\varphi) - 0.056 + 0.537\cdot\sin(2\cdot\varphi))) + \sqrt{4\cdot m^2 - 1}\cdot(-0.04\cdot\cos^2(\varphi) \\ + 0.049 - 0.034\cdot\sin(2\cdot\varphi)) + 0.028\cdot\cos^2(\varphi) - 0.059\cdot\sin(2\cdot\varphi) - 0.028 \end{pmatrix}} \quad (3.11)$$

Here, $\theta_1 = \frac{\pi}{3} - \sin^{-1}(\frac{1}{2\cdot m})$, $\theta_2 = \frac{\pi}{3} - (\frac{\pi}{3} - \sin^{-1}(\frac{1}{2\cdot m}))$, $I_{\text{pon}} = I_{\text{m}}\cos(\alpha - \varphi)$, $I_{\text{pnn}} = I_{\text{m}}\cos(\alpha - \varphi)$ and $I_{\text{ppn}} = -I_{\text{m}}\cos(\alpha - \varphi - \frac{4\pi}{3})$.

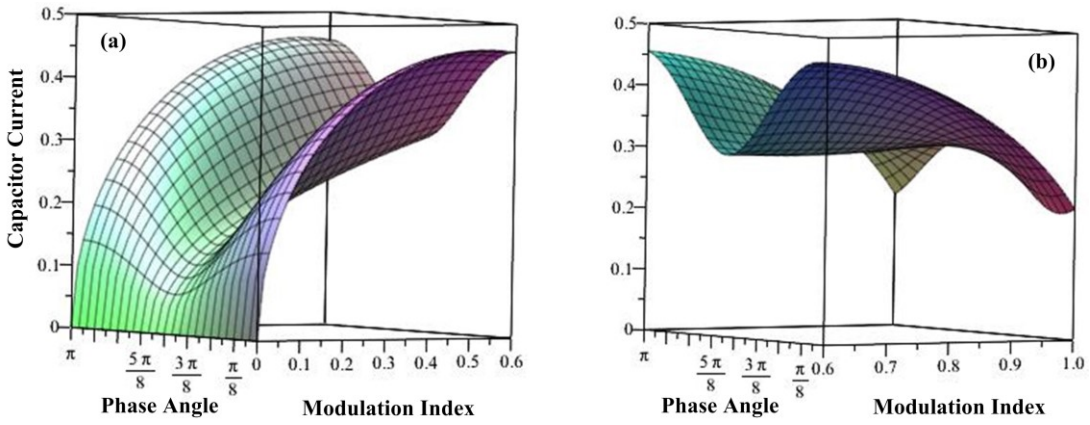


Figure 3.5 RMS capacitor current in three-level inverter, for (a) m = 0 to 0.6 and (b) 0.6 to 1.0.

When *m* lays between regions I and II, it uses vectors from both sub-sector 1 and 2. For the sake of simplicity of calculation, the third region is not considered for RMS capacitor current calculation. This is clearly depicted in regions I and II. For this reason, a discontinuity is observed at around *m* = 0.6. Moreover, film capacitors are used for DC-link capacitors, which have very low ESR. So, effects of ESR are also not considered for this study.

3.3. SIMULATION RESULTS

Figs. 3.6 and 3.7 shows the total harmonic distortion (%THD) for phase voltages applied to machine and the variation in capacitor RMS current for change in modulation index. It can be observed that in case of three-level inverter the harmonic distortion is almost 50% lesser than the two level inverter for same modulation index. This significant reduction in harmonic distortion will be going to reduce the passive component sizes, like the load side filter inductor, EMI filter which are used in source side and also the machine losses. Capacitor current is also shown for both two- and three-level inverters. It can be observed that the capacitor current peak occurs at near 0.5 modulation index, which are correlated with the analytical expression. It can also be observed that the neutral current shown for three-level inverter is almost double to the capacitor current. The reason behind is that, when the modulation index is lower than 0.5, the control strategy try to use the two capacitor equally, so either for upper or lower capacitor current is going to come back through the neutral point or it is going to source from neutral point. Again when the modulation index is higher than 0.5 the medium vector is going to use the neutral point. So the total current occurs in the neutral wire is almost double than each capacitor current.

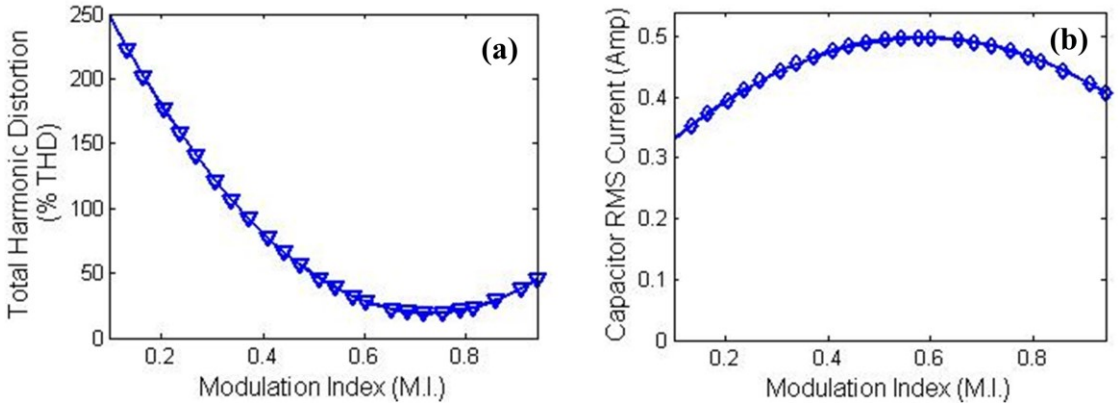


Figure 3.6 (a) Phase voltage total harmonic distortion (%THD) and (b) RMS capacitor current for two-level inverter.

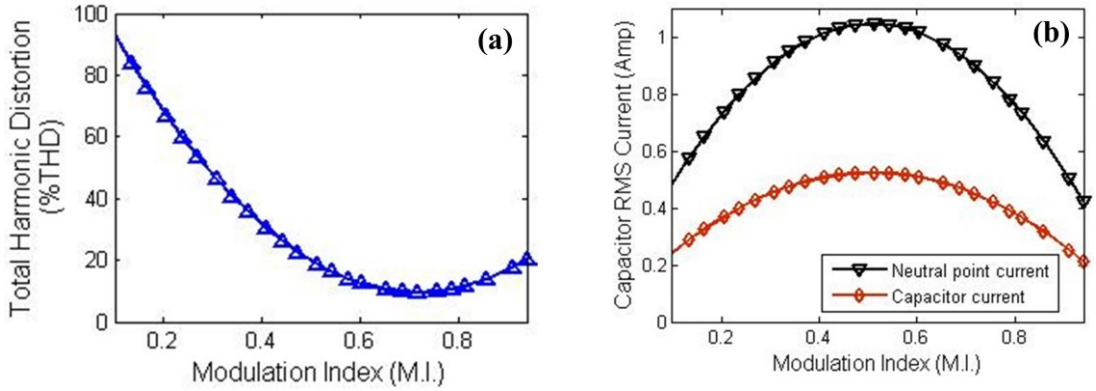
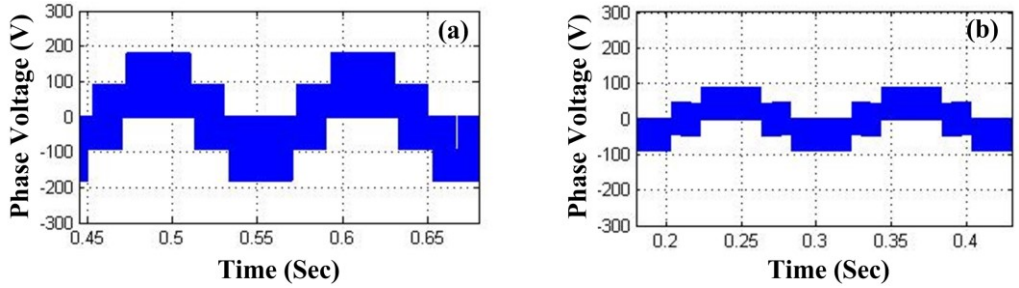
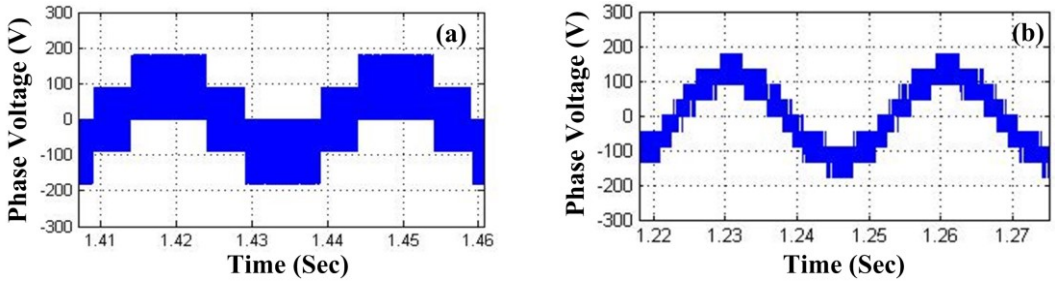


Figure 3.7 (a) Phase voltage total harmonic distortion (%THD) and (b) RMS capacitor current for three-level inverter.



M.I = 0.19



M.I = 0.814

Figure 3.8 Inverter phase voltages at low and high modulation indexes for (a) Two- and (b) three-level.

Fig. 3.8 shows the phase voltages for both the inverters with low (M.I = 0.19) and higher (M.I = 0.814) modulation indices. From the wave form we can observe that, at low

modulation index to produce the same reference voltage three-level inverter uses the low voltage step compared to the two level inverter and for high modulation index three-level use more number of steps, which makes it closer to sinusoid.

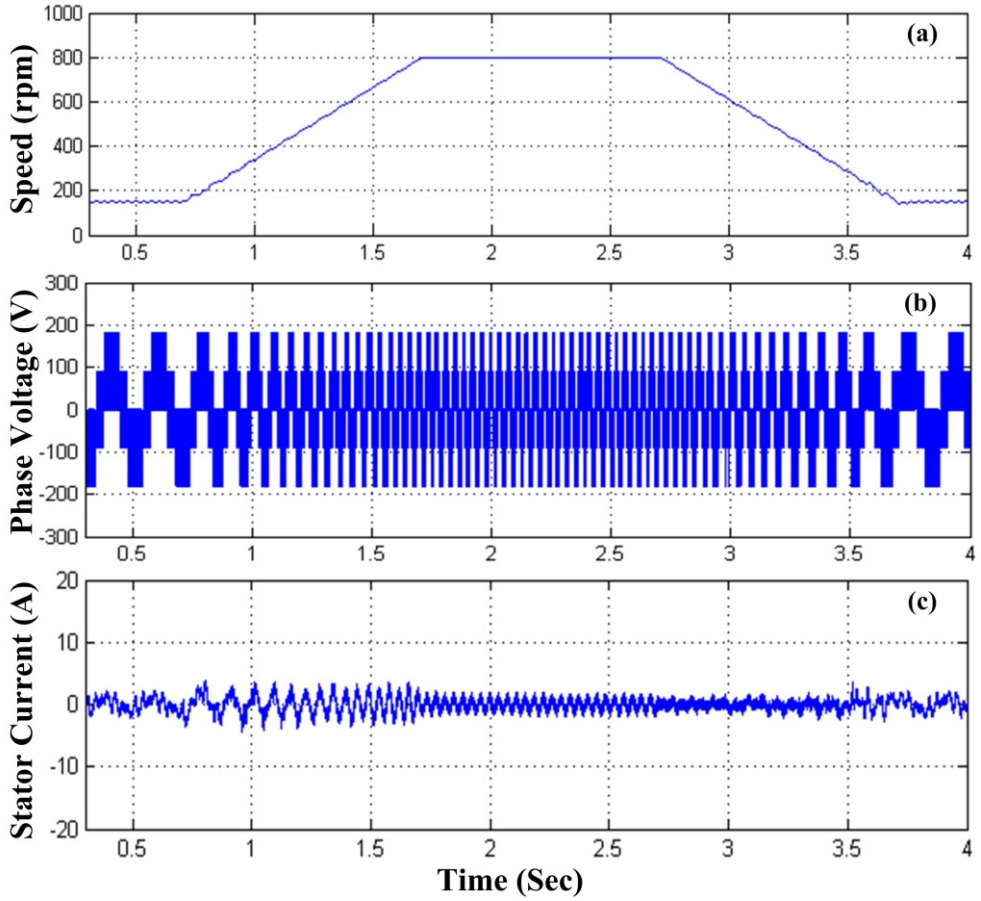


Figure 3.9 Simulation results for two-level inverter with change in speed from 150.0 rpm to 800.0 rpm at 4.0 N.m. load torque; (a) Motor speed; (b) Phase voltage; (c) Stator Current.

Fig. 3.9 shows the performance of the two-level inverter with change in speed form 150.0 rpm to 800.0 rpm at 4.0 N.m. load torque. It can be observed that with increase in modulation index for three-level inverter, phase voltage steps increases, which brings the phase voltage more toward sinusoidal wave shape compared to the two-level inverter. Also due to the increased number of voltage steps, dv/dt stress across the load terminals also gets reduced.

Fig. 3.10 shows the performance of the 2-level inverter due to change in load torque from 4.0 to 24.0 N.m., while speed was kept constant at 500.0 rpm. From the waveform it can be observed that although wave shapes are similar because of low modulation index, three-level inverter voltage magnitudes are lower than the two-level inverter.

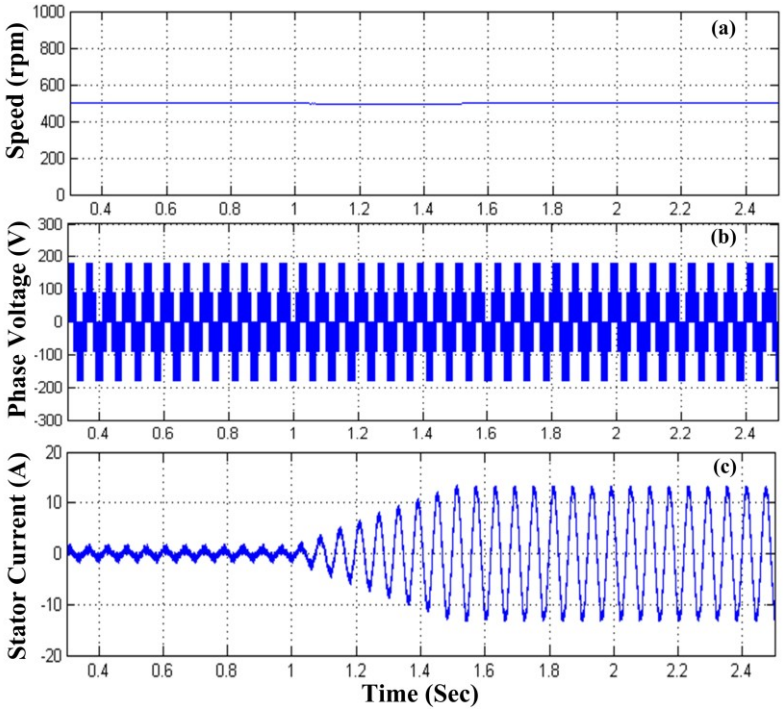


Figure 3.10 Simulation results for two-level inverter with change in load torque from 4.0 to 24.0 N.m at 500.0 rpm machine speed; (a) Motor speed; (b) Phase voltage; (c) Stator Current.

Fig. 3.11 shows the variation in the total inverter loss for two-level and three-level inverter with proposed DC-bus voltage balancing scheme for a 54.0 kW SPMSM. During the simulation study machine speed was kept constant at 5000.0 rpm and load torque was at 70.0 N.m. IGBT and diode conduction and switch losses are calculated using PLECS based simulation tool. All the control logics are developed in MATLAB/ Simulink platform. For comparison of both the inverters switch losses, device characteristics are taken from Infineon FF300R12ME4, 1200.0 V switches for two-level inverter and F3L300RO7PE4, 650.0 V switches for three-level inverter. DC-bus voltage was kept at 600.0 V. The DC-link capacitance values were at 500.0 μF for each capacitor. It can be observed that, with the proposed low switching loss based strategy, total inverter loss has reduced down to 60% of the two-level scheme and around 54% lower than the higher switching loss based space vector modulation technique.

Fig. 3.12 shows the average torque ripple comparison for both two- and three-level topology. Two-level system has the higher torque ripple and the proposed low switching loss based topology has the lowest torque ripple below 20.0 kHz. After that they are almost similar. Fig. 3.13 shows the average neutral point potential variation (NPP), as shown in (3.12) with change in modulation index. It can be observed that, high switching loss based topology has almost half voltage deviation compared to the low switching loss based

topology. It is because of the change in duty takes place in between the switching cycles depending on capacitor voltage difference.

$$V_{capdiff} = V_{capupper} - V_{caplower} / V_{DC} \tag{3.12}$$

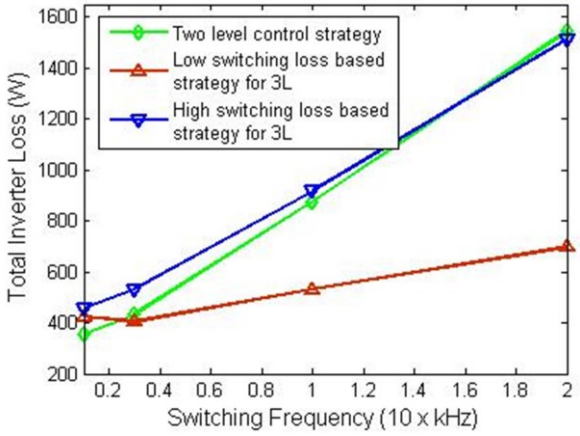


Figure 3.11 Total loss comparison between two- and three-level inverter with different switching frequencies.

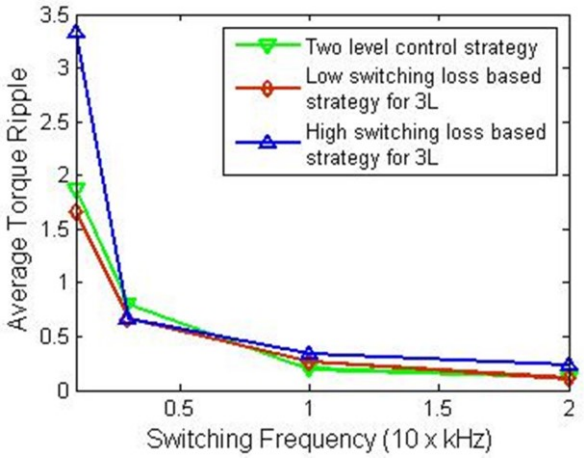


Figure 3.12 Load torque ripple comparison between two- and three-level inverter with different switching frequencies.

Fig. 3.14 shows the loss distribution in IGBTs and diode modules while modulation index is kept constant at 0.713. It can be observed that for two-level inverter the loss distribution is symmetrical for upper and lower half of inverter leg. However, for three-level inverter distribution is not exactly equal. This is because of the frequent change in switching sequence to keep the two DC-link capacitor voltages equal and longer conduction time of the inner IGBT switches compared to the outer ones. It will be discussed in more details in chapter V. Also the antiparallel diode losses are almost negligible at higher modulation index. This is because of the larger power sharing by the NPC diodes, which passes the load current when the main power switches turned off (Like T_{A1}, T_{A4}). Moreover, it can also be observed that in

case of three-level inverter conduction losses are dominant and for two-level, switching losses are dominant.

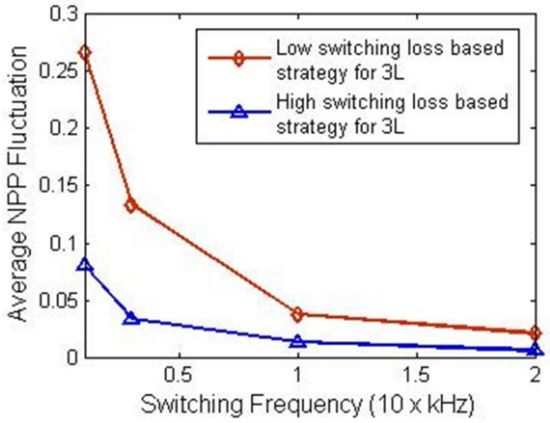


Figure 3.13 Variation in two capacitor voltages with change in switching frequency for 3- level inverter.

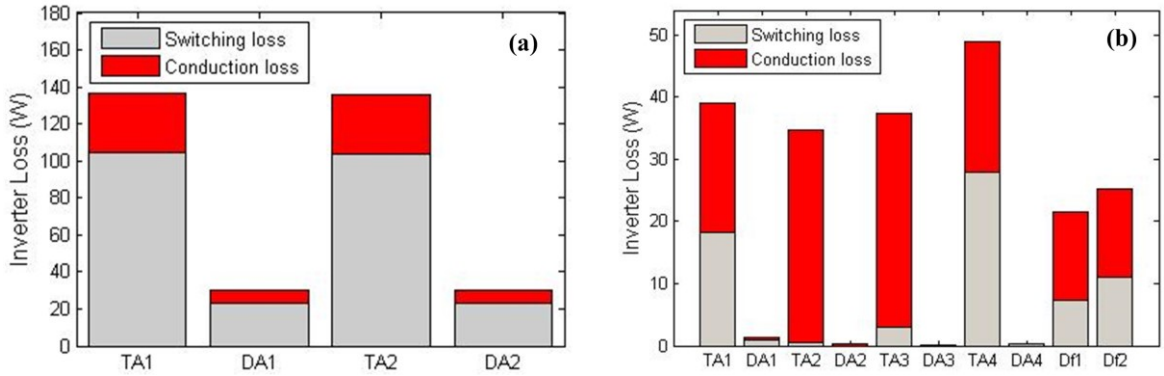


Figure 3.14 Conduction and switching losses of (a) Two-level and (b) Three-level inverter at modulation index of 0.713.

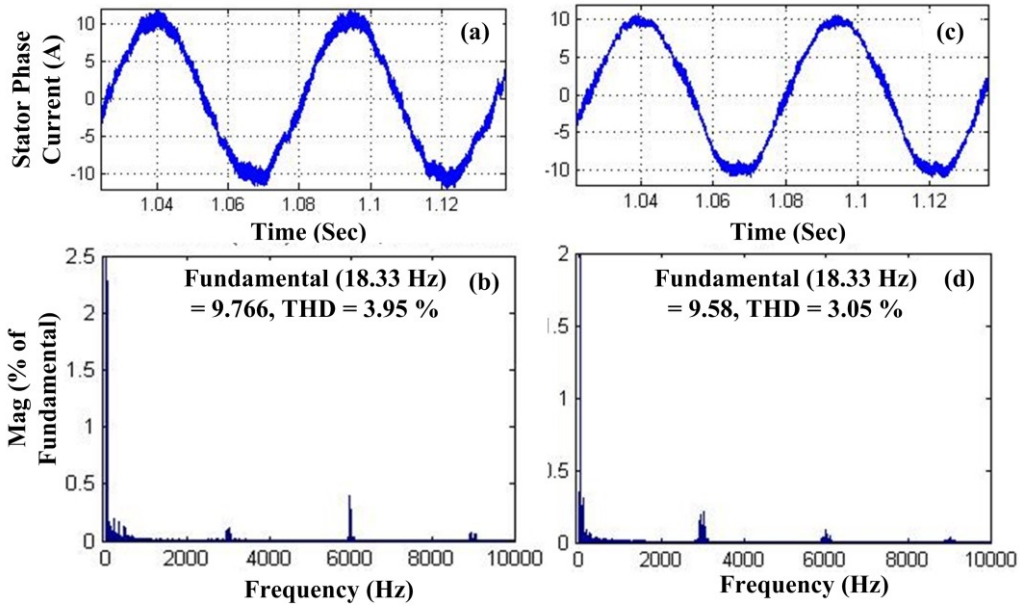


Figure 3.15 Current harmonic distortion comparison between (a, b) two- and (c, d) three-level inverter.

Fig. 3.15 shows the current harmonic comparison of both the two- and three-level inverter. As was expected the three-level inverter corresponding current harmonics are lower.

3.4. Experimental Results

Figs. 3.16, 3.17 show the experimental results for the total harmonic distortion and capacitor current for both the inverters. It can be observed that total harmonic distortion for three-level is less than 50% as compared to the two-level inverter. The capacitor current has also its peak near to 0.5 modulation index as shown in the simulation and analytical studies. From eq. (3.11), it can observe that the capacitor current wave shape depends on the modulation index, peak load current and power factor. So if the load current is kept constant then capacitor current peak is going to occur at 0.5 modulation index. However in case of machine, no load losses like friction and windage losses keep on increasing with speed. So the current supplied by inverter in going to increase with higher modulation index, which in turn shift the peak of the capacitor current more than 0.5. This phenomenon we can observe from the wave shapes collected from the experimental data.

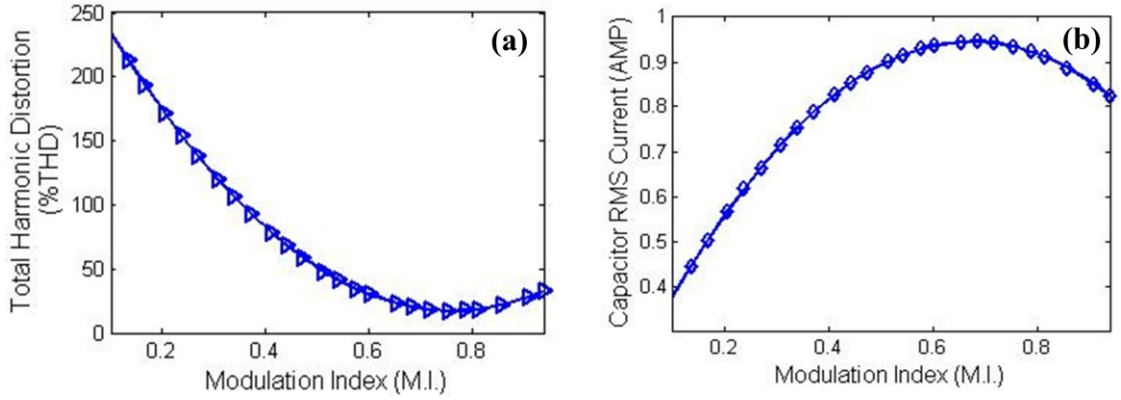


Figure 3.16 Phase voltage total harmonic distortion (%THD) and RMS capacitor current for two-level inverter.

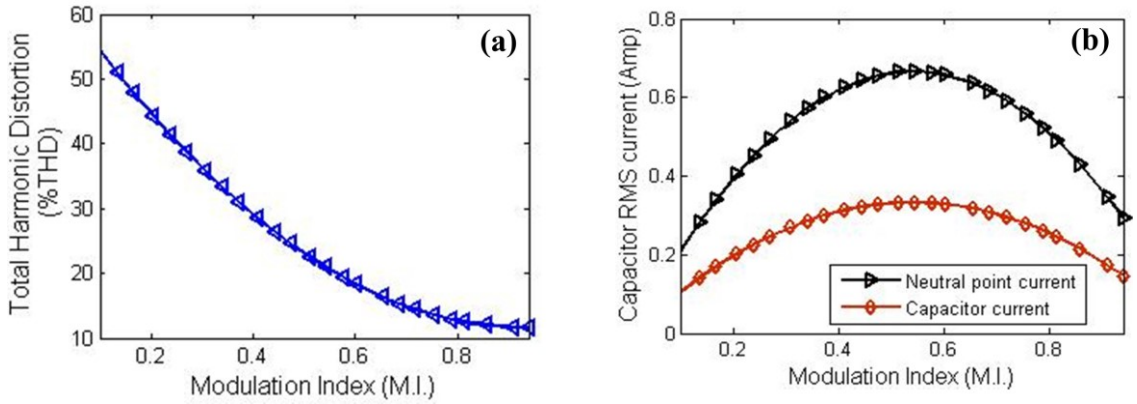
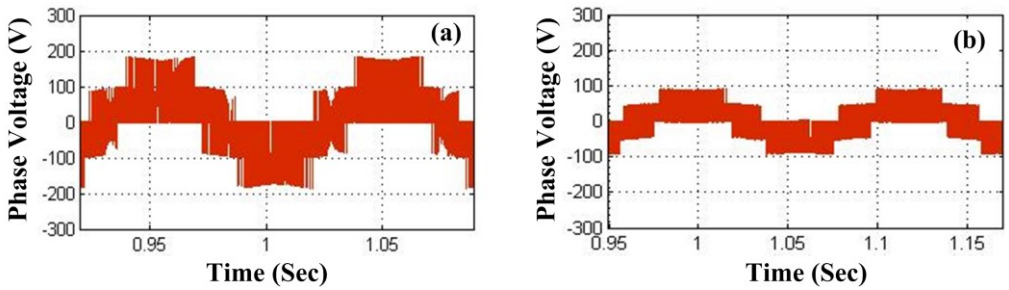
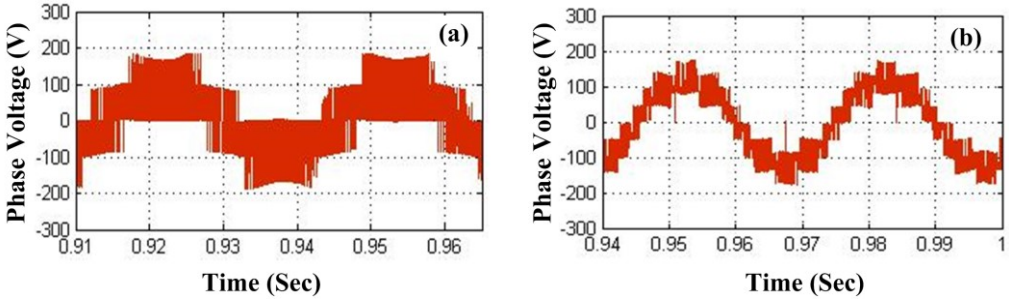


Figure 3.17 (a) Per-phase voltage total harmonic distortion (%THD) and (b) RMS capacitor current for three-level inverter.



M.I = 0.19



M.I = 0.814

Figure 3.18 (a) Two- and (b) three-level inverter phase voltage with low and high modulation index.

Fig. 3.18 shows the experimental wave shapes for the both inverter output voltages for low and high modulation indexes. Wave shapes are correlated with the simulation results shown in Fig. 3.8. At higher modulation indices the three-level inverter has more numbers of steps compared to the two-level inverter, which helps to reduce the total harmonic distortion and voltage transients across the switching devises.

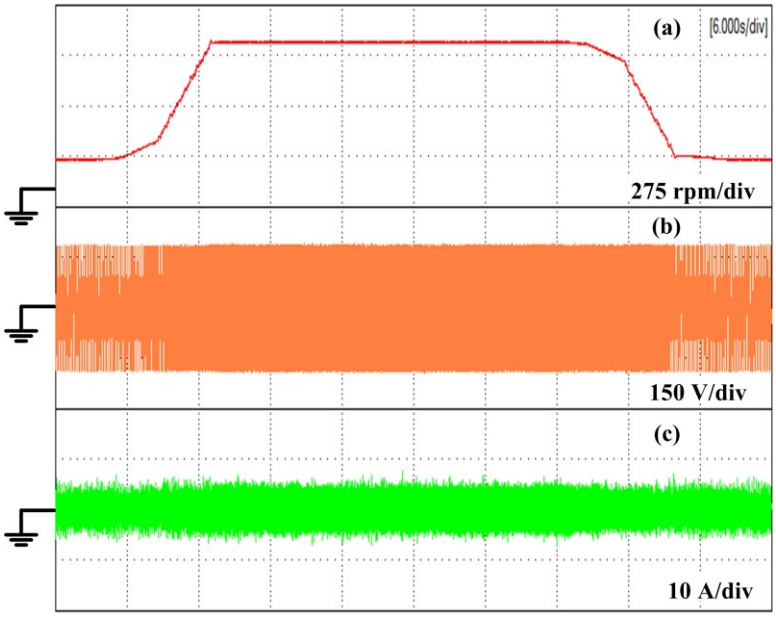


Figure 3.19 Experimental results for two-level inverter with change in speed from 150.0 rpm to 800.0 rpm at 6.0 N.m. load torque; (a) Motor speed; (b) Phase voltage; (c) Stator Current.

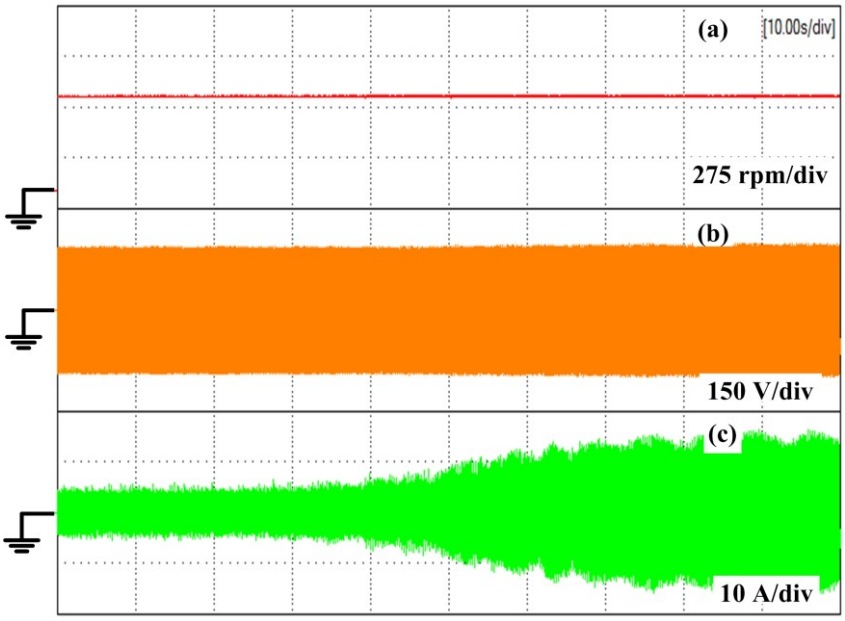


Figure 3.20 Experimental results for two-level inverter with change in load torque from 6.0 N.m. to 24.0 N.m., with 500.0 rpm machine speed; (a) Motor speed; (b) Phase voltage; (c) Stator Current.

Fig. 3.19 shows the performance of the machine with change is speed from 150.0 rpm to 800.0 rpm with 6.0 N.m. load torque. It can be observe that machine speed has followed the reference command. While in case of three-level inverter, we can observe a change in number of voltage steps, in case of two-level inverter, it is not there.

Fig. 3.20 shows the performance of the machine with change in load torque from 6.0 N.m. to 24.0 N.m. Experimental results show good transient and steady state performance of the system for both the inverters.

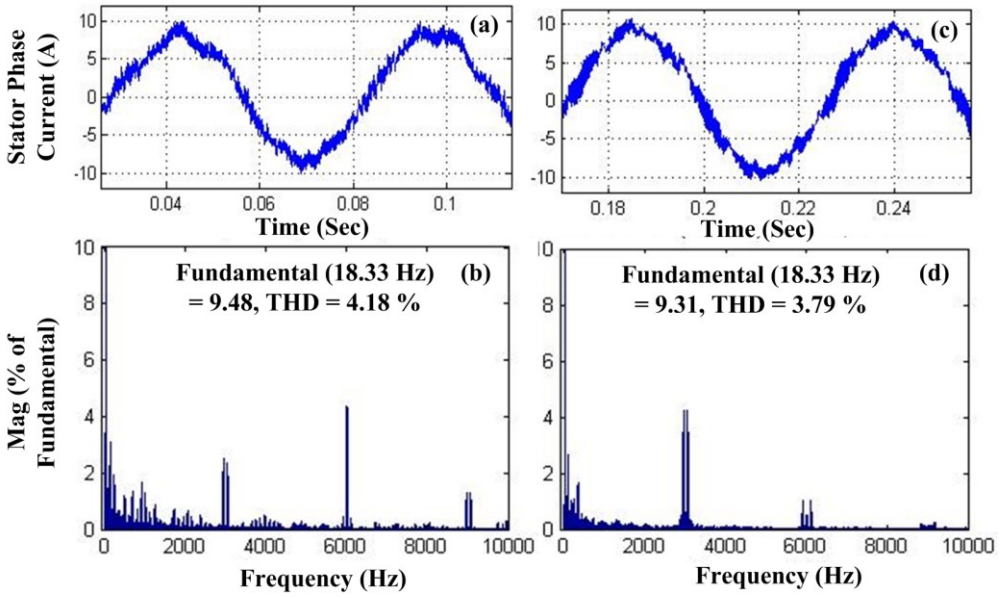


Figure 3.21 Experimental results for current harmonic distortion comparison between (a, b) two- and (c, d) Three-level inverter.

Fig. 3.21 shows the current harmonic distortion comparison for both two- and three-level inverter. Results show two-level inverter has comparatively higher harmonic distortion than three-level, as already shown in simulation studies. Moreover, FFT analysis shows a higher amount of lower order harmonic distortion with the two-level inverter.

3.5. Performance Comparison between Simulation and Experimental Results

The simulation and experimental results for a 2-level inverter are found to be nearly similar. However, change of speed and torque in experimental results are not as smooth as observed in the simulations. The reason is obvious – during the experimental tests, speed and load changes are performed manually, which adds an additional delay in the results.

3.6. Summary of Chapter 3

This chapter presents a detailed comparison study of two- and three-level inverter with PMSM drive. Analytical calculations of both two- and three-level inverter RMS capacitor currents are also derived. Simulation and experimental results show significant improvement in the total voltage harmonic distortion, which intern helps to reduce EMI and output filer size of inverter for three-level inverter. It also helps to reduce voltage stress across power switches. Furthermore, a considerable amount of reduction in the total inverter losses at high switching frequencies and low torque ripple can also be achieved by three-level inverter.

Chapter 4. Carrier Based PWM Techniques for Three-Level Traction Inverter Drive with Surface PMSM

Compared to the SVPWM based strategies carrier based PWM (CB-PWM) strategy is the simplest one to implement. It directly generates the duty cycles for the switches from the reference voltage vector, instead of the sector identification and reduces the extensive numeric calculations of the switching periods, as in the case for SV-PWM based strategies. Moreover, this reduces the total computation time of the controller, which in turn allows the system switching frequency to increase.

The different available carrier based strategies can be summarized as follows.

4.1. Carrier Based PWM (CB-PWM) Technique

4.1.1. Sinusoidal PWM with 3rd Harmonic Injection

In this scheme, a common 3rd harmonic voltage is added to the three reference phase voltages generated from the control loop [70], as shown in Fig. 4.1 (a). The addition of a 3rd harmonic voltage helps the modulation index to increase to 1.15, compared to the typical SPWM based scheme. Hence, there exists an additional 15% increase in modulation index.

$$v_{a\_ref} = v_a - v_z;\ v_{b\_ref} = v_b - v_z;\ v_{c\_ref} = v_c - v_z$$
$$\text{Where, } v_z = (\max(v_a, v_b, v_c) + \min(v_a, v_b, v_c))/2 \tag{4.1}$$

Equation (4.1) shows the three reference voltage vectors (v_{abc_ref}) generated from the three phase voltages (v_{abc}) and the zero-sequence voltage (v_z). Zero-sequence voltage is generated from the minimum and maximum value of the phase voltages.

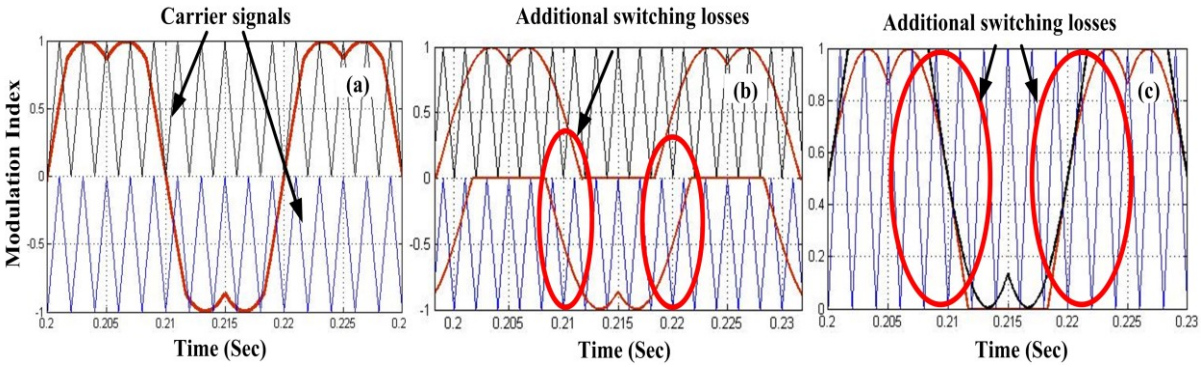


Figure 4.1 Modulation and carrier signal for (a) Min-max control; (b) Double signal PWM (DSPWM); (c) DS-PWM with single-carrier.

4.1.2. Double Signal PWM (DS-PWM)

DS-PWM is also referred to as "fast-processing" modulation [82]. This scheme adopts two-modulation signals; one positive and one negative, as shown in Fig. 4.1 (b). Eq. (4.2)

shows the two duty cycles that are generated for the upper two switches of each inverter phase.

$$v_{ip} = \frac{v_i - \min(v_a, v_b, v_c)}{2}; v_{in} = \frac{v_i - \max(v_a, v_b, v_c)}{2} \tag{4.2}$$

In order to calculate v_{ip} and v_{in} signals, a condition on the neutral point current (i_{np}), has to be imposed. Instantaneous neutral point current can in fact be expressed as follows:

$$i_{np}(t) = s_{ao}(t) \cdot i_a(t) + s_{bo}(t) \cdot i_b(t) + s_{co}(t) \cdot i_c(t) \tag{4.3}$$

In order to preserve the DC bus voltage balanced, the locally averaged neutral point current within a modulation period must be zero. Thus:

$$i_{np}(t) = d_{ao} \cdot i_a + d_{bo} \cdot i_b + d_{co} \cdot i_c \tag{4.4}$$

Here, $d_{io}=S_{io}$ is the duty cycle of the zero voltage conditions for each NPC phase. $S_{a,b,co}$ are the three phase pole voltages.

DS-PWM is equivalent to the previously presented third harmonic injection PWM as far as the maximum voltage range for linear operation mode is considered. It also helps to eliminate low-frequency harmonic oscillations from the neutral point, which helps to reduce the DC-link capacitor size. However, it increases the number of commutation cycles of the inverter, compared to the typical SPWM scheme. Around 33% more commutation occurs in case of DS-PWM, compared to the third harmonic injected PWM. This increased commutation increases the inverter switching losses significantly.

4.1.3. Single-Carrier Based DS-PWM Control Strategy

To overcome the computational problem with the two carriers [147] based strategy, a novel, modified control strategy is proposed here. The proposed scheme is practically an extension of the DS-PWM scheme. As is clear from (4.5), the negative modulating signal of v_{in} is just shifted up by adding it with unity. Hence, this scheme gets rid of the additional carrier signal.

$$v_{ip} = \frac{v_i - \min(v_a, v_b, v_c)}{2}; v_{in} = \frac{v_i - \max(v_a, v_b, v_c)}{2} + 1 \tag{4.5}$$

Here, $v_{i\_p,n}$ are the duty cycles for the upper two IGBT switches.

However, this scheme has a common modulation signal between the positive and negative part, as shown in Fig. 4.1 (c). This introduces additional switching losses.

4.2. PROPOSED SINGLE-CARRIER BASED THPWM WITH DC-LINK VOLTAGE BALANCING

The proposed control circuit for 3rd harmonic PWM based DC-link capacitor voltage balancing for a 3-level inverter driven PMSM is shown in Fig. 4.2. The 3-phase currents and machine speed are taken into the vector controller block, which generates the three modulating signal (v_{abc_ref}). The difference between the two capacitor voltages (v_{dc1}, v_{dc2}) is then passed through a PI-controller, to generate the DC-offset voltage (v_o) for the control circuit.

$$\begin{aligned} \delta_{a\_ref} &= (v_{a\_ref}/(0.5\cdot v_{dc})) - v_o \\ \delta_{b\_ref} &= (v_{b\_ref}/(0.5\cdot v_{dc})) - v_o \\ \delta_{c\_ref} &= (v_{c\_ref}/(0.5\cdot v_{dc})) - v_o \end{aligned} \tag{4.6}$$

$$\begin{aligned} \delta_{ap} &= \delta_{a\_ref}, && \text{When, } \delta_{a\_ref} > 0 \\ &= 0, && \text{When, } \delta_{a\_ref} <= 0 \\ \delta_{an} &= \delta_{a\_ref} + 1, && \text{When, } \delta_{a\_ref} < 0 \\ &= 1, && \text{When, } \delta_{a\_ref} >= 0 \end{aligned} \tag{4.7}$$

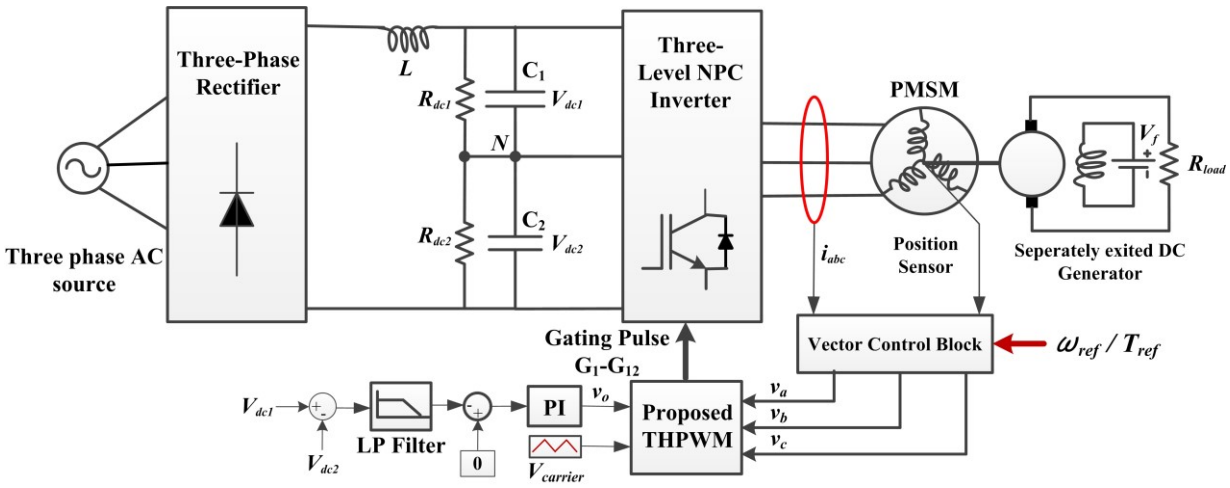


Figure 4.2 Block diagram of proposed single-carrier based PWM control strategy.

A three phase modulating signal is then produced (δ_{abc_ref}) as shown in eq. 4.6, from the reference phase voltages and dc offset voltage generated from the PI controller. However, the generated phase voltages have both positive and negative polarity. To make the modulation signals unipolar, so to make use of one carrier signal, the negative signal is then shifted to the positive half, as shown in eq. 4.7. A limiter is used at the output of v_o, to restrict the dc-offset to go beyond one.

4.2.1. SIMULATION RESULTS

Detailed simulation studies were carried out on a 6.0 kW surface PMSM. The DC-link voltage was kept constant at 270.0 V and the machine is loaded with a DC-dynamometer. The switching frequency is kept constant at 3.0 kHz. Fig. 4.3 shows the duty ratios with the both control strategies at a modulation index of 0.3. It can be observed that, Fig. 4.3 (a, b) which corresponds to the space vector based control strategy shows a higher order of switching compared to the carrier based strategy (c, d). The reason behind it is that, space vector based strategy obtains its duty ratios based on the two separate positive and negative switching sequences, which flips at the carrier frequency depending on the capacitor voltage difference. However, in the case of the carrier based switching sequence, it adds or subtracts a zero sequence voltage from the reference modulation index. Hence, the carrier based control strategy works with a smoother duty cycle compared to the SV-PWM based strategy.

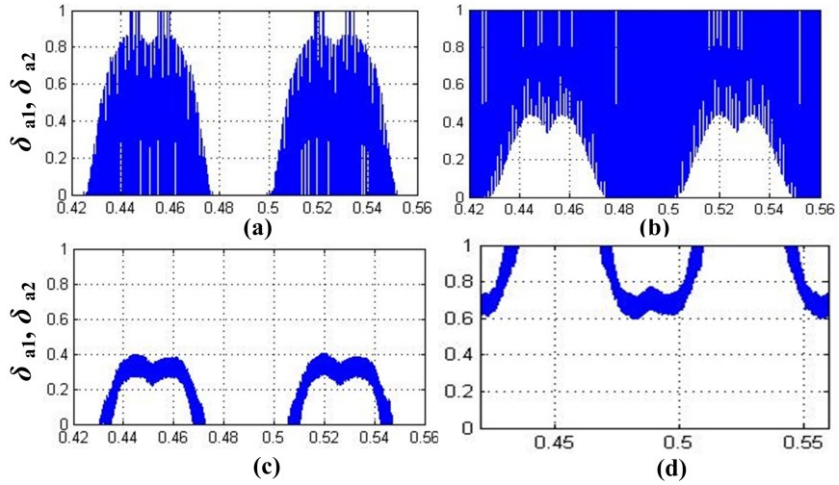


Figure 4.3 Duty ratios for each leg top two switches for the, (a, b) SV-PWM and (c, d) Carrier-based PWM control strategy.

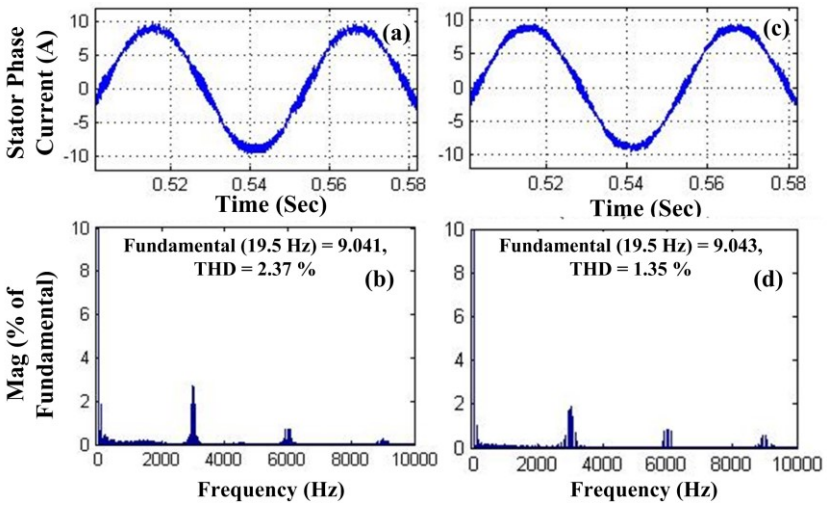


Figure 4.4 Phase current and total harmonic distortion analysis for (a, b) SV-PWM and (c, d) carrier based control strategy.

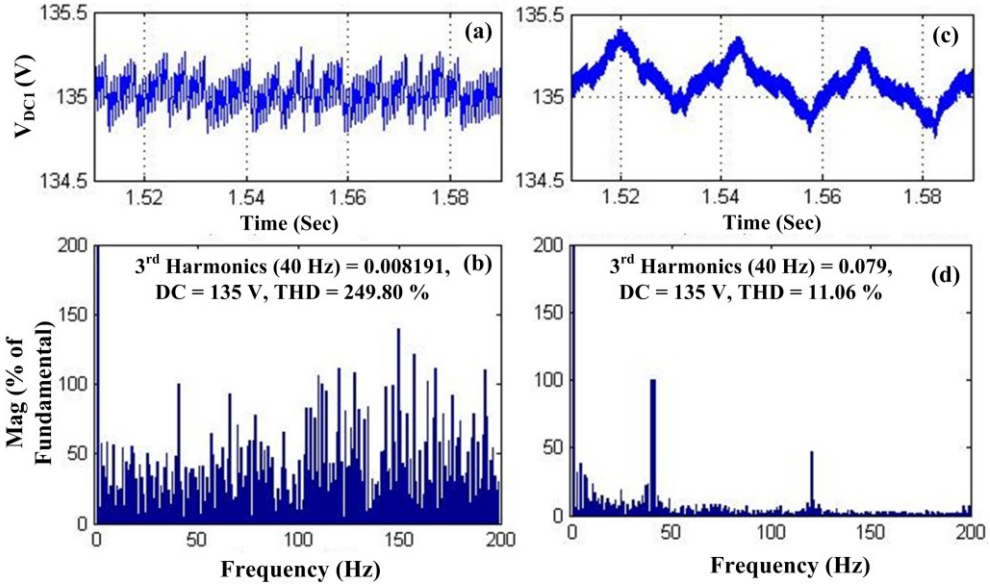


Figure 4.5 Capacitor voltage and total harmonic distortion analysis for the (a, b) SV-PWM and (c, d) Carrier-based control strategy.

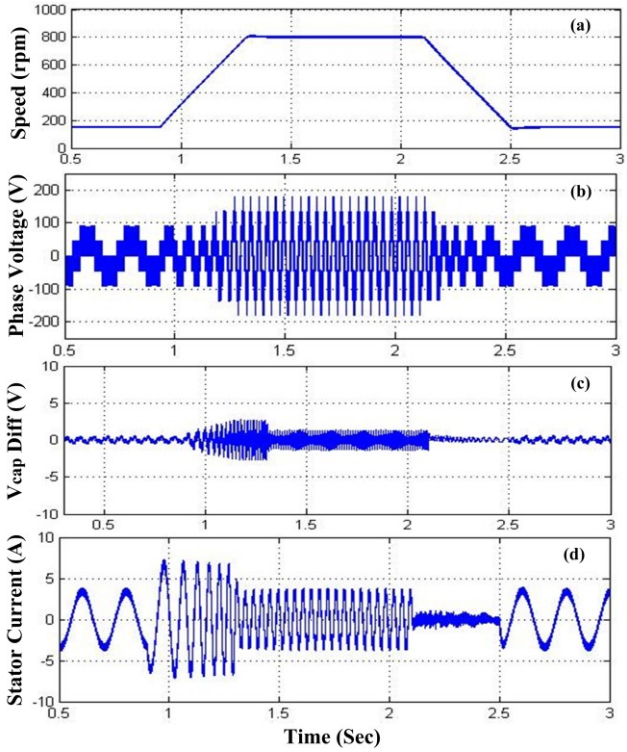


Figure 4.6 Performance results for three-level inverter with change in speed from 150.0 rpm to 800.0 rpm, while the load torque was kept constant at 6.0 N.m.; (a) Change in machine speed; (b) Phase voltage; (c) Difference between two DC-link capacitor voltages; (d) Stator current.

Fig. 4.4 shows the simulation results for the stator phase current and total harmonic distortion of the two control strategies, while the machine was operating at 19.5 Hz. The results show similar performance and %THD is also at the required tolerance level. However, with the proposed carrier based control strategy, harmonic distortions are a bit lower

compared to the SV-PWM based strategy. This is because of the uniform duty ratios generated for the carrier based strategy.

Fig. 4.5 shows the capacitor voltage (a, c) and their harmonic spectra (b, d), which influences the neutral point potential (NPP) and additional voltage stress across power switches. Here the machine is operated at 19.5 Hz and the third harmonic component (3x19.5=40.0 Hz) is observed at the neutral point. With a SV-PWM based strategy a lot of higher order harmonic components which are present in the DC-link capacitor voltage can be observed, compared to the carrier based strategy which has only the third order harmonic components. However, the DC components for both the capacitor voltages are fixed at 135.0 V, which is half of the total DC-link voltage of 270 V. As in the space vector based strategy duty ratio alternate in each switching cycle, it helps to attenuate the lower order harmonic (3^{rd}) components from the neutral point.

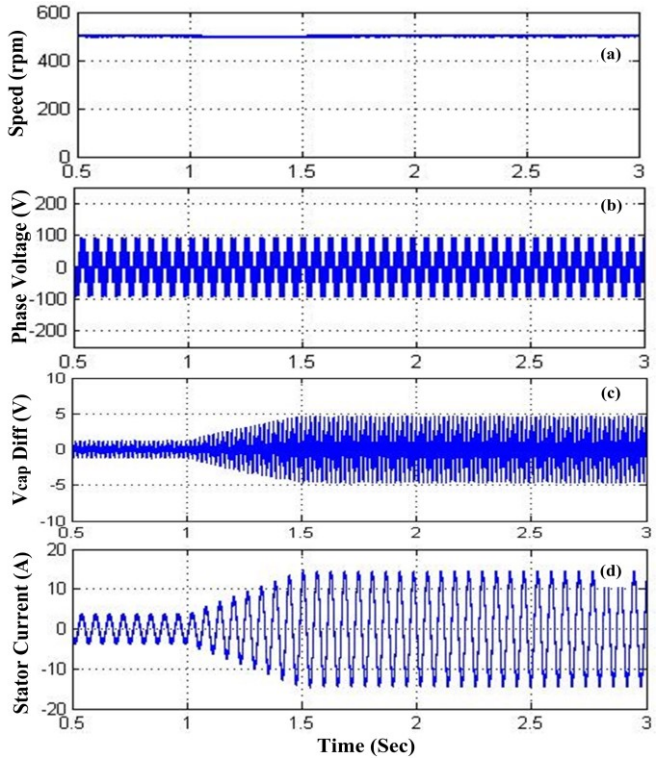


Figure 4.7 Performance results for three-level inverter with change in torque from 6.0 to 24.0 N.m., while the speed was kept constant at 500.0 rpm; (a) Machine speed; (b) Phase voltage; (c) Difference between two DC-link capacitor voltages; (d) Stator current.

The absence of the lower order harmonic components from the neutral point helps to reduce the capacitance value, which in turn reduces the capacitor size and additional space requirements.

Fig. 4.6 shows the simulation test results with the proposed carrier based control strategy, depicting a change in speed from 150.0 rpm to 800.0 rpm, while load torque was kept constant at 6.0 N.m. Fig. 4.7 shows the machine performance with change in load torque from 6.0 N.m. to 24.0 N.m., while the speed was kept constant at 500.0 rpm. It can be observed that during a change in speed, the DC-link voltage difference was balanced to its desired level. The maximum variation in the DC-link capacitor voltage difference is 4.0 V, which is 1.0% of the total DC-link voltage. Also, during change in load torque, the maximum capacitor voltage difference was less than 3.0% of the total DC-link voltage. Moreover, the performance of the system with change in speed and torque is also smooth, which shows the required performance of the proposed scheme.

4.2.2. EXPERIMENTAL TEST VERIFICATION

All the experimental test setup parameters are kept same as discussed in the earlier chapter. Fig. 4.8 shows the experimental results of the duty ratios for both the strategies. It can be observed that, the wave shapes are quite similar to the simulation results.

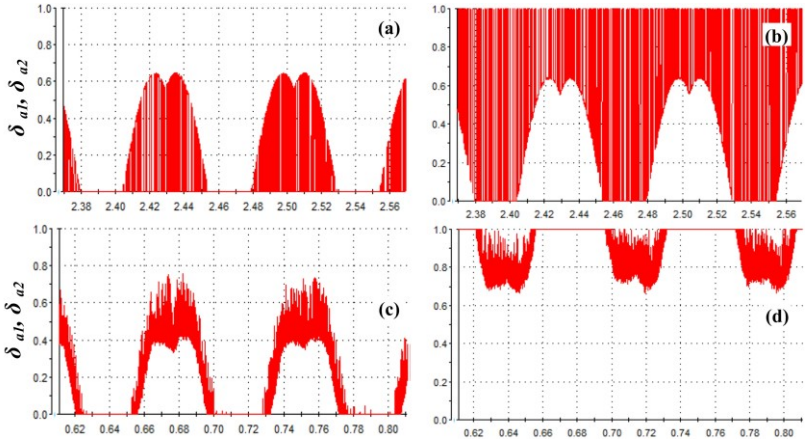


Figure 4.8 Experimental results of the duty ratios for each leg top two switches; (a), (b) For SV-PWM based control strategy. (c), (d) for carrier based PWM control strategy.

Fig. 4.9 shows the machine phase current harmonic distortion (%THD), when machine speed was kept constant at 585.0 rpm. From the results is can be observed that, with the SVPWM control strategy current harmonics are quite low (2.84%), as also shown in simulation results. However, the carrier based strategy corresponding current harmonics are bit higher. As with the carrier based strategy difference between the two capacitor voltages are directly passed through a PI controller and output from the PI controller adds to the reference voltage, all harmonics presents in the DC-link capacitor sensed voltages are going to affect the reference modulation signal. If the reference modulation signals are distorted, it is going to affect the machine torque and current harmonics as well. Hence, a low pass filter

can be used to filter out the higher frequency noise from the sensed DC-link voltage, before it is passed through the PI controller.

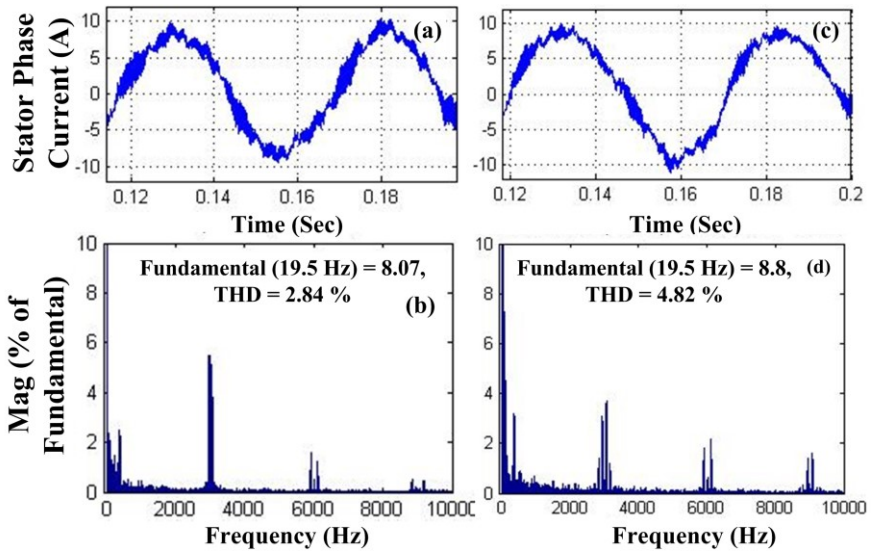


Figure 4.9 Experimental results for the phase current and the total harmonic distortion analysis for the (a, b) SV-PWM and (c, d) carrier-based PWM control strategy.

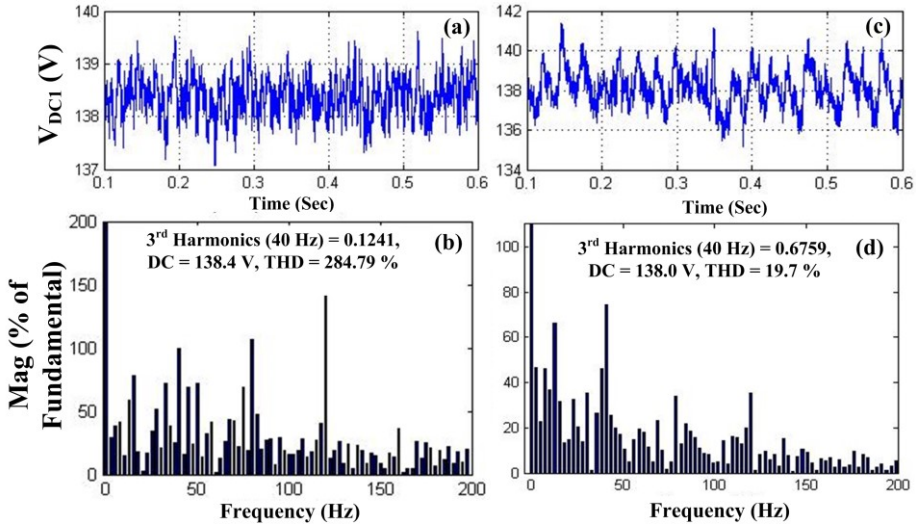


Figure 4.10 Experimental results for the capacitor voltage and the total harmonic distortion analysis for the (a, b) SV-PWM and (c, d) Carrier-based PWM control strategy.

Fig. 4.10 shows the experimental results for the change in capacitor voltage, which affects the neutral point potential and its harmonics. The machine was operated at 13.33 Hz, which corresponds to 400.0 rpm of machine speed and the corresponding third harmonic voltage was observed at 40.0 Hz. It is clear from the results that, the SV-PWM technique shows higher order harmonic components, compared to the carrier based strategy. The neutral point potential (NPP) of the carrier based strategy is dominated by the third order harmonic components. Hence, it can be concluded that the SV-PWM technique helps to reduce these lower order harmonic components by sampling the neutral point voltage more frequently.

Moreover, with SV-PWM technique the maximum peak to peak capacitor voltage deviation was 2.0 V, whereas with the carrier based strategy it was 4.0 V.

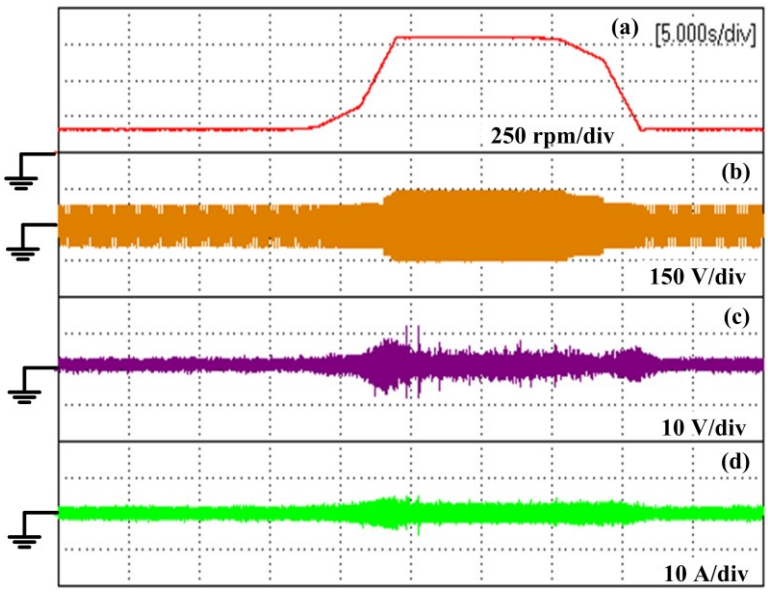


Figure 4.11 Experimental results for change in speed for the carrier based strategy from 150.0 rpm to 800.0 rpm at 6.0 N.m. load torque; (a) Machine speed; (b) Phase voltage; (c) Difference in two capacitor voltages; (d) Stator current.

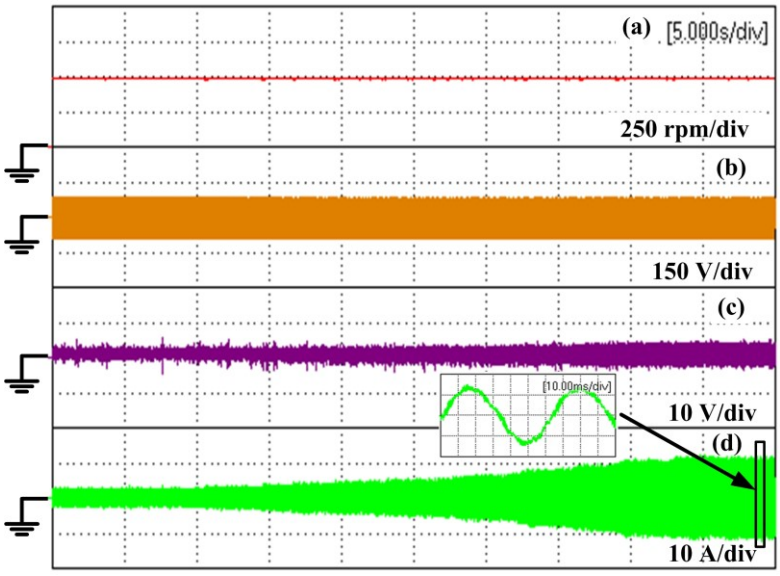


Figure 4.12 Experimental results for change in torque for the carrier based strategy from 6.0 to 24.0 N.m. while speed is kept constant at 500.0 rpm.; (a) Machine speed; (b) Phase voltage; (c) Difference in two capacitor voltages; (d) Stator current.

Fig. 4.11 shows the experimental results with the carrier based strategy when the machine speed changes from 150.0 rpm to 800.0 rpm at no load. The maximum capacitor voltage deviation is around 5.0 V, which is below 2% of the total DC-link capacitor voltage. It shows the required controllability of the proposed DC-link balancing algorithm.

Fig. 4.12 shows the machine performance during change in load torque from 6.0 N.m. to 24.0 N.m., while the machine speed was kept constant at 500 rpm. During the change in load torque, the controller was able to keep the machine speed constant at the required level and the two capacitor voltages were also balanced. The maximum DC-link capacitor voltage deviation at full load is around 5.0 V, which is around 1.85% of the total DC-link capacitor voltage.

4.3. SINGLE CARRIER-BASED HYBRID-PWM CONTROL WITH DC-LINK VOLTAGE BALANCING

The duty cycle generated in (4.1) does not take into consideration the DC-link capacitor voltage unbalanced condition, which is a potential problem with the NPC inverters. Most of the proposed control strategies use neutral point current as an indicator of voltage unbalance, which is in turn integrated, to generate the DC-offset voltage (v_o). This DC-offset voltage is then added to the original duty-cycle, to generate the compensated duty, as shown in the earlier section. However, larger variations in v_o can distort the duty-cycle, and significantly affect the phase-voltage harmonics. This situation may even over-stress the inverter switches. This may lead to over-voltage breakdown of the switches. Hence, in order to generate smaller voltage harmonics, as well as in order to reduce the voltage stress across the inverter switches, and also to eliminate additional PI controller requirement to generate the DC offset voltage a hybrid-PWM strategy is proposed here. The proposed strategy depicts the advantages of the both classic space-vector pulse-width modulations (SV-PWM) as well as carrier-based PWM. The duty-cycles for the traction inverter switches are calculated using carrier-based PWM, to reduce computational time and control complexity of the system. The redundancies of the switching states are then used to balance the two DC-link capacitor voltages, similar to SV-PWM. The proposed scheme is capable of maintaining the difference between the two DC-link capacitor voltages for a wider range of machine speed-torque variations. This is essential of EV traction applications. Furthermore, a single carrier is used for PWM, instead of multiple carriers, which reduces computational complexity. A detailed comparative study is carried out, to prove the performance difference between the existing SV-PWM techniques and the proposed hybrid-PWM strategy. In addition, total harmonic distortion of voltage and current (%$THD_{v,i}$), duty-cycles of the switches, as well as DC-link voltage balancing capabilities are also compared. Detailed simulation and experimental studies are also carried out to prove the superior performance of the proposed control strategy.

4.3.1. Principle of Operation

The proposed control circuit for 3rd harmonic PWM-based hybrid DC-link capacitor voltage balancing is shown in the Fig. 4.13. The 3-phase currents and machine speed are used to generate the three reference phase voltages (v_{abc}). A zero-sequence voltage, v_z is then generated from v_{abc}, as shown in eq. (4.1). This is then subtracted from v_{abc}, to generate the reference phase voltage (v_{abc_ref}), which is equivalent to the classic space-vector pulse-width modulation (SV-PWM) scheme. It is then converted to an appropriate duty-ratio (δ_{a,b,c_ref}), as shown in eq. (4.8). Here, it can be observed that, no DC-offset voltage it added with the reference duty cycle as shown in eq. (4.6). It eliminates the problem of getting the duty saturated in transients and in sudden load changes. However, the generated duty from this expression has both the positive and negative polarities. Hence, to convert the bipolar duty-ratio to unipolar format, so that only one carrier wave can be used, a modified control strategy is derived in (4.9), similar to (4.7). In this strategy, the negative polarity is shifted by adding the negative part with unity. Compare to the strategy proposed in [147], where there is a common overlap period in generated duty as shown in Fig. 4.1, in this proposed scheme, this overlap period is eliminated. This helps to reduce increased harmonic distortion.

$$\begin{aligned}
\delta_{\text{a_ref}} &= (v_{\text{a_ref}} / (0.5 \cdot v_{dc})) \\
\delta_{\text{b_ref}} &= (v_{\text{b_ref}} / (0.5 \cdot v_{dc})) \\
\delta_{\text{c_ref}} &= (v_{\text{c_ref}} / (0.5 \cdot v_{dc}))
\end{aligned} \tag{4.8}$$

$$\begin{aligned}
\delta_{ap} &= \delta_{a_ref}, && \text{When, } \delta_{a_ref} \rangle 0 \\
&= 0, && \text{When, } \delta_{a_ref} \langle = 0 \\
\delta_{an} &= \delta_{a_ref} + 1, && \text{When, } \delta_{a_ref} \langle 0 \\
&= 1, && \text{When, } \delta_{a_ref} \rangle = 0
\end{aligned} \tag{4.9}$$

Equation (4.9) shows the duty-cycle generated only for one phase. However, similar expressions can be used for generating the other phase duties as well.

The duty cycle generated in eq. (4.9) does not take into consideration the DC-link capacitor voltage imbalanced condition, which is a potential problem with the NPC inverters. Most of the proposed control strategies use neutral point current as an indicator of voltage imbalance, which is in turn integrated, to generate the DC-offset voltage. This DC-offset voltage is then added to the original duty-cycle, to generate the compensated duty. However, larger variations in the DC-offset voltage or "α" can distort the duty-cycle, and significantly affect the phase-voltage harmonics. This situation may even over-stress the inverter switches.

This may lead to over-voltage breakdown of the switches, as shown in chapter 2. Hence, in order to generate smaller voltage harmonics, as well as in order to reduce the voltage stress across the inverter switches, and also to eliminate additional PI controller requirement to generate the DC offset voltage a hybrid-PWM strategy is proposed here.

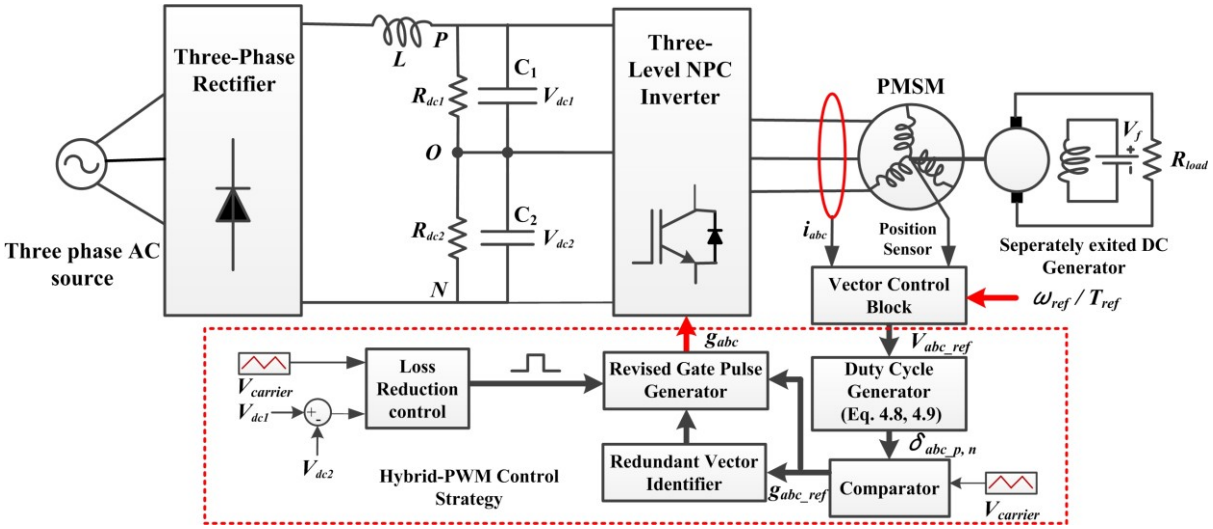


Figure 4.13 Block diagram of the proposed single carrier-based hybrid-PWM control strategy.

In the proposed hybrid carrier-based PWM control strategy, three logical control blocks are introduced. The loss reduction block updates the variation in the two capacitor voltages at the start of each switching cycle. This helps to reduce the switching losses, because it restricts the change in duty cycle between each carrier frequency cycle. The output from the comparator block generates the inverter gating signals (g_{abc_ref}), after comparing the three phase duties ($\delta_{abc\_p,n}$) with the single carrier wave. Since this block does not take care of the DC-link capacitor voltage imbalance condition, it is passed on to revised gate-pulse generator block. Another part of g_{abc_ref} goes to the redundant vector identifier block, which gives information about the redundant vector states. If g_{abc_ref} consists of any redundant states, then depending on the output from the loss reduction block, modified control pulses are generated for the inverter, as shown in Table VIII.

Table VIII: HYBRID PWM DC-LINK VOLTAGE BALANCING SCHEME

Redundant States	Balancing Ability	Switching State
POO	$v_{dc1} > v_{dc2}$	POO
	$v_{dc2} > v_{dc1}$	ONN
ONN	$v_{dc1} > v_{dc2}$	POO
	$v_{dc2} > v_{dc1}$	ONN
PPO	$v_{dc1} > v_{dc2}$	PPO
	$v_{dc2} > v_{dc1}$	OON
OON	$v_{dc1} > v_{dc2}$	PPO
	$v_{dc2} > v_{dc1}$	OON

OPO	$v_{dc1} > v_{dc2}$	OPO
	$v_{dc2} > v_{dc1}$	NON
NON	$v_{dc1} > v_{dc2}$	OPO
	$v_{dc2} > v_{dc1}$	NON
OPP	$v_{dc1} > v_{dc2}$	OPP
	$v_{dc2} > v_{dc1}$	NOO
NOO	$v_{dc1} > v_{dc2}$	OPP
	$v_{dc2} > v_{dc1}$	NOO
OOP	$v_{dc1} > v_{dc2}$	OOP
	$v_{dc2} > v_{dc1}$	NNO
NNO	$v_{dc1} > v_{dc2}$	OOP
	$v_{dc2} > v_{dc1}$	NNO
POP	$v_{dc1} > v_{dc2}$	POP
	$v_{dc2} > v_{dc1}$	ONO
ONO	$v_{dc1} > v_{dc2}$	POP
	$v_{dc2} > v_{dc1}$	ONO
PON,OPN,NPO,NOP,ONP,PNO	$v_{dc1} > v_{dc2}$ *or* $v_{dc2} > v_{dc1}$	PON,OPN,NPO,NOP,ONP,PNO
PNN,PPN,NPN,NPP,NNP,PNP	$v_{dc1} > v_{dc2}$ *or* $v_{dc2} > v_{dc1}$	PNN,PPN,NPN,NPP,NNP,PNP

From Table VIII, it can be observed that, g_{abc} is different from g_{abc_ref}, only if redundant voltage states exist. For medium- and large-voltage vectors, gating signals do not change their sequence, since they cannot affect capacitor voltage balancing ability. As positive voltage vectors are related to the upper capacitor voltage, and negative vectors are related to the lower capacitor voltage, if $v_{dc1} > v_{dc2}$, the positive vectors are utilized and if $v_{dc1} < v_{dc2}$, the lower capacitor voltages are used. Hence, the complicated and time consuming duty-cycle calculation process of the SV-PWM strategy (as shown in Table III), is replace by a much more efficient, single carrier-based strategy. Once the duties of the individual inverter switches are generated, redundant states of the switches are used to keep the DC-link capacitor voltages stable, with equal distribution of positive and negative switching states. The proposed strategy helps to keep the harmonic voltage distortion low, while maintaining the difference between the two capacitor voltages in between tolerance band (5% of the total DC-link voltage) even at high torque-speed transients.

Fig. 4.14 shows the duty cycle redistribution with the proposed control strategy depending on the two DC-link capacitor voltages. Suppose initial duty ratio generated form the machine control loop operates the system with POO switching sequence, and if the upper capacitor voltage is larger than the lower one, system will operate with the initial sequence only (Fig. 4.14, a). However, if the lower capacitor voltage appears to be higher than the upper one, the duty ratio will be going to redistribute according to table VIII. Because of this change in switching states in between one switching cycle, could introduce additional switching losses compared with the conventional space vector PWM strategy. However,

because of the loss reduction block, which allows any change in switching sequence only at the starting of each switching cycle, the additional switching losses can be reduced. Moreover, because of this hybrid-PWM control the additional PI controller requirement to balance the DC-link capacitor voltages is completely eliminated.

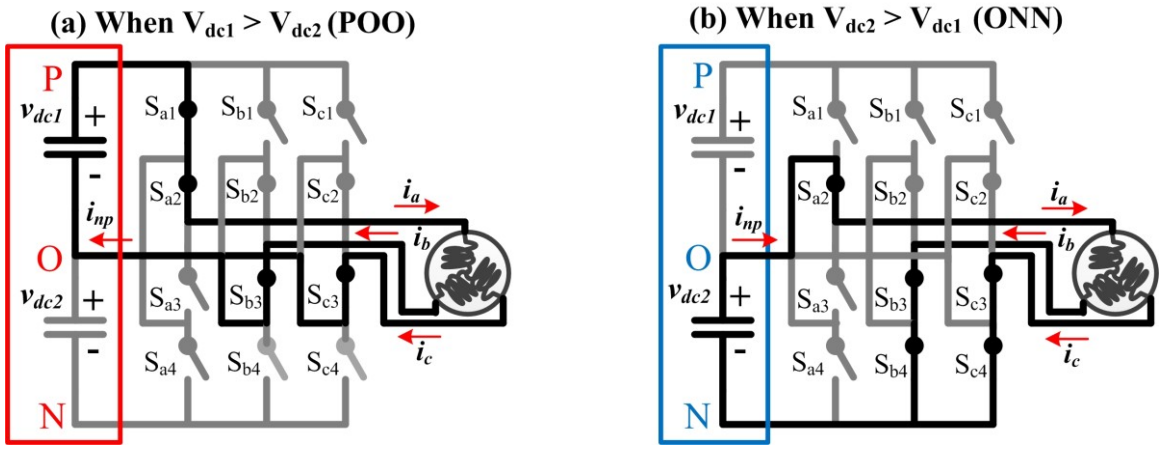


Figure 4.14 Switching state with the proposed Hybrid-PWM control strategy.

4.3.2. SIMULATION TEST RESULTS

Fig. 4.15 shows the duty ratios with the proposed hybrid-PWM based control strategy, at a modulation index of 0.38. In case of the hybrid carrier-based strategy, duty ratio calculation does not change, as there is no dc-offset voltage added with the duties generally being done for carrier based strategy. However, voltage sharing between the 2 capacitor voltages indeed changes. Hence, from the resultant plots, it is obvious that the generated duty cycle will derive much lower transients, compared to the SV-PWM based strategy.

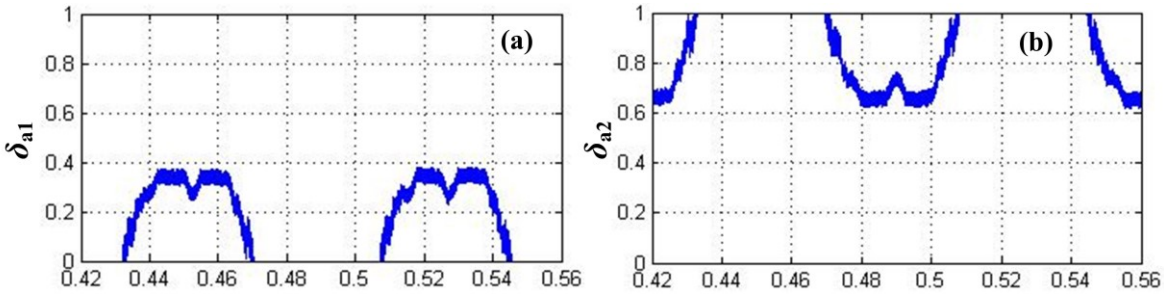


Figure 4.15 Duty ratios for each leg (top 2 switches) with Hybrid PWM control strategy.

Fig. 4.16 shows the simulation results for the stator phase current [Fig. 4.16 (a)] and the total harmonic distortion [Fig. 4.16 (b)], while machine was operates at 585.0 rpm (19.5 Hz). The harmonic distortion levels are observed to be significantly lower for the proposed hybrid carrier-based control strategy, compared to the classic SV-PWM strategy.

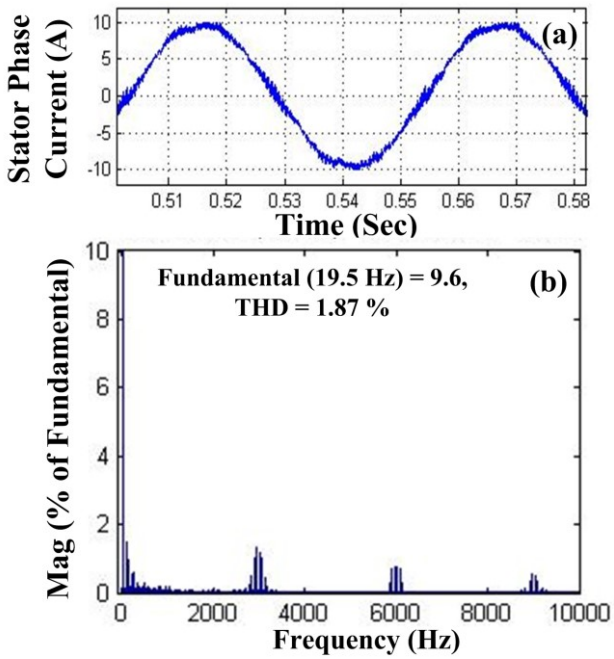


Figure 4.16 Phase current and total harmonic distortion analysis for the hybrid carrier-based control strategy.

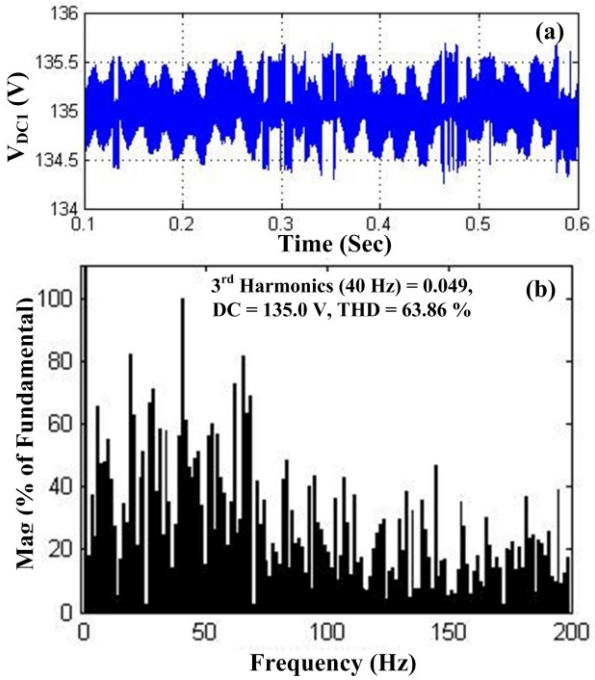


Figure 4.17 Capacitor voltage deviation and total harmonic distortion analysis for the proposed hybrid carrier-based control strategy.

Fig. 4.17 shows the capacitor voltage deviation [Fig. 4.17 (a)] and their harmonic spectra [Fig. 4.17 (b)], which influences the neutral point potential (NPP) as well as the additional voltage stress across the inverter switches. The fundamental system frequency was kept at 13.33 Hz and the corresponding 3rd harmonic voltage component is observed at 40 Hz. Compared to the SV-PWM based strategy the lower order harmonics are bit higher in case of hybrid-PWM based strategy. Hence, it can be concluded that in terms of 3rd harmonic

components at the neutral point, it performs in between the space vector PWM and carried based PWM strategy.

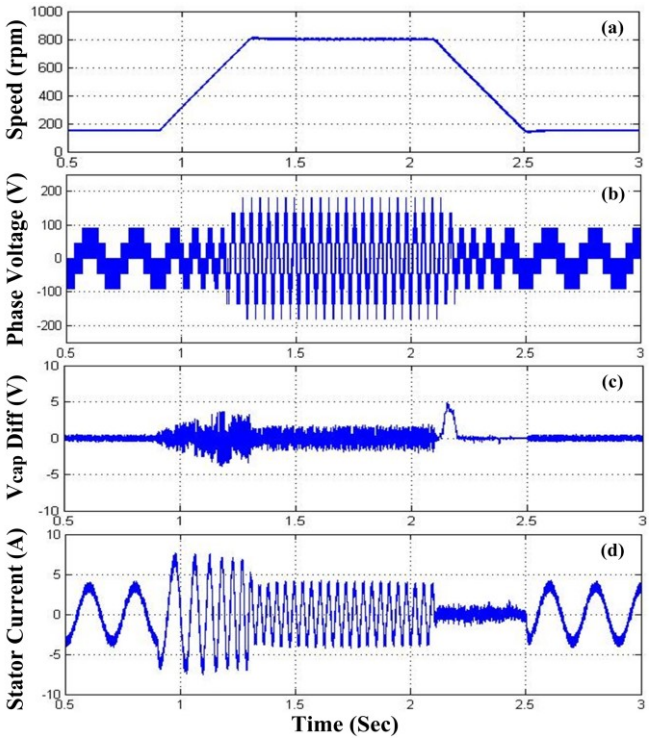


Figure 4.18 Performance results for 3-level inverter – Change in speed from 150.0 rpm to 800.0 rpm; Load torque is constant at 6.0 N.m.; (a) Change in machine speed; (b) Phase voltage; (c) Difference between two DC-link capacitor voltages; (d) Stator current.

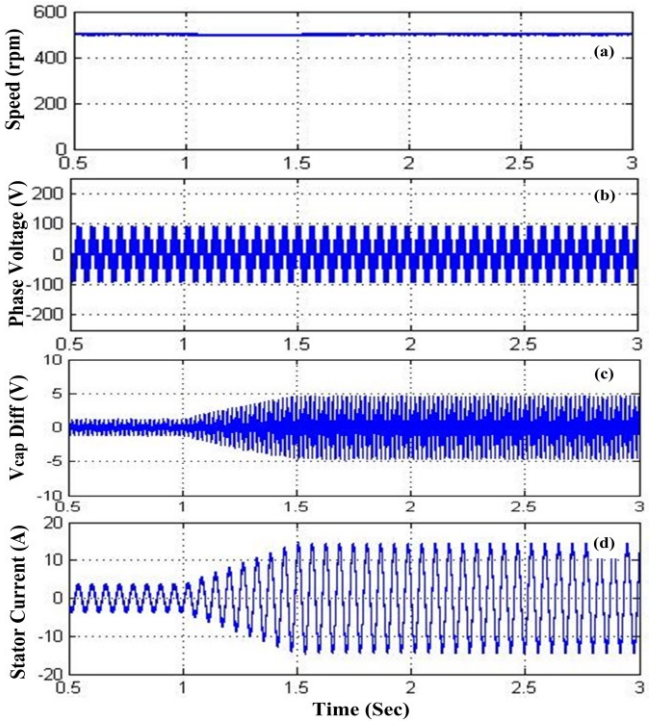


Figure 4.19 Performance results for 3-level inverter – Change in torque from 6.0 to 24.0 N.m.; Speed is constant at 500.0 rpm: (a) Machine speed; (b) Phase voltage; (c) Difference between two DC-link capacitor voltages; (d) Stator current.

Fig. 4.18 shows the simulation test results with the proposed hybrid carrier-based control strategy, depicting change in speed from 150.0 rpm to 800 rpm, while load torque was kept constant at 6.0 N.m. Furthermore, Fig. 4.19 shows the machine performance with change in load torque from 6.0 N.m. to 24.0 N.m., while the speed was kept constant at 500.0 rpm. It can be observed that during change in speed and torque, the DC-link voltage difference was balanced to its desired level. The maximum variation in DC-link capacitor voltage during change in speed is 2.0 V, which is below 1.0% of the total DC-link voltage. In addition, during a change in load torque, the maximum capacitor voltage difference was 4.0 V, which is again 1.48% of the total DC-link voltage. Moreover, the performance of the system with change in speed and torque is also smooth, which illustrates the superior performance of the proposed scheme.

Fig. 4.20 shows the switching sequence with the proposed hybrid PWM control strategy, for sub-sector I in sector I. In this subsector there are total four redundant voltage vectors (POO, ONN, PPO, OON) and three null vectors available (PPP, NNN, OOO). From the switching sequence it can be observed that, the redundant vectors are symmetrical to the carrier and total numbers of switching sequences are 7.

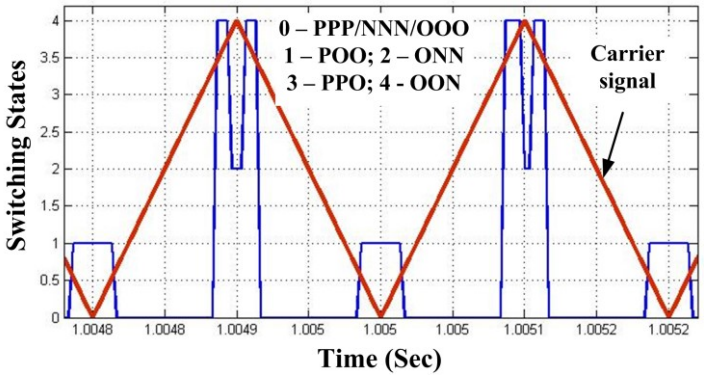


Figure 4.20 Switching sequence for proposed hybrid PWM control strategy for 1st sub-sector in sector I.

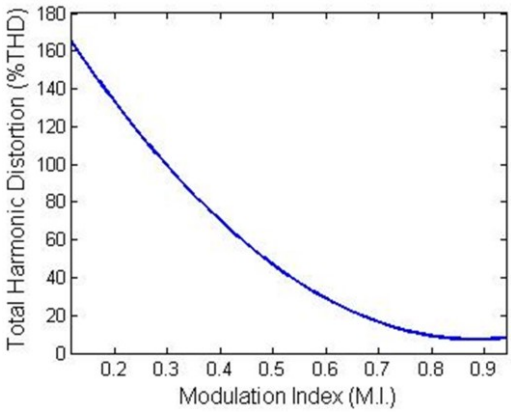


Figure 4.21 Total voltage harmonic distortion for hybrid PWM.

Fig. 4.21 shows the total harmonic distortion of hybrid PWM strategy with change in modulation index. Results show uniform reduction in harmonic distortion with higher modulation indices.

4.3.3. EXPERIMENTAL TEST SETUP AND VERIFICATION STUDIES

Fig. 4.22 shows the experimental results of the duty ratios for the hybrid PWM based control strategy. It can be observed that the plots are quite similar to the simulation results. Moreover, the duty cycle generated from the proposed carrier-based strategy has much lower transients compared to the SV-PWM based strategy, as already shown in simulation results.

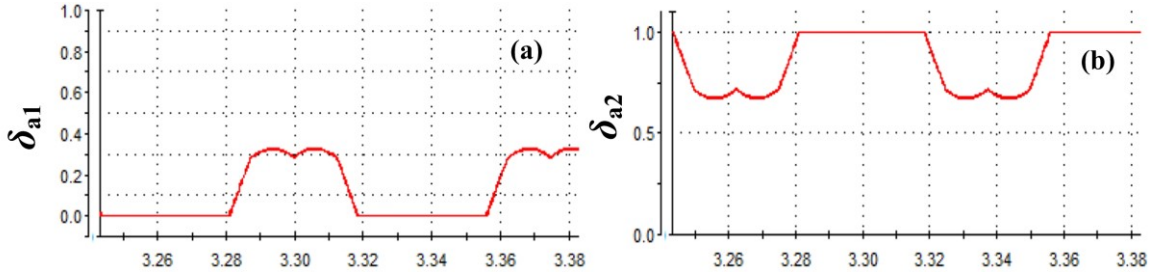


Figure 4.22 Experimental results for duty ratios for each leg (top 2 switches) with Hybrid PWM control strategy.

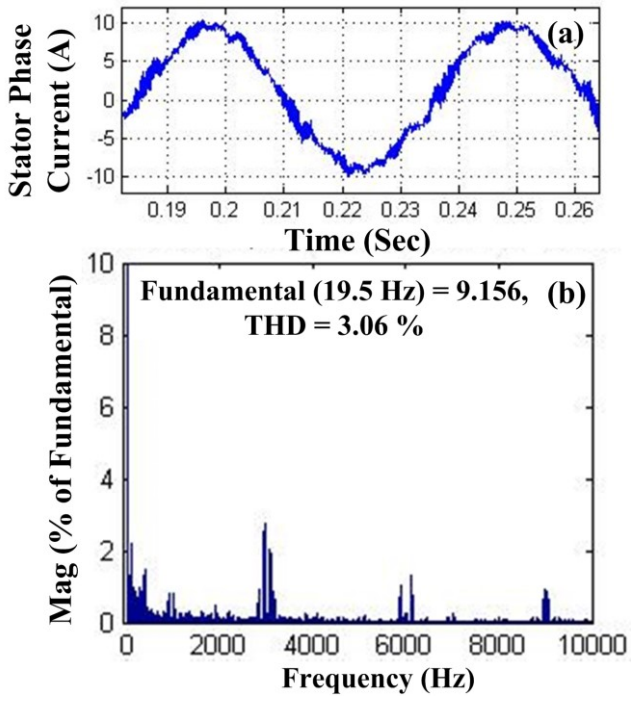


Figure 4.23 Experimental results for phase current and total harmonic distortion using the developed hybrid carrier-based control strategy.

Fig. 4.23 shows the machine phase current harmonic distortion (%THD), when machine speed was kept constant at 585.0 rpm (19.5 Hz). With the carrier-based strategy, the corresponding current harmonics are lower as compared to carrier based strategy.

Furthermore, Fig. 4.24 shows the experimental results for the change in capacitor voltage, which affects the neutral point potential and harmonics. The machine was operated at 13.33 Hz, which corresponds to 400.0 rpm machine speed, and the corresponding third harmonic voltage was observed at 40.0 Hz. Results are quite similar to the simulation studies.

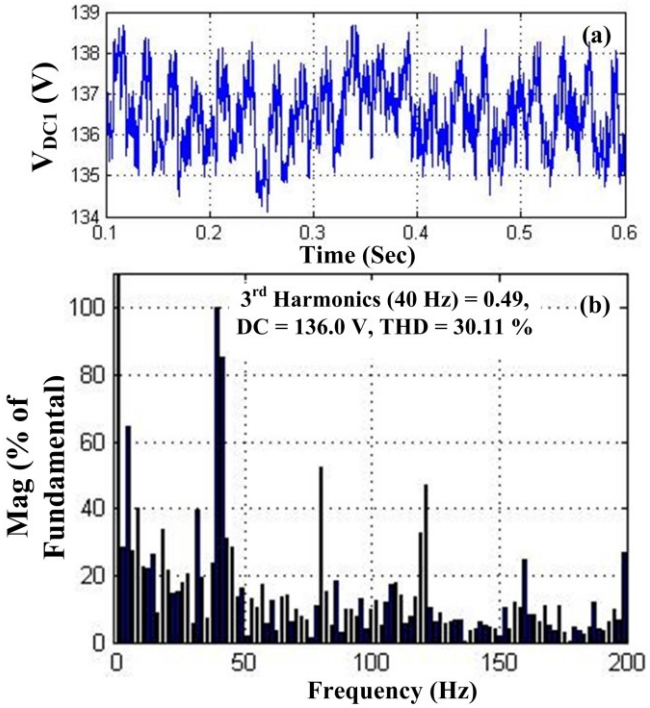


Figure 4.24 Experimental results for the capacitor voltage deviation and the total harmonic distortion analysis for the hybrid PWM based control strategy.

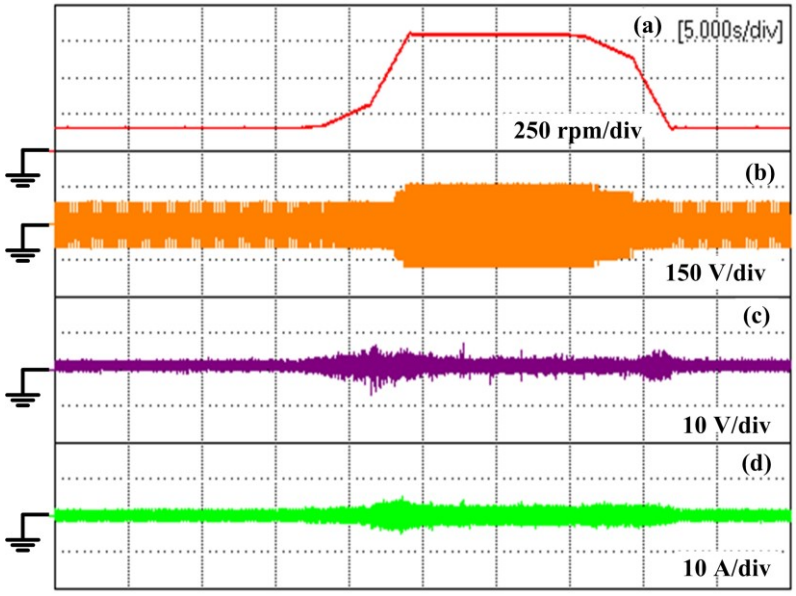


Figure 4.25 Experimental results for change in speed for the hybrid PWM based strategy from 150.0 rpm to 800.0 rpm at 6.0 N.m. load torque; (a) Machine speed; (b) Phase voltage; (c) Difference in two capacitor voltages; (d) Stator current.

Fig. 4.25 shows the experimental results with the hybrid PWM strategy, when the machine speed changes from 150.0 rpm to 800.0 rpm with 6.0 N.m. load torque. The maximum capacitor voltage deviation is around 3.0 V, which is 1.1% of the total DC-link capacitor voltage. It shows the required controllability of the proposed DC-link balancing algorithm. Fig. 4.26 shows the machine performance during change in load torque from 6.0 N.m. to 24.0 N.m., while the machine speed was kept constant at 485.0 rpm. During the change in load torque, the controller is able to keep the machine speed constant at the required level, while keeping the two capacitor voltages balanced at the same time. The maximum DC-link capacitor voltage deviation at full load is around 10.0 V, which is around 3.7% of the total DC-link capacitor voltage.

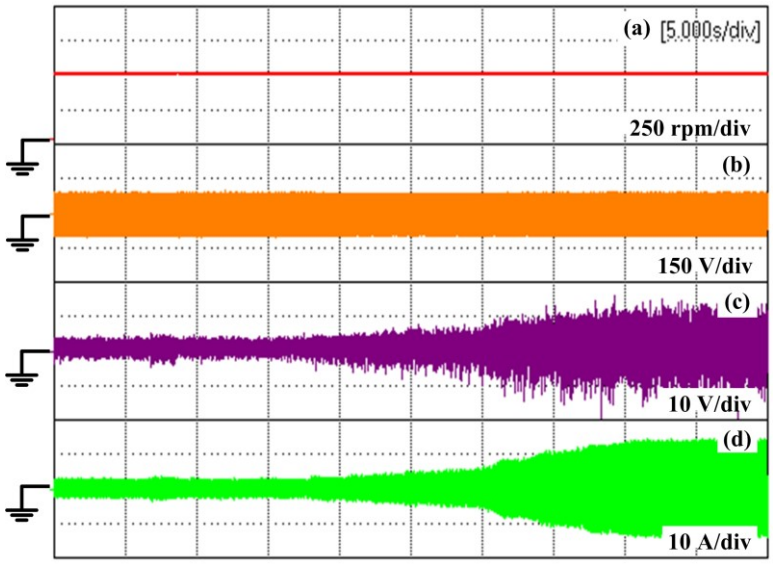


Figure 4.26 Experimental results for change in torque for the hybrid PWM based strategy from 6.0 to 24.0 N.m. while speed was kept constant at 485.0 rpm; (a) Machine speed; (b) Phase voltage; (c) Difference between two DC-link capacitor voltages; (c) Stator current.

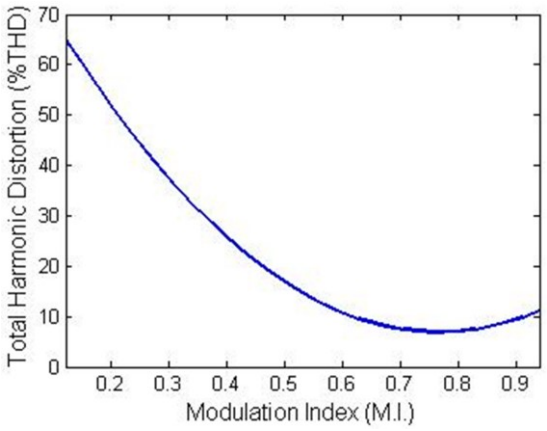


Figure 4.27 Experimental results for total voltage harmonic distortion for hybrid PWM.

Fig. 4.27 shows the total harmonic distortion for the hybrid carrier based strategy with change modulation index. Results follow quite similar trend as link the simulation results.

4.4. HYBRID-PWM BASED DISCONTINIOUS-PWM STRATEGY WITH DC-LINK VOLTAGE BALANCING

A modified discontinuous-PWM (DPWM) based DC-link voltage balancing strategy is proposed based on the proposed hybrid PWM strategy. It also helps to reduce the total inverter losses considerably, as like in 2-level inverter DPWM strategy. The proposed strategy is also able to balance the two DC-link capacitor voltages for the entire range of machine speed torque variations and also reduces the total inverter losse considerably. To overcome the problem with DC-link voltage balancing with carrier based DPWM strategy, a simple single carrier based PWM technique is proposed in this paper. In this strategy, the modulation signals are generated based on the hybrid PWM strategy, and then compared with a triangular carrier signal. It is then passed through a redundant vector identification table to find the redundant voltage vectors. During the neutral point voltage fluctuation, redundant states are used as like in case of SVPWM based strategy to keep the fluctuation low. As there is no use of any offset with the reference modulation signals or no change with the duration of +ve or –ve bus clamping time, it will also reduce the voltage harmonic distortion. Moreover, as change in the two capacitor voltages are sampled at each switching cycle, the proposed system is quite fast for any amount of load change. Detailed simulation and experimental performances are carried out to show the performance of the system.

4.4.1. Conventional DPWM Control Strategy

Discontinuous PWM is a widely used method to keep the inverter losses low at higher load currents. In this type of control strategy one of the inverter lags is generally clamped to the positive or negative DC-bus as shown for the two-level inverter. However, the total harmonic distortion is comparatively higher than the continuous PWM. The modulation signal used for two-level inverter can be used for the three-level inverter as well. However, there will be two carrier signals instead of one, as in case of three-level inverter, as shown in Fig. 4.28 (b).

There are different kinds of DPWM techniques available depending on the load power factor. The purposes of all these modulation techniques are to make the pole of any one of the legs to stop switching for 120° in one power cycle. To combine all these PWM techniques to one, a generalized PWM strategy is proposed in [39]. The zero sequence voltage (v_z) generated in (4.11) is then added with the phase voltage signals (v_{abc}) as shown in (4.13) to

generate the reference phase voltages (v_{abc_ref}). The ranges of discontinuous functions are realized by selecting α (Eq. 4.10). Choosing constant values of α to 0, 0.5 and 1.0, DPWMMAX, SVPWM, and DPWMMIN can be generated. As SPMSM machine mostly operates close to unity power factor, we will keep the modulation angle δ to Π/6.

$$\alpha = 1 - 0.5[1 + \text{sgn}(\cos\ 3(\theta_{re} + \delta))] \tag{4.10}$$

$$\upsilon_z = 0.5 \cdot \upsilon_{dc}(2 \cdot \alpha - 1) - \alpha \cdot \upsilon_{\max} + \upsilon_{\min}(\alpha - 1) \tag{4.11}$$

Here, θ_{re} is the rotor position in rad, v_{dc} is the DC-link voltage and $v_{min,\ max}$ are the minimum and maximum values of the three reference voltage signals, shown in Eq. (4.12).

$$\upsilon_{\max} = Max\ (\upsilon_a, \upsilon_b, \upsilon_c);\ \upsilon_{\min} = Min\ (\upsilon_a, \upsilon_b, \upsilon_c) \tag{4.12}$$

Where, $v_{a,\ b,\ c}$ are the three reference phase voltages.

$$\begin{aligned} \upsilon_{a\_ref} &= \upsilon_a + \upsilon_z \\ \upsilon_{b\_ref} &= \upsilon_b + \upsilon_z \\ \upsilon_{c\_ref} &= \upsilon_c + \upsilon_z \end{aligned} \tag{4.13}$$

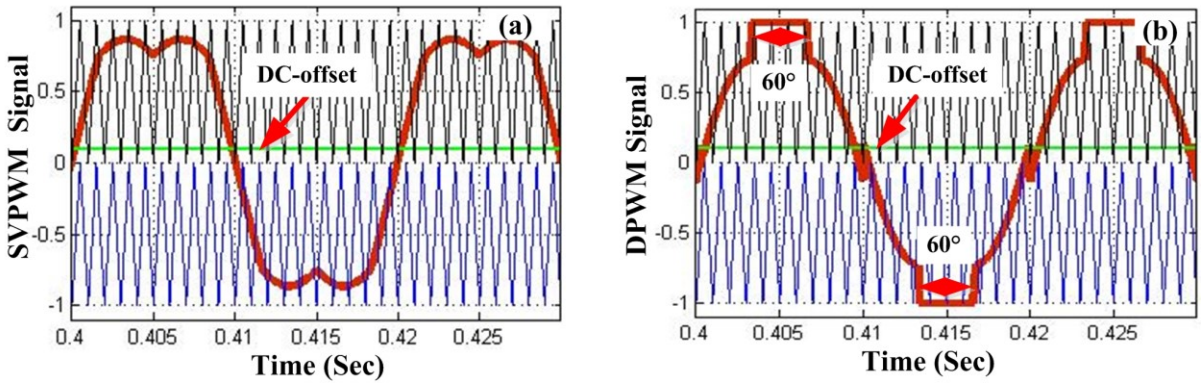


Figure 4.28 Continuous (SVPWM) (a) and discontinuous PWM (b) signals.

The modulating signals ($v_{a,b,c}$) are generated from the control loop, can be added with the zero sequence voltage component (v_z) to produce the reference voltage for the inverter switches (v_{a,b,c_ref}) as shown in Eq. 4.13. Fig. 4.28 shows the two different modulation signals by adding different zero sequence voltages with similar reference modulation signal, as shown in Eq. 4.13. Fig. 4.28 (a) shows the space-vector PWM corresponding modulation signal and Fig. 4.28 (b) shows the DPWM signal. With the control strategy shown in Fig. 4.28, two carrier signals are required to trigger the four switches for each leg. The upper carrier signal with the positive modulation signal generate gate pulses for T_{A1}, T_{A3} and the lower carrier signal with the negative side of the modulating signal produces the gate pulses for T_{A2}, T_{A4}.

4.4.2. Conventional DC-Link Capacitor Voltage Balancing Schemes and Associated Problems

In this type of strategy a DC-offset voltage is generally being added with the reference modulating signal [126], [148], [149] as shown in Fig. 4.28, (b). Hence, when the upper capacitor voltage is higher than the lower capacitor voltage, a positive DC-offset voltage is added, to make use of the positive redundant voltage vectors more than the negative voltage vectors. The same is true when the lower capacitor voltage is higher than the upper one. In that case a negative DC-offset voltage is required to add. However, this strategy has a problem with the range of the DC-offset, because if the offset is higher than the required value, it may create more neutral point voltage deviation. Addition of DC-offset shifts the modulating signal vertically up or down wards. Hence, in case of larger transients when capacitor voltages are unbalanced, it may happen that, a larger value of DC-offset could be generated from the control circuit, which shifts the signal completely in positive or negative half. It will make the generated PWM waveform asymmetrical, which could make the system uncontrollable. Hence there is always a limit of DC-offset voltage that is required to set, to avoid such condition. The value of DC-offset voltage is generally being generated by directly measuring the two capacitor voltages and then passing the difference between them through a PI controller, which generate the offset voltage (v_o). Alternatively, the neutral point current can be sensed or generated from the three phase current and duty ratios and integrated them over one carrier cycle to generate the DC-offset voltage. As the results shown in [149], there is always a time (0.3 Sec) required to balance the two capacitor voltages, even with a stable RL load, without any transients. Moreover, the current waveforms shown have spikes, in steady state. In case of DPWM this strategy is even trickier. During the positive 60° clamping period, the upper capacitor voltage is going to discharge more than the lower capacitor voltage, as it is clamped to the positive DC-bus voltage. Even though the negative DC-offset voltage would be applied to keep the capacitor voltages balanced, it might not be possible to balance the system as shown in [128]. This problem is more Sevier with more frequent transients systems, like for electric vehicle applications, due to rapid change in speed and torque demands. The same argument hold good for negative DC-bus clamping period as well.

To overcome this problem, a modified strategy is proposed in [128]. Instead of adding additional DC-offsets, the clamping period for the upper and the lower cycle is redistributed. If the upper capacitor voltage is higher than the lower capacitor voltage, its total clamping period will increase to more than 60° where that of the lower cycle will go below 60°. The reverse is true, when the lower capacitor voltage is higher than the upper capacitor voltage. In

case of a transient system, it may happen that the total 120° clamping duration could appear in positive half or in the negative half cycle. It will introduce asymmetry in the generated voltage spectra and will increase the total voltage and current harmonic distortion in the system. From the results shown it can be depicted that, there is also a certain time delay, between applying the control strategy and before the two capacitor voltage get balanced, similar to previously proposed strategy. Moreover, the phase voltage has different clamping period in positive and negative half, which will introduce asymmetry and harmonics in the generated voltage. Hence this system is also not a good choice for EV applications.

4.4.3. Proposed DC-link Balancing Strategy

The reference duty cycles ($\delta_{a,b,c\_p,n}$) for the switches are generated similar like the proposed hybrid PWM based control strategy, as shown in (4.8, 4.9). However, the zero sequence voltage (v_z) is generated from (4.11). The generated duty cycle will look similar to fig. 4.29. However, with the duty ratios generated for the power switches the DC-link balancing is not considered. The following section describes the proposed control strategy that keeps the DC-link capacitor balanced for wider range of machine torque speed variations for an electric vehicle.

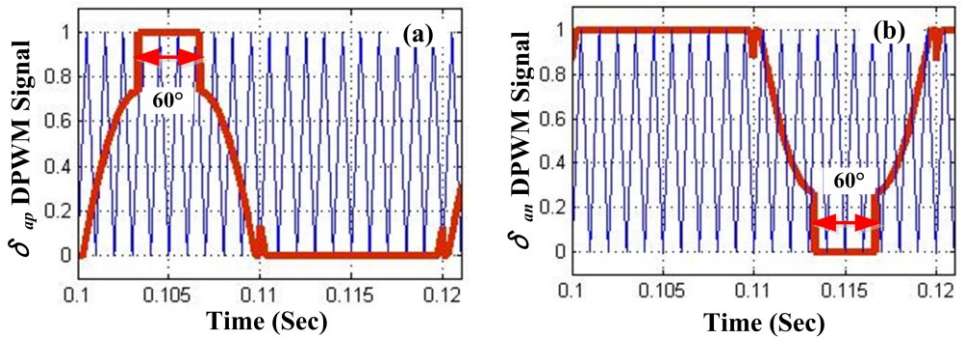


Figure 4.29 Modified DPWM reference signals; (a) Corresponding to upper modulating signal for TA1, TA3 ; (b) Lower modulating signal TA2, TA4.

Fig. 4.30 shows the basic flow chart for the proposed DC-link balancing strategy, as also shown in the earlier hybrid PWM strategy. In this strategy, first the reference phase voltages (v_{abc_ref}) are generated from the vector control block and then converted to the corresponding duty ratios ($\delta_{abc\_p,n}$). In the generated duty cycles the negative half is also shifted to the positive side, which eliminates the requirement of an additional carrier signal compared to the conventional one as shown in Fig. 4.28. It is then compared with the carrier signal to generate the gate signals for the power switches (g_{abc_ref}). These pulses are then passed through a conditional block, which decides whether there is any redundant small voltage vector

available. If there is no small vector available, signal directly goes to the inverter switches. However, if there is any redundant voltage vector present, then according to the two capacitor voltages, the duty ratios redistributed according to table VIII.

The control circuit diagram will be similar like the hybrid PWM strategy as shown in Fig. 4.13.

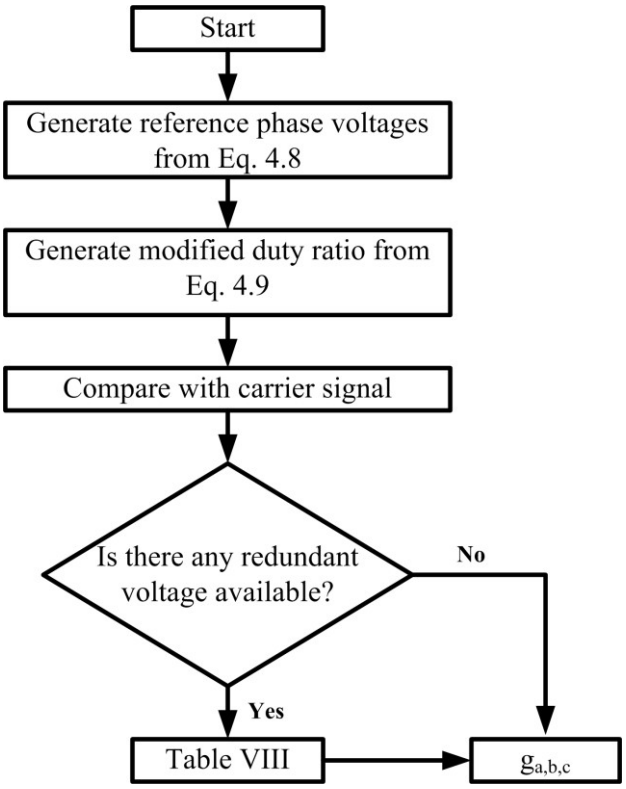


Figure 4.30 Flow chart for the proposed DC-Link voltage balancing scheme for DPWM

4.4.4. Simulation Results for Discontinuous-PWM Control Strategy

Fig. 4.31 shows the duty ratios for the phase A power switches at two different modulation indexes of 0.23 (a, b) and 0.87 (c, d). From the simulation results it can be observed that at each half cycle, the modulating signal is clamped to either positive or in the negative DC-bus voltage.

Fig. 4.32 shows the phase voltages with the conventional DC-offset based DPWM and the proposed DPWM control strategy with modulation index (M.I.) of 0.46. From the results, phase voltages look almost similar, however with the conventional strategy; the voltage spikes are bit higher than the proposed strategy. Fig. 4.33 shows the stator current with both the strategies. Here also, the current harmonic distortion with conventional strategy is bit higher than the proposed scheme.

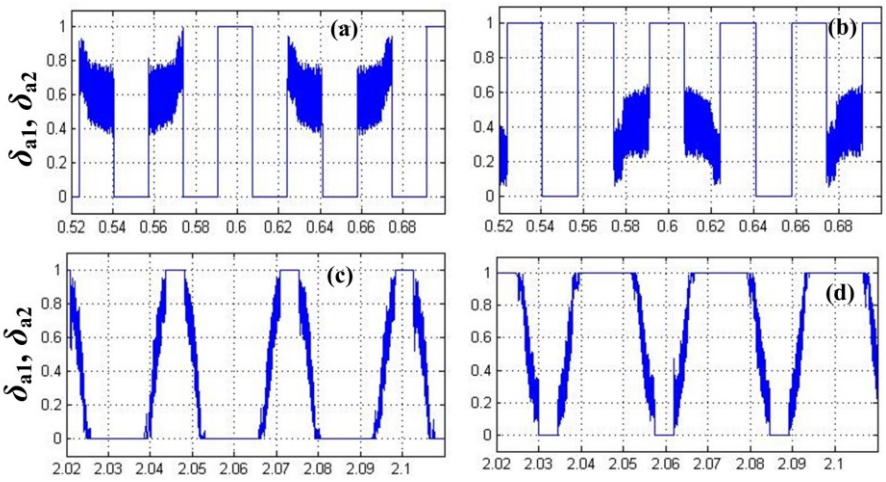


Figure 4.31 Duty ratios with proposed DPWM strategy at modulation index of; (a), (b) 0.23. (c), (d) 0.87.

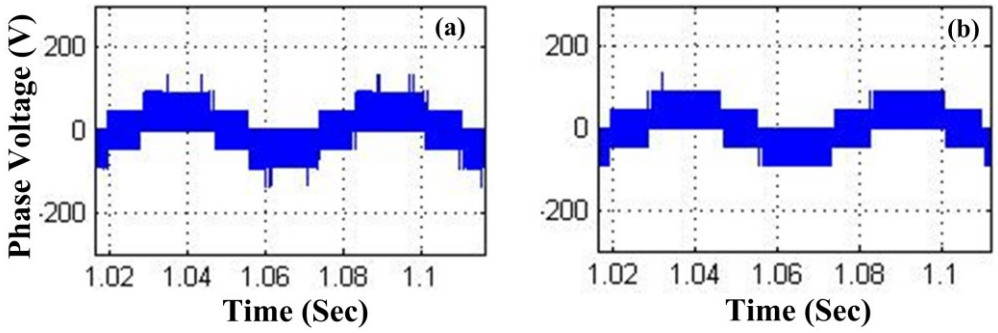


Figure 4.32 Phase voltage comparison of the (a) Conventional DC-offset based DPWM and (b) Proposed DPWM based control scheme.

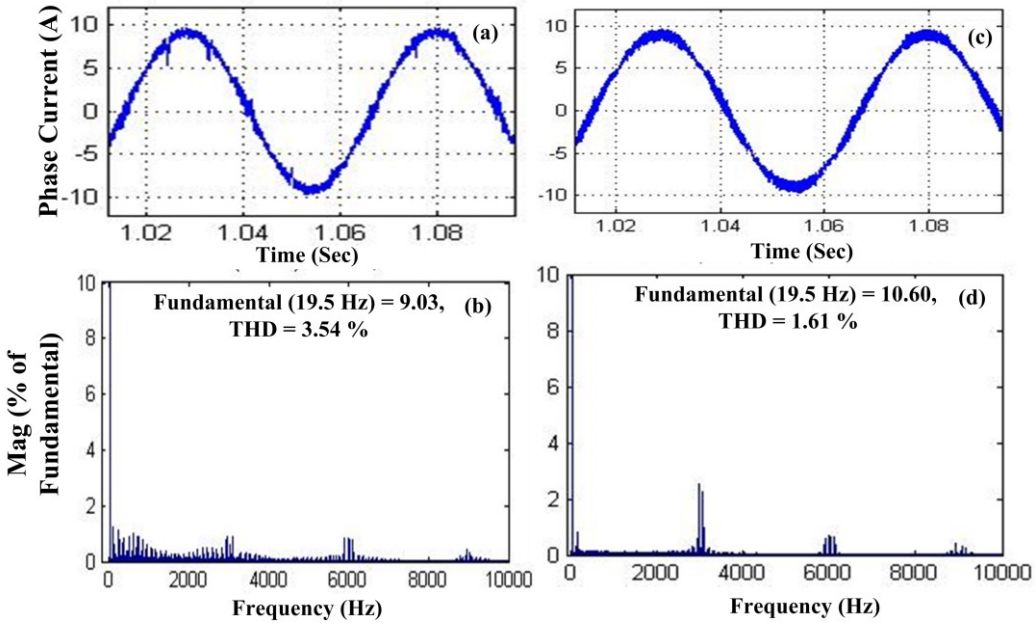


Figure 4.33 Phase current and total harmonic distortion analysis of the (a, b) Conventional DC-offset based DPWM and (c, d) Proposed DPWM based control scheme.

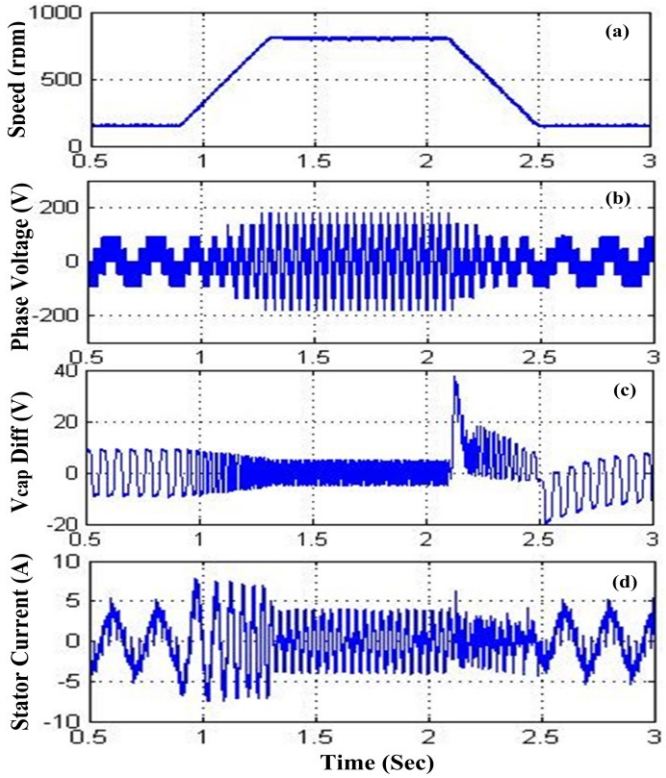


Figure 4.34 Performance results for the three-level DPWM with conventional DC-offset based DPWM technique for change in speed from 150.0 rpm to 800.0 rpm, while the load torque was kept constant at 6.0 N.m.; (a) Change in machine speed; (b) Phase voltage; (c) Difference between two DC-link capacitor voltages; (d) Stator current.

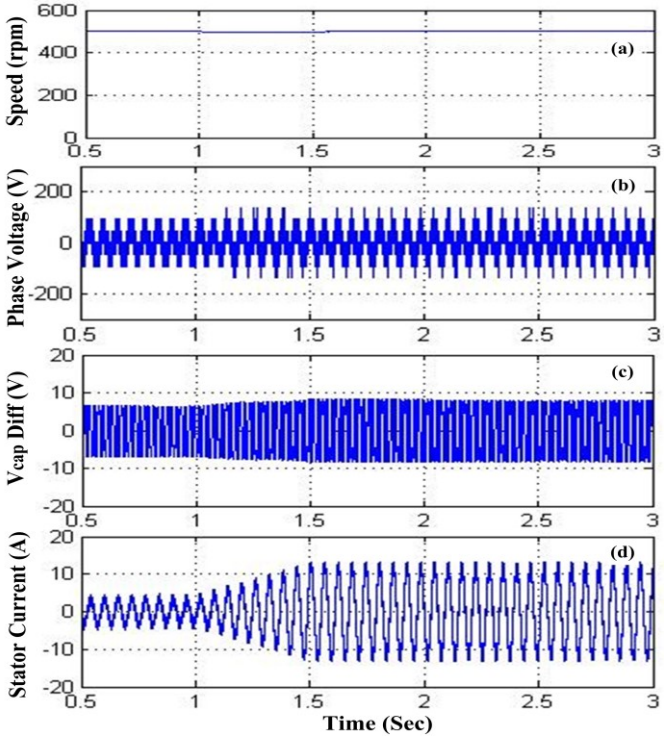


Figure 4.35 Performance results for three-level DPWM with conventional DC-offset based DPWM technique for change in torque from 6.0 to 24.0 N.m., while the speed was kept constant at 500.0 rpm.; (a) Machine speed; (b) Phase voltage; (c) Difference between two DC-link capacitor voltages; (d) Stator current.

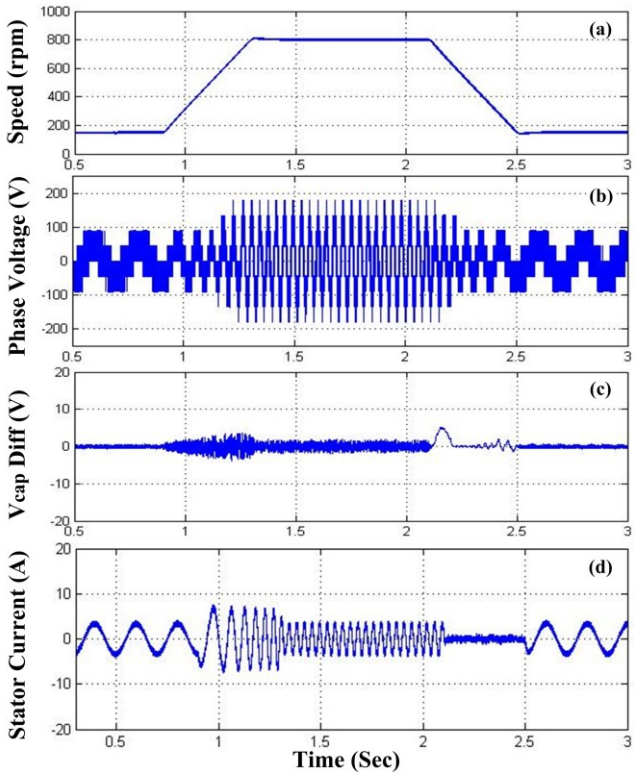


Figure 4.36 Performance results for proposed DPWM based three-level inverter with change in speed from 150.0 rpm to 800.0 rpm, while the load torque was kept constant at 6.0 N.m.; (a) Change in machine speed; (b) Phase voltage; (c) Difference between two DC-link capacitor voltages; (d) Stator current.

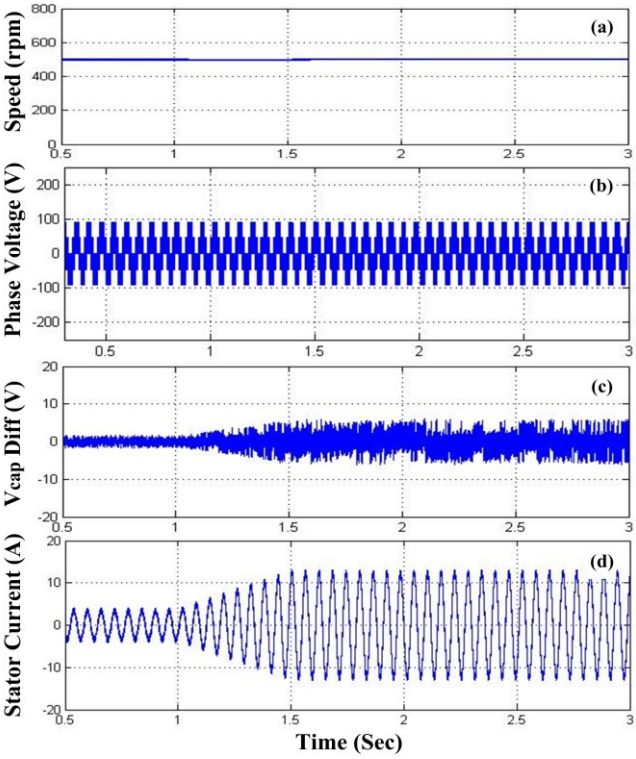


Figure 4.37 Performance results for the proposed DPWM based three-level inverter with change in torque from 6.0 to 24.0 N.m., while the speed was kept constant at 500.0 rpm.; (a) Machine speed; (b) Phase voltage; (c) Difference between two DC-link capacitor voltages; (d) Stator current.

Fig. 4.34 shows the machine performance with the DC-offset based DPWM scheme for three-level inverter, during change in machine speed from 150.0 rpm to 800.0 rpm, while load torque was kept constant at 6.0 N.m. and fig. 4.35 shows the change in load torque from 6.0 N.m. to 24 N.m., while speed kept constant at 500.0 rpm. In Both the conditions capacitor voltage deviation is as high as 20.0 V, which in turn introduces current and voltage harmonic distortion, as already shown in Figs. 4.32 (a) and 4.33 (a, b).

Figs. 4.36 and 4.37 show the simulation results with the proposed DPWM based control strategy during change is speed from 150.0 rpm to 800.0 rpm at 6.0 N.m. of load torque and while load torque was changed from 6.0 N.m. to 24 N.m. at 500.0 rpm machine speed. With change in speed, the maximum capacitor voltage difference goes to 2.0 V, which is 0.7% of the total DC-link capacitor voltage and during change in torque; maximum capacitor voltage difference goes to 5.0 V, which is 1.85% of the total DC-link capacitor voltage.

Hence, from both speed and torque responses, it can be concluded that with the proposed DPWM control strategy, the machine was able to perform the required performance and kept the NPP below 5% of the total DC link capacitor voltage compared to the earlier proposed scheme.

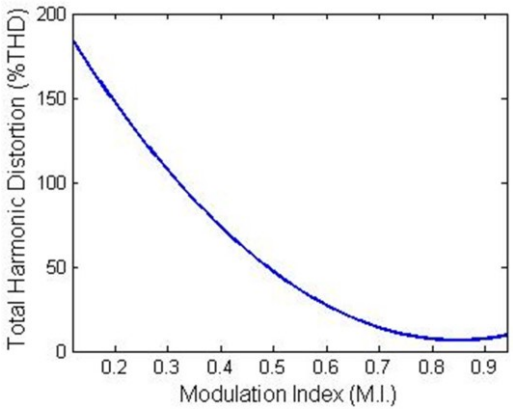


Figure 4.38 Simulation results for total voltage harmonic distortion for DPWM scheme.

Fig. 4.38 shows the simulation results for the harmonic distortion during change in modulation index. Results show a uniform reduction in the harmonic distortion at higher modulation indices.

4.4.5. Experimental Results for DPWM Scheme

Fig. 4.39 shows the duty ratios with low (0.23) and high modulation indexes (0.87). Results are quite similar to the simulation results.

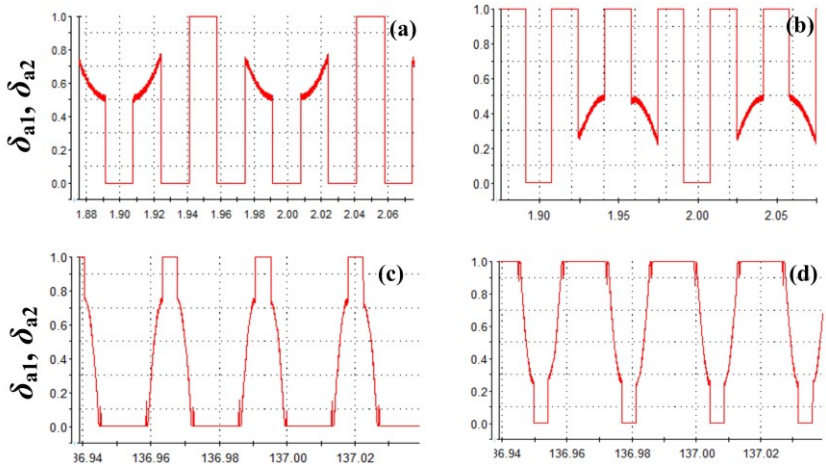


Figure 4.39 Experimental results for the duty ratios with proposed DPWM strategy and with modulation index of; (a, b) 0.23. (c, d) 0.87.

Fig. 4.40 shows the phase voltages with both the control strategies with modulation index (M.I.) of 0.46. Compared to the simulation results, the voltage harmonic distortions are high with the conventional strategy (Fig. 4.40, a). The reason behind is that, in real experimental setup the effects of the capacitor voltage deviation changes the generated phase voltages, which in turn influences the machine speed. As an effect, machine speed keeps on oscillation around its steady state value, which introduces further transients in the system. It also makes the phase current drown from the source distorted, as shown in Fig. 4.41 (a, b). However, with the proposed DPWM control strategy, in the phase voltage (Fig. 4.40, b) and current waveforms (Fig. 4.41, c, d) these types of transients cannot be observed.

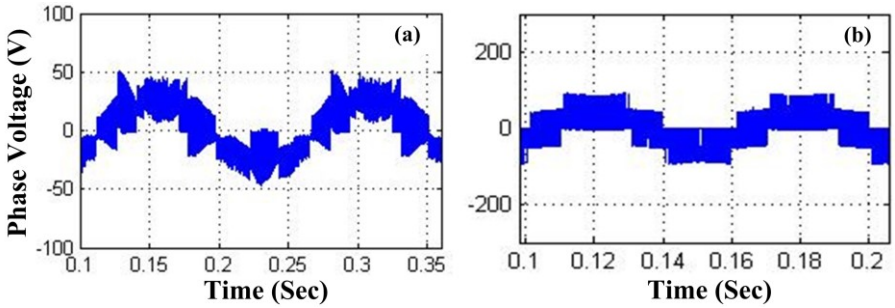


Figure 4.40 Experimental results for the phase current and total harmonic distortion analysis for DPWM based control strategy.

Fig. 4.42 shows the experimental results with the conventional DC-offset based strategy, while machine speed was kept constant at 200.0 rpm and DC-link voltage at 100.0 V. Due to the enormous fluctuation at the two capacitor voltages, the DC-link voltage was kept low as compared to the simulation studies. It is clear from the results that, with this type of control strategy, machine was not able to attain the steady state speed, which intern introduces additional voltage and current harmonic distortions.

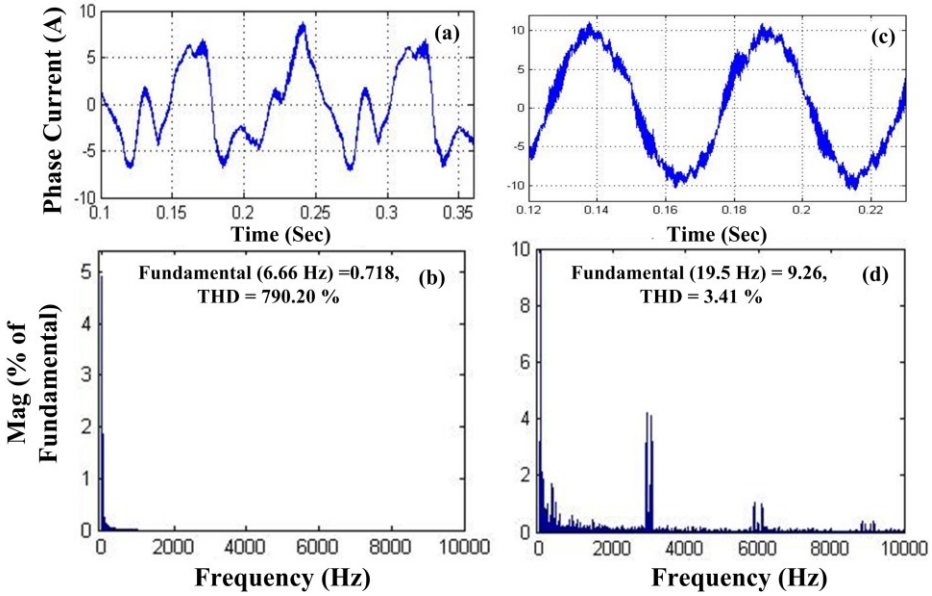


Figure 4.41 Experimental results for the harmonic distortion comparison between the two control strategies.

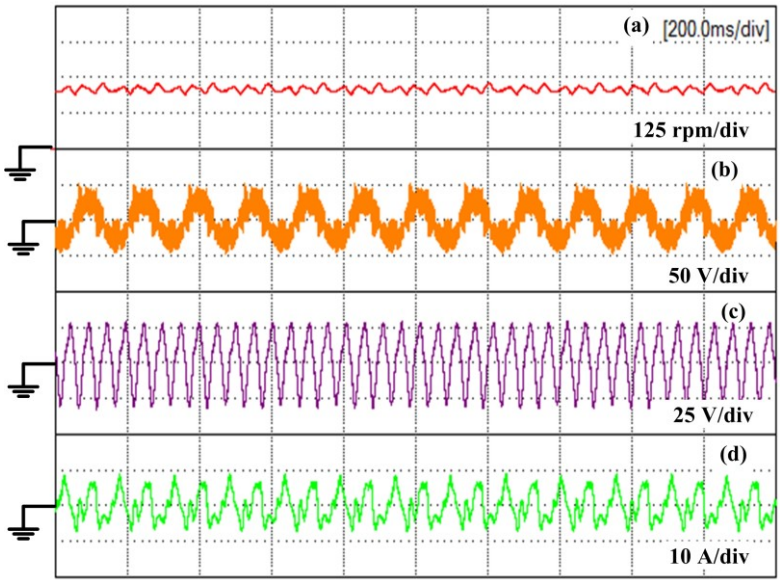


Figure 4.42 Experimental results with conventional DC-offset based control strategy with 200.0 rpm machine speed and at no load condition; (a) Machine speed; (b) Phase voltage; (c) Difference in two capacitor voltages; (d) Stator current.

Fig. 4.43 shows the experimental results with a change in machine speed from 150.0 rpm to 800.0 rpm, while load torque was kept constant at 6.0 N.m., and Fig. 4.44 shows the results while load torque was changed from 6.0 N.m. to 24.0 N.m. with 500.0 rpm machine speed. The DC-link voltage was kept constant at 270.0 V. The maximum capacitor voltage deviation during speed change is around 3.0 V and during change in load torque it is around 12.0 V at rated load condition. Hence compared to the conventional strategy, the proposed strategy provides a considerable reduction in the capacitor voltage deviation and also reduced the

current and voltage harmonic distortion even at rated load torque condition and at speed and torque transients.

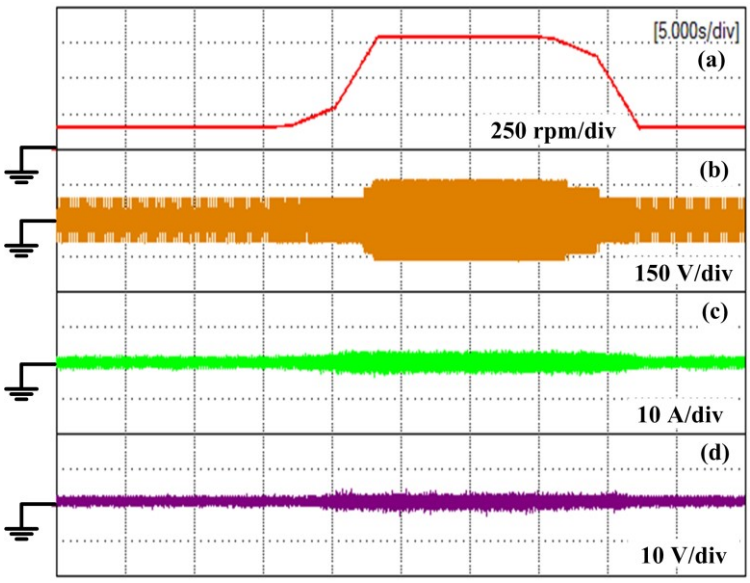


Figure 4.43 Experimental results for change in speed for the proposed DPWM based strategy from 150.0 rpm to 800.0 rpm at 6.0 N.m. of load torque; (a) Machine speed; (b) Phase voltage; (c) Stator current; (d) Difference in two capacitor voltages.

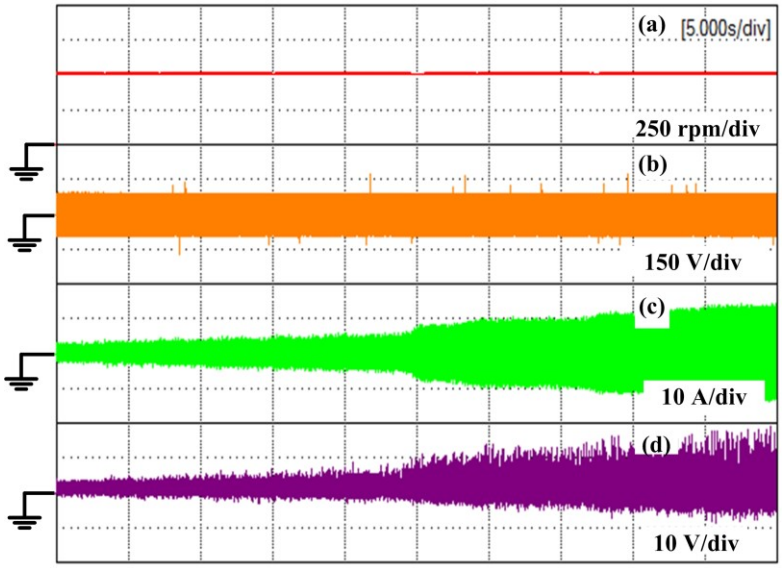


Figure 4.44 Experimental results for change in torque for the proposed DPWM based strategy from 4.0 to 24.0 N.m. while speed kept constant at 500.0 rpm; (a) Machine speed; (b) Phase voltage; (c) Stator current; (d) Difference in two capacitor voltages.

Fig. 4.45 shows the experimental results for the DPWM harmonic distortion with change in modulation index. Harmonic distortion follows almost the same trend as like the simulation results.

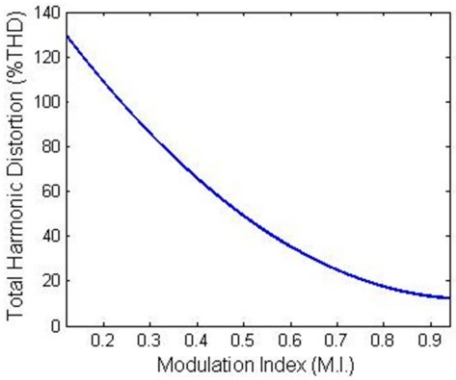


Figure 4.45 Experimental results for total voltage harmonic distortion for DPWM scheme.

4.5. Summary of Chapter 4

This chapter presents three carrier based PWM control strategies. The performances of these strategies are then compared with the SVPWM based strategy. Results show that the proposed strategy works well for wider range of machine torque-speed variation and keeps the neutral point potential (NPP) at the required tolerance label. Moreover, the proposed hybrid PWM based strategy for DPWM is compared with the conventional DPWM scheme. Simulation and experimental results shows a considerable amount of reduction in harmonic distortion with the proposed scheme. Furthermore, the proposed DPWM strategy keeps the neutral point potential balanced at all operating points.

Chapter 5. Performance Comparison Studies Between Various Proposed Control Strategies

In this chapter initially a detailed analytic calculation of the switching and conduction loss distribution of different IGBT and their anti-parallel diodes will be carried out, with change in modulation indices for both two- and three-level inverters. Then simulation studies will be carried out with different proposed PWM strategies, to show their effects on loss distribution. Moreover, average torque ripple, average neutral point potential (NPP) variation, total voltage, current harmonic distortions and total program execution times will also be compared. For all these analysis a 54.0 kW surface PMSM will be considered.

5.1. Analytical Switching Loss Calculation of Two-Level Inverter

Fig. 5.1 shows the duty cycle (δ_a) and phase current (i_a) for the two-level inverter phase A. As can be seen from the figure, the current lags phase voltage duty by an angle of $\varphi°$. Hence, the conduction and switching periods of the IGBT switches and their anti-parallel can be distributed in to four regions as A, B, C, D.

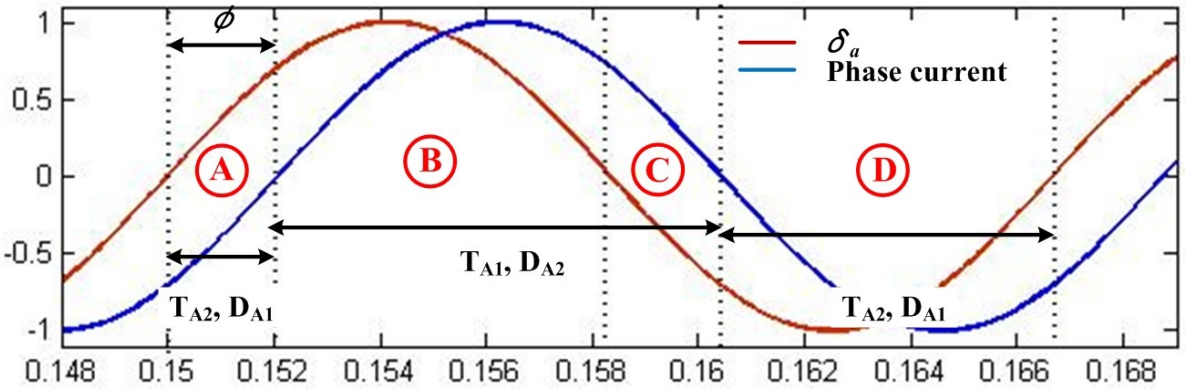


Figure 5.1 Duty cycle and phase current for the Two-level inverter phase A.

As shown in Fig. 5.1 region A, where phase current is negative and duty is positive, state I and IV as shown in Fig. 5.2 will be applicable. Here, the anti-parallel diode D_{A1}, will allow the current to pass when T_{A1} will be turned on and T_{A2} will allow the current to flow when it will be turned on. In region B, where both the duty and current are positive, state II, III will be applicable. IGBT T_{A1} will carry the load current when it is turned on and anti-parallel diode D_{A2}, will carry the positive load current otherwise. In region C, load current is still positive, but duty is negative, so state II, III will also be applicable. In region D both the duty and current are negative. So IGBT T_{A2}, will carry the load current when it is on (state IV) and diode D_{A1} will be conducted when T_{A2} is off (state I).

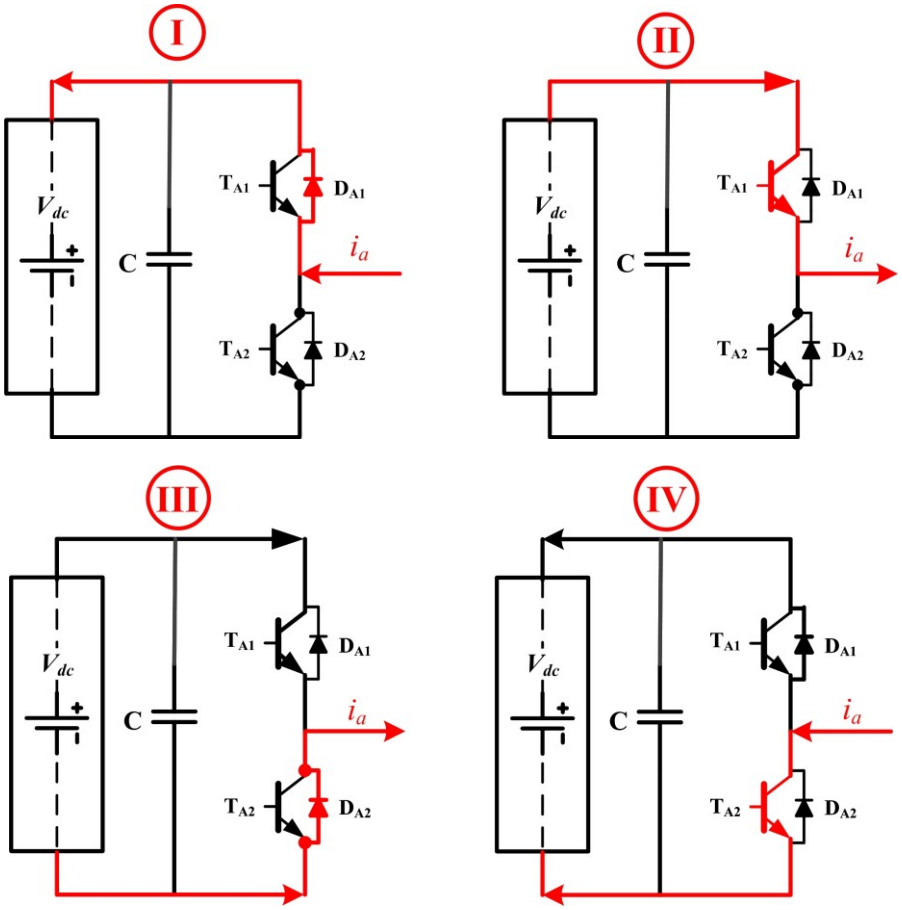


Figure 5.2 Current direction for two-level inverter for all four regions.

Here, it can be observed that at low power factor and modulation indices, anti-parallel diodes conduct more load current than the active switches.

5.1.1. Conduction Loss Calculation

For switching and conduction loss calculation Infineon FS400R12A2T4, 1200.0 V IGBT module is considered for the two-level inverter. Conduction loss (P_c) in power switches and diodes are the product of saturation voltage (v_{ce}) at a particular load current and the load current (i) itself, as shown in eq. (5.1). The average conduction loss (P_{c_avg}) for one fundamental power cycle can be represented by eq. (5.2).

$$P_C(t) = v_{ce}(t) \cdot i(t) \tag{5.1}$$

$$p_{c\_avg} = \left(\frac{1}{2\pi}\right) \int_{\varphi}^{\pi+\varphi} (M \cdot v_{ce} \cdot i)\, d\alpha \tag{5.2}$$

Where, $M = 0.5 \cdot \{1 + m \cdot \sin(\alpha)\}$, $i = I_m \cdot \sin(\alpha - \varphi)$, m is the modulation index, I_m is the maximum phase peak current, and $\alpha = \omega.t$.

As shown in Fig. 5.1, the conduction losses for IGBT T_{A1}, T_{A2} can be expressed as shown in eq. (5.3), and (5.4).

$$p_{c\_avg\_TA\_1} = \left(\frac{1}{2\pi}\right)\int_{\varphi}^{\pi+\varphi} (M \cdot v_{ceT} \cdot i)\, d\alpha$$

$$p_{c\_avg\_TA\_1} = (V_{ceT} \cdot I_m) \cdot \left\{\frac{1}{2\pi} + \frac{0.7853}{2\pi} \cdot m \cdot \cos(\varphi)\right\} \tag{5.3}$$

$$p_{c\_avg\_TA\_2} = \left(\frac{1}{2\pi}\right)\int_{\pi+\varphi}^{2\pi+\varphi} \{(1-M) \cdot v_{ceT} \cdot i\}\, d\alpha$$

$$p_{c\_avg\_TA\_2} = (V_{ceT} \cdot I_m) \cdot \left\{\frac{1}{2\pi} + \frac{0.7853}{2\pi} \cdot m \cdot \cos(\varphi)\right\} \tag{5.4}$$

Similarly, conduction losses for anti-parallel diodes can be expressed as shown in eq. (5.5), (5.6). As diodes conducts only when the power switches are turned off, to calculate the conduction loss (1-M) has to be used instead of M.

$$p_{c\_avg\_DA\_1} = \left(\frac{1}{2\pi}\right)\int_{\pi+\varphi}^{2\pi+\varphi} \{M \cdot v_{ceD} \cdot i\}\, d\alpha$$

$$p_{c\_avg\_DA\_1} = (V_{ceD} \cdot I_m) \cdot \left\{\frac{1}{2\pi} - \frac{0.7853}{2\pi} \cdot m \cdot \cos(\varphi)\right\} \tag{5.5}$$

$$p_{c\_avg\_DA\_2} = \left(\frac{1}{2\pi}\right)\int_{\varphi}^{\pi+\varphi} \{(1-M) \cdot v_{ceD} \cdot i\}\, d\alpha$$

$$p_{c\_avg\_DA\_2} = (V_{ceD} \cdot I_m) \cdot \left\{\frac{1}{2\pi} - \frac{0.7853}{2\pi} \cdot m \cdot \cos(\varphi)\right\} \tag{5.6}$$

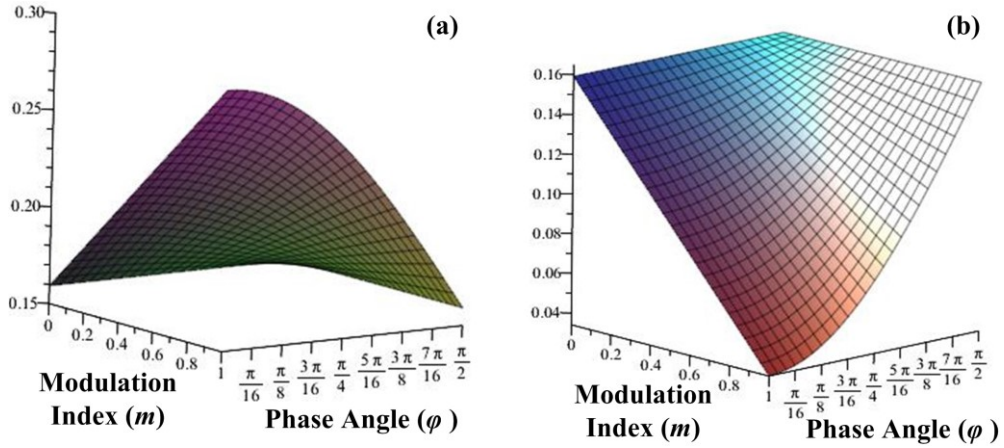


Figure 5.3 Conduction loss distribution for (a) IGBT and (b) their anti-parallel diode, with change in modulation index and power factor.

Fig. 5.3 shows the conduction losses (In watt) for both IGBT and their anti-parallel diodes, with change in modulation index and power factor. From the wave shapes it is clear

that, with higher modulation index, conduction losses for IGBT switches are going to increase, as the conduction time is going to increase and the diode conduction losses are going to come down. However, with change in power factor angle, the IGBT losses are going to come down as their conduction time will reduce and the diode losses are going to increase. For this study V_{ce} for both IGBT and diodes are set at 1.0 V and peak phase current is considered as unity.

5.1.2. Switching Loss Calculation

Switching losses in any device is a function of load current and the voltage across those power devices. In IGBT there are basically two kinds of switching losses can be observed; turn on (E_{on}) and turn off (E_{off}) losses. Both of them are generally provided by the device manufacturer. However, for diodes there is only reverse recovery losses (E_{rr}), that are present during turn off. Hence, average switching loss can be represented by eq. (5.7), and (5.8).

$$p_{\text{sw\_avg\_IGBT}} = \left(\frac{1}{2\pi}\right)\int_{\varphi}^{\pi+\varphi}\{(E_{\text{on}} + E_{\text{Off}})\cdot\left(\frac{V_{ce}}{V_{nom}}\right)\cdot f_{sw}\}\,\mathrm{d}\alpha \tag{5.7}$$

$$p_{\text{sw\_avg\_diode}} = \left(\frac{1}{2\pi}\right)\int_{\varphi}^{\pi+\varphi}\{E_{\text{rr}}\cdot\left(\frac{V_{ce}}{V_{nom}}\right)\cdot f_{sw}\}\,\mathrm{d}\alpha \tag{5.8}$$

From the IGBT data sheet using quadratic interpolation, the total switching loss ($E = E_{on} + E_{off}$)), can be expressed as shown in eq. (5.9). Similarly, diode losses (E_{rr}) can also be expressed as a function of load current [$i(t)$], as shown in eq. (5.10).

$$E_{IGBT} = -2\cdot e^{-7}\cdot i^2 + 2\cdot e^{-4}\cdot i + 4\cdot e^{-4} \tag{5.9}$$

$$E_{diode} = -9\cdot e^{-8}\cdot i^2 + 8\cdot e^{-5}\cdot i + 6\cdot e^{-3} \tag{5.10}$$

Hence, replacing the values of switching losses from eq. (5.9) and (5.10) into eq. (5.7) and (5.8) following expression can be derived.

$$P_{sw\_avg\_IGBT} = \frac{1}{2\pi}(-3.141\cdot e^{-7}\cdot {I_m}^2 + 4\cdot e^{-4}\cdot I_m + 0.00125)\cdot\left(\frac{V_{ce}}{V_{nom}}\right)\cdot f_{sw} \tag{5.11}$$

$$P_{sw\_avg\_diode} = \frac{1}{2\pi}(-1.413\cdot e^{-7}\cdot {I_m}^2 + 1.6\cdot e^{-4}\cdot I_m + 0.0188)\cdot\left(\frac{V_{ce}}{V_{nom}}\right)\cdot f_{sw} \tag{5.12}$$

Here, V_{ce} is the actual voltage applied across the device, V_{nom} is the nominal voltage in the datasheet for total IGBT loss calculation, and f_{sw} is the switching frequency. Hence, with higher switching frequencies these losses goes higher, and it does not depends on the modulation index.

5.2. Analytical Switching Loss Calculation of Three-Level Inverter

Fig. 5.4 shows the duty cycles for four power switches and the A phase current for tree-level inverter. Instead of one modulation signal for two-level inverter, it has two modulating signals. δ_{ap} is for T_{A1} and δ_{an} is for T_{A2}. T_{A3} and T_{A4} are complement to T_{A1} and T_{A2}. Like fig. 5.1, fig.5.4 can also be divided into four regions.

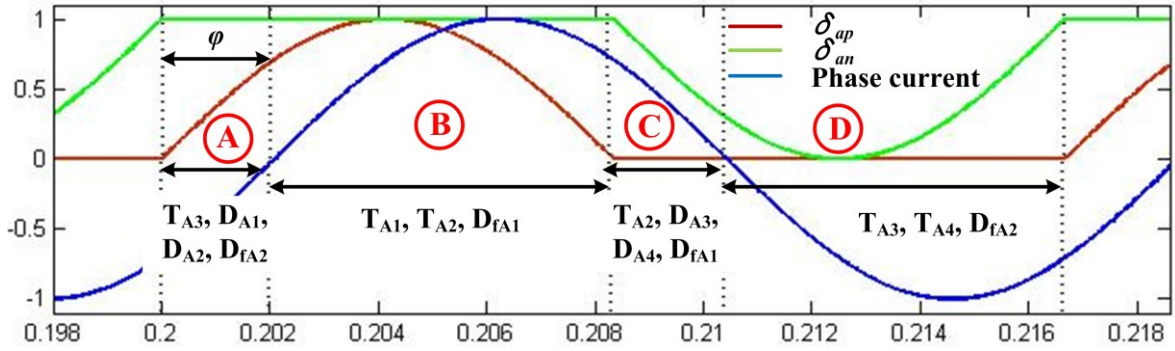


Figure 5.4 Duty cycle and phase current for the Three-level inverter phase A.

In region A, δ_{an} is clamped to one, so T_{A2} will always be on. Hence, when T_{A1} will be turned on, current will flow according to state I in fig. 5.5, through the anti-parallel diodes D_{A1}, D_{A2} and when T_{A1} is off, current will flow according to state II, through T_{A3} and D_{fA2}.

In region B, duties are similar like region A, however, current is positive. Hence, when switch T_{A1} is turned on, current flows through T_{A1}, T_{A2} as shown in state III, and when T_{A1} is turned off, current flows through D_{fA1} and T_{A2}, as shown in state IV.

In state C, δ_{ap} goes down to zero, which makes T_{A1} to switch off all the time and T_{A2} starts switching. As current is positive, when T_{A2} is on, current flows through D_{fA1} and T_{A2} as shown in state IV, and when it is off, current flows through the anti-parallel diodes D_{A3} and D_{A4}, as shown in state V.

Like region C, in region D duties remain same, but current goes negative. Hence, when T_{A2} is on, current flows through T_{A3} and D_{fA2} like shown in state II, and when T_{A2} is turned off, current flows through T_{A3}, T_{A4} as shown in state VI.

Compared to the two-level inverter in three-level inverter, it can be observed that, the conduction time for the anti-parallel diodes have reduced drastically. This is basically due to the power shared by the neutral point clamped diodes, which starts conducting, whenever, the power switches are turned off.

As the basic expression for conduction and switching loss calculation will remain the same like in the two-level inverter, as shown in eq. (5.2), (5.7) and (5.8), the three-level inverter power switches will be calculated directly.

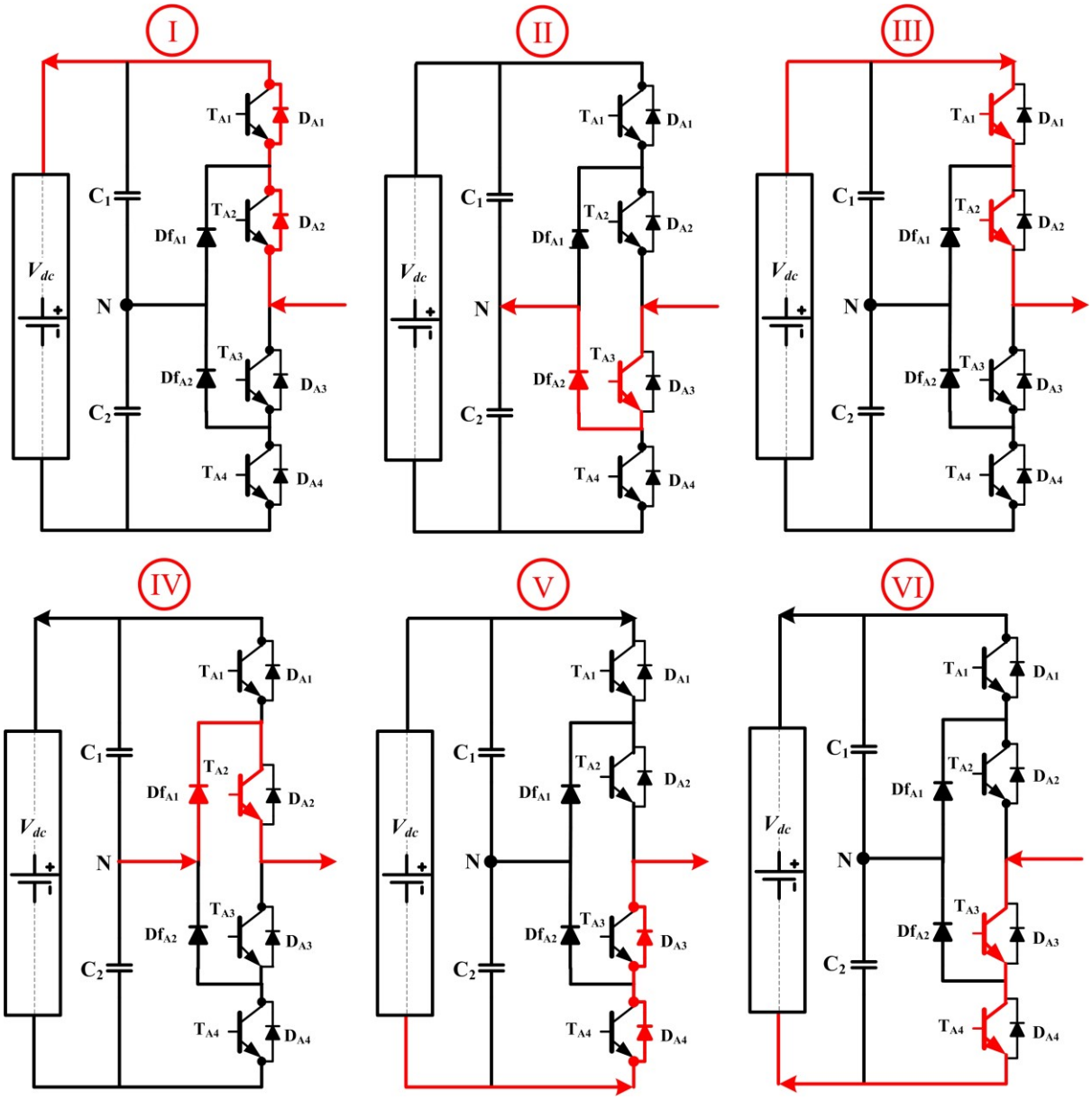


Figure 5.5 Current direction for three-level inverter for all four regions.

5.2.1. Conduction Loss Calculation

For three-level inverter loss calculation Infineon F3L300R07PE4, 650.0 V NPC modules are used. The conduction losses for IGBT T_{A1}, T_{A2}, T_{A3}, T_{A4}, D_{fA1} and D_{fA2} can be expressed as follows.

$$p_{c\_avg\_TA\_1} = \left(\frac{V_{ceT}}{2\pi}\right)\int_{\varphi}^{\pi}(m\cdot\sin(\alpha)\cdot i)\,d\alpha$$

$$p_{c\_avg\_TA\_1} = \left(\frac{V_{ceT}\cdot I_m\cdot m}{4\pi}\right)\cdot\{(\pi-\varphi)\cdot\cos(\varphi)+\sin(\varphi)\} \tag{5.13}$$

$$p_{c\_avg\_TA\_2} = \left(\frac{V_{ceT}}{2\pi}\right)\left(\int_{\varphi}^{\pi}(i\cdot 1)\,d\alpha + \int_{\pi}^{\pi+\varphi}(i\cdot(1+m\cdot\sin(\alpha)))\,d\alpha\right)$$

$$p_{c\_avg\_TA\_2} = (\frac{V_{ceT} \cdot I_m}{\pi}) + \{\frac{V_{ceT} \cdot I_m \cdot m}{4\pi}(\varphi \cdot \cos(\varphi) - \sin(\varphi))\} \tag{5.14}$$

$$p_{c\_avg\_TA\_3} = -(\frac{V_{ceT}}{2\pi})(\int_{\varphi+\pi}^{2\pi}(i \cdot 1)\,d\alpha + \int_{0}^{\varphi}(i \cdot (1 - m \cdot \sin(\alpha)))\,d\alpha$$

$$p_{c\_avg\_TA\_3} = (\frac{V_{ceT} \cdot I_m}{\pi}) + \{\frac{V_{ceT} \cdot I_m \cdot m}{4\pi}(\varphi \cdot \cos(\varphi) - \sin(\varphi))\} \tag{5.15}$$

$$p_{c\_avg\_TA\_4} = -(\frac{V_{ceT}}{2\pi})\int_{\varphi+\pi}^{2\pi}(i \cdot (1 - (1 + m \cdot \sin(\alpha))))\,d\alpha$$

$$p_{c\_avg\_TA\_4} = (\frac{V_{ceT} \cdot I_m \cdot m}{4\pi}) \cdot \{(\pi - \varphi) \cdot \cos(\varphi) + \sin(\varphi)\} \tag{5.16}$$

$$p_{c\_avg\_DfA\_1} = (\frac{V_{ceT}}{2\pi})(\int_{\varphi}^{\pi}(i \cdot (1 - m \cdot \sin(\alpha)))\,d\alpha + \int_{\pi}^{\pi+\varphi}(i \cdot (1 + m \cdot \sin(\alpha)))\,d\alpha$$

$$p_{c\_avg\_DfA\_1} = (\frac{V_{ceT} \cdot I_m \cdot m}{4\pi}) \cdot \{4 + m \cdot ((2\varphi - \pi) \cdot \cos(\varphi) - 2\sin(\varphi)\} \tag{5.17}$$

$$p_{c\_avg\_DfA\_2} = -(\frac{V_{ceT}}{2\pi})(\int_{\varphi}^{\pi}(i \cdot (1 - m \cdot \sin(\alpha)))\,d\alpha + \int_{\pi+\varphi}^{2\pi}(i \cdot (1 + m \cdot \sin(\alpha)))\,d\alpha$$

$$p_{c\_avg\_DfA\_2} = (\frac{V_{ceT} \cdot I_m \cdot m}{4\pi}) \cdot \{4 + m \cdot ((2\varphi - \pi) \cdot \cos(\varphi) - 2\sin(\varphi)\} \tag{5.18}$$

In all these equations values of *m* are directly obtained from Fig. 5.4. Similarly, anti-parallel diodes conduction losses can be obtained as follows.

$$p_{c\_avg\_DA\_1} / p_{c\_avg\_DA\_2} = -(\frac{V_{ceD}}{2\pi})\int_{0}^{\varphi}(i \cdot m \cdot \sin(\alpha))\,d\alpha$$

$$p_{c\_avg\_DA\_1} / p_{c\_avg\_DA\_2} = (\frac{V_{ceD} \cdot I_m \cdot m}{4\pi}) \cdot \{\sin(\varphi) - \varphi \cdot \cos(\varphi)\} \tag{5.19}$$

$$p_{c\_avg\_DA\_3} / p_{c\_avg\_DA\_4} = (\frac{V_{ceD}}{2\pi})\int_{\pi}^{\pi+\varphi}(i \cdot (1 - (1 + m \cdot \sin(\alpha))))\,d\alpha$$

$$p_{c\_avg\_DA\_3} / p_{c\_avg\_DA\_4} = (\frac{V_{ceD} \cdot I_m \cdot m}{4\pi}) \cdot \{\sin(\varphi) - \varphi \cdot \cos(\varphi)\} \tag{5.20}$$

Fig. 5.6 shows the conduction loss distribution for all the power switches and the diodes. It can be observed that at high power factor, which is the case for permanent magnet machines, the conduction loss for the inner two IGBT switches T_{A2}, T_{A3} are higher than the outer most ones (T_{A1}, T_{A4}). Moreover, the conduction losses for the anti-parallel diodes are very low, as most of the power is shared by the NPC diodes (D_{fA1}, D_{fA2}), when outer IGBT switches are turned off. With an increase in modulation index the active IGBT switches (T_{A1}, T_{A4}) takes more share of the load current, which makes their conduction losses to increase and the conduction losses for the NPC diodes goes down.

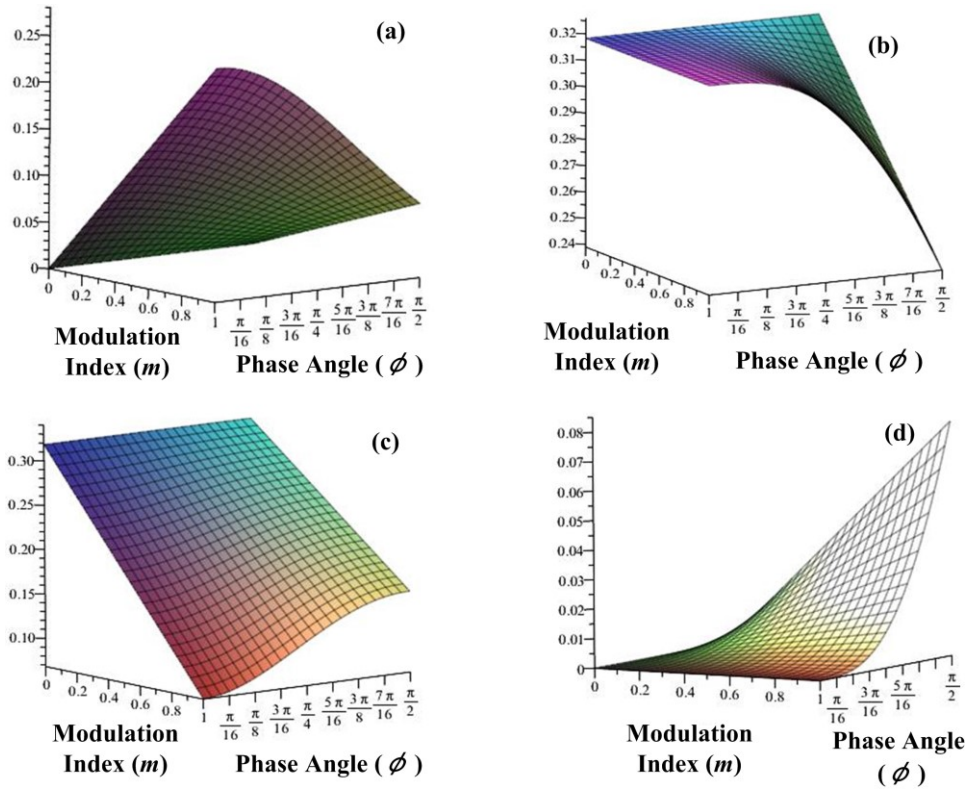


Figure 5.6 Conduction loss distribution for IGBT (a) T_{A1}, T_{A4}, (b) T_{A2}, $T_{A3,}$ (c) NPC diode D_{fA1}, D_{Fa2} and (d) anti-parallel diode with change in modulation index and power factor.

In comparison to the conduction losses for two-level inverter switches, shown in Fig. 5.3, the loss distributions between different power switches are not symmetrical in three-level inverter. This will overheat some of the switches than the other.

5.2.2. Switching Loss Calculation

Analytic formulation for the switching loss is already shown in eq. (5.7) and (5.8). The quadratic interpolation for the IGBT, anti-parallel diodes and the NPC diode switching losses calculated from the device data sheet are shown below,

$$E_{IGBT} = -1 \cdot e^{-8} \cdot i^2 + 6 \cdot e^{-5} \cdot i + 31 \cdot e^{-4} \tag{5.21}$$

$$E_{diode} = -3 \cdot e^{-8} \cdot i^2 + 3 \cdot e^{-5} \cdot i + 11 \cdot e^{-4} \tag{5.22}$$

Here, it can be noted that, the losses for the anti-parallel diodes and the NPC diodes are similar, which is shown in eq. (5.10). The switching losses for all the switches are shown below.

$$p_{sw\_avg\_TA\_1} = \left(\frac{V_{ce}}{V_{nom}}\right) \cdot f_{sw} \cdot \left(\frac{1}{2\pi}\right) \int_{\varphi}^{\pi} (E_{IGBT})\, d\alpha$$

$$p_{sw\_avg\_TA\_1} = \frac{1}{2\pi}\{I_m{}^2 \cdot (5e^{-9}\varphi - 1.57e^{-8} - 25e^{-10} \cdot \sin(2\varphi)) \quad (5.23)$$
$$+ 6e^{-5} \cdot I_m (1 + \cos(\varphi)) - 31e^{-4} \cdot \varphi + 0.00973\} \cdot (\frac{V_{ce}}{V_{nom}}) \cdot f_{sw}$$

$$p_{sw\_avg\_TA\_2} = (\frac{V_{ce}}{V_{nom}}) \cdot f_{sw} \cdot (\frac{1}{2\pi}) \int_{\pi}^{\pi+\varphi} (E_{IGBT})\, d\alpha$$

$$p_{sw\_avg\_TA\_2} = \frac{1}{2\pi}\{I_m{}^2 \cdot (25e^{-10} \cdot \sin(2\varphi) - 5e^{-9}\varphi) + 6e^{-5} \cdot I_m (1 - \cos(\varphi)) \quad (5.24)$$
$$+ 31e^{-4} \cdot \varphi\} \cdot (\frac{V_{ce}}{V_{nom}}) \cdot f_{sw}$$

$$p_{sw\_avg\_TA\_3} = (\frac{V_{ce}}{V_{nom}}) \cdot f_{sw} \cdot (\frac{1}{2\pi}) \int_{0}^{\pi} (E_{IGBT})\, d\alpha$$

$$p_{sw\_avg\_TA\_3} = \frac{1}{2\pi}\{I_m{}^2 \cdot (25e^{-10} \cdot \sin(2\varphi) - 5e^{-9}\varphi) - 6e^{-5} \cdot I_m (1 - \cos(\varphi)) \quad (5.25)$$
$$+ 31e^{-4} \cdot \varphi\} \cdot (\frac{V_{ce}}{V_{nom}}) \cdot f_{sw}$$

$$p_{sw\_avg\_TA\_4} = (\frac{V_{ce}}{V_{nom}}) \cdot f_{sw} \cdot (\frac{1}{2\pi}) \int_{\pi+\varphi}^{2\pi} (E_{IGBT})\, d\alpha$$

$$p_{sw\_avg\_TA\_4} = \frac{1}{2\pi}\{I_m{}^2 \cdot (5e^{-9}\varphi - 1.57e^{-8} - 25e^{-10} \cdot \sin(2\varphi)) \quad (5.26)$$
$$+ 6e^{-5} \cdot I_m (1 + \cos(\varphi)) - 31e^{-4} \cdot \varphi + 0.00973\} \cdot (\frac{V_{ce}}{V_{nom}}) \cdot f_{sw}$$

$$p_{sw\_avg\_dA\_1} / p_{sw\_avg\_dA\_2} = (\frac{V_{ce}}{V_{nom}}) \cdot f_{sw} \cdot (\frac{1}{2\pi}) \int_{\varphi}^{\pi} (E_{diode})\, d\alpha$$

$$p_{sw\_avg\_dA\_1} / p_{sw\_avg\_dA\_2} = \frac{1}{2\pi}\{I_m{}^2 \cdot (75e^{-10} \cdot \sin(2\varphi) - 15e^{-9}\varphi) \quad (5.27)$$
$$+ 3e^{-5} \cdot I_m (\cos(\varphi) - 1) + 11e^{-4} \cdot \varphi\} \cdot (\frac{V_{ce}}{V_{nom}}) \cdot f_{sw}$$

$$p_{sw\_avg\_dA\_3} / p_{sw\_avg\_dA\_4} = (\frac{V_{ce}}{V_{nom}}) \cdot f_{sw} \cdot (\frac{1}{2\pi}) \int_{\pi+\varphi}^{2\pi} (E_{diode})\, d\alpha$$

$$p_{sw\_avg\_dA\_3} / p_{sw\_avg\_dA\_4} = \frac{1}{2\pi}\{I_m{}^2 \cdot (75e^{-10} \cdot \sin(2\varphi) - 15e^{-9}\varphi) \quad (5.28)$$
$$+ 3e^{-5} \cdot I_m (\cos(\varphi) - 1) + 11e^{-4} \cdot \varphi\} \cdot (\frac{V_{ce}}{V_{nom}}) \cdot f_{sw}$$

$$p_{sw\_avg\_DfdA\_1} = (\frac{V_{ce}}{V_{nom}}) \cdot f_{sw} \cdot (\frac{1}{2\pi}) \int_{\varphi}^{\pi+\varphi} (E_{diode}) \, d\alpha$$

$$p_{sw\_avg\_DfA\_1} = \frac{1}{2\pi} \{6e^{-5} \cdot I_m - 4.71e^{-8} I_m^{\,2} + 0.0034\} \cdot (\frac{V_{ce}}{V_{nom}}) \cdot f_{sw} \quad (5.29)$$

$$p_{sw\_avg\_DfdA\_2} = (\frac{V_{ce}}{V_{nom}}) \cdot f_{sw} \cdot (\frac{1}{2\pi}) \int_{\pi+\varphi}^{2\pi} (E_{diode}) \, d\alpha$$

$$p_{sw\_avg\_DfA\_2} = \frac{1}{2\pi} \{6e^{-5} \cdot I_m - 4.71e^{-8} I_m^{\,2} + 0.0034\} \cdot (\frac{V_{ce}}{V_{nom}}) \cdot f_{sw} \quad (5.30)$$

From the derived switching loss expressions it can be seen that, switching losses for IGBT T_{A1}, T_{A4} are similar, T_{A2}, T_{A3} are almost similar, all anti-parallel diodes have similar losses and the two NPC diodes also have similar switching losses as well.

5.3. Simulation Based Loss calculation for Two-Level Inverter with SV-PWM Schemes

To perform the loss calculation, simulation studies are carried out in Matlab/ Simulink® platform with PLECS simulation software. A 54.0 kW surface PMSM is considered and it is loaded with 70.0 N.m. load torque. The switching frequency was kept constant at 10.0 kHz and the DC-link voltage was at 600.0 V and two capacitors are 500.0 µF each. The RMS phase voltage and current was observed as 172.5 V and 77.78 A. It gives a power factor of around 0.78, power factor angle of (φ) 38.73°.

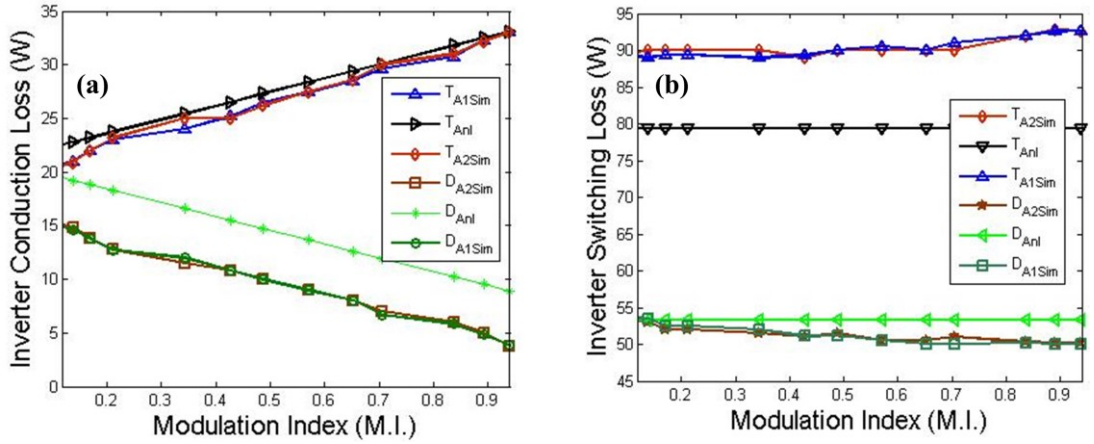


Figure 5.7 (a) Conduction and (b) Switching loss distribution in different IGBT and the anti-parallel diodes with simulation and analytical calculation.

Fig. 5.7 shows the simulation and analytically derived conduction and switching losses for 2-level inverter. Analytically derived losses are quite similar to the simulation studies and follow the same trend. However, in analytically derived losses, effects of current ripple, variation in V_{ce} with load current was not included, which lead to the mismatch in two

results. Compared to the 2-level inverter in 3-level, switching losses are function of load power factor. Hence, with change in load power factor, some of the switches will have more switching losses than the other.

5.4. Simulation Based Loss calculation for Three-Level Inverter

To show the loss profile with the three-level inverter, similar conditions are applied like in the two-level inverter. In case of three-level inverter four proposed control strategies will be compared. As carrier based strategy, uses almost ideal duty ratio compared to the SV-PWM based strategy; firstly we are going to compare the analytically derived losses with the proposed carrier based strategy derived in chapter 4 section 4.1.3.

Fig. 5.8 shows the loss distribution in different power switches with change in modulation index for the proposed carrier based three-level inverter control strategy and then it is compared with the analytically derived losses. Both the results are quite similar. However, the difference between the two results comes because of the capacitor voltage balancing issue which introduce neutral point voltage fluctuation, current ripple, and power factor which are not possible to include in to the analytical equation.

In Fig. 5.8 (a) conduction loss distribution of the four IGBT switches are shown. It can be observed that T_{A2}, T_{A3} conduction losses are constant. The reason for this would be due to their unity modulation index, which leads to the continuous conduction of these devices for each half cycle. However, T_{A1}, T_{A4} conducts only in proportion to the duty ratio, and for this reason the losses increase linearly with modulation index. As the switching for IGBT T_{A2}, T_{A3} shown in Fig. 5.8 (b), occurs when current goes negative to positive or vice versa, only a small amount of switching losses happens due to the lagging power factor as shown in Fig. 5.4 region C, A. As the power factor goes more lagging, it will introduce more switching losses in the inner switches. In normal operation, IGBT T_{A1}, T_{A4} produces more switching losses compared to the inner ones, as they switch with active load current.

Fig. 5.8 (c, d) shows the conduction and switching losses of the antiparallel diodes. These diodes only conducts when the IGBT switches are turned off ideally, as shown in two-level inverter. However, in case of three-level inverter, because of the NPC diodes, they don't share much load current. Hence, it shows very low conduction and switching losses, as shown in the simulation results. Moreover, when the modulation index increases, the reference voltage vector goes to the outmost subsector, which uses mostly the large and medium voltage vector, and allows the flow of current to increase on those diodes. Hence,

from the analytically derived equation and corresponding waveforms, a uniform increase in conduction losses can be seen with the antiparallel diodes.

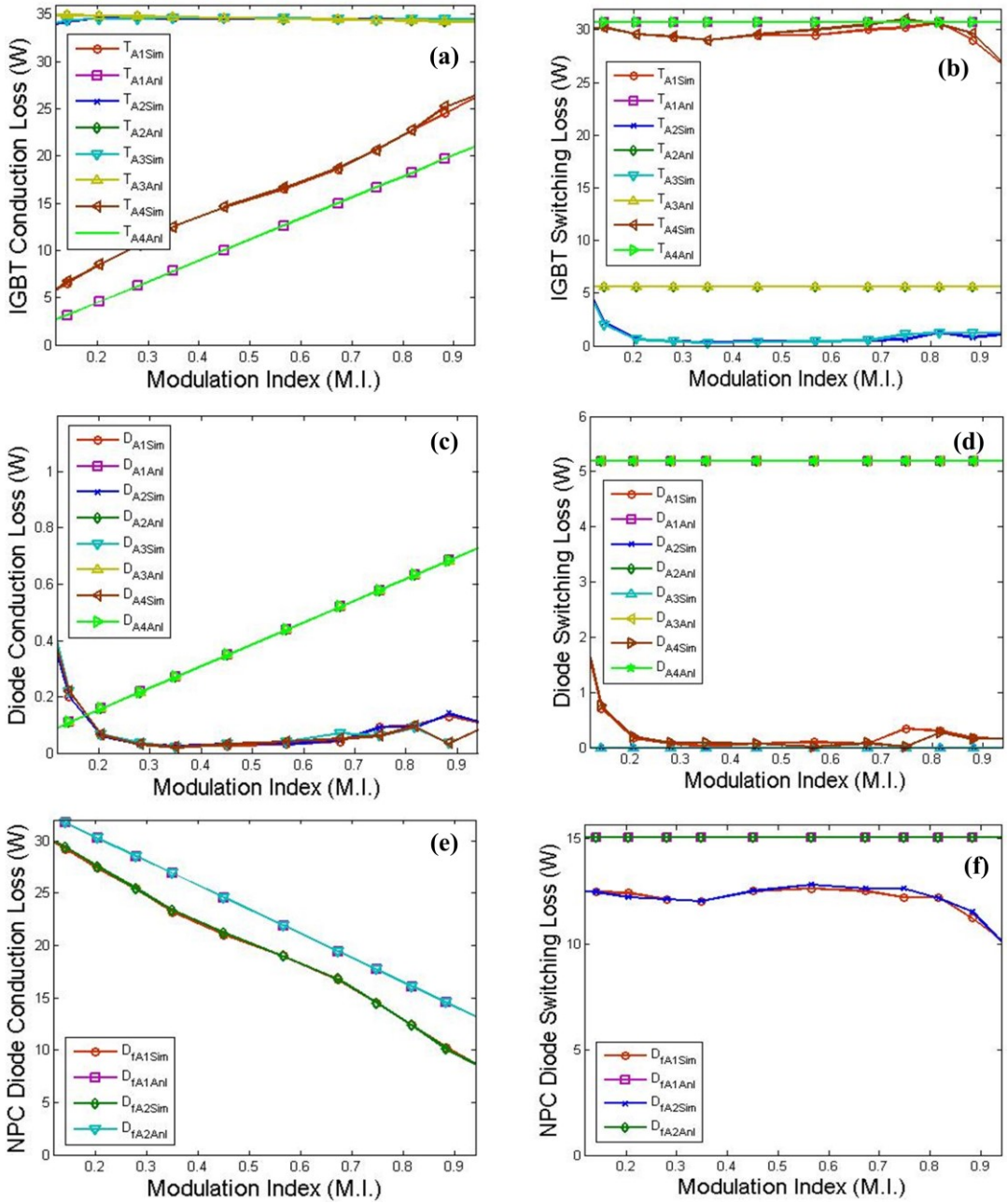


Figure 5.8 Switching and conduction losses for each IGBT and diodes for each leg with carrier based control strategy and analytically derived equations, (a) IGBT conduction loss, (b) IGBT switching loss, (c) IGBT anti parallel diode conduction loss, (d) IGBT anti parallel diode switching loss, (e) NPC diode conduction loss, (f) NPC diode switching loss.

In fig. 5.8 (e, f) conduction and switching losses for the NPC diodes are shown. As already explained in the earlier stage, when IGBT T_{A1}, T_{A4} are turned off, load current passes through the NPC diodes, and it introduces the larger amount of conduction and switching

losses on them. However, as the modulation index increases and IGBT T_{A1}, T_{A4} takes the larger share of the load current; the losses on the NPC diodes reduce.

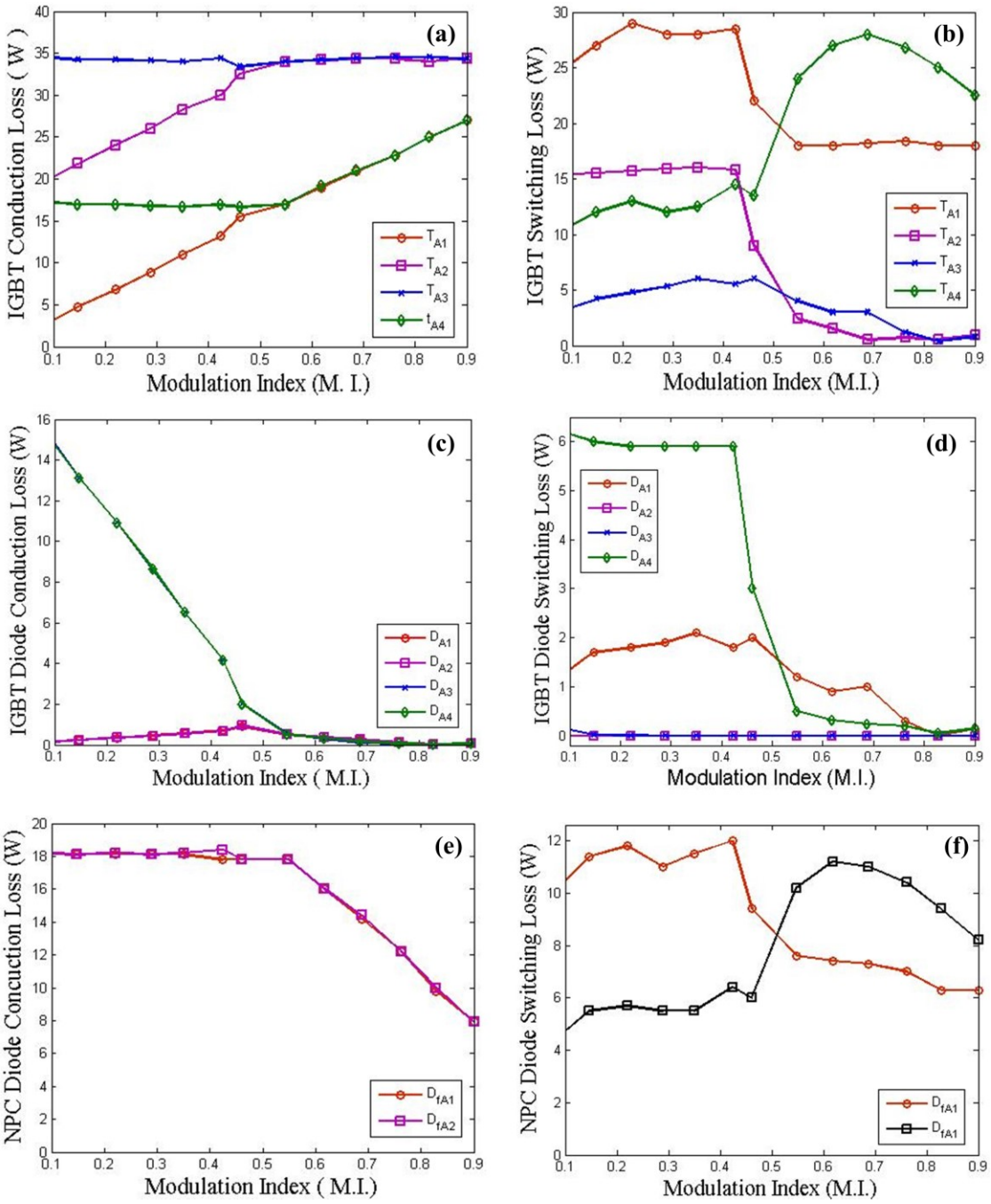


Figure 5.9 Switching and conduction losses for each IGBT and diodes for each leg with SV-PWM based control strategy, (a) IGBT conduction loss, (b) IGBT switching loss, (c) IGBT anti parallel diode conduction loss, (d) IGBT anti parallel diode switching loss, (e) NPC diode conduction loss, (f) NPC diode switching loss.

Fig. 5.9 shows the low distribution with the proposed reduced loss based SVPWM strategy with DC-link voltage balancing. Compared to the earlier shown loss distribution, where a uniform modulation index was generated, in SVPWM strategies based on the two-capacitor state of charge, duties are generated. Hence, losses will not follow as symmetrical

as carrier based strategy. Fig. 5.9 (a, b) shows the conduction and switching loss distribution for IGBT switches. Conduction losses for T_{A1} are linear with the modulation index. Hence the corresponding switching loss is almost constant. Conduction loss for T_{A2} has also increased with modulation index till 0.56, where redundant voltage vectors are dominant and after that it remains constant, as more medium and large vectors are used. Change in conduction loss shows that, T_{A2} was switching to keep the capacitors balanced. Hence corresponding switching losses were also high. However, after 0.56 when the conduction losses went to a constant value, a very small value of switching losses can be seen. This is because of the reduced switching. T_{A3} conduction losses are quite constant, as there was not much switching and for this reason switching losses are also low. The conduction losses for T_{A4} are constant, as there was not much switching and switching losses for that also is low.

Fig. 5.9 (c, d) shows the conduction and switching losses for anti-parallel diodes. Results showed a bit higher conduction losses for lower two diodes till modulation index of 0.56, and then after it will reduce the losses. Fig. 5.9 (e, f) shows the conduction and switching losses for the NPC diodes. The losses are constant till 0.56, which shows continuous used of NPC diodes, to keep the neutral point potential low, and after that losses will start to reduce.

Fig. 5.10 shows the loss distribution with the hybrid carrier based strategy. As in the hybrid carrier based strategy the duty ratios are generated like in carrier based strategy, the conduction and switching loss distribution follows the similar trend as like the carrier based strategy. Hence, the proposed HPWM strategy was able to keep the loss distribution similar like the carrier based strategy and in the same time was also able to eliminated the problem with DC-offset and additional PI controller.

Fig. 5.11 shows the results with discontinuous PWM strategy. As with the DPWM strategy the phase voltage is clamped with one of the DC-bus voltages, it will reduce the switching losses and will introduce a constant conduction loss as shown in fig. 5.11 (a, b). It can also be observed that, after modulation index of 0.56, the switching losses of T_{A2}, T_{A3} goes down, and conduction loss is also constant. This is because of the continuous conduction of those switches. As the T_{A1}, T_{A2} starts to take the power sharing after 0.56, the anti-parallel diodes conduction and switching losses are also goes down as shown in Fig. 5.11 (c, d). The NPC diodes conduction time increase with T_{A2}, T_{A3}, and it will helps to reduce the conduction losses of anti-parallel diodes up to 0.56 modulation index and after that, it will follow the standard carrier based profile, as there is not much influence of the redundant voltage vectors to play.

Comparing all four control strategies, it can be observed that, depending on the DC-link voltage balancing control strategy the loss sharing between different power switches and diodes changes till 0.56 of modulation index, where the redundant voltage vectors are dominant. When modulation index pass 0.56 and enter to the outer subsectors, the influence of redundant voltage vector reduces and all of them shows almost the similar loss profile.

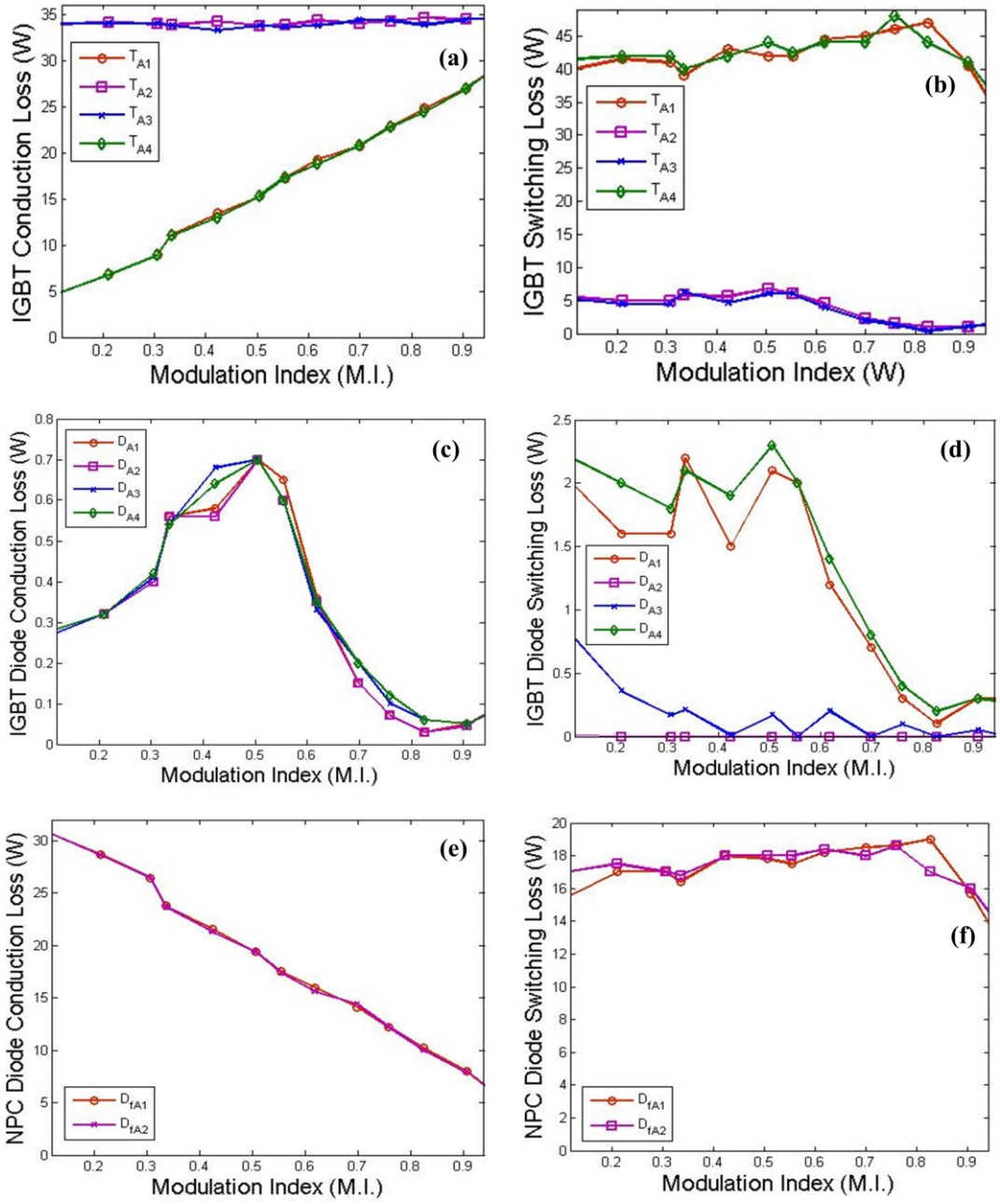


Figure 5.10 Switching and conduction losses for each IGBT and diodes for each leg with Hybrid-PWM based control strategy, (a) IGBT conduction loss, (b) IGBT switching loss, (c) IGBT anti parallel diode conduction loss, (d) IGBT anti parallel diode switching loss, (e) NPC diode conduction loss, (f) NPC diode switching loss.

Fig. 5.12 shows the total IGBT and diode conduction and switching losses for each lag with change in modulation index. With carrier base strategy the losses keep on increasing with modulation index for outer two switches, as shown in Fig. 5.12 (b). Hybrid PWM strategy shows similar trend (Fig. 5.12 (c)) like the carrier based strategy. However, with the proposed discontinuous PWM strategy (Fig. 5.12 (d)) the loss distribution is balanced over the modulation cycle as the earlier proposed SVPWM strategy (Fig. 5.12 (a)).

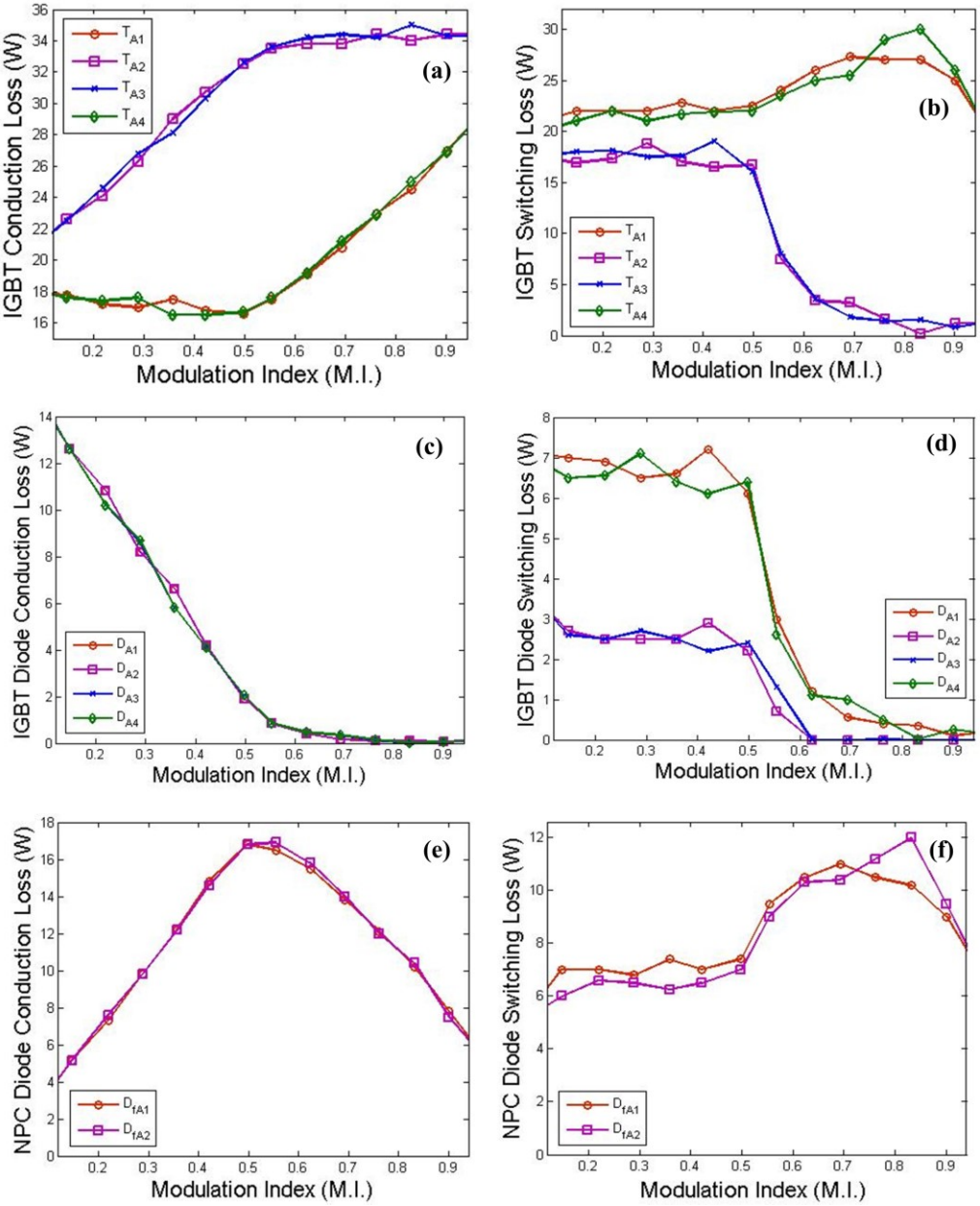


Figure 5.11 Switching and conduction losses for each IGBT and diodes for each leg with Discontinuous-PWM based control strategy, (a) IGBT conduction loss, (b) IGBT switching loss, (c) IGBT anti parallel diode conduction loss, (d) IGBT anti parallel diode switching loss, (e) NPC diode conduction loss, (f) NPC diode switching loss.

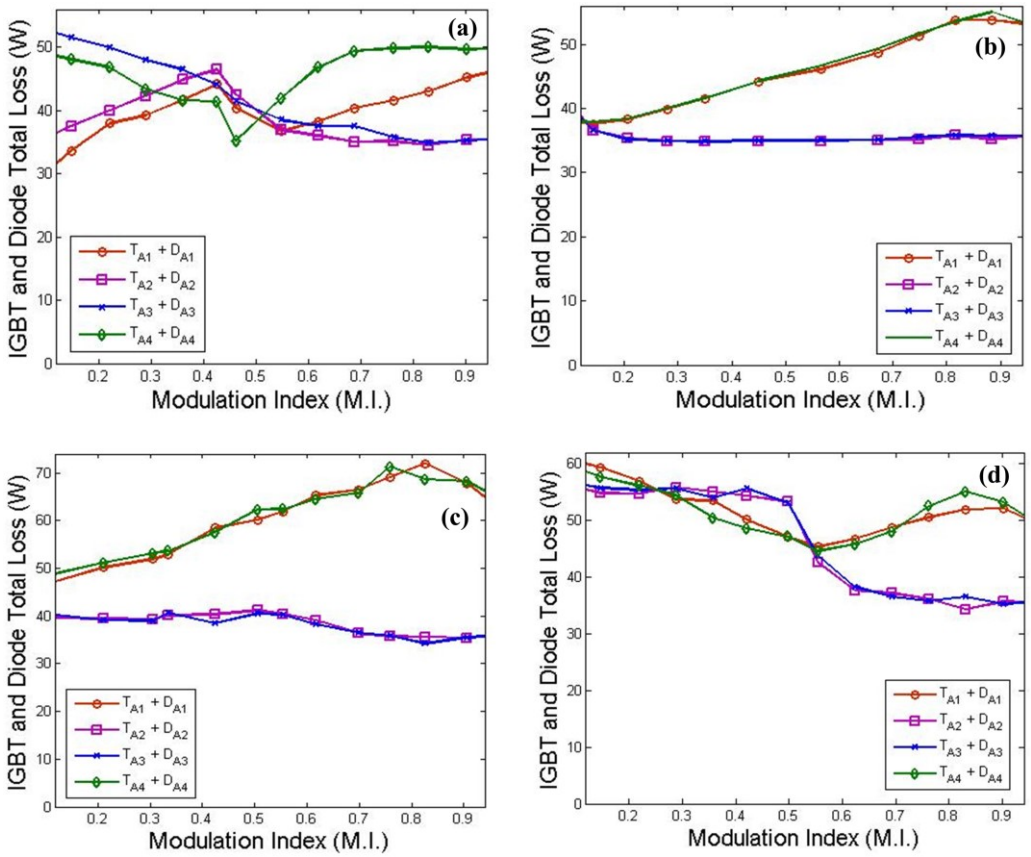


Figure 5.12 IGBT and anti-parallel diode total conduction and switching loss for each power switch and inverter lag, with proposed; (a) SV-PWM, (b) Carrier-based PWM, (c) Hybrid-PWM and (d) DPWM based control strategy.

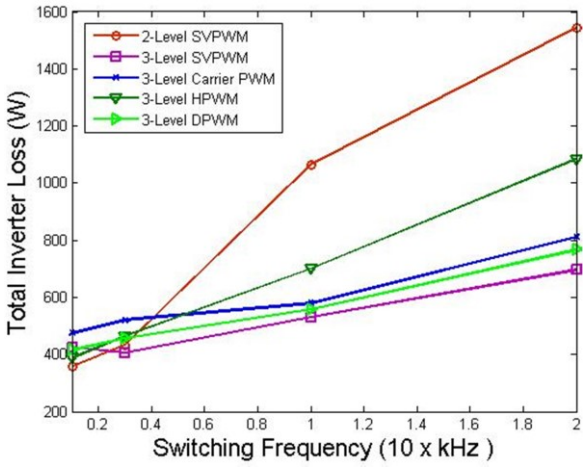


Figure 5.13 Total inverter loss comparison with different proposed control strategies.

Fig. 5.13 shows the total inverter loss comparison between different proposed control strategies for three-level inverter and conventional two-level inverter loss. Due to the optimized switching vectors used for the proposed SV-PWM strategy, it shows the lowest inverter loss at higher switching frequencies among the other proposed strategies. In carrier

based strategy, there is no control over the switching vectors; hence it produces a bit higher inverter losses compared to the SVPWM strategy.

In case of proposed HPWM strategy, the losses are higher than the carrier based strategy. The addition loss component in HPWM strategy comes from the change in switching sequence, to keep the capacitor voltages balanced. This additional cost we have to pay to improve the transient performance of the system and to eliminate the DC-offset problem with the conventional carrier based strategy. However, the proposed DPWM strategy reduces the inverter losses lower than the carrier based strategy, but still it is bit higher than the SVPWM strategy. Hence, if the total inverter loss is considered for selecting a control strategy, then SVPWM would be the best choice. However, DPWM will reduce the computational complexity of the system compared to the SVPWM strategy, with bit higher inverter losses.

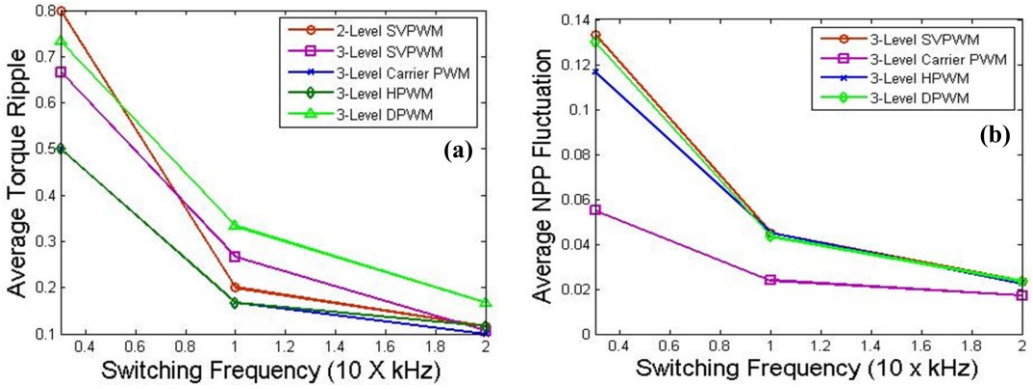


Figure 5.14 (a) Average torque and (b) Neutral point potential fluctuation (NPP), with the proposed control strategies

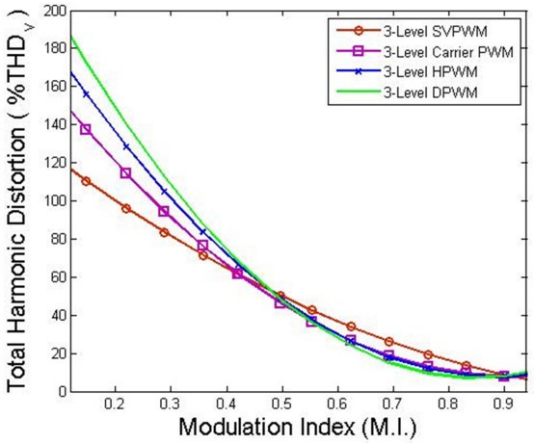


Figure 5.15 Simulation results for total harmonic distortion comparison between proposed PWM strategies for three-level inverter.

Fig. 5.14 (a) shows the average torque ripple comparison between different proposed schemes. Two-level inverter has the highest torque ripple at lower switching frequencies and at high switching frequencies above 10.0 kHz it is comparable with other three-level

strategies. However, carrier based PWM showed the lowest torque ripple among them. Fig. 5.14 (b) shows the NPP fluctuation in different three-level inverter control strategies. The carrier based PWM showed the lowest NPP fluctuation and SVPWM or other proposed strategies shows bit higher cap voltage deviation.

Fig. 5.15 shows the simulation results for total harmonic distortion with 6.0 kW SPMSM and proposed four DC-link voltage balancing strategies for three-level inverter. SVPWM strategy shows the lowest harmonic distortion and DPWM shows the highest %THD among the four. This is because of the clamping of the phases with one of the DC-bus for DPWM based strategy. However, with higher modulation index above 0.5, when the effects of the redundant voltage vectors get reduced, all of them show almost the similar performance results.

5.5. Experimental Results Based Performance Comparison Study

Fig. 5.16 shows the experimental study based %THD comparison for all four control strategies. Results trends are quite similar with the simulation as shown in Fig. 5.15. However, hybrid-carrier based strategy shows a bit lower harmonic distortion. As the %THD for the control strategies are calculated at steady state when machine is allowed to run at fixed speed, no system transients were present and it helps to reduce the harmonic distortion considerably. Moreover, with carrier based PWM there was no change in switching sequence based on capacitor voltage deviation like SVPWM based strategy, which also helps to reduce the harmonic distortion.

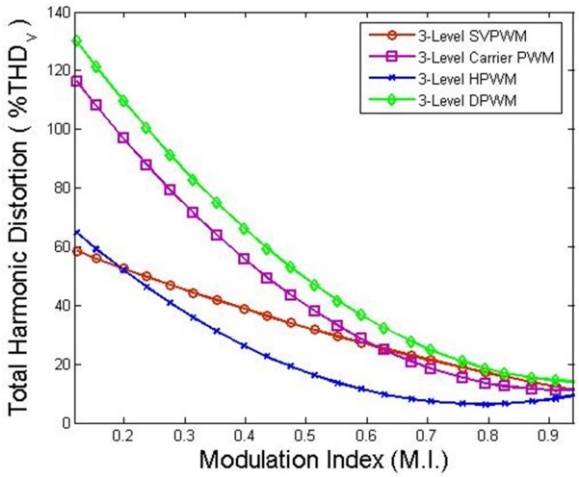


Figure 5.16 Experimental results for total harmonic distortion comparison between proposed PWM strategies for three-level inverter.

Table IX shows the performance comparison study based on the experimental results. Results show a considerable reduction in computational time with the proposed carrier based strategies compared to the SVPWM based strategy. This will help to accommodate other computational logic and protections to facilitate and improve the performance of entire drive system. Current harmonic distortions are also compared. Results showed that SVPWM strategy has the lowest harmonic distortion and among the carrier based strategies HPWM produces the lower current harmonics.

Table IX: EXPERIMENTAL RESULTS BASED PERFORMANCE COMPARISON STUDY FOR DIFFERENT PROPOSED CONTROL STRATEGIES

	SV-PWM	**Carrier-PWM**	**HPWM**	**DPWM**
Total program execution time	25 µsec	16 µsec	16 µsec	16 µsec
Current harmonics ($\%THD_i$)	2.84	4.82	3.06	3.41

5.6. Summary of Chapter 5

This chapter provided a detailed analytical derivation of switching and conduction losses for both two- and three-level inverter with change in modulation index and switching frequencies. Simulation studies are also performed to compare the two-level inverter and proposed control strategies for there-level inverters. Loss distribution in different power switches, total inverter loss, average torque and NPP fluctuation are also compared.

Chapter 6. IPMSM Operation with Three-Level Inverter for Wider Speed-Torque Range

Interior permanent magnet machines (IPMSM) are also used in electric vehicle propulsion applications for wider speed range of operation. Due to the presence of the reluctance torque it can produce more torque compared to the surface PMSM, for same per unit of stator current. As the magnets are buried into the rotor, as compared to the surface PMSM where magnets are on the surface, it produces a difference in *d*- and *q*- axis inductances, L_d and L_q. As, magnets are buried in the d-axis, L_q is always higher than L_d.

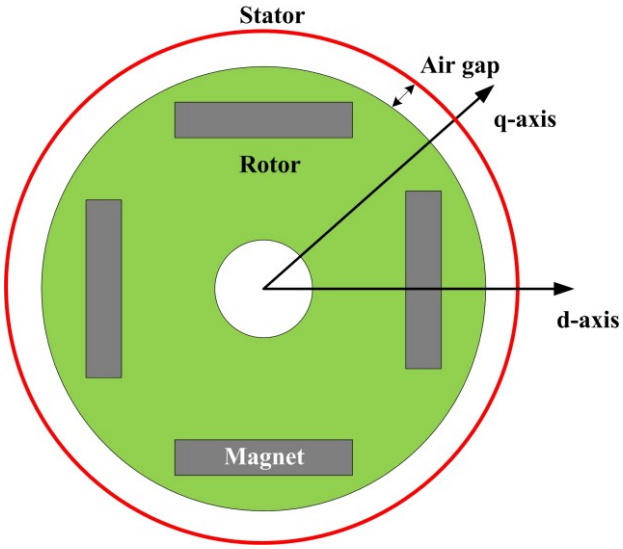


Figure 6.1 Interior PMSM rotor

6.1. SVPWM Based Control Strategy for IPMSM with DC-Link Voltage Balancing

The SVPWM strategy developed for surface PMSM is now applied to the IPMSM and the performance of the system will be observed for change in speed and torque. All the machine equations will remain same as shown in (2.1), (2.2) and (2.7). The *d*- and *q*- axis currents can be expressed as shown eq. (6.1) and (6.2).

$$i_{qs} = I_s \cdot \cos(\beta) \tag{6.1}$$

$$i_{ds} = I_s \cdot \sin(\beta) \tag{6.2}$$

6.1.1. Maximum Torque per Ampere Control Strategy

To achieve the maximum torque from per ampere of stator armature current (MTPA), there are control strategies which generate the reference current by solving numeric equations, or by using a lookup table approximation. In this study the reference currents (i_d,

i_q) are calculated based on the stator current reference (i_s) generated from the difference between the reference and actual speed, as shown in Fig. 6.2 and from the torque angle, which gives the maximum toque for minimum stator current. Table X shows the data collected based on the maximum torque per ampere (MTPA) scheme and (6.3) shows the torque angle calculated from the table using third order polynomial. This is the required torque angle, where torque generated will be maximum for a given stator current requirement.

Table X: A SET OF CORRESPONDING DATA, I_s and β.

Stator Current (I_s)	**Current Angle (β)**
0.2	0.0
2.0	0.0
5.0	4.0
10.0	8.0
15.0	12.0
20.0	15.0
25.0	18.0
30.0	20.0
35.0	22.0

Using third order polynomial approximation, current angle can be expressed by (6.3) as shown below.

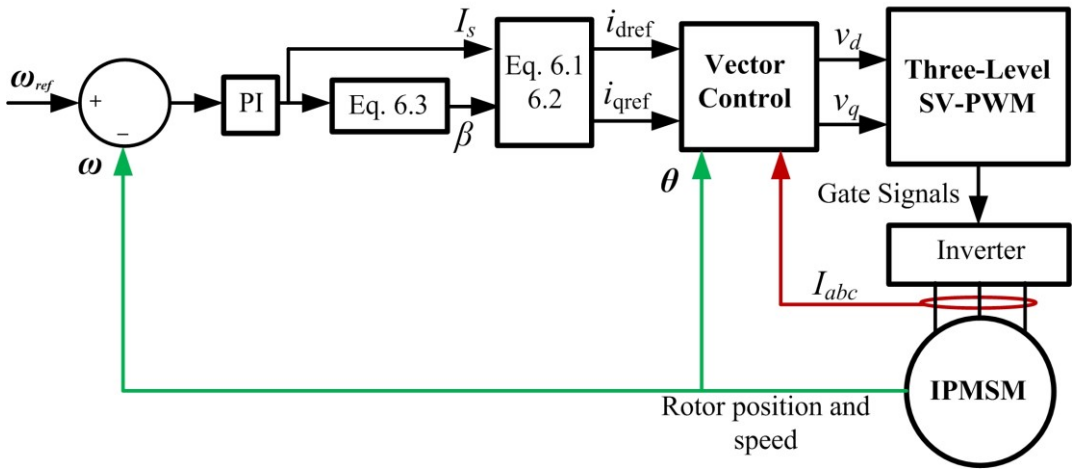


Figure 6.2 Control circuit diagram of IPMSM with three-level inverter.

$$\beta = -(2\cdot 10^{-4})\cdot I_s^3 - (3\cdot 10^{-16})\cdot I_s^2 + 0.812\cdot I_s + (6\cdot 10^{-14}) \tag{6.3}$$

As shown in Fig. 6.2, the reference value of i_d, i_q are generated from the stator current reference I_s and the current angle β is calculated from (6.3). Reference voltage vectors, v_d and v_q, are generated from the vector controller, which feeds to the 3-level SV-PWM block.

To control the IPMSM with DC-link capacitor voltage balancing SVPWM strategy is used, as already been used for surface PMSM in chapter 2. The table to generate the switching pulses is already shown in table VI.

6.1.2. Problem with DC-link Voltage Balancing at Field Weakening Region

As shown in chapter 2, fig. 2.2, with increase in negative *d*-axis current to drive the machine into deep field weakening region, the power factor improves and after a certain time it even goes leading (i_{s1}, i_{s2}). At this point when the modulation index is one (M.I. = 1.0) and the reference phase voltage is in one of the outer most sub-sectors (sub-sector 2, 3, 4), redundant voltage vectors cannot control the neutral point voltage fluctuation most effectively. In this sub-sectors difference in capacitor voltages are mostly dominated by the medium voltage vectors. The situation goes worse, when the phase current starts leading the phase voltage and starts to flow through the antiparallel body diodes of the power switches and come back to the source side.

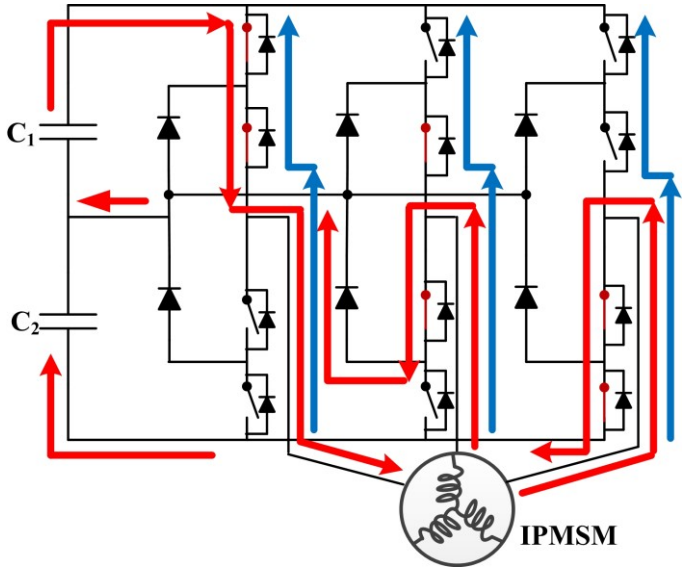


Figure 6.3 Direction of current flow with medium (PON) voltage vector during normal and leading power factor condition.

Fig. 6.3 shows the current direction during application of medium voltage vector PON. The red arrow shows the normal operation when the power factor is unity or lagging and blue line shows the current direction during leading power factor condition for sector one. Fig. 6.4 (a), shows the simulation results for time duration for which different voltage vectors are applied (small, medium, large) and fig. 6.4 (b), shows their effects on the DC-link capacitor

voltage deviation. It can be seen that with the large voltage vectors there is no change in capacitor voltage deviation as was expected, with the redundant voltage vectors the capacitor voltages was trying to decrease, but due to the short time duration, it was not able to make the difference zero. The maximum capacitor voltage deviation is contributed by the medium voltage vectors, and there is no control over the capacitor voltage difference caused by them. From the results it is obvious that the only way to remove this additional neutral point voltage fluctuation is by reducing the use of medium voltage vectors. Till now no research work is shown to reduce the neutral point voltage fluctuation in the field weakening region at modulation index of one.

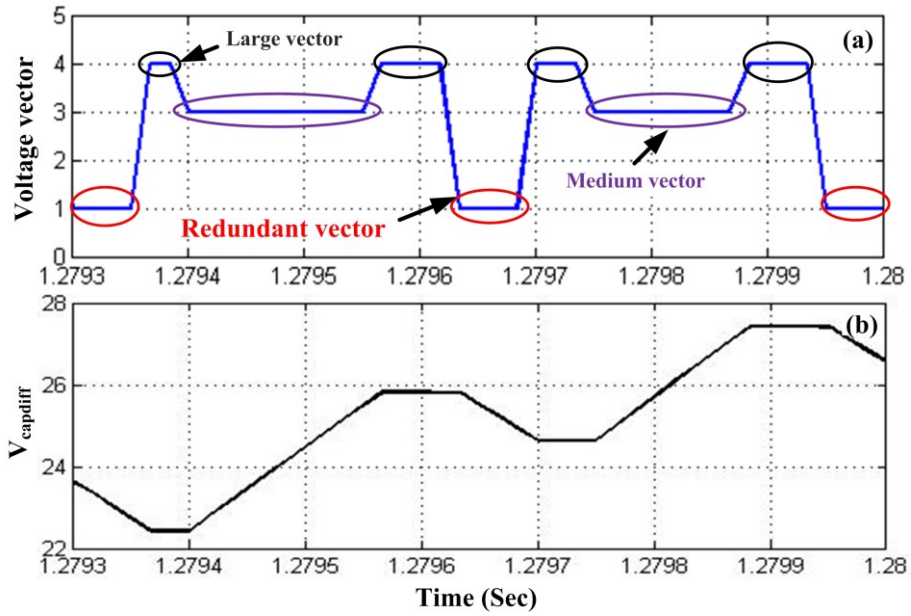


Figure 6.4 Effects of different voltage vectors at higher modulation index (M ~ 1.0) and at leading power factor in subsector-III of sector-I.

6.2. Proposed DC-link Voltage Balancing Algorithm at Leading Power Factor

To reduce the capacitor voltage deviation caused by the medium voltage vectors, four strategies are proposed. Three of them use the two large and one redundant voltage vector without any medium voltage vectors and one of them uses two large and one null voltage vector. The detailed analytical calculation of the power switches duty cycles are developed in the following subsections.

6.2.1. Lower Triangle Vector Sequence Based Control Strategy

Fig. 6.5 (a) shows the vector diagram with the lower triangle. Here, two large voltage vectors and a small or redundant voltage vector are considered to generate the reference phase voltage while modulation index is unity. Here, it can be observed that the use of the

medium voltage vector is completely removed, which produces the NPP fluctuation at leading power factors. The calculations of the time duration for the respective voltage vectors are derived from eq. 6.4 for sector I.

$$V_{ref} \cdot T_S = V_{poo/onn} T_a + V_{ppn} T_b + V_{pnn} T_C \tag{6.4}$$

$$T_a = T_s \cdot \left(2 - \frac{\sqrt{3}}{2} \cdot m \cdot \left(\frac{2}{\sqrt{3}} \cdot \sin(\theta) + 2 \cdot \cos(\theta) \right) \right)$$

$$T_b = T_s \cdot \left(m \cdot \sin(\theta) \right) \tag{6.5}$$

$$T_c = T_s \cdot \left(\sqrt{3} \cdot m \cdot \cos(\theta) - 1 \right)$$

Solving equation (6.4) by splitting the vectors in the real and imaginary parts, the corresponding duty cycles can be obtained, as shown in eq. 6.5. As all other sectors are symmetrical, similar expressions can be obtained for other sectors as well. The switching sequences with the proposed strategy are shown in table XI.

Table XI: SWITCHING SEQUENCE WITH LOWER TRIANGLE BASED STRATEGY

Subsector	Balancing Ability	Switching Sequence
1	$V_{dc1}>V_{dc2}$	POO-PNN-PPN-PNN-POO
	$V_{dc2}>V_{dc1}$	ONN-PNN-PPN-PNN-ONN
2	$V_{dc1}>V_{dc2}$	PPO-PPN-NPN-PPN-PPO
	$V_{dc2}>V_{dc1}$	OON-PPN-NPN-PPN-OON
3	$V_{dc1}>V_{dc2}$	OPO-NPN-NPP-NPN-OPO
	$V_{dc2}>V_{dc1}$	NON-NPN-NPP-NPN-NON
4	$V_{dc1}>V_{dc2}$	OPP-NPP-NNP-NPP-OPP
	$V_{dc2}>V_{dc1}$	NOO-NPP-NNP-NPP-NOO
5	$V_{dc1}>V_{dc2}$	OOP-NNP-PNP-NNP-OOP
	$V_{dc2}>V_{dc1}$	NNO-NNP-PNP-NNP-NNO
6	$V_{dc1}>V_{dc2}$	POP-PNP-PNN-PNP-POP
	$V_{dc2}>V_{dc1}$	ONO-PNP-PNN-PNP-ONO

6.2.2. Upper Triangle Vector Sequence Based Control Strategy

In fig. 6.5 (b) the upper tringle is considered instead of the lower triangle as shown in fig. 6.5 (a). Similar to eq. 6.4, the reference phase voltage can be divided in to real and imaginary axes and expression of duty cycles can be obtained as shown in eq. 6.6. All the other sector duty ratios can be calculated similarly.

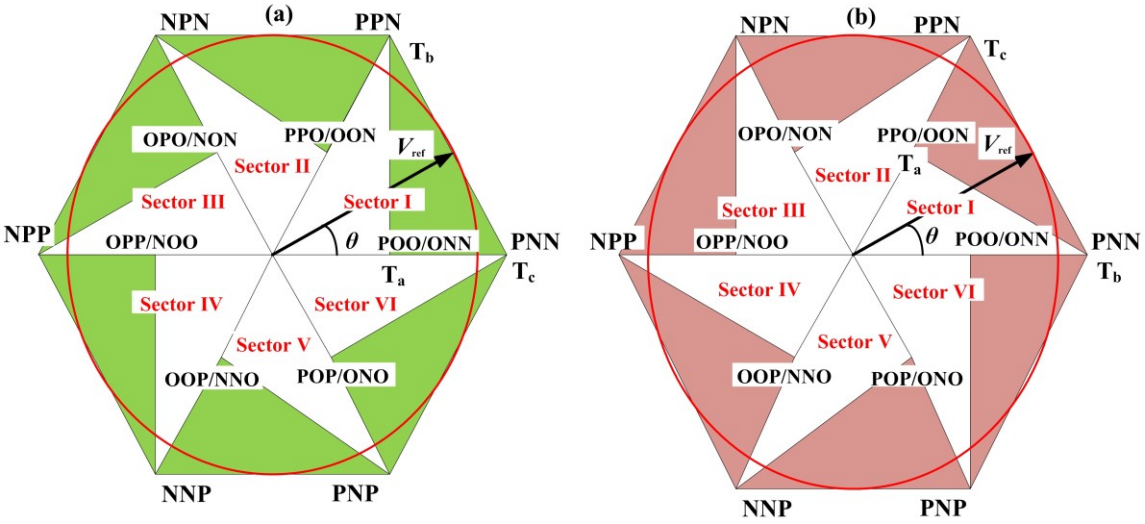


Figure 6.5 Vector diagram with the (a) Lower and (b) Upper triangle vector sequence based strategy.

$$
\begin{aligned}
T_a &= T_s \cdot \left(2 - \frac{\sqrt{3}}{2} \cdot m \cdot \left(2 \cdot \cos(\theta) + \left(\sqrt{3} - \frac{1}{\sqrt{3}} \right) \cdot \sin(\theta) \right) \right) \\
T_b &= T_s \cdot \left(\frac{\sqrt{3}}{2} \cdot m \cdot \left(\cos(\theta) - \frac{1}{\sqrt{3}} \cdot \sin(\theta) \right) \right) \\
T_c &= T_s \cdot \left(\left(\frac{\sqrt{3}}{2} \cdot m \cdot \left(\cos(\theta) + \sqrt{3} \cdot \sin(\theta) \right) \right) - 1 \right)
\end{aligned}
\tag{6.6}
$$

The switching sequence corresponding to this control strategy is shown in table XII.

Table XII: SWITCHING SEQUENCE WITH UPPER TRIANGLE BASED STRATEGY

Subsector	Balancing	Switching Sequence
1	$V_{dc1}>V_{dc2}$	PPO-PPN-PNN-PPN-PPO
	$V_{dc2}>V_{dc1}$	OON-PPN-PNN-PPN-OON
2	$V_{dc1}>V_{dc2}$	OPO-NPN-PPN-NPN-OPO
	$V_{dc2}>V_{dc1}$	NON-NPN-PPN-NPN-NON
3	$V_{dc1}>V_{dc2}$	OPP-NPP-NPN-NPP-OPP
	$V_{dc2}>V_{dc1}$	NOO-NPP-NPN-NPP-NOO
4	$V_{dc1}>V_{dc2}$	OOP-NNP-NPP-NNP-OOP
	$V_{dc2}>V_{dc1}$	NNO-NNP-NPP-NNP-NNO
5	$V_{dc1}>V_{dc2}$	POP-PNP-NNP-PNP-POP
	$V_{dc2}>V_{dc1}$	ONO-PNP-NNP-PNP-ONO
6	$V_{dc1}>V_{dc2}$	POO-PNN-PNP-PNN-POO
	$V_{dc2}>V_{dc1}$	ONN-PNN-PNP-PNN-ONN

6.2.3. Mix Vector Sequence Based Control Strategy

In this control sequence both the upper and the lower vector sequences are used. When the reference voltage vector (V_{ref}) position (θ) is below 30°, the lower triangle vector sequences are used and when the position is more than 30°, upper triangular vector sequences are used. It is used to reduce the possible reduction in torque ripple that could appear due to the larger time sharing between the further voltage vectors. When the reference voltage vector position is below 30°, and the upper triangle sequences are used, than the two voltage vector (PPO, PPN) out of the three are further than the closer one which is PNN for sector one. Similarly when the reference voltage vector position is more than 30°, the lower triangle vector sequence will have more distance vectors. Hence, it could be more convenient to use the nearest voltage vectors to produce the reference voltage than the distance one. This strategy is just an extension of the earlier two proposed strategies.

In all these control strategies no medium voltage vectors are used and hence it will eliminate the capacitor voltage fluctuation produced by those vectors. However, the phase voltage produced by these strategies will have a higher harmonic distortion, due to the elimination of the one voltage vector, as compared to conventional three-level inverter phase voltages.

6.2.4. Two-level Equivalent of Three-level Inverter

Fig. 6.6 shows the two-level equivalent of three-level inverter at leading power factor. This will completely eliminate the neutral point voltage fluctuation because it does not use any one of the small or medium voltage vectors.

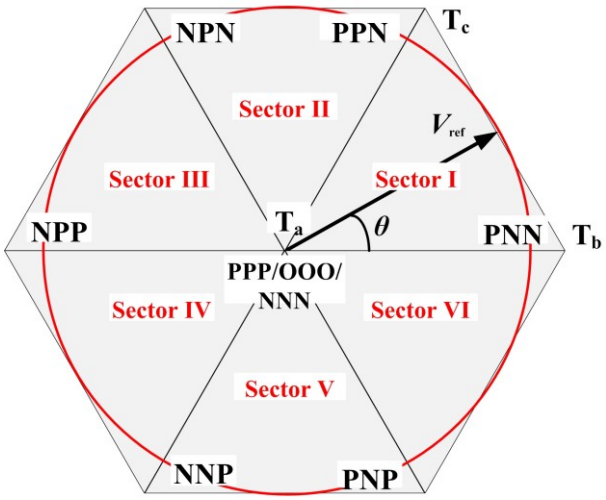


Figure 6.6 Two-level equivalent of a three-level inverter

$$T_a = T_s \cdot \left(m \cdot \sin\left(\frac{\pi}{3} - \theta \right) \right)$$
$$T_b = T_s \cdot \left(m \cdot \sin(\theta) \right) \tag{6.7}$$
$$T_c = T_s \cdot \left(1 - \frac{m}{2} \cdot \cos\left(\frac{\pi}{6} - \theta \right) \right)$$

However, it will produce a higher harmonic distortion than the earlier proposed strategies like the two-level inverter. The switching duty cycles time period will be similar like the two-level inverter as shown in eq. 6.7.

6.3. Simulation Studies

During the simulation studies the switching frequency was kept constant at 3.0 kHz and DC-link voltage was kept constant at 270.0 V. Fig. 6.7 shows the machine performance during a change in machine speed from 150.0 rpm to 800.0 rpm. Speed was changed in ramp. It can be observed from the results that the machine speed changed quite steadily with load torque of 6.0 N.m. and the peak to peak voltage differences between the two capacitors is around 2.0 V, which is below 1.0 % of the total DC-link voltage. During the deceleration period at 2.7 sec, the capacitor voltage difference increases, which could be coming from the deceleration rate or the PI controller gains used for vector controller. However, the voltage difference is about 8.0 V, which is less than 3.0% of the total DC-link voltage.

Fig. 6.8 shows the machine performance during change in load torque from 6.0 N.m. to 24.0 N.m. It can be observed that the motor speed gets reduced during transients and gets back to the reference speed of 550.0 rpm, when transients settle down, which shows the required controllability of the proposed system.

The capacitor voltage difference and stator currents have increased at higher machine torque, because the capacitor needs to supply more power. The maximum peak capacitor voltage difference is 7.0 V, which is 2.5 % of total DC-link voltage.

Fig. 6.9 to fig. 6.12 shows the result with the four proposed control strategies. In all these simulation studies, speed is changed to above base speed at 1298.0 rpm, which leads to an increase in the modulation index to go higher than one. To bring back the modulation index to one, a negative *d*-axis current of -6.0 Amp was injected in to the *d*-axis at 1.7 sec. It can be observed that the modulation index has now dropped down to one and the capacitor voltage deviation has now also increased.

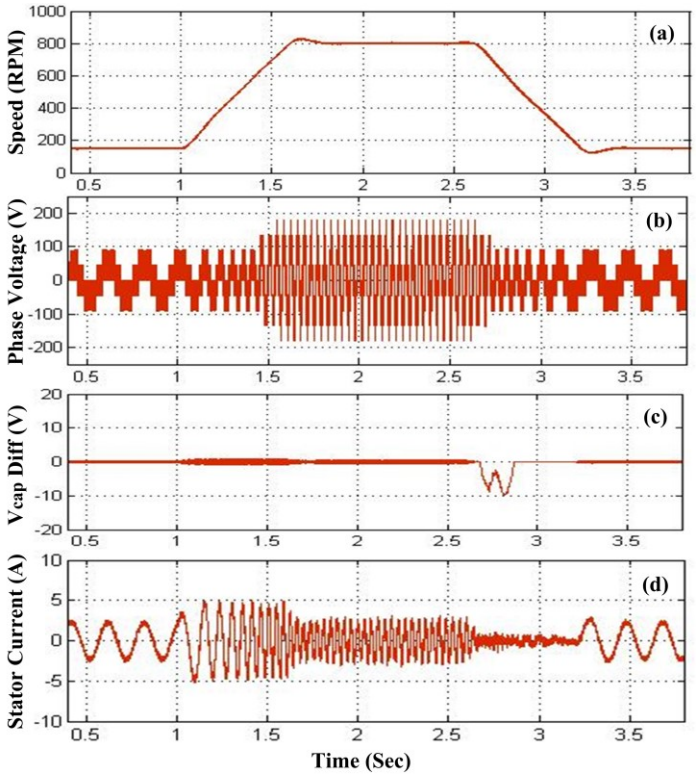


Figure 6.7 Performance results for the three-level inverter with change in speed from 150.0 rpm to 800.0 rpm at 6.0 N.m. load torque; (a) Change in machine speed; (b) Phase voltage; (c) Difference between two DC-link capacitor voltages; (d) Stator current.

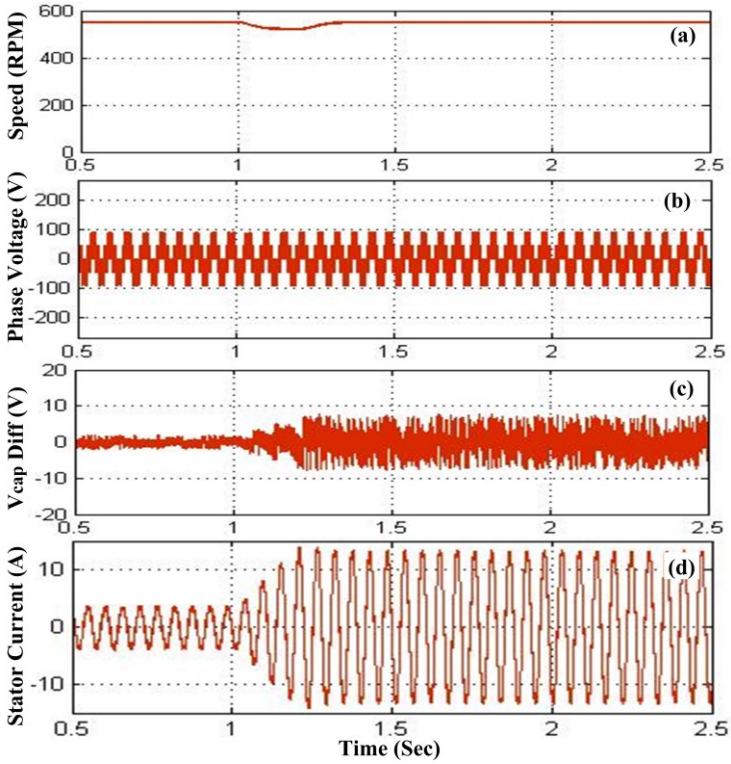


Figure 6.8 Performance results for three-level inverter with change in load torque from 6.0 N.m. to 24.0 N.m. at 550.0 rpm machine speed; (a) Change in machine speed; (b) Phase voltage; (c) Difference between the two DC-link capacitor voltages; (d) Stator current.

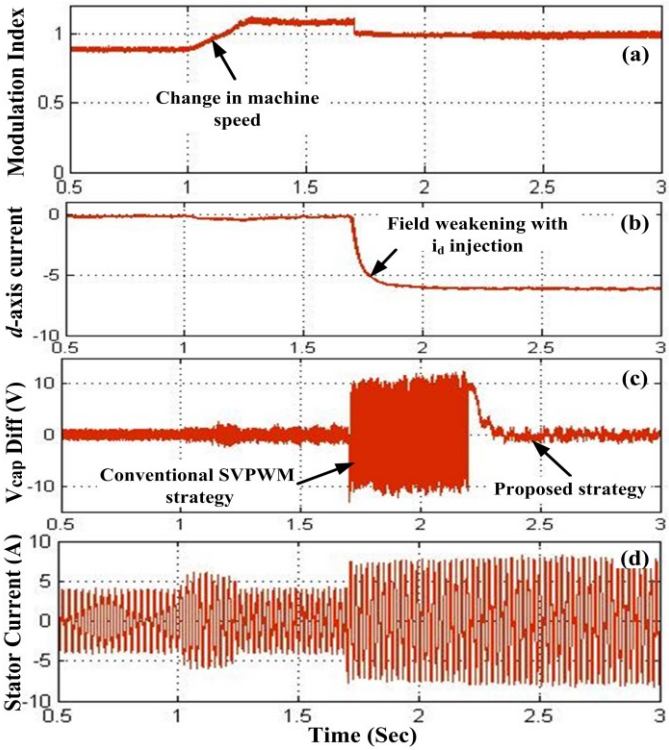


Figure 6.9 Performance results for three-level inverter with lower tringle based control strategy; (a) Change in modulation indices; (b) *d*-axis current; (c) Difference between the two DC-link capacitor voltages; (d) Stator current.

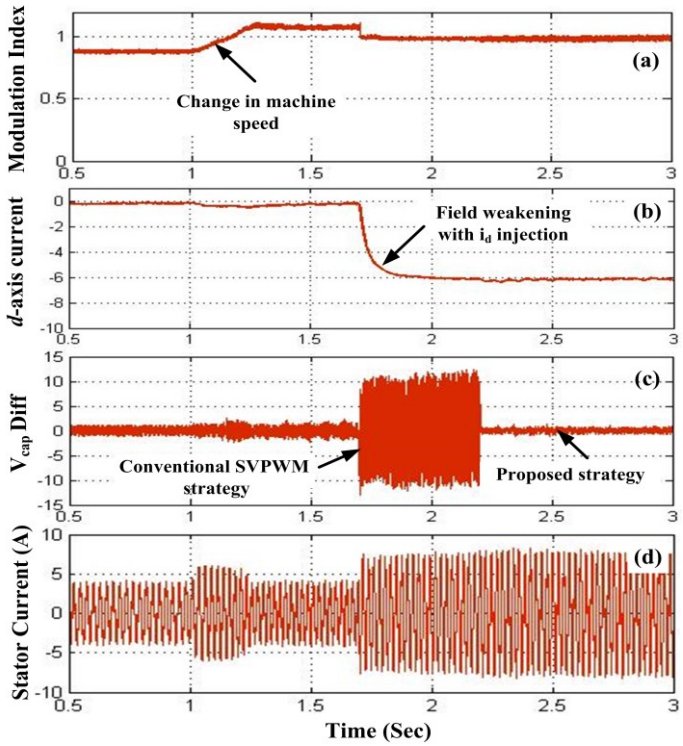


Figure 6.10 Performance results for three-level inverter with upper tringle based control strategy; (a) Change in modulation indices; (b) *d*-axis current; (c) Difference between the two DC-link capacitor voltages; (d) Stator current.

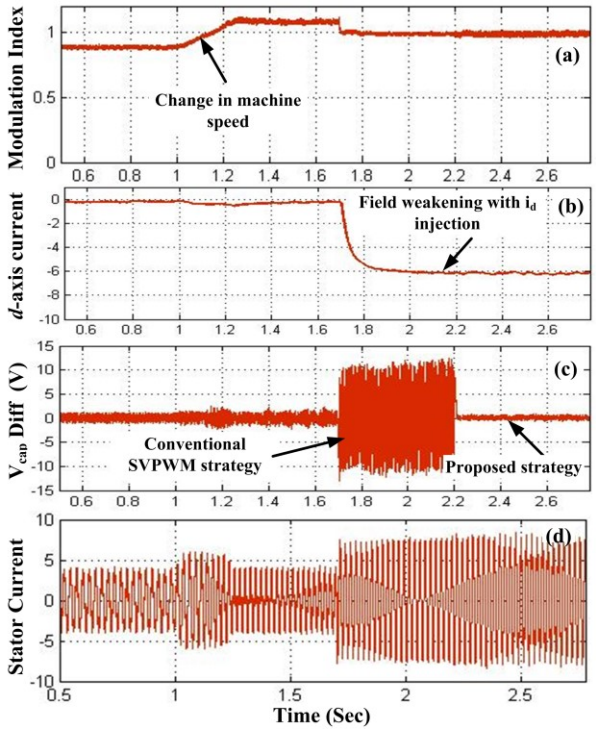


Figure 6.11 Performance results for three-level inverter with mix vector sequence based control strategy; (a) Change in modulation indices; (b) *d*-axis current; (c) Difference between the two DC-link capacitor voltages; (d) Stator current.

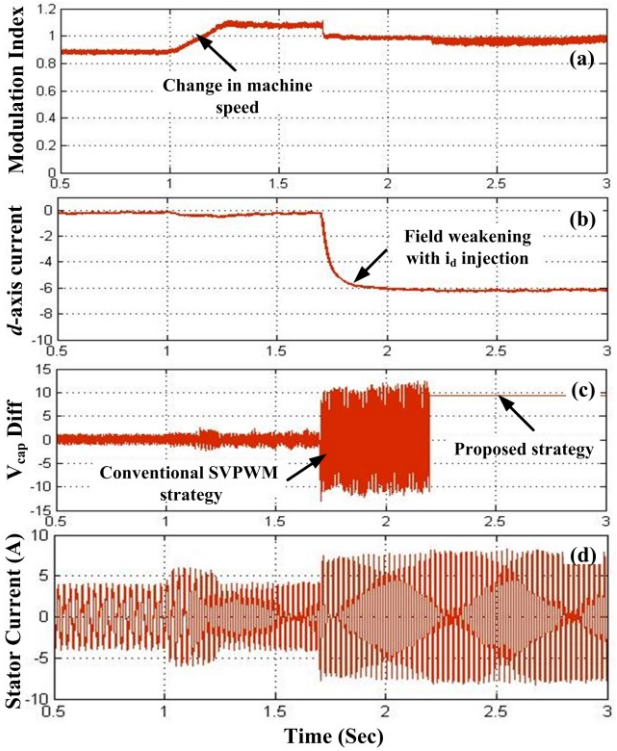


Figure 6.12 Performance results for three-level inverter with 2-level sequence based control strategy; (a) Change in modulation indices; (b) *d*-axis current; (c) Difference between the two DC-link capacitor voltages; (d) Stator current.

The increase in the capacitor voltage deviation is basically due to the leading power factor effect that is explained in section 6.1.2. At 2.2 sec the four proposed control strategies are applied. It can be seen that with the first three control strategies, the voltage deviation has almost reduced to 10.0% of the conventional strategy. Moreover, with the mix sequence based control strategy the capacitor voltage deviation is more ripple free, then that of the other two strategies (Lower and upper triangle based). The possible reason for this reduction is already explained in section 6.1.2.

Fig. 6.12 shows the similar results with two-level equivalent strategy. As it was expected there is no capacitor voltage deviation, as no small and medium voltage vectors are used.

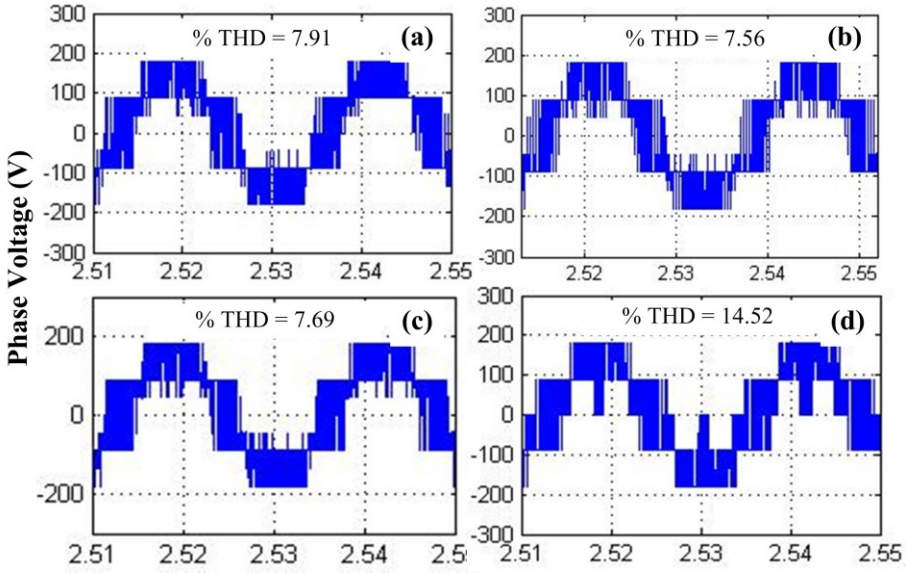


Figure 6.13 Phase voltage harmonic distortion comparison with (a) Lower triangle; (b) Upper triangle; (c) Mix sequence; (d) 2-level equivalent control based DC-link voltage balancing strategy.

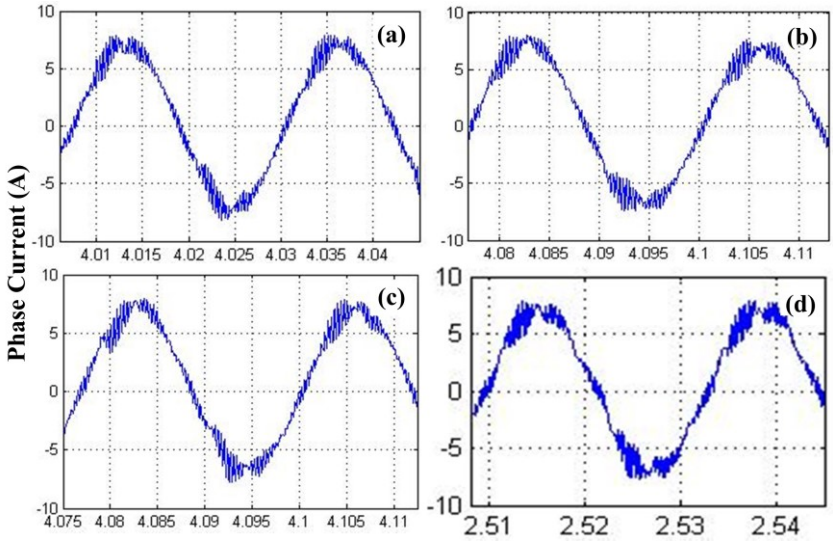


Figure 6.14 Phase current comparison at 43.33 Hz with; (a) Lower triangle; (b) Upper triangle; (c) Mix sequence; (d) 2-level equivalent control based DC-link voltage balancing strategy.

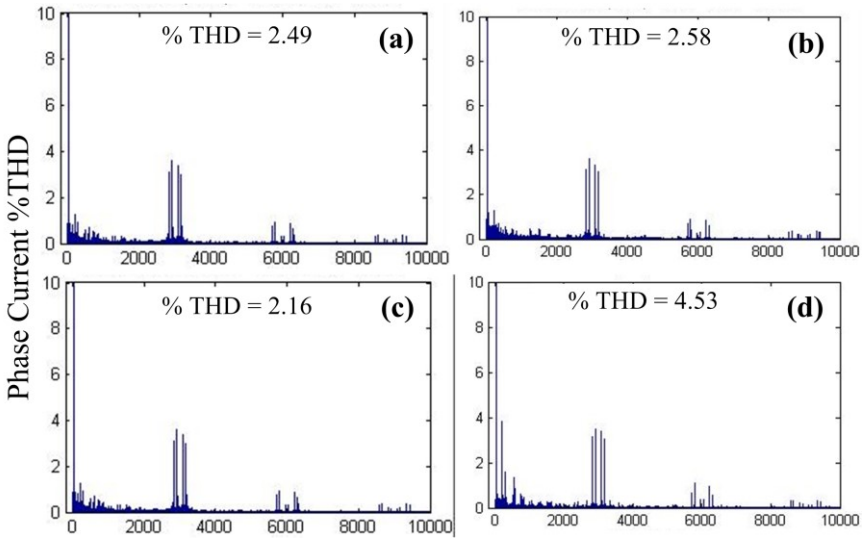


Figure 6.15 Phase current harmonic distortion comparison at 43.33 Hz with (a) Lower triangle; (b) Upper triangle; (c) Mix sequence; (d) 2-level equivalent control based DC-link voltage balancing strategy.

Fig. 6.13 shows the phase voltage harmonic distortion with the four proposed control strategies. With the two-level equivalent strategy the harmonic distortion is the highest among the four. From the current harmonic distortion analysis shown in Figs. 6.14, 6.15, it is clear that, with the mix sequence based strategy the current distortion is less, which also helps to keep the capacitor voltage deviation low as shown in Fig. 6.11. With the 2-level based sequence, the current harmonic distortion is the highest among them.

6.4. Experimental Results

The proposed control algorithm is tested with a prototype of 6.0 kW IPMSM machine. Experimental work is carried out with a dspace® based real time operating system with 25.0 μsec of step time and switching frequency is kept constant at 3.0 kHz.

Fig. 6.16 shows the performance of the machine with change in speed from 150.0 rpm to 800.0 rpm, with 6.0 N.m. of load torque. Here, we can observe that the machine speed has changed in ramp and the level of phase voltage has also increased as shown in the simulation. This increase in the voltage level with modulation index helps to reduce the harmonic distortion (%THD). The capacitor peak voltage differences are also around 1.5 V at top speed, which is below 1.0% of the total DC-link voltage. Fig. 6.17 shows the machine performance during change in load torque from 6.0 N.m. to 24.0 N.m., while machine speed was kept constant at 550.0 rpm. From the experimental results, it can be observed that, while load is changed, the capacitor voltage difference is increased, as shown in simulation results. However, the differences are well below the tolerance level. The maximum capacitor voltage difference goes 2.23 % of the total DC-link voltage.

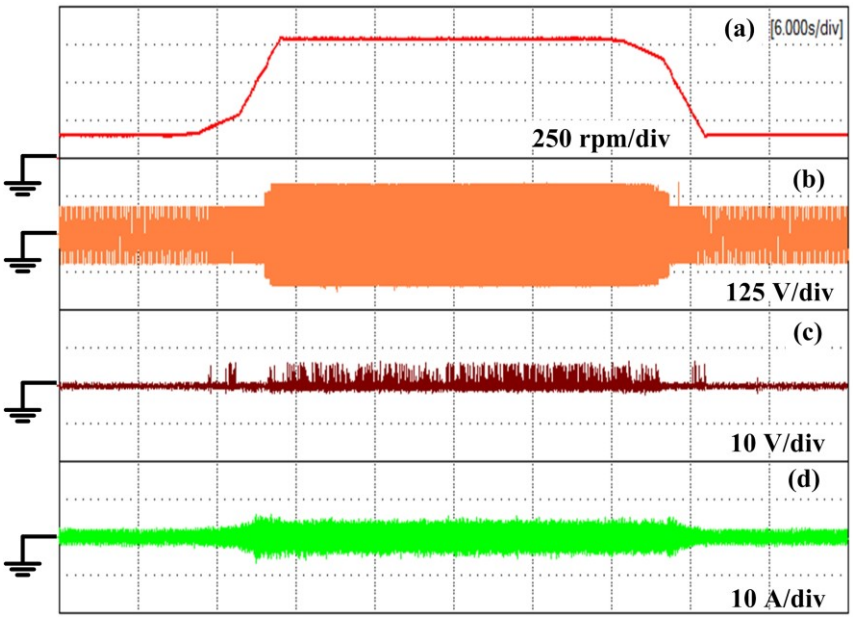


Figure 6.16 Experimental results for three-level inverter with change in speed from 150.0 rpm to 800.0 rpm at 6.0 N.m. load torque; (a) Change in machine speed; (b) Phase voltage; (c) Difference between the two DC-link capacitor voltages; (d) Stator current.

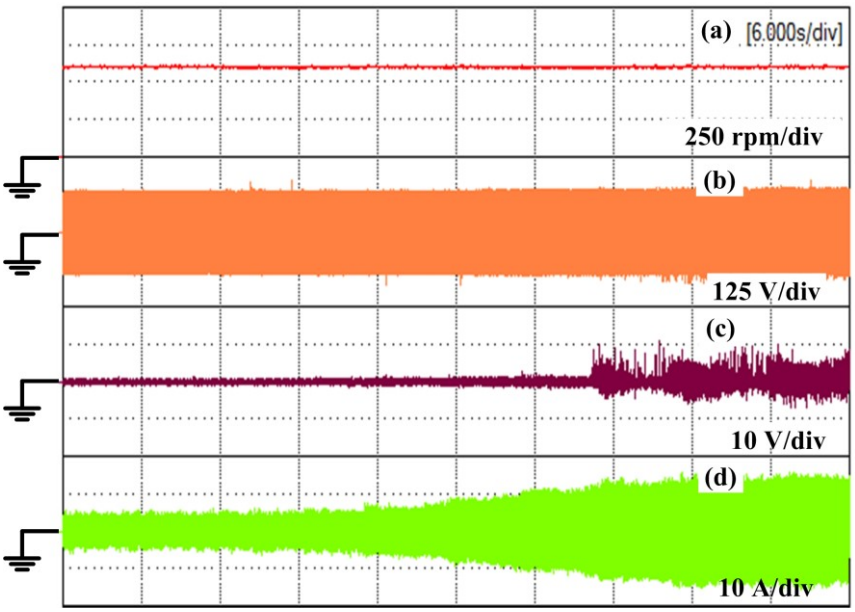


Figure 6.17 Experimental results for three-level inverter with change in load torque from 6.0 N.m. to 24.0 N.m. at 550.0 rpm machine speed; (a) Change in machine speed; (b) Phase voltage; (c) Difference between the two DC-link capacitor voltages; (d) Stator current.

From both the simulation and experimental results it can be observed that the proposed DC-link voltage balancing scheme for the IPMSM machine works well below the base speed and torque transients as well.

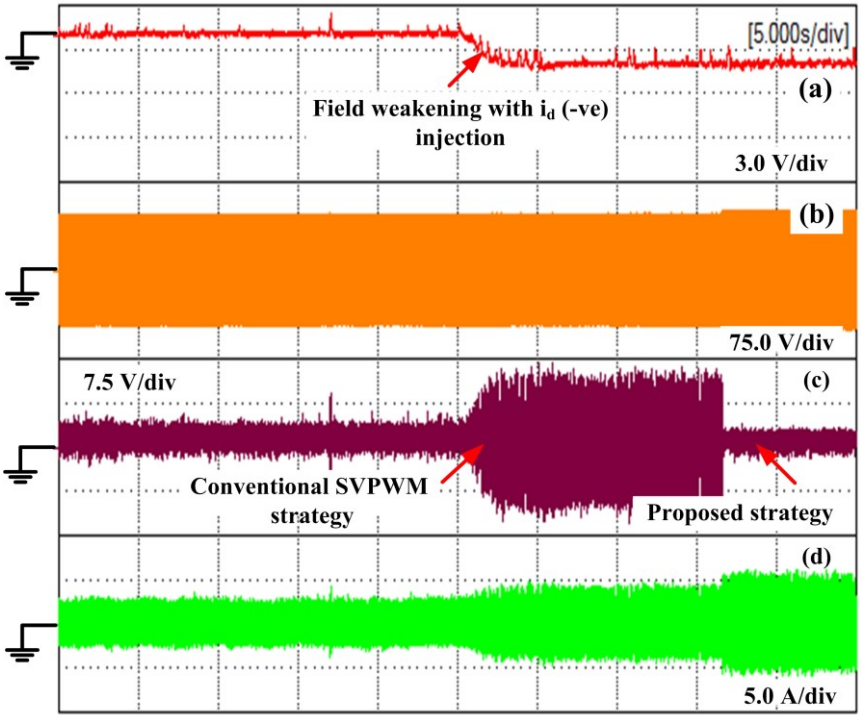


Figure 6.18 Performance results for three-level inverter with lower tringle based control strategy; (a) Change in *d*-axis current; (b) stator phase voltage; (c) Difference between the two DC-link capacitor voltages; (d) Stator current.

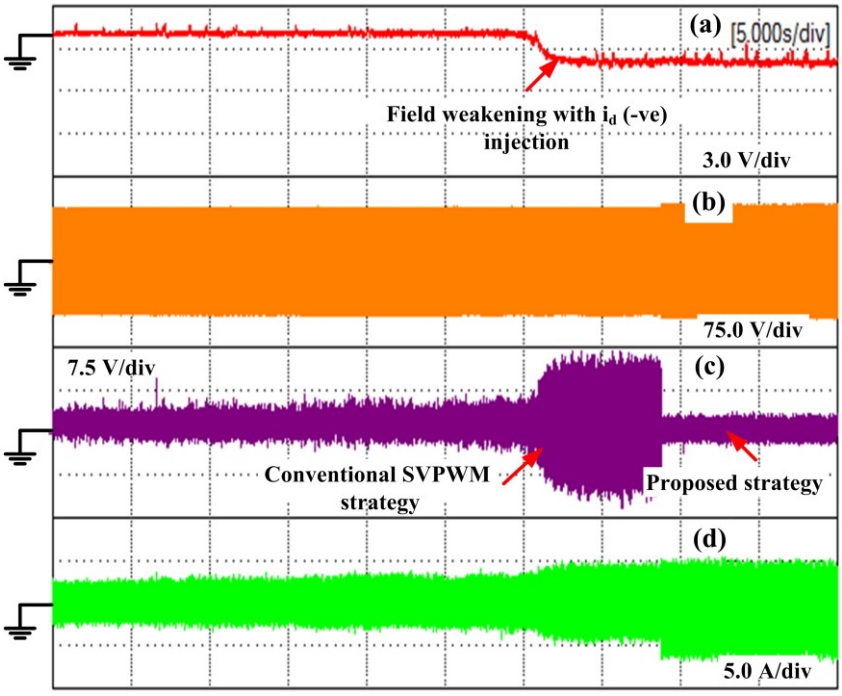


Figure 6.19 Performance results for three-level inverter with upper tringle based control strategy; (a) Change in *d* -axis current; (b) stator phase voltage; (c) Difference between the two DC-link capacitor voltages; (d) Stator current.

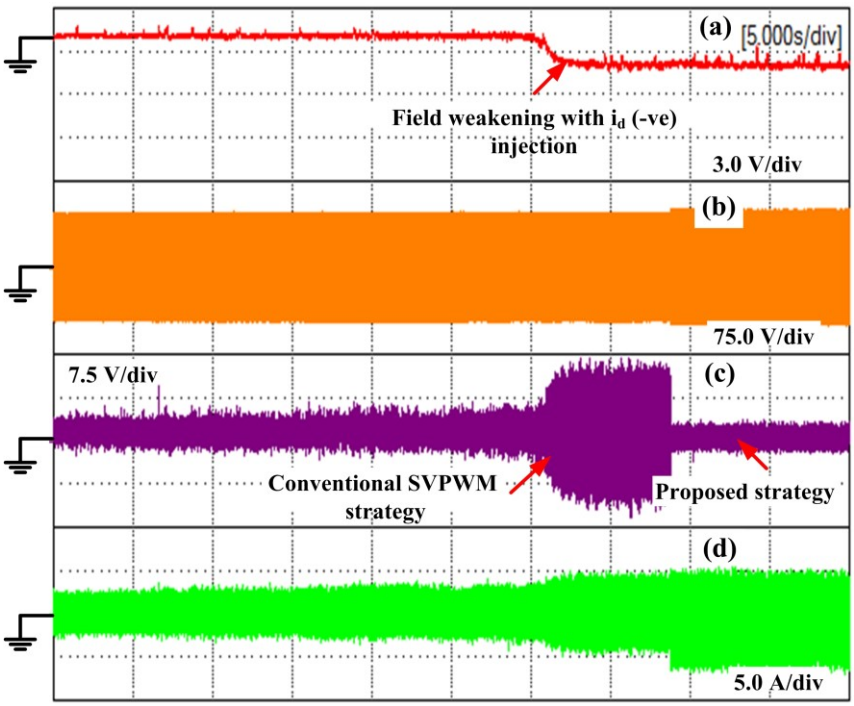


Figure 6.20 Performance results for three-level inverter with mix vector sequence based control strategy; (a) Change in *d* -axis current; (b) stator phase voltage; (c) Difference between the two DC-link capacitor voltages; (d) Stator current.

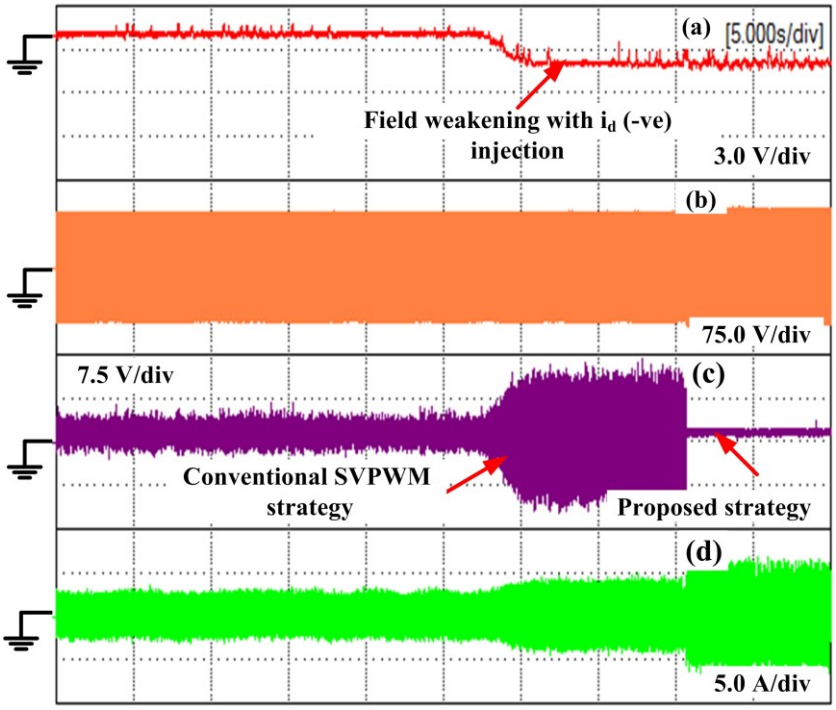


Figure 6.21 Performance results for three-level inverter with 2-level sequence based control strategy; (a) Change in *d* -axis current; (b) stator phase voltage; (c) Difference between the two DC-link capacitor voltages; (d) Stator current.

Figs. 6.18-6.21 show the performance comparison with all the four proposed control strategies, in the field weakening region. The DC-link voltage was kept at 150.0 V, for this study. As with the previously proposed DC-link balancing scheme a lot of capacitor voltage deviation occurs at neutral point in field weakening region, to keep the system safe, DC-link voltage was kept low at 150.0 V. The motor was run at above base speed and 2.0 A of negative *d*-axis current was injected. From the results it can be seen that, with the conventional strategy the peak to peak capacitor voltage deviation goes around 28.0 V and with the proposed control strategies it is only 4.5 V.

Hence, there is a reduction of 83.9% compared to the conventional strategy. Moreover with the 2-level sequence based strategy there is no voltage deviation, because it does not use any other medium or small voltage vectors.

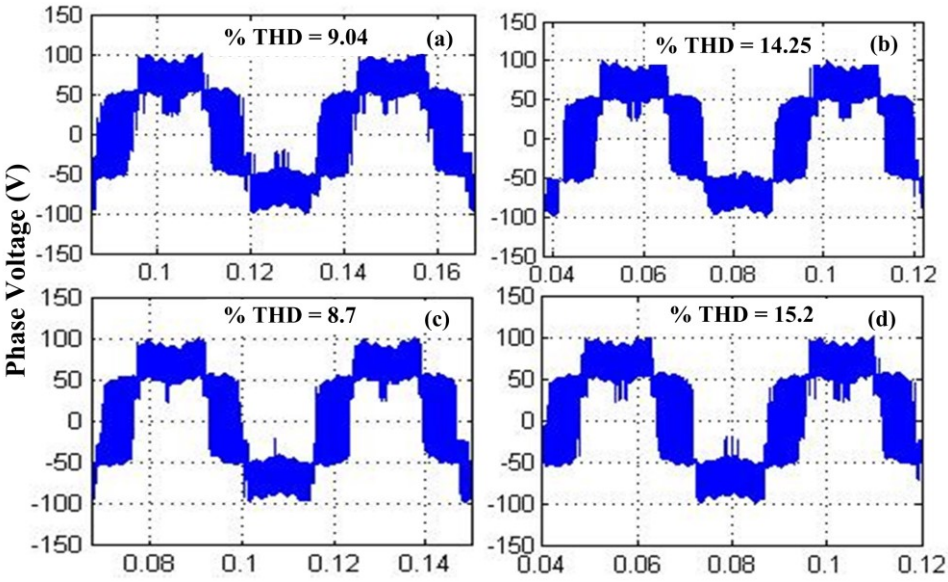


Figure 6.22 Experimental results for phase voltage harmonic distortion comparison with (a) Lower triangle; (b) Upper triangle; (c) Mix sequence; (d) 2-level equivalent control based DC-link voltage balancing strategy.

Fig. 6.22 shows the experimental results for phase voltage harmonics with the proposed four control strategies at field weakening region. As it was expected from the simulation results with the mix sequence based control strategy voltage harmonic could be low, now it can be seen from the experimental results. Although, the voltage harmonic distortions are quite close, mix sequence strategy produces the lowest harmonics content and the two-level strategy produces the maximum distortion among the four strategies.

6.5. Summary of Chapter 6

A detailed study of the proposed modified DC-bus voltage balancing algorithm for three-level traction inverter based drive with IPMSM is carried out. Both the speed and torque

transients are performed in simulation and experimental studies. The maximum capacitor voltage difference observed is around 4.0 % of the total DC-link voltage at full load. Four different control strategies are proposed to keep the DC-link capacitor voltages balanced in the field weakening region. The proposed control strategies do not use any of the medium voltage vectors, which contribute to the larger capacitor voltage deviation in the field weakening region at modulation index of one. Although the proposed strategy makes the phase voltage harmonic distortion higher than the conventional one, it keeps the capacitor voltages balanced at any leading power factor condition. It also helps to save the power switches from high voltage break down, due to capacitor voltage fluctuations. Detailed simulation and experimental results show the effectiveness of the proposed control strategy.

Chapter 7. CONCLUSIONS AND FUTURE WORK

7.1. Conclusions

Compared to the two-level inverter three-level inverter, considerably reduces the total inverter loss and harmonic distortion at the output voltage and current waveforms. The reduced harmonic distortion in turn helps to reduce the size of output sine filter and other magnetic components to reduce the system size and helps to increase the system power density. However, three-level inverter has a potential problem of DC-link capacitor voltage balancing. Detailed literature survey is carried out to shows the available DC-link voltage balancing strategies and their associated problem for electric vehicle applications.

A space vector (SVPWM) based DC-link voltage balancing strategy is proposed with reduced switching vector per switching sequence and detailed simulation and experimental studies are also performed with a surface and interior permanent magnet synchronous machines. Results showed the required steady state and transient stability with the proposed scheme. The proposed strategy is further modified with current direction taken into consideration, which affects the DC-link voltage balancing ability at lower factor based systems.

To reduce the system computational time and complexity, carrier based strategies are also developed and compared with the conventional carrier based strategies. The proposed strategy can reduce the switching losses by eliminating the common switching interval proposed by the conventional strategies. Moreover, a hybrid carrier based PWM and DPWM strategies are also proposed to eliminate the problem with DC-offset voltage addition to keep the NPP fluctuation low. Compared to the continuous HPWM, DPWM strategy reduces the switching losses and shows almost the similar loss distribution pattern like the earlier proposed SVPWM based strategy.

Detailed analytical derivation of the switching and conduction losses for two- and three-level inverters are also carrier out and results are then compared with the results obtained from the simulation based studies. Results are quite similar. Total voltage and current harmonic distortion, capacitor voltage deviation and torque ripples are also compared.

To reduce the NPP fluctuation for IPMSM in at leading power factor condition, four control strategies are proposed. All These proposed control strategies do not take any medium voltage vectors to generate the reference voltage vector, which helps to reduce the capacitor voltage deviation at neutral point.

7.2. Future Work

As a continuation of this project following topics can be considered.

7.2.1. Regenerative Breaking

Regenerative breaking is an important point to be considered in terms of electric vehicle perspective. When the vehicle goes downhill or when the driver brakes, the energy stored in the machine can be feed back to the battery to charge them and it also helps to increase the whole drive train efficiency. As for two-level inverters regenerative breakings are discussed in literature, for three-level inverter it is not a straight forward approach, because of the split capacitor voltages.

7.2.2. Common Mode Voltage (CMV) Reduction

Common mode voltage is a crucial problem for all electric drive train. It is basically the potential difference between the common start point of the stator winding and ground. Due to the stray capacitances present in the windings and the bearing, leakage current can flow very easily and damage the bearing. In this thesis CMV problem is not considered and as a future work it could be included. It would also be interesting to see how a control strategy can take care of DC-link voltage balancing, reduce the switching losses and also be able to reduce the CMV at the same time.

7.2.3. Equal Power Sharing between All Power Switches

From the analytical and simulation based studies shown in chapter 5, it can be observed that, the conduction losses for inner IGBT switches (T_{A2}, T_{A3}) are higher than the outer switches and switching losses for out switches (T_{A1}, T_{A4}) are more than the inner switching devices. This unequal loss distribution can overstress one switch compared to the other, which leads to overrating of that particular switch to operate them in safe operating region. Control strategies can be proposed to distribute the power losses equally in all power switches and can also be able to keep the neutral point balanced for all transient load torque variations.

7.2.4. Replacement of Higher Switching Loss Based Devices with Wide Band Gap materials

As wide band gap material based devices like SiC, reduces the switching losses considerably compared to the Si based switches, these switches (SiC) can be used for outer IGBT's or neutral point clamped diodes to reduce the switching losses. A case study can be

done to see the reduction in total inverter loss and their effect on system efficiency and the increase in total system cost.

7.2.5. Optimum Use of Medium Voltage Vectors with field Weakening Region for IPMSM

In the proposed control strategies shown in chapter 6, to reduce the NPP fluctuation in field weakening region for IPMSM, medium voltage vectors are completely removed. It reduces the NPP fluctuation considerably; however, phase voltage harmonic distortion goes bit higher. A study can be done, to see an optimum value of medium voltage vector which can help to reduce the harmonic distortion compared to the proposed scheme and at the same time keeps the DC-link capacitor voltage deviation below the maximum tolerance band.

References

[1] D. Schneider, "Plug-ins proliferates," Spectrum, *IEEE*, vol. 49, no. 1, pp. 36-37, Jan. 2012.

[2] K. Rajashekara, "Present Status and Future Trends in Electric Vehicle Propulsion Technologies," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 1, no. 1, pp. 3-10, Mar. 2013.

[3] Z. Wang and K. T. Chau, "Design, analysis, and experimentation of chaotic permanent magnet DC-motor drives for electric compaction," *IEEE Trans. on Circuit and Systems-II: Express Briefs*, vol. 56, no. 3, pp. 245-249, Mar. 2009.

[4] J. M. Knezevic, "Low-cost low-resolution sensor less positioning of DC-motor drives for vehicle auxiliary applications," *IEEE Trans. on Vehicular Technology*, vol. 62, no. 9, pp. 4328-4335, Nov. 2013.

[5] Y. A. Rady and I. Mohamed, "A newly designed instantaneous-torque control of direct-drive PMSM servo actuator with improved torque estimation and control characteristics," *IEEE Trans. on Industrial Electronics*, vol. 54, no. 5, pp. 2864-2873, Oct. 2007.

[6] M. Preindl and S. Bolognani, "Model predictive direct torque control with finite control set for PMSM drive systems, part 2: field weakening operation," *IEEE Trans. on Industrial Informatics*, vol. 9, no. 2, pp. 648-657, May 2013.

[7] A. Sarikhani, O. A. Mohammed, "Demagnetization control for reliable flux weakening control in PM synchronous machine," *IEEE Trans. on Energy Conversion*, vol. 27, no. 4, pp. 1046-1055, Dec. 2012.

[8] A. Kolli, O. Bethoux, A. D. Bernardinis, E. Laboure and G. Coquery, "Space-vector PWM control sysnthesis for an H-bridge drive in electric vehicles," *IEEE Trans. on Vehicular Technology*, vol. 62, no. 6, pp. 2441-2451, July 2013.

[9] C. Choi and W. Lee, "Analysis and compensation of time delay effects in hardware-in-loop simulation for automotive PMSM drive system," *IEEE Trans. on Industrial Electronics*, vol. 59, no. 9, pp. 3403-3410, Sept. 2012.

[10] K. Jezernil, R. Horbat and M. Curkovic, "A switching control strategy for the reduction of torque ripple for PMSM," *IEEE Trans. on Industrial Informatics*, vol. 9, no. 3, pp. 1272-1279, May 2013.

[11] Y. Inoue, S. Morimoto and M. Sanada, "Control method suitable for direct-torque-control-based motor drive system satisfying voltage and current limitation," *IEEE Trans. on Industry Applications*, vol. 48, no. 3, pp. 970-976, May 2012.

[12] S. Y. Kim, C. Choi, K. Lee and W. Lee, “An improved rotor position estimation with vector-tracking observer in PMSM drives with low-resolution hall-effect sensors,” *IEEE Trans. on Industrial Electronics*, vol. 58, no. 9, pp. 4078-4086, Sept. 2011.

[13] K. Sun, Q. Wei, L. Huang and K. Matsuse, “An over modulation method for PMSM-inverter-fed IPMSM drive with single current sensor,” *IEEE Trans. on Industrial Electronics*, vol. 57, no. 10, pp. 3395-3404, Oct. 2010.

[14] J. A. Firouzjaee, "Remediation Strategies of Shaft and Common Mode Voltages in Adjustable speed Drive Systems," School of Engineering Systems, Queensland University of Technology, Queensland, Australia, Doctor in Philosophy Thesis August 2010.

[15] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, “Multilevel voltage-source-converter topologies for industrial medium-voltage drives,” *IEEE Trans. on Industrial Electronics*, vol. 54, no.6, pp. 2930-2945, Dec. 2007.

[16] L. Clotea, A. Forcos, C. Marinescu, and M. Georgescu, “Power loss analysis of two-level and three-level neutral point clamped inverters for a wind pump storage system,” in *Proc. on IEEE 12th Int. Conf. on Optimization of Electrical and Electronic Equipment*, Brasov, Romania, May 2010, pp. 1174-1179.

[17] R. Macke, “Multilevel NPC inverter for low-voltage applications,” in *Proc. IEEE 14th European Conf. on Power Electronics Applications,* Birmingham, UK, Sept. 2011, pp. 1-10.

[18] Z. Chen, L. Yuan, and Z. Zhao, “Power losses in 2- and three-level three-phase photovoltaic inverters equipped with IGBT’s,” in *Proc. IEEE 15th Int. Conf. on Electrical Machines and Systems,* Sapporo, Japan, Oct. 2012, pp. 1-6.

[19] R. Teichmann and S. Bernet, “A comparison of three-level converter versus two-level converters for low-voltage drives, traction, and utility applications,” *IEEE Trans. on Industry Applications*, vol. 41, no. 3, pp. 855-865, May 2005.

[20] K. H. Kim, I. C. Baik, and M. J. Youn, “Simple and robust digital current control scheme of permanent magnet synchronous motor using time delay control approach,” *IEEE Electronics letter, vol. 35, no. 12,* pp. 1027-1028, April. 1999.

[21] B. J. Kang and C. M. Liaw, “A robust hysteresis current controlled PWM inverter for linear PWM driven magnetic suspended positioning system,” *IEEE Trans. on Industrial Electronics*, vol. 48, no. 5, pp. 956-967, May 2001.

[22] K. H. Kim, H. S. Kim, and M. J. Youn, "An improved stationery frame based current control scheme for a permanent magnet synchronous motor," *IEEE Trans. on Industrial Electronics*, vol. 50, no. 5, pp. 1065-1068, Oct. 2003.

[23] C. Allen and P. Pillay, "TMS320 design for vector and current control of AC motor drives," *IEEE Electronics Letter*, vol. 28, no.23, Nov. 1992.

[24] P. Pillay and R. Krishnan, "Modelling, simulation, and analysis of permanent-magnet motor drives, part I: The permanent-magnet synchronous motor drives," *IEEE Trans. on Industry Applications*, vol. 25, no. 2, pp. 265-273, April. 1989.

[25] A. Kwasinski, P. T. Krein, and P. L. Chapman, "Time domain comparison of pulse-width modulation scheme," *IEEE Power Electronics Letter*, vol. 1, no. 3, pp. 64-68, Sept. 2003.

[26] Z. Shu, J. Tang, Y. Guo, and J. Lian, "An efficient SVPWM algorithm with low computational overhead for three-phase inverters," *IEEE Trans. on Power Electronics*, vol. 22, no. 5, pp. 1797-1805, Sept. 2007.

[27] M. A. Jabbar, A.M. Khambadkone, and Y. Zhang, "Space-vector modulation in a two-phase induction motor drive for constant-power operation," *IEEE Trans. on Industrial Electronics*, vol. 51, no. 5, pp. 1081–1088, Oct.2004

[28] S. R. Bowes and L. Yen-Shin, "The relationship between space-vector modulation and regular-sampled PWM," *IEEE Trans. on Industrial Electronics*, vol. 44, no. 5, pp. 670–679, Oct. 1997.

[29] Z. Keliang and W. Danwei, "Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis," *IEEE Trans. on Industrial Electronics*, vol. 49, no. 1, pp. 186–196, Feb. 2002.

[30] A. K. Gupta and A. M. Khambadkone, "A space vector pwm scheme for multilevel inverters based on two-level space vector pwm," *IEEE Trans. on Industrial Electronics*, vol. 53, no. 5, pp. 1631–1639, Oct. 2006.

[31] W. Sanmin, W. Bin, L. Fahai, and L. Congwei, "A general space vector PWM control algorithm for multilevel inverters," in *Proc. Appl. Power Electronics. Conf. Expo.*, 2003, vol. 1, pp. 562–568.

[32] K. Zhou, and D. Wang, "Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis," *IEEE Trans. on Industrial Electronics*, vol. 49, no. 1, pp. 186-196, Feb. 2002.

[33] A. M. Hava, R. J. Kerkman and T. A. Lipo, "Simple analytical and graphical methods for carrier-based PWM-VSI drive," *IEEE Trans. on Power Electronics*, vol. 14, no. 1, pp. 49-61, Jan.1999.

[34] V. Blasko, “Analysis of a hybrid PWM based on modified space-vector and triangle-comparison methods,” *IEEE Trans. on Industry Applications*, vol. 33, no. 3, pp. 756-764, Feb.1997.

[35] T. Bruckner, and D. G. Holmes, “Optimal pulse-width modulation for three-level inverters,” *IEEE Trans. on Power Electronics*, vol. 20, no. 1, pp. 82-89, Jan. 2005.

[36] M. Sushama, and A. J. Laxmi, “Generalized PWM algorithm for VSI feed induction motor drives based on unique zero sequence signal over the entire modulation region,” in *Proc. IEEE India Conf.*, Hyderabad, India, Nov.2011, pp. 1-7.

[37] Y. Wu, M. A. Shafi, A. M. Knight and R. A. McMahon, “Comparison of the effects of continuous and discontinuous PWM scheme on power losses of voltage-sourced inverters for induction motor drives,” *IEEE Trans. on Power Electronics*, vol. 26, no. 1, pp. 182-191, Jan. 2011.

[38] O. R. Solomon, andP. Famouriand, “A novel approach for evaluating performance of discontinuous pulse width modulation scheme for three phase voltage source inverter,” in *Proc. IEEE International Symposium on Industrial Electronics*, Montreal, QC, Canada, July2006, pp. 870-875.

[39] O. Ojo, “The generalized discontinuous PWM scheme for three-phase voltage source inverters,” *IEEE Trans. on Industrial Electronics*, vol. 51, no. 6, pp. 1280-1289, Jan. 2004.

[40] A. Nabae, I. Takahashi, and H. Akagi, “A new neutral-point-clamped PWM inverter,” *IEEE Trans. on Industry Applications*, vol. IA-17, pp. 518-523, Sept. 1981.

[41] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, “Medium-voltage multilevel converters-state of the art, challenges, and requirements in industrial applications,” *IEEE Trans. on Industrial Electronics*, vol. 57, no. 8, pp. 2581-2596, Aug. 2010.

[42] Z. Du, L. M. Tolbert, B. Ozpineci, and J. N. Chiasson, “Fundamental frequency switching strategies of a seven-level hybrid cascaded H-bridge multilevel inverter,” *IEEE Trans. on Power Electronics*, vol. 24, no. 1, pp. 25-33, Jan. 2009.

[43] F. Khoucha, S. M. Lagoun, K. Marouani, A. Kheloui, and M. E. H. Benbouzid, “Hybrid cascaded H-bridge multilevel inverter induction-motor-drive direct torque control for automotive applications,” *IEEE Trans. on Industrial Electronics*, vol. 57, no. 3, pp. 892-899, Mar. 2010.

[44] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, “Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems,” *IEEE Trans. on Industrial Electronics*, vol. 56, no.11, pp. 4399-4406, Nov. 2009.

[45] Z. Du, B. Ozpineci, L. M. Tolbert, and J. N. Chiasson, "DC-AC cascaded H-bridge multilevel boost inverter with no inductors for electric/hybrid electric vehicle applications," *IEEE Trans. on Industry Applications*, vol. 45, no.3, pp. 963-970, June 2009.

[46] N. A. Rahim, M. F. Elias, and W. P. Hew, "Transistor-clamped H-bridge based cascaded multilevel inverter with new method of capacitor voltage balancing," *IEEE Trans. on Industrial Electronics*, vol. 60, no.8, pp. 2943-2956, Aug. 2013.

[47] P. Samuel, R. Gupta, and D. Chandra, "Grid interface of wind power with large split-winding alternator using cascaded multilevel inverter," *IEEE Trans. on Energy Conversion*, vol. 26, no.1, pp. 299-309, Mar. 2011.

[48] T. A. Meynard, H. Foch, "Multi-Level Conversion: High Voltage Choppers and Voltage-Source Inverters," *IEEE Power Electronics Specialists Conference*, 1992, pp. 397-403.

[49] A. Shukla, A. ghosh, and A. Joshi, "Flying-capacitor-based chopper circuit for DC capacitor voltage balancing in diode-clamped multilevel inverter," *IEEE Trans. on Industrial Electronics*, vol. 57, no.7, pp. 2249-2261, July 2010.

[50] J. Mathew, P. P. Rajeevan, K. Mathew, N. A. Azeez, and K. Gopakumar, "A multilevel inverter scheme with dodecagonal voltage space vector based on flying capacitor topology for induction motor drives," *IEEE Trans. on Power Electronics*, vol. 28, no.1, pp. 516-525, Jan. 2013.

[51] A. Shukla, A. Ghosh, and A. Joshi, "Improved multilevel hysteresis current regulation and capacitor balancing scheme for flying capacitor multilevel inverter," *IEEE Trans. on Power Electronics*, vol. 23, no.2, pp. 518-529, Mar. 2008.

[52] D. W. Kang, B. K. Lee, J. H. Jeon, T. J. Kim, and D. S. Hyum, "A symmetric carrier technique of CRPWM for voltage balance method for flying-capacitor multilevel inverter," *IEEE Trans. on Industrial Electronics*, vol. 52, no.3, pp. 879-888, June 2005.

[53] M. F. Escalante, J. C. Vannier, and A. Arzande, "Flying capacitor multilevel inverters and DTC motor drive application," *IEEE Trans. on Industrial Electronics*, vol. 49, no. 4, pp. 809-815, Aug. 2002.

[54] J. Huang and K. A. Corzine, "Extended operation of flying capacitor multilevel inverters," *IEEE Trans. on Power Electronics*, vol. 21, no.1, pp. 140-147, Jan. 2006.

[55] K. Cai, B. Liu, Z. Xu, Y. Kang and S. Cheng, "General analysis on imbalanced voltage of DC capacitors in NPC three-level inverter," in *Proc. IEEE Int. Conf. on Electrical Machines and Systems*, Beijing, China, Aug. 2011, pp. 1-6.

[56] B. P. Schmitt and R. Sommer, "Retrofit of fixed induction motors with medium voltage drive converters using NPC three-level inverter high voltage IGBT based topology," in *Proc. IEEE International Symposium on Industrial Electronics*, Pusan, Korea, June 2001, vol. 2, pp. 746-751.

[57] F. Wang, "Multilevel PWM VSIs," *IEEE Industry Applications Magazine*, vol. 10, no. pp. 51-58, Aug. 2004.

[58] J. Pou, R. Pindado, D. Boroyevich, and P. Rodríguez, "Limits of the neutral-point balance in back-to-back-connected three-level converters," *IEEE Trans. on Power Electronics*, vol. 19, no. 3, pp. 722-731, May 2004.

[59] R. C. Portillo, M. A. Martín Prats, J. I. León, J. A. Sánchez, J. M. Carrasco, E. Galván, and L. Garcia Franquelo, "Modeling strategy for back-to-back three-level converters applied to high-power wind turbines," *IEEE Trans. on Ind. Electron*ics, vol. 53, no. 5, pp. 1483–1491, Oct. 2006.

[60] J. Rodriguez, S. Bernet, P. K. Steimer and I. E. Lizama, "Survey on neutral-point-clamped inverters," *IEEE Trans. on Industrial Electronics*, vol. 57, no.7, pp. 2219-2230, July 2010.

[61] A. Maheshwari, and K. D. T. Ngo, "Synthesis of six-step pulse width-modulated waveform with selective harmonic elimination," *IEEE Trans. on Power Electronics*, vol. 8, no. 4, pp. 554-561, Oct. 1993.

[62] W. Fei, Y. Zhang, and X. Ruan, "Solving the SHEPWM nonlinear equations for three-level voltage inverter based on computed initial value," in *Proc. on IEEE Appl. Power Electron. Conf. Expo.,* Anaheim, California, USA, Mar. 2007, pp. 1084-1088.

[63] Y. Zhang, Z. Zhao, and J. Zhu, "A hybrid PWM applied to high-power three-level inverter-fed induction-motor drives," *IEEE Trans. on Ind. Electronics*, vol. 58, no. 8, pp. 3409-3420, Aug. 2011.

[64] Z. Zhao, Y. Zhang, H. Gao, L. Yuan, and T. Lu, "Hybrid selective harmonic elimination PWM for common-mode voltage reduction in three-level neutral-point-clamped inverters for variable speed induction drives," *IEEE Trans. on Power Electronics*, vol. 27, no. 3, pp. 1152-1158, Mar. 2012.

[65] J. K. Steinke, "Switching frequency optimal PWM control of a three-level inverter," *IEEE Trans. on Power Electronics,* vol. 7, no. 3, pp. 487-496, July 1992.

[66] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters," in *Proc. on IEEE Industry Applications Society Annual Meeting*, Toronto, Canada, Oct. 1993, pp. 965-970.

[67] R. K. Behera, T. V. Dixit, and S. P. Das, "Analysis of experimental investigation of various carrier-based modulation schemes for three-level neutral point clamped inverter-fed induction motor drive," in *Proc. IEEE Power Electronics, Drives and Energy Systems Conf.,* New Delhi, India, Dec. 2006*,* pp. 1-6.

[68] R. Rojas, T. Ohnishi, and T. Suzuki, "An improved voltage vector control method for neutral-point-clamped inverters," *IEEE Trans. on Power Electronics* , vol. 10, no. 6, pp. 666-672, Nov. 1995.

[69] C. Newton and M. Sumner, "Neutral point control for multi-level inverters: Theory, design and operational limitations," in *Proc. on IEEE Industry Applications Society Annual Meeting*, New Orleans, LA, Oct. 1997, pp. 1336-1343.

[70] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, and D. Boroyevich, "A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter," *IEEE Trans. on Power Electronics* , vol. 27, no. 2, pp. 642-651, Feb. 2012.

[71] J. Pou, J. Zaragoza, P. Rodriguez, S. Ceballos, V. Sala, R. Burgos, and D. Boroyevich, "Fast-processing modulation strategy for the neutral-point clamped converter with total elimination of the low-frequency voltage oscillations in the neutral point," *IEEE Trans. on Industrial Electronics*, vol. 54, no. 4, pp. 2288-2299, Aug. 2007.

[72] R. Maheshwari, S. M. Nielsen, and S. B. Monge, "Neutral-point current modeling and control for neutral-point clamped three-level converter drive with small dc-link capacitors," in *Proc. IEEE Energy Conversion Congress and Expo.*, Phoenix, AZ, Sept. 2011, pp. 2087-2094.

[73] R. Maheshwari, S. Munk-Nielsen, and S. Busquets-Monge, "Design of neutral point voltage controller of a three-level NPC inverter with small DC link capacitor," *IEEE Trans. on Industrial Electronics*, vol. 60, no. 5, pp. 1861–1871, May 2013.

[74] A. Bendre, G. Venkataramanan, D. Rosene, and V. Srinivasan, "Modeling and design of a neutral-point voltage regulator for a three-level diode-clamped inverter using multiple-carrier modulation," *IEEE Trans. on Industrial Electronics*, vol. 53, no. 3, pp. 718-726, June. 2006.

[75] P. Chaturvedi, S. Jain, and P. Agarwal, "Carrier-based neutral point potential regulator with reduced switching losses for three-level diode-clamped inverter," *IEEE Trans. on Industrial Electronics*, vol. 61, no. 2, pp. 613-624, Feb. 2014.

[76] X. Lin, S. Gao, J. Li, H. Lei, and Y. Kang, "A new control strategy to balance neutral-point voltage in three-level NPC inverter," in *Proc. IEEE Power Electronics and ECCE Asia,* Jeju, South Coria, June 2011, pp. 2593-2597.

[77] Q. Song, W. Liu, Q. Yu, X. Xie, and Z. Wang, "A neutral point potential balancing algorithm for three-level NPC inverters using analytically injected zero sequence voltage," in *Proc*. *IEEE APEC*, Feb. 2003, vol. 1, pp. 228-233.

[78] K. R. M. N. Ratyanake, Y. Murai, and T.Watanabe, "Novel PWM scheme to control neutral point voltage in three-level voltage source inverter," in *Proc. IEEE Industry Applications Society Annu. Meeting*, Phoenix, AZ, 1999, vol. 3, pp. 1950–1955.

[79] M. K. Mishra, A. Joshi, and A. Ghosh, "Control schemes for equalization of capacitor voltage in neutral clamped shunt compensator," *IEEE Trans. on Power Delivery*, vol. 18, no. 2, pp. 538–544, April 2003.

[80] S. K. Lim, J. H. Kim, and K. Nam, "A DC-link voltage balancing algorithm for 3-level converter using the zero sequence current," in *Proc. IEEE Power Electronics Spec. Conf. (PESC)*, Jun. 27–Jul. 1, 1999, vol. 2, pp. 1083–1088.

[81] R. M. Tallam, R. Naik, T. A. Nondahl, "A carrier-based PWM scheme for neutral-point voltage balancing in three-level inverters," *IEEE Trans. on Industry Applications*, vol. 41, no. 6, pp. 1734-1743, Dec. 2005.

[82] J. Jaragoza, J. Pou, S. Ceballos, E. Robles, C. Jaen, and M. Corbalan, "Voltage-balance compensator for a carrier-based modulation in the neutral-point-clamped converter," *IEEE Trans. on Industrial Electronics*, vol. 56, no. 2, pp. 305-314, Feb. 2009.

[83] W. Song, X. Feng, and K. M. Smedley, "A carrier-based PWM strategy with the offset voltage injection for single-phase three-level neutral-point-clamped converters," *IEEE Trans. on Power Electronics*, vol. 28, no. 3, pp. 1083-1095, Mar. 2013.

[84] W. Srirattanawichaikul and Y. Kumsuwan, "A carrier based PWM strategy for three-level neutral-point-clamped voltage source inverters," in *Proc. 9th IEEE Int. Conf. on Power Electronics and Drives Systems*, Singapore, Dec. 2011, pp. 948-951.

[85] J. H. Kim and S. K. Sul, "Carrier based pulse width modulation for three-level inverters: neutral point potential and output voltage distortion," in *Proc. IEEE 13th Int. Conf. on Systems, Signals & Devices,* Hammamet, Tunisia, Mar. 2013, pp. 1-7.

[86] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. on Industry Application*, vol. 37, no. 2, pp. 637-641, March 2001.

[87] Y. Katsutoshi and M. H. Ahmet, "A novel neutral point potential stabilization technique using the information of output current polarities and voltage vector," *IEEE Trans. on Industry Applications*, vol. 38, no. 6, pp. 1572-1580, Nov. 2002.

[88] Y. H. Ko, B. G. Park, R. Y. Kim, D. S. Hyun, and H. J. Jung, "A simple space vector PWM scheme with neutral point balancing for three-level neutral point clamped inverter," in *Proc. IEEE Industrial Application Society Annu. Meeting,* Orlando, FL, USA, Oct. 2011, pp. 1-6.

[89] H. R. Pinkymol, A. I. Maswood, and A. Venkataraman, "Space vector based field oriented control of permanent magnet synchronous motor with a 3-level inverter scheme," in *Proc. IEEE Transportation Electrification Conference and Expo.*, Detroit. MI, June. 2013, pp. 1-6.

[90] K. Gupta and M. Khambadkone, "A simple space vector PWM scheme to operate a three-level NPC inverter at high modulation index including over modulation region, with neutral point balancing," *IEEE Trans. on Industry Applications*, vol. 43, no. 3, pp. 751–760, May/Jun. 2007.

[91] J. Pou, R. Pindado, D. Boroyevich, and P. Rodriguez, "Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter," *IEEE Trans. on Industrial Electronics*, vol. 52, no. 6, pp. 1582-1588, Dec. 2005.

[92] R. Krishna, E. S. Deepak, S. K. Kottayil, and M. Leijon, "Space vector modulation method to balance the neutral voltage for a three level inverter," in *Proc. IEEE Power Electronics, Drives and Energy Systems Conf.,* New Delhi, India, Dec. 2010, pp. 1-6.

[93] S. B. Monge, J. Bordonau, D. Boroyevich, and S. Somavilla, "The nearest three virtual space vector PWM-a modulation for the comprehensive neutral point balancing in the three-level NPC inverter," *IEEE Power Electronics Letters*, vol. 2, no. 1, pp. 11-15, March 2004.

[94] W. X. Song, Y. Han, Q. Ai, and C. Chen, "A novel space vector modulation method of three-level inverter based on the synthesized middle space vectors," in *Proc. IEEE Asia Pacific Conf. on Circuits and systems,* Macao, China, Dec. 2008, pp. 1020-1028.

[95] A. Lewicki, Z. Krzeminski, and H. Abu-Rub, "Space-Vector pulse width modulation for three-level NPC converter with the neutral point voltage control," *IEEE Trans. on Industrial Electronics*, vol. 58, no. 11, pp. 5076-5086, Nov. 2011.

[96] S. B. Monge, J. D. Ortega, J. Bordonau, J. A. Beristain, and J. Rocabert, "Closed-loop control of a three-phase neutral-point-clamped inverter using an optimized virtual-vector-

based pulse width modulation," *IEEE Trans. on Industry Electronics*, vol. 55, no. 5, pp. 2061-2071, May 2008.

[97] G. I. Orfanoudakis, A. Yuratich, and S. M. Sharkh, "Nearest-vector modulation strategies with minimum amplitude of low-frequency neutral-point voltage oscillations for the neutral-point-clamped converter," *IEEE Trans. on Power Electronics,* vol. 28, no. 10, pp. 4485-4499, Oct. 2013.

[98] J. Shen, S. Schroder, B. Duro, and R. Roesner, "A neutral point balancing control for three-level inverter with full power factor range and low distortion," *IEEE Trans. on Industry Applications*, vol. 49, no. 1, pp. 138-148, Feb. 2013.

[99] C. Wang and Y. Li, "Analysis and calculation of zero-sequence voltage considering neutral-point potential balancing in three-level NPC converters," *IEEE Trans. on Industrial Electronics*, vol. 57, no. 7, pp. 2262-2271, July 2010.

[100] Y. S. Lai, Y. K. Chou, and S. Y. Pai, "Simple PWM technique of capacitor voltage balance for three-level inverter with DC-link voltage sensor only," in *Proc. Annual Conf. of the Industrial Electronics Society*, Taipei, Taiwan, Nov. 2007, pp. 1749-1754.

[101] J. H. Seo and C. H. Choi, " Compensation for the neutral-point potential variation in three-level space vector PWM," in *Proc. IEEE Applied Power Electronics Conf. and Exposition*, Anaheim, CA. USA, Mar. 2001, vol. 2, pp. 1135-1140.

[102] P. M. Meshram, D. Hanote, and M. M. Renge, "A simplified space-vector PWM for three level inverters applied to passive and motor load," in *Proc. IEEE International Conf. on Industrial Electronics and Applications*, Xi'an, China, May 2009*,* pp. 3383-3393.

[103] O. Bouhali, B. Francois, E. M. Berkouk, and C. Saudemont, " DC link capacitor voltage balancing in a three-phase diode clamped inverter controlled by a direct space vector of line-to-line voltages," *IEEE Trans. on Power Electronics*, vol. 22, no. 5, pp. 1636-1648, Feb. 2007.

[104] D. Boroyevich, J. Pou, and R. Pindado, "Effects of imbalanced and nonlinear loads on the voltage balance of a neutral point clamped inverter," in *Proc. IEEE PESC*, 2003, pp. 53–58.

[105] S. Das and G. Narayanam, "Novel switching sequences for a space-vector-modulated three-level inverter," *IEEE Trans. on Industrial Electron*ics, vol. 59, no. 3, pp. 1477–1487, Mar. 2012.

[106] D. W. Feng, B. Wu, S. Wei, and D. Xu, "Space vector modulation for neutral point clamped multilevel inverter with even order harmonic elimination," in *Proc. IEEE*

Canadian Conf. on Electrical and Computer Engineering, Niagara Falls, Ontario, Canada, May. 2004*,* pp. 1471-1475.

[107] U. M. Choi, K. B. Lee, and F. Blaabjerg, "Method to minimize the low-frequency neutral-point voltage oscillations with time-offset injection for neutral-point-clamped inverters," in *Proc. IEEE Energy Conversion Congress and Exposition,* Denver, CO, USA, Sept. 2013*,* pp. 4022-4029.

[108] C. Xia, H. Shao, Y. Zhang, and X. He, "Adjustable proportional hybrid SVPWM strategy for neutral-point-clamped three-level inverters," *IEEE Trans. on Industrial Electronics*, vol. 60, no. 10, pp. 4234-4242, Oct. 2013.

[109] W. D. Jiang, S. W. Du, L. C. Chang, Y. Zhang, and Q. Zhao, "Hybrid PWM strategy of SVPWM and VSVPWM for NPC three-level voltage-source inverter," *IEEE Trans. on Power Electronics*, vol. 25, no. 10, pp. 2607–2619, Oct. 2010.

[110] H. Zhang, S. J. Finney, A. Massoud, and B. W. Williams, "An SVM Algorithm to balance the capacitor voltages of the three-level NPC active power filter," *IEEE Trans. on Power Electronics*, vol. 23, no. 6, pp. 2694-2702, Nov. 2008.

[111] H. Alloui, A. Berkani, and H. Rezine, "A three level NPC inverter with neutral point voltage balancing for induction motors direct torque control," in *Proc. IEEE XIX Int. Conf. on Electrical Machines*, June. 2010*,* pp. 1-6.

[112] H. J. Kim, H. D. Lee, and S. K. Sul, "A new PWM strategy for common mode voltage reduction in neutral-point clamped inverter-fed AC motor drives," in *Proc. IEEE Industry Application Conf.,* Rome, Oct. 2000*,* pp. 2032-2036.

[113] A. Videt, P. L. Moigne, N. Idir, P. Baudesson, and X. Cimetiere, "A new carrier-based PWM providing common-mode-current reduction and DC-bus balancing for three-level inverters," *IEEE Trans. on Industrial Electronics*, vol. 54, no. 6, pp. 3001-3011, Dec. 2007.

[114] K. H. Bhalodi and P. Agarwal, "Space vector modulation with DC-link voltage balancing control for three-level inverters," in *Proc. IEEE Int. Conf. on Power Electronic, Drives and Energy Systems,* New Delhi, India, Dec. 2006*,* pp. 1-6.

[115] J. Shen, S. Schroder, R. Rosner, and S. E. Barbari, "A comprehensive study of neutral-point self-balancing effect in neutral-point-clamped three-level inverters," *IEEE Trans. on Power Electronics*, vol. 26, no. 11, pp. 3084-3095, Nov. 2011.

[116] T. Ghennam, E. M. Berkouk, and B. Francois, "A novel space-vector current control based on circular hyteresis areas of a three-phase neutral-point-clamped inverter," *IEEE Trans. on Industrial Electronics*, vol. 57, no. 8, pp. 2669-2678, Aug. 2010.

[117] R. Davoodnezhad, D. G. Holmes, B. P. McGrath, "Three-level hysteresis current regulation for a three phase neutral point clamped inverter," in *Proc. IEEE Power Electronics and Motion Control Conf.,* Orlando, Novi Sad, Serbia, Sept. 2012*,* pp. 1-6.

[118] G. S. Perantzakis, F. H. Xepapes, S. A. Papathanassiou, and S. N. Manias, "A predictive current control technique for three-level NPC voltage source Inverters," in *Proc. IEEE Power Electronics Specialists Conf.*, Recife, Brazil, June 2005*,* pp. 1241-1246.

[119] A. Bellini, G. Figalli, S. Bifaretti, and S. Costantini, "Experimental development of a hysteresis modulated NPC inverter," in *Proc. IEEE Conf. on Control Applications*, Rome, Italy, Sept. 2003*,* pp. 588-593.

[120] K. A. Corzine, "A hysteresis current-regulated control for multi-level drives," *IEEE Trans. on Energy Conversion*, vol. 15, no. 2, pp. 169-175, June. 2000.

[121] L. Ning, W. Yue, J. Y. Wei, Z. Changsong, and W. Zhaoan, "The control region of hysteresis control for neutral-point voltage balancing of NPC three-level inverters," in *Proc. IEEE Int. Power Electronics Conf.*, Sapporo, Japan, June 2010*,* pp. 209-212.

[122] J. C. Zabalza, P.L. Moreno, D. Madariaga, G. Calvo, and M. A. Rodriguez, "Voltage balancing control in 3-level neutral-point clamped inverters using triangular carrier PWM modulation for FACTS applications," *IEEE Trans. on Power Electronics*, vol. 28, no. 10, pp. 4473-4484, Oct. 2013.

[123] J. Li, A. Q. Huang, Z. Liang and S. Bhattacharya, "Analysis and design of active NPC (ANPC) inverters for fault-tolerant operation of high-power electrical drives," *IEEE Trans. on Power Electronics*, vol. 27, no. 2, pp. 519-533, Feb. 2012.

[124] J. Li, S. Bhattacharya, and A. Q. Huang, "A new nine-level active NPC (ANPC) converter for grid connection of large wind turbines for distributed generation," *IEEE Trans. on Power Electronics*, vol. 26, no. 3, pp. 961-971, Mar. 2011.

[125] H. J. Kim, D. W. Jung and S. K. Sul, "A new discontinuous PWM strategy of neutral-point clamped inverter," in *Proc. IEEE Industrial Applications Society Annual Meeting*, Rome, Italy, Oct.2000*,* pp. 2017-2023.

[126] A. Pevere, and R. Petrella, "Discontinuous hybrid modulation technique for three-phase three-level neutral point clamped inverters," in *Proc. IEEE Energy Conversion Congress and Exposition,* Denver, USA, Sept.2013*,* pp. 3992-3999.

[127] C. Ma, T. Kim, D. Kang and D. Hyun, "A simple control strategy for balancing the DC-link voltage of neutral-point-clamped inverter at low modulation index," in *Proc. IEEE Industrial Electronics Society Annual Conf.,* Virginia, USA, Oct.2003*,* pp. 2167-2172.

[128] Ui-Min. Choi, H. H. Lee, and K. B. Lee, "Simple neutral-point voltage control for three-level inverters using a discontinuous pulse width modulation," *IEEE Trans. on Energy Conversion*, vol. 28, no. 2, pp. 997-1004, June 2013.

[129] F. Wang, "Sine-triangle versus space-vector modulation for three-level PWM voltage-source inverters," *IEEE Trans. on Industry Applications*, vol. 38, no. 2, pp. 500-506, April. 2002.

[130] N. V. Nho and M. J. Youn, "Comprehensive study on space vector-pwm and carrier-based-pwm correlation in multilevel inverters," *Proc. Inst. Elect. Eng.*, vol. 153, no. 1, pp. 149–158, 2006.

[131] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverter," *IEEE Trans. on Power Electronics,* vol. 15, no. 2, pp. 535-541, March 2000.

[132] O. Dordevic, M. Jones, and E. Levi, "A comparison of carrier-based and space vector PWM techniques for three-level five-phase voltage source inverters," *IEEE Trans. on Industrial Informatics*, vol. 9, no. 2, pp. 609-619, May 2013.

[133] S. Huang, Z. Chen, K. Huang and J. Gao, "Maximum torque per ampere and flux-weakening control for pmsm based on curve fitting," in *Proc. IEEE International Conf. on Vehicle Power and Propulsion Conf.*, Lille, France, Sept. 2010*,* pp. 1-5.

[134] S. Kim, Y. D. Yoon, Y. K. Sul and K. Ide, "Maximum torque per ampere (MTPA) control of an IPM machine based on signal injection considering inductance saturation," *IEEE Trans. on Power Electronics*, vol. 28, no. 1, pp. 488-497, Jan. 2013.

[135] Y. Sai, K. Sun, L. Huang and Y. Li, "Control strategy of high performance IPMSM drive in wide speed range," in *Proc. IEEE Annual Conf. on Industrial Electronics Society*, Melbourne, Australia, Nov. 2011*,* pp. 1783-1788.

[136] S. M. Sue, and C. T. Pan, "Voltage-constraint-tracking-based field-weakening control of IPM synchronous motor drives," *IEEE Trans. on Industrial Electronics*, vol. 55, no. 1, pp. 340-347, Jan. 2008.

[137] J. Ottosson, and M. Alakula, "A compact field weakening controller implementation," in *Proc. IEEE International Symposium on Power Electronics, Electrical Drives*, Automation and Motion, Taormina, Italy, Nov. 2006*,* pp. 696-700.

[138] B. H. Bae, N. Patel, S. Schulz and S. K. Sul, "New field weakening technique for high saliency interior permanent magnet motor," in *Proc. IEEE Industry Application Society Annual Meeting*, Salt Lake City, Utah, Nov. 2003*,* pp. 898-905.

[139] M. S. Uddin, T. S. Radwan and M. Z. Rahman, "Performance Interior permanent magnet motor drive over wide speed range," *IEEE Trans. on Energy Conversion*, vol. 17, no. 1, pp. 340-347, March. 2002.

[140] J. M. Kim, and S. K. Sul, "Speed control of interior permanent magnet synchronous motor drive for the flux weakening operation," *IEEE Trans. on Industry Applications*, vol. 33, no. 1,pp. 43-48, Feb.1997.

[141] R. F.Schiferi, and T. A. Lipo, "Power capability of salient pole permanent magnet synchronous motors in variable speed drive applications," *IEEE Trans. on Industry Applications*, vol. 26, no. 1, pp. 115-123, Feb.1990.

[142] T. M. Johns, "Flux-weakening regime operations of an interior permanent-magnet synchronous motor drive," *IEEE Trans. on Industry Applications*, vol. 23, no. 4,pp. 681-689, Aug.1987.

[143] W. L. Soong, and T. J. E. Miller, "Theoretical limitations to the field-weakening performance of the five classes of brushless synchronous AC motor drive," in *Proc. IEEE International Conf. On Electrical Machines and Drives*, Rugby, UK, Nov.1993, pp. 127-132.

[144] B. Sneyers, D. W. Novotny and T. A. Lipo, "Field weakening in buried permanent magnet AC motor drives," *IEEE Trans. on Industry Applications*, vol. 21, no. 2,pp. 398-407, Apr.1985.

[145] S. R. Macminn and T. M. Jahns, "Control techniques for improved high-speed performance of interior PM synchronous motor drives," *IEEE Trans. on Industry Applications*, vol. 27, no. 5, pp. 997-1004, Feb.1991.

[146] J. W. Kolar and S. D. Round, "Analytical calculation of the RMS current stress on the dc-link capacitor of voltage-PWM converter systems," in Proc. *IEE Electric Power Appl.*, vol. 153, no. 4, pp. 535-543, July 2006.

[147] S. Calligaro, F. Pasut, R. Petrella, and A. Pevere, "Modulation techniques for three-phase three-level NPC inverters: a review and a novel solution for switching losses reduction and optimal neutral-point balancing in photovoltaic applications," in *Proc. IEEE Applied Power Electron. Conf. and Exposition*, Long Bitch, CA, USA, Mar. 2013, pp. 2997-3004.

[148] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, "Voltage-balance compensator for a carrier-based modulation in the neutral-point-clamped converter," *IEEE Trans. on Industrial Electronics*, vol. 56, no. 2, pp. 305-314, Feb. 2009.

[149] Z. Zhang, O. C. Thomsen, and M. A. E. Andersen, "Discontinuous PWM modulation strategy with circuit-level decoupling concept of three level neutral-point clamped (NPC)

inverter," *IEEE Trans. on Industrial Electronics*, vol. 60, no. 5, pp. 1897-1906, May 2013.

Appendix A

All the machine parameters used for simulation and experimental studies are listed below.

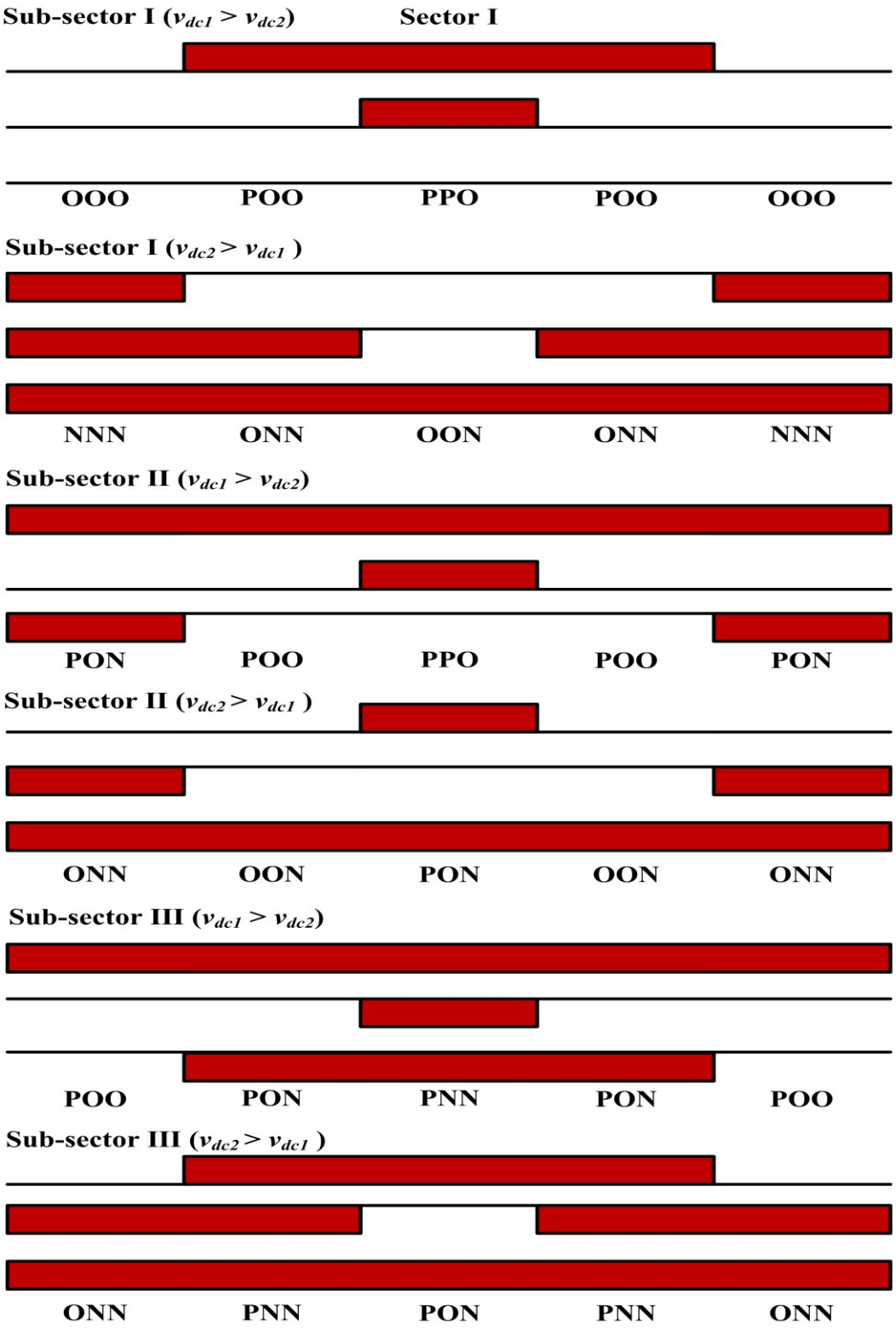
SPMSM rating, V_{LL}	6.0 kW, 220.0 V
Stator Resistance (r)	0.1718 Ω
Stator Self Inductances (L_d, L_q)	0.00336 H, 0.00336 H
Flux Linkage (λ)	0.591 Wb/m^2
Motor Inertia (J)	0.03334 kg-m^2

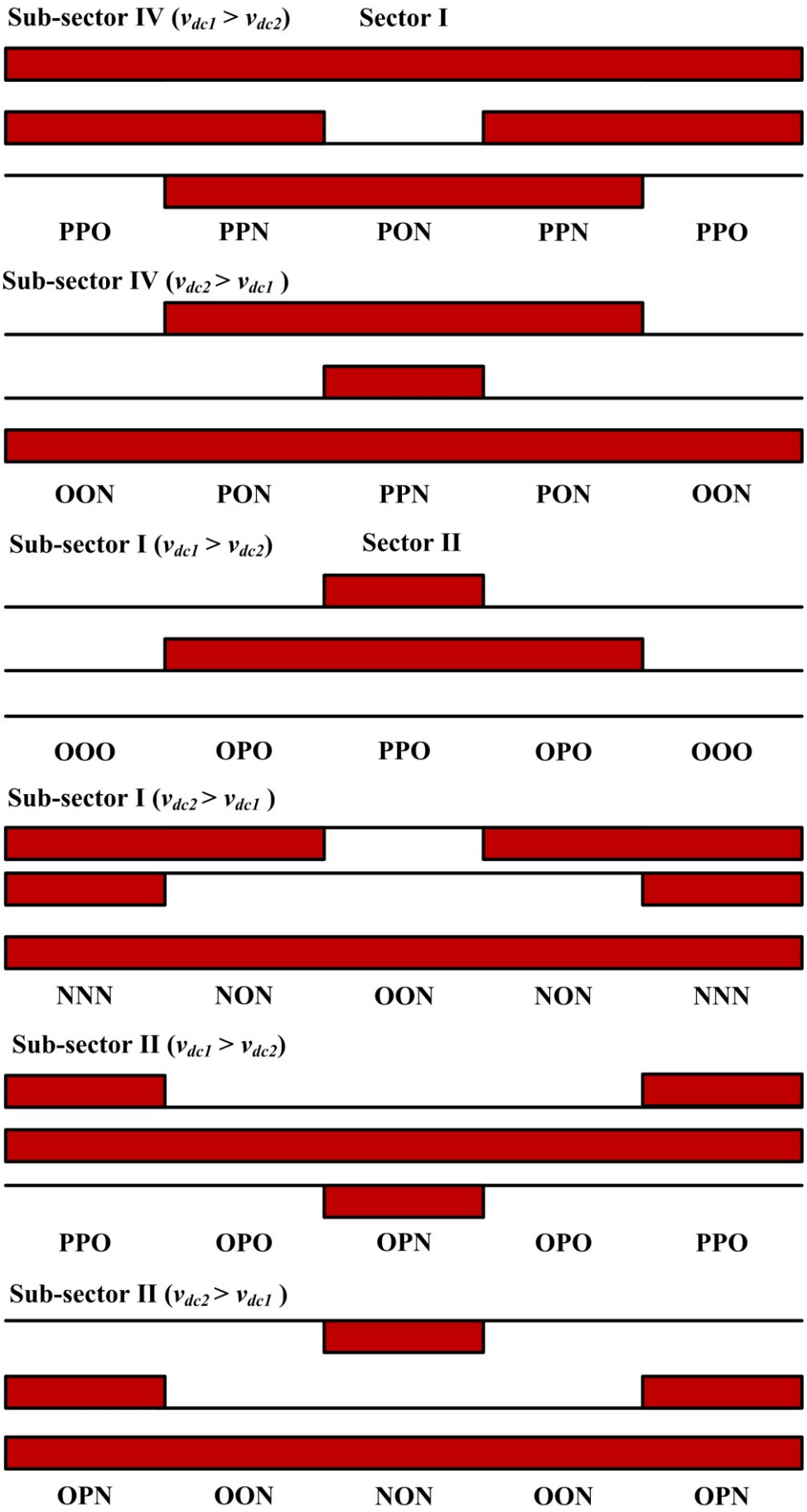
IPMSM rating, V_{LL}	6.0 kW, 220.0 V
Stator Resistance (r)	0.1718 Ω
Stator Self Inductances (L_d, L_q)	0.00514 H, 0.01419 H
Flux Linkage (λ)	0.591 Wb/m^2
Motor Inertia (J)	0.03334 kg-m^2

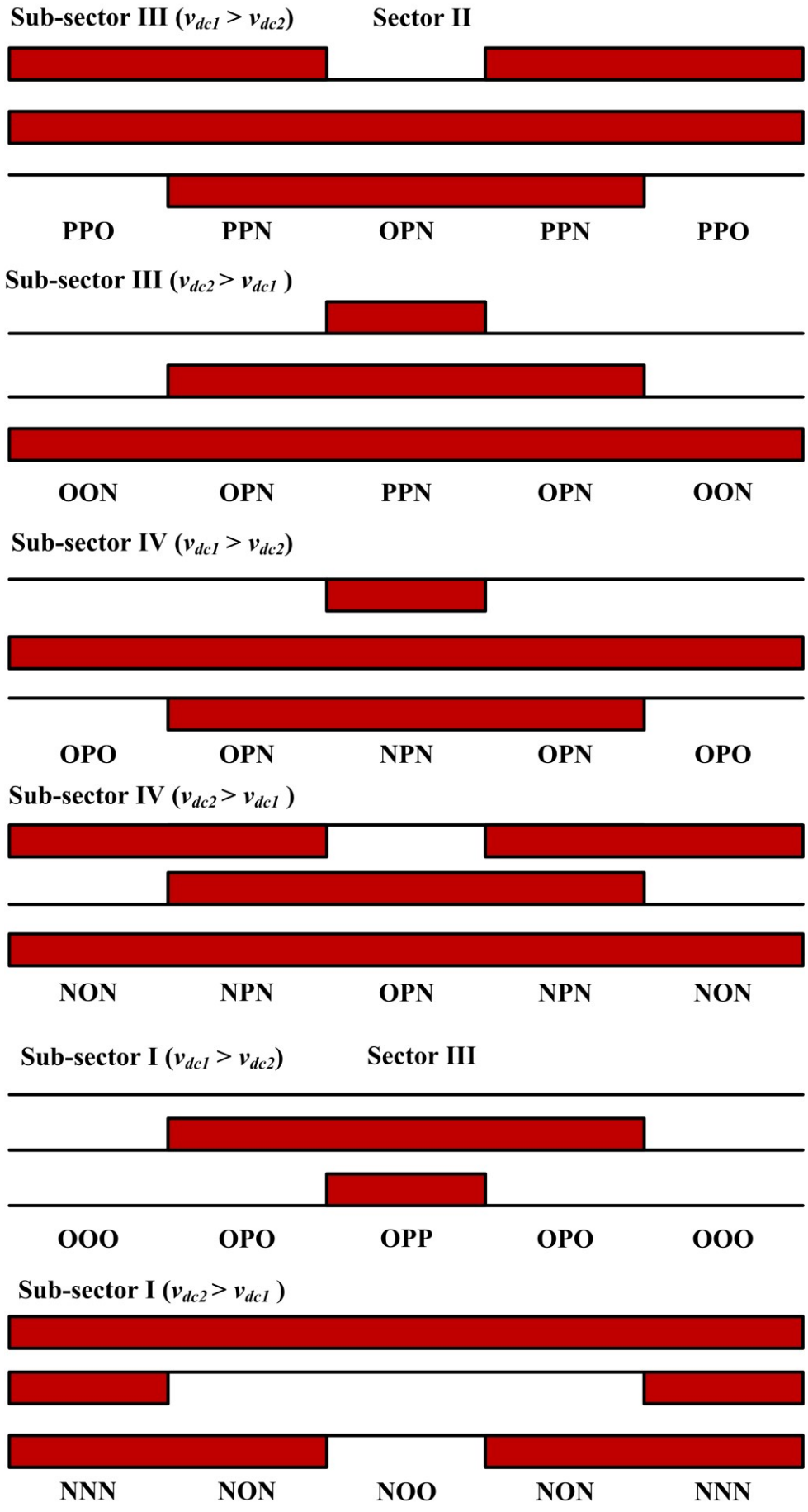
PMSM rating, V_{LL}	54.0 kW, 440.0 V
Stator Resistance (r)	0.054Ω
Stator Self Inductances (L_d, L_q)	270.0 μH, 270.0 μH
Flux Linkage (λ)	0.084419Wb/m^2
Motor Inertia (J)	0.05 kg-m^2

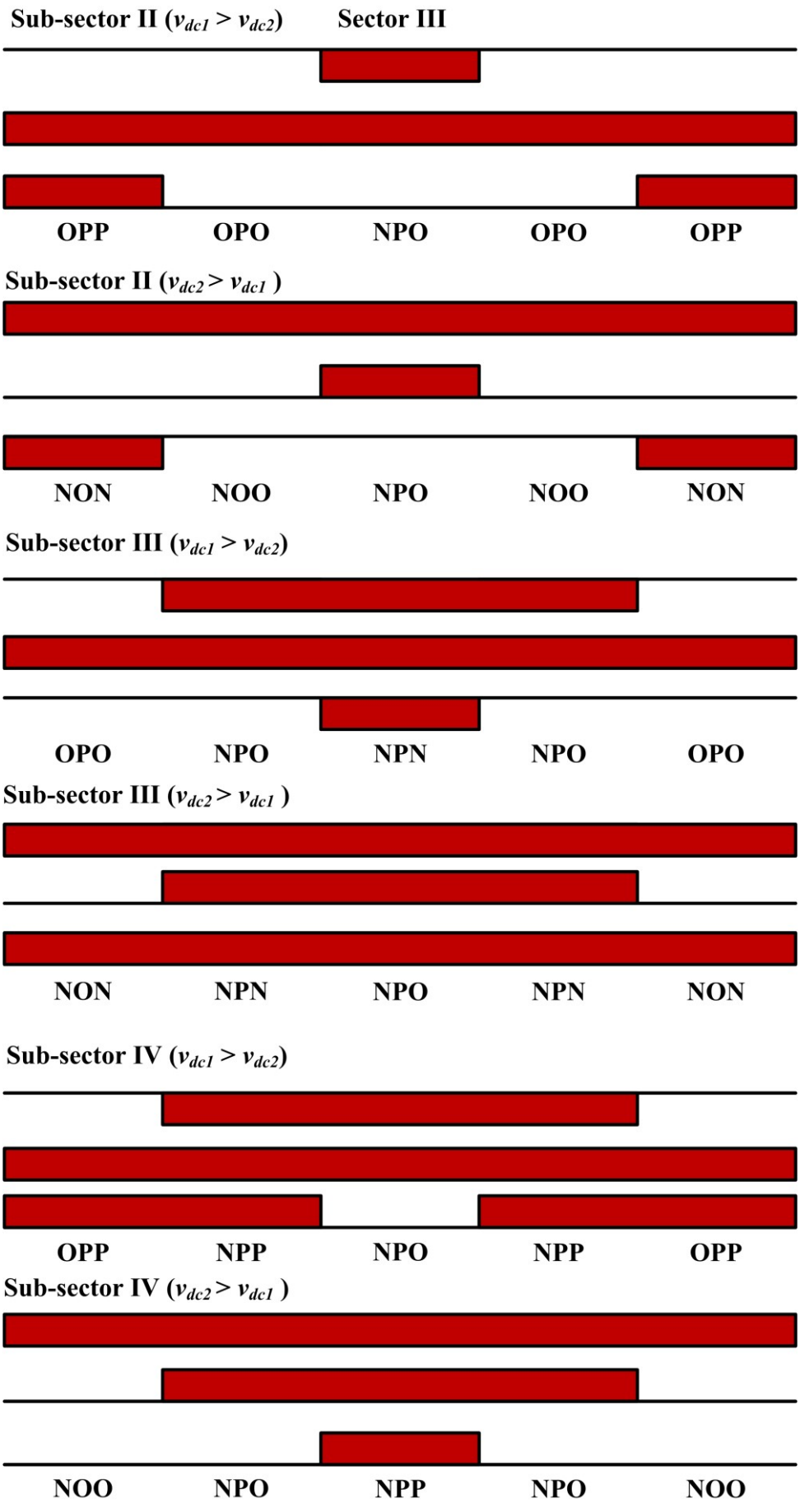
Appendix B

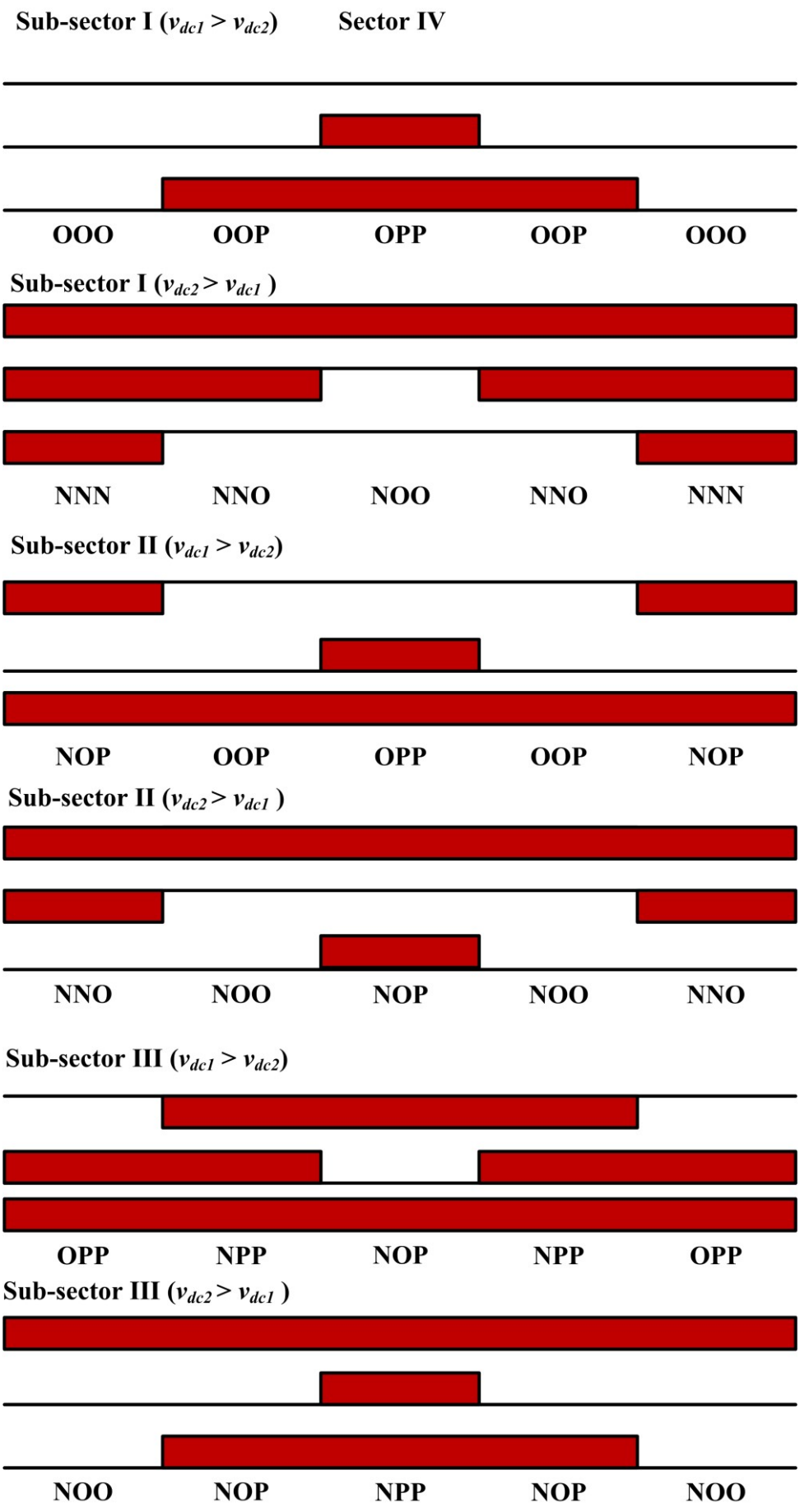
All the switching sequences for sectors and subsectors of the proposed SVPWM strategy are shown below.

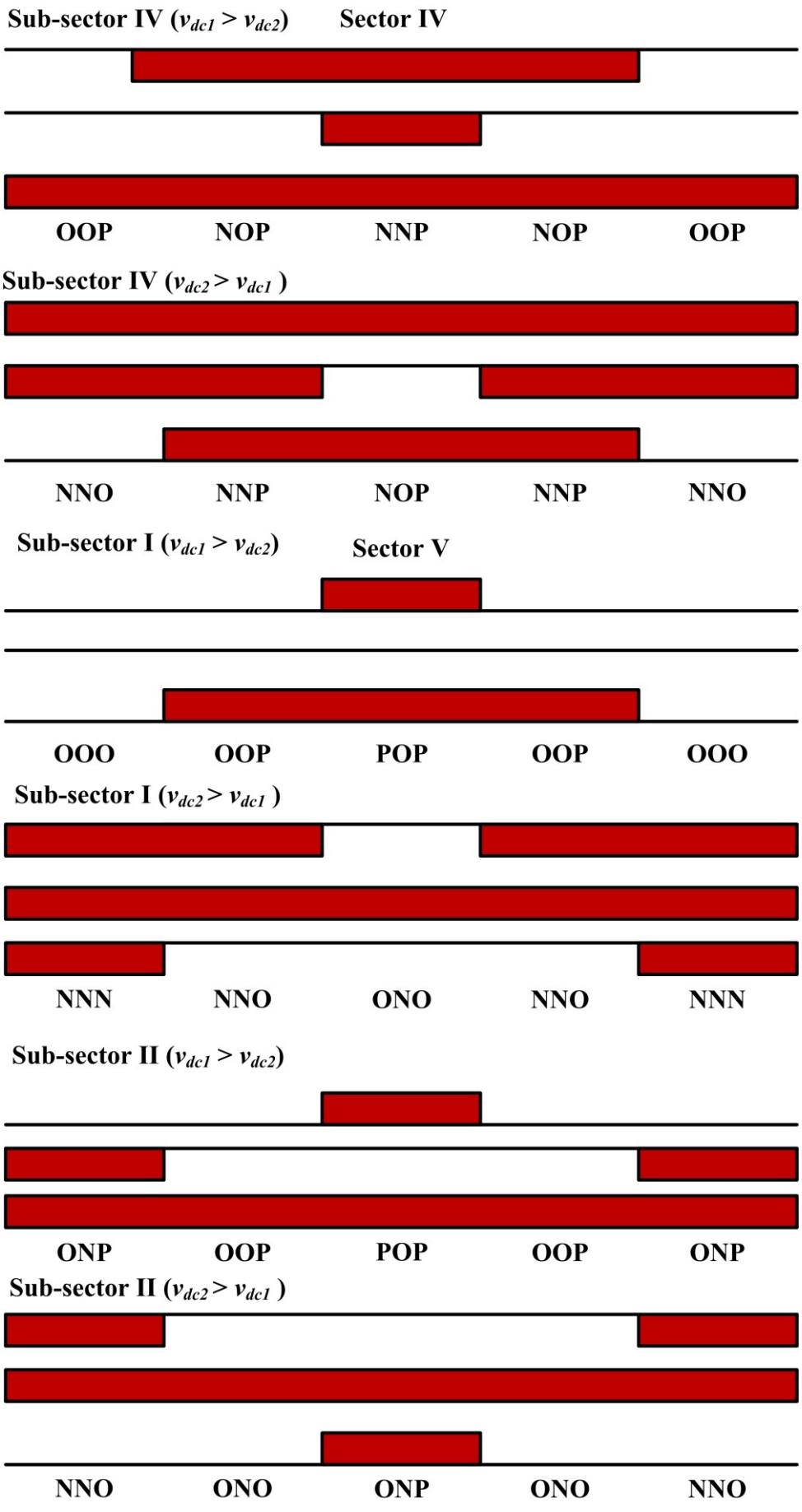


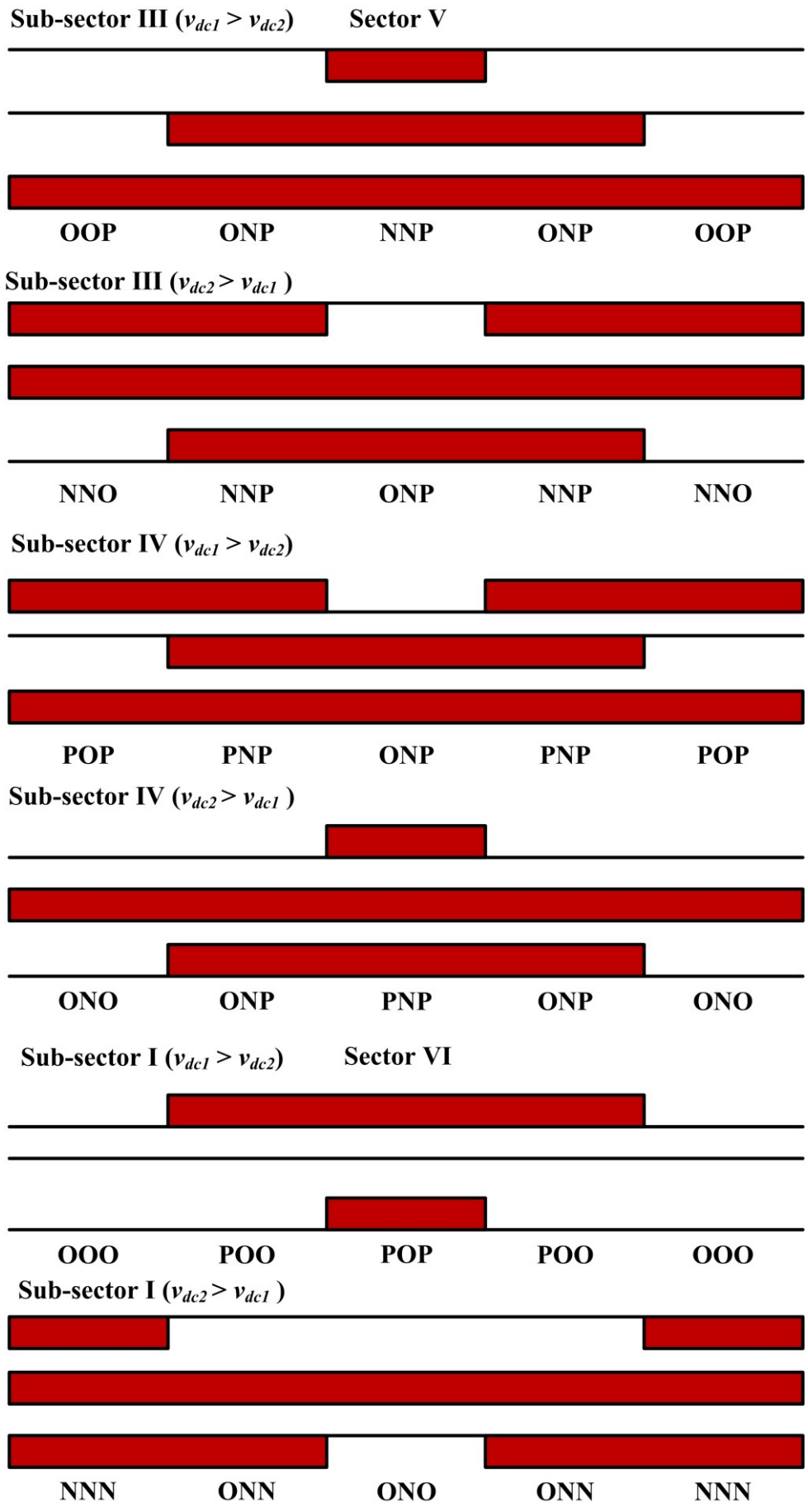

Sub-sector IV ($v_{dc1} > v_{dc2}$)
Sector I
PPO
PPN
PON
PPN
PPO
Sub-sector IV ($v_{dc2} > v_{dc1}$)
OON
PON
PPN
PON
OON
Sub-sector I ($v_{dc1} > v_{dc2}$)
Sector II
OOO
OPO
PPO
OPO
OOO
Sub-sector I ($v_{dc2} > v_{dc1}$)
NNN
NON
OON
NON
NNN
Sub-sector II ($v_{dc1} > v_{dc2}$)
PPO
OPO
OPN
OPO
PPO
Sub-sector II ($v_{dc2} > v_{dc1}$)
OPN
OON
NON
OON
OPN


Sub-sector III ($v_{dc1} > v_{dc2}$)
Sector II
PPO
PPN
OPN
PPN
PPO
Sub-sector III ($v_{dc2} > v_{dc1}$)
OON
OPN
PPN
OPN
OON
Sub-sector IV ($v_{dc1} > v_{dc2}$)
OPO
OPN
NPN
OPN
OPO
Sub-sector IV ($v_{dc2} > v_{dc1}$)
NON
NPN
OPN
NPN
NON
Sub-sector I ($v_{dc1} > v_{dc2}$)
Sector III
OOO
OPO
OPP
OPO
OOO
Sub-sector I ($v_{dc2} > v_{dc1}$)
NNN
NON
NOO
NON
NNN

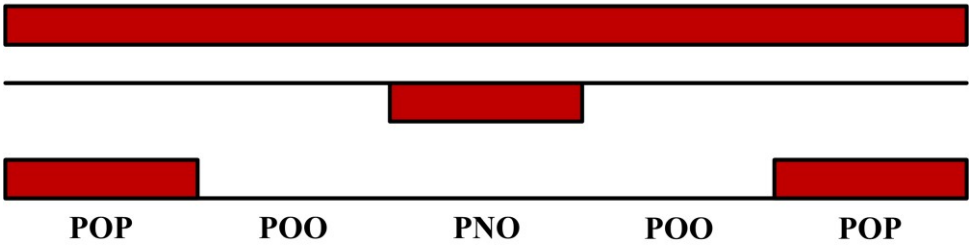

Sub-sector II ($v_{dc1} > v_{dc2}$)
Sector III
OPP
OPO
NPO
OPO
OPP
Sub-sector II ($v_{dc2} > v_{dc1}$)
NON
NOO
NPO
NOO
NON
Sub-sector III ($v_{dc1} > v_{dc2}$)
OPO
NPO
NPN
NPO
OPO
Sub-sector III ($v_{dc2} > v_{dc1}$)
NON
NPN
NPO
NPN
NON
Sub-sector IV ($v_{dc1} > v_{dc2}$)
OPP
NPP
NPO
NPP
OPP
Sub-sector IV ($v_{dc2} > v_{dc1}$)
NOO
NPO
NPP
NPO
NOO


Sub-sector I ($v_{dc1} > v_{dc2}$) Sector IV
OOO OOP OPP OOP OOO
Sub-sector I ($v_{dc2} > v_{dc1}$)
NNN NNO NOO NNO NNN
Sub-sector II ($v_{dc1} > v_{dc2}$)
NOP OOP OPP OOP NOP
Sub-sector II ($v_{dc2} > v_{dc1}$)
NNO NOO NOP NOO NNO
Sub-sector III ($v_{dc1} > v_{dc2}$)
OPP NPP NOP NPP OPP
Sub-sector III ($v_{dc2} > v_{dc1}$)
NOO NOP NPP NOP NOO

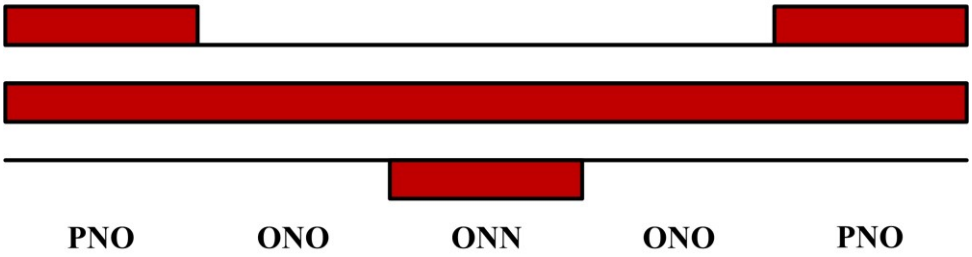

Sub-sector IV ($v_{dc1} > v_{dc2}$)
Sector IV
OOP
NOP
NNP
NOP
OOP
Sub-sector IV ($v_{dc2} > v_{dc1}$)
NNO
NNP
NOP
NNP
NNO
Sub-sector I ($v_{dc1} > v_{dc2}$)
Sector V
OOO
OOP
POP
OOP
OOO
Sub-sector I ($v_{dc2} > v_{dc1}$)
NNN
NNO
ONO
NNO
NNN
Sub-sector II ($v_{dc1} > v_{dc2}$)
ONP
OOP
POP
OOP
ONP
Sub-sector II ($v_{dc2} > v_{dc1}$)
NNO
ONO
ONP
ONO
NNO


Sub-sector III ($v_{dc1} > v_{dc2}$)
Sector V
OOP
ONP
NNP
ONP
OOP
Sub-sector III ($v_{dc2} > v_{dc1}$)
NNO
NNP
ONP
NNP
NNO
Sub-sector IV ($v_{dc1} > v_{dc2}$)
POP
PNP
ONP
PNP
POP
Sub-sector IV ($v_{dc2} > v_{dc1}$)
ONO
ONP
PNP
ONP
ONO
Sub-sector I ($v_{dc1} > v_{dc2}$)
Sector VI
OOO
POO
POP
POO
OOO
Sub-sector I ($v_{dc2} > v_{dc1}$)
NNN
ONN
ONO
ONN
NNN

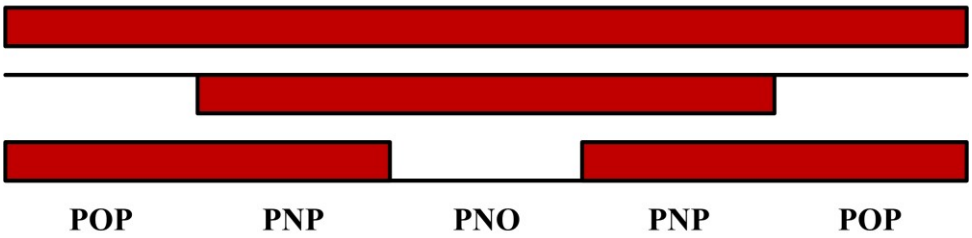
Sub-sector II ($v_{dc1} > v_{dc2}$) Sector VI



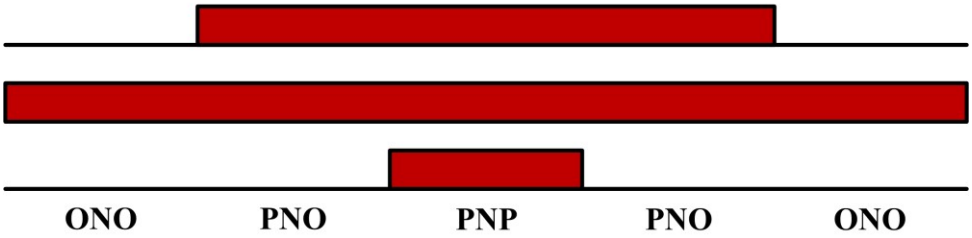
Sub-sector II ($v_{dc2} > v_{dc1}$)



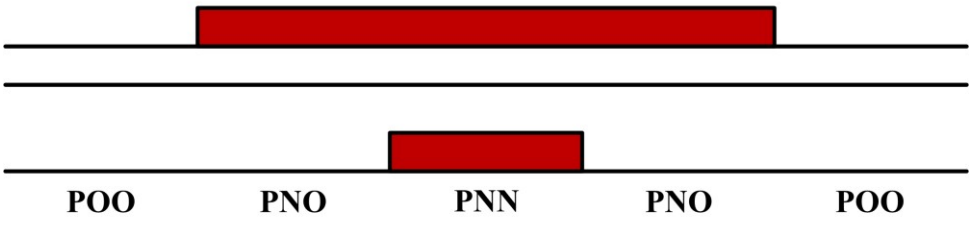
Sub-sector III ($v_{dc1} > v_{dc2}$)



Sub-sector III ($v_{dc2} > v_{dc1}$)



Sub-sector IV ($v_{dc1} > v_{dc2}$)



Sub-sector IV ($v_{dc2} > v_{dc1}$)