FABRICATION AND MAGNETOTRANSPORT STUDIES OF Bi_2Se_3 TOPOLOGICAL INSULATOR TRANSISTORS

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Abstract

Fabrication and Magnetotransport Studies of Bi_2Se_3 Topological Insulator Transistors

James Porter

Topological insulators (TI) are a unique class of materials that can support 2-dimensional (2D) metallic states on the surfaces of 3-dimensional insulating crystals. These 2D surface states are predicted to be spin polarized and topological, leading to potential applications in spintronics and quantum computing. While signs of surface transport have recently been observed in magneto transport experiments, many applied and theoretical questions remain to produce robust Bi_2Se_3 transistors. We first present the fabrication methods we developed to create high quality devices. We address the first main road block the community is facing to explore topological charge transport: making low resistance contacts to TI's. Using our devices, we then explore magneto transport. At cryogenic temperatures we observe the classical Hall effect as well as Shubnikov-de Haas oscillations consistent with the presence of Landau levels and surface transport in Bi_2Se_3 thin crystals. We focus on a thin crystal made of two regions with two thicknesses. We use our data to address the second major roadblock faced by the TI community: bulk-defect conduction versus surface transport. We discuss the evidence we have to support 2D surface transport in our devices, and the outlook for the exploration of the topological aspects of these surface states.

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Chapter 1

Introduction

Over the last several years a new class of materials known as topological insulators (TI's) has been studied both theoretically [1, 3], and experimentally [39, 16]. The unique quality of a three-dimensional topological insulator is that they can support 2-dimensional (2D) metallic states on their surfaces while their bulk is an insulating crystal [28]. Bismuth Selenide (Bi_2Se_3), long known for its thermoelectric properties, was only recently fully investigated in thin films, is selected as the TI material for our studies due to its large bandgap of 0.3 eV [15], which makes it more likely that its topology is robust against disorder. Optical studies have probed the surface states of Bi_2Se_3, and confirmed the Dirac surface dispersion [21]. Experimental electron transport in topological Bismuth Selenide is still waiting to take fully off. Much of the material's potential remains to be unlocked due to fabrication difficulties and material impurites. Predicted to be spin polarized, the 2D surface states (see Figure 1.1.1(b)) could have applications in spintronics and quantum computing [15]. There

are several competing methods to make Bi_2Se_3 thin films, such as crystal growth and mechanical exfoliation. We present the fabrication methods and measurement techniques required to explore the magneto transport properties of nanometer scale Bi_2Se_3 samples.

The structure of this chapter is as follows: section 1.1 gives a short introduction to topological insulators, in particular Bi_2Se_3, and section 1.2 gives an overview of the fabrication processes we developed, transistor specifications we could produce and the the magneto transport properties observed in our fabricated devices.

1.1 Introduction to thin Bismuth Selenide topological insulators

Topological insulators are characterized by an insulating bulk band gap and protected surface or edge states [28, 4, 3]. To show how these surface states come about, we first explain what how topology of a material is defined. Figure 1.1.1 (a) shows the band structure of a trivial insulator with a large insulating bandgap. As there are no points at which the valence and conduction bands meet this is referred to as a Z_0 topology. In panel (b) the conduction and valence bands meet and there is a finite density of states at all energies. In this case, one point of crossing is referred to as a Z_1 topology.

Topological insulator materials exhibit a strong spin-orbit interaction (SOI), arising from the coupling of an electron's magnetic spin to the magnetic field setup

by the motion of the electron around it's orbital. This coupling can lead to the bending of energy bands in solids, which is known as the Rashba Effect [31, 33]. In topological insulators and particularly Bi_2Se_3, the SOI is so strong that the valence and conduction energy bands will actually switch places. Figure 1.1.2 (a) shows the band structure of a topological insulator, in which the valence and conduction band have two crossing points or a Z_2 topology. The valence and conduction bands are inverted (switch places) near the Γ-pt in reciprocal momentum space, creating topologically protected surface states (straight lines in Figure 1.1.2 (a)) within a bulk bandgap [28, 3]. The black arrows represent the conduction (up) and valence (down) bands [24]. The insulating bandgap opened by the band inversion in the material must close at the boundaries in order to re-open to the vacuum bandgap, which is topologically different in that it has a Z_0 band structure of a trivial insulator.

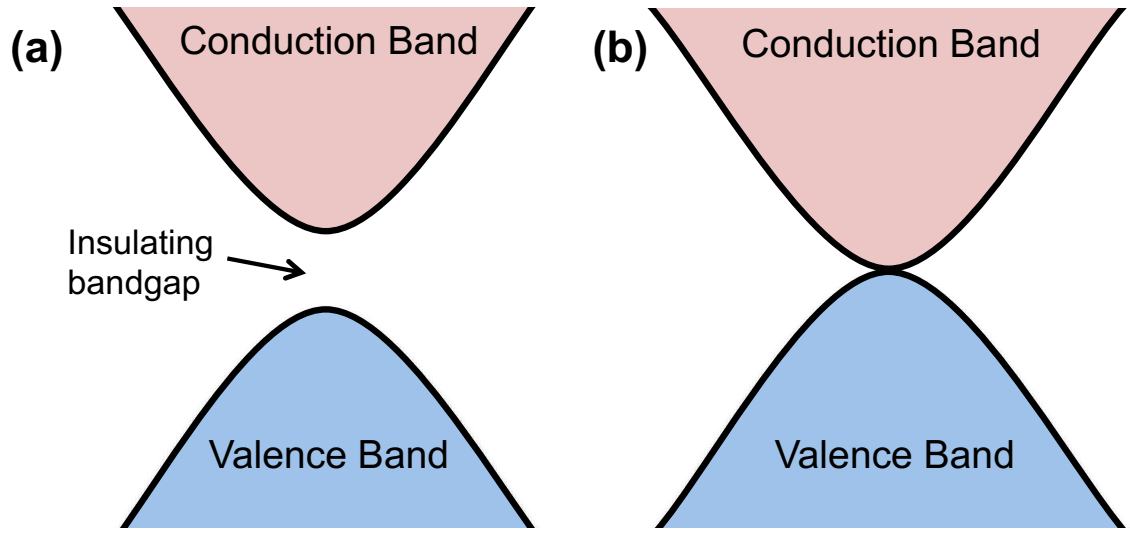

Figure 1.1.1: Band structure in solids: (a) A trivial insulator with Z_0 topology has a large insulating energy gap where no conduction occurs, (b) When the valence and conduction bands meet, a Z_1 crossing occurs resulting in metallic conduction states

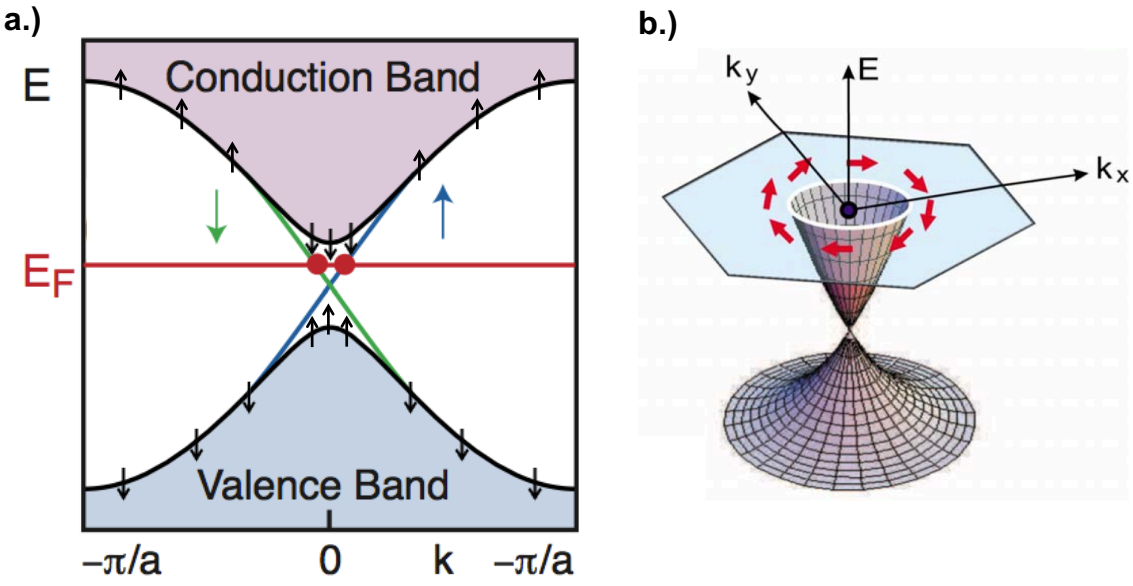

Figure 1.1.2: Band Structure of a topological insulator. (a) Band inversion results in topologically protected surface states in a bulk bandgap (green and blue lines). Figure adapted from *Hasan* et al. [28] (b) Spin-momentum locking on a topological surface state. Figure from *Hsieh* [3].

At the surfaces (i.e. boundaries) of the material we therefore have a nonzero density of states, represented by the conducting surface states which are protected by the topology of the band inversion. As a result of the strong SOI, surface carriers are spin-polarized due to a locking of spin to momentum, shown in Figure 1.1.2 (b). The spin of surface carriers (red arrows) related to their position in $k-$space. With a single cone on each surface, up and down spin states are prevented from collapsing due to their large separation distance setup by an insulating bulk. Bi_2Se_3 is a layered crystal made up of alternating planes of Bi and Se trigonal lattice. Figure 1.1.3 shows how adjacent planes bond together 5 at a time to form so called quintuple layers (QL). Bonded together by Van der Waals forces, the layers may be easily separated from one another to make thin films from the bulk material. Previously known for its thermoelectric qualities, Bi_2Se_3 has become popular again in the search for topological surface states. Due to its large bandgap, Bi_2Se_3 supports a robust topological state, predicted by theory to survive even up to room temperature [15].

So called parity-inversion symmetry (see section 3.1.1 for more details) leads to charge carriers having a negative effective, meaning we have band inversion (holes and electrons switch places) [26]. By tuning the Fermi Energy (using a back gate electrode) we should theoretically be able to observe scatter free spin-polarized surface states up to room temperature. In practice it has proven impossible to obtain pure surface transport without contamination from bulk defect mediated transport. Impurities in the bulk such as Se vacancies contribute charge carriers which may overwhelm the surface transport. Similar to many other topological insulator materials, Bi_2Se_3

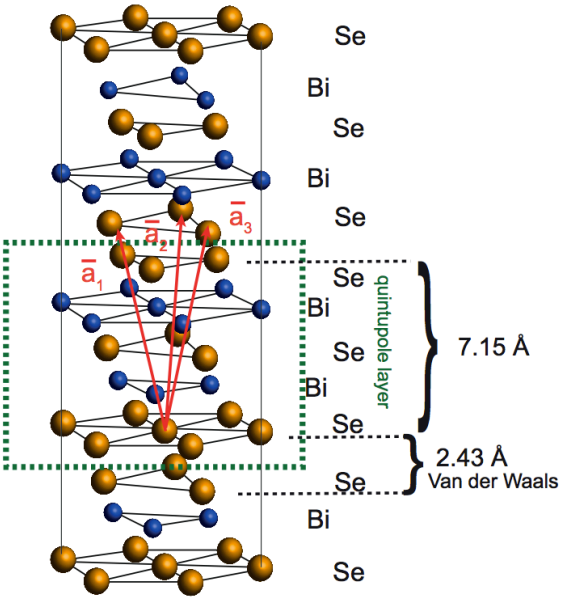

Figure 1.1.3: The crystal structure of bismuth selenide is made of planar trigonal lattices, bonded together 5 layer stacks at a time. Figure taken from *Bianchi* et al. [26]

belongs to the chalcogenides compound group known to readily react with oxygen [36]. Oxidation leads to Se vacancies and contamination of the surface transport properties.

The Bi_2Se_3 electronic Hamiltonian in equation (1), shows a parabolic energy vs momentum dispersion in the bulk, as well as a linear energy dispersion for surface carriers:

$$H(k) = -Dk^2 + v_F(k_y\hat{\sigma}_x - k_x\hat{\sigma}_y) \tag{1}$$

We expect to observe both the classical and quantum Hall effects in thin films at low temperatures, which would allow the measurement of the charge carrier densities pertaining to respectively the bulk and surface transport contributions. Some experiments have recently shown that thin Bi_2Se_3 can exhibit a non linear magnetoresistance, in the way of Shubnikov-de Haas oscillations (not fully formed quantum Hall phases) and localization effects [10, 25, 21].

1.2 Summary of our fabrication and transport results in Bi_2Se_3

In this work we use mechanical exfoliation to produce Bi_2Se_3 thin films of thicknesses ranging from several hundred microns down to a few nanometers. Low resistance contacts were fabricated after minimizing the crystal surface oxidation effects. This

was done through a combination of vacuum storage, rapid fabrication and plasma etching oxidized regions under the contact areas. A catalogue of devices was created so that the fabrication methods could be evaluated and calibrated based on the measured electron transport properties of the devices. A few select devices were selected for detailed magneto transport studies as a function of crystal thickness, gate voltage, and magnetic field at cryogenic temperatures. Figure 1.2.1 shows the magnetoresistance of a 38 nm thick crystal measured at 1.5 K. The Classical Hall density, $n_{Hall} = 7.48 \times 10^{14} cm^{-2}$, is found from the slope of R_{xy} vs B. This value indicates the sample is in the electron-doped (n-doped) regime, likely due to carrier contributions from the bulk layers. On top of the linear behaviour of R_{xy} vs B, Shubnikov-de Haas oscillations are visible, indicating the formation of Landau levels. The extracted 2D charge density of $n_{SdH}^{2D} = 6.45 \times 10^{11}$ cm^{-2} suggests that we are measuring a combination of bulk and top layer surface transport, in parallel.

1.3 Structure of thesis

Chapter 2 will present the the microfabrication techniques we developed to fabricate thin film Bi_2Se_3 field effect transistors. In Chapter 3 we discuss the electron transport measurement techniques and transport data allowing the performance classification of the fabricated devices. In Chapter 4 we take an in depth look at the magneto transport behaviour of a few selected devices. The data is tested for the weak anti-localization (WAL) and Shubnikov-de Haas (SdH) effects. We demonstrate both

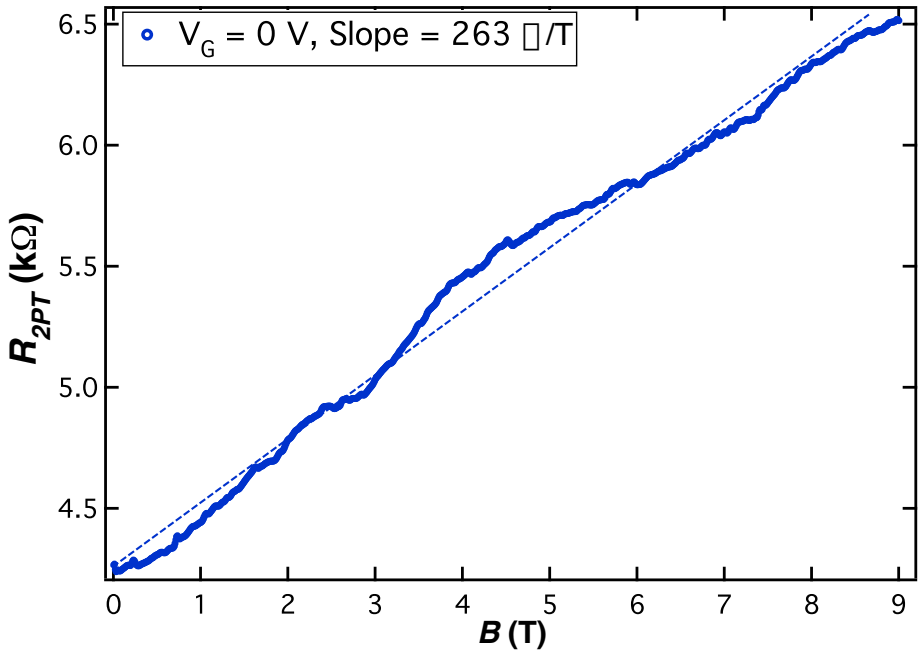

Figure 1.2.1: Resistance vs magnetic field in sample C shows small oscillations on top of a linear slope, indicating parallel bulk and surface transport

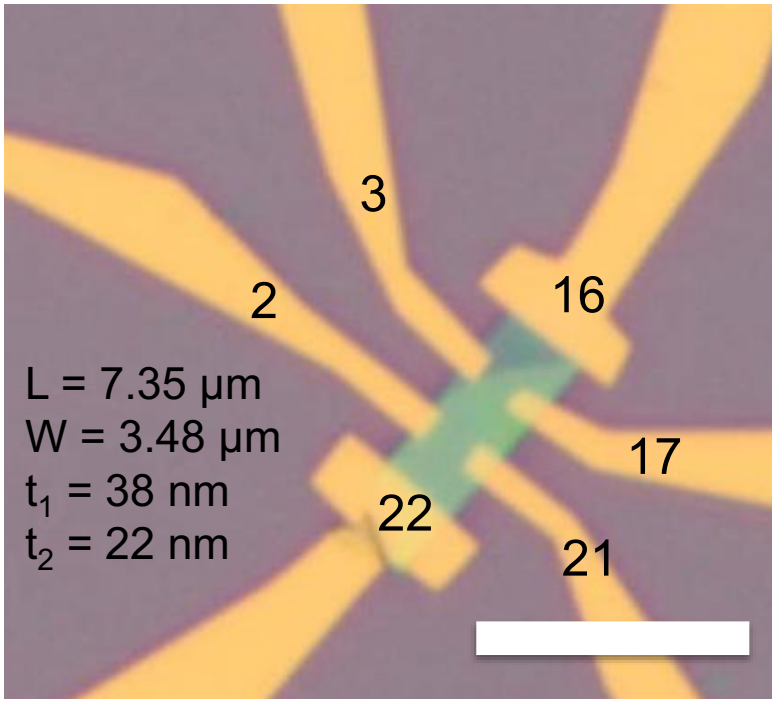

Figure 1.2.2: Mechanically exfoliated Bi_2Se_3 of 22 nm with lithographically defined Gold electrodes. Scale bar is 10 μm.

linear and oscillatory behaviour of transverse resistance R_{xy}, and oscillatory behaviour of the longitudinal resistance R_{xx} in magnetic fields. We extract 2D carrier densities on the order of 10^{12} cm^{-2}, indicative of surface transport. Finally, future experiments and conclusions are presented in Chapter 5.

Chapter 2

Fabrication of ultra-thin Bi_2Se_3 transistors

In this chapter we describe the fabrication methods we developed to make thin Bi_2Se_3 transistors suited for the magneto-transport studies which will be discussed in chapters 3, 4 and 5. Figure 2.0.1 depicts a thick Bi_2Se_3 flake contacted with pre-patterned Gold electrodes. These devices have the standard source/drain/back gate geometry of a field effect transistor to tune the Fermi energy of the gold leads and the carrier density in the crystal.

The foremost hurdles to achieving transport will be synthesizing thin films with a uniform crystal surface, making low resistance contacts including an efficient gate electrode without current leakage. We make 2-point and 4-point contact geometries on crystals of varying thickness, from hundreds of nanometers down to the 20 nm in the ultra thin regime. We use either an etched substrate or suspension techniques

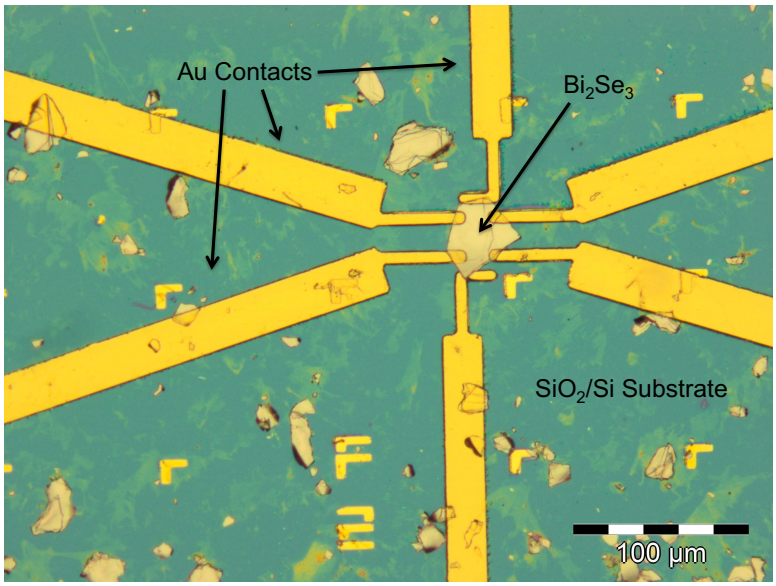

Figure 2.0.1: Photolithographically defined electrodes on a Bi_2Se_3 crystal with a Hall bar geometry

to compare against on-substrate devices of varying thickness, in order to study both the effect of crystal thickness and substrate disorder. This chapter begins with the substrate preparation for and mechanical exfoliation of Bi_2Se_3 thin films in section 2.1. In section 2.2 we discuss methods for obtaining Bi_2Se_3 thin film structures that may used for measurement devices. In section 2.3 we outline the methods of characterizing the crystal sample for thickness and surface uniformity, using optical and atomic force microscopy. In section 2.4 we explain the photolithography and electron beam lithography techniques, as well as metal evaporation methods employed in making electrical contact to the crystal surface. Finally in section 2.5 we introduce the cryogenic fridge and measurement setup to be used in low-temperature studies of Bi_2Se_3 devices at magnetic fields up to 9 Tesla. In Chapter 3 we will study the contact

resistance of these devices, and in Chapter 4 we investigate the magnet-transport properties in search of 2D topological surface states.

2.1 Coordinate grid on Si/SiO_2 substrates

The substrates used in this experiment are highly doped Si/SiO_2 wafers, polished on one side on which a 300 nm thick SiO_2 film is grown. We use a reactive ion etch with CHF_3 plasma to remove the insulating SiO_2 on the back side only to allow for back gate electrical connection. Due to the exfoliated deposition method (see 2.2), crystal flakes of Bi_2Se_3 are randomly distributed over the substrate surface. In order to facilitate locating and connecting the crystals, the substrates are prepared with coordinate grids made of evaporated gold markers (see Figure 2.4.2) on photolithographically defined patterns. Gold is used for the alignment markers since its large reflectance makes them visible under both optical and scanning electron microscopes. The coordinate grids spans from A1 to I9, with L-markers spaced apart by 100 μm. The L-shapes double as size comparison standards, with dimensions 5 x 15 μm. The wafers are highly polished on one surface for crystal deposition, while we etch the other side clean of SiO_2 for back gate connection. We use a reactive ion plasma etch with a recipe of 9 sccm CHF_3, 1 sccm O_2 at 100 mTorr pressure and 300 W for 15 m. On certain chips designated for suspended devices, the same plasma etch recipe is done after photolithography to define trenches in the substrate surface (discussed in chapter 5). Prepared substrates are diced, labelled and stored in an

anti-static Gel-Pak until needed.

2.2 Deposition of thin Bi_2Se_3 crystals

Since the explosion of graphene studies in the mid 2000's [11], the method of mechanical exfoliation has revolutionized the synthesis of atomically thin materials. Although other growth techniques such as molecular beam epitaxy (MBE) are capable of delivering single-layer sheets with large surface area, the quality provided by mechanical exfoliation is unmatched. Whereas MBE grown films are plagued by surface wrinkles and the challenge of transferring the crystal to a desired substrate, mechanical exfoliation deposits two-dimensional flakes of pristine crystallinity onto the substrate of choice. Verified by AFM and Raman spectra, exfoliated graphene crystals are single layer with uniform surfaces and regular edges. Here we demonstrate the mechanical exfoliation technique as applied to Bismuth Selenide (Bi_2Se_3), and show that it also produces thin flakes with uniform surfaces. As Bi_2Se_3 is a topological insulator, which is predicted to exhibit novel surface states, it is imperative that we preserve its surface quality.

2.2.1 Mechanical Exfoliation

Manual mechanical exfoliation, known colloquially as the tape peeling method, is in principal very simple and cheap to carry out. However, it can be difficult to calibrate the procedure and get reproducible results.

The crystal structure of Bi_2Se_3 is divided up into so called quintuple layers - two embedded sheets of Bi sandwiched between layers of Se on all sides. Adjacent quintuple layers are held together by the rather weak van der Waals forces making Se - Se bonds at a distance of up to 350 pm [36]. This layered stacking is what allows the crystal to be easily cleaved during mechanical exfoliation. Tearing quintuple layers apart from one another, the exfoliation process leaves a layered crystal with a Se terminated surface.

We begin exfoliation with a bulk piece of Bi_2Se_3, and breaks it up into the thinnest slices possible by hand using a razor blade. We then place a thin slice onto the sticky side of a piece of adhesive tape, and the tape is folded onto itself to sandwich the Bi_2Se_3 flake. Since the in-plane bonding of atoms within the crystal is much stronger than the Van der Waals interactions holding the sheets together, an interlayer tear can propagate through the crystal as the scotch tape is peeled apart. The process of folding and peeling the tape is repeated several times, separating the crystal layer by layer. If we make the approximation that the crystal thickness is halved with each peel, then the crystal height after n peels will be $h_0{*}(1/2)^n$, where h_0 is the initial thickness before exfoliation. It is easy to see then how a macroscopic piece of bulk Bi_2Se_3 can be thinned down to the nanometer scale with this technique, as 20 folds results in a height reduction of over one million times. Once the Bi_2Se_3 thin films have been prepared, they are ready to be deposited onto the substrates for device design. We use 550 μm thick highly doped silicon wafers (N/ARS, $\rho < 0.005$ Ωcm), with a 300 nm thick layer of SiO_2 to insulate the source and drain electrodes from the back

gate (Si wafer). The flake deposition procedure is straightforward: place the diced substrates facedown onto the sticky side of the scotch tape (uniformly covered with Bi_2Se_3 flakes of various thickness), and then peel off the tape. The substrates are left to sit underneath the tape for 10 minutes before removing, massaging the tape on top of the substrates to encourage crystal adhesion. When the tape is removed, it is done carefully and slowly, attempting to have the best transfer from the tape to substrate, to minimize any further tearing of the crystals. Substrates bearing crystal flakes are immediately placed into vacuum storage in order to protect the freshly cleaved crystal surfaces from oxygen degradation in atmosphere. This oxidation and the strategies to deal with it will be the subject of Chapter 3. The sample storage space contains a desiccant to aid in dehumidifying the chamber.

2.2.2 Vapor-Solid growth of Bi_2Se_3 nanocrystals

An alternate method to fabricate thin films of Bi_2Se_3, is the Vapor-Solid (VS) growth method, which we also investigated. Figure 2.2.1 shows the growth setup: a 99.999% Bi_2Se_3 solid source crystal is placed at the center of a quartz tube furnace and heated to 700 C. The source crystals were either freshly cleaved using scotch tape, or powdered to maximize their surface area. We did not find that powderizing the source crystal yielded better results than using a large piece of bulk crystal with a clean surface. Solvent cleaned and N_2 dried target substrates of SiO_2/Si were placed 14 - 15.5 cm down the tube, where it was determined to have an optimal temperature gradient for crystal condensation, based on the methods of *D. Kong* et al [6]. Gas

flow rates are set to 200 sccm Argon and 5 sccm Hydrogen while the furnace heats up. Argon is used as an inert transport gas to flow vaporized Bi_2Se_3 down the tube towards the deposition region. The Hydrogen gas acts as a catalyst for the process and is turned off once the temperature peaks at 700 C. Once the temperature reaches 700 C, the Argon transport gas is kept on, as the furnace is allowed to cool down.

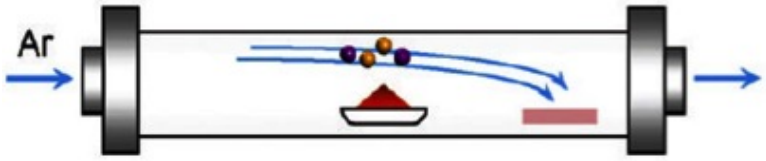

Figure 2.2.1: Argon transport gas flows Bi_2Se_3 vapour down the quartz tube towards target substrate. Figure from *Mlack* [23]

The morphologies of the deposited thin Bi_2Se_3 crystal varies with their position along the quartz tube. Depending on the temperature (i.e. distance from the center of the tube) at the location where the crystals condensed, we may find a spectrum of crystal density and appearance. Flat surfaces and straight or stepped edges are indicators that the vapour has condensed into a crystalline form. Of potential crystal candidates to make transistor devices, the most interesting are Bi_2Se_3 nanoribbons (1 x 50 μm in dimension), and large surface area platelets. The VS method offers a spectrum of morphologies to study the effects of edge versus surface transport in thin ($<$ 50 nm) films of topological Bi_2Se_3. Using these VS grown crystals poses additional challenges, fabrication steps, due to the need for a clean surrounding area

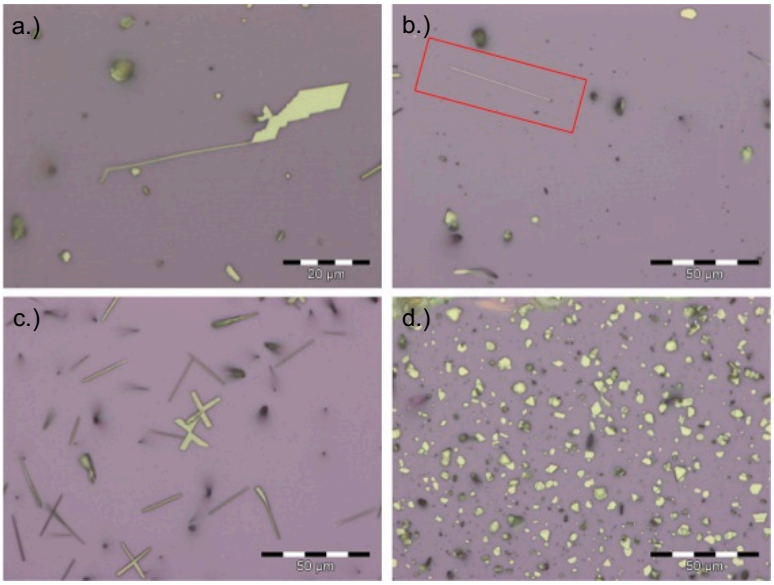

Figure 2.2.2: Vapor-Solid growth from powderized Bi_2Se_3 a.) Interesting step-like growth results in a nanoribbon attached to a planar crystal with many corners b.) 50 μm long nanoribbon c.) X-shaped crystals d.) Triangular and hexagonal stacked nano plates.

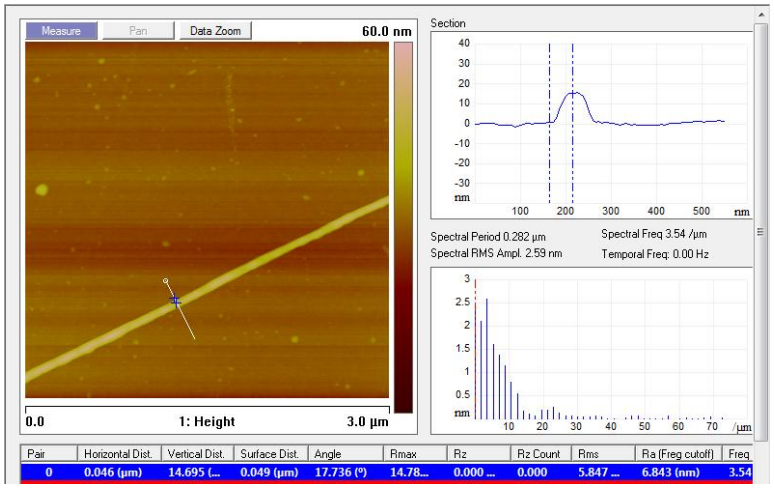

Figure 2.2.3: AFM measurement of a 15 nm thick ribbon with uniform edges

of neighbouring crystals for electrical contacts. This could be done by making a box of photoresist to protect the target crystal, and plasma etching the surrounding area clean. For an eventual mass production of these transistors the VS growth method could dominate mechanical exfoliation in terms of throughput. However, in the pursuit of individual working transistors, the scotch tape method is more suitable to us.

2.3 Structural characterization of deposited thin films

To start our fabrication of thin Bi_2Se_3 transistors, we have to sift through the synthesized flakes and select the best candidates for devices. Optical microscopy gives a good initial impression of a flake's surface roughness, edge uniformity and relative thickness. A large number of crystals can be inspected quickly using optical microscopy and we, catalogue those with potential for transistor application. To get precise thickness measurements and surface information, we use atomic force microscopy (AFM) to build a topographical image of the flake. This process is much longer than optical investigation, therefore only a few selected crystals are imaged using AFM. Imaging can also be done after completing the charge transport measurements on a device in order to avoid wasting time imaging devices which end up failing for various reasons.

2.3.1 Optical microscope characterization

The mechanical exfoliation method gives us a random dispersion of crystals of varying shapes and sizes across the substrates. Individually diced silicon substrates are inspected one by one with optical microscopy, while the other samples awaiting characterization remain under vacuum. The microscope we used is an Olympus BX51M, with a digital camera attached directly to a desktop computer for taking pictures. The substrate grids (see section 2.1) are slowly scanned, looking for flakes which are thin, uniform, large and isolated from the other flakes. The thickness of the flakes can be approximated to within 20 nm for thin flakes, and 100 μm for thick flakes, by observing the colour of the crystal and the uniformity of the surface.

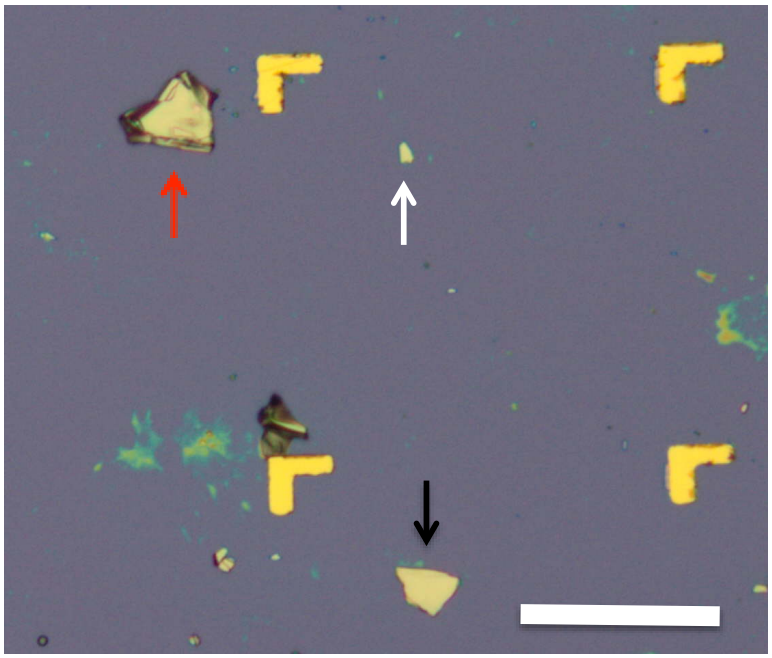

Figure 2.3.1: Preliminary characterization of mechanically exfoliated flakes using an optical microscope

In Figure 2.3.1 we see how thicker flakes are easily discerned by the multilayering of opaque yellow surfaces and dark, jagged edges (red arrow). Flakes of this kind are typically 800+ μm. A singular edge and flat surface (black arrow) indicates a thickness of 100-300 μm. Thinner flakes on the order of 30-80 nm will begin to show translucent blue coloured edges (white arrow). High quality flakes are characterized by having a uniform surface thickness and more straight, crystalline edges. Dark-field imaging is very useful in noticing height changes on the surface of a crystal. In this setting of the optical microscope, light that is scattered off the surface is collected, as opposed to the reflected light observed in usual optical microscopy. A directory of flakes is constructed, and selected samples will go for precise height measurement by atomic force microscopy (AFM). Samples are chosen based on their thickness, uniformity, surface area, and their location on the substrate. Typically, lithography patterns will require 500 -1,000 μm of free space, so the flakes which land close to each other or close to the substrate's edges need to have custom designed electrodes in order to prevent discontinuities of the contacts. Sometimes flakes landing too close to the substrate edge are overlooked, as edge effects when spinning photoresist lead to a non-uniform resist thickness.

2.3.2 Atomic Force Microscope measurements

For precise thickness measurements of our devices, we use atomic force microscopy (AFM) to obtain 3-dimensional height maps of the crystals. Figure 2.3.2 shows a translucent thin film identified by optical microscopy and measured by AFM.

The AFM operates by reflecting a laser beam off a cantilever tip towards a CCD photodiode. The cantilevers we use were typically made of Silicon. Upon analyzing the received signal, the cantilevers vibrational amplitude is determined, and translated into a height (z-position). The tool used in these studies is a digital instrument 622VJ, operated in tapping mode. A vertical resolution better than 5 nm is easily attained. Height measurements can be taken on the crystal before lithography, or after metal evaporation to include the of gold contacts.

Line scans are assembled into 2-dimensional height maps, with colour denoting the z-axis. The data is analyzed by taking line cuts perpendicular to crystal edges and along surfaces. Exact thickness values are necessary for extracting transport properties from transport data (e.g. change density, mobility) and will thus be very useful in the following chapters.

2.4 Making electrical contacts to ultrathin topological Bi_2Se_3 crystals

Here we discuss the construction of a Bi_2Se_3 thin film transistor. Figure 2.4.1 shows a cartoon of a device with source, drain, and electrostatic ally coupled gate electrodes. The two methods used in this project for designing micron-scale circuits are the traditional photolithography, using ultraviolet exposure of photoresist, and the higher-precision electron beam lithography (EBL), which makes use of a shorter wavelength beam of electrons for fine details. Photolithography has a higher throughput, making

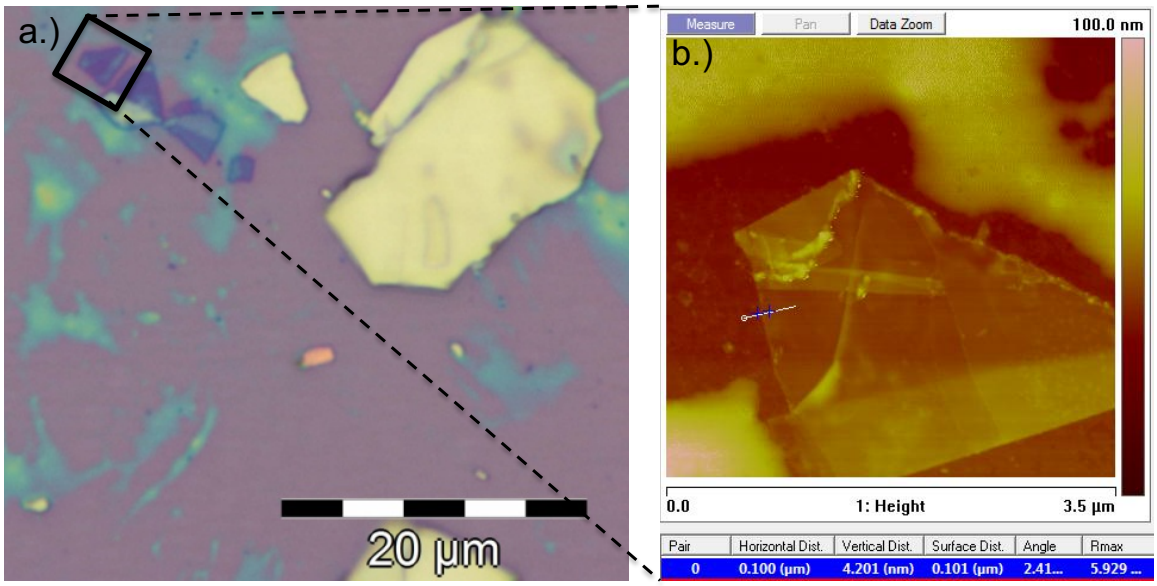

Figure 2.3.2: Thin flake characterization: a.) Optical and b.) Atomic Force Microscope images of a 6 nm-thick exfoliated Bi_2Se_3 flake

use of predefined patterns on a photomask, whereas EBL is used for custom designs, in which the beam writes out the circuit according to a CAD file. Metal electrodes are evaporated onto the lithographic patterns using a diffusion vacuum pumped thermal evaporator. Following the metal evaporation,the samples are placed into an acetone bath (at 60 C) for lifting off the photoresist. The entire fabrication process takes on average one week for a round of samples, but can be done in one day to minimize the samples exposure to air.

2.4.1 Electron beam lithography of micron-sized contacts

To prepare samples for EBL exposure, substrates with selected crystals are spin-coated first with a copolymer (MMA 8.5 MAA) at 4000 rpm for 60 seconds. They are

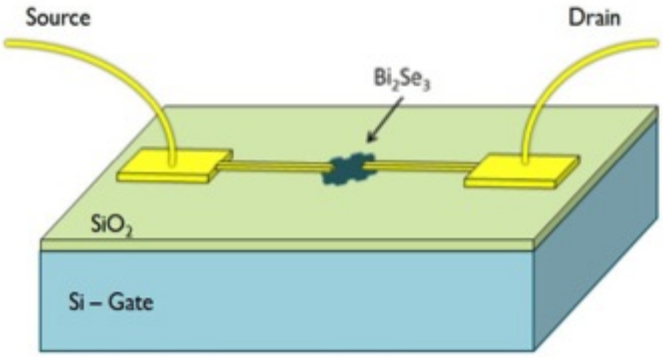

Figure 2.4.1: Source and drain electrodes physically contact the Bi_2Se_3 crystal, while the gate is capacitively coupled via the SiO_2 dielectric film.

then baked at 170 C for 15 minutes, then spin-coated with another layer of PMMA 2% at 2000 rpm for 60s, and given another 15 minute hard bake. This bi-layer resist technique adds resolution to the exposure by the fact that the 2 layers will absorb energy and develop at slightly different rates. This results in what is called an "undercut", which helps to have clean metal liftoff for narrow and close together electrodes (distances here of the order of 1 μm).

The electron beam lithography system we used is a Hitachi SU-70 with a thermal emission Zinc Oxide coated tungsten tip. EBL contact patterns are designed in the lab beforehand using the Nanometer Pattern Generation System (NPGS) software, by overlaying computer designed grids on optical images of device candidates. Circuit patterns can be tested with a mock exposure before final execution. The EBL system uses a 20 kV voltage, accelerating the beam electron through a focusing aperture onto the sample. The sample chamber is under high vacuum (1×10^{-8} Pa). The Gold-L reference markers are used to adjust the substrate rotation and align the

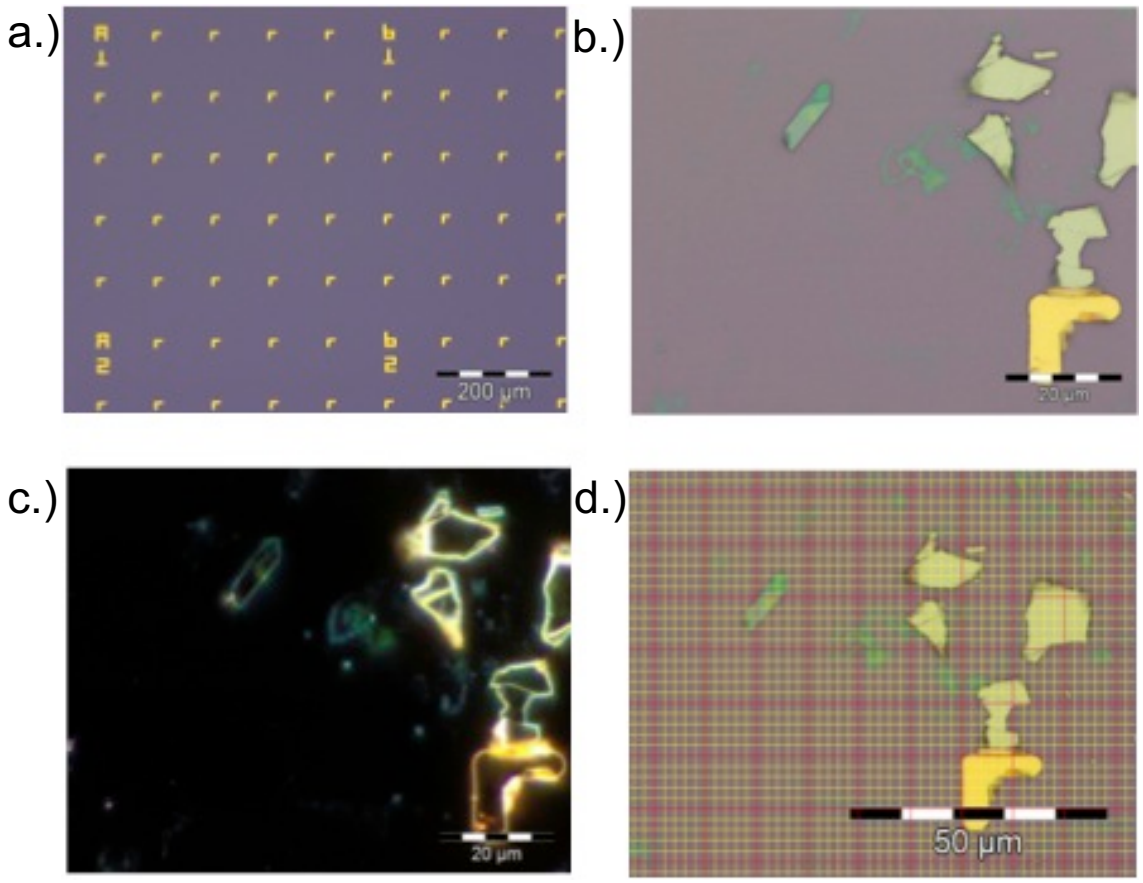

Figure 2.4.2: a.) Prepatterned Gold reference grid for flake location b.) Bi_2Se_3 flakes are exfoliated onto the grid c.) Dark field imaging shows surface and edge uniformity, suggesting the crystalline nature of the flake d.) Optical image overlaid with a digital coordinate system for CAD design of EBL electrodes

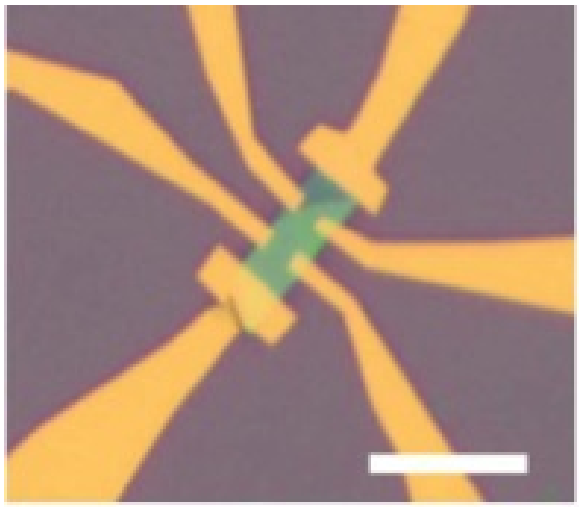

Figure 2.4.3: Bi_2Se_3 flake with Hall bar geometry after metal electrode evaporation (scale bar is 10 μm)

design file with the actual substrate via a global coordinate grid. Once the crystal position has been found, the beam is moved to a nearby empty space for focusing and stigma optimization. The electron beam must be blanked off during translations to avoid exposing the sample area. Once the coordinates have been verified and the beam is tuned, the system is put into automatic mode for exposure, which takes roughly half an hour depending on the area enclosed by the contacts. Once the exposure is completed the sample is removed from the vacuum chamber and developed. Due to the long time required to expose large contacts, generally only the fine electrodes contacting small crystals will be written using EBL, and larger electrode arms and contact pads will be added using standard patterns selected from one of our photomasks. This is done in another round of photolithography, using the MA4 photo-aligner. Chips are coated using S1813 photoresist and developed for

45 seconds in MF319 developer. Chips are then placed into a hand pumped vacuum container for transport, and are ready for metal deposition. A finished device is shown in Figure 2.4.3.

2.4.2 Metal contact evaporation and device packaging

Metal contacts are laid onto lithography patterns using our thermal evaporation system. Samples are loaded into a bell jar which is pumped down to a pressure of 5×10^{-6} Torr, evacuated by an oil diffusion pump backed by a roughing pump.

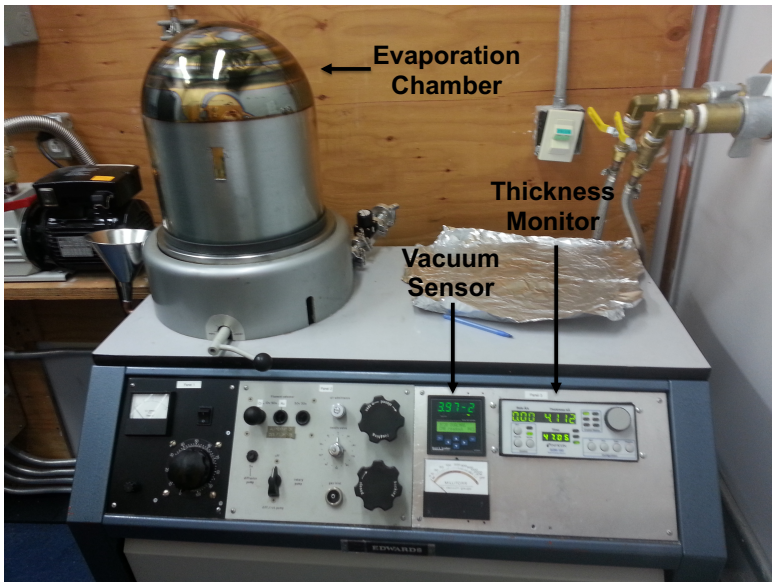

Figure 2.4.4: Metal deposition of the contacts is done using a diffusion pumped thermal evaporator

The sample stages are suspended face down above the source materials, in this case a chromium bar and a gold nugget placed in a tungsten-molybdenum boat. The electrical circuit is setup to pass current through one source at the time, using

an external switches enabling the chamber to remain under vacuum. The standard evaporation recipe used here calls for a 5 nm sticking layer of Chromium, followed by 80 nm of Gold contacts. The crystal thickness monitor shown in Figure 2.4.6 employs a quartz microbalance calibrated to each material to display live readouts of film thickness during deposition. This results in a high level of confidence and reproducibility in the deposited thickness across many evaporations, even though the deposition rates and times will vary. A shutter is opened between the source material and the lithographically patterned substrates once an acceptable deposition rate is achieved, and closed upon reaching the desired thickness. The bell jar is kept under vacuum while the source materials cool off, at which point the freshly coated substrates can be put into warm acetone for photoresist or EBL resist liftoff. At this stage the device is ready to be checked for electrical connection under a probe station and packaged for permanent safe keeping.

The prepared transistors are mounted onto a 24-pin carrier using conductive Silver paint, making electrical contact to the silicon backside of the substrate for gate connection. Once the metal contacts and back gate are connected the sample is susceptible to electrostatic shocks. It is at this packaging stage of microfabrication that the sample is at a high risk of being damaged. Utmost care is given to grounding during wire bonding and while transferring the sample to and from storage. Our WestBond wirebonder shown in Figure 2.4.7 uses a microscope and lever arm setup to scale down the user's movements, allowing delicate control of the ultrasonic tooltip.

Even with proper grounding safeguards for static electricity, the tooltip itself can

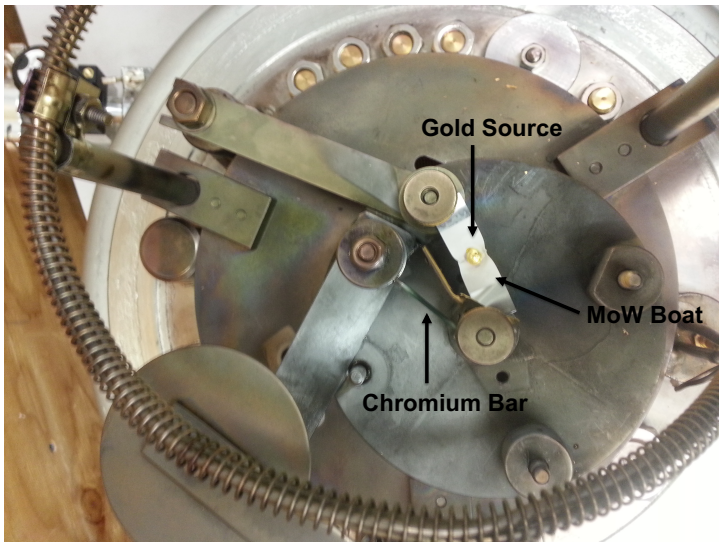

Figure 2.4.5: Current is passed through either a Chromium bar or a Gold nugget, creating metal vapour under vacuum

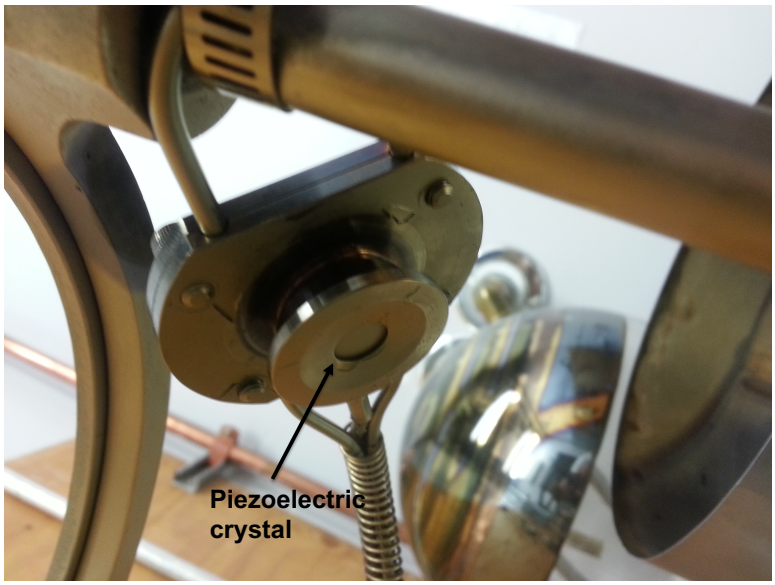

Figure 2.4.6: The resonance frequency of the crystal thickness monitor is measured by a RF circuit, and is sensitive to nanometer thick metal layers

Figure 2.4.7: Device packaging: our wire bonder scales down the users movements in order to precisely attach 25 micron thick Aluminum wires using an ultrasonic pulse

easily damage the contact pads and cause gate leakage if the ultrasonic power or stage height are improperly tuned. Aluminum wire is bonded from the gold contact pads on the SiO_2/Si surface to the chip carrier. The chip must be either transferred directly to a measurement probe or safely stored in anti-static GelPaks under vacuum until it will be measured (storage container shown in Figure 2.4.8). The attached wire bonds act as antennae for ambient electric fields, and for this reason the sample is generally measured immediately after packaging.

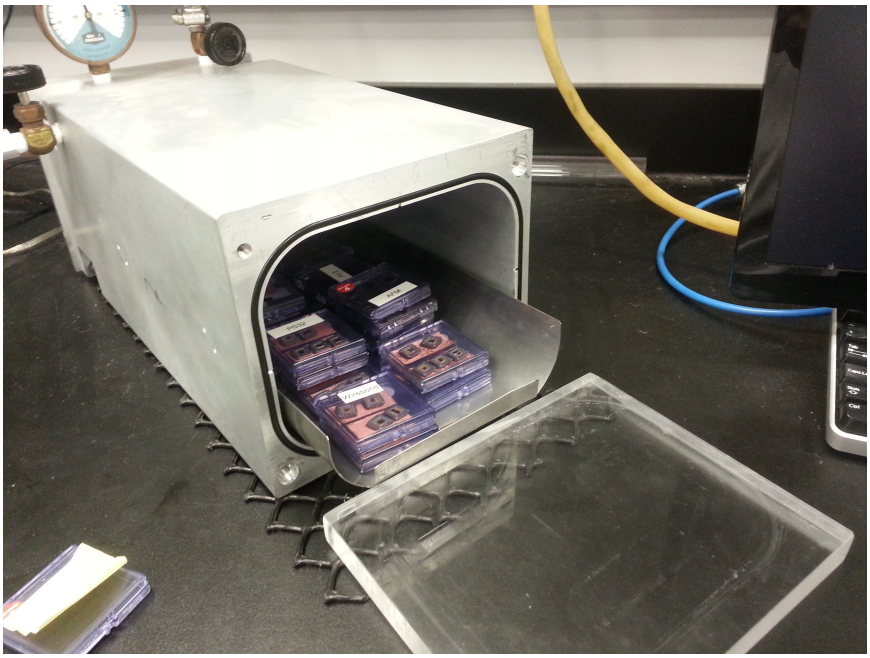

Figure 2.4.8: Prepared samples are stored under vacuum to minimize exposure to air

2.5 Electronic measurement setup and cryostat

While Bi_2Se_3 is known to display good thermoelectric properties across a range of temperatures [4], we aim to observe signatures of coherent 2D surface transport at

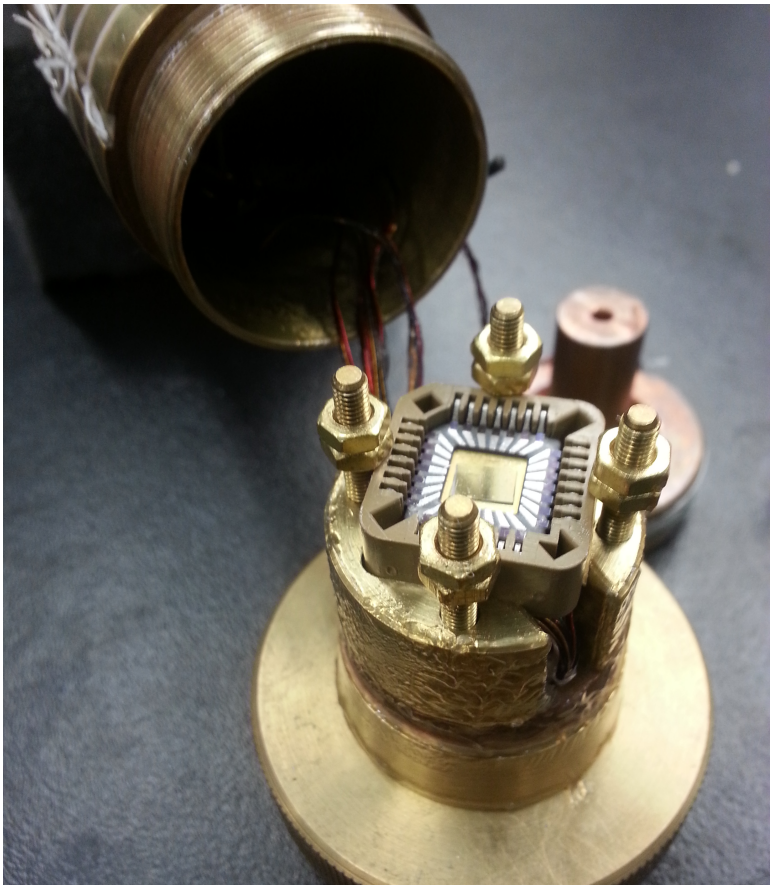

Figure 2.5.1: Sample testing: A packaged sample, loaded in the measurement probe of our ^{3}He cryostat

low energies. Due to the high signal sensitivity required to resolve delicate quantum effects, the samples must be cooled as much as possible. Taking transport data at cryogenic temperatures allows for precise electronic measurements due to the reduction of thermal fluctuations which add noise to the current. Figure 2.5.2 shows our liquid Helium-3 (LHe-3) cryostat, capable of reaching temperatures as low as 0.3 K. This cryogen free system recirculates LHe-3 and LHe-4 with no need of refilling. A cold trap freezes out impurities down to 77 K in the ^{4}He gas lines, and should be refilled with liquid Nitrogen (LN2) periodically. Packaged transistors are loaded into the sample probe shown in Figure 2.5.1 and tested electrically at room temperature. The probe stick is pumped to high vacuum and checked for leaks before loading into the fridge. The LHe-3 cryostat is also equipped with a 9 Tesla (-/+ 9 T) superconducting magnet for B-field studies.

Data is collected using a custom user interface and a National Instruments Data Acquisition system (DAQ). As static electricity poses a constant threat of sending a shock to the sample, a grounding strap is worn on the wrist and contact electrodes are left grounded between measurements. Different electronic circuit setups can be used depending on the type of measurement we would like to make. For making 2-point resistance measurements and taking gatesweeps, a DC circuit is used. In this configuration, the DAQ card is used as a bias voltage source, sending a source signal through a voltage divider towards the sample. The drain current goes through an Ithaco 1211 current preamplifier and sent to a desktop computer. Our custom

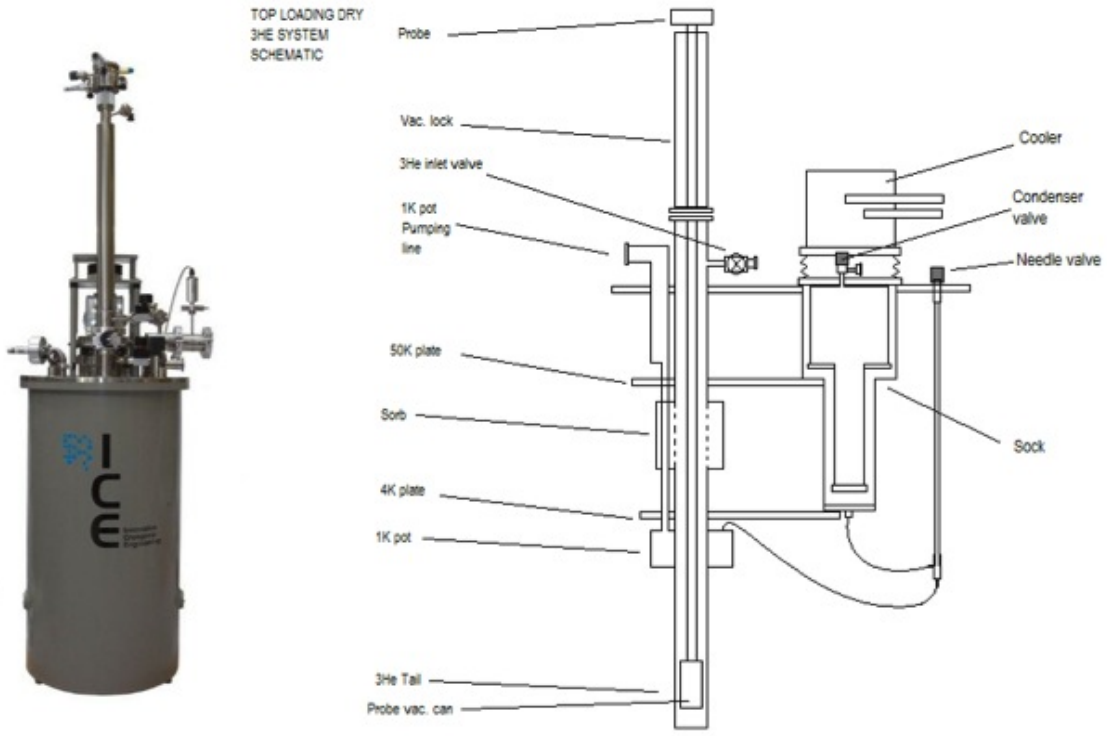

Figure 2.5.2: 0.3 K fridge: The LHe-3 cryostat has an inner sample space buffered by a LHe-4 pot held at 1.2 K. The needle valve allows controlling the flow of LHe-4

MotorCurve software plots the data sweep in realtime and saves the data in a text file to the hard disk. Sampling rates, time constants and sensitivities are optimized, and offsets zeroed to optimize the data. For instance, the rise time on the current preamplifier should be inversely proportional to the sampling rate. Usually an extra factor of 3 is introduced to prevent taking the same data point twice. A low pass filter on the Keithley gate source prevents high voltage spikes from reaching the sample. Data is analyzed using Igor Pro software. Using an AC circuit, we can directly measure the differential conductivity by using the low noise circuit shown in Figure 2.5.3. Using a transformer we add the signals of a DC and AC voltage sources. A lock-in amplifier syncs onto the source frequency of the AC signal, filtering out noise. In this fashion, we can make use of the lock-in amplifier's ability to take a precise reading of a small signal (μV range), while either sweeping the source/drain bias, or holding the bias constant and taking a gate voltage sweep. We use a SR560 voltage preamplifier to modify the circuit when taking 4-point data. In this chapter we summarized the deposition of thin films of Bi_2Se_3 on Si/SiO_2 substrates, and the patterning of electrical contact on them to create transistor devices. These samples are then loaded into a cryostat for electron transport measurements. In the next chapter we will discuss the electronic characterization of our samples and our solutions to the contact resistance problems faced by all research groups working on Bi_2Se_3 thin crystals.

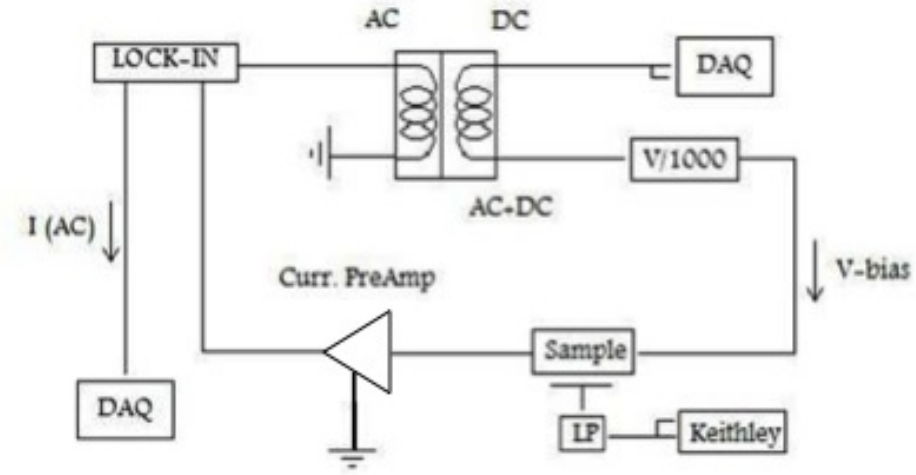

Figure 2.5.3: Our AC circuit uses a transformer to add an AC perturbation atop a DC source signal

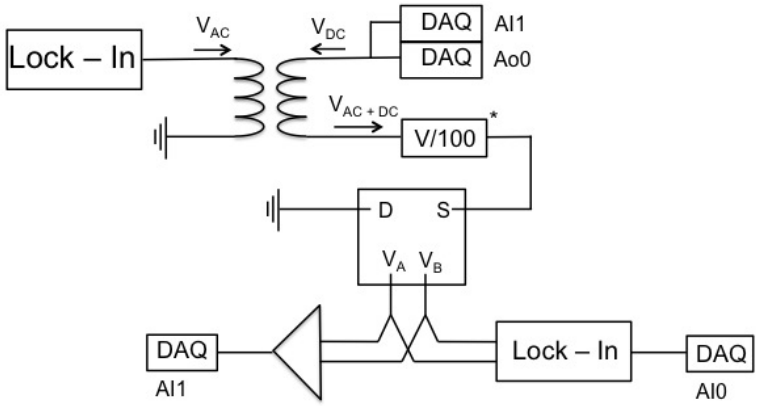

Figure 2.5.4: The 4-pt AC circuit uses a transformer to add an AC perturbation atop a DC source signal and measure the DC bias separately from the AC contribution

Chapter 3

Characterizing and optimizing electrical contacts to thin Bi_2Se_3 crystals

This project's main objective is to explore electronic transport in Bi_2Se_3 topological insulator transistors, and to distinguish bulk conduction from surface state conduction. Cleaved Bi_2Se_3 was chosen as the TI of interest due to its large bandgap of 0.3 eV which is topologically non-trivial as observed in optical experiments [9]. Now that we have fabricated thin film transistors, it is important that we ensure the quality of electrical contact to the Bi_2Se_3 crystal and trust that our transport data reflects the physics of the Bi_2Se_3 channel rather than the contacts before moving on to making magneto-transport measurements. It is known that the Bi_2Se_3 crystal surfaces oxidize in open atmosphere, creating Se vacancies and affecting the topological surface

transport [36]. Very few successful transport experiments have been reported in Bi_2Se_3 in large part due to the difficulty to make good electrical contacts to the crystal. We would like to investigate the effect of atmosphere exposure on the quality of our electrical contacts, and see if modestly oxidized crystals can be contacted with low resistance contacts. Device design elements such as the contact surface area and the crystal thickness are explored as parameters affecting the contact resistance. We also attempt various etches prior to contact deposition.

This chapter begins with section 3.1, where we present data for contact resistance on Bi_2Se_3 crystals in recent literature, and use these as benchmarks to achieve in order to be able to carry out magneto-transport studies on Bi_2Se_3 crystals. The measurement methods we use to characterize the contact quality of our Bi_2Se_3 transistors include both DC and AC + DC circuit configurations with either 2-point (voltage probes are also injecting and draining the current) or 4-point (separate voltage probes and current leads) contact geometries. In section 3.2 we discuss the problem of oxidation in Bi_2Se_3 thin films, and what can be done to minimize its effects. In section 3.3 we collect statistics on fabrication methods to understand that inter-dependence of the controlling factors are thickness, contact area, and we find that minimizing the amount of air exposure is the most important aspect to produce high quality Bi_2Se_3 thin film transistors. We show a decrease in 2-point resistances for samples on which we used a short plasma etch prior to metal contact deposition. We reach a satisfactory understanding of the optimization of Bi_2Se_3 transistors and show electrical contact resistance comparable to key references [30, 8]. In section 3.4

we discuss the effect of thickness on contact resistance. We are then ready to move on to studying samples' the magnetic transport properties of interest in Chapter 4.

3.1 Brief overview of electron transport in Bi_2Se_3 transistors

In this section we will present a review of selected theoretical and experimental aspects of electron transport in topological Bi_2Se_3 transistors. This information will be useful for discussing our data in Chapters 3, 4 and 5. Since the discovery of the topological insulator as a phase of matter, theoretical advances have abounded [1, 2, 38], while transport realization of devices lags behind [27, 7]. There has been some success, however, with a few groups achieving good contacts and interesting transport data. We will present some of these as references for the transistors we should aim to achieve in order to study the behaviour of topological insulators at low temperature and high magnetic field. Following this review we will present the results of corresponding contact resistance measurements taken on the devices we fabricated in Chapter 2. we evaluate the status of transport in these devices with respect to literature, the initial challenges faced, and outline the steps we took towards improving the contact to a satisfactory level.

3.1.1 Background on Bismuth Selenide transistors

The crystal structure of Bi_2Se_3 is made up of alternating layers of trigonal lattices made of Bi and Se. These layers are bonded into so-called quintuple layers (QL's) held together by Van der Waals forces (see Figure 3.1.1 (a)). The topological nature of Bi_2Se_3 follows from a parity inversion at zero momentum (the Γ point) in the first Brillouin Zone (FBZ). In quantum mechanics the parity transformation operator acts on the wave function ψ such as: $\boldsymbol{P}\psi(r) = e^{i\phi/2}\psi(-r)$. The operator is unitary and therefore must satisfy $\boldsymbol{P}^2\psi(r) = e^{i\phi}\psi(r)$, meaning that $\boldsymbol{P}$ is an internal symmetry of the system and rotates its eigenstates by $e^i\phi$. To illustrate this, consider any time-reversal invariant momenta Γ_i characterized by $-\Gamma_i = \Gamma_i + G$, where G is lattice vector in $k-$space (Figure 3.1.1 (b)) [26]. It can be seen that the $\Gamma-$point acts as a center for parity inversion in the BZ. In a Z_2 class topological insulator, one can take linear combinations of the quantum states giving either an even or odd parity (±1 refers to the combination being symmetric or antisymmetric under such a parity transformation). The parity invariant can be found by multiplying all parity eigenvalues at each momentum. The $\Gamma-$point is the only point which gives a -1 parity invariant, with all other points giving 1. This product of all points with time reversal invariant momenta gives -1, which ensures the bulk is a strong topological insulator [26].

The low-energy bandstructure of Bismuth Selenide is composed of surface states with a linear energy-momentum dependence that span a bulk bandgap. Spin-orbit coupling reduces the quantum degrees of freedom, the surface state dispersion exhibits

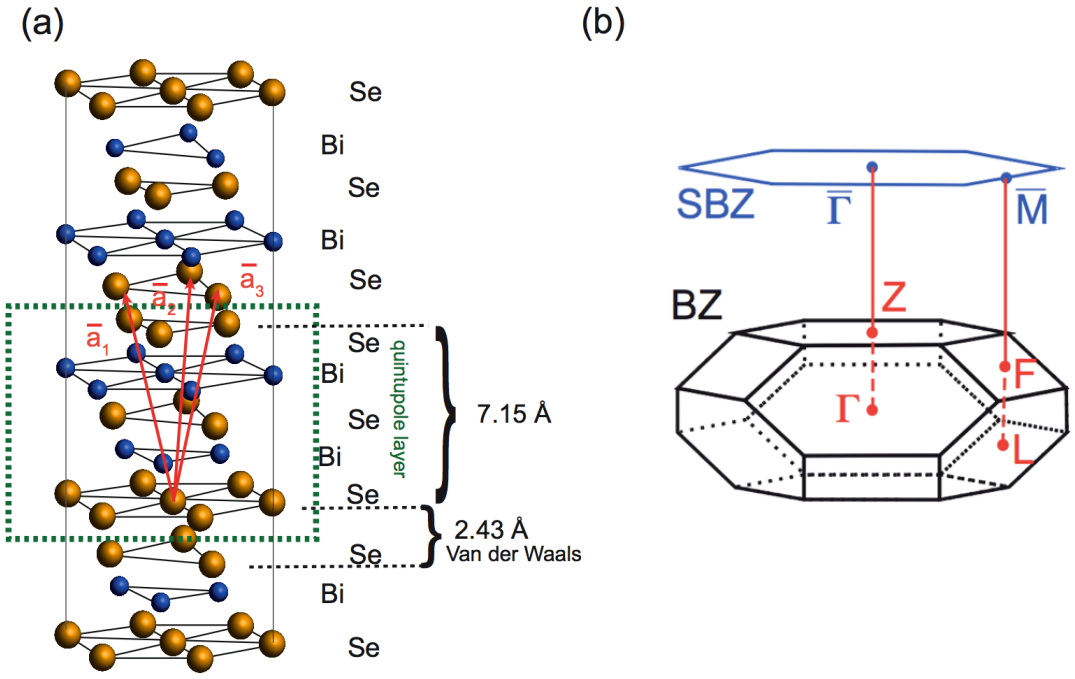

Figure 3.1.1: (a) The lattice structure and (b) the bulk and surface Brillouin zones of crystal Bi_2Se_3 Figure from *Bianchi* [26]

a single Dirac cone per surface compared to graphene's double spin degeneracy [8]. The effective Hamiltonian for charge carrying electrons on the surfaces of a 3-dimensional TI is given in equation (2):

$$H(k) = -Dk^2 + v_F(k_y\hat{\sigma}_x - k_x\hat{\sigma}_y) + (\frac{\Delta}{2} - Bk^2)\tau_z\hat{\sigma}_z + g\hat{\sigma}_z \tag{2}$$

The first term leads to band inversion (with non-trivial topology) when $B^2 - D^2 > 0$. The next two terms are for isolated surfaces (top and bottom surface of the crystal) with v_F the Fermi velocity of charge carriers, and σ's are the Pauli spin matrices:

$$\sigma_x = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix},\ \sigma_y = \begin{pmatrix} 0 & -i \\ i & 0 \end{pmatrix},\ \sigma_z = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix} \tag{3}$$

The τ_z term represents the coupling that occurs between opposing surfaces in film of sufficiently low thickness [13], with $\tau_z = 1$ and $\tau_z = -1$ representing the bonding and anti-bonding regimes, respectively. The hybridization gap Δ can be controlled by thickness, and is related to the inter-surface tunnelling time by $\tau_t = h/2\Delta$ [4]. This τ_t will play a role in the crossover from the Weak Localization (WL) regime to one where it is suppressed (discussed further in chapter 4). Here we do not approach the ultra thin regime of < 6 nm in which inter-surface coupling occurs (except maybe one device discussed in Chapter 4.3), and this coupling term can therefore be omitted. In the last term g represents the strength of the exchange field in the crystal. *J. Chen* et al. [20] showed that this term is negligible in Bi_2Se_3 as the strong spin orbit interaction suppresses the Zeeman splitting term, and so we leave this term out as

well. Upon these omissions we look at our effective, simplified Hamiltonian:

$$H(k) = -Dk^2 + v_F(k_y\hat{\sigma}_x - k_x\hat{\sigma}_y) \tag{4}$$

The conductive surface states can be thought of as semi metallic and spin-polarized as opposed to having both up and down spin states everywhere on the Fermi surface [28]. Figure 3.1.2 depicts (a.) the theoretically calculated, and (b.) experimentally obtained density of states for Bi_2Se_3. The bandstructure was observed in-situ using angle resolved photoemission spectroscopy (ARPES) on 10 nm-thick grown films [8].

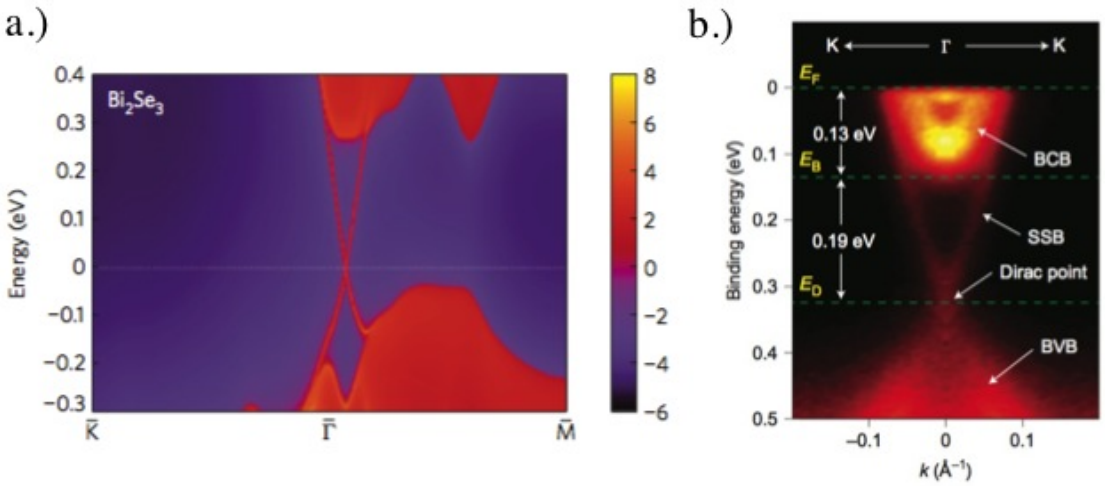

Figure 3.1.2: The band structure of crystal Bi_2Se_3: a.) Theoretically calculated local density of states [9], and b.) The bandstructure experimentally observed via ARPES [8]

While the surface states are theorized to be topologically protected, these states are difficult to realize in practice due to selenium vacancy defects in the bulk layers. These vacancies add free charge carriers which n-dope the sample and wash out or

dilute the surface state signal [8]. Selenium vacancies arise during oxidation of the crystal when the surface is exposed to open atmosphere. We expect that thicker crystals will show little or no gate-voltage tunability of the Fermi level of the 2D surface states due to screening from the bulk layers. Our goals are first to make low resistance contacts to the crystal surface, then search for evidence that the transport is across the contacted surface, the bulk layers, or some mixture of the two. Evidence for surface transport can be found in the thickness dependence of the crystal's resistance and in magneto-transport [29, 14]. The effects of sample thickness on the device resistance will be discussed further in section 3.4. Next we look at what has been achieved recently in transport experiments on Bi_2Se_3, and what difficulties remain in the field of experimental transport in topological insulators.

3.1.2 Bi_2Se_3 transistors: recent results and challenges

Topological insulators are a playground for theoretical physicists yet remain difficult to study experimentally due to fabrication challenges. Here I present some of the few examples in recent literature of working Bi_2Se_3 transistors that show magneto-transport behaviour. I will discuss how these devices are characterized electronically, and compare them to the fabricated devices. The purpose is to show a roadmap towards improving contact and device performance.

The first and simplest measurement to characterize a sample is to measure its 2-point resistance. The resistance is obtained from the slope of y-axis current versus x-axis source-drain bias voltage (V_B) graph. The $I-V_{bias}$ plot shows whether the gold

electrodes have made good contact, and if the crystal is conducting. The source-drain voltage is initially set to a modest range (such as -10, +10 mv) to avoid damaging or heating the sample. Output current is typically in the microamps range for a sample with kΩ resistance.

Taking a look at contact resistance in recent literature, *M. S. Fuhrer* et al. achieved a Bi_2Se_3 sheet resistance of 140 Ω/sq and a contact resistance of 176 Ω (on a 70 nm-thick crystal). Contact patterns were etched using N_2 plasma before evaporating Cr/Au (10/100 nm) metal contacts [30]. *H. Peng* et al. measured bias sweeps on a 10 nm-thick sheet of Bi_2Se_3, epitaxially grown on a mica substrate. Researchers found a sheet resistance of 330 Ω/sq with a contact resistance of 30 Ω per contact. Contacts were evaporated Cr/Au (5 nm/50 nm) [8]. These benchmarks provide a target for us to achieve in order to be in line with the best experimental research to date.

Here we discuss representative $I - V_{Bias}$ and $I - V_{Gate}$ for as fabricated Bi_2Se_3 transistors from Chapter 2. Despite efforts to select suitable device candidates based on optical and atomic force microscopy, samples must ultimately be characterized via electron transport. What we are looking for are devices that have a high signal to noise ratio, and ones with low enough contact resistance such that it does not dominate the transport. Following microfabrication, another hurdle we had to be overcome was gate leakage. It often reduced the sample yield below a useful level. Gate leakage occurs when the insulating oxide on the substrate breaks down and one or more of the gold electrodes contacting the crystal making a connection to the gate

electrode. This short circuits the device and makes it unfit for transport studies. Gate leakage can occur due damage to the oxide layer, or electrostatic damage. A device with an undamaged oxide should be able to withstand gate voltages up to 60 V without problem. Any small scratch on the surface of the substrate will increase the probability of gate leakage. Thus, care must be taken to transport unmounted chips in GelPaks so that they do not touch one another, as their sharp edges can easily scratch the surfaces. Plastic tipped-tweezers are used for handling the substrates during fabrication to protect the oxide layer. The main source of oxide damage was wirebonding (see Chapter 2.4.2). The metal tooltip we use is sharp and can poke right through the 80 nm-thick contact pads. If the ultrasonic power is not tuned such that the first attempt at bonding is a success, successive attempts will often tear the gold film from the surface. This leaves exposed areas of SiO_2 that are susceptible to scratching by the tooltip. Figure 3.1.3 shows an example of a thin (12 nm-thick) film device which shows gate leakage:

Oxide breakdown is rarely caused by electrostatic shocks for on-substrate samples (i.e. not suspended) since the gate is protected from short voltage spikes by a low-pass filter in the circuit. The main causes of gate leakage are fabrication related. The diagnosis of the problem, however, can only be done through the electrical testing of the device. This is why the sample is tested upon loading into the probestick at room temperature, thereby avoiding going through the lengthy cool down process only to find that the sample is faulty.

Looking at the transport data for this sample, the bias sweep (shown in Figure

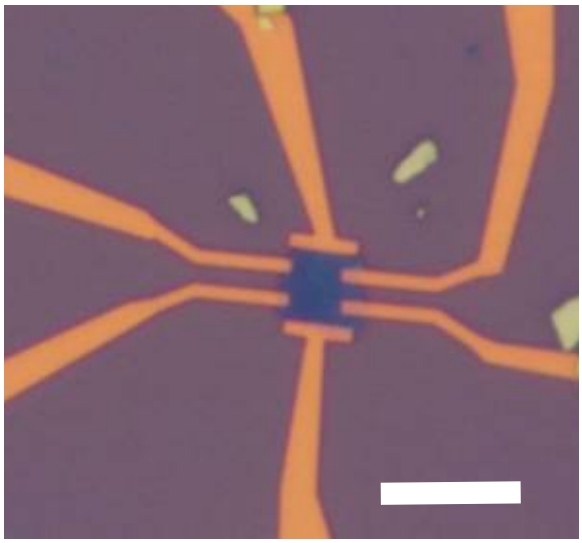

Figure 3.1.3: Ultrathin Bi_2Se_3 crystal with EBL defined contacts (Scale bar = 10 μm)

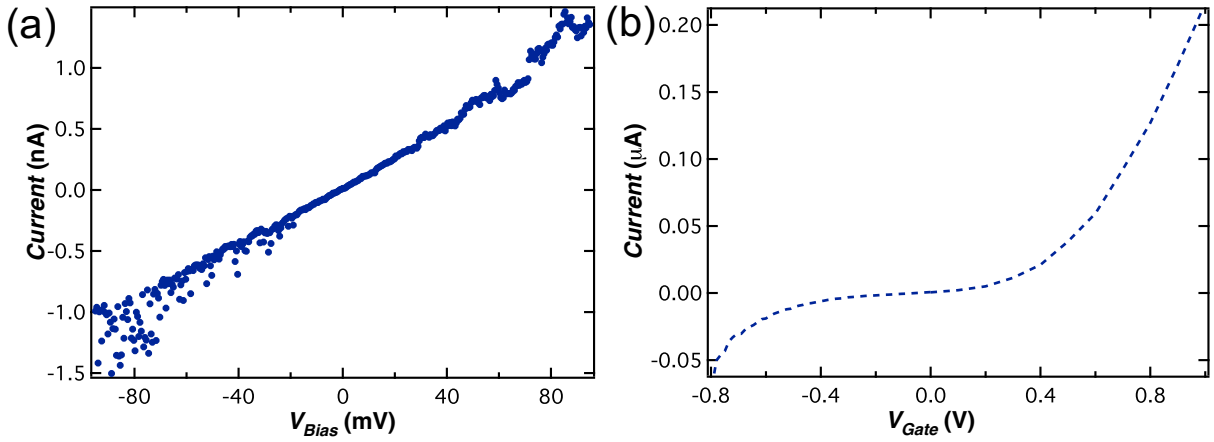

Figure 3.1.4: (a) A 2-point bias sweep reveals a large resistance $R = 74$ MΩ, and shows disorder, (b) With constant source/drain voltage, the gate voltage is swept over $\pm$ 1 V. A breakdown of the SiO_2 substrate leads to the backgate making a current connection directly to the gold electrodes

3.1.4 (a)) alone shows that a few things are wrong; it deviates from a linear line shape at higher biases, and gives an extremely high device resistance (74 MΩ). The high resistance could possibly either be due to the extremely low crystal thickness, high contact resistance of leakage from source to the gate such that no current reaches the drain electrode. This can be clarified by $I - V_G$ data (Figure 3.1.4 (b)) current versus V_G data. This means that the device is shorted by leakage to the gate electrode, i.e. no current passes through the actual crystal. Such a sample cannot be studied. Repeated tests showed that the wire bonder we were using was causing many cases of gate leakage, so we carefully re-calibrated the instrument. We found that the highest bonding success rate occurred at a power/time setting of 700 mW/500 ms. Stage levelling and height adjustments are also extremely important settings when it comes to bonding to the delicate gold films without damage. Figure 3.1.5 shows the $I - V$ plot for sample G. This thick flake (estimated thickness 600 nm) should be n-doped due to bulk defects and its channel having a low resistance. From the slopes of two bias sweeps using different sets of contacts (all other unused contacts would be floated during the sweep), we measure resistances respectively of 58 kΩ and 1.8 MΩ.

These high device resistances are very likely due to the contacts, and not the actual Bi_2Se_3 crystal. By the fact the the two values differ by a factor of more than 20x, we can rule out the possibility that these are readings of crystal resistance simply by a geometric factor (contact geometry could account for a L/W ratio of up to 3x). Further, if we apply a constant bias voltage (20 mV) and vary the back gate voltage, we obtain a gatesweep plot that shows the carrier density on the crystal is relatively

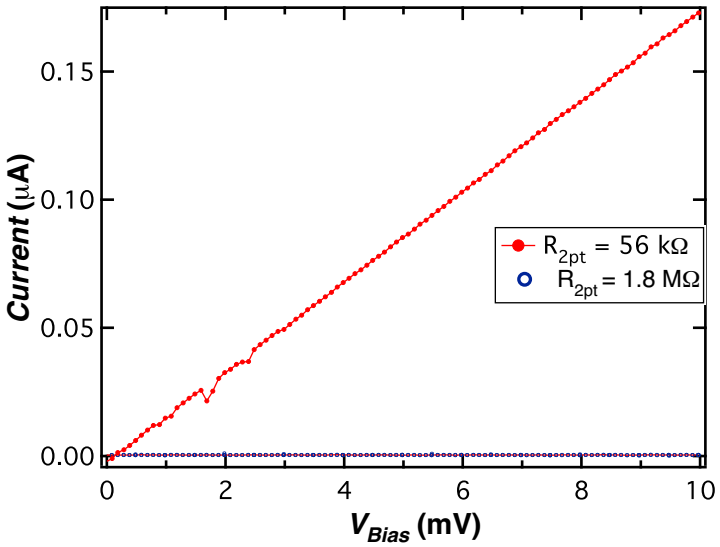

Figure 3.1.5: $I - V$ plot shows a linear source/drain dependence. 2pt resistance is extracted from the slope

unaffected in a 120 V range (see Figure 3.1.6).

It is not surprising that this sample shows no gate tuning of the resistance given the thickness and measured resistance of the device. To make gate-tunable devices we need to make contacts with a lower resistance on thinner crystals. High contact resistance can arise from a number of factors. One of the main causes is that immediately after bulk Bi_2Se_3 is cleaved in air, it begins to oxidize. High R contacts can be due to an oxide barrier between the gold contacts and Bi_2Se_3 crystal. We next try to better quantify this oxidation effect and determine a microfabrication route to make low-resistance devices.

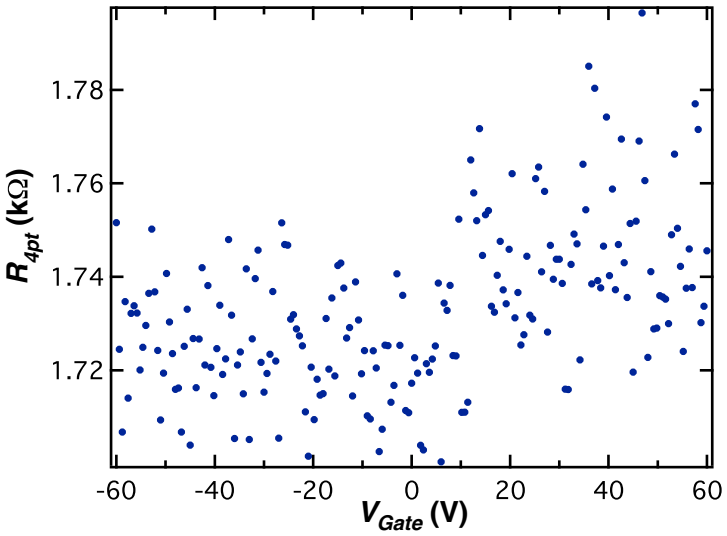

Figure 3.1.6: With a constant source/drain voltage applied, the 4-point resistance does not show gate dependence

3.2 Quantifying the impact of surface oxidation on contact resistance

Along with many other topological insulators, Bi_2Se_3 belongs to the halcogenides compound group known to be highly reactive with oxygen [36]. Unlike other halcogenides whose cleaved surfaces are generally inert, Bi_2Se_3 will react with oxygen in the open air to the point of complete crystal degradation. Figure 3.2.1 shows two images of the same crystals taken a few months apart. In the meantime, the crystals had been continuously exposed to air. One can clearly see the devastating effect this exposure had on the crystals. Exfoliated flakes of Bi_2Se_3 were etched away, from hundreds of nanometers to only a few or no quintuple layers. By optical microscopy alone it is easy to see the drastic change in colour due to thickness changes, from an

opaque yellow to varying shades of green and blue indicative of sub 50 nm thicknesses. The flake above and to the left of the C7 marker appears to be the thinnest in the left picture, judging by it's smooth surface. In the right image there is almost nothing left of the crystal.

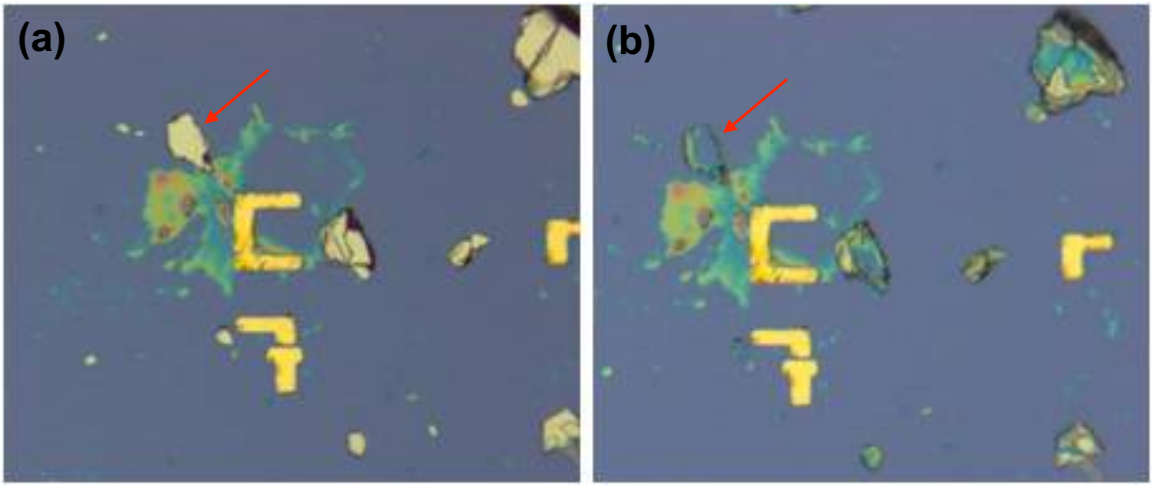

Figure 3.2.1: (a) Freshly exfoliated Bi_2Se_3 crystal flakes, (b) Left in open air for 3 months, the crystals are severely degraded

This is an extreme case of air exposure, as no sample intended for transport studies would be left in the open for so long. While long term exposure is observed to cause irreparable damages to the crystal structure, in this project we are concerned with the effect short term air exposure on the electron transport properties of the material. Short air exposures have been shown to cause an n-type doping, contaminating the surface state contribution to transport [21]. *D. Kong* et al. found upon conducting an X-Ray Photoelectron Spectroscopy (XPS) study that a native oxide growth occurs on Bi_2Se_3 for both nanoribbons and bulk crystals that have been exposed to air [7]. Figure 3.2.2 shows the XPS spectra for Bi_2Se_3 bulk crystals under vacuum. The

topmost spectra were taken on fresh crystal surfaces, transferring samples within 10s of cleavage into vacuum with an inert N_2 gas flux. Adjacent to the expected Bi_2Se_3 peaks, the oxidized form of Bismuth BiO_x appears small following cleavage and increases with continued exposure time. The BiO_x grows over a period of 2 days to the point of surpassing the Bi_2Se_3 signal. This corresponds to the formation of a layer of oxide on the crystal surface with an estimated thickness of 0.38 nm at the outset to an estimated 1.94 nm after 2 days. The appearance of the small BiO_x signal in the initial spectra indicates that the surface of freshly cleaved Bi_2Se_3 begins to oxidize very quickly. The fact that SeO_x is also observed (Figure 3.2.2 (b)) suggests that the oxidation diffuses into the crystal, affecting both the Bi and the Se crystal planes within a quintuplelayer. *Kong* et al. propose a transport model where carriers from the bulk layers and the surface oxide layer both contribute to the transport signal along with the topological surface state. How much each one of these different regions appears in the measurements depends on the thickness of the sample and the amount of oxygen exposure it received. These researchers found that a short Argon (Ar) ion etch (5 min, 10 mA, 5 kV) resulted in a reduction of the oxide peak to about 19% to 13% weight (middle panels, Figure 3.2.2). This means that the crystal's surfaces can be improved prior to transport studies even if a significant oxidation took place.

In the next section we will test plasma etching on our sample, but for now we take a look at the effect of the duration of air exposure on the sample resistance. To compare against the sample discussed in section 3.1.2 (sample G, with R_{2pt} =

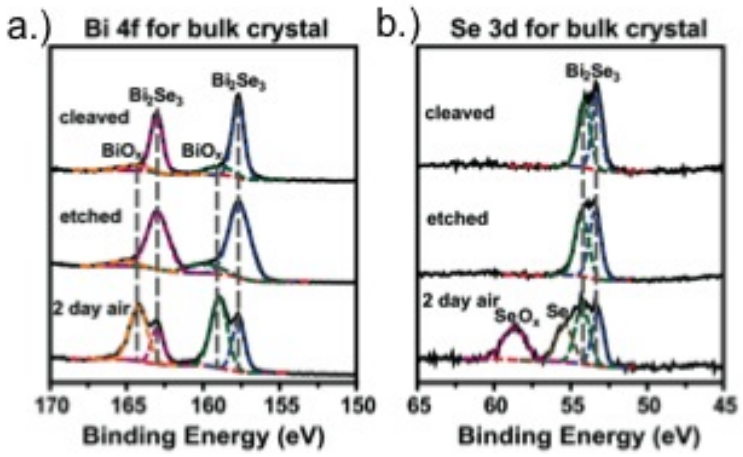

Figure 3.2.2: (a) Bi and (b) Se XPS Spectra for Bi_2Se_3 shows the formation of an oxide layer over 2 days, with both Bi and Se binding to Oxygen in the air. Samples etched with an Argon plasma (middle panel) display a reduction in the level of oxidation [7]

56 kΩ) we present another sample fabricated with only a moderate exposure to the atmosphere. The exposure time was limited to 20 days, corresponding to roughly half the time of sample G, which was approximately 6 weeks.

Figure 3.2.3 shows the 4-point device sample B, which is roughly 291 nm-thick, as recorded by AFM. Intuitively, the lower thickness of sample B compared to sample G (600 nm) should correspond to fewer layers of parallel conduction and a higher resistance. In fact, the measured resistance of sample B of Figure 3.2.4 is dramatically lower than for sample G.

Everything about the fabrication process was the same for these two samples, from lithography recipes to metal electrodes, excluding only the time of air contact. With the 2-point signal coming from a combination of the crystal itself and the contact resistance at the metal-surface interfaces we decomposed R_{2pt} into its constituent

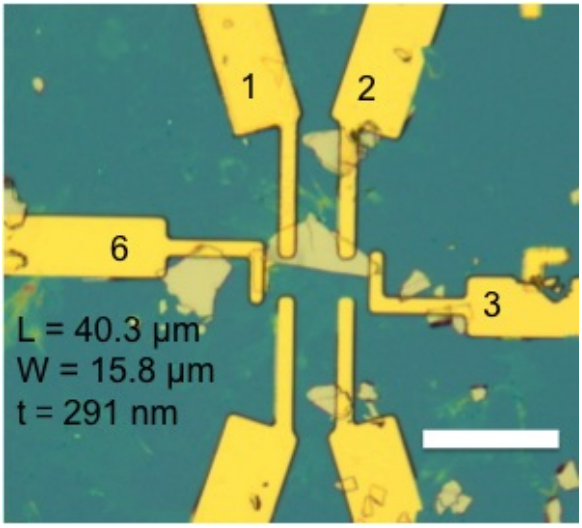

Figure 3.2.3: 4-point sample B, fabricated with moderate air exposure (20 days)

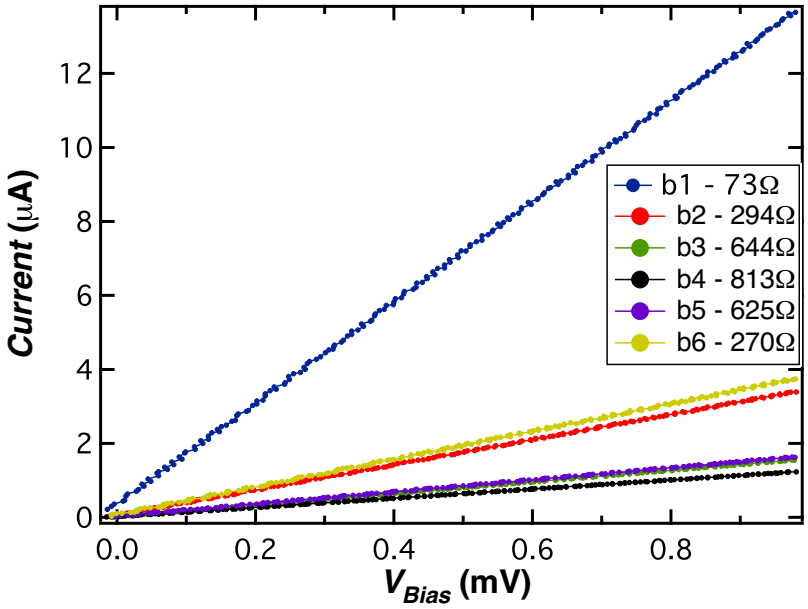

Figure 3.2.4: Current-Bias curves show a significantly lower resistance compared to sample G

parts:

$$R_{2pt} = R_{Crystal} + R_{C1} + R_{C2} \tag{5}$$

Where R_{C1} and R_{C2} are the series contributions to the resistance due to the contacts at each of the two metal-Bi_2Se_3 interfaces. In principle, it is difficult to ascertain how much of the signal is coming from the crystal and how much is due to contact resistance with only 2 contacts. However, devices patterned with 4 or more contacts permit a more accurate calculation of Bi_2Se_3 sheet resistance via the Van der Pauw method [37]:

$$\rho_{VdP} = \frac{\pi d}{2ln2} \frac{R_{AB,CD} + R_{BC,DA}}{2} f(\frac{R_{AB,CD}}{R_{BC,DA}}) \tag{6}$$

where the sheet resistance ρ_{VdP} can be measured directly using a $4-$contact geometry. The $4-$pt resistance $R_{AB,CD}$ refers to the resistance value attained by dividing the voltage measured across contacts A and B with the current flowing between contacts C and D. The measurement orientation is then rotated, and the 2 resistances are averaged. The correction coefficient f is a function of the ratio of $R_{AB,CD}/R_{BC,DA}$, which varies from 0 to 1. Another method can also be employed for devices with multiple contacts. By constructing a system of linear equations for each set of 2-pt resistances, one can determine the resistance of each contact, as well as the Bi_2Se_3 sheet resistance. Using the bias sweeps from sample B as an example, we constructed the linear system of equations of the type shown in equation (6). Here,

the $R_{Crystal} = \frac{L}{W}\rho$, and we solve for the sheet resistivity, ρ and compare it with the one from the Van der Pauw method.

$$\begin{bmatrix} 1 & 0 & 0 & 1 & 1.05 & 769 \\ 0 & 1 & 0 & 1 & 1.07 & 581 \\ 0 & 0 & 1 & 1 & 1.07 & 600 \\ 1 & 0 & 1 & 0 & 1.17 & 250 \\ 1 & 1 & 0 & 0 & 1.19 & 226 \end{bmatrix} \tag{7}$$

The bias sweeps provide linear equations of the form $aR_{C1} + bR_{C2} + cR_{C3} + dR_{C4} + (L/W)\rho = R_{2pt}$. Reducing the matrix gives a value of $\rho = 9.12\ \Omega$, compared to $\rho_{VdP} = 10.6\ \Omega$, giving an error of about 15%. This provides an alternate means of deriving the contact resistance, given a sufficient number of independent equations. In order to compare contact resistance between samples, we introduce the quantity "R-square", denoting the contact resistance per square micron of contact area, defined as:

$$R_{SQ} = (R_{2pt} - R_{4pt}) * \frac{A_1 A_2}{A_{tot}} \tag{8}$$

where A_1, A_2 are the respective areas of the two contacts, and A_{tot} is the total contact area, $A_1 + A_2$. We make the assumption that each square of contact area conducts in parallel, making up the series contributions to the $2-$point resistance shown in equation (6). Using this method, we extract the contact resistance for many samples made with varying air exposure times. The histogram in Figure 3.2.5

shows the correlation between contact resistance and the time of exposure to air.

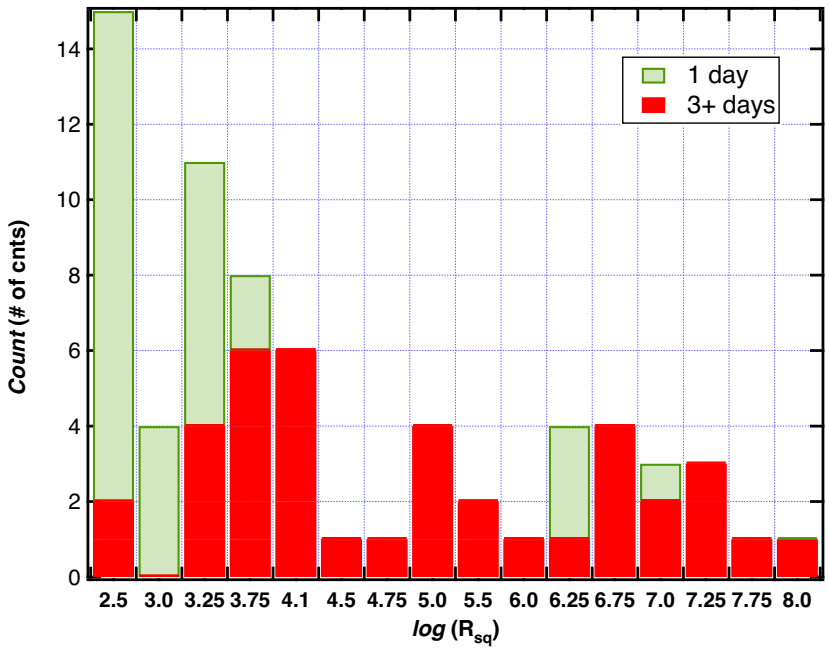

Figure 3.2.5: Histogram showing the number of low resistance contacts is increased by limiting the time of air exposure to 1 day

The 4 outlying high resistance contacts observed with low exposure time in Figure 3.2.5 are from a sample which was extremely thin (roughly 25 nm). This suggests that the contact resistance depends not only on the surface area of the metal/crystal overlap, but also on the thickness of the Bi_2Se_3 flake. Thicker flakes have a larger number of n-doping impurities [7] which can both dope surface states and the bulk, leading to lower contact resistance. Figure 3.2.6 shows the exponential relationship we measured between the contact resistance and the product of contact area $\times$ sample thickness in two different samples. The resulting units of this multiplication are μm^3, relating to a contact volume rather than an area, suggesting bulk doping of surface

conduction. Both these samples had a low exposure time, the difference between the two fits is likely to arise from the difference in sample thickness. The sample for the red curve in panel (a) is much thicker at 352 nm, compared to 22 nm and 38nm in panel (b) (this device has a step edge resulting in two thicknesses in one sample) for the green curve. With a factor of 10 times different thickness, the thin sample in panel still shows the same thickness dependence, consistent with bulk doping.

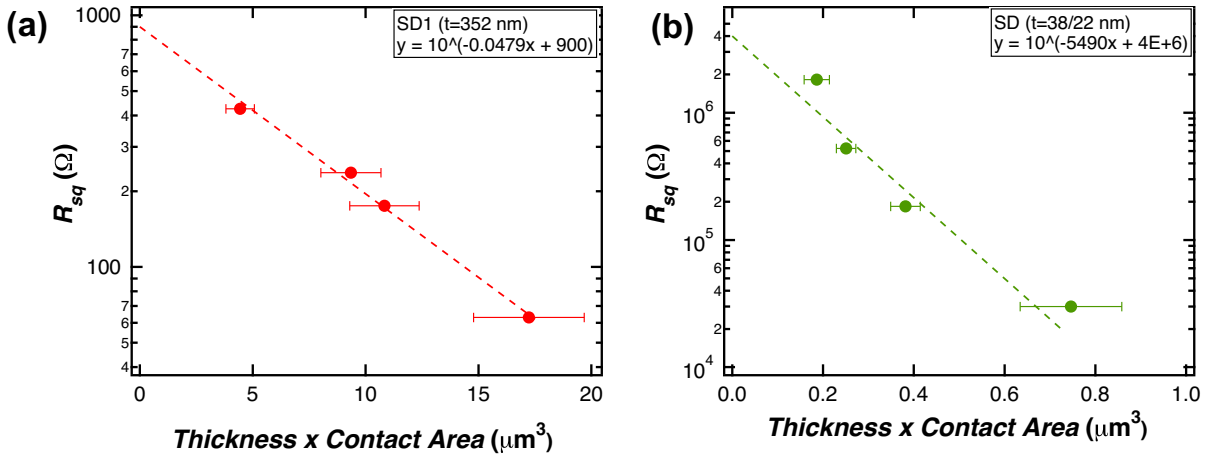

Figure 3.2.6: In two samples of thickness (a) $t = 352$ nm and (b) $t = 38$ nm, 22 nm, the contact resistance per unit area scales logarithmically with the volume of the contact, defined by contact area times sample thickness.

This could mean that unless the sample thickness is very low (< 20 nm), the contact resistance is similar for a range of thicknesses. Next we address the means of dealing with contact resistance caused by exposure to air.

3.3 Contact resistance vs microfabrication techniques

To minimize contact resistance, we tested several fabrication techniques with varying degrees of success. In light of what was learned in the previous section, it seems paramount to minimize crystal doping from exposure to oxygen. Beyond the simplest approach of limiting exposure time, several methods were tried in order to reduce the effect of oxidation. The first method was to etch a few nm off the top of the SiO_2 substrates prior to crystal deposition. The idea was to remove the water layer trapped in the top layer of SiO_2, and therefore reduce the amount of oxide of the bottom surface of the crystals upon deposition. Substrates were etched with 2 recipes. The first etch was done by cleaning the wafer using a reactive ion etching with the recipe of 20 sccm O_2 at 200 W and 200 mT for 12 minutes. The other method used was cleaning substrates with Trichloroethylene (TCE), which is a commonly used industrial solvent. Having a boiling point of 87.2 ^{o}C and being non-flammable, TCE presented a relatively safe option for chemical cleaning. Substrates were placed in boiling in TCE for 10 minutes before removing the heat source. In either case the substrate etching played a non-discernable role in device performance. This strongly suggests that transport in our devices is dominated by either or both top surface transport or bulk transport, but that the bottom surface contributes little. This can be rationalized by the fact that it is the top surface on which we deposit the contacts, and the bottom surface is in direct contact with a disordered SiO_2 film.

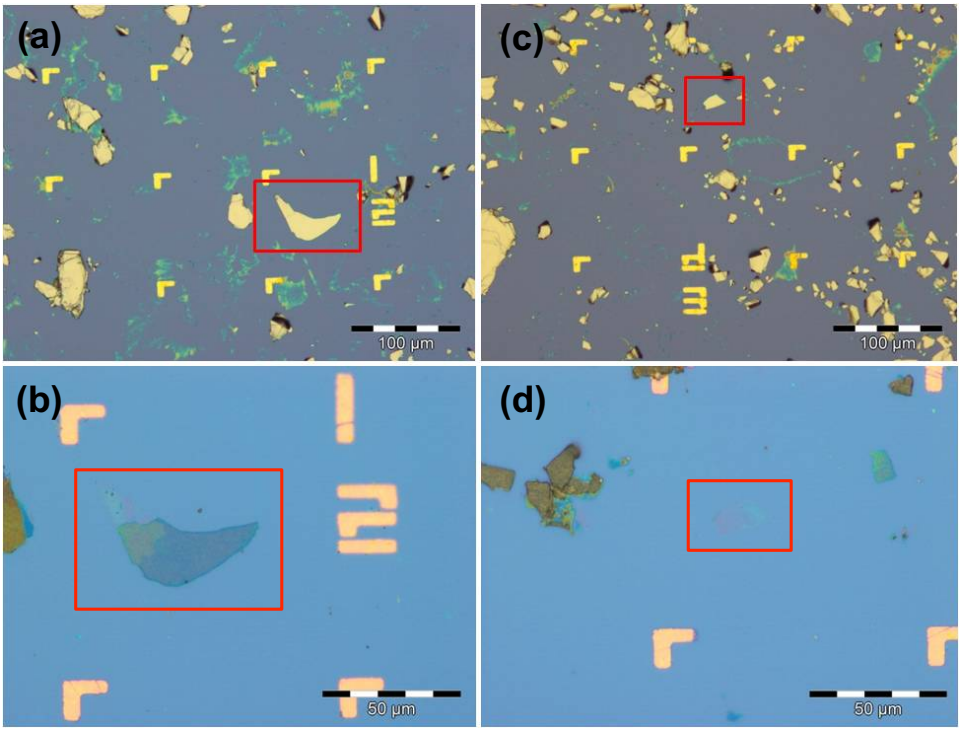

Figure 3.3.1: Non selective Argon plasma etches the surface of Bi_2Se_3 crystals: (a) An opaque flake of a higher thickness is reduced to the point of becoming translucent, shown in (b). The smaller flake in panel (c) is reduced to effectively nothing in (d)

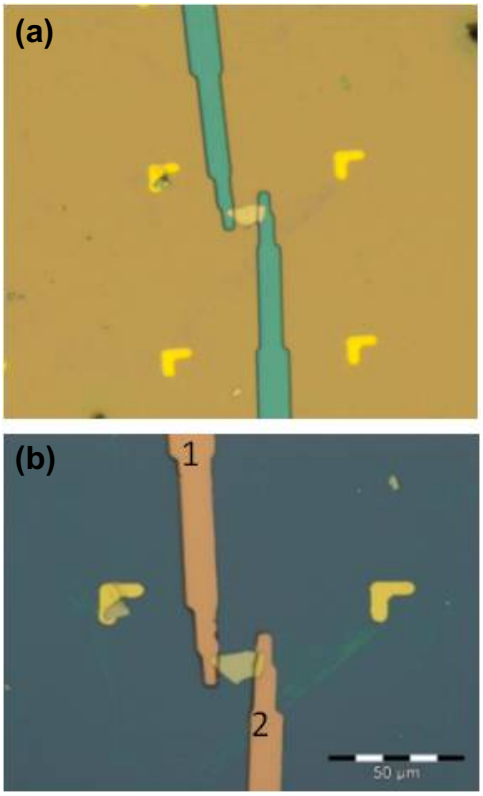

Figure 3.3.2: (a) After defining electrode positions using photolithography, a plasma etch is done to clean the exposed area of Bi_2Se_3 under the contacts (b) Metal electrodes are evaporated and the photoresist is lifted off, resulting in a sample with gold contacts on the surface

In terms of dealing with native oxide growth, again 2 methods were put to the test. The first being a 24 hour start to finish device fabrication as a means of minimizing air contact. This meant scotch tape exfoliation, photolithography, metal contact deposition and wire bonding all done in a single day. Once the device was packaged, it was pumped to a high vacuum and cooled to cryogenic temperatures for testing. The other method was to take crystals of varying exposure time and submit them to an RIE cleaning before contact deposition. A non selective Argon plasma etch under a flow rate of 2.5 sccm at 200 W and 75 mT was applied to devices after photolithography in order to clean the contact areas. Figure 3.3.1 shows a calibration test for this etching recipe. An AFM thickness measurement was taken before and after the RIE etching, giving a measured etch rate of 13 nm/min. During device fabrication, the etching was done between photolithography and metal deposition of the contact (Figure 3.3.2), using etch times on the order of $5 - 30$ seconds. Figure 3.3.3 shows a histogram of the measured R_C using these two fabrication techniques. These methods did not lead to any systematic R_C improvement.

As we saw in Figure 3.2.6 however, samples approaching the ultra thin limit are not easily contacted with low contact resistance due to the small volume of material under the contact. This was also apparent in Figure 3.2.5, and can be seen in the graphs in Figure 3.3.4.

Here we show that for thin samples ($t < 340$ nm), minimizing the exposure to air was insufficient to create very low resistance contacts. On the other hand, thick samples responded well to a reduction of air exposure, resulting in a good control

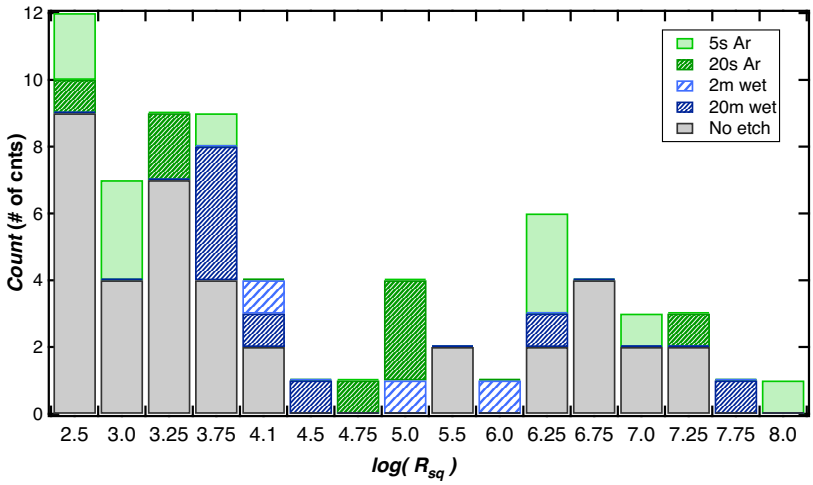

Figure 3.3.3: Number of contacts vs log(R_{sq}) for many devices whose contacts were made with 5s and 20s long Ar RIE etches, 2m and 20m TCE cleaning and without any additional contact cleaning

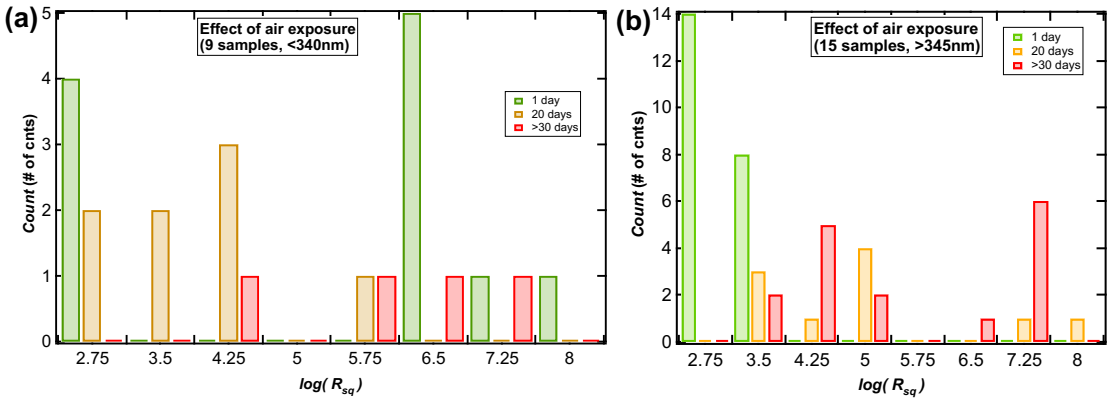

Figure 3.3.4: Contact resistance vs air exposure time: (a) For thin samples, minimizing exposure to air is insufficient to create low resistance contacts. (b) In thicker samples the contact resistance is reduced by minimizing air exposure

of contact resistance. The fact that thin samples with low air exposure times have high resistance contacts does not necessarily mean that the contacts are not good. We expect a large increase in sample (transistor channel) resistance with decreasing crystal thickness due to a reduction in doping from bulk layers. So as long as our contacts do not largely dominate the sample resistance, it is still possible to measure the crystal contribution to the sample resistance.

We aim to use transport (and magneto transport in Chapter 4) to distinguish the surface state contribution from the from bulk layer conduction, and from contact resistance. In the next section we look at a few ways this can be done in zero-magnetic field transport by using the gate electrode and thickness measurements.

3.4 Gating Bi_2Se_3 transistors and thickness effects

In an ideal topological insulator, perfect surface conduction is maintained by a complete suppression of bulk states. Band inversion topologically protects surface states while creating a bulk insulating bandgap, meaning a crystal of arbitrary size can support two-dimensional transport on its surfaces. In reality it is near impossible to achieve a perfect bulk insulating state, and there are always contributions to the conduction from the bulk layers beneath the surface. *Steinberg et al.* found the conductance of Bi_2Se_3 increases proportional to the sample thickness [14]. Taken at zero thickness this line fit gives the amount of surface conduction in the sample, $G(t = 0) = 200e^2/h$. This corresponds to a resistance of 64.5 Ω. If the linear fit is

accurate it can be used as a calibration curve for determining the crystal's thickness by measuring it's conductance.

Another approach to isolate the surface conductance is electrostatic gating. We naively expect that a back gate would only affect the bottom surface of the crystal, and screening from the bulk will wash out any gating effect on the top layer of very thick or highly doped devices. This may have been what is happening in the sample discussed in Figure 3.1.7, whose resistance was in the kΩ range. Taking a look at another sample with a much lower 2-pt resistance of 70.4 Ω, we observe a more pronounced gating effect, shown in Figure 3.4.2.

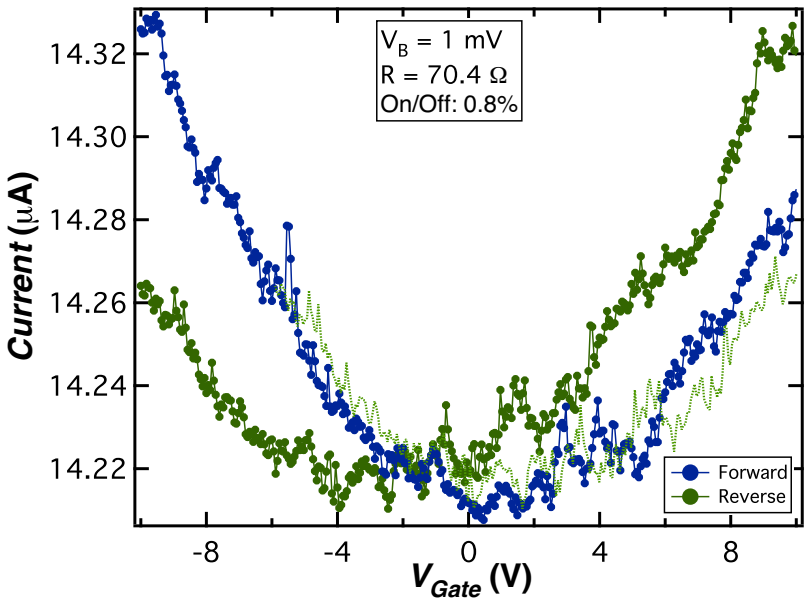

Figure 3.4.1: Current versus back gate voltage graph in a low contact resistance sample

The sample is low resistance, is close to the 200 e^2/h intercept for surface transport in Figure 3.4.1 and suggests that this sample is of low bulk doping. This allows the

effect of the gate to be noticeable amongst the bulk contributions. The gate affected portion of the signal is still small, at 0.8% the total signal, showing a large portion of the conductance is ungateable and therefore likely arises from the bulk layers. Assuming a parallel plate capacitor model, the change in carrier density induced by the gate may be calculated as follows:

$$\Delta n = \frac{C_G(V_G)}{eA} = \frac{\epsilon V_G}{ed} \tag{9}$$

where the sample capacitance, $C = \epsilon A/d$, depends solely on the device geometry, giving the change in carrier density to be $\Delta n = 7.19{\times}10^{10} cm^{-2}/V$. With $10\,V$ applied and observing a 0.8% change in resistance, it can be deduced that $7.19 \times 10^{11} cm^{-2}$ makes up 0.8% of the total density of $8.99 \times 10^{13} cm^{-2}$. We note that in most TI experiments a gate voltage up to 100 V is applied. In Chapter 4 we will discuss a device where the gating effect can reach up to 33%.

Chapter 4

Magneto-transport in Bi_2Se_3 and evidence for topological surface states

In Chapter 3 we learned that minimizing oxygen exposure is critical to obtaining good electrical contacts to Bi_2Se_3 thin crystals. Having an exposure time to air less than one day resulted in micron sized contacts with a resistance less than 1.7 kΩ. Samples could also be cleaned with RIE prior to contacting, and we achieved well behaved transistors with some gate control. To test for surface transport, we now make use of 3 high quality samples, which we study at low temperature and in high magnetic field. From these detailed magnetic-field studies we observe Classical Hall behaviour as well as Shubnikov-de Haas oscillations in our devices, allowing us to discriminate between 2D and bulk conduction. Tuning the Fermi level with the gate changes the Hall slope,

and suggests bottom layer screening of top layer transport. While a relatively thick (250 nm) sample displays a magnetoresistance which remains linear up to 9 Tesla, clear oscillations that are symmetric in B are observed in a thin (25 nm) sample. Low-field magnetoresistance is tested for weak-antilocalization (WAL), and shows no such effect. However, at high field we observe Shubnikov-de Haas oscillations, and the 2D carrier density is extracted via a Landau fan diagram. This fan diagram can also be used to infer whether or not the surface transport is topological (Berry Phase of π) or not (Berry phase of 0). We find that our data is not sufficiently precise to determine a Berry Phase, but does not rule out a phase of π.

While the state of scientific literature in this field is young, there have been some positive indications. H. Wang et. al observed a linear Classical Hall effect yielding a carrier density $n_{Hall} = 1.89 \times 10^{13}$ cm^{-2} and a mobility of $\mu = 316.6$ cm^2/Vs [16]. The sample studied was 5 nm thin film Bi_2Se_3 grown by molecular beam epitaxy (MBE). Weak anti-localization was also seen at low-field in the same device. In a report by *M. S. Fuhrer* et al., a 13 nm mechanically exfoliated Bi_2Se_3 was found to have a Hall density $n_H = 3 \times 10^{12}$ cm^{-2} and mobility 1100 cm^2/Vs. Researchers used an evaporated layer of p-doping material to counter the high n-doping in this material [5]. Both WAL and SdH effects allow calculation of the Berry's Phase which tells if the surface states are topological or not. We would like to see if WAL and SdH can be observed in our devices and what information they relate about the topology of the transport.

The outline of this chapter is as follows: in section 4.1.1 we present the samples to

be discussed throughout the chapter. In section 4.1.2 we extract the carrier density via the Classical Hall effect. We find a bulk density of $n_{3D}^{Hall} = 3.01 \times 10^{19}$ cm^{-3}, suggesting a highly n-doped crystal. Testing the low-field peak for WAL in section 4.2 rules out localization behaviour as seen in a quantum diffusive regime. In 4.3 we investigate the Shubnikov-de Haas oscillations in our device, allowing calculation of n_{2D} and a comparison of surface to bulk contributions. Finally, in section 4.4 we discuss the observation of fringe patterns and compare the data to interference peaks consistent with Fabry-Perot predictions.

4.1 Selected devices and classical Hall behaviour

In this section we present 3 devices selected from chapter 3 for their different thicknesses and low contact resistance. These devices will serve as the sample set for magneto transport studies, in search of evidence for surface transport. With 4 contacts we are able to measure either the voltage perpendicular to or parallel with the path of current, giving R_{xy} and R_{xx}, respectively. The first piece of the puzzle is to extract the carrier density from the R_{xy} vs B plot; the Hall slope. This can be compared with density values extracted from other methods. Not all samples display a linear magnetoresistance, which we attribute to a low thickness.

4.1.1 High quality Bi_2Se_3 transistors

In order to select devices for magneto transport studies, we use a few criteria. We want to study a range of varying thickness, to ideally be able to perform 4-point resistivity measurements, and to have a working gate electrode to tune the charge carrier density. Figure 4.1.1 depicts the samples to be studied in this chapter. Samples A and B are moderately thick flakes, with 4 or more low resistance contacts and gate electrode. Sample C is the same device as sample D, with a different contact orientation caused by an electrostatic cleaving of the top surface by the gate electrode. With a thickness of 38 nm, this sample is an order of magnitude thinner than samples A and B, presenting the opportunity to study the surfaces of thin film Bi_2Se_3 at low temperatures. Sample D has the unique quality of having a thickness step on its surface. AFM measurement confirms that while 4 of the contacts are on the thicker portion (38 nm), contacts 3 and 16 are contacting a section of the crystal that is only 22 nm. This allows us to study the effects of thickness within one sample.d

For the measurements in this chapter we use either a 2_{pt}, or 4_{pt} AC measurement. The circuit shown in Figure 4.1.2 shows the method of adding a small AC signal atop a larger DC voltage. In this way, we may use a Lock-In amplifier to isolate the AC signal and filter extraneous noise. This AC + DC method is suitable for acquiring low noise resistance vs magnetic field data.

Now that we have obtained a set of known samples we are set to study the effect of magnetic field on resistance.

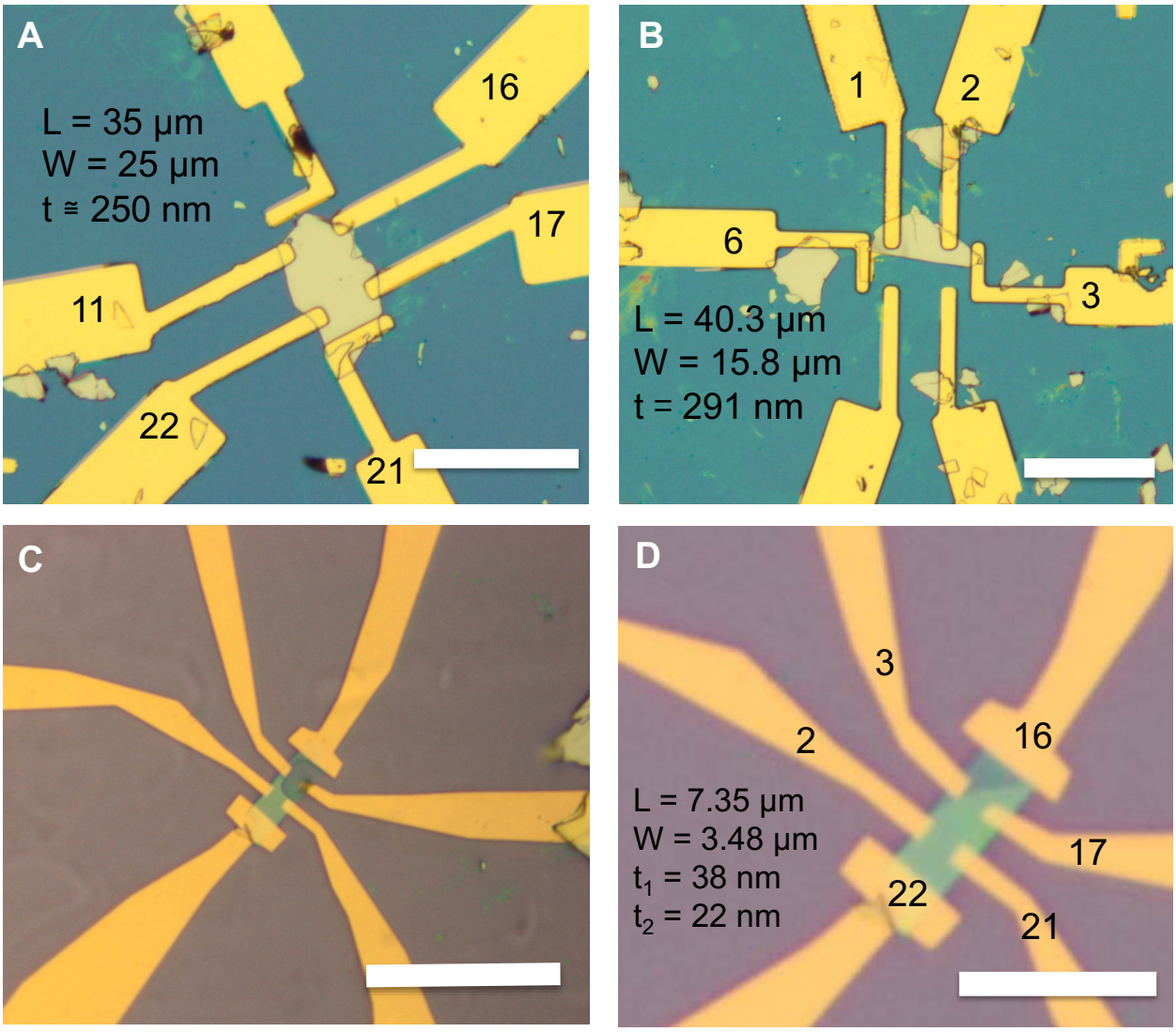

Figure 4.1.1: Samples to be discussed in this chapter a.) & b.) Scale bar = 50 μ m c.) & d.) Scale bar = 10 μ m

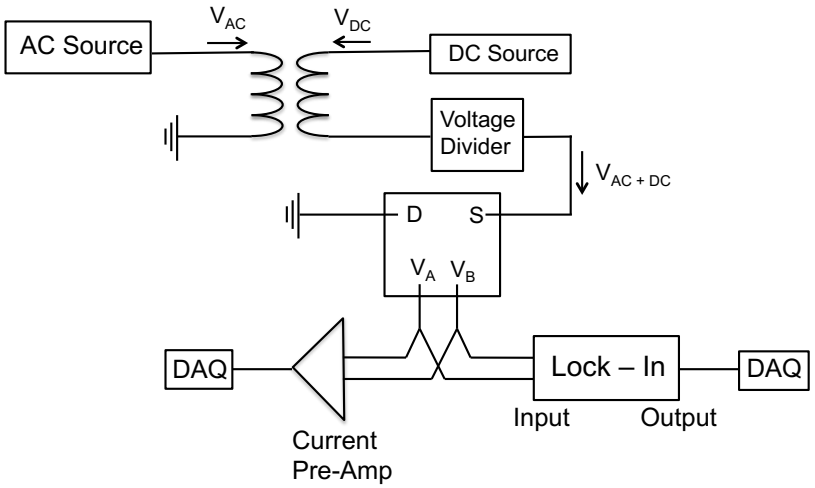

Figure 4.1.2: 4-pt surface adds an AC signal atop a DC bias. Voltage is sent to the sample via the source (S) electrode, and sent to ground by the drain (D). Voltage

4.1.2 Classical Hall effect

The Classical Hall effect manifests as a linear slope of the transverse resistance versus magnetic field. Figure 4.1.3 (a) shows the contact geometry for measuring the transverse Hall (xy) and longitudinal (xx) voltages. A charge carrier travelling along I_{xx} will experience a Lorentz force in magnetic field, perpendicular to its motion. Figure 4.1.3 (b) shows the longitudinal and transverse resistance versus magnetic field. At low fields, we see a linear R_{xy}, the slope of which gives the classical Hall density. At higher magnetic fields the carriers will form closed orbits, behaving as individual harmonic oscillators [35]. When the number of cyclotron orbits is equal to the magnetic flux density on the sheet, there is a minimum in conduction, and we say we have completed a Landau Level (LL). Appearing as plateau's in R_{xy}, we may assign to these a Landau filling fraction ν according to the position of the minimum

in B.

Using the aforementioned AC + DC method, we probe the Bi_2Se_3 crystal's resistance at varying magnetic fields. Acting as a magneto-sensor with a change in resistance proportional to magnetic field, the sample carrier density is extracted via a linear data fit. The measured density of $n_{3D}^{Hall} = 3.01 \times 10^{19}$ cm^{-3} compares well with a highly n-doped 3D topological insulator [22].

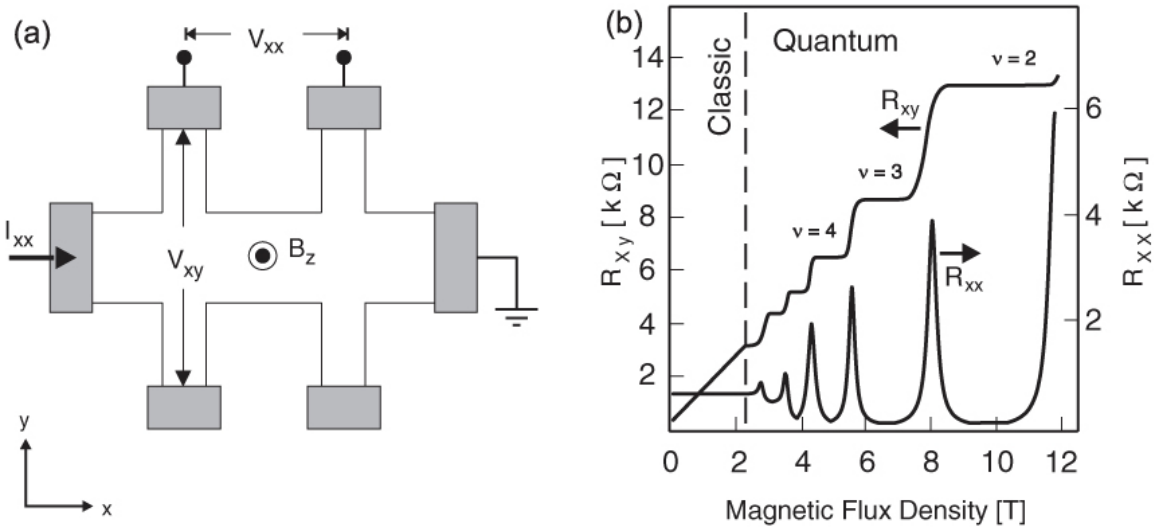

Figure 4.1.3: a.) 6-point Hall Bar geometry b.) Longitudinal and transverse Hall resistance. Figure from Janssen et al. [35]

For samples which do not exhibit simple linear Hall magnetoresistance, we will test for quantum localization and Shubnikov-de Haas oscillations in sections 4.2 and 4.3, respectively.

4.1.3 Extracting the Hall density

A reliable method for extracting the charge carrier density in a thin crystal is by measuring the slope of the Hall resistance vs magnetic field. The data for sample A, shown in Figure 4.1.4, is linear over the entire B range up to 9 Tesla.

Following the method used by H. Xu et. al [17] to extract the carrier density and mobility from a linear R vs B curve, we define the current mode sensitivity as:

$$V_H = S_I I B \tag{10}$$

where the linear proportionality constant S_I is related to the carrier density n_S by:

$$S_I = \frac{1}{I}\frac{\delta V_H}{\delta B} = \frac{1}{q n_S} \tag{11}$$

Noting that $(\delta V_H/I)/\delta B = \delta R_H/\delta B$, we may use the slope of the Hall trace to determine carrier density by writing

$$n_{2D} = \frac{1}{e(\delta R/\delta B)} = \frac{1}{e(Slope)} \tag{12}$$

If we begin with a thicker device (250 nm), one might expect to find a higher relative carrier density due to n-doping from bulk layer contributions. The Hall measurements shown in Figure 4.1.4 are taken at 1.2 K:

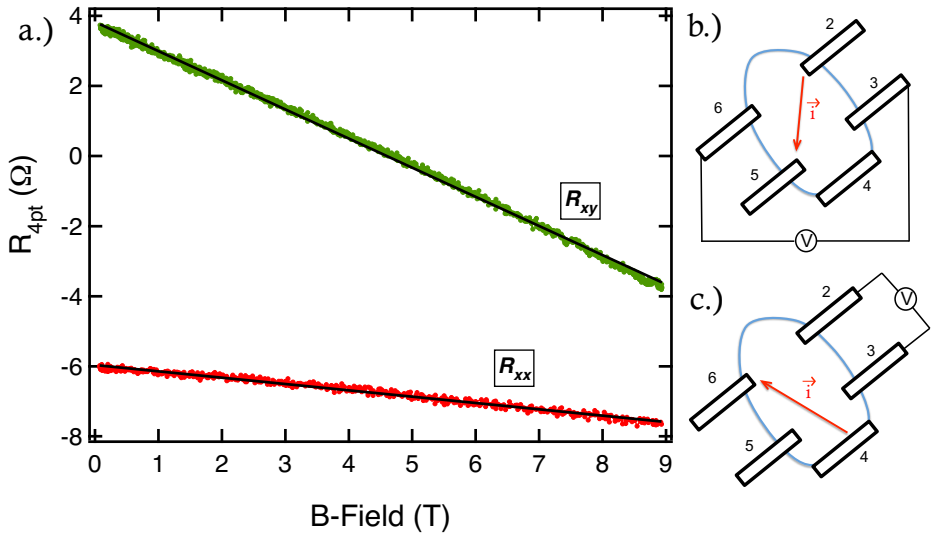

Figure 4.1.4: a.) The 4-probe Hall measurement shows partial mixing of transverse and longitudinal modes due to contact geometry: b.) Transverse Hall signal (ρ_{xy}, Green line) c.) Longitudinal Hall signal (ρ_{xx}, Red line)

the transverse and longitudinal contact geometries depicted in the sidebar. By fitting the slope of R_{xy} we find $n_{Hall} = 7.52 \times 10^{14} cm^{-2}$. Due to the contact geometries we have some mixing between longitudinal and transverse Hall signals, otherwise we should expect R_{xx} to have no slope.

This also allows us to determine the carrier's mobility, μ, using $\sigma = ne\mu$. Using the Hall density (R_{xy}), we may calculate the mobility to be $\mu \cong 1390 cm^2/Vs$. If we were to treat the sample as a 3D conductor, we find $n_{3D}^{Hall} = n_{2D}^{Hall}/t$, where t is the sample thickness, giving $n_{3D}^{Hall} = 3.01 \times 10^{19} cm^{-3}$. Comparing this to $n_{3D} = 2.3 \times 10^{19} cm^{-3}$ found by J. G. Analytis et. al [22], on a sample which is microns thick, we say that this device is behaving as a 3D conductor.

In Figure 4.1.5 we have magnetic field sweeps of samples B and C, showing

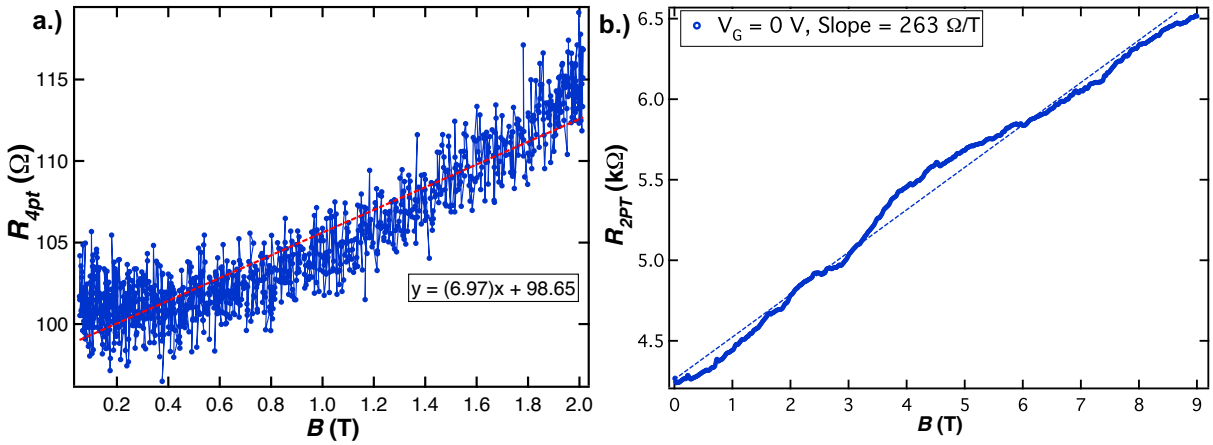

Figure 4.1.5: R vs B: a.) The 4-point measurement in sample B shows a partial mixing of R_{xx} and R_{xy} at low-fields b.) The 2-point measurement in sample C displays oscillations on top of a linear slope.

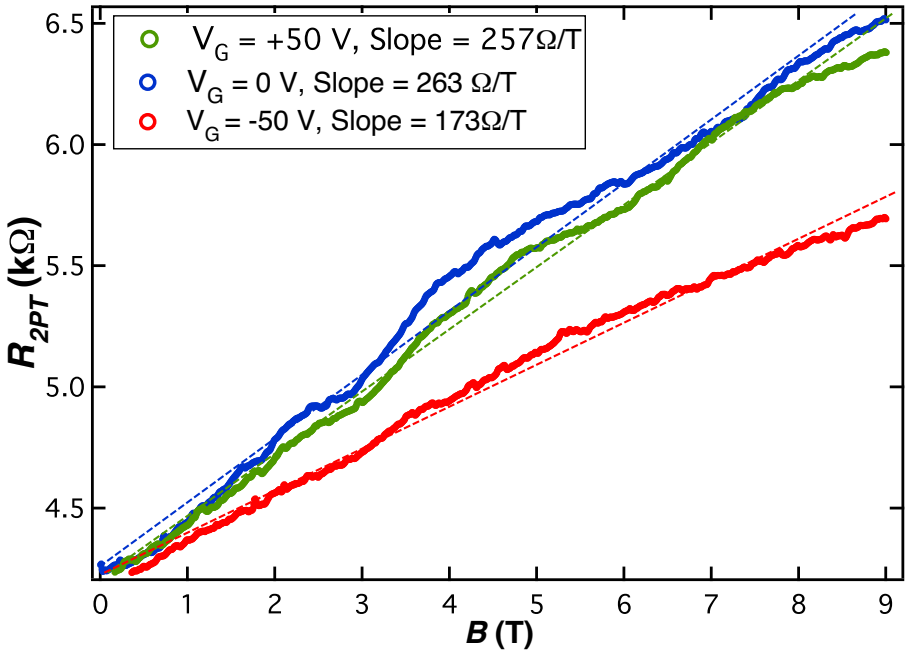

Figure 4.1.6: Resistance vs magnetic field for different gate voltages. The slope of linear fits: (+50V): 257 Ω/T, (0V): 263 Ω/T, (-50V): 173 Ω/T

predominately linear behaviour with some deviation. The measured Hall densities are $n_{Hall} = 8.97 \times 10^{13}$ cm^{-2}, and $n_{Hall} = 2.38 \times 10^{12}$ cm^{-2} in samples B and C, respectively. The appearance of the fluctuations in panel B suggests the sample is displaying both Classical Hall, and quantum behaviour. The magneto resistance of sample C for different gate voltages is shown in Figure 4.1.6. As above, we may find the carrier density for each gate voltage by taking a linear slope. This gives the carrier densities: $n_{+50V} = 2.43 \times 10^{12}$ cm^{-2}, $n_{0V} = 2.38 \times 10^{12}$ cm^{-2}, and $n_{-50V} = 3.61 \times 10^{12}$ cm^{-2}. If we compare to the theoretical change in carrier density caused by the gate electrode: $\Delta n_G = \frac{C_G}{eA}|V_G|$, we find $\Delta n_G = 7.19 \times 10^{10}$ cm$^{-2}|V_G|$, or $\Delta n_G(50V) = 3.59 \times 10^{12}$ cm^{-2}. It is clear that we are not seeing the full effect of the gate, seeing only roughly 1/3 the change in carrier density expected for $50V$. This can be explained by the fact the gate electrode is coupled to the bottom surface, and we are contacting the top surface. It is reasonable to expect some screening from the bulk layers in this highly n-doped material. The fact that the crystal is asymmetrically n-doped also explains why we don't see as much of a change going to $+50$ V as we do for $-50V$. Now we turn to another sample which will aid in our search for surface states. Sample D is a factor of 10x thinner than sample A, with transport flowing over a step edge on the crystal surface. In Figure the magnetic field sweep over $\pm 9T$ we can immediately see a strong deviation from the linear, followed by clear oscillations. This sample also offers the unique possibility to study the effect of thickness within the same device. As this sample does not exhibit any linear region, we save the discussion of this curve for sections 4.2 and 4.3. Now that

we have established a starting point with the carrier densities from the linear Hall slope, we move on to investigating non linear magnetic field effects. First we test the low-field peak for WAL, and then move on to Shubnikov-de Haas oscillations.

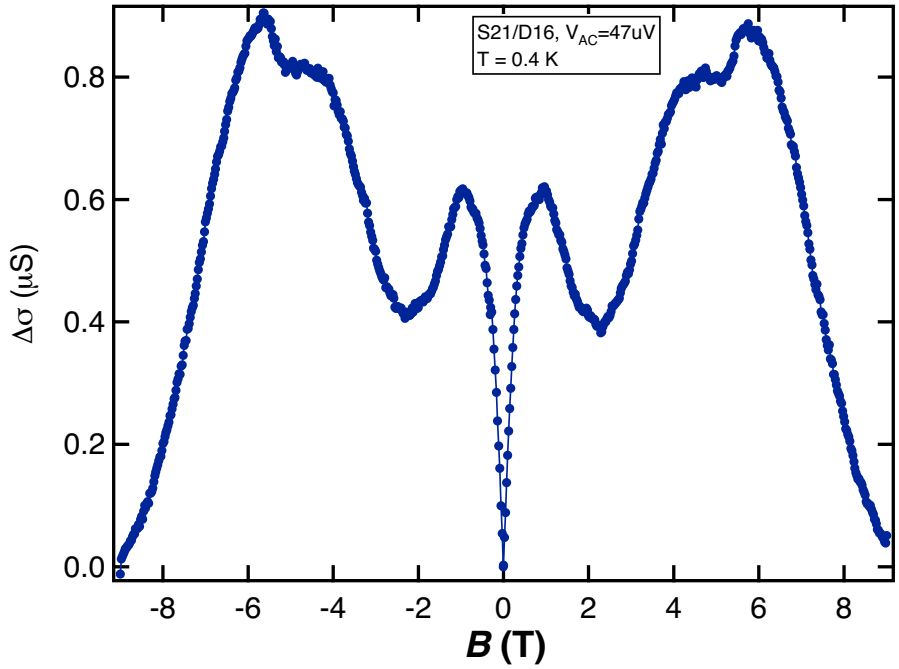

Figure 4.1.7: A clear low B-field peak is observed along with subsequent large oscillations at increasing field strength

4.2 Testing for localization effects: the quantum diffusive regime

This project is motivated by a search for evidence of the topological surface state. The low-field peak of sample D in Figure 4.1.7 is very similar to that seen in 2-dimensional transport on the surface of a topological insulator displaying localization

effects [25, 27]. If we observe localization we could test the data quantitatively to learn if the states are topological or not. To understand the weak anti-localization effect, we first introduce the average distance a charge carrier travels in between collisions. In a thermal scattering regime, the mean free path of electrons is found through the Boltzmann relation:

$$L_{Thermal} = \frac{\pi \hbar v_F}{k_B T} \tag{13}$$

where v_F is the Fermi velocity in the crystal, and T is the temperature. Fabricating small samples ($< 10\mu m$) and measuring at cryogenic temperatures allows for the possible observation of coherent ballistic transport [34]. In a system with strong spin orbit coupling (SOC), it is possible to have wavelike effects at distances longer than the thermal length, as a net phase coherence may be maintained over many scattering events [19]. The phase coherence length may be determined by examining a low−field correction to the conduction, which is a result of charge carriers who pick up a phase shift when travelling along a self intersecting path under time reversal symmetry [16]. This occurs only when the phase coherence length is much larger than the mean free path, $l_{phi} >> l$ (Figure 4.2.1 c).

Shown in Figure 4.2.2, the resulting phase shift can manifest as a constructive or destructive interference, leading to either a positive or negative correction. The so called Weak anti-localization (WAL) and Weak-Localization (WL) effects are the two sides of the same physical phenomenon. A surface state with SOC will always display

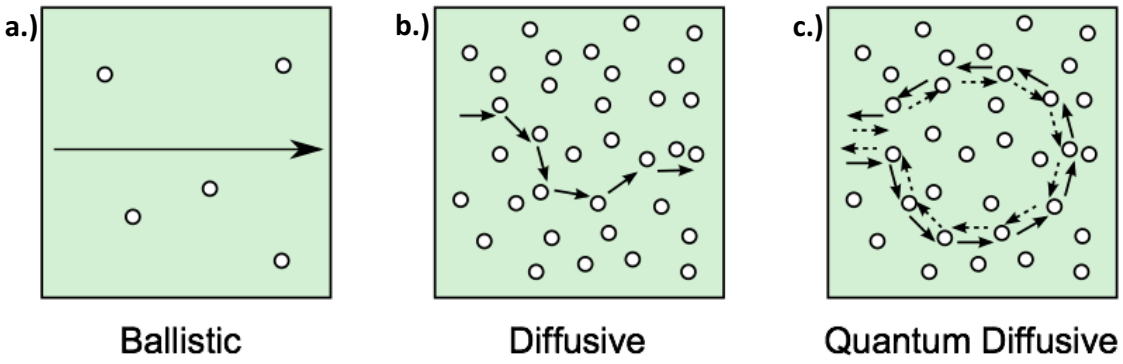

Figure 4.2.1: Three different transport regimes in solids: a.) In a ballistic regime carriers encounter few collisions and thus retain their phase over long distances. b.) In a scattering diffusive regime, collisions are frequent and transport is based on the averaged drift velocity. c.) In the Quantum Diffusive regime where we see localization effects, the phase coherence length ($l_\phi >> l$) is much larger than the mean free path, therefore enabling interference over many collisions (Figure from Lu et. al [19])

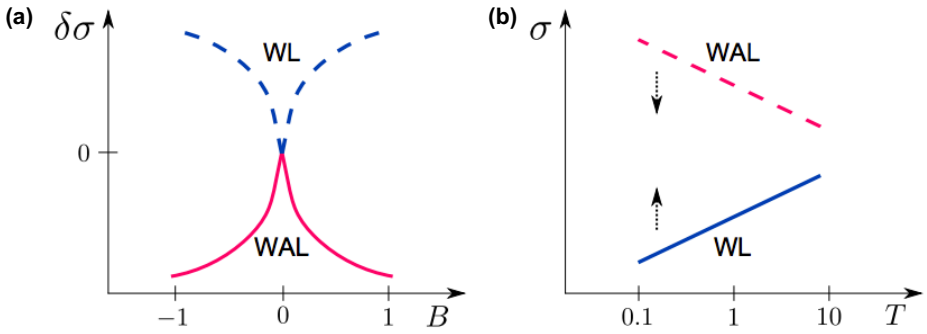

Figure 4.2.2: a.) Weak localization and anti-localization display opposing peaks near zero magnetic field b.) Both WAL and WL display a linear magnetoresistance at higher fields [19]

the WAL effect as a result of the π cumulative phase shift, whereas bulk states can exhibit either WL or WAL[16]. The mathematical function describing the effect is given by the Hikami-Larkin-Nagaoka (HLN) model[25]:

$$\Delta G_{WAL}(B) \equiv G(B) - G(0) \simeq \frac{\alpha e^2}{2\pi^2 \hbar}[\Psi(\frac{1}{2} + \frac{B_\phi}{B}) - ln(\frac{B_\phi}{B})] \tag{14}$$

with leading coefficient $\alpha = -1/2, 1/2$ for the WAL, WL effects respectively[27]. The fit parameter α provides a means of determining whether surface or bulk states are dominating the transport simply by noting whether the $0-$field peak is inverted or not. The HLN formalism makes use of the exotic digamma function, which relates a gamma function to its derivative such as:

$$\Psi(z) = \frac{\Gamma'(z)}{\Gamma(z)} \tag{15}$$

where the gamma function represented by $\Gamma(n) = (n-1)!$. Inside the argument of the digamma function and the natural logarithm, one finds the independent variable, B, and our second fit parameter, B_ϕ:

$$B_\phi = \frac{\hbar}{4el_\phi^2} \tag{16}$$

allowing calculation of the phase coherence length, l_ϕ. In Figure 4.2.3 we see the magneto conductance data ($1/R$ vs B) for sample D. The change in conductance is found by $\Delta\sigma(B) = \sigma(B) - \sigma(0)$. In Figure 4.2.4, a partial fit over 0.6 T gives a phase coherence length of 120 nm and a WAL coefficient of $\alpha = 0.024$. This coefficient

should be 0.5 for WAL, or 1 for two surfaces [27]. By using the composite form of the HLN formula, accounting for possible WL contributions from bulk states, we find similar l_ϕ and α. Given that fitting does not yield the expected coefficient $\alpha = 0.5$ for the WAL state, we fix this parameter and find the HLN model does not fit the data (Figure 4.2.5).

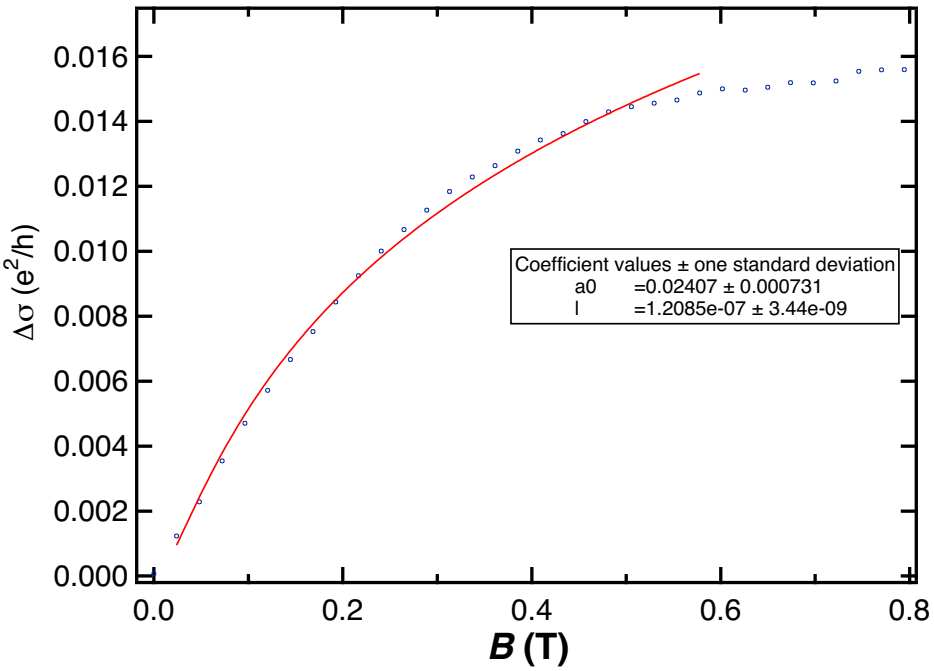

Figure 4.2.3: Fitting the HLN model to the data of sample D, we extract a value of α=0.024

The peak in resistance of sample D is very similar to that seen in 2-dimensional transport on the surface of a topological insulator displaying localization effects. The HLN model describing weak anti-localization in the quantum diffusive regime is fit to the data and shows a significant disagreement, indicating the observed peak is not due to WAL. The extracted magnetic coherence length and interference factor

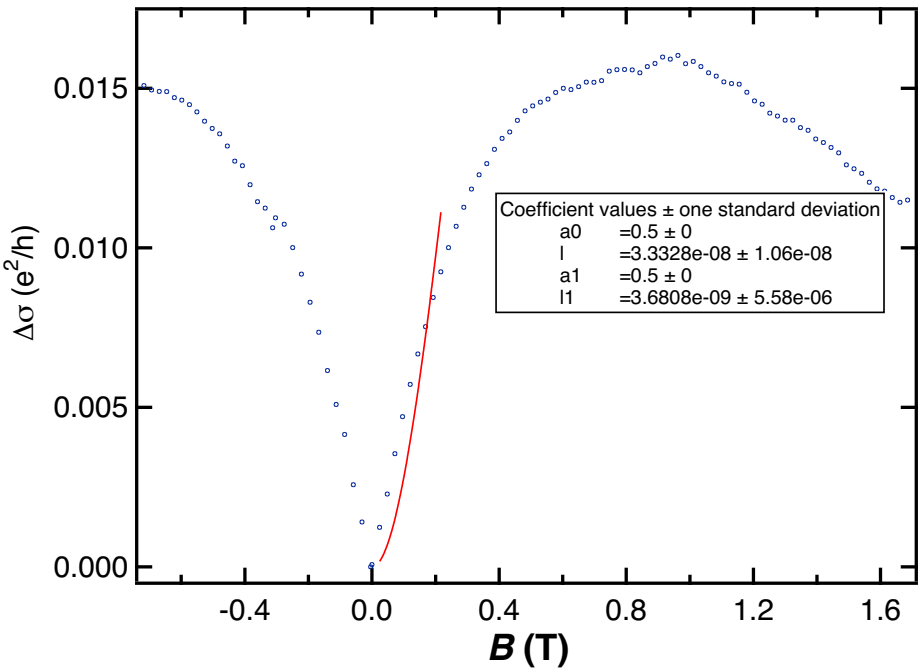

Figure 4.2.4: Fixing $\alpha = 0.5$ we find the HLN model does not fit the data, suggesting the low-field peak is not due to WAL

are disregarded as the model does not apply well to this data range. This does not rule out the presence of a topologically protected surface state, as the quantitative agreement with the model may be due to surface oxidation or the nature of the contact geometry over the step.

As the fitting parameters do not yield any meaningful values, and the range of the observed peak is roughly an order of magnitude off that observed in literature, we say that our data does not coincide with the HLN model. Thus, we have ruled out WAL as the origin of the magnetoresistance at low-B in sample D. Next we consider the Shubnikov-de Haas effect to describe this data in section 4.3.

4.3 Shubnikov-de Haas oscillations on the surface of Bi_2Se_3 thin films transistors

In our search for evidence of surface transport, we have seen clues in the gate dependence of Classical Hall effect, and have ruled out the presence of the WAL effect. In this section we take a look at the oscillations in resistance observed in samples C and D. The carrier density is extracted from the spacing of peaks in magnetic field, and compared to the density obtained from the linear fit of the Hall slope in the same data.

4.3.1 Gateable Shubnikov de Haas density

In a 2-dimensional electron gas under a magnetic field, in-plane carriers experience the Lorentz force in a direction perpendicular to their motion. If the B-field is strong enough, electrons become trapped in localized orbits, each behaving as a harmonic oscillator [35]. When the number of electrons in the sheet is less than the available states, conduction is possible. If however all orbit states are filled, we have completed a Landau Level and the average conductance within the sheet goes to zero, the only channels available being 1D edge states. A Landau fan diagram is constructed by assigning a filling fraction to the observed oscillations in R, and plotting versus the reciprocal of their position in magnetic field [12]. We extract a density $n_{SdH} = 6.45 \times 10^{11}$ cm^{-2} at zero volts gate in sample C, compared to $n_{SdH} = 6.72 \times 10^{11}$ cm^{-2} in sample D with different surface structure. The Shubnikov-de Haas density is mildly gateable, showing a change to $n_{SdH}(50V) = 8.21 \times 10^{11}$ cm^{-2}. We argue that the magnitude of n_{SdH} compared to n_{Hall}, combined with the gating effect suggests we are contacting the top surface of the crystal.

As observed by C. Bao et. al, a periodic oscillation occurs atop a linear magneto-dependence of resistance. We see this in our data shown in Figure 4.3.1. To construct the Fan diagram, one assigns a Landau Level filling fraction ν to each oscillation in 1/B. When the filling fractions are plotted vs $1/B$, the resulting linear dependence yields both the 2D carrier density and the Berry's Phase [10]:

$$\nu = \frac{\hbar}{e} n_S (\frac{1}{B}) + \beta \tag{17}$$

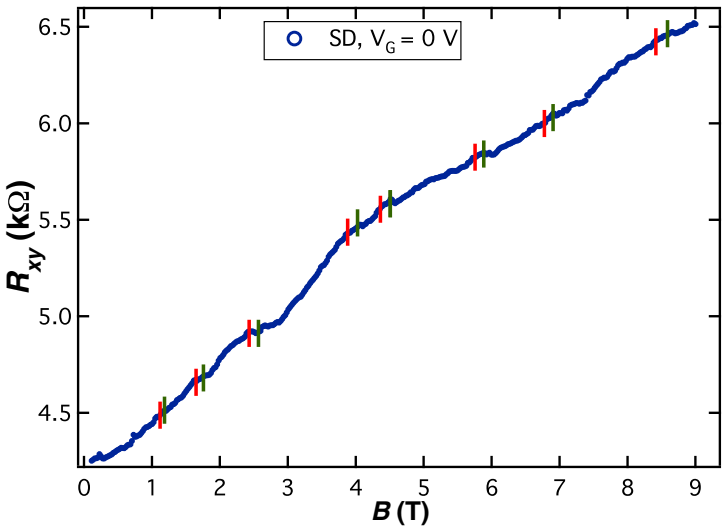

Figure 4.3.1: The position in magnetic field of plateaus in R_{xy} is marked with error shown by red and blue lines

and so

$$n_{SdH}^{2D} = \frac{e}{h}(Slope) \tag{18}$$

The expected filling fraction may be calculated using the quantum of magnetic flux:

$$n_{\phi} = \frac{eB}{h} \tag{19}$$

which gives $n(9T) = 4.35 \times 10^{11}$ cm^{-2}. If now we take a linear fit to the magneto resistance curve (ignoring any oscillations), we find $n_{Hall} = 2.38 \times 10^{12}$ cm^{-2}. This gives a theoretical starting point for the filling fraction at $9T$:

$$\nu = \frac{n_e}{n_\phi} = \frac{2.45 \times 10^{12} cm^{-2}}{4.35 \times 10^{11}} \cong 5.6 \tag{20}$$

The assigned Landau filling fractions are plotted vs 1/B in the fan diagram shown in Figure 4.3.2, the slope of which gives $n_{2D} = 6.45 \times 10^{11} cm^{-2}$. We can immediately see that this density is roughly a factor of 5 times smaller than the one taken from the classical Hall slope. As we have seen carrier density scales with thickness, this suggests the surface nature of carriers involved in these oscillations.

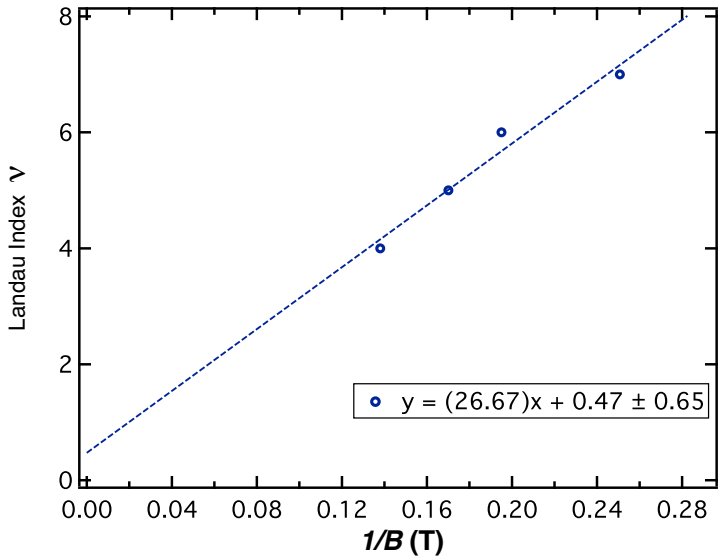

Figure 4.3.2: Landau fan diagram for sample C (t = 38 nm, T = 1.5 K) shows the filling fraction assignment vs 1/magnetic field

The fan diagram for sample C is shown in Figure 4.3.3, for three different gate voltages. The linear fits all have an intercept that is within the error of the origin. A π-Berry Phase would correspond to a y-intercept of 0.5. We can see the fits converge to a point around $\nu = 2$, when we should expect to see this convergence at zero. This

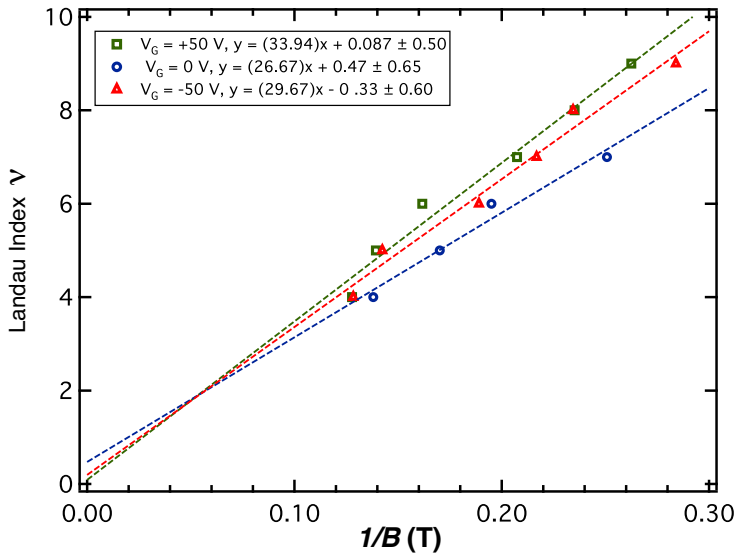

Figure 4.3.3: Landau fan diagram shows the change in carrier density with electric field

represents the level of error in the data. Using equation (16) we calculate the densities at the each gate voltage to be: $n(+50V) = 8.21 \times 10^{11}$ cm^{-2}, $n(0V) = 6.45 \times 10^{11}$ cm^{-2}, $n(-50V) = 7.18 \times 10^{11}$ cm^{-2}. Whereas the change in carrier density induced by the gate electrode, calculated from the sample capacitance, is a factor of 5x larger: $n(\Delta 50V) = 3.59 \times 10^{12}$ cm^{-2}. We take this to say that the bottom gate is only affecting the top surface at roughly 20% efficiency. The decrease in effectiveness is likely due to top surface transport being screened by bottom surface and bulk layers, mentioned in section 4.1.3. Next we return to sample D before the gate shock, we may assign LL filling fractions to apparent plateaus in R_{xx}, discussed in section 4.3.2.

4.3.2 Two different contact geometries: R_{xx} vs R_{xy}

Due to the change in sample geometry, we saw that after the gate cleavage the R_{xx} path was removed, leaving only the R_{xy} component. Figure 4.3.4 shows the magnetoresistance data of sample D, with assigned filling fractions in R_{xx}. Parallel lines indicate minima in R_{xx} often occur at the same magnetic field as the plateaus in R_{xy}. This graph is used to zone in on Shubnikov-de Haas features more precisely. In Figure 4.3.5 we plot the filling fractions for this sample using the information from both the longitudinal and transverse data:

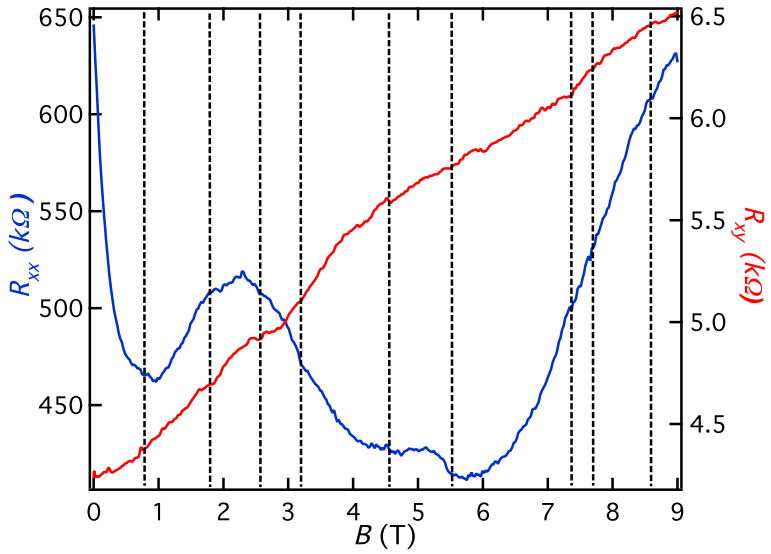

Figure 4.3.4: Landau fan diagram shows the filling fraction assignment vs 1/magnetic field

with extracted carrier density $n_{SdH}(before) = 1.14 \times 10^{12}$ cm^{-2}. The $y-$intercept reveals a Berry's Phase of 0, however the associated error has increased to 0.91, meaning we cannot conclusively comment on the nature of charge carriers being

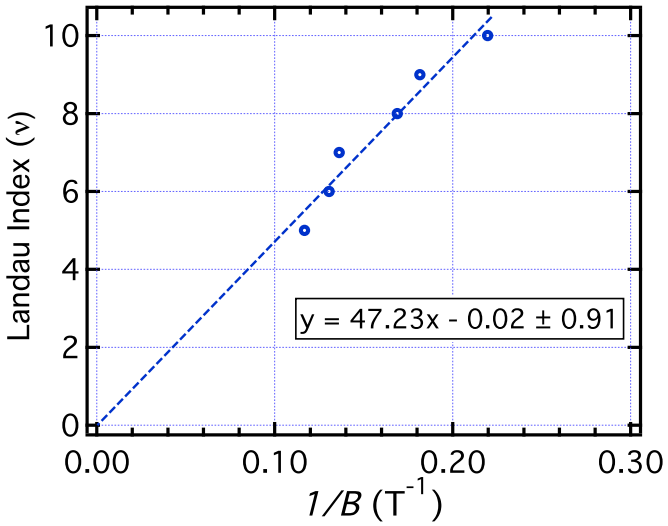

Figure 4.3.5: Replotting the fan diagram using both R_{xx} and R_{xy} to locate oscillations, we find an intercept of 0, however with an error of $\pm$ 0.91 we cannot conclude about the Berry's Phase

topological or not. The fact that plateau's in R_{xy} coincide with minima in R_{xx} is strong evidence for the observation of Landau levels, indicating the onset of the quantum Hall regime. Next we take a look at some possible interference fringes and test for the coherence length in another manner.

4.4 Fabry-Perot

Here we discuss the observation of a different type of interference effect, one that is independent of magnetic field. Figure 4.4.1 shows reproducible current peaks in gate voltage at different magnetic field values. The regular spacing of fringes suggests that in this thin portion of sample D, electrons are behaving as optical waves in a resonator cavity. We would expect to see such behaviour if this 20 nm thin flake has effectively

become a 2D TI with 1D edge states. 'Fabry-Perot' oscillations are observed in 1 or 2-dimensional ballistic devices. Ballistic conductors, as opposed to diffusive, allow scatter-free states to exist on a length scale comparable to that of the device. Now that we have ruled out the WAL effect, which occurs in the quantum diffusive regime [19], it is instructive to test for ballistic phenomena.

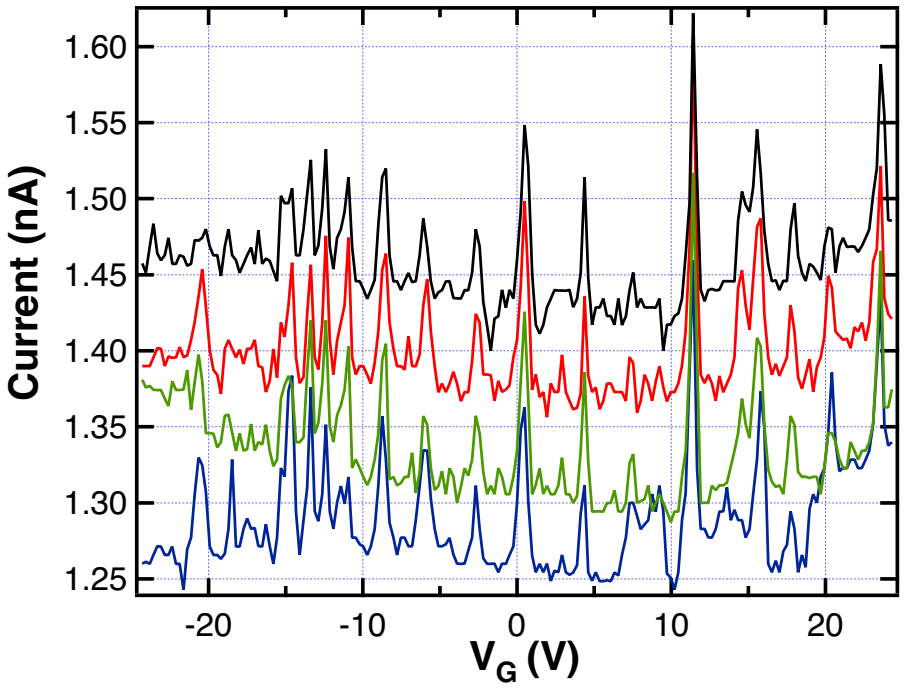

Figure 4.4.1: Current peaks in V_{Gate}: Robust spikes in current in gatesweeps at constant magnetic field (B = 0, 5, 6 7 Tesla). The change in current over 50 V change in gate voltage is roughly 5%

Evidence for ballistic conduction in graphene is reported the Ph. D. thesis of Vahid Tayari, in which the the so called Fabry-Perot coherence length is defined [34]:

$$L_{FP} = \frac{\pi \hbar v_F}{\Delta E} \tag{21}$$

which can be no longer than the thermal scattering length, inversely proportional to the Boltzmann constant:

$$L_{Thermal} = \frac{\pi \hbar v_F}{k_B T} \tag{22}$$

in order to exhibit coherence ballistic transport. At a crystal lattice temperature of 1.3 K, the length is given:

$$L_{Thermal} = \frac{\pi(6.58 \times 10^{-16} eVs)(4.5 \times 10^5 m/s)}{(1.38 \times 10^{-23} J/K)(1.3K)} = 8.42 \mu m \tag{23}$$

The presented device has a physical length $L = 1.8 \mu m$, well under the thermal scattering distance. The theoretical Fabry-Perot length can be calculated for Bi_2Se_3 based on the Hamiltonian given by the Rashba Model[18]:

$$H_R = \frac{\hbar^2 k^2}{2m*} + \lambda(\sigma_x k_y - \sigma_y k_x) \tag{24}$$

for systems with strong spin orbit coupling (SOC), which Bi_2Se_3 is known to have. We may look at the terms independently as a parabolic contribution from the bulk states:

$$\Delta E_{3D} = \frac{\hbar^2 k^2}{2m*} \tag{25}$$

and a linear energy dispersion for coherent surface states:

$$\Delta E_{2D} = \hbar k v_F \tag{26}$$

(note: the density of states is derived in Appendix .1) and so we have the change in the 2D surface Fermi Energy as it relates to the charge carrier density as

$$\Delta E_F \cong \hbar v_F \sqrt{4\pi} \frac{\Delta n}{2\sqrt{n_1}} = \frac{\pi \hbar v_f}{L_{FP}} \tag{27}$$

and so I can either set L_{FP} to the actual length of the device and extract the resulting carrier density, or vice versa, using the measured Hall density and extracting the Fabry-Perot cavity length. The change in carrier density may be calculated as $\Delta n = C\Delta V_G/e$, which, for the observed contacts the separation of peaks is on average $\Delta V_G = 2.5 \pm 0.01V$, resulting in $\Delta n_G(2.5V) = 1.8 \times 10^{11} cm^{-2} = 1.8 \times 10^{15} m^{-2}$. Using this number, and setting the Fabry-Perot length to the distance between the two contacts, $L_{FP} = 1.8\mu m$, we find a total carrier density of

$$n_1 = (\frac{\Delta n L_{FP}}{\sqrt{\pi}})^2 = (\frac{(1.8 \times 10^{-6} m) * (1.8 \times 10^{15} m^{-2})}{\sqrt{\pi}})^2 \tag{28}$$

$$n_1 = 3.41 \times 10^{18} m^{-2} = 3.41 \times 10^{14} cm^{-2} \tag{29}$$

This density is roughly 100 times higher than the Hall density measured in the thicker portion of the sample. This carrier density is not non sensical, but it is high, when compared to even the density found by *H. Wang et al.* of $n_{Hall} = 1.89 \times 10^{13} cm^{-2}$

in 5 nm-thick MBE grown Bi_2Se_3 [16]. One possibility is that this 2D calculation does not work for 1D edge states that may have formed around the 2D TI. Figure 4.4.2 shows 2D $I - B - V_G$ data in 3 sections of the sample. We see almost no fringes in the thickest section (panel a), a few fringes in the data across the step involving both thick and thin portions (panel b), and numerous fringes in the thinnest section (panel c). The absence of SdH oscillations in the thin section is consistent with the notion that the thin portion of the sample is no longer in the 3D regime with 2D surface states. Indeed, further data analysis is required to understand this complex geometry. In the conclusion we present a method for improving the device performance using suspension of TI thin films.

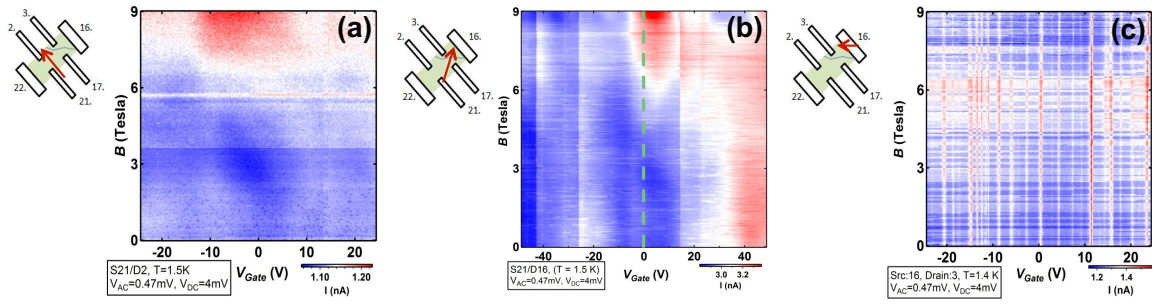

Figure 4.4.2: 2D Maps: a.) Interference fringes not apparent in the thick portion b.) some mix of behaviour in transport over the step c.) fringes are seen mainly in the thin portion of the sample (c)

Chapter 5

Conclusion

This project was aimed at developing robust Bi_2Se_3 devices to study the topological transport properties in this material. The inverted band structure in thin Bi_2Se_3 results in protected surface states that could have applications in spintronics and room temperature magneto-electronic devices [15]. The main difficulty to overcome was the degradation of Bi_2Se_3 surfaces in air. We have developed a reliable fabrication procedure in Chapter 2 for contacting thin films of Bi_2Se_3 (down to 22 nm-thick), even when their surface has roughly 1 nm of oxide growth (corresponding to about one day of air exposure) [7]. Using a plasma etching after lithography, prior to metal contact evaporation, we can inject current directly into a crystal despite a modest layer of surface oxide. In Chapter 3 we demonstrated the methods to characterize the performance of devices via their channel and contact resistances. Based on minimizing oxygen exposure and RIE contact etching, our technique allowed us to demonstrate high quality transistor devices and measure their magnetoresistance properties at

temperatures down to 0.3 K. This capability to make high mobility devices (up to 1393 cm^2/Vs) without making use of a high-vacuum preparation environment is an important step forward for realistic fabrication procedures for Bi_2Se_3 transistors. In Chapter 4 we observed Shubnikov-de Haas oscillations in transport experiments in our devices, indicating the formation of Landau levels. Future magneto-transport will be useful to probe the physics of topological surfaces which could lead to building fault-tolerant quantum computing.

The layout of this chapter is as follows: in section 5.1 we take a look at the most important results from this paper. In section 5.2 we present the outlook of this project and prototype devices for future experiments, including sample suspension and the use of a top gate.

5.1 Main results

In Chapter 2 we detailed the sample fabrication methods and experimental setup to measure electron transport at low temperatures and high magnetic fields in our thin film topological insulator devices. We explained how Bi_2Se_3 oxidizes with exposure to air, degrading the crystal surface structure. Extended air exposure was found to degrade even the bulk of 100s of nm-thick crystals and made transport studies impossible. Long term exposure must be avoided at all costs. If fabrication could be carried out in-situ, such as inside a glovebox, much of the degradation from oxidation could be prevented. Mechanically exfoliated thin films are patterned with

gold electrodes and packaged for transport studies. A back gate is capacitively coupled to the substrate, allowing control of the ambient electric field. The use of a top gate in addition to the back gate would provide independent surface control helping to elucidate the penetration depth of capacitively coupled charges. Measures such as polymer encapsulation and p-doping would help protect the surface and accentuate the surface state. *D. Kim* and *M. S. Fuhrer* et. al [4] employed both a top gate electrode and a p-doping deposited polymer, observing bipolar transport, with the Dirac point at 0 V_G.

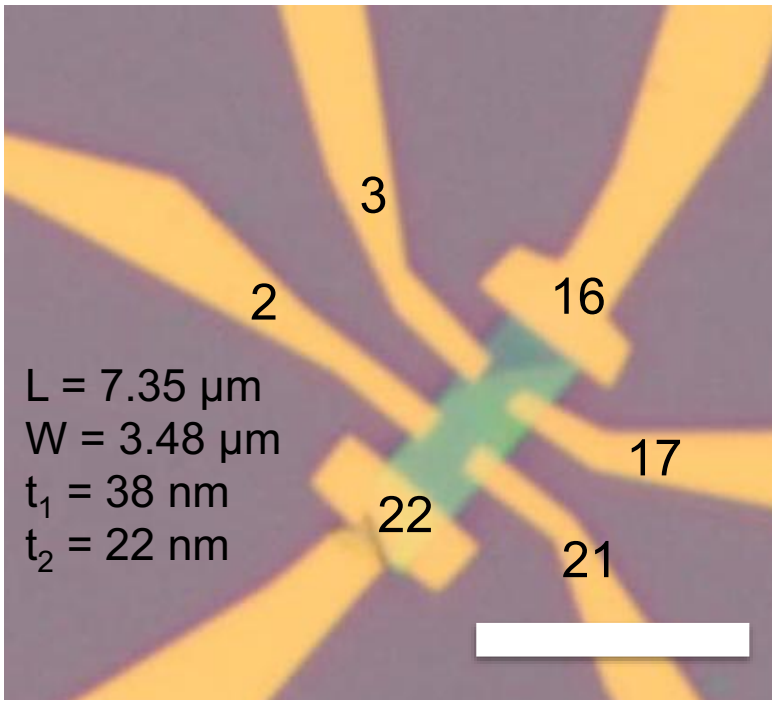

Figure 5.1.1: Mechanically exfoliated Bi_2Se_3 of 22 nm with lithographically defined Gold electrodes. Scale bar is 10μm.

In Chapter 3 we tested the quality of our devices using electrical characterization. Measuring the resistance and gate action of many samples we compiled an archive

of samples. The lowest resistances were found in samples with limited exposure to oxygen. Samples with 1-3 days of exposure to air (relating to roughly 1-3 nm surface oxide) could be cleaned using RIE etching before contact deposition, obtaining $R_{Contact} \cong 1$ kΩ. We showed how the sheet resistivity and contact resistance can be extracted using 4-point measurements, and how it can be approximated for 2-point samples. We showed that the logarithm of contact resistance inversely scaled with the crystal thickness multiplied by the contact area, in two samples whose thickness was an order of magnitude apart (Figure 3.2.6). A small gate dependence was observed, with an $\Delta R/R$ ratio of only 0.8% over 20V in sample B, with thickness 291 nm.

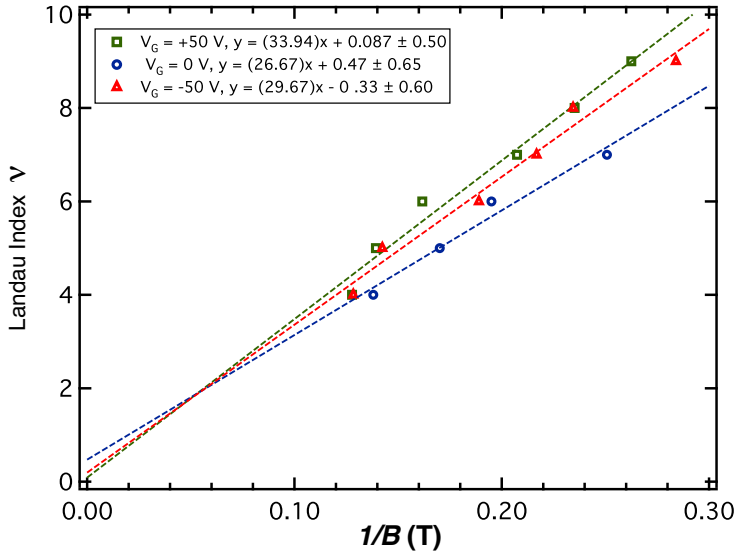

Figure 5.1.2: Landau fan diagram showing the filling fraction assignment vs 1/B, for sample C with thickness 38 nm, at T = 1.5 K

In Chapter 4 we explore our best devices with magneto transport studies, searching for evidence of 2D surface transport. Devices were selected based on their resistance, thickness, and contact geometry. We used an AC lock-in measurement circuit and a

custom data acquisition software to measure the resistance as the magnetic field was swept over ± 9 T at temperatures down to $0.3K$. We extracted the Hall density by measuring the slope of R_{xy} vs B. The extracted 3D bulk density n_{Hall}^{3D} matches well with a highly n-doped Bi_2Se_3 topological insulator. Using a gate voltage of 100 V we see a very significant 33% change in carrier density. We ruled out quantum localization effects at low field by fitting R vs B data to the Hikami-Larkin-Nagaoka model. We also observed Shubnikov-de Haas oscillations in our thinnest sample ($t_{eff} \cong 20$ nm), which were symmetric for ± B. The surface density extracted from the Landau fan diagram in Figure 5.1.2, $n_{SdH}^{2D} = 6.45 \times 10^{11}$ cm^{-2}, is gate tuneable by 22% using a voltage of 100 V. The fact that the gate response is a factor of 10x smaller than that observed in classical Hall density is consist with the Shubnikov-de Haas oscillations originating from the top surface. This is consistent with the roughly 5x drop in carrier density between classical Hall and quantum Hall measurements, as the carrier density was found to scale with thickness. We attribute the reduction of the gate response to the top surface being electrostatically screened by the bulk and/or bottom layer. We saw some evidence of Fabry-Perot interferences, although more data are required for a detailed analysis. It should be noted that although Bi_2Se_3 was chosen for its large surface bandgap, depending on the application there could be a more suitable choice of material from the family of topological insulator crystals.

5.2 Outlook: suspended Bi_2Se_3 devices

One of the largest hurdles in separating surface transport from bulk effects, besides surface oxidation, is the high level of n-doping present in Bi_2Se_3 thin films due to bulk impurities, especially in mechanically exfoliated crystals [4]. Additional charge transfer may occur when separating quintuple layers, and from the contact to the SiO_2 substrate. The SiO_2 substrate used for flake deposition is porous, and likely contains trace amounts of water and therefore represents a significant source of device contamination. Suspending the Bi_2Se_3 crystal above the substrate would restore inversion symmetry by removing contact with the substrate. We would also like to employ a method of device suspension and annealing called Joule heating to clean the surface of the crystals as well as to entirely remove the SIO_2 substrate, used by Serap Yigen in "Electronic Thermal Conductivity Measurements in Intrinsic Graphene" (2013) [32]. Joule heating, or self heating refers to flowing a large current through the suspended sample in order to raise its temperature and bake off adsorbed impurities. To facilitate annealing, we need suspended samples for two reasons: the SiO_2 substrate acts as a large heat sink preventing the flake from heating up, and SiO_2 induces disorder in the bottom surface of the TI film. With a suspended sample we hope to better understand the behaviour of un-doped pristine Bi_2Se_3 thin films and preserving the crystal inversion symmetry in thin flakes, by having the same environment for the top and bottom surfaces.

The magnetoresistance of suspended samples E and F is shown in Figure

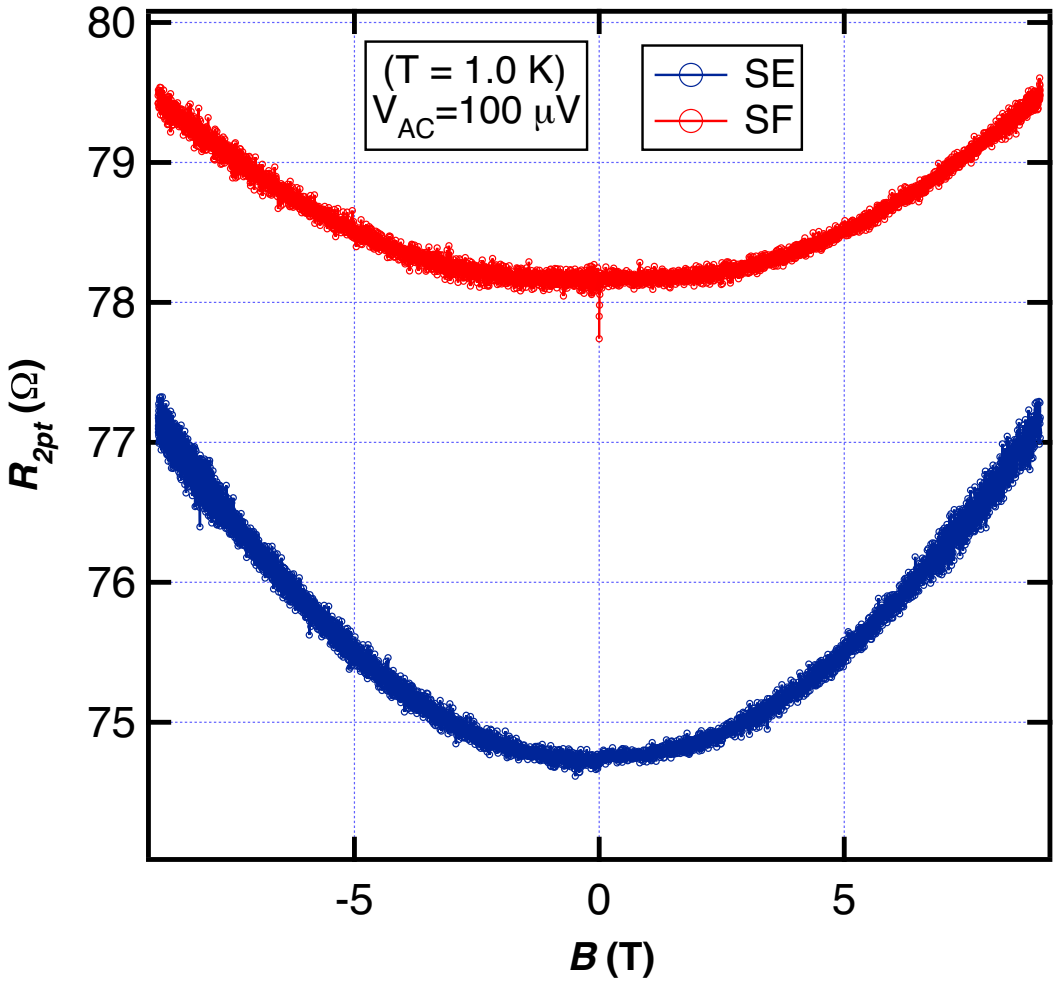

Figure 5.2.1: Magnetic-field dependence of suspended topological insulator transistors E and F at $T = 1$ K

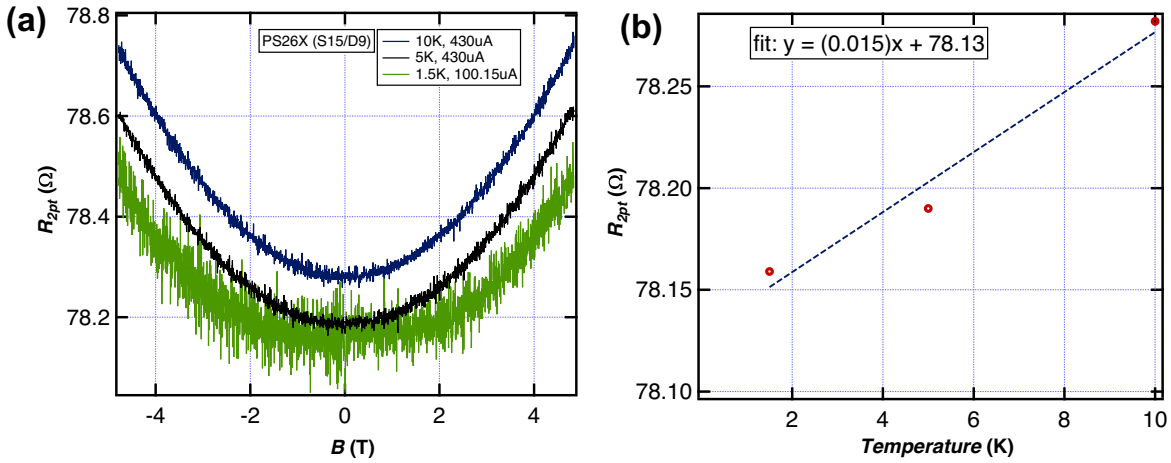

Figure 5.2.2: (a) Magnetic-field dependence of sample E at $T = 1.5, 5, 10$ K, (b) The 2-point resistance at $B = 0$ Tesla

5.2.1. The parabolic line shape is quite different from either the linear or oscillatory behaviour previously observed in this works. In Figure 5.2.2 we see the magnetoresistance of sample E at $T = 1.5, 5$ and 10 K. The inset shows that the 0-field resistance is linearly proportional to temperature in this range. The magneto transport behaviour of suspended samples is not yet well understood, though definitely merits further investigation.

Figures 5.2.3 and 5.2.4 depict 2 suspended samples and their annealing data. The samples were suspended by first etching a series of trenches into the substrate prior to flake deposition. This is done with a separate round of photolithography and surface RIE etching, followed by mechanical exfoliation of the crystals on the trench covered substrate, and finally contact placement. The standard method of suspension via HF acid etching cannot be used for this material as Bi_2Se_3 crystals react with HF and would not survive the process. Care is taken to ensure the RIE etches only

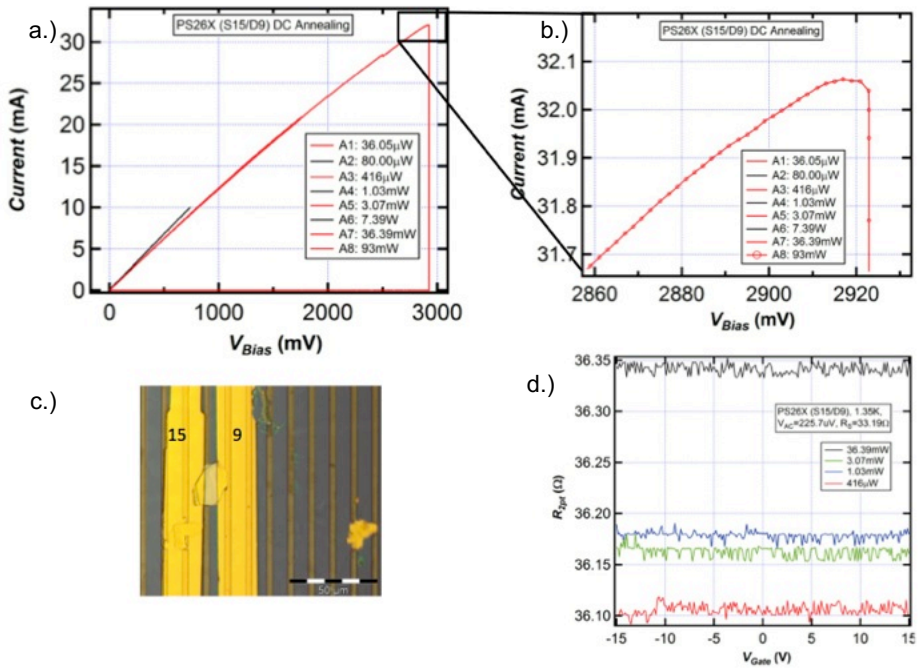

Figure 5.2.3: Joule Heating in suspended sample E: a.) Repeatedly ramping up the current b.) Current saturation leading to device failure c.) Optical image of suspended sample d.) Gatesweeps show resistance is converging with annealing

100-150 nm of the 300 nm SiO_2 film, otherwise the gold contacts will leak current to the gate electrode (Si-substrate). As can be seen in Figures 5.2.3 and 5.2.4 these prototype devices are not suspended over their full length, forming a series connection between two segments of the crystal; one that is suspended and one on the substrate. Nonetheless, we expect to be able to anneal the suspended portion enough to detect the changes with a 2-point measurement.

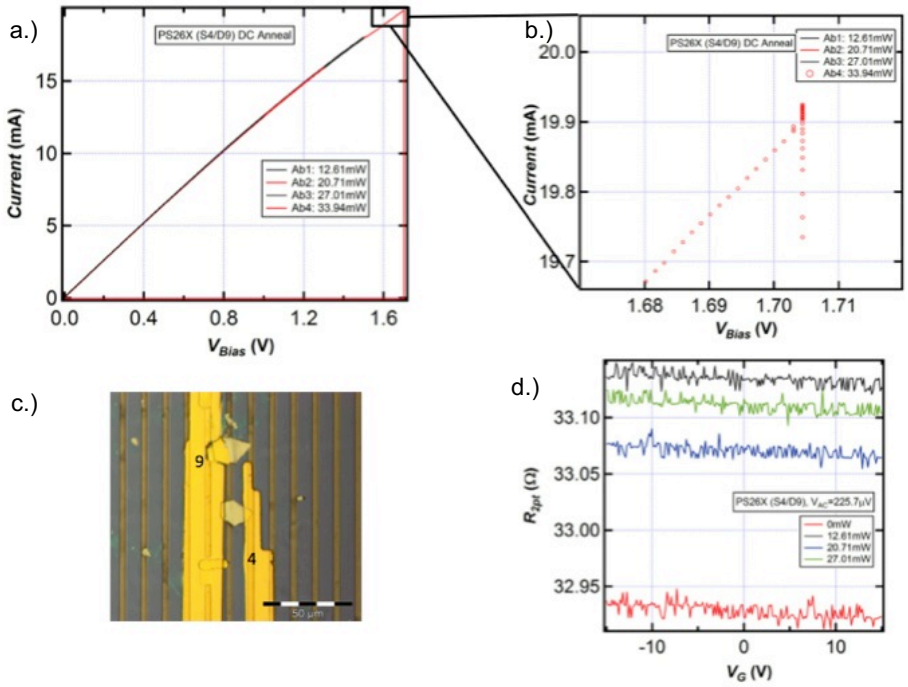

Figure 5.2.4: Joule Heating in suspended sample F: a.) Repeatedly ramping up the current b.) Current saturation leading to device failure c.) Optical image of suspended sample d.) Gatesweeps show resistance is converging with annealing

The annealing method is to slowly increase the flow of current through the sample to a point where Joule heating occurs (Figures 5.2.3 and 5.2.4 a). The heating should result in a change in resistance appearing as a change of slope in the $I-V_b$ plot (panel

a). After heating the sample for 5 minutes, we slowly ramped back down the current to zero V_{Bias}, and the new sample state was checked with a gate sweep (panel d). The $I - V_G$ sweeps show no change in line shape, only a vertical shift in resistance. Figure 5.2.3 (b) shows the breakdown point in current where the device was destroyed and its current dropped suddenly to zero. The change in slope of the annealing curves (before breakdown of sample) are subtle. By analyzing the gate sweeps after each successive annealing (Figures 5.2.3 and 5.2.4 d) we see that the resistance seems to be converging towards a final value, changing by a smaller amount each time the sample is annealed.

Both samples showed a similar convergence towards a final resistance, suggesting that Joule Heating is a viable technique for removed adsorbed impurities in the crystal surface. Caution must be used when approaching the point of current saturation, as device failure will result from overheating. Self heating could be used prior to encapsulation to preserve the pristine surface, or be used to repeatedly anneal and expose the sample in adsorption studies.

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Appendices

.1 Deriving the density of states

To derive the density of states in 3 dimensions, we start with a spherical shell in 3D $k-$space:

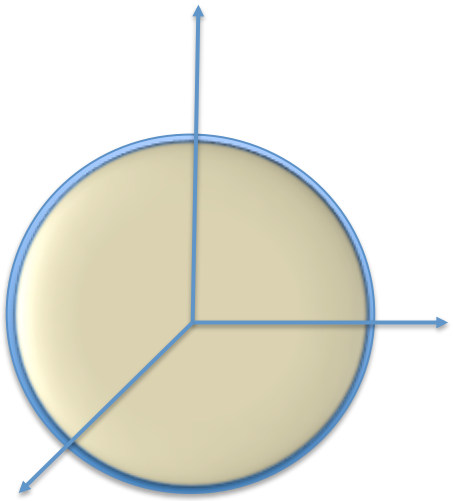

Figure .1.1: A megasweep shows resonances in conductance that appear periodically in magnetic field as in gate voltage

The space taken up by each state in $k-$space is $\pi^3/L_xL_yL_z$, defined by the dimensions of the lattice in 3D. The density can be found by taking the reciprocal: $D = V/\pi^3$. Now we find an integral element by looking at a 3D sphere (Figure .1.1). The volume of a spherical shell in $k-$space is given as $4\pi k^2 dk$, and the number of states within the shell of radius k and thickness dk is given as

$$g(k)dk = 4\pi k^2[\frac{V}{\pi^3}]dk \tag{30}$$

Using equation (25): $\Delta E_{3D} = \frac{\hbar^2 k^2}{2m*}$, the momentum may be expressed in terms of

energy, written ΔE to mean the difference in energy to the bottom of the conduction band:

$$k = \frac{\sqrt{2m^*\Delta E}}{\hbar} \tag{31}$$

With differential:

$$dk = \frac{\hbar}{\sqrt{2m^*\Delta E}} \frac{m^*}{\hbar^2} dE \tag{32}$$

Now the density of states may be written in terms of energy:

$$g(E)dE = \frac{m^*}{\hbar^3\pi^2}\sqrt{2m^*\Delta E}(dE) \tag{33}$$

Similarly, in 2 dimensions, we take a ring of radius k and width dk, with and area $2\pi kdk$. The space taken by each state is $4\pi^2/L_xL_y$, with density A/π^2. The number of states at a given k value within range dk:

$$g(k)dk = [\frac{A}{4\pi^2}]2\pi kdk \tag{34}$$

dividing by A,

$$g(k)dk = \frac{k * dk}{2\pi} \tag{35}$$

and converting to energy using equation (37):

$$k = \frac{E}{\hbar v_F} \tag{36}$$

$$dk = \frac{dE}{\hbar v_F} \tag{37}$$

Giving the 2 dimensional density of surface states in Bi_2Se_3:

$$g(E)dE = \frac{E}{2\pi(\hbar v_F)^2}dE \tag{38}$$

Now we must integrate this differential from 0 up to the Fermi Energy, in order to relate to the total number of charge carriers:

$$n = \int g(E)dE = \frac{1}{2\pi(\hbar v_F)^2}\int_0^{E_F} EdE \tag{39}$$

$$n = \frac{1}{2\pi(\hbar v_F)^2}\frac{E_F^2}{2} \tag{40}$$

$$E_F = \sqrt{4\pi n(\hbar v_F)^2} = \hbar v_F\sqrt{4\pi n} \tag{41}$$

$$\Delta E_F = E_F(n_1 + \Delta n) - E_F(n_1) \tag{42}$$

$$\Delta E_F = \hbar v_F(\sqrt{4\pi(n_1 + \Delta n)} - \sqrt{4\pi(n_1)}) \tag{43}$$

Here we expand the term $\sqrt{4\pi(n_1 + \Delta n)}$ in a Taylor series upon the assumption that the effective change in carrier density influenced with the gate, Δn is much

smaller than the total number of carriers, n_1 ($n_1 >> \Delta n$), by writing:

$$\sqrt{n_1}[1 + \frac{\Delta n}{n_1} - \sqrt{1}] \tag{44}$$

and call the term $\Delta n/n_1 = \epsilon << 1$, then you can say $\sqrt{1+\epsilon} = 1 + \epsilon/2 - 1$ and so

$$\sqrt{n_1}\frac{\Delta n}{2n_1} = \frac{\Delta n}{2\sqrt{n_1}} \tag{45}$$

and so finally we have the change in the 2D surface Fermi Energy as it relates to the charge carrier density as

$$\Delta E_F \cong \hbar v_F \sqrt{4\pi}\frac{\Delta n}{2\sqrt{n_1}} = \frac{\pi \hbar v_f}{L_{FP}} \tag{46}$$