Fabrication, Characterization, and Simulation of Gallium-Nitride Heterojunction Field-Effect Transistors

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Abstract

This thesis presents the fabrication, characterization, and off-state gate leakage simulation of $Al_xGa_{1-x}N$/GaN Heterojunction Field-Effect Transistors (HFETs). GaN HFETs are promising devices for high power, high frequency applications such as microwave amplifiers. This is due to the numerous benefits of the GaN material system including high electron mobility, breakdown field, saturation velocity, and thermal conductivity. This thesis is broken down into two major components. The first and most significant covers the fabrication and characterization of $Al_xGa_{1-x}N$/GaN HFETs. Devices were fabricated at McGill University's Nanotools Microfabrication laboratory using a custom designed process flow. This process flow builds on previous work and presents Ohmic contact results of Ti/Al/Ti/Au and Ti/Al/Ti/Al/Ti/Au metalizations. A complete description of the process flow is provided including technology characterization results, such as mesa height profiling, where applicable. Electrical characterization of fabricated devices is performed. Results show an average contact resistance across temperature of 3.39 Ω mm for the Ti/Al/Ti/Au metalization and 3.22 Ω mm for the Ti/Al/Ti/Al/Ti/Au metalization. Full contact resistance results are provided over a wide range of temperature. The Ti-Al multi-layer metalization also outperforms the Ti/Al/Ti/Au metalization in terms of drain current density (0.12 A/mm vs. 0.09 A/mm) and transconductance (60 mS/mm vs. 40 mS/mm). Off-state gate leakage and current-voltage profiling are also carried out.

The second part of this thesis concerns gate leakage current in $Al_xGa_{1-x}N$/GaN HFETs. A new off-state gate leakage model is presented to determine the variation in leakage mechanisms with the change in barrier layer aluminum mole fraction. A new metric of turning point is introduced to show where Fowler-Nordheim tunneling becomes the dominant leakage mechanism. Results show that as Al mole fraction is increased, the turning point becomes more negative and total gate leakage increases. Finally, improvements to the fabrication process and simulations are presented.

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Chapter 1

Introduction

AlGaN/GaN Heterojunction Field-Effect Transistors (HFETs) are the leading contender for next generation high power and high frequency applications. First demonstrated in 1993 [1], AlGaN/GaN HFETs have continually improved and currently outperform most other semiconductor technologies in terms of the combination of frequency performance and power density. AlGaN/GaN HFETs have produced maximum current gain cut-off frequency, f_T, of 163 GHz and maximum power gain cut-off frequency, f_{max}, of 230 GHz at current densities of 2 A/mm [2]. This makes AlGaN/GaN HFETs ideal for power amplification and power conversion. End-use applications include military radar and high power inverters, among others.

1.1 III-Nitride Material System: AlGaN/GaN HFETs

AlGaN/GaN HFETs achieve their superior performance due to the numerous superb qualities of the III-Nitride material system, of which AlGaN/GaN is only a subset of. The AlGaN/GaN material system, owing to its many unique and beneficial properties, lends itself to use in semiconductor devices and HFETs in particular. The material system exhibits excellent breakdown field, electron mobility, electron saturation velocity, and thermal conductivity. AlGaN/GaN HFETs are more precisely refereed to as $Al_xGa_{1-x}N$/GaN HFETs where x represents the Al mole fraction. This is significant in understanding the benefits of the AlGaN/GaN system. In addition to the material

parameters mentioned above, the adjustment of Al mole fraction provides the device engineer with another knob with which to improve device performance for a given application. Adjusting the Al mole fraction of AlGaN opens up many interesting possibilities. Among which, it can allow for reduced strain by a more acceptable level of lattice matching AlGaN to a growth substrate. This possibility affects device qualities such as contact resistance, gate leakage, and virtually all other device characteristics.

Table 1.1 compares some of the material properties of GaN to its main competitors. In this table, the so called combined figure of merit (CFOM) factors all material parameters into a single figure (which is normalized to silicon). It is noted that although GaAs has a much higher electron mobility, the wide bandgap, large breakdown field, and good thermal conductivity of GaN suggests that overall, GaN outperforms GaAs. Although applicable to certain device applications, the below definition of CFOM is not an impartial representation of all material parameters, simply those deemed most relevant to high power, high frequency performance.

Table 1.1: Selected GaN material properties compared to competitor semiconductors [3].

Property	**Si**	**GaAs**	**4H-SiC**	**GaN**
Bandgap, E_g (eV)	1.12	1.42	3.25	3.40
Breakdown field, E_B (MV/cm)	0.25	0.4	3.0	4.0
Electron mobility, μ (cm^2/Vs)	1350	6000	800	1300
Saturation velocity, v_s (10^7 cm/s)	1.0	2.0	2.0	3.0
Thermal conductivity, χ (W/cmK)	1.5	0.5	4.9	1.3
Relative dielectric constant, ε_r	11.8	12.8	9.7	9.0
Combined figure of merit, $\chi\varepsilon_r\mu v_s E_B^2/(\chi\varepsilon_r\mu v_s E_B^2)_{\mathrm{Si}}$	1	8	458	489

1.2 Theory of AlGaN/GaN HFETs

In its simplest form, an AlGaN/GaN HFET consists of a substrate, usually sapphire, SiC, or sometimes Si, a metalorganic chemical vapor deposited (MOCVD) or molecular beam epitaxy (MBE) grown GaN channel layer, and a similarly grown $Al_xGa_{1-x}N$ barrier layer with Ohmic source and drain contacts and a Schottky gate defined over a selectively etched mesa into the

heterostructure. A basic HFET structure can be seen in Figure 1.1.

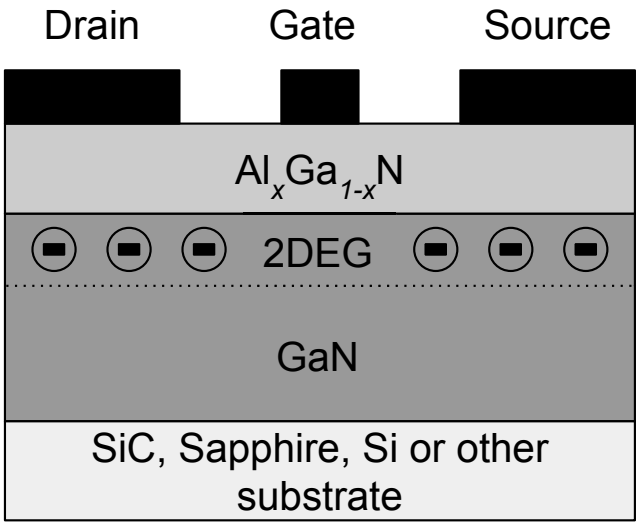


Figure 1.1: A basic HFET structure. Width is defined normal to this surface.

If one examines the band diagram of the HFET, one can see the benefits of the heterostructure. Figure 1.2 shows such a band diagram. An almost triangular quantum well is formed at the heterointerface between the AlGaN barrier and the GaN channel. This gives rise to an ensemble of free electrons, creating what is known as a two-dimensional electron gas (2DEG). This 2DEG forms a conduction path along the channel of the HFET from source to drain. In the standard case of an AlGaN/GaN HFET and unlike the case of an inversion MOSFET, this 2DEG forms without any applied gate bias. In order to deplete the channel, a negative bias must be applied between the gate and the GaN channel layer. An AlGaN/GaN HFET is therefore a "normally-on", or a "depletion mode" device. Techniques such as fluoride ion implantation into the AlGaN layer can shift the threshold voltage of an HFET and create "enhancement mode" devices, which require a positive gate-channel bias for maintaining a conductive path between the source and the drain contacts.

The band diagram of Figure 1.2 illustrates the existence of the 2DEG but does not explain its root cause. The ingenuity behind the AlGaN/GaN HFET lies in the fact that both GaN and AlGaN are polar materials. The combination of certain orientations of GaN and AlGaN crystal structures creates both spontaneous and piezoelectric polarization discontinuity at the heterointerface. By

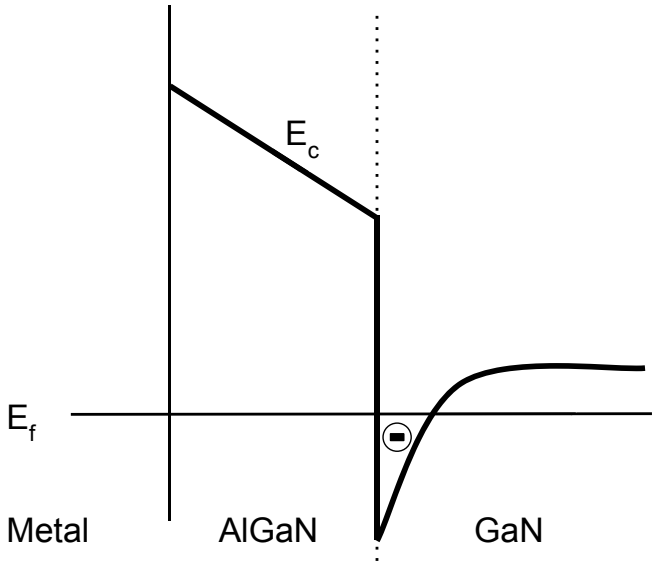


Figure 1.2: A simple conduction band-edge diagram at the AlGaN/GaN heterointerface under thermal equilibrium. An almost triangular quantum well is formed at the heterointerface yielding a reservoir of electrons, known as a two-dimensional electron gas (2DEG).

engineering the GaN and AlGaN growth, one can ensure crystal orientations in which the electric fields due to spontaneous and piezoelectric polarization act to confine electrons at the AlGaN/GaN interface thereby creating the 2DEG.

Initial work describing the phenomena of spontaneous and piezoelectric polarization creating 2DEGs in AlGaN/GaN HFETs was put forth by Ambacher et al. [4, 5]. To understand 2DEG formation, one must first explain the crystal structure of GaN and AlGaN. In this discussion one can ignore the zinc-blend crystal structure of GaN as the majority of electronic GaN applications are concerned with the wurtzite structure. For wurtzite binary A–B compounds, as is the case of GaN, the sequence of Ga and N atoms is reversed for the $[0001]$ and $[000\bar{1}]$ directions [4]. This is illustrated in Figure 1.3. The (0001) face is known as the Ga-face and the $(000\bar{1})$ face is known as the N-face [4]. The Ga-face is not equivalent to the N-face as they have different chemical and physical properties [4]. This is important as a given heterojunction of one face will yield a different concentration of 2DEG than the other face or none at all. By growing one Ga-face wafer and two N-face wafers, Ambacher et al. found that a 2DEG was formed at the AlGaN/GaN interface in the case of the Ga-face GaN but neither N-face GaN structures resulted in the formation of a 2DEG

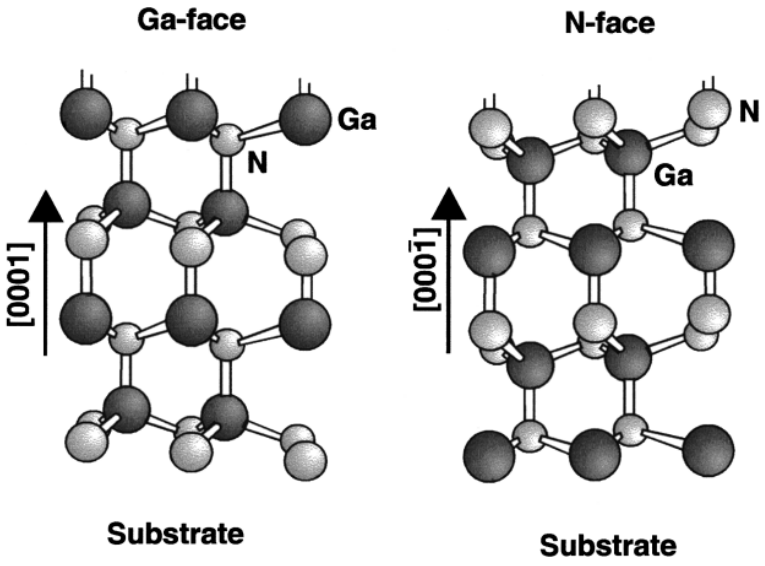


Figure 1.3: Crystal structure of Ga-face and N-face GaN [4].

at the AlGaN/GaN interface [4]. This is due to the different direction of polarizations in Ga-face and N-face GaN. As mentioned before, there are two components to total polarization, spontaneous polarization P_{SP} and piezoelectric polarization P_{PE}. The sum of the two is the total macroscopic polarization, P [4]. Polarization sheet charge density, σ, is a useful metric to describe the net effect of polarizations in the GaN and AlGaN layers. σ is defined as

$$\sigma = P(\text{top}) - P(\text{bottom}) \tag{1.1}$$

$$\sigma = [P_{SP}(\text{top}) + P_{PE}(\text{top})] - [P_{SP}(\text{bottom}) + P_{PE}(\text{bottom})] \tag{1.2}$$

where $P(\text{top})$ represents total macroscopic polarization in the top layer and $P(\text{bottom})$ the same for the bottom layer. In order to achieve a 2DEG at the interface, the value of σ must be positive [4]. Figure 1.4 illustrates the different scenarios in terms of relaxed, tensile strained, and compressively strained for Ga- and N-face AlGaN where σ is positive or negative. The tensile and compressive modes of growth are identified in terms of the difference between the freestanding in-plane lattice constants. Thick layers tend to relax to their freestanding lattice constant. Thin layers tend to adapt a strain, either tensile or compressive, based on the layer they are grown on, assuming that layer is thick. In the case of AlGaN and GaN, the in-plane lattice constant of AlGaN is smaller, hence

when AlGaN is grown over a relaxed thick GaN layer, AlGaN will experience a tensile strain. This is evident in subfigures (b) and (e) of Fig. 1.4. In the case where a thin layer of GaN is grown over a thick AlGaN layer, the GaN will experience a compressive strain. This case is illustrated in subfigures (c) and (f) of Fig. 1.4. If both layers are sufficiently thick, both will relax to their freestanding lattice constants and no piezoelectric polarization will be present. For a structure where

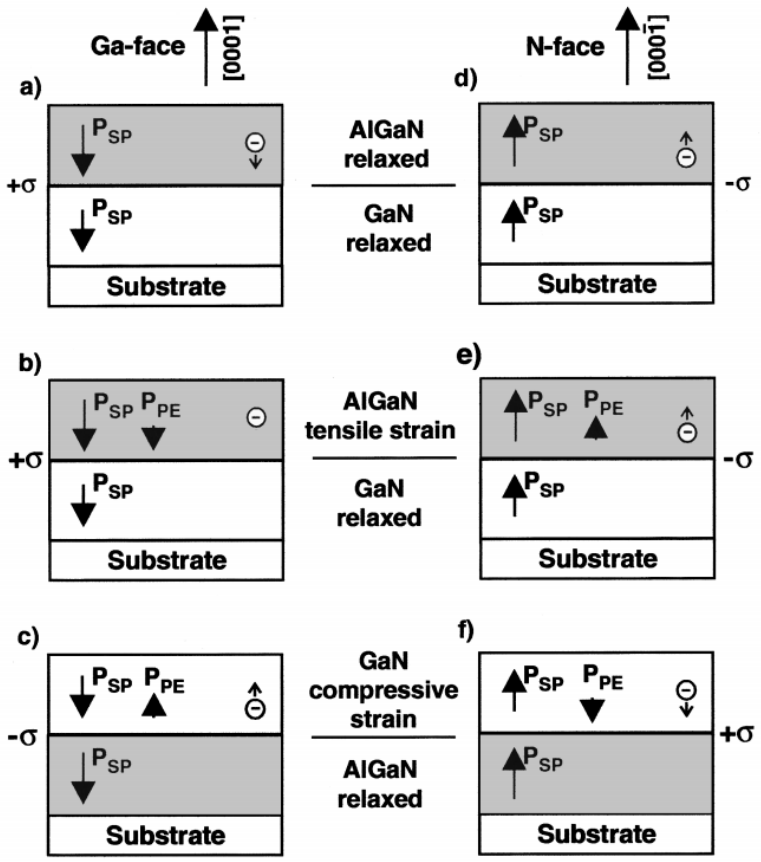


Figure 1.4: Illustration showing the the effect of spontaneous and piezoelectric polarization on the net macroscopic polarization for relaxed, tensile, and compressively strained AlGaN/GaN heterojunctions [4].

AlGaN is grown on top of GaN (the usual case for AlGaN/GaN HFETs), the GaN must be Ga-face to achieve a 2DEG at the interface. In the case where GaN is grown on AlGaN, N-face GaN will yield a 2DEG at the interface [4]. In other words, for the simple HFET structure represented in Figure 1.1, the GaN must be Ga-face to produce the shown 2DEG.

One of the unique aspects of $Al_xGa_{1-x}N$/GaN HFETs is that the Al mole fraction x provides

the device engineer with an additional knob with which to alter the transistor structure to achieve a desired end. For instance, $Al_xGa_{1-x}N$ transition layers can be grown on top of a non-native lattice mismatched substrate to help lattice match the GaN layer to the substrate. Transition layer's Al mole fraction can be slightly tuned across a number of monolayer such that the overall composition of the buffer layer is graded. This lattice matching helps reduce stress and defects in the GaN layer, leading to better device performance. The Al mole fraction in the barrier layer can also be adjusted.

1.3 Problems with AlGaN/GaN HFETs

III-Nitrides and AlGaN/GaN HFETs in particular are relatively new technologies. For this reason there are many kinks in the technology that need to be worked out before mass adoption and commercialization can take place. These problems include the lack of a lattice matched substrate, difficulty in growing high quality AlGaN/GaN films by MBE and MOCVD, difficulty in fabricating enhancement mode devices, and difficulty in forming high quality Ohmic contacts, among others. There are also reliability concerns. Chief among these are current-collapse, gate-lag, gate leakage, and strain relaxation. Of these concerns, Ohmic contact formation and gate leakage will be discussed in detail in this thesis.

1.4 Thesis Outline

One of the major focuses of this thesis is on the fabrication and characterization of Ohmic contacts to AlGaN/GaN HFETs. For this reason, Chapter 2 will discuss Ohmic contacts in detail. Section 2.1 describes the measurement technique used to determine contact resistance, specific contact resistivity, and sheet resistance. Section 2.2 discusses the theory of Ohmic contact formation. Section 2.3 provides a complete literature review of Ohmic contacts to AlGaN/GaN, highlighting the best published results. Finally, Section 2.4 discusses the chosen metalization schemes for the fabricated devices.

Chapter 3 discusses the process details of the fabrication of AlGaN/GaN HFETs. Each unit step

is explained and rationale on process recipes is provided. Technology characterization such as mesa height profiling is provided where applicable.

Chapter 4 provides electrical characterization results. Contact resistance is analyzed over temperature in Section 4.1. Section 4.2 analyzes current-voltage characteristics. Section 4.3 presents capacitance-voltage profiling over temperature to determine carrier concentration.

Chapter 5 presents the simulation of off-state gate leakage mechanisms as a function of Al mole fraction. Four leakage mechanisms are examined: Fowler-Nordheim, Poole-Frenckel, Thermionic Field Emission, and Trap Assisted Tunneling. Analytical models of each mechanism are presented. Variation with gate bias and Al mole fraction are shown.

Finally, Chapter 6 presents the conclusion and suggests future work.

Chapter 2

Ohmic Contacts to AlGaN/GaN 2DEGs

The ability to form low resistance Ohmic contacts is critical to any semiconductor fabrication technology. Good Ohmic contacts are important for numerous reasons. Reduced contact resistance will reduce resistive heating, allow for high transconductance and high saturation currents [6], and reduce knee voltage [7]. Besides reduced contact resistance, Ohmic contact structure also affects the surface morphology of the source/drain contacts. One aspect of surface morphology is the roughness of the contact. A rough contact does not lend itself to easy probing when attempting to measure contact resistance and other device characteristics. Another important aspect of surface morphology is lateral diffusion of metal during the high temperature annealing process. It is necessary to limit this diffusion to achieve good edge acuity for use in small channel devices [7, 8]. For these reasons, an in-depth discussion of Ohmic contacts is merited.

2.1 Ohmic Contact Measurement

There are numerous test structures defined on the mask set used for fabrication. The most significant of these test structures for the purpose of this thesis are the transfer length method (TLM) patterns. Transfer length method patterns allow for the characterization of contact resistance, R_C, specific contact resistivity, ρ_c, and sheet resistance, R_{sh}. TLM patterns are especially useful as they allow one to characterize the quality of ohmic contact formation to the 2DEG in AlGaN/GaN HFETs.

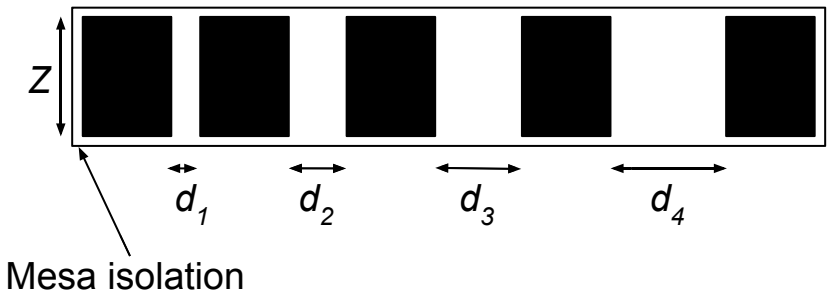


Figure 2.1: Graphical representation of the TLM Patterns.

Figure 2.1 is a graphical representation of the TLM patterns as they appear on the die. According to the figure, Z represents the pad height and d_i represents the spacing between TLM pads. On our mask set $d_1 = 1\,\mu\text{m}$, $d_2 = 2\,\mu\text{m}$, $d_3 = 3\,\mu\text{m}$, and $d_4 = 4\,\mu\text{m}$. By looking at the I-V curves for each of the four pad spacings, we can measure the total resistance, R_T, across each two adjacent pads. From this total resistance, we can extract out the effect of the channel resistance and find the contact resistance. After the I-V characteristics for a pad spacing d_i is measured, the total resistance of that spacing is simply the reciprocal of the linear current vs. voltage curve. This characteristic will only be linear in the case of Ohmic contacts to the pads and the 2DEG and when the applied voltage between the pads is limited to small or moderate values. This total resistance is defined in terms of two factors [9]: contact resistance, R_C, and sheet resistance, R_{sh}, the later of which is related to the conductivity of the 2DEG. The total resistance is given by [9] as

$$R_T = \frac{R_{sh}d}{Z} + 2R_C \approx \frac{R_{sh}}{Z}\left(d + 2L_T\right). \tag{2.1}$$

In the TLM procedure, first, for different pairs of adjacent pads, the total resistance is measured and recorded. Next, by plotting R_T vs. pad spacing, we can derive the effect of contact resistance ignoring the channel resistance. Figure 2.2 illustrates this technique. From the figure, L_T is known as the transfer length and R_C is the contact resistance. This technique can be simply understood as the extrapolation of total resistance to an infinitesimally small pad spacing, thus neglecting any sheet resistance. The y-intercept of Figure 2.2 is $2R_C$ rather than R_C as there are two contacts whose effect is additive. The contact resistance, R_C, is presented in units of Ω. In the literature, however,

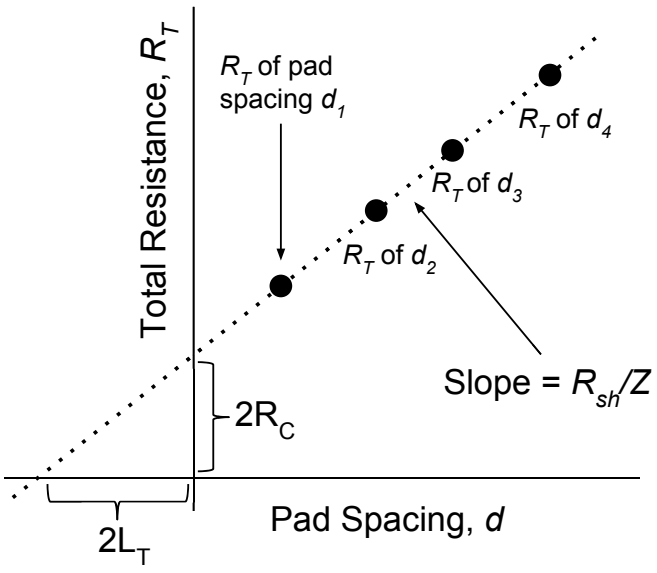


Figure 2.2: Plot of the total resistance vs. pad spacing.

contact resistance is normalized to the pad width and is presented in units of Ω mm. This is done simply by multiplying R_C by the pad width, Z, in units of millimeters. Herein, contact resistance will be assumed to have units of Ω mm unless otherwise stated.

As mentioned above, two other parameters, namely sheet resistance, R_{sh} and specific contact resistivity, ρ_c can be determined from Figure 2.2. Sheet resistance in the context of AlGaN/GaN HFETs is synonymous with the 2DEG channel resistance. From Figure 2.2, sheet resistance is defined as the slope of fitted line multiplied by the pad width. That is,

$$R_{sh} = \frac{\Delta R_T}{\Delta d} Z. \tag{2.2}$$

Sheet resistance has units of Ω/□. Specific contact resistivity, ρ_c is defined according to [9] as

$$\rho_c = R_C L_T Z \tag{2.3}$$

where in the literature, specific contact resistivity is presented with units of Ω cm^2.

The TLM method relies on several assumptions. First, Equation (2.1) assumes that the sheet resistance under the contact is the same as the sheet resistance between the contacts [9]. Strictly

speaking, this is not the case in Ohmic contacts made to AlGaN/GaN HFETs. In short, this is since the mechanism of alloyed contact formation that allows for the making of Ohmic contacts between source/drain metal and 2DEG is bound inherently to change the sheet resistance under the contact. In this technique, R_c is a measure of contact resistance whereas ρ_c depends on L_T according to (2.3), which itself changes with R_{sh} according to Figure 2.2. In addition to implications of the assumption of a constant sheet resistance, even in the case of non-alloyed contacts, sometimes the x-intercept at $R_T = 0$ is not well defined leading to incorrect values of ρ_c [9]. In spite of these deficiencies, the TLM measurement technique is the most widely used technique used to compare the quality of Ohmic contacts in III-Nitride technology. As the majority of published works on Ohmic contact formation to III-Nitride materials use this technique, our use of this technique allows for more accurate comparison of results between this study and other works.

The optimal test structure for an alloyed Ohmic contact, as in the case of AlGaN/GaN HFETs, is a trilayer transmission line model (TLTLM) [9, 10]. This model more accurately describes the physical situation in AlGaN/GaN HFETs by simulating a metal layer, alloyed layer, and an un-alloyed layer between contacts [10]. This model defines specific contact resistivities for the metal-alloyed interface and the alloyed-unalloyed interface as well as sheet resistances for each layer. The specific details of the model are presented in [10]. Unfortunately, standard TLM patterns present on the mask set used in our studies do not provide sufficient data for the determination of TLTLM parameters [10].

2.2 Theory of Ohmic Contacts to AlGaN/GaN

In the dominant silicon technology, Ohmic contacts can be formed in various ways. In the most simple form, a metal of appropriate work function can be deposited on the silicon and a reasonable quality Ohmic contact can be achieved. AlGaN/GaN HFETs, however, present some challenges to this problem that the Si technology does not. The AlGaN layer serves as an effective barrier to carrier transport due to its wide bandgap. Thus any effective ohmic contact must enhance the

tunneling of electrons through this layer (i.e. from the source/drain contact to the 2DEG).

Typically, Ohmic and Schottky metalizations to III-Nitrides are done by e-beam evaporation of a multi-layered stack of different metals. For Ohmic contacts, the metal stack usually follows a Ti/Al/metal/Au pattern. The top Au layer is used to provide a smooth surface. The third layer metal, usually Ti or Ni, serves to prevent the combination of Al with Au, since $AlAu_y$ compounds have high resistivity. The first two layers of Ti and Al serve to combine and form compounds with work functions that allow for Ohmic contact formation to AlGaN. Metal stack compositions and annealing temperature impact both contact resistance and surface morphologies of Ohmic contacts. Various metalizations and annealing conditions are described in greater detail below.

2.2.1 Formation of Ohmic Contacts

There are two general theories as to how Ohmic contacts to AlGaN/GaN structures are formed. The first posits that the formation of TiN or $AlTi_2N$ at the interface of the metal and AlGaN layer is the source of the Ohmic contact formation via the *n*-type doping of the AlGaN barrier layer [7, 11]. Ruvimov et al. [11] were the first to note the formation of $AlTi_2N$ at the metal/AlGaN interface. This study provided evidence to support the fact that $AlTi_2N$ was necessary for Ohmic formation to the AlGaN/GaN 2DEG. Reactions during the high temperature annealing process performed after patterning the Ohmic contact were shown to create a nitrogen-containing interfacial layer, which creates N-vacancies in the barrier layer leading to conduction [11]. This was one of the first studies to note that contact resistance increases with Al mole fraction in the AlGaN barrier layer and that the contact resistance depends on metalization scheme, and therefore that the contact resistance depends on the formation of certain alloys at the metal/AlGaN interface [11]. Bright et al. [7] supported the idea that diffusion of metals into the AlGaN barrier layer could yield an *n*-type doped barrier and therefore a conduction path from metal to 2DEG. Bright et al. showed that while TiN protrusions did directly penetrate the AlGaN barrier to a depth of 10 nm, this was not sufficient to create a direct electrical path in the case of a 30 nm barrier thickness [7].

The second theory proposes that the direct penetration seen in [7] causes the formation of TiN

islands or protrusions along threading dislocations or defects in the AlGaN barrier, which allows for direct connection between the metal and 2DEG [8, 12, 13]. In this case, the addition of high conductivity Al is believed to improve the contact resistance of the direct electrical connection through the AlGaN [12].

The reality is that both mechanisms likely play a role in Ohmic contact formation. Depending on the metal stack composition, anneal conditions and substrate quality, one mechanism may outweigh the other but both mechanisms are clearly present [7, 8, 12, 13].

2.2.2 Surface Morphology

Contact resistance is not the only important metric in characterizing Ohmic contacts. Surface morphology of the contacts is also critical. One measure of surface morphology is lateral diffusion of contact metal during annealing [12]. When the third metal fails to prevent the diffusion of Au, it has been shown that $AlAu_y$ alloys with low melting points can cause lateral diffusion of source/drain metals [12]. During annealing, these metals can spread and expand their feature size beyond the mask-defined size. In the case of short channels, this lateral spread of metal can cause shorts between the gate and source/drain metals. It is therefore important that the Ohmic metal stack also be designed to limit such lateral diffusion, as well as to achieve low contact resistance. In the study done by Mohammed et al., in addition to contact resistance of metal stacks [12], lateral diffusion of metals was also analyzed. In this study, a 2 µm spacing was defined between two Ohmic metal stacks for a variety of third layer metals. Distance of the spacing was measured before and after annealing. Results of this analysis are shown in Figure 2.3. It was found that Ti diffused the greatest distance after annealing while Pt diffused the least. The amount of diffusion is temperature dependent, however, the overall trend for each temperature seems to be approximately the same.

Interestingly, for third layer titanium, lateral diffusion is worse at 850 °C than at 950 °C. This runs contrary to what might be expected from a simplistic analysis. For example, it may be assumed that higher temperature would cause greater lateral diffusion for all metals due to the increased kinetic energy. This is clearly not the case as seen in Figure 2.3. However, no theory for this fact

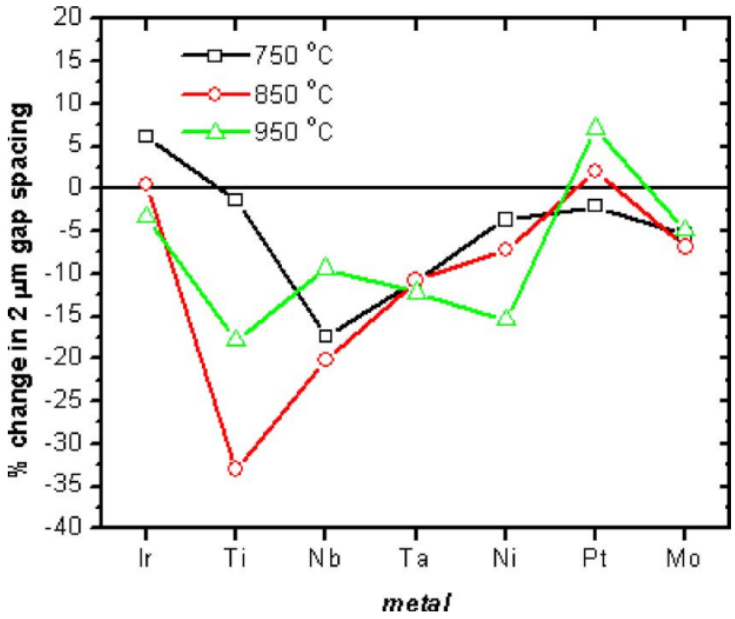


Figure 2.3: Lateral diffusion of third layer metals with temperature [12].

was presented in [12].

The issue of lateral diffusion of Ohmic metals will be further discussed in Chapter 3 in the analysis of the fabrication results.

2.3 Literature Review of Ohmic Contact Performance

As mentioned earlier, the first AlGaN/GaN HFET was developed by Khan et al. [1] in 1993. In this device, Ti/Au Ohmic contacts of 25 Å/1500 Å were deposited and annealed at 250 °C for 60 s [1]. Unfortunately, no results for contact resistance or specific contact resistivity were published in this initial report.

One of the first reports of Ohmic contacts to GaN was published by Foresi et al. in the same year [14]. This study, instead of a multilayered metal stack, analyzed simple Au and Ti contacts annealed at 575 °C for 10 min [14]. This is both significantly lower temperature and longer duration than modern anneals. Results showed specific contact resistivities of $\rho_c = 1.6 \times 10^{-5}$ to $3.1 \times 10^{-5}\,\Omega\text{cm}^2$ and $\rho_c = 0.12 \times 10^{-5}$ to $4.4 \times 10^{-5}\,\Omega\text{cm}^2$ for Au and Ti, respectively [14]. The large variation of ρ_c was attributed to the nonuniformity of the GaN film [14].

Khan et al. later investigated Ohmic contact formation to AlGaN/GaN heterojunctions [6]. This study, however, does not present the metal stack or thicknesses used for the Ohmic contacts, only specifying that the contacts are alloyed. The best results presented are a contact resistance of 2.3 Ω mm and a specific contact resistivity of 8.8×10^{-5} Ω cm^2. Burm et al. built on this work and presented some early work on Ohmic contact formation to AlGaN/GaN HFETs [15]. In this study, two Ohmic contacts were tested. The first was an unalloyed Ti/Au metal stack that achieved a contact resistance of 10 Ω mm. In the second, the simple annealed Ti contact achieved a contact resistance of 4.8 Ω mm.

The initial values of contact resistance measured by Khan, Burm, and colleagues are relatively high, especially considering more recent published results. The results of Fan et al. [16] and Wu and colleagues [17] showed that these values of contact resistance could be brought down by altering metal stack composition, thickness, and annealing conditions.

Fan et al. [16] were the first to employ a Ti/Al/Ni/Au metal stack to *n*-GaN. They used metal thicknesses of 150 Å/2200 Å/400 Å/500 Å with the Ti and Ni layers deposited by e-beam evaporation and the Al and Au layers deposited by thermal evaporation. Annealing temperature and duration were 900 °C for 30 s. According to these conditions, they achieved specific contact resistivity of 1.19×10^{-7} and 8.9×10^{-8} Ω cm^2 for doping levels of 2×10^{17} and 4×10^{17} cm^{-3}, respectively [16]. This study is slightly unusual as before the mesa isolation stage, the surface of the GaN is roughened by RIE. This likely leaves the surface highly *n*-type [16]. Additionally, this surface roughening allows fairly good Ohmic contact formation without annealing the metal stack. A non-alloyed Ti/Al/Ni/Au non-alloyed contact achieved $\rho_c = 3.3 \times 10^{-6}$ Ω cm^2 [16].

Wu et al. [17] confirmed the benefits of a Ti/Al/Ni/Au metal stack by replicating the same metal stack and RTA conditions used in [16]. They achieved a contact resistance of 0.5 to 0.7 Ω mm [17]. These results were roughly an order of magnitude better than initial studies reported in [6] and [15].

In 1997, Chu et al. presented an improved Ohmic contact metal stack and RTA process [18]. In this study, two metal stacks were used that yielded very good Ohmic contacts to a modulation-doped HFET structure. For both contacts, annealing conditions were 800 °C for 30 s (i.e. 100 °C less than

previous studies) [18]. This was done to reduce surface roughness of the contacts [18]. The first contact was Ti (200 Å)/Al (1000 Å)/Ti (450 Å)/Au (550 Å) and achieved minimum contact resistance of 0.6 Ω mm and specific contact resistivity of $3.44 \times 10^{-6}\,\Omega\,\mathrm{cm}^2$ [18]. The second contact was Pd (200 Å)/Al (1000 Å)/Ti (450 Å)/Au (550 Å) and achieved minimum contact resistance of 0.25 Ω mm and specific contact resistivity of $5.95 \times 10^{-7}\,\Omega\,\mathrm{cm}^2$ [18].

Ping et al. presented results of simple Ti/Al ohmic contacts with typical contact resistances of 0.5 Ω mm [19]. No information on the thicknesses or annealing temperatures were provided in this study.

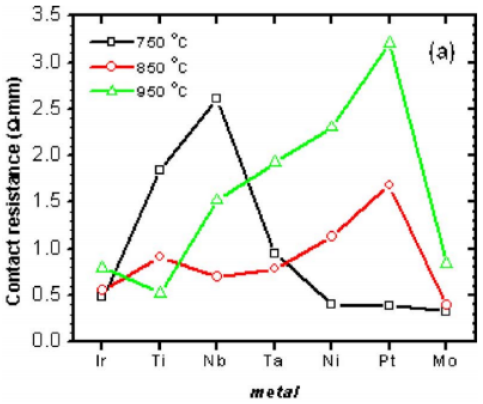
Cai et al. investigated a variety of metalization schemes including Ti/Al, Ti/Al/Ni, Ti/Al/Pt, Ti/Al/Ni/Au, and Ti/Al/Pt/Au [20]. A Ti (200 Å)/Al (800 Å)/Pt (400 Å)/Au (1500 Å) metal stack annealed at 900 °C for 35 s in N_2 ambient achieved a minimum contact resistance of 0.039 Ω mm and specific contact resistivity of $5.38 \times 10^{-8}\,\Omega\,\mathrm{cm}^2$, the lowest published value at the time in 1998 [20]. The contact resistances for the other metalizations are given as 0.15 Ω mm, 0.36 Ω mm, 0.52 Ω mm, however it is not explained which metalization these values correspond to [20]. It is interesting to note that the Ti/Al/Pt/Au outperformed the other metal stacks by nearly an order of magnitude. The observation that Ti/Al/Pt/Au outperforms Ti/Al/Ni/Au by such a large amount does not fit with the later findings of Mohammed et al. [12].

Hilsenbeck et al. analyzed a Ti (100 Å)/Al (500 Å)/Ti (250 Å)/Au (300 Å)/WSiN (1200 Å) Ohmic metalization annealed at 850 °C for 30 s in N_2 [21]. Measured contact resistance was 0.9 Ω mm directly after fabrication and 1.05 Ω mm after one day of aging [21]. The WSiN encapsulation layer was borrowed from GaAs technology and appeared to help limit surface roughness during annealing [21].

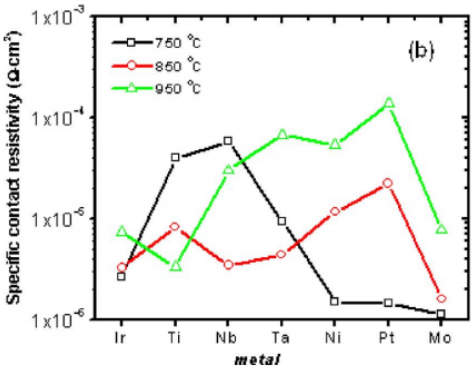
Work by Wang et al. explored Ti/Al/Pt/Au versus V/Al/Pt/Au on n-type $Al_{0.4}Ga_{0.6}N$/GaN [22]. With Ti (260 Å)/Al (740 Å)/Ti (500 Å)/Au (500 Å) and anneal conditions of 800 °C for 30 s in N_2 ambient, a specific contact resistance of $2 \times 10^{-5}\,\Omega\,\mathrm{cm}^2$ was achieved accounting for the effect of the sheet resistance of the metal contact [22]. When the initial Ti layer was replaced with V, thicknesses of 150 Å/850 Å/500 Å/500 Å yielded the lowest contact resistance with a specific

contact resistance of $(1.1 \pm 0.1) \times 10^{-5}\,\Omega\,\mathrm{cm}^2$ [22]. It was found that with the V/Al/Pt/Au metal stack anneal temperature could be lowered compared to the traditional metal stack. For the case of the V/Al/Pt/Au metal stack, the optimal anneal conditions were 650 °C for 30 s [22]. For these conditions with the Ti/Al/Pt/Au stack, the highest specific contact resistivity achieved was $10^{-3}\,\Omega\,\mathrm{cm}^2$ [22]. The study of Wang et al. is notable because it provides a method for reducing the thermal budget of the fabrication process by altering the metal stack composition and thicknesses.

One of the first studies to systematically determine the effect of metal composition and anneal temperature on the quality of Ohmic contacts was performed by Mohammed et al. [12]. In this study, Ti/Al/metal/Au Ohmic contacts are analyzed across anneal temperatures from 750 °C to 950 °C where the metals are Ir, Ti, Nb, Ta, Ni, Pt, and Mo. All metal stack thicknesses were Ti (150 Å)/Al (600 Å)/metal (350 Å)/Au (500 Å). A summary of the Ohmic contact quality can be seen in Figure 2.4. From this figure one can see that Ti, Ni, Pt, and Mo perform roughly the same although at



(a) Contact resistance vs. metal and anneal temperature



(b) Specific contact resistivity vs. metal and anneal temperature

Figure 2.4: Effect of metal composition and anneal temperature on Ohmic contact quality [12].

different anneal temperatures. Extracting from the figure, one can estimate a contact resistance of 0.4 to 0.5 Ω mm for these metals. One of the interesting results of this study is the variation of contact resistance and specific contact resistivity with metal. As the third metal layer was originally only suspected to act as a diffusion barrier to prevent Al combining with Au, it is surprising that this metal layer plays such an important role in determining the quality of the Ohmic contact.

From Fig. 2.4, it is evident that each metal has its own unique optimal anneal temperature. In

other words, the temperature that one should perform the anneal at is dependent on the metal stack composition. Ni, Pt, and Mo prefer a lower anneal temperature while Ti, the most common metal in this position of the stack, prefers a higher temperature. The fact that there are such large differences in Ohmic contact quality across metals and temperatures suggests that contact formation is not only dependent on interfacial reactions but also on the barrier layer [12].

The success of such schemes that use the Ti/Al/metal/Au structure rests on the formation of TiN penentrating through the barrier creating donor-like N-vacancies which then lowers the barrier at the GaN surface [23]. Recent work by Pang et al. has postulated that by allowing for Ti-Al alloy formation penetrating through the barrier, superior Ohmic contacts can be achieved due to Ti-Al alloy's lower resistivity and work function when compared to Ti [23]. However, AlN does not behave in the same way as TiN. In fact, AlN formation is unwanted because, unlike TiN, it is nonmetallic and can actually increase contact resistance [23].

Pang et al. proposed a novel Ti/Al multilayered structure to eliminate AlN formation while still allowing for Ti-Al alloying across the barrier layer [23]. In the study, they compare a traditional Ti (300 Å)/Al (900 Å)/Ti (300 Å)/Au (600 Å) metal stack to a multilayered Ti (300 Å)/Al (300 Å)/Ti (300 Å)/Al (300 Å)/Ti (300 Å)/Au (600 Å) metal stack. Both samples are annealed at 830 °C for 30 s in an N_2 ambient. The traditional Ti/Al/Ti/Au metal stack had a contact resistance of $R_c = 1.7\,\Omega\,\text{mm}$ and specific contact resistivity of $\rho_c = 5.69 \times 10^{-5}\,\Omega\,\text{cm}^2$, while the multilayer scheme achieved $R_c = 0.52\,\Omega\,\text{mm}$ and $\rho_c = 4.52 \times 10^{-6}\,\Omega\,\text{cm}^2$ [23]. Under the same conditions, a multilayered scheme that prevents the diffusion of AlN outperformed the traditional metal stack. Pang et al. also analyzed a third sample with Ti (300 Å)/Al (300 Å)/Ti (300 Å)/Au (600 Å) metal stack. the purpose of this third sample was to prove that it is not only in-diffusion of Al that should be minimized. By reducing the thickness of the second layer Al, in-diffusion should thereby be reduced. However, this third sample measured $R_c = 18\,\Omega\,\text{mm}$ and $\rho_c = 3.42 \times 10^{-3}\,\Omega\,\text{cm}^2$ under the same anneal conditions as the other two samples [23]. This showed that while you can minimize in-diffusion of Al, the overall reduced thickness allows for Au to penetrate the entire metal stack and thereby increases contact resistance due to its high work function and the combination of Al and Au [23].

The Ti/Al multilayered structure solves both problems (i.e. the overall thickness of the metal stack prevents Au from penetrating the barrier while the thinner Ti/Al layers allow Ti-Al-Au formation rather than just Al-Au formation) all while low resistance Ti-Al alloys are able to penetrate the barrier.

Recent work by Mahajan et al. on Ti/Al/Ni/Au metal stacks to $Al_{0.28}Ga_{0.72}N$/GaN has investigated the optimal ratio of Ti to Al [24]. This study investigated Ti:Al ratios of 1:0, 1:1.5, 1:5, and 1:7. The total metal stack thickness are shown in Table 2.1. Results of the study indicated that minimum contact resistance was achieved for a Ti:Al ratio of 1:5. This sample had a contact resistance of 0.3 to 0.6 Ω mm when annealed at 820 °C [24]. This study also showed that sample "a" with no Al layer did not produce an Ohmic contact, as expected. Also, x-ray diffraction (XRD) showed a high likelyhood of TiN in samples "c" and a low likelyhood of TiN in sample "d" [24]. This supports the above studies indicating that TiN is necessary in Ohmic contact formation.

Table 2.1: Optimal Ti:Al ratios [24].

		Thicknesses [Å]			
Sample name	Ti:Al Ratio	Ti	Al	Ni	Au
a	1:0	200	0	400	1000
b	1:1.5	200	300	400	1000
c	1:5	200	1000	400	1000
d	1:7	200	1400	400	100

Table 2.2 presents an overview of published results of contact resistances. Where multiple values for a particular metalization scheme and RTA condition are given, the minimum value is presented in the table. The table is presented in chronological order.

Table 2.2: Summary of Ohmic contact quality to GaN or AlGaN/GaN.

Metal layers	**Thickness [Å]**	**Layer Structure**	**RTA Condition**	R_c **[Ω mm]**	ρ_c **[Ω cm^2]**	**Ref.**
Au		Undoped GaN	575 °C 10 min		1.6×10^{-5}	[14]
Ti		Undoped GaN	575 °C 10 min		1.2×10^{-6}	[14]
Ti/Au		Si doped $Al_{0.15}Ga_{0.85}N$/GaN		2.3	8.8×10^{-5}	[6]
Ti/Au		Si doped $Al_{0.15}Ga_{0.85}N$/GaN	Unalloyed	10		[15]
Ti		Si doped $Al_{0.15}Ga_{0.85}N$/GaN	800 °C 120 s	4.8		[15]
Ti/Al/Ni/Au	150/2200/400/500	Si doped n-GaN (5×10^{17} cm^{-3})	900 °C 30 s		8.9×10^{-8}	[16]
Ti/Al/Ni/Au	150/2200/400/500	Si doped n-GaN (5×10^{17} cm^{-3})	Unalloyed		3.3×10^{-6}	[16]
Ti/Al/Ni/Au	150/2200/400/500	Si doped $Al_{0.15}Ga_{0.85}N$/GaN (2×10^{18} cm^{-3})	900 °C 30 s	0.5		[17]
Ti/Al/Ti/Au	200/1000/450/550	Si doped $Al_{0.3}Ga_{0.7}N$/GaN (7×10^{19} cm^{-3})		0.6	3.44×10^{-6}	[18]
Pd/Al/Ti/Au	200/1000/450/550	Si doped $Al_{0.3}Ga_{0.7}N$/GaN (7×10^{19} cm^{-3})		0.25	5.95×10^{-7}	[18]
Ti/Al		Doped $Al_{0.2}Ga_{0.8}N$/GaN		0.5		[19]
Ti/Al/Pt/Au	200/800/400/1500	AlGaN/GaN	900 °C 35 s N_2	0.039	5.38×10^{-8}	[20]
Ti/Al	1000/1000	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	900 °C	0.15	4.30×10^{-7}	[25]
Ti/Al/Ti/Au/WSiN	100/500/250/300/1200	Si doped $Al_{0.25}Ga_{0.75}N$/GaN	850 °C 30 s N_2	0.9		[21]
Ti/Al/Ti/Au	260/740/500/500	n-type $Al_{0.4}Ga_{0.6}N$/GaN	800 °C 30 s N_2		2×10^{-5}	[22]
V/Al/Ti/Au	150/850/500/500	n-type $Al_{0.4}Ga_{0.6}N$/GaN	650 °C 30 s N_2		1.1×10^{-5}	[22]
Ti/Al/Ni/Au	200/2200/550/450	Undoped $Al_{0.33}Ga_{0.67}N$/GaN	870 °C 30 s			[26]
Ti/Al/Ni/Au	300/1800/400/1500	Si doped $Al_{0.25}Ga_{0.75}N$/GaN (1×10^{19} cm^{-3})	900 °C 30 s N_2	0.20	7.30×10^{-7}	[27]
Ti/Al/Mo/Au	150/600/350/500	Doped $Al_{0.2}Ga_{0.8}N$/GaN (2×10^{18} cm^{-3})	800 °C 30 s N_2	0.20	4.5×10^{-7}	[28]
Ti/Al/Mo/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	850 °C 30 s	0.17	2.96×10^{-7}	[8]
Ti/Al/Mo/Au	150/600/350/500	AlGaN/GaN	850 °C 30 s	0.25		[29]
Ti/Al/Ni/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	750 °C 30 s N_2	0.40	1.06×10^{-5}	[12]
Ti/Al/Ni/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	850 °C 30 s N_2	1.10	1.01×10^{-5}	[12]
Ti/Al/Ni/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	950 °C 30 s N_2	2.30	2.04×10^{-5}	[12]
Ti/Al/Pt/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	750 °C 30 s N_2	0.40	1.04×10^{-6}	[12]
Ti/Al/Pt/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	850 °C 30 s N_2	1.70	1.12×10^{-5}	[12]
Ti/Al/Pt/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	950 °C 30 s N_2	3.20	1.03×10^{-4}	[12]
Ti/Al/Mo/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	750 °C 30 s N_2	0.31	1.01×10^{-6}	[12]
Ti/Al/Mo/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	850 °C 30 s N_2	0.40	1.06×10^{-6}	[12]
Ti/Al/Mo/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	950 °C 30 s N_2	0.82	4.55×10^{-6}	[12]
Ti/Al/Ta/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	750 °C 30 s N_2	0.95	5×10^{-6}	[12]
Ti/Al/Ta/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	850 °C 30 s N_2	0.80	1.5×10^{-6}	[12]
Ti/Al/Ta/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	950 °C 30 s N_2	1.90	2.2×10^{-5}	[12]
Ti/Al/Ti/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	750 °C 30 s N_2	1.85	1.4×10^{-5}	[12]

Table 2.2: Summary of Ohmic contact quality to GaN or AlGaN/GaN (continued).

Metal layers	**Thickness [Å]**	**Layer Structure**	**RTA Condition**	R_c **[Ω mm]**	ρ_c **[Ω cm^2]**	**Ref.**
Ti/Al/Ti/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	850 °C 30 s N_2	0.90	4×10^{-6}	[12]
Ti/Al/Ti/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	950 °C 30 s N_2	0.50	1.3×10^{-6}	[12]
Ti/Al/Ir/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	750 °C 30 s N_2	0.49	1.2×10^{-6}	[12]
Ti/Al/Ir/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	850 °C 30 s N_2	0.55	1.3×10^{-6}	[12]
Ti/Al/Ir/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	950 °C 30 s N_2	0.80	2.5×10^{-6}	[12]
Ti/Al/Nb/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	750 °C 30 s N_2	2.60	2×10^{-5}	[12]
Ti/Al/Nb/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	850 °C 30 s N_2	0.70	1.3×10^{-6}	[12]
Ti/Al/Nb/Au	150/600/350/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	950 °C 30 s N_2	1.50	1.25×10^{-5}	[12]
Ti/Al/Mo/Au	150/600/350/500	n-GaN (5×10^{16} cm^{-3})	850 °C 30 s N_2		2.96×10^{-7}	[13]
Ti/Mo/Au	450/150/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	900 °C 30 s	0.66	1.08×10^{-5}	[30]
Ti/Al/Au	150/600/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	750 °C 30 s	0.55	9.31×10^{-6}	[30]
Ti/Al/Au	150/600/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	850 °C 30 s	0.71	1.64×10^{-5}	[30]
Ti/Al/Au	150/600/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	950 °C 30 s	0.75	1.89×10^{-5}	[30]
Ti/Al/Au	500/600/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	850 °C 30 s	0.33	2.99×10^{-6}	[30]
Ti/Al/Au	500/600/500	Undoped $Al_{0.3}Ga_{0.7}N$/GaN	950 °C 30 s	0.68	1.36×10^{-5}	[30]
Ti/Al/Ti/Au	200/800/500/550	Undoped $Al_{0.28}Ga_{0.72}N$/GaN		0.41		[31]
Ti/Al/Ti/Au	200/800/600/550	Undoped $Al_{0.28}Ga_{0.72}N$/GaN		0.55		[31]
Ti/Al/Ti/Au	200/800/700/550	Undoped $Al_{0.28}Ga_{0.72}N$/GaN		0.35		[31]
Ti/Al/Ti/Au	200/800/900/550	Undoped $Al_{0.28}Ga_{0.72}N$/GaN		0.90		[31]
Ti/Al/Ti/Au	200/1000/400/550	Undoped $Al_{0.28}Ga_{0.72}N$/GaN	875 °C	0.40		[31]
Ti/Al/Ni/Au	200/1600/500/1000	Undoped $Al_{0.25}Ga_{0.75}N$/GaN	900 °C 30 s	1.05	1.92×10^{-5}	[32]
Ti/Al/Mo/Au	150/600/350/500	Undoped $Al_{0.25}Ga_{0.75}N$/GaN	850 °C 30 s N_2	0.30		[33]
Ti/Al/Ta/Au	200/800/400/1000	Si doped $Al_{0.3}Ga_{0.7}N$/GaN	850 °C 30 s		20.3×10^{-6}	[34]
Ti/Al/Ti/Au	200/800/400/1000	Si doped $Al_{0.3}Ga_{0.7}N$/GaN			2×10^{-6}	[34]
Ti/Al/Ni/Au	200/800/400/1000	Si doped $Al_{0.3}Ga_{0.7}N$/GaN			1.35×10^{-6}	[34]
Ti/Al/Ta/Au	200/800/400/1000	Si doped $Al_{0.3}Ga_{0.7}N$/GaN			1.11×10^{-6}	[34]
Ti/Al/Ta/Au	200/800/400/1000	Si doped $Al_{0.3}Ga_{0.7}N$/GaN	850 °C 30 s		7.27×10^{-7}	[34]
Ti/Al/Ta/Au	200/800/200/1000	Si doped $Al_{0.3}Ga_{0.7}N$/GaN	850 °C		5.0×10^{-5}	[34]
Ti/Al/Ta/Au	200/800/400/1000	Si doped $Al_{0.3}Ga_{0.7}N$/GaN	850 °C		1.1×10^{-6}	[34]
Ti/Al/Ta/Au	200/800/600/1000	Si doped $Al_{0.3}Ga_{0.7}N$/GaN	850 °C		1.5×10^{-5}	[34]
Ti/Al/Ta/Au	200/800/800/1000	Si doped $Al_{0.3}Ga_{0.7}N$/GaN	850 °C		1.02×10^{-5}	[34]
Ti/Al/Ni/Au	200/0/400/1000	Undoped $Al_{0.28}Ga_{0.72}N$/GaN	810 °C	5.80		[24]
Ti/Al/Ni/Au	200/300/400/1000	Undoped $Al_{0.28}Ga_{0.72}N$/GaN	740 °C	2.50		[24]
Ti/Al/Ni/Au	200/1000/400/1000	Undoped $Al_{0.28}Ga_{0.72}N$/GaN	820 °C	0.40		[24]
Ti/Al/Ni/Au	200/1400/400/1000	Undoped $Al_{0.28}Ga_{0.72}N$/GaN	820 °C	1.40		[24]

Table 2.2: Summary of Ohmic contact quality to GaN or AlGaN/GaN (continued).

Metal layers	**Thickness [Å]**	**Layer Structure**	**RTA Condition**	R_c **[Ω mm]**	ρ_c **[Ω cm^2]**	**Ref.**
Ti/Al/Ni/Au	150/2200/400/500	AlGaN/*n*-GaN (10^{18} cm^{-3})	700 °C 60 s Ar	0.15	2.8×10^{-6}	[7]
Ti/Al/Ti/Au	300/900/300/600	*n*-GaN	830 °C 30 s N_2	1.7	5.69×10^{-5}	[23]
Ti/Al/Ti/Al/Ti/Au	300/300/300/300/300/600	*n*-GaN	830 °C 30 s N_2	0.52	4.52×10^{-6}	[23]

2.4 Choosing an Ohmic Metalization

This in-depth literature review was conducted to determine the current state-of-the-art and the best practices for designing Ohmic contacts to AlGaN/GaN HFETs. As a result of this work, two different Ohmic contact structures were chosen to be fabricated.

The first is what will be referred to as the traditional Ohmic contact metalization as it is the most widely used in the literature. This consists of a Ti/Al/metal/Au metal stack. Titanium was chosen as the third layer metal as it is the most common found in the literature, closely followed by nickel. The chosen thicknesses are 250 Å/1500 Å/100 Å/250 Å. This is a 1:6 Ti:Al ratio, slightly higher than what Mahajan et al. [24] found to be the optimal ratio of 1:5 but somewhat less than the ratio used by Fan et al. [16] to achieve low specific resistivity. During this project, Ti was the only common third layer metal available in the cleanroom.

The second Ohmic contact metal stack is what will be referred to as a Ti-Al multilayered structure. In this multilayered structure, the metal stack consists of Ti/Al/Ti/Al/Ti/Au. The thicknesses of this metal stack are 250 Å/750 Å/100 Å/750 Å/100 Å/250 Å. This metal stack is modeled of the one used by Pang et al. [23] and is similar in nature to the one used by Gong et al. [32]. The rational for the thicknesses are as follows. First, it was known that a Ti (250 Å)/Al (1500 Å)/Ti (100 Å)/ Au (250 Å) metal stack would produce good Ohmic contacts. By keeping the Al content the same (1500 Å), and leaving the Ti barrier layer thickness the same (100 Å), it was believed that the relative ratios would remain the same as in the traditional structure with the added benefit of the additional Al/Ti layers hypothesized earlier in this chapter by Pang et al. [23].

The only difference in terms of process flow between these two Ohmic contact structures occurs during the source/drain deposition stage. The general process flow described later therefore applies to both Ohmic contact metalizations.

Chapter 3

Fabrication of AlGaN/GaN HFETs

This chapter presents the fabrication process used to create AlGaN/GaN HFETs. The HFET layer structure consists of an unintentionally doped $Al_{0.3}Ga_{0.7}N$ barrier layer of 20 nm thickness. Two different Ohmic contact metalization schemes were used in the fabrication of devices. Fabrication results and characterization of each unit step are given where applicable. Completed device photographs are provided at the end of the chapter.

3.1 Process Flow

The general process flow consists of four main stages. These are: 1) mesa isolation, 2) source/drain deposition, 3) gate deposition, and 4) pad deposition. Each stage corresponds to its own photo mask and therefore its own photolithography step. In the following sections, each unit process used in device fabrication will be described. The procedure and conditions outlined for these unit steps may or may not be unique to a particular step. For example, the lithography process for patterning the gate metal is the same as for the pad metal but both are different from the mesa isolation lithography — the details of all of which are described below. Each unit step, however, is presented in a roughly chronological order.

3.1.1 Sample Cleaning

In this fabrication process, sample cleaning consists of two major steps. The first is a solvent cleaning to remove organic compounds such as grease, oil, or dust. This is done to ensure that these contaminants are not present on the sample and therefore do not introduce defects during fabrication. The second step of cleaning is an acid bath to remove naturally occurring oxide layers. This is done to ensure that process steps occur on top of the wafer rather than on the oxide films that tend to grow naturally in the presence of sufficient temperature and oxygen.

The basic solvent cleaning must occur at the beginning of each of the four main stages of fabrication mentioned above. The solvent cleaning process consists of placing the sample in a series of solvents to remove contaminants. First, the sample is placed in a beaker of acetone for two minutes. Next, the sample is placed in isopropyl alcohol (IPA) for two minutes. Finally, the sample is placed in deionized (DI) water for two minutes and rinsed to ensure no solvents remain.

Removal of native oxide is the second step of cleaning. This may also be considered a wet etching process. The removal of native oxide needs only to occur before the deposition of the Ohmic contact metal stack. The removal of native oxide can be done with either hydrogen fluoride (HF) or hydrochloric acid (HCl). Due to the extremely volatile nature of HF and the security concerns of working in a student cleanroom, HCl was chosen. To perform the cleaning, HCl is diluted with DI water in a 1:4 ratio. The sample is then placed in the acid bath and is lightly agitated for two minutes. Mileham [35] has shown that HCl cannot effectively etch any of the the III-nitrides. This means there is essentially no way of interfering with the heterostructure by over-etching a sample in HCl.

After either the solvent cleaning or the native oxide removal steps, the sample is then dried with a nitrogen gun to remove excess water. To ensure that absolutely no water is on the sample for the remaining steps, the sample is put on a hotplate at 150 °C to evaporate any remaining water.

3.1.2 Photolithography

For the sake of this thesis we will consider photolithography to be the general process of of spin coating of photoresist (PR), ultra-violet (UV) exposure, and development. The exact steps are somewhat more complicated, however, and the complete process will be described in the subsections below. These steps are highly dependent on one another and therefore merit being considered together under the umbrella term photolithography.

Photolithography is the use of light to define patterns on a photosensitive material, (i.e. PR). The patterns on the PR cover the sample such that additive (i.e. deposition of metal) or subtractive (i.e. etching) processes can act on the exposed surface of the sample. Thus the features defined by the mask are transfered first to the resist, then to the sample. In understanding photolithography, it is essential to discuss exposure in general. Figure 3.1 provides a basic overview of the process.

There are two factors affecting the shape of the features transferred to the PR film. The first is the mask. This is quite obvious. If the desired image is a cross, we can represent that cross either as a nontransparent film of chromium on the quartz mask or, complementary to that, as the absence of chromium such that everything on the mask is covered in chromium except the desired cross which is left as transparent quartz. This is depicted in Figure 3.2. These are called clear and dark field masks, respectively. The other factor that can invert an image is the polarity of the PR. This is less obvious. Based on the chemistry of the PR or on the process of exposure/baking of that photoresist, a PR can be a positive or negative in polarity. In a positive PR, parts of the photoresist exposed to light will become soluble, which can then be removed in a bath of developer. The inverse is true with a negative photoresist. This basic process is shown in Figure 3.1.

These photolithography basics are essential to understanding the two different types of photolithography used in this fabrication process. The first type is a traditional or non-image reversal (non-IR) technique. The second is image reversal (IR). The two techniques are described in the subsections below.

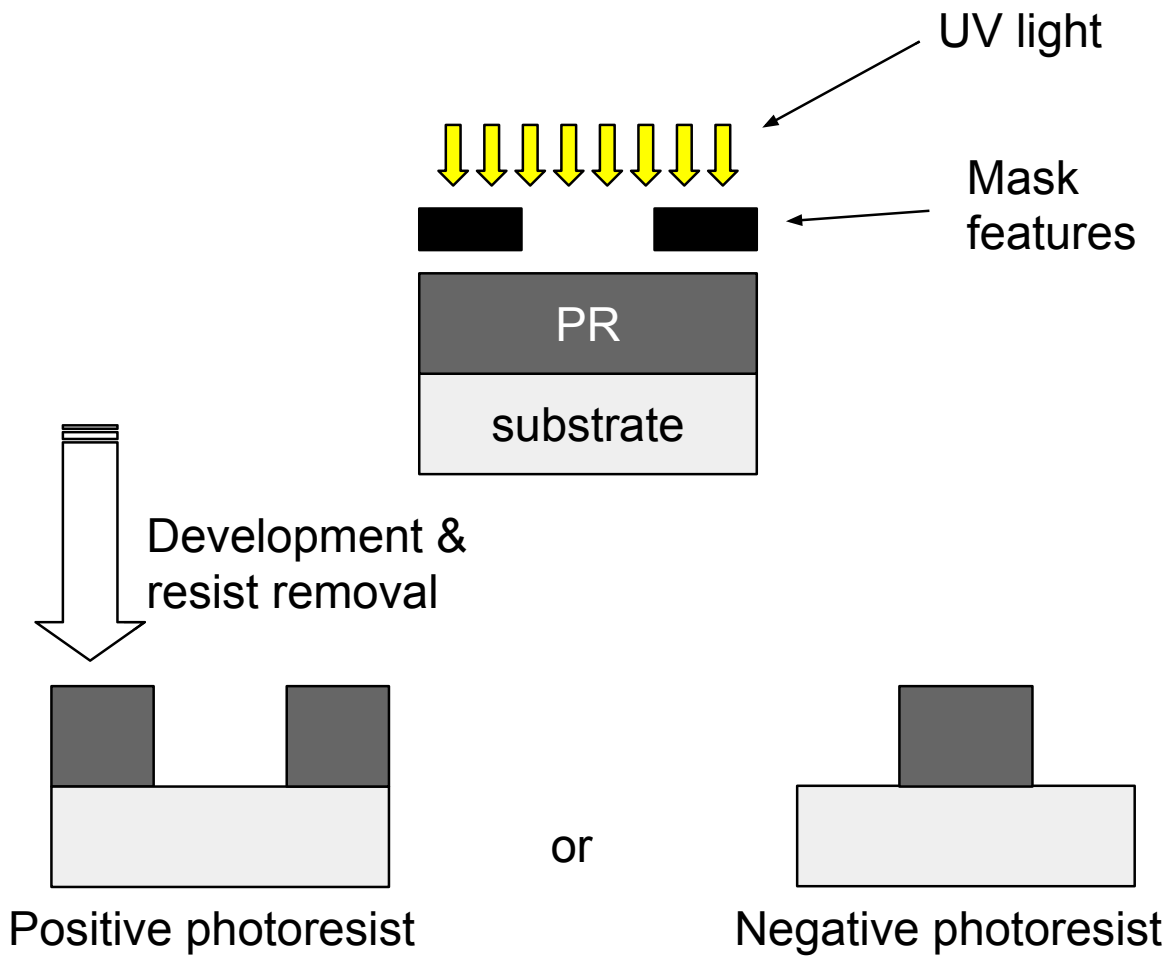


Figure 3.1: Basic photolithography steps. With a positive photoresist, those parts of the photoresist that were not exposed to light remain on the wafer after development. The opposite is true for a negative photoresist.

Non-Image Reversal

The specific steps of the non-image reversal photolithography consist of (1) dehydration of the sample, (2) application of an adherence promoter, (3) spin coating of a PR, (4) softbake of that PR, (5) exposure of the sample to UV light, (6) development of the PR, and, (7) hardbake. The above steps are implemented as follows. Given that photolithography occurs after cleaning of the sample, the first step of dehydration can be considered the final step of cleaning. In step (2), hexamethyldisilazane (HMDS) is spin-coated on the sample and is used as an adherence promoter to help the PR properly stick to the sample. HMDS also allows for a more uniform thickness

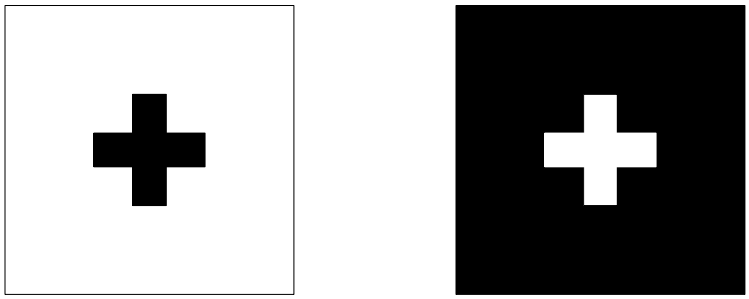


Figure 3.2: Example of a clear field mask (a) versus a dark field mask (b). The dark areas are those covered with chromium.

of PR on the sample and helps deposited metals to adhere to the sample during liftoff [36]. The HMDS is spin coated at 4000 rpm and then baked at 100 °C for 60 s. Next, Shipley 1813 positive polarity photoresist is spin coated at 4000 rpm and softbaked at 115 °C for 60 s. The sample is then exposed to near UV light (350–450 nm) following the non-IR exposure recipe shown in Table 3.1. The sample is developed in MF319 developer for 30 s and then hardbaked at 90 °C for 90 s. Hardbake protects the photoresist against future energetic processes to ensure proper masking of the substrate [36]. These recipes have been standardized by the cleanroom staff to ensure fitness with the cleanroom tools. After this step, the photolithography is complete and the next unit process takes place. In this specific process flow, the non-image reversal technique is used only on the photolithography of the mesa isolation step.

Table 3.1: Exposure recipe details for the three different exposure processes.

	Exposure Mode	**Contact mode**	**Dose [mJ/cm^2]**	**Exposure time [s]**	**Resist thickness [µm]**	**Substrate thickness [mm]**
Non-IR	Constant dose	Soft	60	0.6	1.4	0.4
IR	Constant time	Soft	N/A	N/A	1.4	0.5
Flood	Constant dose	None	250	N/A	1.5	0.5

Image Reversal

As discussed above, there are two aspects that can invert an image — that is, the image realized on PR on a sample. In the design of the masks used in this fabrication process, for the additive steps (source/drain deposition, gate deposition, and pad deposition) the masks are clear field. This means that for these three layers, seemingly a negative photoresist is needed.

Another way to implement these steps is to use a process called image reversal by employing a so-called image reversal PR. An image reversal PR does not simply produce an inverse image of a positive photoresist but also has the additional benefit of producing what are known as negative sidewalls. These negative sidewalls aid in metal liftoff as will be described later. Hence, throughout this recipe the IR process is adopted. The particular image reversal photoresist used is AZ 5214E from Clariant. AZ 5214 is in fact a positive photoresist that can be used as such [37]. Using this PR, only through a second exposure called a "flood exposure" can we get the resist to behave in the manner of a negative photoresist. During flood exposure no mask is employed.

The specific process steps for the image reversal photolithography are implemented as follows: (1) dehydration of the sample, (2) application of HMDS, (3) spin coating of the PR, (4) softbake, (5) IR exposure, (6) postbake, (7) flood exposure, and (8) development. Steps (1–2) are the same as in the non-IR photolithography. In step (3) AZ 5214 resist is spin coated at 3000 rpm and in step 4 it is softbaked at 90 °C for 55 s. The non-IR exposure recipe details can be found in Table 3.1. Postbake is done at 105 °C for 120 s. Flood exposure details are also in Table 3.1. Development is done with AZ 726 developer for 15 s.

The images presented in Figure 3.1 are not entirely accurate. With positive photoresist, there is a positive sidewall slope of approximately 80° due to the bulk effect [37]. The bulk effect is when the photoactive compound of the PR attenuates the light traveling through the resist layer [37]. The intensity of the light thus decreases as depth increases, creating a triangular exposure cross section. Figure 3.4 shows what this negative sidewall slope looks like. When image reversal is used, this effect is reversed because the parts of the resist exposed to light in the initial exposure are ultimately hardened and remain on the substrate while the unexposed resist exhibits the positive sidewall as

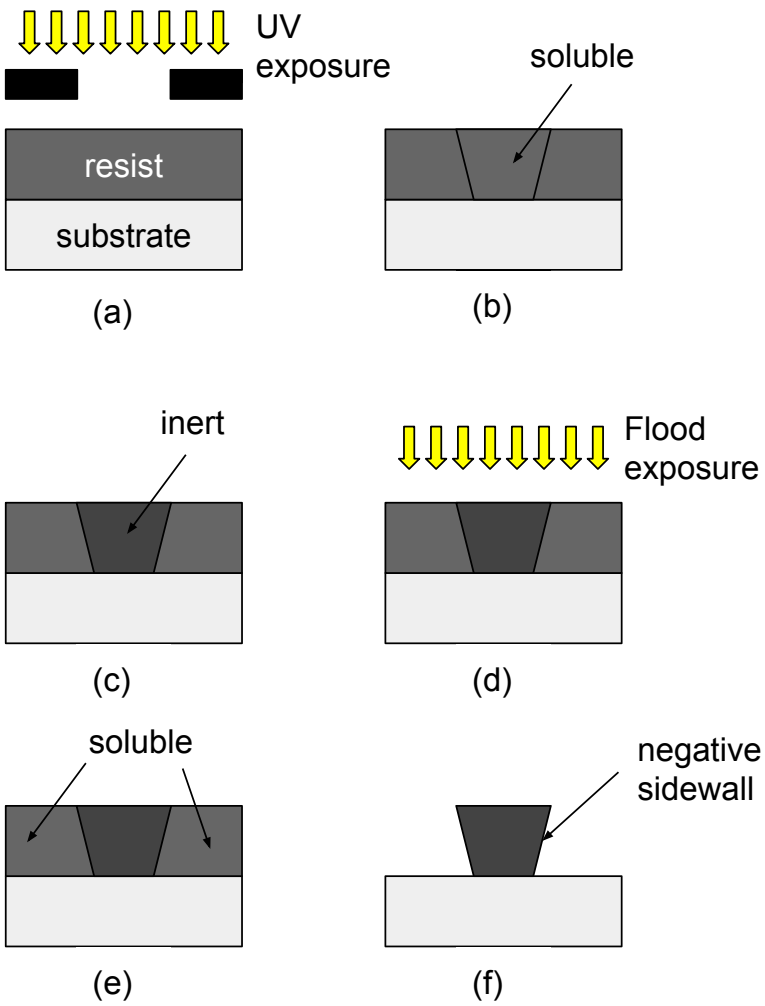


Figure 3.3: Image reversal lithography process [38]. In (a) the sample is exposed to light and patterns are defined via the mask. In (b), PR exposed to light is left soluble. After postbake, the exposed area is inert to future development as seen in (c). After flood exposure in subfigure (d), non-exposed areas are made soluble to developer. Finally, after development, reverse sidewall is present (f).

shown in Figure 3.3.

Image reversal resist produces a better resist profile for liftoff because of the negative sidewalls. This is seen clearly in Figure 3.4. When a metal is deposited onto a sample partially covered with a positive photoresist, the positive sidewall causes metal to adhere to the vertical portion of resist. In the case of an image reversal PR, the PR sidewall presents a protrusion. In this way, the PR sidewalls are shielded from the deposited metal. Ideally, this means that when the resist is stripped with acetone, the acetone can directly contact the exposed sidewall resist and dissolve the resist

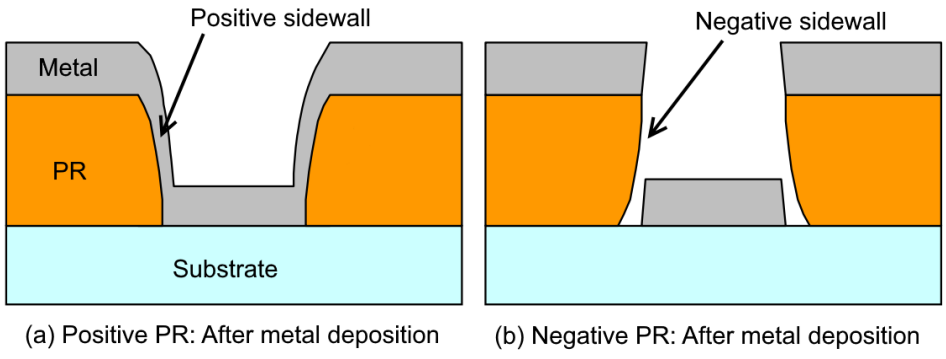


Figure 3.4: Positive sidewalls of a positive PR (a) compared to the negative sidewalls of a negative PR (b) [38]. When depositing a metal, the negative sidewalls are preferred as the PR sidewall is exposed to acetone during liftoff, allowing for easier removal of the PR.

under the metal, yielding a more successful lift-off. More realistically, in the presence of a metal covered sidewall these aforementioned protrusions allow for an easier breaking of the metal at these places where it is thin through the liftoff process. In the case of a positive PR, it is possible that conformal metal coverage prevents the breakage of the metal covering the PR from the metal adhering to the exposed surface and results in failure of the liftoff process.

An EVG620 contact aligner was used for alignment during optical photolithography. Alignment is a critical process step in ensuring functioning devices. This is because the distance between the gate and the source/drain metal is so small it approaches the tolerance of the manual adjustment of the aligner.

Figure 3.5 shows the mask layout from the GDS file. According to the mask file, the gate length is 1 µm, the distance between the gate and drain is $L_{GD} = 3\,\mu\text{m}$, and the distance between the gate and source is $L_{GS} = 2\,\mu\text{m}$. This implies that there is a 2 µm tolerance in the x-direction.

There is an additional problem which makes alignment more difficult. This is the lateral diffusion of source/drain metal after rapid thermal annealing (RTA). Figure 3.6 shows the measured gate length as well as the source/drain pad spacing. Compared to Figure 3.5, we can see that the gate finger has significantly less space than as defined on the mask. The most probable culprit is the lateral diffusion of the Ohmic contacts. As seen in Chapter 1, the RTA process can cause this metal to diffuse laterally. This would explain why the gate finger appears to have so little room.

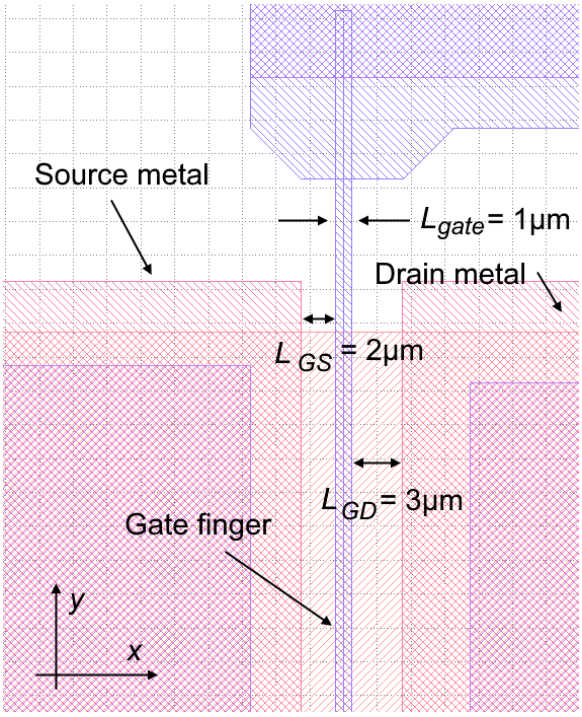


Figure 3.5: Mask layout file showing gate finger spacing. The gate finger length is $L_{gate} = 1\,\mu m$, $L_{GS} = 2\,\mu m$, and $L_{GD} = 3\,\mu m$.

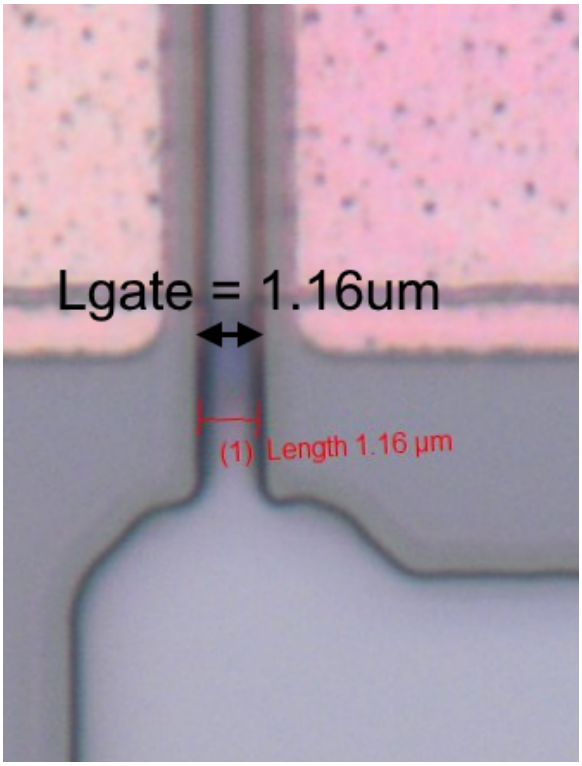


Figure 3.6: Measured gate width post development

Confirming this speculation, it should be highlighted that the choice of Ti/Al/Ti/Au metalization in this work has the worst lateral diffusion performance among the alloyed contacts to AlGaN/GaN heterostructures [12]. Because the gate finger measures roughly the expected 1 µm, this points to the lateral diffusion of the ohmic metal.

3.1.3 Deep Reactive-Ion Etching

Deep reactive-ion etching (DRIE) is required only for the mesa isolation step. In AlGaN/GaN HFETs, mesas serve to isolate individual transistors from one another and greatly reduce leakage and crosstalk by physically disconnecting the 2DEGs of adjacent transistors.

DRIE is performed in an Applied Materials P5000 cluster tool. To utilize the tool, the sample is adhered to a carrier wafer by heating wax and applying it to the underside of the sample and top of the carrier wafer. This is necessary as the tool only accepts 150 mm wafers. The carrier wafer is then placed in a magnetically-enhanced reactive-ion etch (MERIE) chamber. The etch recipe is then run on the wafer in the chamber. The etch recipe is shown in Table 3.2. The first step of the

Table 3.2: DRIE recipe steps.

Step	Cl_2 flow (sccm)	Ar flow (sccm)	Magnetic Field (G)	Power (W)	Pressure (mtorr)	Time (s)
1) Stabilize	20	10	70	0	100	10
2) Etch	20	10	70	170	100	110
3) Ramp down	0	60	0	50	0	10

recipe serves to set and stabilize the gas flow rates and pressures. No actual etching occurs during this step. The second step is the main etch step. The etch rate is a function of the gas flow rates, magnetic field, power, and pressure. Observed etch rates can be deduced from the etch profile such as the one shown in Figure 3.7 showing the mesa height. The final step is a gradual ramp-down step that lowers gas pressure, power, and magnetic field.

After dry etching is complete, mesa height is measured. This is done using an Ambios XP200 Profiler. The profiler runs a stylus across the surface of the substrate and samples the height at

regular intervals. Figure 3.7 shows a sample measurement of mesa height. From the figure one can

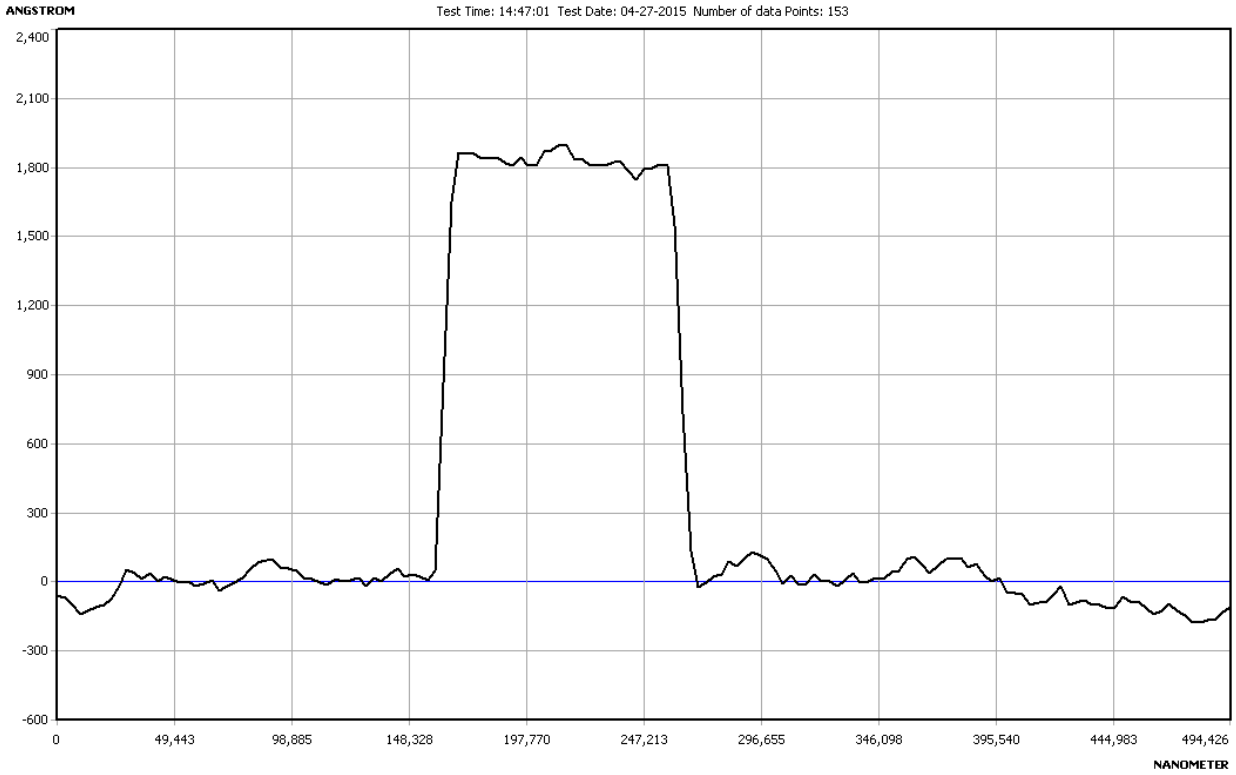


Figure 3.7: Mesa height profile.

see that the mesa height is slightly greater than 180 nm. This is a sufficient etch depth to isolate transistors because the 2DEG occurs at a depth of 20 to 25 nm from the surface. Any crosstalk from transistor to transistor would necessarily involve a leakage path deep through the GaN substrate, effectively eliminating any crosstalk between transistors.

3.1.4 Metalization and Lift-off

Metalization is required after all lithography steps except mesa isolation. Metalization was performed with an Angstrom Engineering NexDep Ebeam Evaporator. Metals were deposited per the standard recipes established by the tool manufacturer and cleanroom staff. All metals are deposited at a rate of 1 Å/s. A base vacuum of at least 9×10^{-6} torr was required to obtain a consistent and high purity deposition.

Lift-off is a process by which a deposited metal is "lifted off" from surfaces where metal covers

photoresist. Through this "lifting off", the only places where metal remains on the surface of the sample are those places in which the metal directly contacted the underlying sample (be that underlying surface semiconductor, metal, or any other material not masked by the PR). This can be seen in Fig. 3.4(b). As all metals in this process are deposited on an IR photoresist, negative sidewalls are present in which the PR remains exposed (i.e. not covered by the deposited metal). By bathing the sample in acetone, the acetone-soluble PR will be removed along with any metal that was deposited on top of the PR. Thus, the PR serves as an effective mask for the deposited metal.

Lift-off was completed in an ultrasonic acetone bath for approximately 5 min. For lift-off of the gate, ultrasonic strength was set to the lowest level to ensure that gate fingers remained adhered to the substrate surface and were not lifted off. For the larger feature sizes of the Ohmic contacts and pad layer, this was not a concern and ultrasonic power could be increased to achieve a faster lift-off. This ultrasonic bath helps agitate the sample and allows the acetone to disolved the PR, leaving only the desired metal adhered to the sample. As mentioned above, the image reversal technique played a critical role in allowing successful lift-off, particularly for the small feature size of the gate fingers. An image of a device after gate lift-off is shown in Figure 3.8.

3.1.5 Rapid Thermal Annealing

As indicated in Chapter 2, rapid thermal annealing (RTA) is necessary to form Ohmic contacts in AlGaN/GaN HFETs. The actual formation kinetics of the Ohmic contacts is not completely understood but it is believed that TiN, through dislocations in the barrier, can form Ohmic contacts to GaN or AlGaN [12]. To achieve this, samples must be annealed at relatively high temperatures compared to silicon technologies. Typical annealing recipes are performed at 750 °C to 950 °C. Extensive work done by Mohammed et al. [12] has compared the effect of annealing temperature on Ti/Al/Ti/Au contacts and shown that 850 °C is the optimal annealing temperature for this particular metal stack.

A JIPELEC JetFirst 200 system was used to perform the RTA. The monitoring of a typical RTA process is shown in Figure 3.9. After stabilization during the first 60 s, the temperature ramps to

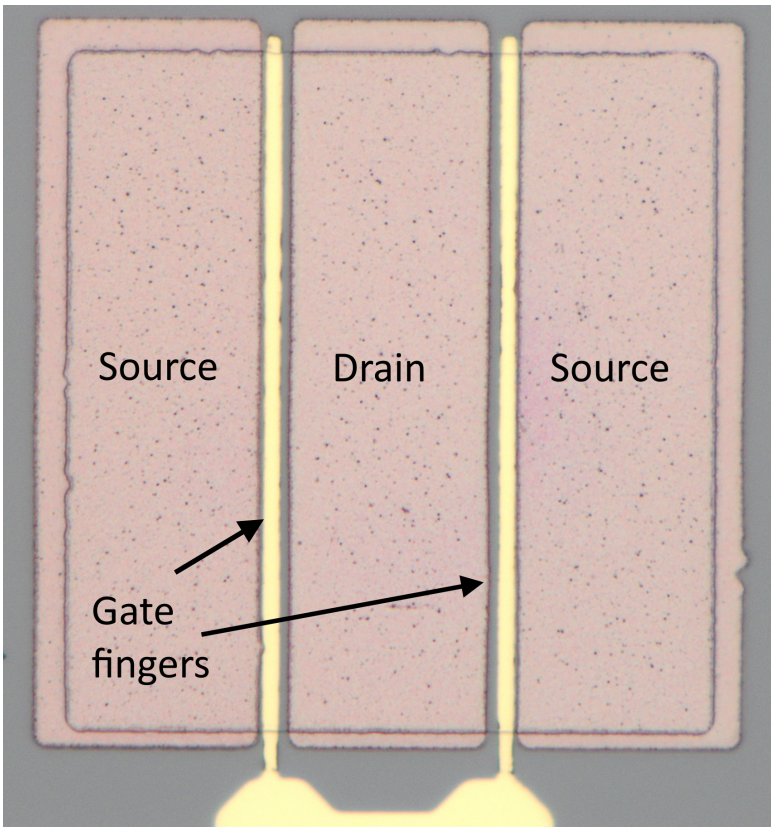


Figure 3.8: A 150 µm gate width HFET post gate lift-off. Alignment tolerances are very small and image reversal allows a successful lift-off of gate fingers which are situated in a valley surrounded by the high sidewalls of the source and drain metals.

850 °C in 5 s and remains at 850 °C for 30 s followed by a gradual ramp down. The fast ramp of the RTA recipe allows for a lower thermal budget which eliminates the negative side effects of applying too much thermal energy to the sample. This helps negate diffusion of dopants, or other effects such as reduction of piezoelectric strain or potential formation of defects due to high temperature stress on the substrate.

After RTA there is notable surface pitting and roughness of the source and drain metals. This is illustrated in Figure 3.10. According to [12], roughening becomes worse as annealing temperature is increased. Mohammed et al. also showed that there was no correlation between surface roughness and quality of Ohmic contact [12]. While surface roughness may not be correlated to the quality of Ohmic contact, it is undoubtedly correlated to the quality of the connection between measurement probes and TLM patterns. Increased temperatures or anneal times, and therefore surface roughness,

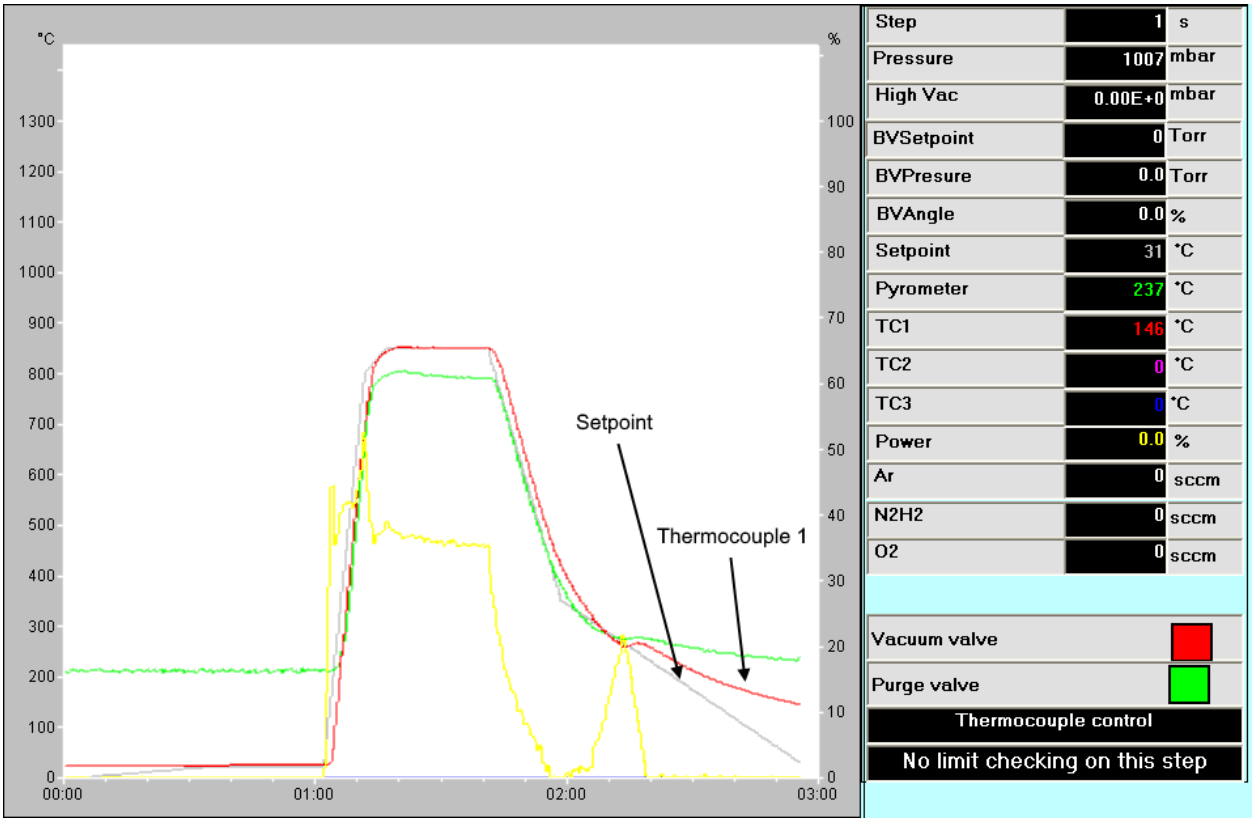
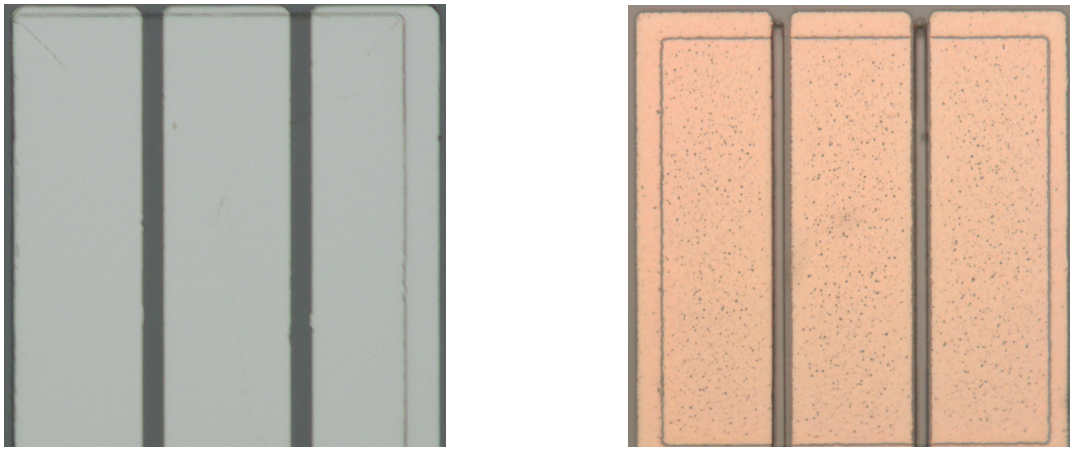


Figure 3.9: RTA process monitoring. The process recipe is controlled via thermocouple 1 (TC1) rather than by pyrometer. The setpoint and measured temperature (thermocouple 1) are indicated in the figure.



(a) Pre-RTA Ohmic surface roughness

(b) Post-RTA Ohmic surface roughness

Figure 3.10: Comparison of pre- and post-RTA surface roughness.

make it exceedingly difficult to have good contact between probe tips and TLM pads. There were multiple samples where contact resistance measurements were impossible due to poor contact

between probe tips and TLM pads. To overcome this problem, gold thickness in the Ti/Al/Ti/Au metal stack was increased by 50 Å. After this slight increase, probing TLM pads became significantly easier.

3.2 Completed Devices

Figure 3.11 shows a zoomed image of a two finger 50 µm wide device with overlays showing key structures. Source pad 1 and source pad 2 are not tied together, therefore Figure 3.11 represents two complete transistors where the gate voltage is the same for both transistors. If the source pads are tied together, the device should be able to handle twice the current, effectively becoming a 100 µm gate width device. There is another benefit to this layout. If one gate finger is misaligned, a correctly aligned second finger can still yield a working device.

Figure 3.12 shows a zoomed view of a completed six finger device. From the figure we see a very successful liftoff as well as gate alignment. The wide devices give a better sense of the angular alignment of the gate. That is, if one compares the source-gate-drain spacing at the beginning of a gate finger and follows that same spacing down the length of the gate finger, one can get a good sense of any misalignment as that error in alignment will propagate down the gate finger.

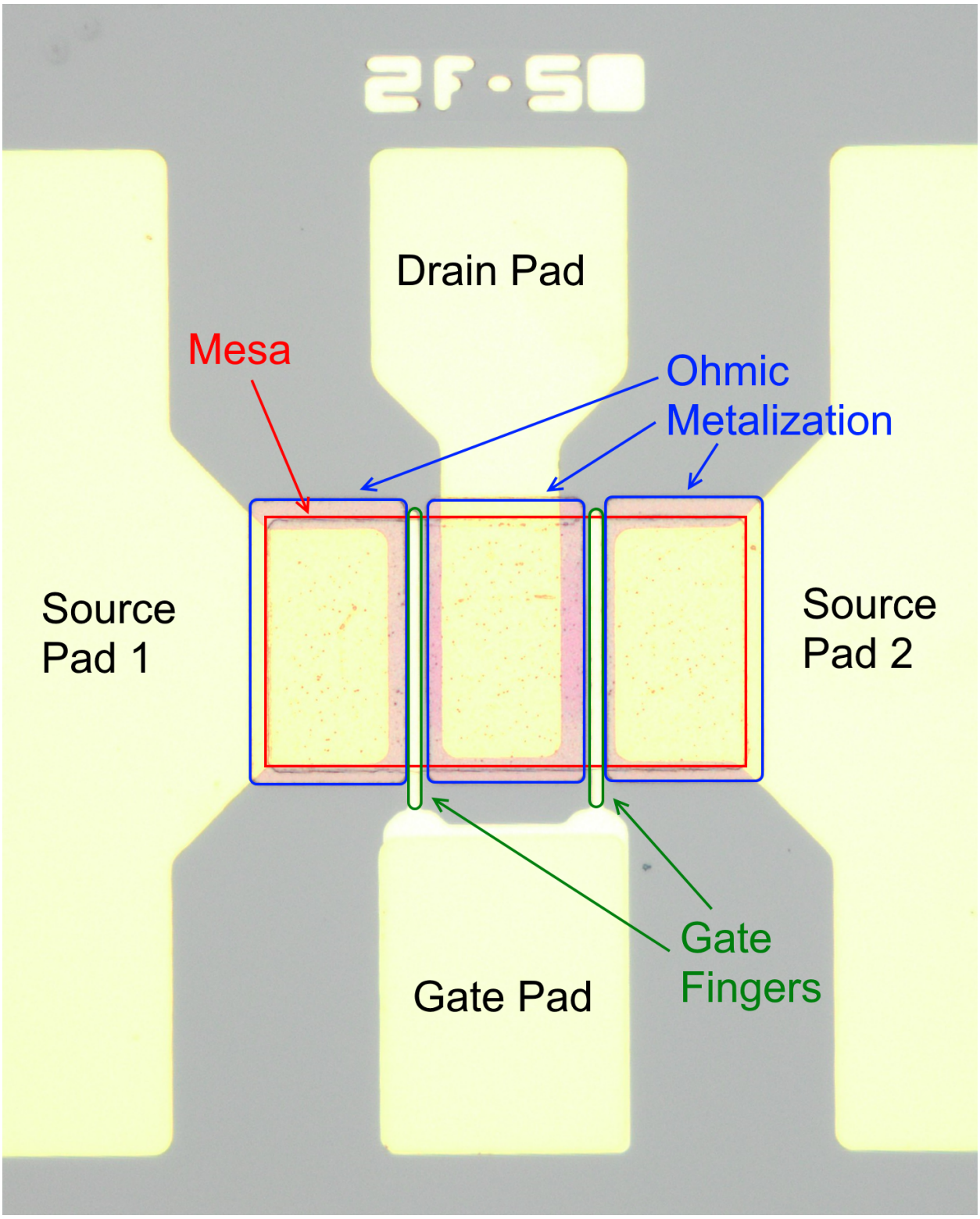


Figure 3.11: Completed fabrication of a 50 µm two finger device with overlays showing key structures.

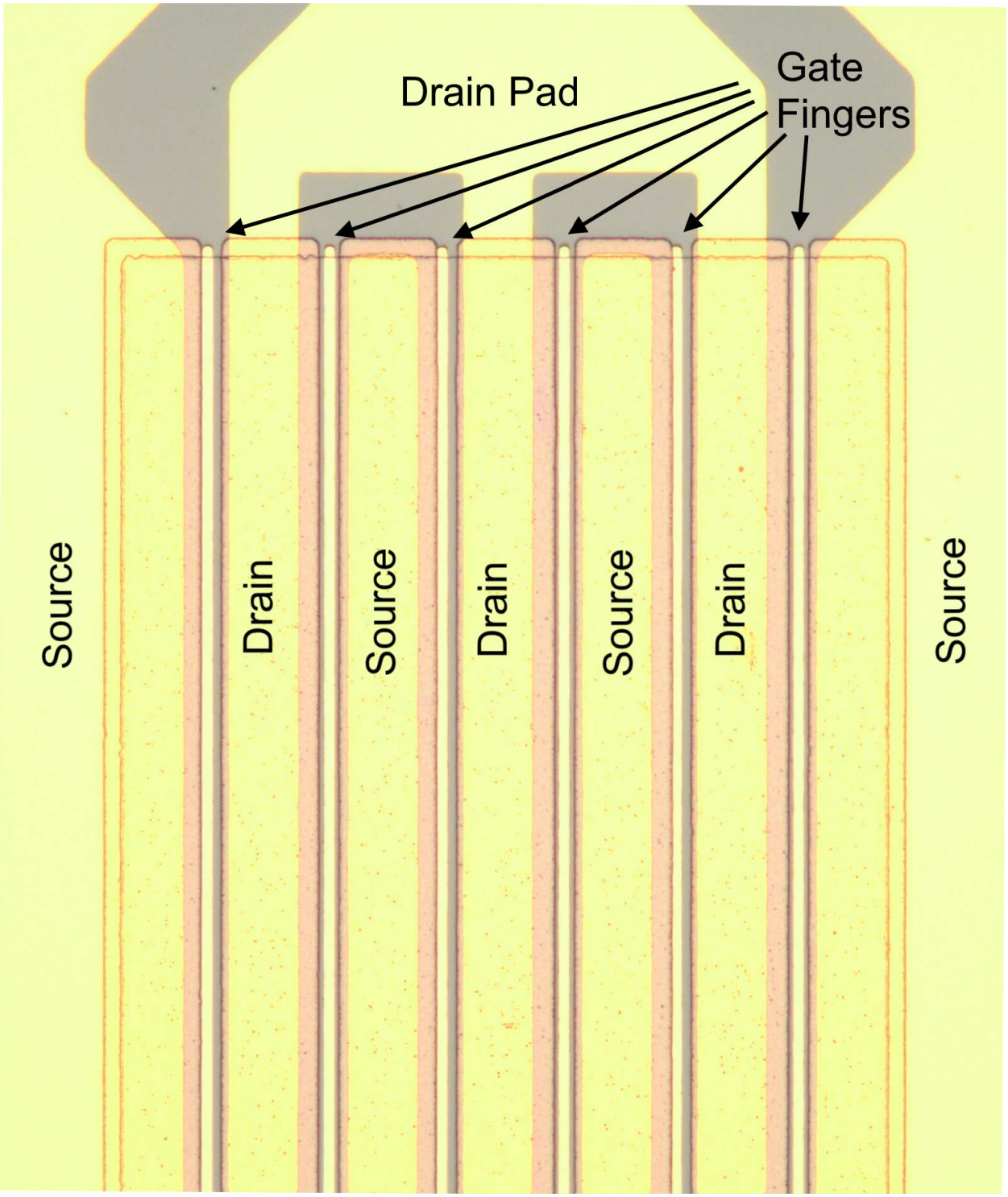


Figure 3.12: Zoomed view of a completed 150 µm six finger device. Interestingly, the right most gate finger appears to be centered to the source and drain whereas the leftmost finger appears slightly misaligned to the left. This is evidence of the sample tilting during exposure. It appears that all gate fingers have sufficient spacing from the source/drain to yield a working device. This device is still missing two fabrication steps: 1) the pillar and 2) the air bridge for connecting the middle source contacts.

Chapter 4

Characterization of Fabricated Devices

This chapter provides characterization results and analysis of the fabricated $Al_{0.3}Ga_{0.7}N$/GaN HFETs. The first section compares contact resistance results of the traditional Ti/Al/Ti/Au metalization scheme and the Ti-Al multi-layered metalization scheme. The second section deals with HFET performance metrics such as current-voltage relationships, subthreshold swing, transconductance, and gate leakage. The final section investigates the capacitance-voltage (C-V) relationship of fabricated fatFETs[1]. Based on C-V results, an analysis of carrier concentration is presented.

4.1 Contact Resistance

As seen in Chapter 2, there is great interest in improving Ohmic contacts to AlGaN/GaN HFETs. Two Ohmic contact schemes are analyzed in this section. The first is the Ti (250 Å)/Al (1500 Å)/Ti (100 Å)/Au (250 Å) metalization scheme traditionally used in AlGaN/GaN HFETs. The second is the newer Ti (250 Å)/Al (750 Å)/Ti (100 Å)/Al (750 Å)/Ti (100 Å)/Au (250 Å) multi-layered scheme.

Contact resistance measurements were carried out per the TLM methodology as described in Chapter 2. To assure the stability of these contacts with temperature, measurements were taken

[1] FatFETs are large gate length devices which are useful tools for C-V characterization in the absence of a comparable fringe capacitance which often has an overwhelming presence in FETs of small gate length.

over a range of temperatures from 170 K to 430 K using a Keithley 4200 Semiconductor Parameter Analyzer and an MRR probe station.

4.1.1 Ti/Al/Ti/Au Ohmic Metalization

Figure 4.1 shows the experimentally recorded resistance versus TLM pad spacing measured over a range of temperatures. For the Ti/Al/Ti/Au Ohmic metalization, it was not possible to record I-V curves at the 1 µm pad spacing. This is likely due to the lateral diffusion of the Ohmic metals during RTA, causing a short between the two pads.

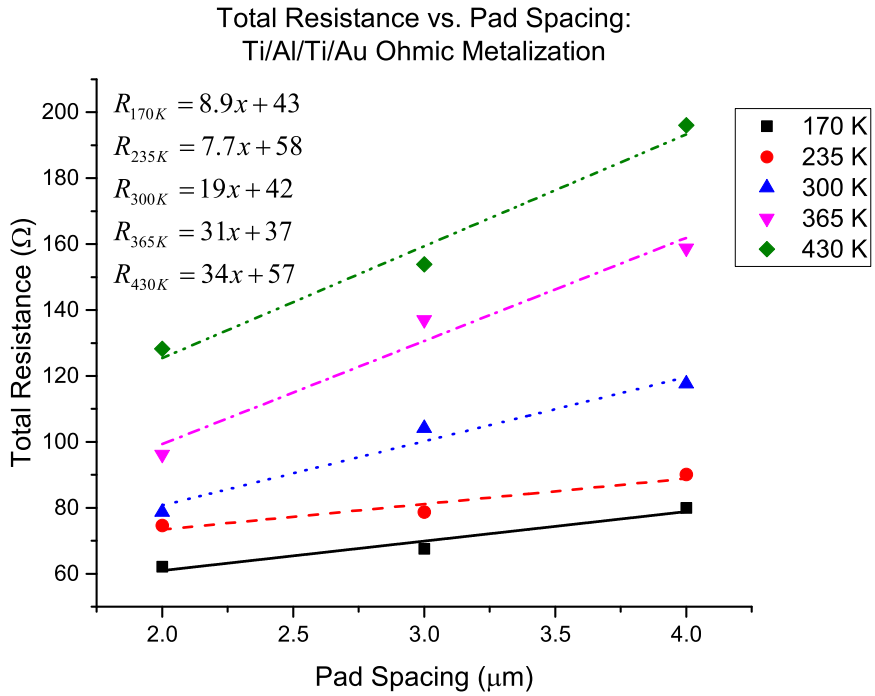


Figure 4.1: TLM Resistance vs. pad spacing over temperature for the traditional Ti/Al/Ti/Au Ohmic scheme. Trend line equations for given temperatures are indicated at the top left.

For the 300 K case, the y-intercept is $R_T = 42\,\Omega$. Using the fact that the TLM pad width is 0.143 mm, the contact resistance is calculated as $R_c = (42\,\Omega)(0.143\,\text{mm})/2 = 3\,\Omega\,\text{mm}$. Table 4.1 shows the result of these calculations for all temperatures and summarizes the contact resistance, R_c, specific contact resistivity, ρ_c, and sheet resistance, R_{sh}, values for each temperature where TLM data was recorded. From Table 4.1, one does not see a clear trend in terms of contact resistance

variation with temperature. This is partially due to the fact that there is no data from the 1 µm pad spacing.

Table 4.1: Ohmic contact summary for the Ti/Al/Ti/Au Ohmic scheme.

Temperature (K)	R_c (Ω mm)	ρ_c (Ω cm^2)	R_{sh} ($\Omega/\square$)
170	3.07	7.43×10^{-4}	1.27
235	4.15	1.56×10^{-3}	1.10
300	3.00	3.32×10^{-4}	2.72
365	2.65	1.58×10^{-4}	4.43
430	4.08	3.42×10^{-4}	4.86

4.1.2 Ti-Al Multi-layered Ohmic Metalization

The TLM measurements over temperature were repeated for the Ti-Al multi-layered metalization. The results of these measurements can be seen in Figure 4.2. In the case of the multi-layered metalization, it was possible to probe the 1 µm pad spacing.

For the 300 K case, the y-intercept is 52 Ω. The contact resistance is therefore $R_c = 52\,\Omega(0.143\,\text{mm})/2 = 3.72\,\Omega\,\text{mm}$. The specific contact resistivity is $\rho_c = 5.09 \times 10^{-4}\,\Omega\,\text{cm}^2$. The results of these calculations for all temperature ranges can be seen in Table 4.2.

Table 4.2: Ohmic contact summary for Ti-Al layered Ohmic scheme

Temperature (K)	R_c (Ω mm)	ρ_c (Ω cm^2)	R_{sh} ($\Omega/\square$)
170	3.15	4.07×10^{-4}	2.43
235	3.36	4.65×10^{-4}	2.43
300	3.72	5.09×10^{-4}	2.72
365	3.07	2.20×10^{-4}	2.72
430	2.79	1.39×10^{-4}	5.58

While the Ti/Al/Ti/Au metalization seems to present slightly better Ohmic contacts at room temperature, the reduced problem of lateral diffusion which was observed in terms of realization of TLM patterns of 1 µm pad spacing suggests that the Ti-Al multi-layer metalization is a superior choice for smaller size devices.

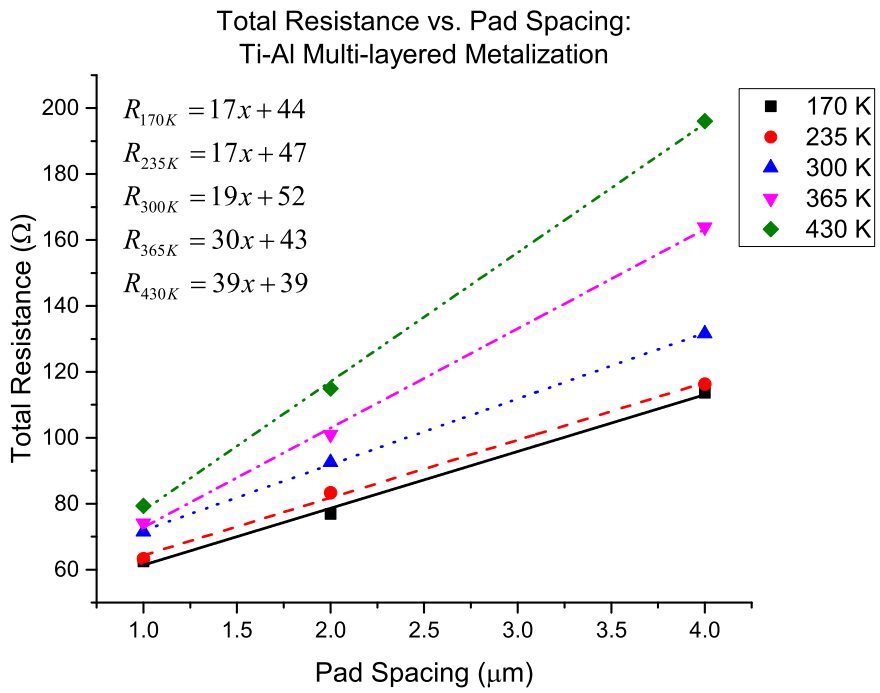


Figure 4.2: TLM Resistance vs. pad spacing over temperature for the Ti-Al multi-layered Ohmic scheme. Trend line equations for given temperatures are indicated at the top left.

From Table 4.1 and Table 4.2, we see that there is no clear trend in terms of the variation of contact resistance with temperature. To analyze this further, we can examine the specific I-V curve for the 4 μm pad spacing of the Ti-Al multi-layered TLM pattern seen in Figure 4.3.

It is interesting to note that in the case of Figure 4.3, as temperature increases, the slope of the I-V curves decreases. This means that resistance, defined as 1/slope, increases with temperature. Although for a specific TLM pad spacing, total resistance, R_T, may increase, this says nothing of the trend of contact resistance, R_c, with temperature. The variation of R_T with temperature can be explained as follows. As the temperature is increased, the crystal lattice possesses more kinetic energy and lattice vibration increases. This means that the likelihood of phonon scattering also increases. If we define μ_L as the mobility due only to lattice vibration, then, at room temperature and above

$$\mu_L \propto T^{-3/2}. \tag{4.1}$$

Therefore, any increase in temperature should result in a corresponding decrease in mobility. If not

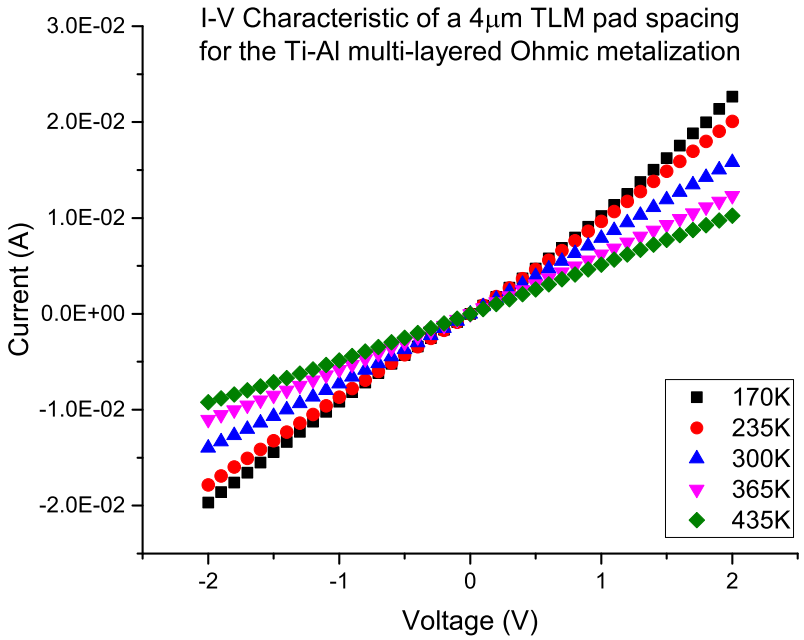


Figure 4.3: TLM current vs. voltage over temperature for the Ti-Al multi-layered Ohmic scheme. Straight lines indicate Ohmic behavior. As temperature is increased, the slope of the I-V curves drops and resistance (1/slope) increases.

offset by an opposite variation of the contact resistance with temperature, this decreased mobility will cause an increase in measured total resistance, R_T. We can assume that a counterbalancing increase in mobility defined in terms of ionized impurity scattering does not occur in the case of AlGaN/GaN heterojunctions because the GaN channel is ideally undoped and the presence of ionized impurities will be negligible. In other words, by Matthiessen's rule, total mobility will be dominated by the phonon scattering term at temperatures close to and above room temperature.

The variation of R_c with temperature is somewhat more difficult to explain analytically. At the metal-semiconductor interface, the Schottky barrier, defined by height ϕ_B, inhibits carrier flow from the metal to the 2DEG. Contact resistance depends heavily on the height and thickness of the Schottky barrier. As temperature is increased, different mechanisms of thermionic and field assisted tunneling through the barrier will play different roles.

Numerous studies have examined the effect of temperature on contact resistance to n-GaN. Lu

et al. [39] derived an expression for specific contact resistivity where tunneling is dominant as

$$\rho_c = \left[\left\{ \frac{A^* \pi q k_B T}{\sin(\pi \sigma k_B T)} \right\} \exp\left(-\frac{\phi_B}{E_{00}} \right) - \frac{A^* q}{\sigma} \exp\left(-\frac{\phi_B}{E_{00}} - \sigma \Phi_F \right) \right]^{-1} \tag{4.2}$$

where A^* is the Richardson constant, ϕ_B is the barrier height, k_B is the Boltzmann constant, T is temperature,

$$E_{00} = \frac{qh}{4\pi} \left(\frac{N_D}{m_n^* \varepsilon_S} \right) \tag{4.3}$$

and

$$\sigma = \frac{1}{2E_{00}} \ln\left(\frac{4\phi_B}{\Phi_F} \right) \tag{4.4}$$

where Φ_F is the difference in energy between the Fermi level and the conduction band edge. This model suggests that contact resistance is weakly dependent on temperature and the study found that specific contact resistivity increased slightly with temperature for Ti/Au/Pd/Au [39]. Iucolano et al. found that ρ_c decreased with temperature for Ohmic contacts to *n*-GaN from 300 to 450 K [40]. Fontsere et al. found that R_c decreased with temperature for Ti (350 Å)/Al (1550 Å) Ohmic contacts *n*-GaN from 25 to 250 °C [41]. Finally, Khanna et al. found that contact resistance of Ti/Al/W_2B/Ti/Au contacts to *n*-GaN were independent of temperature, however, the study examined a temperature range (500 to 800 °C) that was significantly higher than the other studies [42].

Relatively fewer studies have examined R_c as a function of T for Ohmic contacts to AlGaN/GaN heterojunctions. Fay et al. studied the variation of contact resistance with temperature for Ti/Al/Pd/Au Ohmic contacts to $Al_{0.25}Ga_{0.75}N$/GaN heterojunctions [43]. This study found that specific contact resistivity decreased with temperature until 200 °C and slightly increased from 200 to 300 °C [43]. At increased temperatures, thermionic field emission was believed to allow electrons to access thinner regions of the barrier to increase tunneling [43]. Fontsere et al. found that R_c slightly increased with temperature from 25 to 250 °C for AlGaN/GaN heterostructures [41].

In short, there seems to be no consensus as to the variation in contact resistance with temperature. Of course, these studies all examined different metalization schemes, different annealing conditions, different layer structures, and employed different measurement techniques. It may be the case that

for certain metal stacks, contact resistance will decrease with temperature and for other metal stacks contact resistance will increase with temperature. The work by Lu et al. in determining an analytical expression for specific contact resistivity in (4.2) is perhaps the most useful tool to this end. It is, however, very difficult to model barrier height for an alloyed metal stack with varying thicknesses of metals.

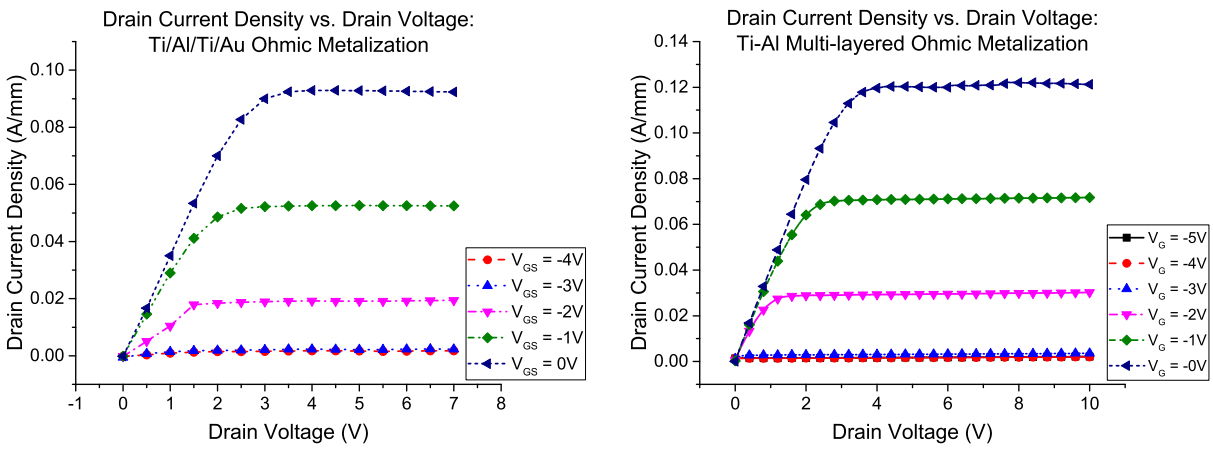
4.2 I-V Characteristics

Current-voltage (I-V) characteristics were also analyzed. Devices were measured with a Keithley 4200 Semiconductor Parameter Analyzer. Device characterization in this section is done at 300 K unless otherwise indicated.

4.2.1 Drain Current

One of the most important device characteristics is indicated by drain current versus drain-source voltage curves. Figure 4.4(a) shows the I_D-V_{DS} curves for a 100 µm gate width Ti/Al/Ti/Au HFET and Fig. 4.4(b) shows the data for a 150 µm gate width device fabricated with the Ti-Al multi-layered Ohmic scheme. The observed maximum current density is 92 mA/mm for the Ti/Al/Ti/Au Ohmic metalization and 121 mA/mm for the Ti-Al multi-layered metalization, both of which occur at a gate voltage of 0 V. Both devices exhibit good pinch-off for more negative values of gate voltage. From Fig. 4.4, the observed threshold voltage is estimated to be between −3 V to −2 V.

The observed values of drain current density are roughly one order of magnitude less than the best published AlGaN/GaN HFETs. There are several reasons which explain this relatively low value. First, published results for contact resistance shown in Table 2.2 outperform the values for contact resistance seen in Section 4.1. Increased contact resistance means it is more difficult to efficiently supply current to the drain and through the source pads. This will decrease the overall drain current density. Second, these devices are 1 µm gate length devices. This too is relatively large compared to the majority of published results. Larger gate lengths imply increased resistance and



(a) (b)

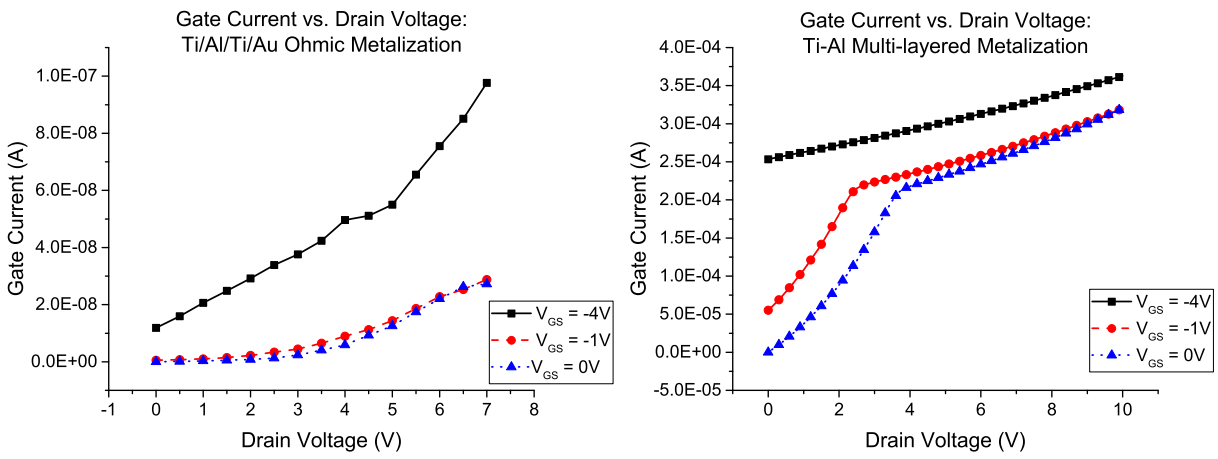
Figure 4.4: Drain current density vs. drain voltage for a 100 µm gate width HFET with the Ti/Al/Ti/Au metalization (a) compared to a 150 µm gate width HFET with the Ti-Al multi-layered metalization (b).

decreased transconductance. This decreased transconductance means a greater voltage is required to achieve the same drain current density. Finally, part of this low current density may be attributable to strain relaxation in the wafer. As wafers have been stored in an oxygen rich environment for over one year it is possible that this relaxation could cause a decrease in 2DEG carrier concentration and thereby a reduction in drain current density.

Figure 4.5 shows gate current versus drain-source voltage. For the Ti/Al/Ti/Au metalization shown in Fig. 4.5(a), at $V_{DS} = 7\,\text{V}$ and $V_{GS} = -4\,\text{V}$, the gate current is approximately 1×10^{-7} A. For the same conditions applied to the Ti-Al multi-layered Ohmic metalization of Fig. 4.5(b), the gate current is approximately 3.2×10^{-4} A. In both metalizations, gate current increases with drain voltage, as expected.

4.2.2 Subthreshold Swing

Subthreshold swing, S, is a parameter used to determine how sharply a transistor is turned off by the gate voltage [44]. It is defined as the gate voltage change required to induce a drain current change of one order of magnitude [44]. Figure 4.6 plots the subthreshold swings for both the Ti/Al/Ti/Au

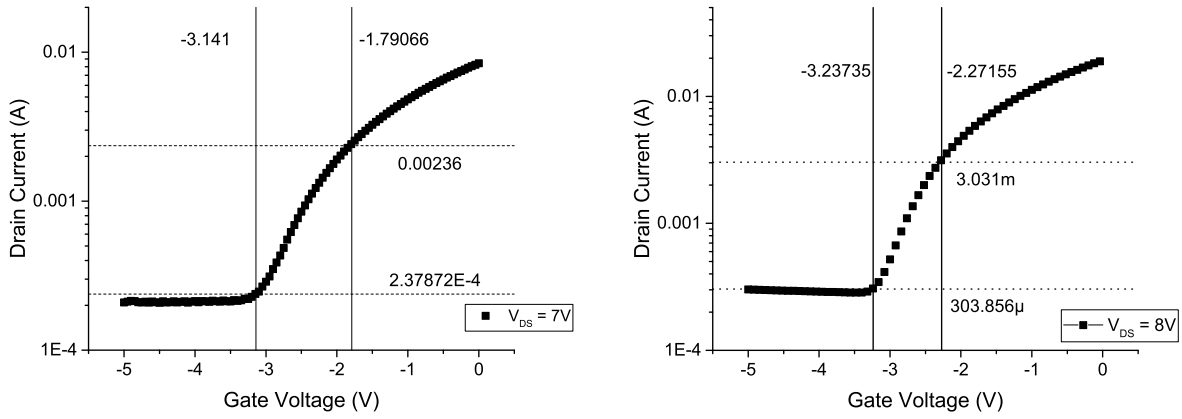


(a) (b)

Figure 4.5: Gate current vs. drain voltage for a 100 µm gate width HFET with the Ti/Al/Ti/Au metalization (a) compared to a 150 µm gate width HFET with the Ti-Al multi-layered metalization (b).

Ohmic metalization and the Ti-Al multi-layered metalization. From Figure 4.6, one can calculate the subthreshold swing to be $S = 1.35\,\mathrm{V/dec}$ and $S = 0.95\,\mathrm{V/dec}$ for the Ti/Al/Ti/Au metalization and Ti-Al multi-layered metalization, respectively. Smaller values of S are better as they indicate that less applied voltage is required to achieve one order of magnitude change in drain current. The Ti-Al multi-layered metalization therefore outperforms the Ti/Al/Ti/Au metalization in terms of subthreshold swing.

Work has been done by Chung et al. showing that there is a direct relationship between gate leakage and subthreshold swing [45]. This makes sense intuitively. A leakier gate implies that charge that could be used to control the channel is tunneling to a different location, thereby requiring a greater voltage to be applied to the gate in order to achieve the same control of the channel that would otherwise be achieved. Specifically, Chung et al. found that reducing vertical tunneling from the gate to the 2DEG by increasing barrier layer thickness and reducing trap assisted tunneling by passivating the gate surface before metalization improved subthreshold swing from 176 mV/dec to 64 mV/dec [45]. We will see that the relatively high gate leakage shown in Section 4.2.4 could be hindering the subthreshold swing.



(a) (b)

Figure 4.6: Subthreshold swing for a 100 µm gate width HFET with the Ti/Al/Ti/Au metalization (a) compared to a 150 µm gate width HFET with the Ti-Al multi-layered metalization (b).

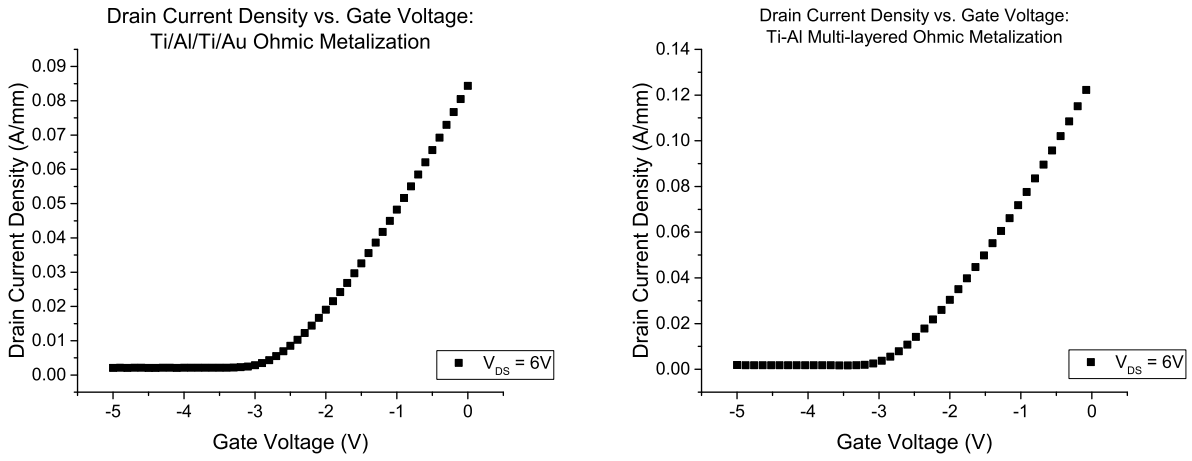
4.2.3 Transfer Characteristics

Device transfer characteristics describe the drain current to gate voltage relationship. Figure 4.7 plots this relationship for $V_{DS} = 6\,\text{V}$ for both Ohmic metalization schemes. From Figure 4.7 we can see that for both Ohmic metalizations, the transistors have a threshold voltage slightly more positive than $-3\,\text{V}$. The observed drain current density at $V_{GS} = 0\,\text{V}$ for the Ti/Al/Ti/Au metalization seen in Fig. 4.7(a) is 0.09 A/mm while under the same conditions, the Ti-Al multi-layered metalization achieves a drain current density of 0.13 A/mm. This amounts to a 44% improvement in drain current density for the Ti-Al multi-layer metalization.

Gate transconductance is another useful transfer characteristic. Gate transconductance is a measure of a transistor's gain. It is defined as

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}. \tag{4.5}$$

It represents a transistor's ability to convert gate voltage to an output drain current. Higher values indicate better ability to amplify voltage. Figure 4.8 shows the transconductance of the two aforementioned devices for given values of V_{DS}. The Ti/Al/Ti/Au and the multi-layered metalization



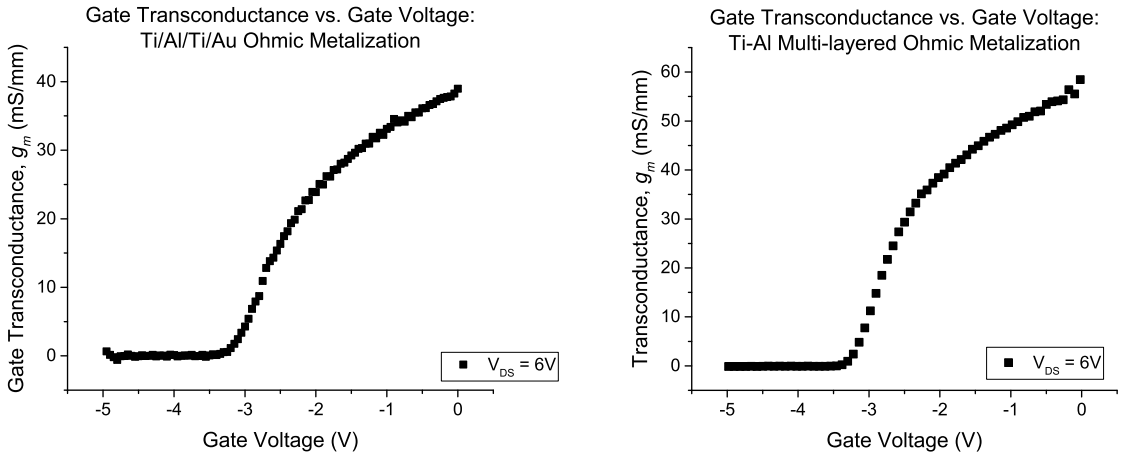
(a) (b)

Figure 4.7: Gate current vs. drain voltage for a 100 µm gate width HFET with the Ti/Al/Ti/Au metalization (a) compared to a 150 µm gate width HFET with the Ti-Al Multi-layered metalization (b).

schemes offer a maximum transconductance of 40 and 60 mS/mm, respectively. The majority of published results typically provide values of transconductance around 200 mS/mm. Obviously drain current density and transconductance are related. This relatively low value of transconductance is also due to strain relaxation and the longer gate.

4.2.4 Off-state Gate Leakage

Off-state gate leakage was measured by biasing the drain at 0 V to ensure the device is in an off-state and sweeping over a range of negative gate voltages. This was done over a range of temperatures to determine the change in gate leakage with temperature. Results of these measurements are shown in Figure 4.9. As further highlighted for the case of the multi-layered Ohmic metalization scheme in Figure 4.10, we see a maximum gate leakage of 3.5 mA at 425 K and $V_{GS} = -6$ V. There is a clear trend with temperature. Leakage tends to increase with increasing temperature. This is because the chance of direct leakage processes such as field emission increases with temperature. As electrons obtain more kinetic energy, it is easier for them to travel over the Schottky barrier gate, thereby increasing leakage.



(a) (b)

Figure 4.8: Gate transconductance for a 100 µm gate width HFET with the Ti/Al/Ti/Au metalization (a) compared to a 150 µm gate width HFET with the Ti-Al Multi-layered metalization (b).

As shown in Figure 4.10, or smaller magnitudes of V_{GS}, gate leakage is less dependent on temperature, although there still remains a small dependence. As the magnitude of V_{GS} increases, temperature dependence becomes more significant. This is due to the more dominant role of the temperature-independent field-emission process in comparison to the thermionic emission process at gate voltages well above the threshold.

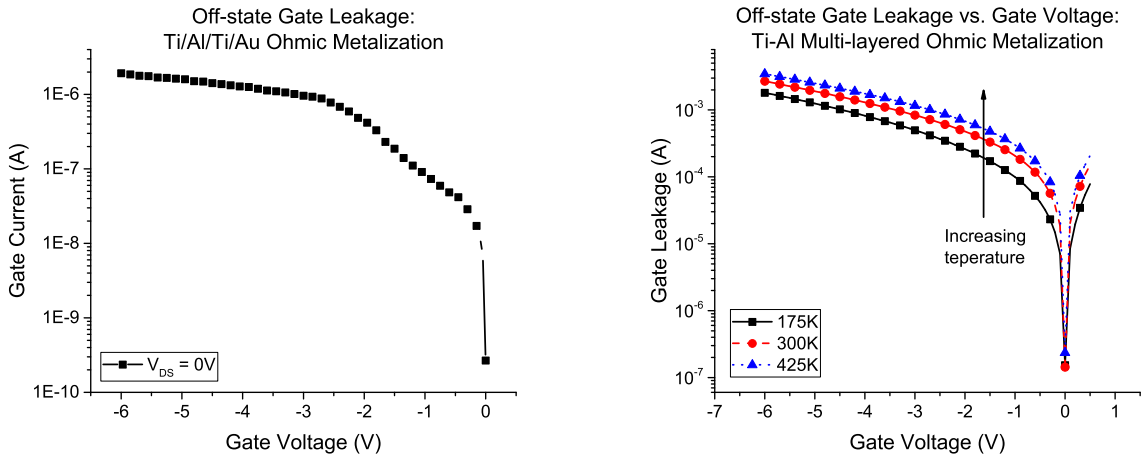
4.3 C-V Profiling

Capacitance-voltage (C-V) profiling is a useful technique which can be used to analyze semiconductor properties such as carrier concentration. C-V profiling is done on characterization devices called fatFETs. FatFETs are so called because of their large gate fingers that allow for easy C-V profiling in the absence of substantial fringing.

The theoretical capacitance of a parallel plate capacitor formed by an $Al_xGa_{1-x}N$/GaN fatFET is

$$C = \frac{\varepsilon_r \varepsilon_0 A}{d} \tag{4.6}$$

where ε_r is the relative permittivity of the AlGaN layer, ε_0 is the permittivity of free space, A is the



(a) (b)

Figure 4.9: Off-state gate leakage for a 100 µm gate width HFET with the Ti/Al/Ti/Au metalization at $T = 300\,\mathrm{K}$ (a) compared to a 150 µm gate width HFET with the Ti-Al multi-layered metalization (b).

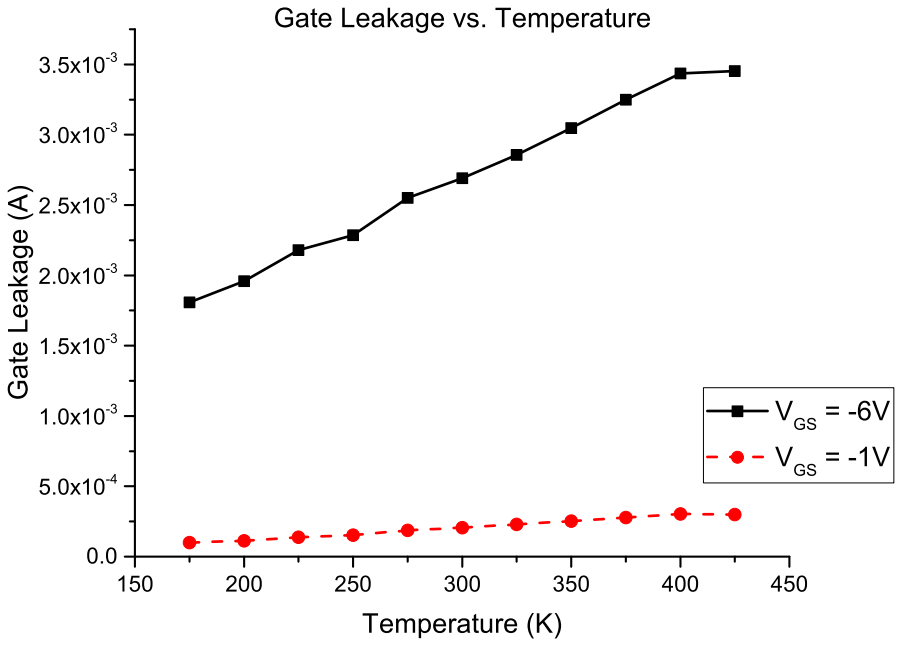


Figure 4.10: Gate leakage vs. temperature for values of $V_{GS} = -6\,\mathrm{V}$ and $V_{GS} = -1\,\mathrm{V}$. The device measured is a 150 µm gate width device.

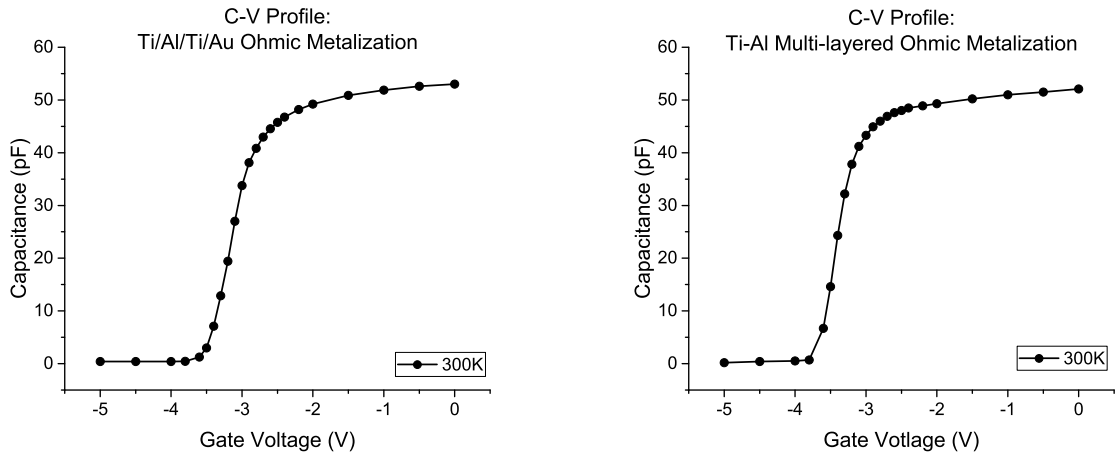
area of the FatFET gate, and d is the effective thickness of the AlGaN layer, defined by summing the physical thickness of the layer and the distance between the charge centroid of the 2DEG and

the heterointerface. The relative permittivity of the AlGaN layer is calculated as [4]

$$\varepsilon_r = 10.4 - 0.3x. \tag{4.7}$$

Given the FatFET dimensions of 50 µm by 161 µm, an AlGaN thickness of 20 nm plus a typical separation between the charge centroid and heterointerface of 5 nm, and the permittivity of free space of 8.85×10^{-14} F/cm one can solve for the capacitance as 58.8 pF. Hence, assuming the 2DEG acts as a perfect conductor, one can expect a maximum capacitance during C-V profiling of 58.8 pF.

C-V profiling was carried out on various fatFET devices. To perform the measurements, one probe was placed on the gate of the fatFET while a second probe was placed on the source. An AC signal at 10 kHz was applied to the gate and the resulting capacitance was measured with an HP 4284A LCR meter. This was done over a range of DC bias voltages applied to the gate from −5 to 0 V. C-V measurements were taken for both the Ti/Al/Ti/Au and Ti-Al multi-layered metalizations. Figure 4.11 shows the results of these measurements at 300 K. For both metalization schemes,



(a) (b)

Figure 4.11: C-V profiles of the Ti/Al/Ti/Au Ohmic metalization (a) compared to the Ti-Al multi-layered metalization (b). Both measurements were performed at a frequency of 10 kHz.

the threshold voltage of the fatFET occurs at −3.5 V and the maximum capacitance is 55 pF. It is expected that the quality of the Ohmic metalization scheme plays no significant role in the formation

of the 2DEG under these test conditions or that the Ohmic contacts affect the carrier concentration of the 2DEG. This is confirmed by the similarity in the C-V profiles between the two metalization schemes.

In order to determine the measurement uncertainty in the setup and test equipment, a single fatFET was tested multiple times at room temperature. These results were averaged and are plotted in Figure 4.12. The error bars in the figure represent the minimum and maximum measured capacitances at a given gate voltage. In the sharp transition period between −3.5 and −2.5 V V_{GS}, the

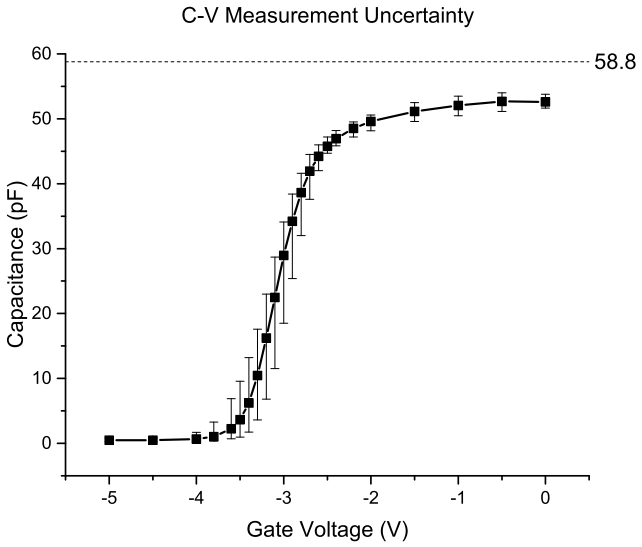


Figure 4.12: C-V measurement error and comparison to expected value. Measurements taken at 10 kHz on a Ti-Al multi-layer Ohmic fatFET at room temperature.

observed uncertainty is greatest. Also, in order to determine if any hysteresis effects were present, this fatFET was tested from −5 V to 0 V V_{GS} and then from 0 to −5 V. It was observed that any hysteresis effects were smaller than the measurement uncertainty shown in Figure 4.12.

As mentioned above, C-V profiling allows for indirect measurement of carrier concentration. To calculate carrier concentration, N_{C-V}, one can use the expression [4]

$$N_{C-V} = \frac{C^3}{q\varepsilon_0\varepsilon_r}\frac{\mathrm{d}V}{\mathrm{d}C} \tag{4.8}$$

where depth into the AlGaN barrier layer is defined as [4]

$$z_{C-V} = \frac{\varepsilon_0 \varepsilon_r}{C}. \tag{4.9}$$

Here, ε_0 is the permittivity of free space, ε_r is the relative permittivity of the barrier layer, C is the measured capacitance per unit area, and q is the charge of an electron. This allows one to determine the carrier concentration at different depths within the semiconductor. This is particularly useful for the characterization of doping profiles in devices such as modulation doped field effect transistors. Kroemer et al. [46] have shown that charge conservation is fulfilled for C-V profiles meaning that it is possible to determine the sheet carrier concentration, n_s, as

$$n_s = \int_{-\infty}^{\infty} N_{C-V}(z_{C-V})\,\mathrm{d}z_{C-V} = \int_{-\infty}^{\infty} n(z)\,\mathrm{d}z. \tag{4.10}$$

We can use this technique to determine the concentration of the 2DEG. Results of this analysis is presented in Figure 4.13. The results of Figure 4.13 show a peak carrier concentration at roughly

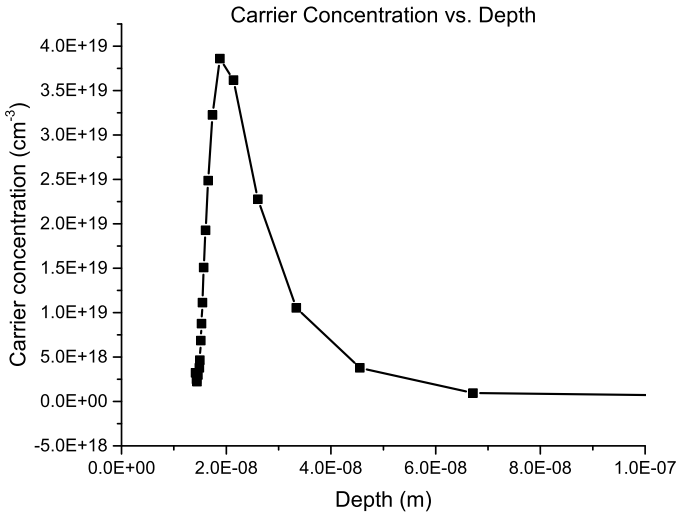


Figure 4.13: Carrier concentration as a function of depth. C-V data in the above figure is from average values of a Ti-Al multi-layered Ohmic fatFET.

20 nm. This fits very well with the actual device geometry. As noted before, the AlGaN thickness is

20 nm so one should expect to see the highest carrier concentration to occur near the heterojunction at a depth of 20 nm.

We can also use (4.10) to plot the sheet carrier concentration, n_s, as a function of depth, z, into the AlGaN barrier layer. Results of these calculations are shown in Figure 4.14. The observed peak sheet carrier concentration is $n_s = 6.7 \times 10^{11}\,\mathrm{cm}^{-2}$. This is about an order of magnitude smaller than the size of the 2DEG expected from such a layer structure, hence supporting our earlier speculation of strain relaxation in the wafers used in these studies.

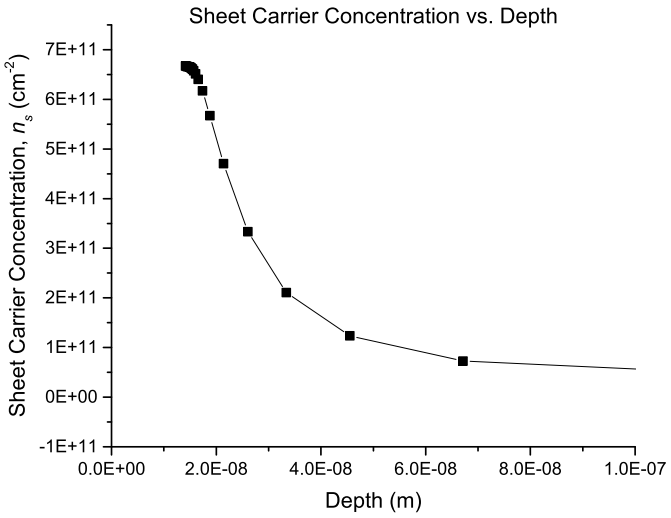


Figure 4.14: Sheet carrier concentration as a function of depth.

Chapter 5

Simulation of Gate Leakage

Gate leakage is a critical aspect of AlGaN/GaN HFET performance that is not yet fully understood. Inital work on gate leakage mechanisms by Miller et al. [47] suggested that vertical tunneling through the gate was the dominant component of leakage current. However, the same study also concluded that other mechanisms were present such as surface leakage. More recent work [48, 49] has suggested a plethora of other leakage mechanisms such as sidewall leakage may be present. The reality of gate leakage is complex and likely depends heavily on material parameters, layout, and fabrication techniques.

Better understanding of gate leakage could lead to significantly lower leakage currents and therefore yield better overall device performance. Mizuno et al. [50] has shown that $Al_{0.3}Ga_{0.7}N$/GaN HFETs have reverse gate leakage roughly two orders of magnitude higher than $Al_{0.3}Ga_{0.7}As$/GaAs HFETs. This suggests much room for improvement with AlGaN/GaN. Reducing this off-state current will yield lower noise and lower power consumption [47]. A more complete picture of gate leakage mechanisms will provide better understanding and ultimately new designs and fabrication techniques to help reduce the high off-state leakage in AlGaN/GaN HFETs.

There are a variety of leakage mechanisms which have been proposed so far. As mentioned above, Miller et al. provided some of the first work examining gate leakage in AlGaN/GaN HFETs. They showed that vertical leakage through the barrier was the predominant source of total gate

leakage, however, they also noted lateral tunneling and defect assisted tunneling were present when gate-drain bias was increased [47]. Later work by Mizuno et al. [50] confirmed vertical tunneling as the main leakage mechanism and suggested thermionic emission was not significant because of the temperature independence of the I_G–V_G curves. Karmalkar et al. [48] went further than Miller in actually developing a theoretical model of defect or trap assisted tunneling. Through this they predicted that leakage was due to two general types of tunneling: direct tunneling and trap assisted tunneling. The total reverse gate leakage current is therefore

$$I_G = I_{TT} + I_{DT} \tag{5.1}$$

where I_G represents the total leakage current, I_{TT} is the current due to trap assisted tunneling, and I_{DT} is the current due to direct tunneling [48]. In their definition of direct tunneling current, I_{DT} is actually composed of two further distinct mechanisms. These are Fowler-Nordheim current, I_{DT}^{FN}, and thermionic field emission current, I_{DT}^{TFE}. I_{DT} is defined as

$$I_{DT} = I_{DT}^{FN} + I_{DT}^{TFE}. \tag{5.2}$$

Often, one of these mechanisms dominates by several orders of magnitude and I_{DT} can be modeled as $\max(I_{DT}^{FN}, I_{DT}^{TFE})$ [48]. This analysis leaves out an additional leakage mechanism due to traps: Poole-Frenckel current. Finally, Mojaver et al. [49] has expanded on the work of Karmalkar and shown that gate leakage is comprised of five different mechanisms, namely: Fowler-Nordheim, Poole-Frenkel, thermionic-field emission, trap assisted tunneling, and a newly defined leakage current that occurs at the sidewall of an isolation feature between gate and 2DEG.

While the recent work in gate leakage has provided useful insights, the effect of Al mole fraction on the gate leakage mechanisms (i.e. in addition to its effect on the threshold voltage) has not been discussed in the literature. This chapter aims to do just that. The following section will describe the four leakage mechanisms simulated in this thesis and analyze the effect on Al mole fraction on them. Threshold voltage will be found and its dependence on Al mole fraction will be analyzed.

5.1 Analytical Models of Reverse Gate Leakage Current

To better understand each individual mechanism that plays a role in gate leakage, Figure 5.1 shows a graphical representation of each mechanism.

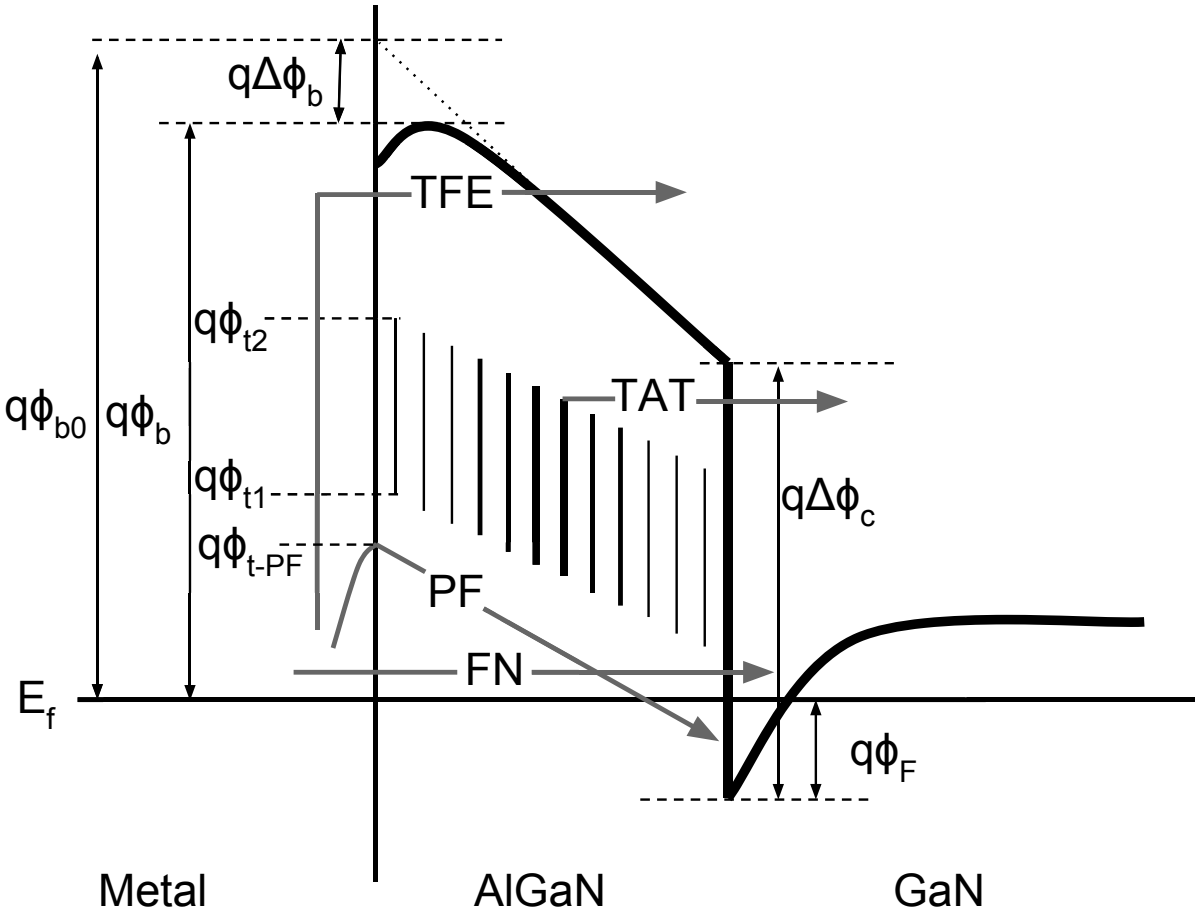


Figure 5.1: Graphical representation of the gate Schottky barrier and conduction band showing each leakage mechanism. $q\phi_{b0}$ is the Schottky barrier height not considering barrier lowering, $q\phi_b$ is the barrier height considering barrier lowering, $q\Delta\phi_b$ is the barrier height difference due to barrier lowering, $q\phi_{t2}$ is the is the upper energy level of traps in the barrier, $q\phi_{t1}$ is the lower energy level of traps in the barrier, $q\Delta\phi_c$ is the conduction band discontinuity between AlGaN and GaN, and $q\phi_F$ is the energy difference between the Fermi level and the lowest energy of the triangular quantum well.

The following subsections will provide a brief overview of the four leakage mechanisms mentioned above. Focus will be given to the physical phenomena taking place and will show via analytical expressions how each mechanism varies with critical variables such as electric field and temperature.

5.1.1 Trap Assisted Tunneling

Figure 5.1 highlights the presence of a trap band that exists in the AlGaN barrier layer. This distribution of traps plays an important role in a leakage mechanism known as trap assisted tunneling (TAT), whereby electrons tunnel from the gate to the various trap levels (depicted by vertical lines in the AlGaN barrier layer) and eventually through to the substrate. Trap assisted tunneling can occur through various multi-step and two-step processes, the most common of which is the two-step process [48]. In this section, an analytical formulation of two-step TAT current as first proposed by Karmalkar et al. is presented [48].

This analysis consists of multiple assumptions which have been spelled out by Karmalkar et al. [48]. First, this model assumes an effective electron mass, m^*, that is constant throughout the barrier layer. Second, the Wentzel-Kramers-Brillouin (WKB) approximation is used in calculating tunneling probabilities. This is the standard methodology for calculation of tunneling probabilities as it is sufficiently accurate and saves computational resources required for calculating the Schrodinger equation. Third, it is assumed that the potential barrier is triangular. This is valid as there is little change in the electric field in the region in which tunneling occurs [48]. This is equivalent to saying that the barrier electric field, E, is equal to the peak electric field at the metal/AlGaN interface. The electric field across the barrier is then [48]

$$E = \frac{V_G + V_0}{d_{AlGaN}} \tag{5.3}$$

where V_G is the applied gate bias, V_0 is the potential barrier height at the metal/AlGaN interface, and d_{AlGaN} is the thickness of the AlGaN barrier layer. V_0 is given as [48]

$$V_0 = \phi_b - \Delta\phi_c + \phi_F. \tag{5.4}$$

Here, ϕ_b is the barrier height, $\Delta\phi_c$ is the conduction band discontinuity at the AlGaN/GaN heterojunction, and ϕ_F is the difference between the Fermi level and the bottom of the conduction band,

all of which are depicted in Figure 5.1.

As depicted in Figure 5.1, the lowest energy of this trap band at the metal/AlGaN interface is defined by $q\phi_{t1}$ while the upper energy is $q\phi_{t2}$. In this two-step TAT, electrons tunnel to and from trap sites close to the band energies defined by $q\phi_{t1}$ and $q\phi_{t2}$ [48]. We define R_1 as the tunneling rate at energy $q\phi_{t1}$ and R_2 as the rate at $q\phi_{t2}$. The trap concentration is defined at N_t. In this analysis, we assume a uniform trap concentration, that is, the trap level N_t is constant throughout the AlGaN barrier.

Trap assisted tunneling consists of two different tunneling probabilities. The first is from the metal to $q\phi_{t1}$ and the second is from the trap level at $q\phi_{t2}$ to the channel. As seen in Figure 5.1, $q\phi_{t1}$ and $q\phi_{t2}$ are the trap levels at the band edges. Thus, the transition between $q\phi_{t1}$ and $q\phi_{t2}$ is considered a conductive transport similar to transport in metals. The derivation of trap assisted tunneling from [48] is as follows. First, the tunneling probabilities of the two sources of TAT are expressed as [51]

$$P_1 = \exp\left[-\frac{\alpha}{E}\left(\phi^{3/2} - (\phi_{t1} - \psi)^{3/2}\right)\right] \tag{5.5}$$

and

$$P_2 = \exp\left[-\frac{\alpha}{E}(\phi_{t2} + \psi)^{3/2}\right] \tag{5.6}$$

where

$$\alpha = \frac{8\pi\sqrt{2m^*q}}{3h}. \tag{5.7}$$

Here, ψ is the potential, E is the electric field across the barrier, m^* is the effective mass of an electron, and h is Planck's constant. A complete derivation of P_1 and P_2 is shown using the WKB approximation in [51].

For values of ψ away from the band edges ϕ_{t1} and ϕ_{t2}, the probabilities P_1 and P_2 decrease dramatically. This is seen in (5.5) and (5.6). This means that traps located near the center of the barrier are more likely to contribute to TAT current. The actual trap distribution with respect to energy can thereby be modeled by effective trap densities N_1 at ϕ_{t1} and N_2 at ϕ_{t2} (these values being analogous to the concept of effective density of states at the conductance and valence band edges,

N_C and N_V) [48]. This allows for any distribution of traps throughout the AlGaN barrier layer as only the distribution at the trap band edge is significant [48].

For the sake of simplicity, a uniform trap distribution is assumed in this work. This is valid as the exact trap distribution of a specific device is very difficulty to accurately determine. Assuming a uniform trap concentration, we can write the effective trap densities as [48]

$$N_{1,2} = \frac{N_t}{(\phi_{t1} - \phi_{t2})} \int_0^{\phi_{t1}-\phi_{t2}} P_{1,2}\, \mathrm{d}\psi / P_{1,2}^0 \tag{5.8}$$

where $P_{1,2}^0 = P_{1,2}|_{\psi=0}$.

Next, expanding the single trap model developed by [51, 52] we can write the tunneling rates as $R_1 = C_1 f_{FD}(1-f_t)N_1 P_1^0$ and $R_2 = C_2 f_t N_2 P_2^0$ [48]. C_1 and C_2 are constants which are trap energy rate dependent and are defined as

$$C_{1,2} = \frac{16\pi q E_1^{3/2}}{3h\sqrt{\phi_{1,2} - E_1}} \tag{5.9}$$

where E_1 is defined as the total energy of an electron in the metal and is given by Karmalkar et al. as 0.2 eV, f_{FD} is the temperature dependent Fermi-Dirac function defined as

$$f_{FD} = \frac{1}{1 + \exp\left[(\phi_B - \phi)/V_t\right]} \tag{5.10}$$

where V_t is the thermal voltage kT/q and f_t is the probability of occupation of a trap by an electron. If we assume a steady state condition, then f_t is constant throughout the system and $R_1 = R_2$. By integrating the tunneling rate $R = R_1 = R_2$ over the barrier layer width we can find the total trap assisted current of a gate area S as [48]

$$J_{TAT} = \frac{qS}{E} \int_{\phi_2}^{\phi_b+\phi_F} R\, \mathrm{d}\phi \tag{5.11}$$

where

$$\frac{1}{R} = \frac{1}{C_1 f_{FD} N_1 P_1^0} + \frac{1}{C_2 N_2 P_2^0}. \tag{5.12}$$

5.1.2 Poole-Frenckel

The Poole-Frenckel (PF) leakage mechanism is a process by which an electron is emitted from the metal to a continuum of trap states in the AlGaN barrier and then through this continuum of states to the 2DEG [49]. Figure 5.1 shows a graphical representation of Poole-Frenckel current.

The analytical expression for Poole-Frenckel current is

$$J_{PF} = C_{PF} E \exp\left[-\frac{q\left(\phi_{t-PF} - \sqrt{qE/\pi\varepsilon_0\varepsilon_s}\right)}{kT} \right] \tag{5.13}$$

where C_{PF} is a constant, $q\phi_{t-PF}$ is the barrier height for electron emission from the trap site, k is the Boltzmann constant, ε_0 is the permittivity of free space, and ε_s is the relative permittivity of the barrier. From (5.13) we can see that Poole-Frenckel current is proportional to $E\exp[-\sqrt{E}/T]$ and hence is temperature dependent unlike TAT.

5.1.3 Fowler-Nordheim

Fowler-Nordheim (FN) tunneling is a direct tunneling mechanism that occurs at energy levels near the Fermi level. A graphical representation of Fowler-Nordheim tunneling is given in Figure 5.1. From the figure one can see that FN tunneling is a one step process of direct transmission across a triangular potential barrier.

The expression for Fowler-Nordheim current is given as [49]

$$J_{FN} = \frac{q^2 (m_0/m^*)}{8\pi h \phi_b} E^2 \exp\left[-\alpha \phi_b^{3/2} \right] \tag{5.14}$$

where m_0 is the free electron mass, m^* is the effective mass of an electron in the barrier, h is Planck's constant, and ϕ_b is the barrier height.

Fowler-Nordheim tunneling dominates the emission at low temperatures [48]. It is noted that (5.14) is not directly related to temperature, however, it is indirectly related through Schottky barrier lowering due to temperature.

5.1.4 Thermionic-field emission

Thermionic-field emission (TFE) is the thermal assisted mechanism of direct tunneling. TFE is a one step tunneling process that occurs at higher electron kinetic energies where the barrier is thinner. TFE is governed by the equation [49]

$$J_{TFE} = \frac{qA^*T}{k} \int_0^{\phi_b} \frac{1}{1+\exp\left[q\left(\phi_b-\phi\right)/kT\right]} \exp\left[-\alpha\phi_b^{3/2}\right] \mathrm{d}\phi \tag{5.15}$$

where α has the same definition as in (5.7) and A^* is the Richardson constant. From (5.15) one can see that TFE increases with temperature and hence usually dominates all other mechanisms at higher temperatures.

5.2 Simulation of Reverse Gate Leakage Current

The effect of Al mole fraction on various leakage mechanisms has not been studied. MATLAB simulation was therefore performed to determine how each leakage component varied versus gate voltage for different Al mole fractions.

Simulations take into account a complete, physics-based model for gate leakage governed by the analytical expressions presented in Section 5.1. Table 5.1 presents the values of parameters used in the calculation of leakage for each of the mechanisms. The parameters for barrier height, ϕ_b, and the trap parameters ϕ_{t-PF}, ϕ_{t1}, and ϕ_{t2} are based on the values presented by Karmalkar et al. [48]. Values for ϕ_{t-PF}, ϕ_{t1}, and ϕ_{t2} presented in Table 5.1 are initial values and are changed throughout the simulation. The methodology for these changes are described below.

Results of the simulation using these parameters for Al mole fraction of $x = 0.3$ and an undoped

Table 5.1: Parameters used in simulation shown in Figure 5.2. Al mole fraction of this simulation is $x = 0.3$. Parameters which are dependent on Al mole fraction are dynamically calculated for each value of x. Values of ϕ_{t-PF}, ϕ_{t1}, and ϕ_{t2} are from [49].

Parameter	Symbol	Value
Electron effective mass	m^*	$0.22 \times 9.11 \times 10^{-31}$kg
Barrier height	ϕ_b	1.1 V
Richardson constant	A^*	2.74×10^{-5} A m^{-2} K^{-2}
PF constant	C_{PF}	1×10^{-9} A m^{-1} V^{-1}
High freq. relative permittivity of barrier	ε_s	5.1
PF trap potential	ϕ_{t-PF}	0.33 V
Lowest trap potential	ϕ_{t1}	0.3 V
Highest trap potential	ϕ_{t2}	1.1 V
Trap density	N_t	1×10^{14} cm^{-3}
Conduction band discontinuity	$\Delta\phi_c$	0.42 V

barrier of thickness 20 nm at room temperature is presented in Figure 5.2 when the HFET is biased at $V_{DS} = 0$ V. The experimental data points plotted in Figure 5.2 are related to a fabricated device with a gate length of 0.5 µm, and gate width of 100 µm.

As observed in Fig. 5.2, while the approximate parameters listed in Table 5.1 produce a relatively well suited match to the experimental data, the mismatch at V_{GS} values higher than −2 V suggest the lack of consideration of the dominate leakage process. That is, an additional leakage mechanism such as sidewall leakage presented by Mojaver et al. [49] is likely the cause of difference between simulated and experimental results. The values of N_t, ϕ_{t1}, and ϕ_{t2} could theoretically be altered such that total simulated leakage more closely matches experimental data. To do so, however, requires values for these parameters which exceed plausible levels. A complete discussion of simulation methodology is explained in Section 5.2.2.

5.2.1 Effect of Al Mole Fraction on Leakage Components

Next, each of the four components of gate leakage were plotted for Al mole fractions of $x = 0.4$, $x = 0.3$, $x = 0.2$, and $x = 0.1$ to see the effect that Al mole fraction has on leakage current. In the simulation, all parameters that clearly vary with Al mole fraction are recalculated for each value of x. The resulting parameters and their variation are shown in Table 5.2. In the first order analysis,

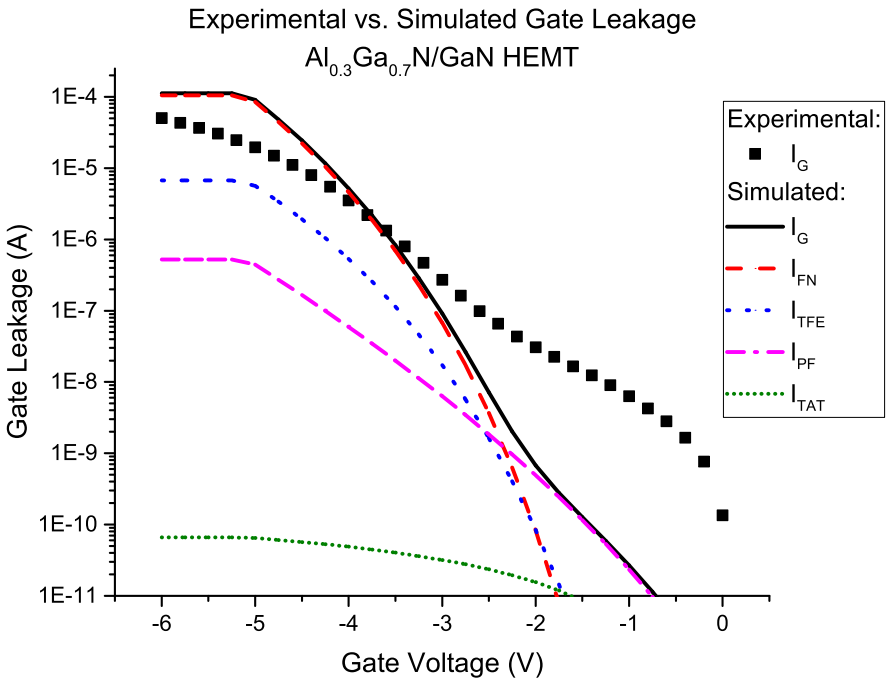


Figure 5.2: Simulated and experimental gate leakage vs. gate voltage for Al mole fraction of $x = 0.3$. $V_{DS} = 0\,\text{V}$. Experimental data is from a CMC fabricated device with gate dimensions 0.5 µm by 100 µm.

due to ambiguity in determining the dependence of trapping parameters on the value of x, these parameters (N_t, ϕ_{t1}, ϕ_{t2}, and ϕ_{t-PF}) are considered x-independent (i.e. according to Table 5.1).

According to the aforementioned simplifying assumptions, for each value of Al mole fraction, simulation results are shown in Fig. 5.3. Where applicable on each graph, a solid vertical line marks the gate voltage where FN becomes the dominant leakage mechanism (when viewed from smaller $|V_{GS}|$ to larger $|V_{GS}|$). We define this value of V_{GS} as the turning point voltage, V_{tp}.

Turning point voltage is a significant metric in analyzing gate leakage. This is because it provides a useful heuristic for determining the major mechanism of leakage current within a particular range of V_{GS}. For example, considering the set of assumptions incorporated into the model, in the case of Al mole fraction of $x = 0.3$ depicted in 5.3(b), FN is dominant for all values of $V_{GS} < -2.34\,\text{V}$. This makes sense intuitively if one examines the analytical model of FN tunneling presented in (5.14). One can see that FN current is proportional to the square of electric field times an exponential function of $-\phi_b/E$. FN therefore has a very high dependence on electric field and thus on voltage.

Table 5.2: Simulation parameters that are directly related to Al mole fraction and their corresponding variation with x according to expressions given in [4].

Parameter	**Symbol**	**Values**			
Al mole fraction	x	0.1	0.2	0.3	0.4
Barrier height without barrier lowering	ϕ_{b0}	0.97	1.1	1.23	1.36
Relative dielectric constant	ε_r	10.37	10.34	10.31	10.28
Conduction band discontinuity	$\Delta\phi_c$	0.1267	0.2674	0.4221	0.591
Spontaneous polarization	P_{sp}	–0.0052	–0.0104	–0.0156	–0.0208
Piezoelectric polarization	P_{pz}	–0.0034	–0.0072	–0.0113	–0.0158
Total polarization	σ	0.0086	0.0176	0.0269	0.0366

Accordingly, leakage mechanisms which depend on tunneling through the barrier tend to have less impact as the magnitude of V_{GS} decreases.

As illustrated in Fig. 5.3, as the Al mole fraction is decreased, the turning point gradually shifts towards smaller gate voltages. For an Al mole fraction of $x = 0.1$ there is no turning point based on the adopted assumptions. This is because for small x, threshold voltage, V_{TH}, is also smaller. Since I_G saturates at $V_{GS} = V_{TH}$ due to the saturation of the electric field across the barrier, all the leakage components saturate before FN overtakes the others.

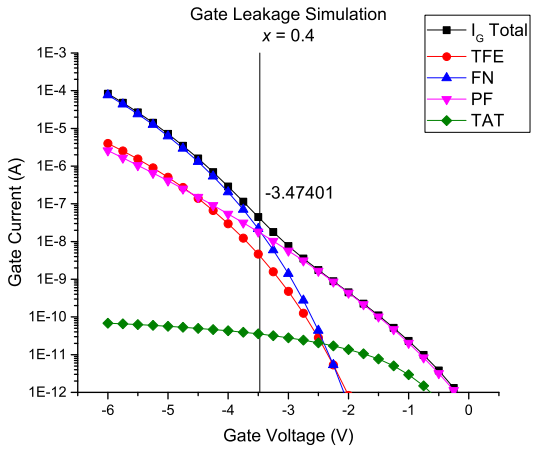
Whereas the results of the present study are biased to the choice of assumptions made especially with regard to the trapping process, the conclusions on the correlation between the turning point voltage, Al mole fraction, and the threshold voltage are deemed extendable to real devices. Values of turning point voltage and threshold voltage extracted from simulations are shown in Figure 5.3.

Another useful metric to examine with respect to Al mole fraction is threshold voltage. From the simulation, threshold voltage is defined as

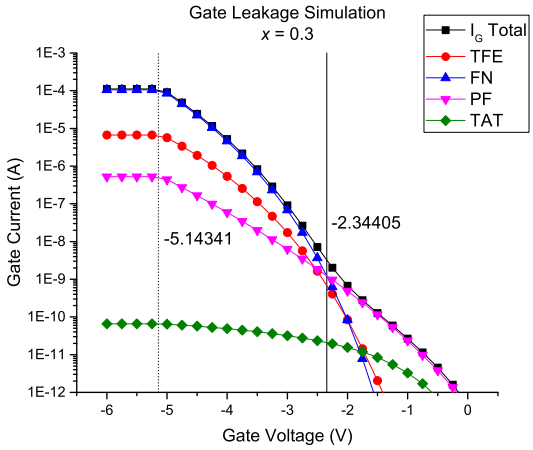
$$V_{th} = \phi_{b0} - \Delta\phi_c - \left(\frac{\sigma d}{\varepsilon}\right) \tag{5.16}$$

where σ is

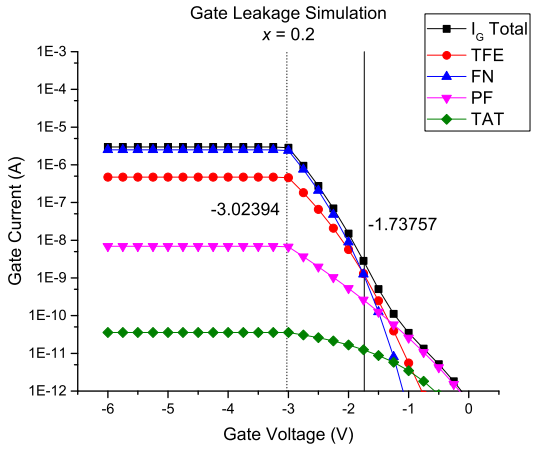
$$\sigma = -\left(P_{sp} + P_{pz}\right). \tag{5.17}$$



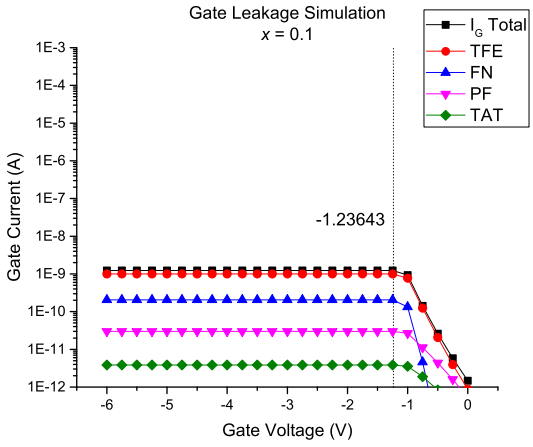
(a) Al mole fraction of $x = 0.4$



(b) Al mole fraction of $x = 0.3$



(c) Al mole fraction of $x = 0.2$



(d) Al mole fraction of $x = 0.1$

Figure 5.3: Simulation of the effect of Al mole fraction on individual leakage mechanisms. The x-axis and y-axis are kept constant for easy comparison between different values of x. All simulations are done at 300 K. Simulated gate dimensions are 0.5 µm by 100 µm. $V_{DS} = 0$ V for all simulations. Threshold voltage is denoted by the dotted vertical line, turning point is denoted by the solid vertical line.

Equation (5.16) can be solved from the expression for sheet carrier concentration presented in [4]

$$n_s(x) = \frac{+\sigma(x)}{q} - \left(\frac{\varepsilon_0 \varepsilon_r}{dq^2}\right)\left[q\phi_b(x) + E_F(x) - \Delta E_C(x)\right]. \tag{5.18}$$

One can see that the expression for threshold voltage is highly dependent on Al mole fraction as the terms ϕ_{b0}, $\Delta\phi_c$, σ, and ε all depend on Al mole fraction in various ways.

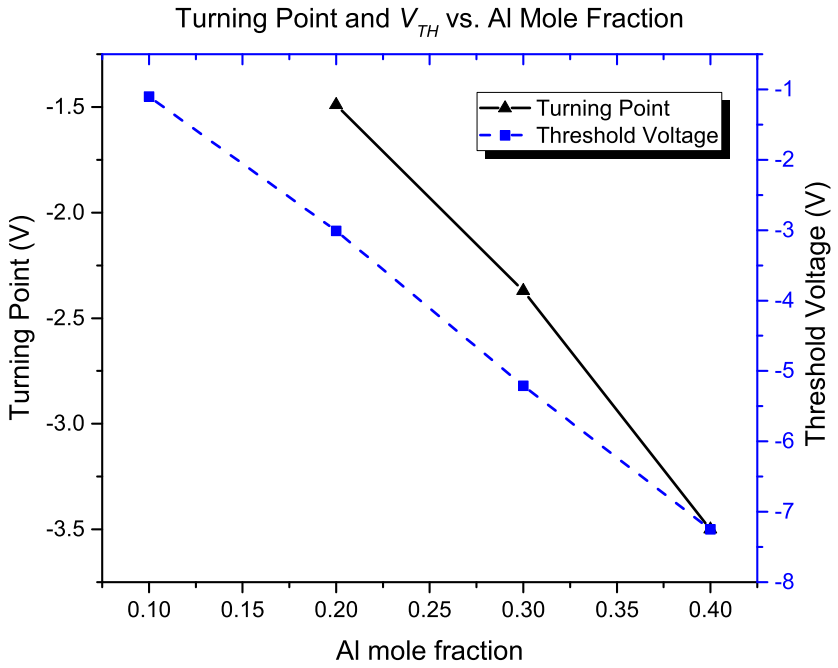


Figure 5.4: Turning point and threshold voltage vs. Al mole fraction. Note that no threshold voltage is shown in 5.3(a) because it occurs outside the axis limits. It can easily be calculated by extending the gate voltage bias range and its value is shown above.

5.2.2 Simulation Methodology: Convergence and Verification

It is critical to validate the simulation results by verifying that the simulation converges. The expressions for Poole-Frenckel current density (5.13) and Fowler-Nordheim current density (5.14) are completely analytical and therefore their convergence is guaranteed. The expression for Trap Assisted Tunneling (5.11) and Thermionic Field Emission (5.15) are solved by numerical integration using MATLAB's `integral` function. This function automatically checks for convergence and will return an error if no solution can be found given an absolute and relative error tolerance of 1×10^{-10} and 1×10^{-6}, respectively [53]. According to MATLAB documentation, the absolute error is defined as $|q - Q|$ where q is the computed value and Q is the unknown exact value. Any returned value from the function will therefore be accurate to within $\pm 1 \times 10^{-10}$. Relative error is $1 \times 10^{-6} \geq |q - Q|/|Q|$. This means a relative error tolerance of 1×10^{-6} will ensure six significant digits of accuracy. Any successfully executed code will therefore converge within an acceptable

degree of accuracy.

That the simulation converges is necessary but not sufficient. The simulation must also be valid, that is, it must accurately model the physical phenomena. This was ensured by first verifying the results with the results presented by Karmalkar [48]. The simulation was performed with the same device constants and parameters presented in [48]. Once the simulation matched the published results, device parameters and constants were changed to accurately reflect those parameters of the experimental device. The methodology for fitting device parameters was also adopted from Karmalkar [48]. The methodology is as follows. First, the parameters ϕ_{b0}, V_0, γ_T, and γ_1 are guessed based on material properties [48]. γ_T and γ_1 are fitting parameters that describe the barrier height such that [4]

$$\phi_b = \phi_{b0} - \gamma_1 \left(\frac{qE}{4\pi\varepsilon} \right)^{1/2} - \gamma_T T. \tag{5.19}$$

Then, parameters N_t, ϕ_{t1}, and ϕ_{t2} are adjusted from their initial values given in Table 5.1. These are the parameters that control the trap concentrations in J_{TAT}. An increase in these parameters have the following effect on the movement of J_{TAT} as shown in Table 5.3 [48]. These trap parameters are slightly altered then the material parameters of ϕ_{B0}, V_0, γ_T, and γ_1 are readjusted. This procedure is done iteratively until a good fit with experimental results in obtained. This methodology ensures that the simulation starts from a known good baseline. Iterative changes are small such that results are not adjusted to fit a local optimum. These methodologies ensure that simulation results are accurate and valid.

Table 5.3: Parameters and their effect on the J_{TAT} graph

Symbol	**Effect**
N_t	Upwards shift
ϕ_{t1}	Upwards shift
ϕ_{t2}	Downwards shift and anitclockwise movement

Chapter 6

Conclusion and Future Work

6.1 Conclusion

This thesis has presented a fabrication process suitable to creating 1 μm gate length AlGaN/GaN HFETs. Two different HFET designs have been fabricated and characterized with particular emphasis given to Ohmic contact formation to the AlGaN/GaN HFETs. The difference between the two HFET types is the source/drain metalization used to produce Ohmic contacts. The first Ohmic metalization scheme is a traditional Ti/Al/Ti/Au metal stack. The second more novel Ohmic scheme is a Ti-Al multi-layered metal stack.

Both HFET types have been fabricated and characterized. Results show that the new Ti-Al multi-layered metalization outperforms the traditional Ti/Al/Ti/Au Ohmic metalization. The average contact resistance across a range of temperatures is 3.22 Ω mm for the Ti-Al multi-layer metal stack compared to 3.39 Ω mm for the Ti/Al/Ti/Au metal stack. In terms of drain current density, the Ti-Al multi-layered metal stack also outperforms the traditional metal stack with maximum current densities of 0.12 A/mm and 0.09 A/mm, respectively. The new Ti-Al multi-layer metalization also bests the Ti/Al/Ti/Au metalization in terms of transconductance (60 mS/mm vs. 40 mS/mm) and subthreshold swing (0.95 V/dec vs. 1.35 V/dec).

C-V profiles of each metalization scheme are performed. Results indicate no difference between

the C-V profiles of the two metalization schemes. The C-V profiling indicates a carrier concentration of 3.75×10^{19} cm^{-3} occuring at a depth of 20 nm which corresponds to the thickness of the AlGaN barrier layer.

Finally, a model for gate leakage that examines the effect of Al mole fraction on different leakage mechanisms has been demonstrated. This is the first known model to examine the effect of Al mole fraction on gate leakage. A new metric of turning point has been introduced to help determine the dominant leakage mechanism at a given bias point. Through this it has been shown that for a larger Al mole fractions, the dominant regime of Fowler-Nordheim tunneling shifts to more negative values of V_{GS}.

6.2 Future Work

6.2.1 Ohmic Contacts

Ohmic contact performance of the Ti/Al/Ti/Au metalization and the Ti-Al multi-layered metalization are roughly a factor of 2 to 3 times inferior to the best published results. Given the state of the theory describing Ohmic contact formation to AlGaN/GaN HFETs, optimizing the metal stack and annealing temperature is more or less simply a matter of trial and error. If one assumes a metal stack of Ti/Al/metal/Au, there are four parameters at play: 1) the chosen barrier metal, 2) the Ti:Al ratio, 3) the barrier metal layer thickness (3rd layer metal), and 4) the annealing temperature. This is ignoring potential Ti-Al multilayered metalizations and other parameters such as annealing time which have less of an effect on contact resistance. Such an exhaustive search may not be worth the considerable investment. In order to improve contact resistance, it is therefore best to pick a given metal stack and try to optimize thicknesses and annealing temperatures. Given the promise of the Ti-Al multilayered metalization, it would be best to attempt to optimize this metal stack. In particular, it would be beneficial to explore the same thicknesses as presented by Pang [23]. Annealing temperatures of 800 °C to 900 °C could then be analyzed in 25 °C steps. It would also be beneficial to characterize the chemical composition of fabricated contact with tools such as XPS.

While minimizing contact resistance is undoubtedly important, good Ohmic behavior has already been observed with both metal stacks and current process recipes.

6.2.2 Lithography

The most immediate improvement to device performance as well as to the ease of fabrication can be made with a change in lithography. Any change in lithography should move the process to a maskless lithography system, either optical or preferably electron beam. The biggest benefit of such a change would be in the alignment of the gate to the source and drain contacts. As has been seen, this alignment currently pushes the bounds of tool tolerance and human error (and human tolerance). This would improve device yield and total fabrication time. Moreover it would allow smaller gate geometries and better device performance.

6.2.3 Gate Leakage

There is considerable gate leakage in measured devices as described in Chapter 4. Chapter 5 has examined the different mechanisms that lead to this observed gate leakage. There is considerable interest, therefore, in improving this gate leakage by altering or adding steps in the fabrication process. These changes would not only improve gate leakage, but as we have seen, would have an impact on other device metrics such as threshold swing and power consumption.

There are several possible steps during fabrication which could be added in order to reduce this gate leakage. The first is O_2 plasma treatment as presented in [45]. The procedure for O_2 plasma treatment is relatively simple. Before the deposition of the Schottky gate metal, the sample is treated in an oxygen asher. This oxidizes the sample surface, creating greater insulation between the gate metal and GaN. Pal et al. [54] has shown that such O_2 plasma treatment creates Ga_2O_3 on the GaN surface. This acts as a high quality gate dielectric, effectively reducing gate leakage. Chung et al. showed that this treatment has reduced gate leakage by four orders of magnitude [45]. Most importantly, this change in possible as the Nanotools cleanroom has an oxygen asher. Any introduction of new process steps is nontrivial and would likely require significant tweaking of the

new process recipe.

6.3 Improving Gate Leakage Modeling

The simulation results presented in this thesis are applicable only to rectangular mesa isolation features. Different isolation feature geometries, however, have been introduced. These isolation features have been shown to impact device characteristics including self-heating and threshold voltage. It is therefore desirable to develop a gate leakage model that fully incorporates the effect of Al mole fraction as well as isolation feature geometry. Such a model would need to include an additional leakage mechanism that occurs at mesa sidewalls. As these different isolation features have different sidewall areas, it should be theoretically possible to determine the contribution of this sidewall leakage to the total gate leakage.

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