Surrogate based Optimization and Verification of Analog and Mixed Signal Circuits

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ABSTRACT

Surrogate based Optimization and Verification of Analog and Mixed Signal Circuits

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Nonlinear Analog and Mixed Signal (AMS) circuits are very complex and expensive to design and verify. Deeper technology scaling has made these designs susceptible to noise and process variations which presents a growing concern due to the degradation in the circuit performances and risks of design failures. In fact, due to process parameters, AMS circuits like phase locked loops may present chaotic behavior that can be confused with noisy behavior. To design and verify circuits, current industrial designs rely heavily on simulation based verification and knowledge based optimization techniques. However, such techniques lack mathematical rigor necessary to catch up with the growing design constraints besides being computationally intractable. Given all aforementioned barriers, new techniques are needed to ensure that circuits are robust and optimized despite process variations and possible chaotic behavior. In this thesis, we develop a methodology for optimization and verification of AMS circuits advancing three frontiers in the variability-aware design flow. The first frontier is a robust circuit sizing methodology wherein a multi-level circuit optimization approach is proposed. The optimization is conducted in two phases. First, a global sizing phase powered by a regional sensitivity analysis to quickly scout the feasible design space that reduces the optimization search. Second, nominal sizing step based on space mapping of two AMS circuits models at different levels of abstraction is developed for

the sake of breaking the re-design loop without performance penalties. The second frontier concerns a dynamics verification scheme of the circuit behavior (i.e., study the chaotic vs. stochastic circuit behavior). It is based on a surrogate generation approach and a statistical proof by contradiction technique using Gaussian Kernel measure in the state space domain. The last frontier focus on quantitative verification approaches to predict parametric yield for both a single and multiple circuit performance constraints. The single performance approach is based on a combination of geometrical intertwined reachability analysis and a non-parametric statistical verification scheme. On the other hand, the multiple performances approach involves process parameter reduction, state space based pattern matching, and multiple hypothesis testing procedures. The performance of the proposed methodology is demonstrated on several benchmark analog and mixed signal circuits. The optimization approach greatly improves computational efficiency while locating a comparable/better design point than other approaches. Moreover, great improvements were achieved using our verification methods with many orders of speedup compared to existing techniques.

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In loving memory of my mother,

To my husband, my father, and my daughter and son.

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ADD	Algebraic Decision Diagram
ADC	Analog-to-Digital Converter
AMS	Analog and Mixed Signal
ASM	Abstract State Machine
BJT	Bipolar Junction Transistor
CAD	Computer-Aided Design
CPU	Central Processing Unit
CMRR	Common-Mode-Rejection-Ratio)
DAC	Digital-to-Analog Converter
DC	Direct Current
DTW	Dynamic Time Warping
EDA	Electronic Design Automation
FD	Frequency Divider
FNN	False Nearest Neighbor
FSM	Finite State Machine
FWER	Family-Wise Error Rate
GA	Genetic Algorithm
GK	Gaussian Kernel
GSA	Global Sensitivity Analysis
IC	Integrated Circuit
IP	Intellectual Property
JRV	Joint Recurrence Verification
KCL	Kirchhoff's Current Law

KVL	Kirchhoff's Voltage Law
LC	Resonant Circuit: Inductor L and Capacitor C
LCSS	Longest Common SubSequence
LDC	Low Discrepancy Sequence
LE	Lyapunov Exponent
LHS	Latin Hypercube Sampling
LSA	Local Sensitivity Analysis
LZC	Lempel-Ziv Complexity
MC	Monte Carlo
MC-JK	Monte Carlo-JacKknife
MHT	Multiple Hypothesis Testing
MNA	Modified Nodal Analysis
MOR	Model Order Reduction
MOS	Metal Oxide Semiconductor
NBTI	Negative-Bias Temperature Instability
NMOS	N channel MOSFET
ODE	Ordinary Differential Equation
PDF	Probability Distribution Function
PFD	Phase Frequency Detector
PLL	Phase Locked Loop
PMOS	P channel MOSFET
PRS	Pseudo Random Sampling
PSS	Periodical Steady State
PV	Process Variation
PVT	Process Voltage Temperature

QMC	Quasi-Monte Carlo
SDE	Stochastic Differential Equation
SET	Single Event Transient
SEU	Single Event Upset
SHD	Sobol-Hoeffding Decomposition
SMC	Smart Monte Carlo
SoC	System on Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static Random-Access Memory
SDE	System of Differential Equation
SDM	Sigma Delta Modulator
SDE	System of Stochastic Equation
SRE	System of Recurrence Equation
SSRE	System of Stochastic Recurrence Equation
TSMC	Taiwan Semiconductor Manufacturing Company
TF	Transfer Function
VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integrated
WCA	Worst Case Analysis

Chapter 1

Introduction

"If the digital designers did verification the way analog designers do verification, no chip would ever tape out."

Sandipan Bhanot, President and CEO of Knowlent.

1.1 Motivation

Analog and Mixed Signal (AMS) circuits hold a great compromise for use in many applications such as automotive electronics, communications, sensor networks, and portable electronics [1]. It is an indispensable block of today's microprocessors and embedded system designs. Indeed, it relates the design to the real world through communicating the analog external world signals to the discrete-valued internal design signals. Therefore, analog circuits perform typical functions that cannot be overtaken by their digital counterparts (e.g., Digital to Analog Converters (DAC), Analog to Digital Converters (ADC), amplification, filtering and clock generation) [2].

In the microelectronics industry, getting to market early with robust and efficient designs is a key aspect to stay competitive. This can be achieved through innovative

tools which on one hand, select optimal topologies and geometries and on the other hand, rigorously verify the design adherence to specifications. Nevertheless, AMS integrated circuits are posing serious bottlenecks in both design and verification. The main challenges stem from the following reasons:

- The fundamental differences of the digital and analog components operating modes. Owing to the nonlinearity of analog circuits, their performance highly depends on circuit parameters and operating conditions.

- The large design space coupled with the high complexity of the circuit dynamics, the various design imperfections that worsen circuit behavior and the increasing tight design constraints (i.e., power, area, speed).

- The trend towards more functionalities makes AMS designs extremely complex and thereby very expensive to design and verify. An enormous amount of time, effort and cost from the overall VLSI design effort are spent in analog parts as shown in Table 1.1 [3].

- The lack of adequate and mature commercial analog CAD tools that are basically limited to some clones of *SPICE* simulator [4].

Table 1.1: The gap between analog and digital productivity

	Analog	Digital
Time Cost	85%	15%
Design Effort	80%	20%
Occupied Area	10-20%	80-90 %
Added Value	90 %	10 %

With the aggressively scaled semiconductor devices, the AMS design task is additionally burdened with the increasingly inevitable process-induced variability owing to the limitation in the lithography and fabrication process. Process variation refers to the

difference between the intended and obtained voltage and process parameters prior and post-fabrication of the circuit. It substantially affects circuit parameters such as the channel length (L), the gate width (W), the threshold voltage (V_{th}) and the oxide thickness (T_{ox}). On the other hand, AMS designs are known for the high dependency of their performance on the circuit geometries, initial conditions and operating points [5]. Hence, even the smallest deviation in the circuit can be large enough to violate the desired circuit performance and consequently results in yield loss. Process variation is, therefore, emerging as a real reliability concern in the realm of AMS designs that hinders more technologies scaling due to the difficulty of fabricating smaller transistor structures [6]. The aforementioned hurdles have hindered the advancement of AMS circuits design and verification methodologies. It is hence not sufficient to design the AMS circuit for solely nominal parameters nor convenient to verify whether the specifications are met for few possible design points.

The AMS circuit design procedure generally consists of the topological-level design and parameter-level design (also called circuit sizing). In this thesis, we are more interested in parameter-level design. The circuit sizing is formulated akin to an optimization procedure wherein optimum circuit parameters are selected with regard to desired performance constraints. Existing approaches for circuit optimization can be broadly classified based on the abstraction level of the design model into two main categories: *Simulation-based* and *equation-based techniques*. At transistor level, simulation-based techniques are used to evaluate the circuit performances based on its fully detailed transistor model using *SPICE* circuit simulator. Thus, very high accuracy can be achieved. However, these techniques are time-consuming since they are purely numerical and need several iterations to converge to a solution. In short, such techniques are yet accurate but tedious and very resource-intensive.

At behavioral level, equation-based optimization techniques are deployed. These techniques model the circuit performance as a set of analytical equations of the circuit variables. Despite their offered speedup over simulation-based techniques, these techniques suffer from a limited accuracy due to the limited amount of details available at high-level circuit models. Consequently, a new mixed optimization approach is much needed, which on one hand would offer better accuracy than the equation-based techniques and on the other hand, would leverage the designers' intent to guide the simulation-based technique quickly to the optimal parameters solution.

Once the circuit is optimized, there is no guarantee that it will fulfill its specification in the presence of nonidealities such as Process, Volatge and Temperature (PVT) variations and noise. In fact, the variation in the geometrical and electrical device parameters can compromise the circuit's performance (e.g., PLL locking, circuit stability, etc.) and consequently can lead to design failures. Subsequently, ensuring correct circuit operation is an essential requirement that dictates careful verification of the AMS circuit under consideration of process variation. Experiments showed that in specific operation conditions (i.e., circuit parameter, initial conditions, and input signals) even remarkably simple AMS circuits are capable of exhibiting a chaotic mode of operation [7]. For instance, the discovery of chaos has been followed by its detection in many circuits such as PLL [8], Colpitts Oscillator [9], and Σ-Δ modulator [10].

The irregular, seemingly random and unpredictable but deterministic behavior of chaos makes it resemble noise. However, when an irregularity is observed in an AMS design output, designers intuitively assume that the circuit exhibits stochastic noise, which is stubbornly present in such designs. Nevertheless, such behavior could emerge from a purely deterministic circuit. Because noise detection is a contentious issue for designers and there is a lack of efficient noise verification tools for AMS designs, a

chaotic circuit could be considered erroneously noisy. Therefore, it is fundamental to investigate circuit dynamics thoroughly and intuitively enough to append the real source of any aberrant circuit behaviors.

Verifying functional properties (i.e., chaotic, noisy, ideal behaviors) to detect inappropriate circuit behaviors is not sufficient to commit optimal analog ICs to the foundry. As mentioned earlier, process variation threatens to worsen overall circuit behavior and impair its performance which culminates in circuit failures and hence yield loss. Therefore, verifying circuit robustness to process variation is an extremely important step in the AMS design flow. Ensuring a robust operation of the AMS designs in light of process variation disturbance is an essential requirement that dictates careful verification. Verification techniques of process verification effect become the frontier research topic in recent years for design and manufacturing of high-performance VLSI circuits. Traditionally, Monte Carlo (MC) simulation techniques [11] are used to verify circuits as well as behavioral models of analog designs. Based on repetitive simulations, Monte Carlo simulation permits the evaluation of substantive design properties based on a statistical estimation of circuit parameters. To do so, this approach needs a pre-specified underlying distribution, mainly uniform, normal, or log-normal to describe the random variables of process variation effects. Hence, a wrong distribution assumption leads to a possibility of outright wrong results [12]. In addition, because the accuracy of this method is directly related to the number of simulation runs, this method results in long simulation times. Therefore, empowering designers with new tools and techniques in order to tape out circuits that withstand process variation while meeting strict specifications is imperative.

In this thesis, we present a surrogate based optimization and verification methodology for AMS circuits. Our proposed methodology tackles the limitations of multi-level optimization approaches. It also efficiently assesses circuit reliability, both qualitatively and quantitatively, in light of process variations. More details about the proposed methodology will be given in Section 1.3. We next provide a critical overview of the state-of-the-art optimization and verification techniques for AMS circuits.

1.2 State-of-the-Art

In this section, we briefly review some relevant literature in the area of circuit optimization-based sizing, dynamical behavior verification as well as circuit robustness verification in terms of yield estimation techniques which are closely related to this thesis.

1.2.1 Analog Circuit Optimization

For a given circuit topology, optimization refers to finding the optimal circuit parameters that result in the best circuit performance with respect to given specifications and constraints. A detailed survey of existing AMS circuit optimization techniques can be found in [13]. According to the abstraction level of the design model on which the optimization is conducted, optimization techniques can be broadly classified into two main categories: Equation-based and simulation-based techniques.

- ***Equation-based Optimization***

  At the behavioral level, equation-based approaches use analytical equations from large and small signal analysis of the circuit topology to relate the circuit's performance to the design variables [14]. These performance equations are evaluated at every iteration of the design space exploration in order to guide

the optimization towards the design specification. Early work [15] defines the optimization problem as a constrained nonlinear optimization problem. In this technique, the circuit performance equations are extracted from its SPICE models and DC operating point constraints which are then solved using sequential quadratic programming. This technique has a convergence problem as the optimization circuit parameter solution might entrap in local minima. To ensure a global minima design solution, the optimization problem is cast as a convex problem which can be then solved very efficiently by numerical algorithms like geometric programming [16]. However, modeling the design objective and the constraints as convex functions of the design variables is not always possible. For instance, when the design objectives involve optimizing large-signal or transient characteristics, it is extremely difficult to manually derive equations that capture all design characteristics in a convex equation form. A breakthrough in automatic generation of optimization equations has been made with the advent of symbolic simulation techniques [17]. These techniques automatically generate small signal transfer functions for any chosen topology and process technology. However, they suffer from major scalability and accuracy drawbacks. For instance, the complexity of exact symbolic solutions scales exponentially with the circuit size. The heuristic simplifications and approximations introduced in the analytic equations make this approach inaccurate especially for complex circuits [18].

- ***Simulation-based Optimization***

  At the circuit level, simulation-based optimization techniques have been proposed. In contrary to the equation-based approach, these techniques do not rely on analytical equations but on a detailed circuit level model, e.g., SPICE

model. At each optimization step, the circuit performance is simulated for a set of design parameters. Although the idea of optimizing AMS circuits using simulation dates back to at least 1969 [19], it is only recently that this approach became popular due to the availability of powerful computers and advances in numerical algorithms. In the literature, optimization procedures were conducted using different global nonlinear optimization algorithms such as simulated annealing [20], stochastic pattern search [21], geostatistics algorithm [22], evolutionary algorithms [23] or a combination of these algorithms [24]. Despite their high accuracy and ability to handle a broad class of circuits, commercial circuit simulators are not designed to be extensively invoked [25]. Hence, a large number of design variables and consequently the large design space make the optimization task extremely difficult even for advanced computational systems.

From the above discussion, it is obvious that a good compromise lies somewhere between these two main optimization approaches. An early attempt for a mixed equation-simulation approach was the ASTRX/OBLX tool [26]. In this tool, the circuit performance is simulated using asymptotic waveform evaluation which is a model reduction technique, to evaluate circuit objectives and performances. However, this technique is only applicable to linear circuits. In this thesis, we propose a novel mixed optimization approach for nonlinear circuits that reduces the simulation time while maintaining accuracy.

1.2.2 Circuit Dynamics Verification

Once the circuit is optimized, techniques that ascertain its intended functionality/behavior in light of process variations and initial conditions uncertainties are essential. In particular, probing chaotic from noisy dynamics in analog circuits is of a great concern

for designers. In fact, chaotic and noisy behaviors present the same salient features of long term unpredictable irregular behavior and broad band spectrum making their distinction far from straightforward. The study of chaotic features in AMS circuits is the subject of an extensive research (e.g., [27, 28]). Available techniques for circuit verification, like spectral analysis, fail to discriminate chaotic from random circuit outputs since both of them have continuous broadband power spectra [29]. Periodic Steady State (PSS) analysis is used in [30] to discriminate periodic from chaotic behavior. A periodic behavior is detected when the obtained convergence norm is equal or less than unity. Conversely, a chaotic behavior is reported when the Spectre simulator [31] does not converge and the PSS analysis fails to find any periodicity in the circuit output. Nevertheless, non-periodic behavior could be due to noise and not to chaos. Moreover, the Newton algorithm used by the PSS method requires the computation of the Jacobian matrix of the output. This seriously limits the scalability of this technique. Moreover, PSS Spectre analysis does not work under an unknown oscillation frequency. Lyapunov Exponent measure [32] is another paradigm that has been adopted to quantify chaos. It indicates the average rates of convergence or divergence of circuit behaviors for close initial conditions. A positive exponent implies divergence and is indicative of chaotic dynamics while a negative one implies convergence and is said to be periodic. Lyapunov Exponent is defined as a limit when time t approaches infinity (see Equation (1.1)), one encounters fundamental difficulties using it for circuits simulated for a limited time.

$$\lambda_i = \lim_{t\to\infty} \frac{1}{t} ln|\sigma_i(t)|, \forall i \in [1, .., n] \tag{1.1}$$

$\{\sigma_i\}_{i=1}^{n}$ are the eigenvalues of the Jacobian matrix of the circuit. This technique is hampered by technical issues related to the signal length and its contamination by noise (known as Perron effects) [33]. Hence, a positive Lyapunov exponent is neither

necessary nor sufficient proof of chaos [34].

In spite of the above-mentioned approaches, a clear differentiation between chaotic and stochastic processes seems to be rather problematic. In this thesis, a novel approach to precisely probe the underlying circuit dynamics at an early stage and so assess qualitatively the observed circuit behavior (deterministic or stochastic) is proposed.

1.2.3 Yield Estimation

Yield analysis and estimation for AMS designs have been greatly debated and have become an appealing area of research in recent years [35, 36]. We review hitherto existing techniques for analog circuits parametric yield analysis.

State of the art parametric yield estimation techniques for AMS designs can be roughly divided into two categories: parameter domain and performance domain techniques. While parameter domain techniques are based on the characterization of a yield boundary defined by the design specification, performance domain techniques rely upon extensive Monte Carlo simulations.

- ***Parameter domain techniques***

  These methods try to extract an analytical relation between the underlying process parameters and the circuit performances/specifications. To aid design exploration in a large process variation space, a number of performance modeling methods have been proposed. For instance, response surface modeling has been adopted to approximate the performances of interest as polynomial functions of process parameters in order to substitute expensive SPICE simulations [37]. Most of the existing response surface modeling techniques rely on linear approximations. However, this would sacrifice accuracy for speedup

particularly in large scaled process variations where a great number of AMS circuit performances are strongly nonlinear. As demonstrated in [38], the resulting accuracy might be unacceptable with an absolute error of 9%. To enhance the accuracy, a quadratic response surface modeling has been used [39] but at the cost of a much more difficult yield estimation. For instance, by mapping the performance constraints dictated by the circuit specifications to a feasible space in the process parameter space, such a mapping becomes nonlinear with a non-convex or even discontinuous feasible space. Hence, the parametric yield which is defined as the integral of the probability density function over the feasible space becomes extremely difficult to compute. Other existing methods rely on a surface boundary, which is the separation between the success and failure regions in the yield estimation. The yield is so estimated using a local search [40] or global search [41] by computing the volume of the failure region without the need for circuit simulation. Nevertheless, such methods suffer from scalability issues with no more than three process parameters.

- ***Performance domain techniques***

  Monte Carlo (MC) [11] is the most widespread performance domain yield estimation technique thanks to its extreme simplicity and general applicability. However, an MC analysis of large-sized circuits is highly inefficient and time consuming since it requires a large number of simulations leading to lengthy analysis time. Several speed-up techniques have been proposed to improve the primitive MC time efficiency and applicability. Quasi-Monte Carlo (QMC) [42] is a variance reduction technique in which Low Discrepancy Sequences (LDS) are utilized to generate more homogeneously distributed process parameters samples rather than purely-random samples. Hence, QMC techniques are able to provide

better integration errors compared to primitive MC. Yet, QMC has a limited performance improvement with a convergence rate that is asymptotically superior to MC only for circuits with a moderate number of process parameters [43]. Furthermore, MC and QMC can estimate only the gross effect of process variation on the circuit performance/yield and hence do not provide information regarding the most influential components/parameters on the yield loss. While aforementioned yield analysis methods present a panoply of approaches to speed-up and enhance the yield estimation accuracy, there are still many limitations that need to be addressed. For instance, they use greedy sole performance yield estimation or perform several independent single parametric yields. Nevertheless, this might significantly compromise the accuracy (i.e., under-estimate the yield) especially in the case of correlated circuit performances.

In summary, nonlinear AMS circuits optimization and verification techniques still lag in providing a unified methodology that is general (i.e., handles single and multiple performances optimization as well as verification problems with correlated performances), accurate in sizing circuits and verifying their robustness, and also scalable with respect to process variations.

1.3 Thesis Methodology

The main goal of this thesis is to develop a means to design high-quality analog and mixed signal designs for which specification requirements are satisfied in the most robust manner. To this end, we have brought together an efficient sizing method formulated akin to an optimization algorithm that replaces the labor intensive parameter tuning process as well as rigorous verification techniques that ensure sized circuit adherence to design specifications in the most robust manner.

The proposed methodology is schematically shown in Figure 1.1 where we outline the main steps thereof: Given an AMS circuit topology, a technology node, and a set of design specifications, a surrogate based optimization method is conducted to extract the set of circuit parameters such as transistor sizes, and capacitors and resistors values. It is a method inspired from formal equivalence checking techniques.

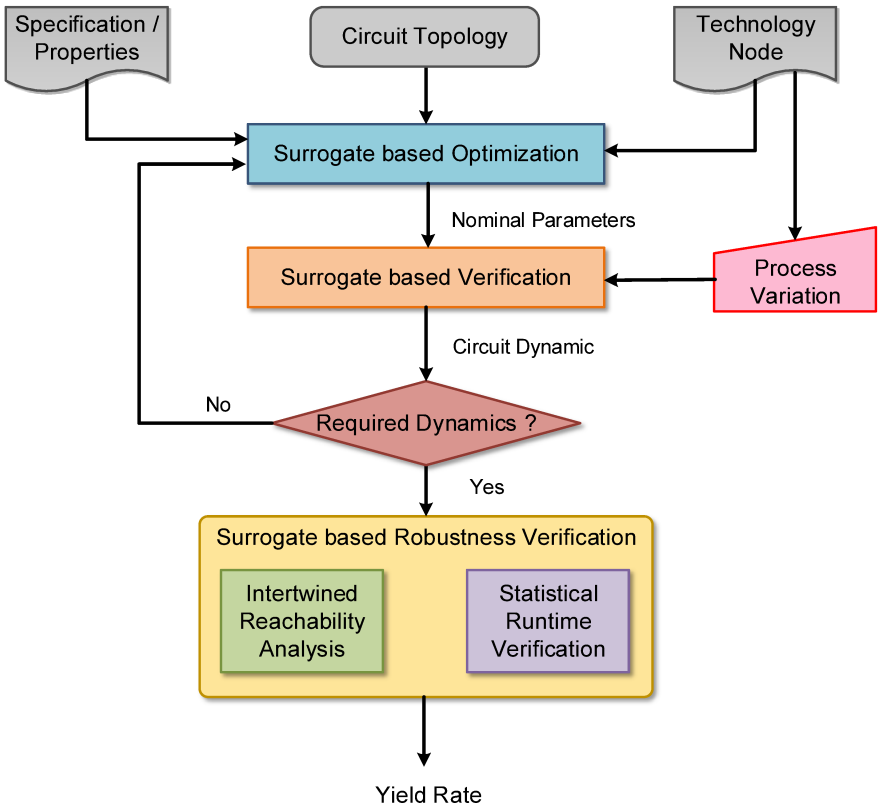

Figure 1.1: Proposed surrogate based optimization and verification methodology

The optimization is performed through a bijection of the circuit parameters solution extracted from a fast/not accurate surrogate circuit model into their corresponding parameters of an accurate yet CPU intensive detailed model. A method by which, we eliminate the need for separate sequential optimization and we shift the computational burden of the complex slow detailed circuit model optimization to the fast surrogate

model. The output of this optimization step is a set of nominal circuit parameters that satisfy the specification constraints and give the best circuit performance in ideal conditions (i.e., does not consider process variations, operating conditions, and noise disturbances). The next step in our methodology is to ensure a robust operation of the AMS circuit for the computed nominal parameters in the presence of process variation disturbance. To do so, we adopt two different verification approaches. The first approach is a surrogate based dynamics verification technique that aims to qualitatively investigate the circuit dynamics for the computed set of so-called optimal design parameters. More specifically, it verifies whether the circuit may drift into a chaotic behavior for the computed optimal parameters. However, since chaos resembles noise and noise is omnipresent in AMS circuits, we propose a novel method that statistically discriminates chaos from noisy circuit dynamics. If it fails, the computed nominal circuit parameters are eliminated from the feasible design space and changed with a new optimal circuit parameters solution. Once these new nominal parameters pass the surrogate based verification, the circuit will be further evaluated in terms of yield. The second verification approach is a surrogate based robustness verification technique. It consists of two verification methods, which ensure that the desired properties of the circuit are satisfied in the most robust manner. The first is an intertwined reachability analysis technique. It is a time domain verification technique for a single circuit performance. It is based on an intertwined forward/backward reachability analysis approach. Next, a single hypothesis testing technique is performed on the obtained reachable sets in order to estimate the system parametric yield caused by the deviation from the nominal/optimal parameter values due to process variation. The second method is statistical runtime verification approach. It is a state space domain verification approach that handles multi-performances yield rate estimation.

It adopts a global sensitivity analysis to reduce and prioritize the process variation space. Thereafter, the acquired sensitivity results are efficiently embedded in a joint recurrence verification scheme for a state space transient circuit behavior verification. Lastly, the multi-performance yield estimation problem is cast into a multiple hypothesis testing problem under the limiting conditions retrieved from the design specifications.

We demonstrate the effectiveness of each part of our methodology on various nonlinear analog and mixed signal circuits. Some of the nonlinear circuits used for this purpose include analog amplifier, Σ-Δ modulator, phase locked loops, ring oscillator, Colpitts oscillator and tunnel diode oscillator. We provide an in-depth analysis of our experimental results and justify the use of every approach proposed in this methodology. All models, methods and applications described in this thesis are implemented in the MATLAB environment, on a Windows 10 operating system with an Intel Core i7 CPU processor running at 2.8 GHz with 24 GB of RAM.

1.4 Thesis Contributions

The primary contribution of this thesis is on the development of a methodology to induct nonlinear AMS circuits sizing and verification using surrogates. It presents new approaches for multi-objective optimization for analog sizing and multi-performances verification of both functional and non-functional properties. It combines mixed simulation/equation based optimization techniques using a state space equivalence scheme, statistical proofs by contradictions, global sensitivity analysis, and nonlinear systems dynamical theory. In the sequel, we list the main contributions of this work along with references to related publications provided in the Publications section at the end of the thesis document.

- The development of surrogate based AMS modeling formalisms for circuit sizing, design space exploration, and circuit debugging and verification. It proposes an initiative towards developing a unified language standards for modeling and defining AMS circuit assertions in a more formal way [Cf3, Cf5].

- The elaboration of a novel multi-level optimization technique that reduces the runtime of the equation based optimization approaches while maintaining the *SPICE* accuracy in a single technique. The technique is able to ensure an exhaustive coverage of the design search space and outputs better design points than other techniques [Jr2].

- The implementation of a surrogate based dynamics verification method to ascertain functional properties. It particularly studies apparently stochastic behavior that at a deeper level could present chaos. The proposed method provides an efficient scheme in detecting chaos over Lyapunov Exponent (LE) method for Gaussian noise [Cf5]. We extended the surrogate based dynamics verification method with a novel test statistic to uncover noisy behavior with non-Gaussian distribution and for hyperchaotic regime [Cf1].

- An intertwined reachability analysis approach is implemented to reduce wrapping effect in the forward only scheme [Cf3, Tr1]. In particular, we extend the forward reachability analysis approach developed in [Cf7] to reduce overbounding.

- The implementation of yield estimation methodology that handles multiple performances constraints and that also opts for a simultaneous yield analysis rather

than multiple single-performance yield estimation. The proposed multiple performance yield estimation scheme prevails over Monte Carlo techniques in accurately assessing the yield with significant speed-up [Jr1, Cf2].

- The genesis of a library of state space yield estimation is developed. A method called Cross Recurrence Verification inspired from pattern matching in DNA sequences is introduced. The main advantage of the proposed methodology is robustness, providing more meaningful quantification of circuit failures and its suitability for verification automation [Cf4].

- A method for non-parametric statistcal runtime verification of AMS circuits is developed. It is a variant of the Monte Carlo method with more effective sampling scheme and variation free distribution. The developed approach provides sound verification results (i.e., good accuracy with a reduced error margin) and so can be used in lieu of the Monte Carlo method [Cf5].

1.5 Thesis Organization

The remainder of this thesis is organized as follows: In Chapter 2, we provide some introductory concepts of the techniques and the basic mathematical methods applied throughout this thesis. Then, in Chapter 3, we describe the proposed surrogate-based optimization methodology in details. We explain how we reduce the feasible parameters search space and how the design centering is performed on the obtained reduced search space. The efficiency of the proposed optimization methodology is demonstrated on two circuits, namely a ring oscillator and a two stage amplifier. Thereafter, the optimized circuit is verified qualitatively and quantitatively. Chapter 4 is devoted to the qualitative verification of the circuit dynamics. We present the

surrogate-based core algorithm involved in discriminating the different behaviors that the circuit might exhibit in the presence of process variation. Then, in Chapter 5, we detail the quantitative time domain verification approach for single performance yield estimation. We explain the proposed intertwined reachability analysis approach that reduces the high reachability overbounding of the forward scheme. We also provide applications results which prove that the proposed method reduces the verification bias while accounting for a wide range of circuits disturbances/variations. Moreover, in Chapter 6, we present our multiple performances yield estimation wherein we analyze the circuit transient behavior under the effect of process variations. We report experimental results for the verification of two analog benchmark circuits, namely a five stage ring oscillator and a phase-locked loop. Moreover, we illustrate the application of the thesis overall methodology on a three stage ring oscillator to prove its effectiveness on achieving the stated thesis objectives of surrogate based optimization and verification. Finally, in Chapter 7, we conclude the thesis by summarizing the main contributions and list some possible future directions.

Chapter 2

Preliminaries

The primary goal of this chapter is to give some background concepts that are needed for the foundation of this thesis. We first provide an overview of the surrogate based circuit modeling. Then, we explain the Sobol-Hoeffding Decomposition (SHD) procedure that will be used later for global sizing during the optimization stage and for process parameter prioritization during the statistical runtime verification. We also present the classical hypothesis testing procedure to statistically verify AMS circuit properties. Finally, we introduce some relevant notions regarding AMS circuits yield rate estimations.

2.1 Surrogate based Circuit Modeling

Surrogate based circuit modeling is a macromodeling technique based on mathematical foundations that capture the actual circuit behavior [44]. It is a fundamental block of any analog optimization and/or verification algorithm at early stage in the VLSI design flow. The generated surrogate models the generic dynamic behavior/characteristic of the circuit for a set of initial conditions and input voltages. In

general, it should comply with the following conditions:

- maintain a certain level of conformance to the real circuit dynamics with appropriate speed/accuracy tradeoff.
- cope with the complexity of the AMS design yet easily amenable to sizing as well as verification approaches.

In this section, we describe in some detail the basic concepts and formulations of the surrogate based modeling techniques used in this thesis, namely Extended-System of Recurrence Equation (E-SRE) and Systems of Stochastic Recurrence Equation (SSRE).

2.1.1 Extended-System of Recurrence Equation

Analog and mixed-signal designs contain both analog and digital modules that are interconnected and interrelated. Therefore, it is not appropriate to model these modules separately. For instance, the continuous (analog) signals and the discrete (digital) signals have to be described using the same approach in order to capture the interrelationships between the two. The behavior of analog circuits can be mathematically modeled by Ordinary Differential Equations (ODEs). Since a closed-form solution for these ODEs is not always obtained, a numerical approximation is needed. Using a System of Recurrence Equations (SREs) [45], it will be possible to handle continuous behaviors like those of currents and voltages in discrete time intervals which can be done for a non-trivial class of analog circuits. An SRE is a set of relations between consecutive elements of a sequence. It is mathematically defined as a system consisting of a set of equations of the form:

$$x_i(n_t) = f_i(x_j(n_t - \delta)), \forall n_t \in \mathbb{Z} \tag{2.1}$$

where $x_i(n_t) \in \mathbb{R}$ is a state variable with $i, j \in 1, .., k$ and $n_t \in \mathbb{Z}$, and $\delta \in \mathbb{N}$ represents the delay. On the contrary, digital designs are described using various frameworks such as Finite State Machines (FSMs) and Petri nets. To alleviate the modeling gap between the digital and analog models, we propose the notion of so-called Extended SRE for interleaving the two [46]. Extended SREs offer a means of modeling more abstracted AMS designs which will significantly speed up the verification execution time. The notion of Extended-SREs (E-SREs) is mathematically defined as follows: Let $\mathbb{K}$ be a numerical domain ($\mathbb{B}, \mathbb{N}, \mathbb{Z}, \mathbb{Q}$ or $\mathbb{R}$), a *generalized If-formula* is one of the following:

- A variable $x_i(n)$ or a constant $C \in \mathbb{K}$.
- Any arithmetic operation $\diamondsuit \in (+, -, \times, \div)$ between variables $x_i(n) \in \mathbb{K}$.
- A logical formula: any expression constructed using a set of variables $x_i(n) \in \mathbb{B}$ and logical operators : not, or, and, nand, nor, etc.
- A comparison formula: any expression constructed using a set of $x_i(n) \in K$ and comparison operators $\alpha \in (<, =, >, <>)$.
- An expression $If(x, y, z)$, where x is a logical formula or a comparison formula and y, z are any generalized If-formula. Here, $If(x, y, z) : \mathbb{B} \times \mathbb{K} \times \mathbb{K} \rightarrow \mathbb{K}$ satisfies the axioms:

$$If(True, x, y) = x$$
$$If(False, x, y) = y$$

2.1.2 System of Stochastic Recurrence Equation

Due to the statistical behavior that AMS circuits exhibit in the presence of uncertainties (such as noise and parameter variability), we are interested in modeling AMS circuits transient behavior as a System of Stochastic Recurrence Equations (SSRE) [47], which is a formalism that allows capturing the statistical properties of the system in a unified discrete-time description. In what follows, we explain the SSRE notations and detail the conversion process of circuit equations to SSREs. A system of recurrence equations is a set of relations between consecutive elements of a sequence. A stochastic recurrence equation can be generated for the case of continuous systems using the discrete version of their Stochastic Differential Equation (SDE) [48]. SDEs have been used in [49] to model non-idealities in analog/RF circuits. However, a closed-form solution cannot be solved explicitly. In the following, we briefly present the SSRE theory. An SSRE is a set of system recurrence equations with stochastic processes. We consider the Euler scheme to define the SSRE. Let us consider the following Itô process $\{X_t, 0 \leq t \leq T\}$ SDE:

$$dX_t(\omega) = f(X_t(\omega))dt + \sigma(X_t(\omega))dW_t(\omega) \tag{2.2}$$

where the stochastic variable W_t is a Brownian motion [50] (see Definition 2.1.1) and σ denotes the diffusion coefficient.

Definition 2.1.1 *(Brownian Motion) A scalar standard Brownian process, or standard Wiener process over [0,T] is a random variable W_t that depends continuously on $t \in [0, T]$ and satisfies the following conditions:*

Condition 1 *$W(0) = 0$ with probability 1.*

Condition 2 *For $0 \leq s < t \leq T$ the random variable given by the increment $W_t - W_s$*

is normally distributed with mean zero and variance $(t-s)$ *(*$W_t - W_s \sim \sqrt{t-s}\mathcal{N}(0,1)$*).*

Condition 3 *For* $0 \leq s < t < u < v \leq T$ *the increments* $W_t - W_s$ *and* $W_v - W_u$ *are independent.*

By integrating in Equation (2.2) between s and $s + \Delta s$, we will have:

$$dX_{s+\Delta s}(\omega) = X_s(\omega) + \int_s^{s+\Delta s} f(X_{s+\Delta s}(\omega))dt + \int_s^{s+\Delta s} f\sigma(X_{s+\Delta s}(\omega))dW_{s+\Delta s}(\omega) \quad (2.3)$$

The Euler scheme [51] consists in approximating the integral Equation (2.3) by the following iterative scheme:

$$\bar{X}_{s+\Delta s}(\omega) = \bar{X}_s(\omega) + f(\bar{X}_s(\omega))\Delta s + \sigma(W_{s+\Delta s}(\omega) - W_s(\omega)) \quad (2.4)$$

2.2 Sobol-Hoeffding Decomposition

Considering process variation and noise, the circuit dynamics can be lumped in the form of a System of Stochastic Recurrence Equations (SSRE) given in Equation (2.4) for $t \in [0, T] \doteq \tau$.

$$\bar{X}_{s+\Delta s}(\omega) = \bar{X}_s(\omega) + C(\bar{X}_s; P)\Delta s + \sigma(\bar{X}_s; P)(W_{s+\Delta s}(\omega) - W_s(\omega)) \quad (2.5)$$

where W is a Wiener process which reflects the random circuit behavior due to uncertainties, C is the drift function, and σ is the diffusion coefficient. The process variation effect is represented as a random variable P with known probability law (extracted from the technology library) in both the drift and diffusion coefficient. The circuit behavior can be seen as a function of W and P: $X_{s+\Delta s} = X(s, W, P)$. Thus, we want to investigate the respective impact of the circuit uncertainty $\omega(t)$ and the parameters uncertainties P on the circuit performances. In the sequel, we recall the Sobol-Hoeffding Decomposition (SHD).

Definition 2.2.1 *(L_2 functions) $L_2(\mathcal{U}^d)$ is the space of real-valued squared integrable functions over the d-dimensional hypercube $\mathcal{U}$:*

$$X : p \in \mathcal{U}^d \rightarrow X(p) \in \mathbb{R},$$
$$X \in L_2(\mathcal{U}^d) \Leftrightarrow \int_{\mathcal{U}^d} X(p)^2 dp < \infty \tag{2.6}$$

$L_2(\mathcal{U}^d)$ is equipped with the inner product $< ., . >$:

$$\forall X, Y \in L_2(\mathcal{U}^d),$$
$$< u, v > := \int_{\mathcal{U}^d} X(p)Y(p)\ dp \tag{2.7}$$

The weighted space $L_2(A, \rho)$ is an extension of L_2 where:

$$P \in \mathcal{A} = A_1 \times A_2 \times \cdots \times A_d \subseteq \mathbb{R}^d,$$
$$\rho : P \in \mathcal{A} \rightarrow \rho(P) \geq 0,$$
$$\rho(P) = \rho_1(p_1) \times \cdots \times \rho_d(p_d)$$

Here, ρ denotes the probability density function of the circuit parameters random vector P with mutually independent components.

Theorem 1 *Any $X \in L_2(A, \rho)$ (see Definition 2.2.1) admits a unique hierarchical orthogonal decomposition. Let $P = (p_1, \cdots, p_d)$ in $\mathbb{R}^d$, the decomposition consists in writing the $X(P)$ as the sum of increasing dimension functions [52]. The expansion in*

Equation (2.9) *exists and is unique under one of the following orthogonality conditions:*

$$\int X_u(p_u) d\rho_{P_i} = 0 \qquad \forall i \in u, u \subseteq \{1, \cdots, d\}$$

or

$$\int X_u(p_u) X_v(p_v) d\rho_P =< X_u, X_v >= 0 \quad \forall u, v \subseteq \{1, \cdots, d\}, u \neq v$$

The independence of the inputs and the orthogonality property in Equation (2.9) ensure the global variance decomposition of the output $X(P)$ as follows:

$$\begin{aligned}
\mathbb{V}[X(P)] &= \mathbb{E}[(X(P) - X_0)^2] \\
&= \mathbb{E}[(\sum_{\{i_1, \cdots, i_d\} \subset \{1, \cdots, d\}} X_{i_1, \cdots, i_d}(P_{i_1, \cdots, P_{i_d}})^2] \\
&= \sum_{\{i_1, \cdots, i_d\} \subset \{1, \cdots, d\}} \mathbb{E}[(X^2_{i_1, \cdots, i_d}(P_{i_1, \cdots, P_{i_d}})] \\
&= \sum_{i \neq \emptyset, i \subseteq \mathcal{D}} \mathbb{V}[X_i], \qquad \mathbb{V}[X_i] =< X_i, X_i >
\end{aligned}$$

$\mathbb{V}[X_i]$ is interpreted as the contribution to the total variance $\mathbb{V}[X(P)]$ of the interaction between parameters $p_{i \in \mathcal{D}}$. Hence, the Sobol-Hoeffding variance decomposition provides a very useful and rich means of analyzing the respective contributions of individual or set of parameters to the circuit output variability. For instance, it partitions the output variance amongst the uncertain factors of the circuit model. Given the structure of the circuit model described in Equation (2.5), the hierarchical orthogonal Sobol-Hoeffding Decomposition (SHD) of X gives:

$$\begin{aligned}
X(\omega, P) &= \bar{X} + X_\omega(\omega) + X_P(P) + X_{\omega,P}(\omega, P), \forall t \in \tau \\
\mathbb{V}[X] &= \mathbb{V}[X_\omega] + \mathbb{V}[X_P] + \mathbb{V}[X_{\omega,P}]
\end{aligned}$$

Therefore, it is possible to determine the global sensitivity analysis as sensitivity measures that define the fraction of variance due to individual effects as well as their interactions. Figure 2.1 illustrates the total variance decomposition from the uncertainty variation space (shown on the left side) to the circuit performance space (depicted on the right side) due to noise and process variation. As it can be remarked, the total performance variance is decomposed into: the main contribution of noise only ($\mathcal{S}_\omega$), the main contribution of process variation only ($\mathcal{S}_P$), and the total contributions of the interactions noise and process variation ($\mathcal{S}_{\omega,P}$).

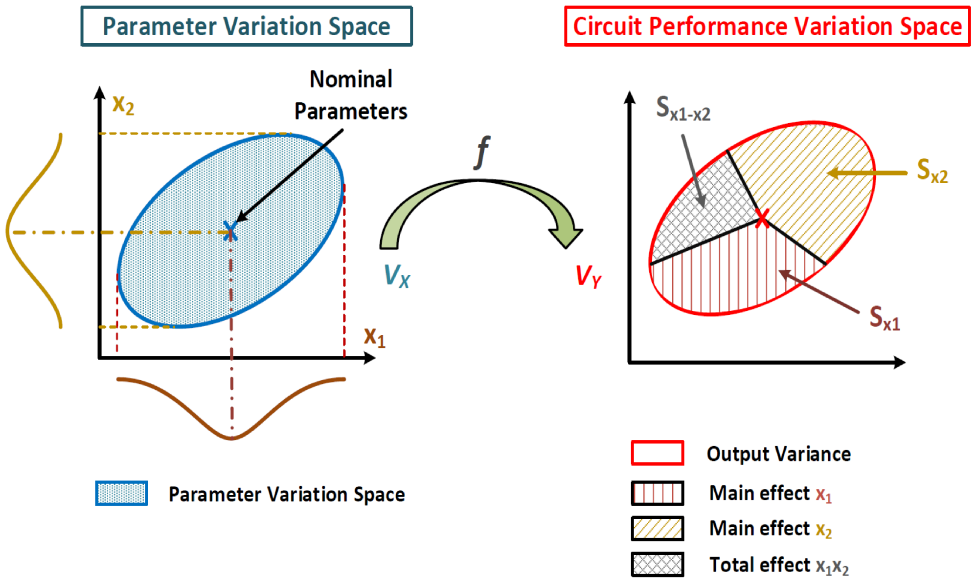

Figure 2.1: Illustration of the global sensistivity analysis concept in a 2-D parameters space

$$\mathcal{S}_\omega = \frac{\mathbb{V}[X_\omega]}{\mathbb{V}[X]}, \quad \mathcal{S}_P = \frac{\mathbb{V}[X_P]}{\mathbb{V}[X]}, \quad \mathcal{S}_{\omega,P} = \frac{\mathbb{V}[X_{\omega,P}]}{\mathbb{V}[X]} \tag{2.8}$$

$$X(P) = X(p_1, \ldots, p_d) = X_0 + \sum_{i=1}^{d} X_i(p_i) + \sum_{i=1}^{d} \sum_{j=i+1}^{d} X_{i,j}(p_i, p_j) \tag{2.9}$$

$$+\sum_{i=1}^{d}\sum_{j=i+1}^{d}\sum_{k=j+1}^{d} X_{i,j,k}(p_i,p_j,p_k)+\ldots+X_{1,\ldots,d}(p_1,\ldots,p_d)$$

2.2.1 Parametric Sensitivity Analysis

Consider x as a set of d independent random parameters which follow a certain distribution on U^d, and $f(x)$ a circuit performance depending on these parameters. It is assumed that f is a second order random variable $f \in L_2(U^d)$. Therefore, the circuit performance of interest f has a unique Sobol-Hoeffding decomposition. Because of the orthogonality of the Sobol-Hoeffding decomposition, the variance of the circuit performance can be decomposed as:

$$V[f]=\sum_{i\subseteq D}^{i\neq\emptyset} V[f_i], V[f_i]=<f_i,f_i> \tag{2.10}$$

where $V[f_i]$ stands for the contribution to the total variance $V[f]$ of the interaction between the parameters x_i. Therefore, the Sobol-Hoeffding decomposition is a rich means of analyzing the respective contribution of individual or sets of parameters to circuit performance variability. However, a more abstract characterization is required to replace the 2^d-1 actual contributions which lead to an intractable number of contributions as d increases.

2.2.2 Sensitivity Indices

To facilitate the prioritization of the respective influence of each parameter x_i, the partial variances $V[f_i]$ are normalized by $V[f]$ to obtain the sensitivity indices:

$$S_i(f)=\frac{V[f_i]}{V[f]}\leq 1, \sum_{i\subseteq D}^{i\neq\emptyset} S_i(f)=1 \tag{2.11}$$

The order of the sensitivity indices S_i is equal to $|i|=Card(S_i)$.

2.3 Statistical Hypothesis Testing

Hypothesis testing [53] uses statistics to make decisions about the acceptance or the rejection of some properties based on data from random samples. In this technique, the property of interest is formulated as a null hypothesis (H_0) which is tested against an alternative hypothesis (H_1). If we reject H_0, then the decision to accept H_1 is made.

Definition 2.3.1 *Given the property $\mathcal{P}$ within the ambit of a null hypothesis H_0, a significance level α, and a test statistic T, hypothesis testing is the process of verifying whether a system $\mathcal{C}$ satisfies H_0 with a probability greater than or equal to α (i.e., $\mathcal{C} \models Pr(T) \geq \alpha$).*

There are two approaches for making this statistical decision regarding a null hypothesis. The first approach is the *rejection region approach* and the second is the *probability value approach* (a.k.a. p-value approach). Regardless of the approach adopted, the conclusions drawn from the two approaches are exactly the same. The prior steps to conduct hypothesis testing:

1- Setting up null and alternative hypotheses.

2- Stating the level of significance α.

3- Calculating the appropriate test statistic.

Depending on the number of null hypotheses to be tested, hypothesis testing techniques can be classified to single hypothesis testing approach and multiple hypothesis testing approach.

2.3.1 Single Hypothesis Testing

Hypothesis testing of a single null hypothesis H_0 is discussed in this section. As depicted in Figure 2.2, single hypothesis testing can be one or two sided. The one

side test is classified into:

- Upper test when a large value of the test statistic provides evidence for rejecting H_0 (see Figure 2.2 (b)).
- Lower test when a small value of the test statistic shows proof of H_0 rejection (see Figure 2.2 (c)).

The two sided test (shown in Figure 2.2 (a)) is determined by a bounded region $[x_1, x_2]$ as follows:

$$H_0 : P(x_1 < X < x_2) = P(X < x_2) - P(X < x_1) = 1 - \alpha \tag{2.12}$$

The hypothesis testing procedure can be summarized as follows:

1. Elucidate the property to be verified and formulate it as H_0 and H_1.
2. Specify the appropriate level of significance α and determine the type of the test, namely, upper test, lower test or two sided test.
3. Select the appropriate test statistic.
4. Compute the critical region or p-value of the test statistic.
5. Compute the test statistic of the observed value for the original data.
6. Make the decision of accepting or rejecting the null hypothesis H_0. If the computed test statistic falls in the critical region, then the null hypothesis is rejected, otherwise H_0 is accepted.

The decision is drawn with certain probability of error for a specific confidence level as summarized in Table 2.1. Basically, the performance criteria of this approach is related to two types of errors:

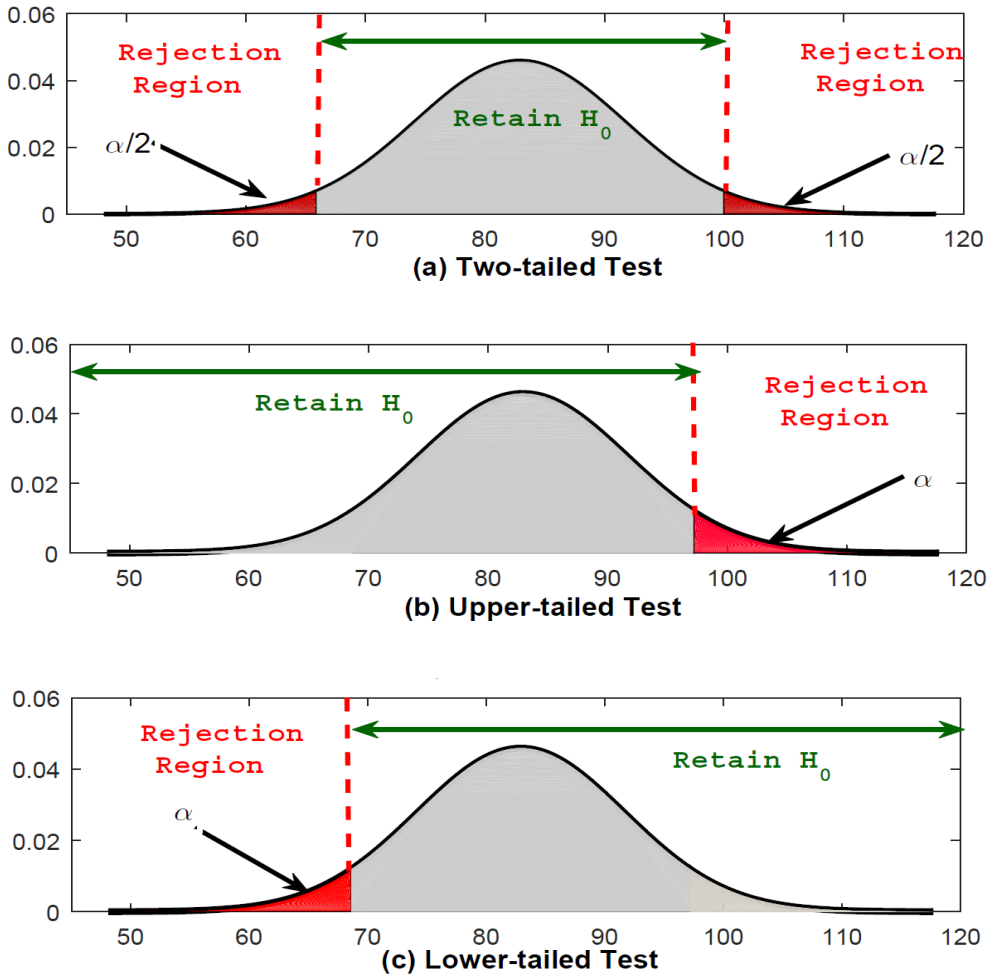

Figure 2.2: Hypothesis testing concept

Type I error (α) or false positive, the null hypothesis H_0 is true but the decision based on the testing process erroneously rejected it. In other words, it represents the probability of accepting H_0 when H_1 holds.

Type II error (β) or false negative, the null hypothesis H_0 is false but the testing process concludes that it should be accepted. In other words, it corresponds to the probability of accepting H_1 when H_0 holds.

In Table 2.1, we define T and V as the probabilities of Type I and Type II errors, respectively.

Table 2.1: Outcomes classification for single hypothesis testing

	Passed	Failed
Good Circuit	✓	T
Defective Circuit	V	✓

2.3.2 Multiple Hypothesis Testing

A multiple hypothesis testing enables to avoid the problem of multiple tests that would arise if we test the effect of different variables on different properties separately. In the sequel, we detail the multiple hypothesis testing procedure.

Definition 2.3.2 ***(Null Hypotheses)*** *In order to cover a broad performance verification problems, we define m null hypotheses in terms of a collection of acceptance region for certain performances metric with distribution κ.*

$$\mathcal{A}_{p_j} \subseteq \mathcal{A}_p, j = 1, \cdots, m$$

The m null hypotheses are defined as $H_{0_j} \equiv \mathrm{I}(\mathrm{k} \in \mathcal{A}_{p_j})$ and the corresponding alternative hypotheses denoted by $H_{1_j} \equiv \mathrm{I}(\mathrm{k} \notin \mathcal{A}_{p_j})$ are the opposite, complementing H_{0_j}. Thus, H_{0_j} holds, i.e., $H_{0j} = 1$, if $\mathrm{K} \in \mathcal{A}_{p_j}$ and is rejected otherwise.

Multiple hypothesis testing is based on a simultaneous statistical inference of the probability that a set of properties G are satisfied with a certain level of confidence α. When conducting the hypothesis testing, the number of null hypotheses, m, is known in advance and corresponds to the number of properties of interest G. However, the number of true null hypotheses H_{0_j} m_0 and false null hypotheses m_1, respectively with $m = m_0 + m_1$, have to be determined. Table 2.2 summarize the possible outcomes when verifying m hypotheses simultaneously. A failure to compensate for multiple verifications can result in two types of erroneous inferences denoted by Type I error and Type II error. As shown in Table 2.2, we define T and V as the probabilities of

Table 2.2: Possible outcomes classification for m hypotheses testing

	Passed	Failed	Total
Good Circuit	✓	T	m-R
Faulty Circuit	V	✓	R
Total	m_0	$m - m_0$	m

Type I and Type II errors, respectively.

$$V = P(\text{Type I error}) = P(\text{reject } H_{0_i} | H_{0_i} \text{ true}) \quad \text{(False Positive)}$$

$$T = P(\text{type II error}) = P(\text{reject } H_{0_i} | H_{1_i} \text{ true}) \quad \text{(False Negative)}$$

Type I and Type II errors are correlated and in direct competition with each other. For instance, computing a subset $\mathcal{R} \subseteq \mathcal{H}$ of hypotheses to reject that has fewer Type I errors usually results in more Type II errors.

2.4 Yield Estimation

Yield is a measure of integrated circuit (IC) failure referring to the fraction of integrated circuits which survive through the manufacturing line. In other words, it represents the ratio of fully functional circuits that comply with specification and standards to the total number of manufactured ICs. It can be classified based on the failure type taxonomy to [54]:

- **Catastrophic yield loss** caused by functional failures such as open or short circuits which cause the circuit to not work at all.

- **Parametric yield loss** caused by a variation in one or a set of circuit parameters due to process variations. The circuit, in this case, is functional but it violates certain power and/or performance criteria.

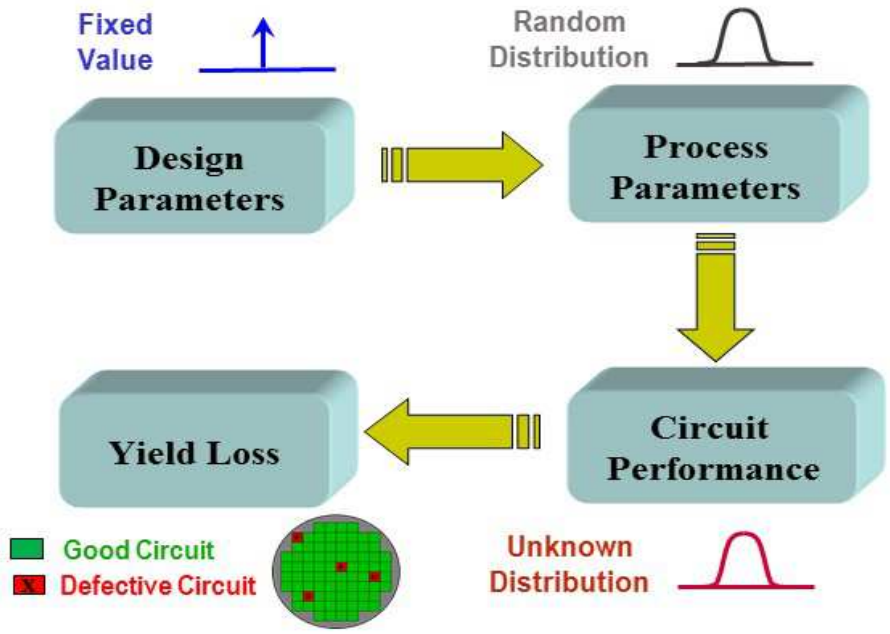

Figure 2.3: Illustration of the process variation effect on circuit yield

For analog and mixed-signal circuits, parametric yield loss is significant and represents the dominant part of the total yield loss. Hence, in this thesis, we are mainly concerned with the parametric yield loss for both single and multiple-parametric yield loss. Figure 2.3 summarizes the process variation concept and visualizes the relationship between process variation and the yield loss.

Given a circuit topology, the circuit performances of interest g (e.g., gain of an amplifier, oscillation frequency of an oscillator, etc.) are functions of the circuit responses which are in turn functions of the circuit parameters. The performance constraints can be expressed in the following standard form:

$$g_i(R(p)) \leq 0 \quad i = 1, 2, \cdots, m \tag{2.13}$$

where $p \in \mathbb{R}^n$ stands for the circuit parameters, $R : \mathbb{R}^n \rightarrow \mathbb{R}^m$ is the circuit response vector, m is the total number of performance constraints, g_i is the i-th performance metric. Without loss of generality, any performance constraints can be reformulated in

the standard form given in Equation (2.13). For instance, $g_i(R(p)) \leq C$, $g_i(R(p)) \geq C$, $g_i(R(p)) \in [C_{min}, C_{max}]$ can be expressed as: $g_i(R(p)) - C \leq 0$, $C - g_i(R(p)) \geq 0$, $(g_i(R(p)) - C_{min} \leq 0$ & $C_{max} - g_i(R(p)) \geq 0)$, respectively.

Given the performance constraints in Equation (2.13), each element of g_i has a certain tolerated lower and/or upper bound. Hence, in the statistical parameter space, certain part of the performance distribution will be cut off wherein a part of the circuit parameter variation falls out of the acceptance region bordered by the specification limits set by the designers given in Equation (2.13). The fraction of the distributions which are within the performance specification is called *acceptance region* A_p and it is mathematically defined as follows:

$$A_p = \{p \mid g_i(R(p)) \leq 0, \quad i = 1, 2, \cdots, m\} \tag{2.14}$$

Figure 2.4 is an illustration of the acceptance region for a single performance metric in a two-dimensional parameter space ($p = 2$). The remaining circuit performance regions in red represent the failure regions, i.e., the regions of the parameters space where the performances are not satisfied.

Parametric yield is the percentage of circuits that satisfy the performance specification considering statistical parameter variations. In other words, it is the probability of satisfying the parametric requirements, i.e., the parameters $p*$ lead to acceptable performance and so belong to the acceptability region A_p.

$$Y(x) = P\{p \in A_p\} = \int_{R^n} \phi_p(p) f_p(p, x) dp = E_p\{\phi_p(p)\} \tag{2.15}$$

where $P\{.\}$, $\phi_p(p)$, and $E_p\{.\}$ denote the probability, an indicator function, and the expectation w.r.t random variable p, respectively. The indicator function ϕ is determined by the performance specification and its corresponding acceptance function described as:

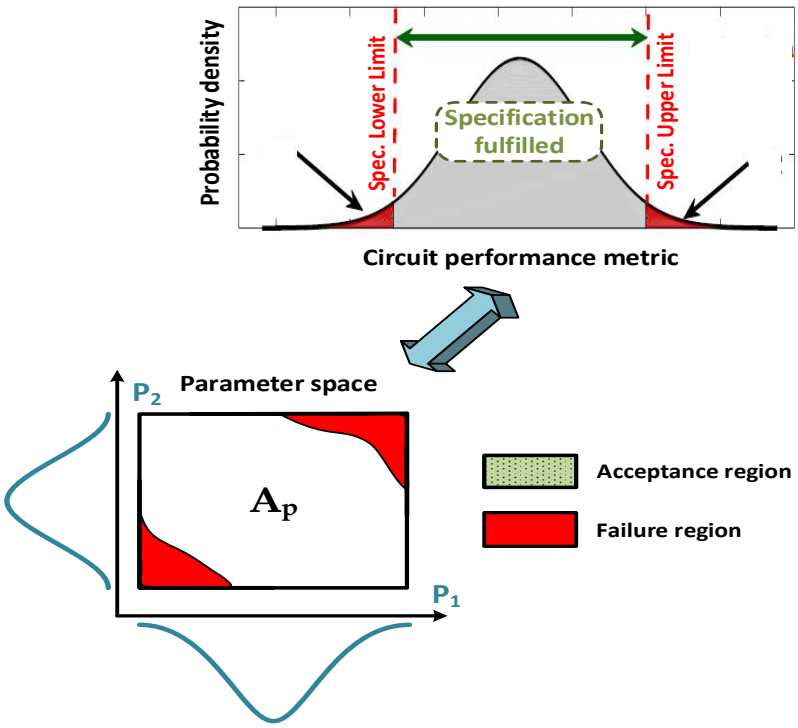

Figure 2.4: Geometrical illustration for 2-D space parameter and a single circuit performance

$$\phi(p) = \begin{cases} 1 \text{ (Pass)} & \text{if } p \in A_p \\ 0 \text{ (Fail)} & \text{otherwise} \end{cases}$$

The n-dimensional integration in Equation (2.15) has a canonical form and can be numerically approximated to:

$$Y_{MC} = \frac{1}{N} \sum_{k=1}^{N} \phi_{\xi}(\xi) \tag{2.16}$$

where Y_{MC} stands for Monte Carlo (MC)-based yield estimator, ξ are independently drawn random samples from the parameter uncertainty domain and N is the MC sample size. The yield estimation formulated in Equation (2.15) is for a single performance metric. A generalization of the yield expansion in the case of multiple performances m-Dimension yield probability is defined as follows:

$$Yield = P(p \in (\bigcup_{i=1}^{m} A_p^i)) \tag{2.17}$$

By applying the inclusion-exclusion principle [55] to Equation (2.17), the total yield for m performance merits is expressed as:

$$\begin{aligned} Yield &= \sum_{i=1}^{m} P(p \in A_p^i) - P_{overlap} \\ P_{overlap} &= -\sum_{i<j} P(A_p^i \cup A_p^j) + \sum_{i<j<l} P(A_p^i \cup A_p^j \cup A_p^l) \\ &\quad -\cdots + (-1)^{m-1} P(p \in (\bigcap_{i=1}^{m} A_p^i) \end{aligned} \tag{2.18}$$

Calculating the yield is equivalent to calculating the failure probability $P_{failure}$ (a.k.a. yield loss). They are related by the following relationship:

$$P_{failure} = 1 - Yield \tag{2.19}$$

Typically the yield should be high and therefore the failure probability should be low for faster time to profit.

Chapter 3

Surrogate based Optimization

In this chapter, we focus on analog nominal sizing. It equally denotes the performance maximization problem in nominal conditions. Nominal sizing is a standpoint of circuit sizing which in turn is a main step in the analog IC flow. This is a critical design stage that aims at determining circuit geometry, namely transistor width (W) and length (L), and resistor, capacitor, and inductor nominal values. Circuit sizing is mostly done using either knowledge based or optimization based approaches. This chapter mainly focuses on optimization based circuit sizing. Particularly, we present a mixed equation-based and simulation-based optimization methodology. It has the advantage to allow a flexible sizing procedure between different abstraction levels. We demonstrate the feasibility and flexibility of the proposed method on a ring oscillator and a two stage operational amplifier.

3.1 Space Mapping based Circuit Sizing

We assume that the circuit topology has been selected. The proposed analog optimization methodology for circuit sizing is shown in Figure 3.1. As it can be noticed,

the proposed methodology consists of two main steps. The first step is the sensitivity analysis stage wherein promising sub-regions of the design space are located. It consists first to subdivide this design space to sub-regions. Afterwards, a regional sensitivity analysis is conducted in order to quantify the dependence of the circuit transient performances on the corresponding sub-region in the feasible design space.

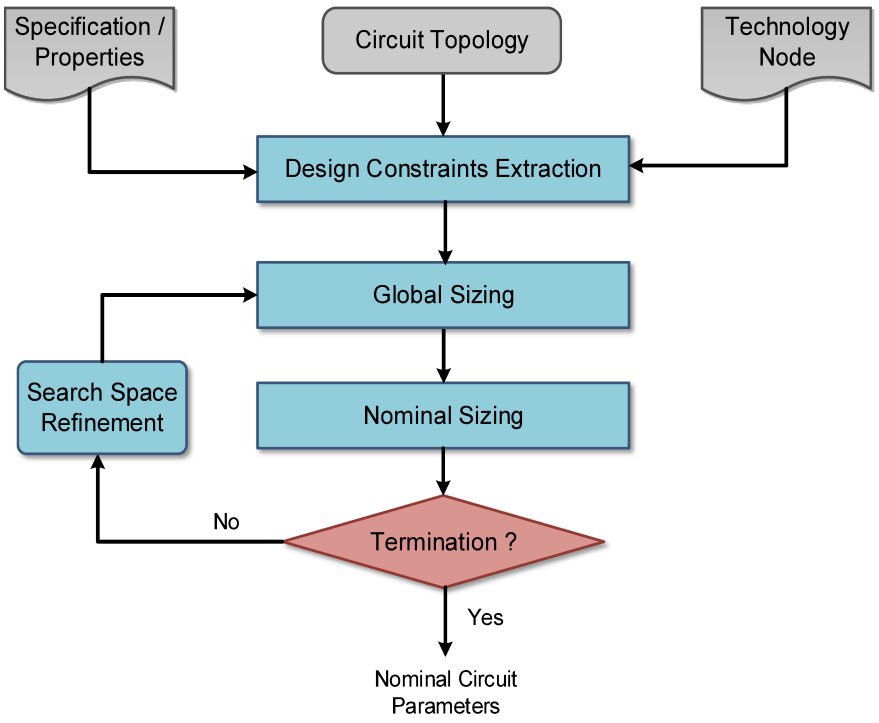

Figure 3.1: Proposed circuit sizing methodology

The sensitivity analysis is performed globally in the design space and not locally as usually done with Spice. This can be justified by the following reasons:

1. Local sensitivity is carried out under the assumption of linear circuit model. Hence, it cannot be applied to complex nonlinear circuit models especially in which there are nonlinear interactions between parameters.

2. Local sensitivity is adequate to measure sensitivity only for nominal circuit

parameters and thereby the performance of the circuit is studied only locally in the design space.

3. Global sensitivity explores the entire possible range of the design space while accounting for interactions between the different circuit parameters without depending on the stipulation of a single circuit parameter feasible solution.

Once the sensitivity analysis is performed, the feasible design sub-regions are classified into *promising* and *non-promising* design sub-spaces in order to facilitate the search for the optimal design parameters. The second step is the nominal circuit parameters selection on the retrieved promising feasible design sub-spaces. The nominal circuit sizing is typically done using knowledge based approaches based on the design experience and expertise. It basically consists of deriving analytical circuit equations that relate circuit performances to device characteristics and parameters. Although this approach worked well for old technologies, it is no more suitable for nano-scale modern technologies. For instance, the modeling of short channel effects makes the circuit equations for large and small signal analysis extremely difficult to derive. Consequently, using simplified equations thereof yields to design solutions that are far from the actual optimal ones. Hence, an optimization based approach is adopted in this thesis. It transforms the circuit sizing procedure to a general optimization problem. The circuit performances are cast to a cost function, and the promising feasible design sub-spaces are explored automatically by an optimization engine in the search of optimal design parameters. If the extracted design point does not fullfil the accuracy requirement, the optimization is repeated until it accomplishes a stopping criterion (i.e., all design specifications have been met). In this case, the design point is considered optimal and the sizing procedure runs are stopped.

3.1.1 Optimization based Circuit Sizing

The task of sizing an analog circuit can be formulated as an optimization problem to substitute a design plan. The circuit optimization corresponds to the process of searching for the circuit parameters value under which the best circuit performance is expected with respect to the desired specifications. Mathematically, this process can be formulated as a nonlinear constrained optimization problem for n variables with m constraints as follows:

$$\begin{aligned} \min_{x} \quad & f(x) && x = (x_1, x_2, ..., x_n) \\ \text{such that} \quad & c_i(x) \leq 0 && i = 1, ..., m \\ & h_i(x) = h_t && i = 1, ..., n \\ & x_l \leq x \leq x_u && i = 1, ..., n \end{aligned} \tag{3.1}$$

where *f(x)* represents the performance function to be optimized according to n circuit parameters x_i, h is the equality constraint which mainly refers to Kirchhoff's Current Law (KCL) and Kirchhoff's Voltage Law (KVL) equations. x stands for the feasible design space vector of dimension n, and x_l and x_u are its lower and upper bounds, respectively. The vector $c_i(x)$ refers to design constraints such as gain, phase margin and slew rate. Table 3.1 summarizes all possible conflicting sizing rules.

For the sake of generality, it is assumed that the optimization problem corresponds to the minimization of the performance function. For example, the objective of the optimization is to determine the sizing of all devices (e.g., transistors width, capacitors, etc.) such that the power consumption is the smallest possible while satisfying all design constraints (e.g., slew rate constraints). However, many challenges arise when optimizing an AMS circuit because its objective function can be very expensive

Table 3.1: Sizing rules and constraints

Geometrical	**Electrical**
Transistor Length/Width	Design works at the expected region. (e.g., saturation region)
Functional	**Robustness**
Operate the desired analog function (e.g., transistors working on saturation)	Define the design margins in order to decrease the sensitivity to process variation and operation conditions. It closely depends on the technology node. (e.g., min length/width/area)
Equality	**Inequality**
Matching constraints. Design parameters have the same values in symmetric designs. (e.g., $L_1 = L_2$)	Upper and lower bounds of the electrical or geometrical circuit quantities (e.g., $V_{DS} \geq V_{GS} - V_{th}$ for transistors in saturation)

to extract, evaluate, and is most of the time non-differentiable. Indeed, the extraction of the equation capturing the behavior of the circuit topology is very complex and prohibitive. Furthermore, the simplification required to obtain a closed-form solution of the optimization problem compromise the accuracy and completeness of the sizing problem. Conversely, simulation based techniques rely on simulation to evaluate the circuit performance during the optimization process offering good accuracy, generality, and ease of use. Clearly, a good compromise lies in mixing both techniques. It is also worth mentioning that a wide feasible design space enables the optimizer to find a better circuit, but the convergence is very slow, thus the time required to find optimal circuit parameters can be very long. It is therefore important to limit the optimization search on sub-regions of the design space where potential global circuit parameters exist. The question that arises is, " *how to shrink the feasible design space and locate the promising design subspaces?*"

3.1.2 Global Circuit Sizing

The aim of the global circuit sizing is to confine the sizing search to promising design subspaces and thereby to cut off non-promising parts from the overall feasible design space. These promising design subspaces will be used thereafter to prevent the optimization approach from entering unrewarding regions in the design space. In other words, it guides the circuit optimization procedure to focus on regions promising optimal design solutions.

The approach is summarized in Algorithm 3.1. It is based on transient regional sensitivity analysis [56] which is a variant of the global sensitivity analysis theory.

Algorithm 3.1 Global Circuit Sizing

Require: D_{init}, F, S
1: $D_0^i \leftarrow$ Divide search space (S)
2: $\Omega_{o_T} = F$
3: $\Omega_{no_T} = \emptyset$
4: **for all** $i \leftarrow 1$ *to* S **do**
5: **while** stopping criteria is unsatisfied **do**
6: Initialize $p_i^* = center(D_0^i)$, f_i^{min}, f_i^{max}
7: $[d_{n,no}, pvalue] \leftarrow$ Run Kolmogorov-Smirnov method (F, D_0^i)
8: $[\Omega_{o_i}, \Omega_{no_i}] \leftarrow$ Identify potential promising sub-regions $(d_{n,no}, p - value, p_{threshold})$
9: **return** $\Omega_{o_T} = \cup_{i=1}^{S} \Omega_{o_i}$, $\Omega_{no_T} = F \cap \Omega_{o_T}^c$

D_{init} is the initial feasible design space, F the set of objective functions, S the number of sub-regions. The global circuit sizing procedure starts by subdivising the feasible design space into S sub-regions (line 1). An illustration of the proposed global sizing feasible design space subdivision is shown in Figure 3.2 for two iterations. It can be noticed that the design space subdivision is performed in such a way that previous sensitivity analysis is at the center of the new sub-regions. Thereafter, a regional sensitivity analysis based on Kolmogorov-Smirnov is conducted (line 7) wherein high

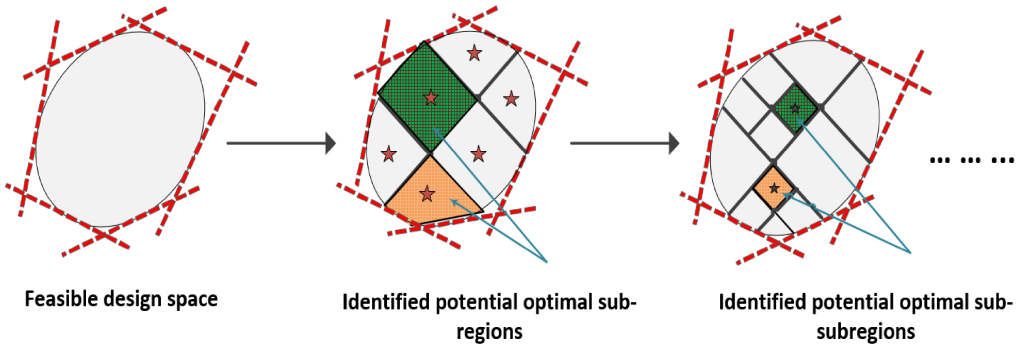

Figure 3.2: Global circuit sizing iterations

sensitivity values designate the most promising design sub-regions. It splits the sub-regions depending on whether the associate circuit performance is above or below a certain threshold ($p_{threshold}$). In the sequel, we detail the Kolmogorov-Smirnov based regional sensitivity method. The Kolmogorov-Smirnov is based on a two-sample test hypothesis testing method (see Equation 3.2) that is carried out for each design sub-region independently. Based on predefined performance limits (f_i^{min}, and/or f_i^{max}), the predicted performances from each design sub-region can be categorized into two subsets as shown in Figure 3.3:

- *Optimal design sub-regions* (denoted as R_o)
- *Non-optimal sub-regions* (denoted as R_{no})

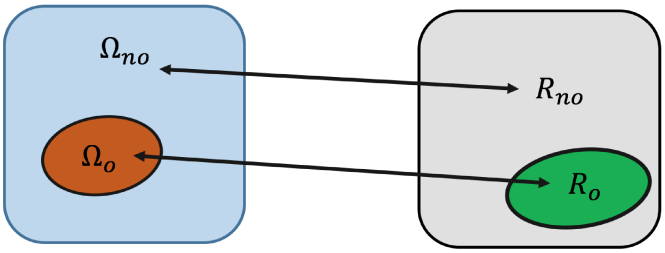

Figure 3.3: Design sub-regions classification

In what follows, we denote by $(\Omega_o = p^i|R_o)$ the circuit parameter p_i region that leads to an optimal design sub-region and $(\Omega_{no} = p^i|R_{no})$ the circuit parameter p_i region that leads to a non-optimal design sub-region, respectively. A conceptualization of this sub-region categorization is depicted in Figure 3.3. The Kolmogorov-Smirnov method is statistically formulated as follows:

$$H_0 : f_{\Omega_o}(p_i \mid R_o) = f_{\Omega_{no}}(p_i \mid R_{no}) \tag{3.2}$$

$$H_1 : f_{\Omega_o}(p_i \mid R_o) \neq f_{\Omega_{no}}(p_i \mid R_{no})$$

where f are probability density functions and $\Omega_o \cup \Omega_{no} = \Omega_T$ is the total design sub-region under analysis. The distance between the empirical cumulative distribution functions for both promising and non-promising sub-regions provides an index for the sensitivity of the design parameter p_i on the desired circuit performances. This sensitivity index is defined as follows:

$$d_{n,no}(p_i) = sup_y \parallel F_n(p_i \mid R_o) = F_{no}(p_i \mid R_{no}) \parallel \tag{3.3}$$

where F is the marginal cumulative probability function.

Figure 3.4 illustrates schematically the regional sensitivity index of the optimal and non-optimal design sub-regions for circuit parameter value p_i. The result of the Kolmogorov-Smirnov test is two measures, the sensitivity index $d_{n,no}$ (a.k.a. D-statistic) and the p-value. $d_{n,no}$ quantifies the distance between the two marginal cumulative probability functions F_n and F_{no}, whereas the p-value defines the significance level of the differences of the latter. The sensitivity index $d_{n,no}$ varies between 0 and 1 and the lower its values is, the less influential parameter p_i. In particular, if $d_{n,no} = 0$, then p_i has no influence on the circuit performance.

These two measures exhibit an inverse relationship. In fact, a large $d_{n,no}$ (or equivalently a small p-value) indicates an important design point in the predefined feasible

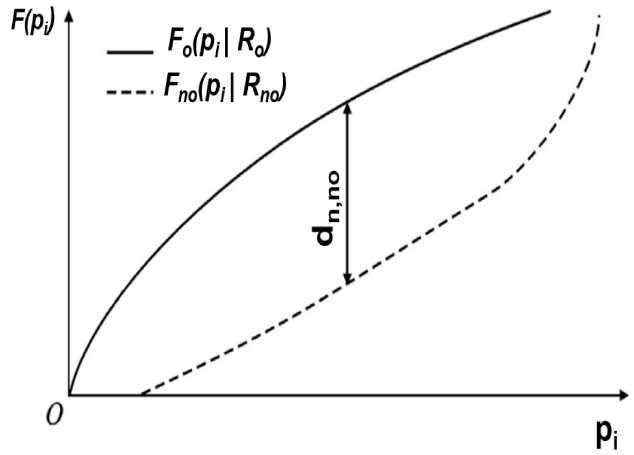

Figure 3.4: Sensitivity index for circuit parameter p_i

design-sub-region. In this thesis, the threshold p-value at which the circuit performance is deemed promising is set to $p_{threshold} = 0.01$ as recommended in the literature [57].

Next, depending on the obtained p-value the sub-region D_0^i is deemed promising or non-promising sub-region of the design space (line 8 of Algorithm 3.1). This p-value reflects the contribution of the circuit parameter p_i to the mean and variance of the circuit performance f. Finally, we confine the feasible design space to these promising design sub-regions Ω_{o_T} that has the potential of having an optimal design solution. It follows that the non-promising design sub-regions Ω_{no_T} wherein optimization is unrewarding are retrieved from the initial feasible design space.

The exhaustiveness feature of the underlying global sizing algorithm relieves the nominal sizing computations. It turns the complex computational task of circuit optimization into many sub-feasible design spaces based on sensitivity analysis. This way, the optimization is carried out only on the sub-optimal design space. Consequently, the search space is constrained to areas where meaningful solutions might be expected to be found. Thus, the computational effort overhead that plagues the simulation-based design space exploration and design optimization is greatly reduced.

3.1.3 Nominal Circuit Sizing

Once the reduced design space Ω_{o_T} is defined in the global circuit sizing step, nominal circuit sizing is performed on this reduced optimal design space (i.e., the design sub-space confined to the promising design sub-regions defined in Section 3.1.2). The aim of this nominal sizing step is to find the optimal design point (i.e., circuit parameters values) in the design space Ω_{o_T} that has the optimal circuit performances set by the specification requirements. The typical AMS circuits nominal sizing flow is illustrated in Figure 3.5. It consists of an iterative process between an optimization engine and a performance evaluation engine. In the optimization iteration, the candidate optimal design points, extracted from an equation based sizing approach, are generated by the optimization engine. The circuit performances for this candidate optimal design point are analyzed and fed-back to the optimization engine for the next iteration.

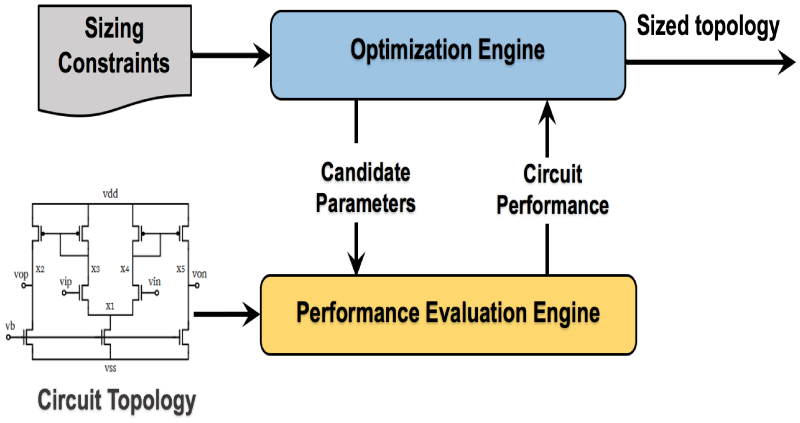

Figure 3.5: Typical analog IC sizing flow

This flow is obstructed by the high expense of the evaluation engine. In addition, the relation between the optimization design point figures and the circuit performances thereof is unknown, rendering this feedback approach inappropriate for design automation. As an alternative, we propose in this chapter a formally coupled optimization

and performance evaluation approach that is similar in spirit to formal equivalence checking as depicted in Figure 3.6. Indeed, the optimization is performed through verifying the equivalence between the circuit responses of the detailed and surrogate models over design point solutions. The coupling is performed through a space mapping approach between the optimization engine which is based on an equation based sizing and the evaluation engine, which is conversely a simulation based approach. This space mapping paradigm [58] was originally developed for microwave circuits optimization, and thereafter gave rise to an entire field of surrogate-based optimization approaches across several engineering disciplines. The two-fold clear benefits of the proposed approach are:

1) Stabilization of the iterative standard sizing process through reducing the simulation overhead.

2) Guaranteed convergence to the optimal design solution for arbitrary geometries.

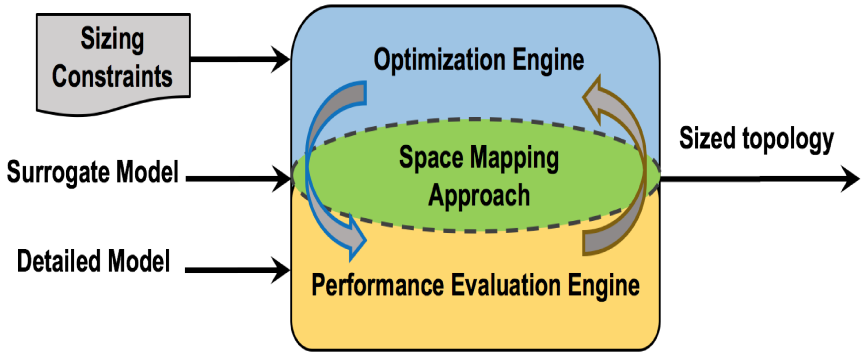

Figure 3.6: Proposed space mapping based nominal sizing flow

In the sequel, we detail our proposed surrogate based space mapping based optimization procedure. The optimization scheme is conducted in a cross detailed-to-surrogate model level driven way referred to as *cross-level mixed equation-simulation based optimization*. For instance, it is performed with an interplay between two different representations of the circuit at different abstraction levels, mainly a detailed

complex model and a behavioral surrogate model. The essence of this method is to use the behavioral model to gain information about the detailed circuit model and to apply this in the search for an optimal solution of the latter. The capability to switch between the two circuit models helps to harness the best features of each of the circuit model. By doing so, our space mapping based optimization method eliminates the need for sequential optimization of each AMS model separately and so breaks the re-design loop and so reduces it by jointly optimizing the two circuit models while maintaining the accuracy in a single step. Besides the runtime and accuracy benefits of the proposed technique, the hierarchical sizing is more in line with the industry practice and how a designer would tackle the sizing of large AMS circuits. Figure 3.7 shows the underlying proposed space mapping based nominal sizing methodology. As it can be seen, it is broadly comprised of four steps:

1. Behavioral circuit model optimization
2. Detailed model parameter simulation
3. Space mapping function refinenment
4. Detailed model circuit parameters sizing

First, the behavioral model is optimized through the search in the optimal design space Ω_{o_T} computed in the previous global circuit sizing step. Then, the resulting optimal parameters of the behavioral model x_b^* are mapped into their corresponding detailed level parameters x_d. x_d and x_b are mapped using a space mapping function $P : X_d \rightarrow X_b$ which is defined by:

$$x_b = P(x_d) \tag{3.4}$$

such that

$$\|R_d(x_d) - R_b(x_b)\| \leq \varepsilon \tag{3.5}$$

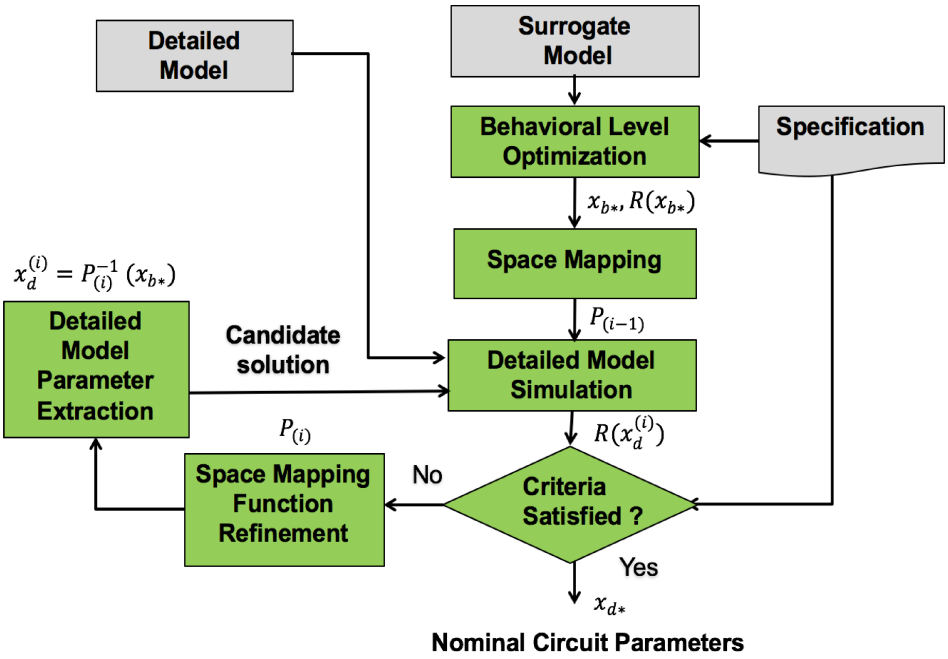

Figure 3.7: Proposed nominal sizing methodology

where R_d and R_b refer to the circuit responses to the detailed and behavioral level models, respectively and ε is a predefined tolerated error. The mapping is established through an iterative process. At the j^{th} iteration, we expand the circuit level parameter set to contain m_j points which are chosen by perturbation around the optimal behavioral model parameters x_b^*. These m_j points are then used to establish a mapping function refinement $P^{(j)}$ which is used to estimate the new detailed model parameter as follows:

$$x_d^{(m_{j+1})} = P^{(j)^{-1}}(x_b^*) \tag{3.6}$$

Algorithm 3.2 summarizes the mapping function P computation at the j^{th} iteration. It is basically a linear combination of the detailed model response to the candidate design point solution $x_d^{(m_{j+1})}$. The least-square solution to the system of equation defined in line 10 determines the mapping function P at the iteration j. The

process continues iteratively until the satisfaction of the termination condition:

$$\|R_b(x_b^*) - R_c(x_d^{(m_{j+1})})\| \leq \varepsilon \tag{3.7}$$

Upon termination, $x_d^* = x_d^{(m_{j+1})}$ is set as the optimal circuit level design solution for the circuit parameters.

Algorithm 3.2 Space mapping function computation

Require: x_b, x_d, R_d, R_b, j
1: $n \leftarrow$ Compute size (x_d)
2: **if** j=1 **then**
3: $A = I(n, n)$
4: **else**
5: **for** $i \leftarrow 1$ *to* n **do**
6: $a_i \leftarrow$ Compute mapping coeifficient$(x_b(i), R_d(x_d(i)))$
7: Update A
8: $[C, D] \leftarrow$ Define new base$(x_b, R_d(x_d))$
9: $W \leftarrow$ Compute weighting matrix(A,D)$(x_b, R_d(x_d))$
10: $A_j^T = (D^T W^T W D)^{-1} D^T W^T W C$
11: $P = A_j^T$
12: **return** P

3.2 Applications

In this section, we present the results of the application of our surrogate based circuit optimization method on the example of a ring oscillator. We also test the efficiency of the proposed method for multi-objective optimization on a two-stage operational amplifier circuit. The detailed circuit models are designed and simulated in TSMC's 65 nm CMOS technology with BSIM4 transistor models. The behavioral circuit models and the proposed optimization based circuit sizing methodology are implemented in MATLAB R2013a [59]. In order to generate a solution in reasonable time, the maximum number of allowable simulation for our method is set to 300.

3.2.1 Ring Oscillator

We consider optimizing a three-stage ring oscillator circuit as shown in Figure 6.16. Ring oscillator is used as a fundamental block in many applications, such as a Voltage Control Oscillator (VCO) in phase locked loops, Radio Frequency (RF) circuits or microprocessors for clock generation and synchronization [35]. It is an important analog IC block and design structure that has been widely used to assess the efficiency of analog optimization and verification methods. The ring oscillator is a closed-loop chain of an odd number of inverters placed in series with a negative feedback to provide oscillation between the ground gnd=0V and the power V_{DD}=1V. To model the influence of the interconnect circuitry, an additional load capacity of C was used. Each inverter is composed of cascaded n-channel and p-channel transistors.

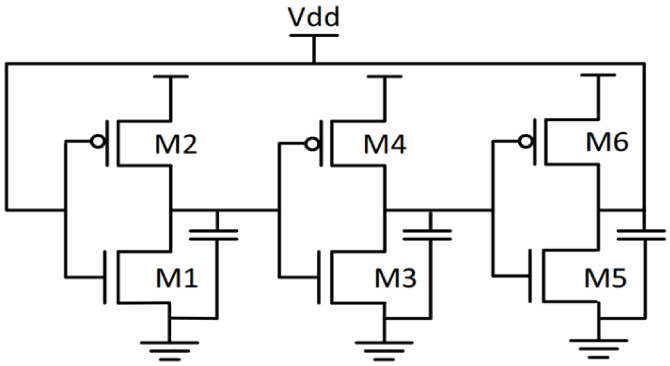

Figure 3.8: Three stage CMOS ring oscillator

The choice of the circuit design parameters should be made so that the circuit satisfies the oscillation fundamental frequency of f_{osc}=3.2 MHz. The three stage ring oscillator oscillation frequency is related to the transistors sizes through the following equation:

$$f_{osc} = \frac{I_D}{3\eta C_{Tot} V_{DD}} \quad \text{with} \quad C_{Tot} = \frac{5}{2} C_{ox}(L_p W_p + L_n W_n) \tag{3.8}$$

where I_D is the drain current flowing through the inverter stage, C_{Tot} is the total capacitance, C_{ox} is the oxide capacitance per unit area, and V_{DD} is the supply voltage. The length of all PMOS and NMOS transistors are set to 65 nm ($L = 65$ nm) as per technology file. Thus, the optimization problem will consist in computing the appropriate transistors widths. Applying the symmetry constraints, we will have $W_{p_2} = W_{p_4} = W_{p_6}$ and $W_{n_1} = W_{n_3} = W_{n_5}$. After performing the space mapping optimization method, the obtained optimal transistors widths are $W_{p_i} = 3$ μm and $W_{n_i} = 2.5$ μm.

In order to evaluate the performance of our proposed sizing methodology, we compare our results with other optimization based methods, namely Genetic Algorithm (GA) [60] and ANFIS [61] methods.

Table 3.2: Comparison with other techniques in terms of number of iterations

Optimizer	Obtained frequency
HSpice	3.207
GA [60]	3.06
ANFIS [61]	3.15
Our method	3.206

The obtained oscillation frequency performances are reported in Table 3.2. The performance of the sized circuit is also confirmed using Spice simulation. It can be observed that our method gives the best operating frequency compared to the other optimization methods with a very close figure to the Spice simulation based approach. It can be inferred that our mixed equation/simulation based optimization approach offers a superior accuracy to equation based methods while being very close to HSpice figures.

In Table 3.3, a comparison in terms of required number of iterations, runtime, speed-up, and relative error between the different above-mentioned methods is shown.

As it can be observed, our sizing scheme is found to be highly efficient. For instance, it significantly reduces the number of optimization iterations needed to converge to an optimal design solution compared to the ANFIS method. In addition, it offers a large speed-up gain of almost 12.5X compared to the HSpice simulation approach while having only 0.031% relative error in the computed oscillation frequency f_{osc}. Therefore, the gains of our proposed methodology are reflected not only in the good performances attained but also with a significant runtime saving. It is hence a good alternative to the existing optimization approach while integrating HSpice accuracy.

Table 3.3: Optimization results for ring oscillator

Optimizer	Total number of iterations	Runtime [h]	Speed-up Ratio	Relative Error (%)
HSpice	–	12.33	–	–
GA [60]	–	7.12	1.74X	4.58
ANFIS [61]	173	2.56	4.8X	1.77
Our method	68	0.58	12.62X	0.031

3.2.2 Two stage Operational Amplifier

As a second application, we consider a two-stage amplifier (op-am) as depicted in Figure 3.9. The circuit consists of eight transistors $\{M_i\}_{i=1}^{8}$, compensation and load capacitance and a reference bias current. The length of all transistors is set to 1μ m. In order to illustrate the design and optimization of the operational amplifier circuit, the list of specifications is summarized in Table 3.4. It is known that one of the main amplifiers performance characteristics is their gain. It follows that the aim of the optimization scheme for this application is to maximize the open-loop gain.

The Least Square Support Vector Machine SVM toolbox interfaced with MATLAB was employed for the behavioral circuit model using multivariate SVM regressor

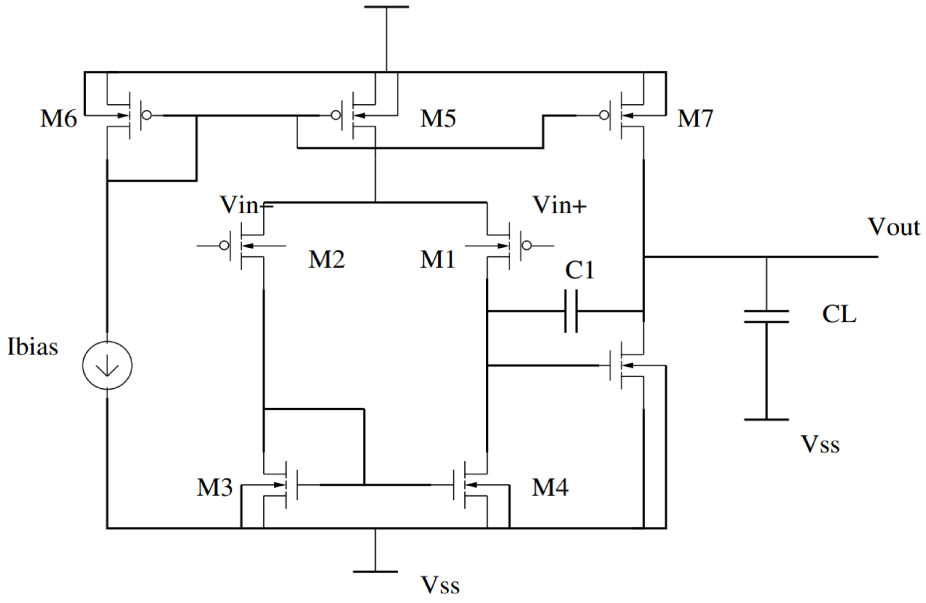

Figure 3.9: Two stage operational amplifier circuit

Table 3.4: Performance specifications of the two stage operational amplifier

Performance metrics	Specification
Gain (dB)	Maximize
Bandwidth (MHz)	[80, 90]
Slew Rate (V/μs)	[60, 75]

models for the different performance parameters. The Genetic Algorithm is chosen as the optimization engine since it is known to be robust for multiple constraints optimization. In addition, the Spice op-am model was adopted as a detailed circuit model for the proposed space mapping sizing approach.

The results of the obtained circuit performance through HSpice, SVM, and the proposed sizing approaches are reported in Table 3.6. The amplifier gain achieved by our space mapping surrogate based optimization is better than the one obtained with the SVM approach and matches to *0.28dB* relative error. Apart from the gain, we were able to fullfill all other design requirements in terms of bandwidth and slew rate with comparable accuracy to HSpice.

Table 3.5: Feasible design space

Circuit parameter	Parameter range
$W_1 = W_2$	$[1\mu, 100\mu]$
$W_3 = W_4$	$[1\mu, 50\mu]$
W_5	$[1\mu, 100\mu]$
W_7	$[1\mu, 100\mu]$
Cc	$[5pF, 20pF]$

Table 3.6: Optimization results for the two stage operational amplifier circuit

Performance metrics	HSpice	SVM	Our method
Gain (dB)	65.27	60.12	64.98
Bandwidth (MHz)	83.7	80	83
Slew Rate (V/μs)	71.4	63.07	70.2

The outcomes of the runtime comparison between the HSpice, SVM, and our proposed method is shown in Table 3.7. It can be seen that our proposed method can achieve significantly better speed-up than both HSpice and SVM based optimization method. This is mainly thanks to the global sizing procedure wherein the regional sensitivity analysis pruned the feasible design space avoiding unnecessary nominal optimization. In summary, both SVM and Spice methods can find design solutions

Table 3.7: Efficiency of the proposed method

Optimizer	Runtime (h)	Speed-up
HSpice	17.18	–
SVM	5.51	3.11X
Our method	3.22	5.33X

that meet the design specifications. However, our method is the only one that reached a good trade-off between the accuracy and runtime. Indeed, it offers a spice like accuracy in significantly less runtime.

3.3 Summary

In this chapter, we presented a methodology for determining optimal design solution using a space mapping scheme. It is based on a coupled simulation/equation based optimization approach. The optimization is formulated as a mapping function between two models of the circuit and the optimization problem is translated to finding the inverse of this mapping function. The proposed scheme is an alternative to classical optimization based analog sizing techniques with better convergence and superior performance with respect to direct optimization techniques. We present two applications that illustrate how the proposed methodology can be applied to the design and optimization of representative analog blocks. From the experimental results, it is established that our proposed methodology is Spice accurate while being up to 12.5X faster. In addition, it can successfully handle single as well multi-objective optimizations. Nevertheless, in real life, designers are facing inevitable variations in the structural and electrical circuit parameters due to environmental and physical factors. In the next chapter, we will focus on verifying the circuit behavior due to parametric variation as it is becoming a major concern that significantly impacts not only the yield but also the dynamics and so the functionality of analog circuits.

Chapter 4

Surrogate based Verification

Given the set of so-called optimal design parameters computed in Chapter 3, this chapter is concerned with the verification of possible aberrant circuit dynamics. The verification methodology is based on a statistical proof by contradiction technique to probe deterministic from stochastic circuit dynamics. It combines a surrogate generation scheme with a statistical hypothesis testing procedure. We demonstrate the feasibility and efficiency of the proposed methodology on several AMS circuits, namely a Colpitts oscillator, a first and a third order Σ-Δ modulators, and a phase locked loop.

4.1 Circuit Dynamics Verification

Figure 4.1 details our surrogate based methodology to statistically probe deterministic from stochastic dynamics of AMS circuits. Given a sized circuit topology, a design specification and a technology library, the AMS circuit behavior is modeled as Extended-System of Recurrence Equations (E-SREs) that describes its behavior with and without noise. The methodology starts by conducting transient simulations

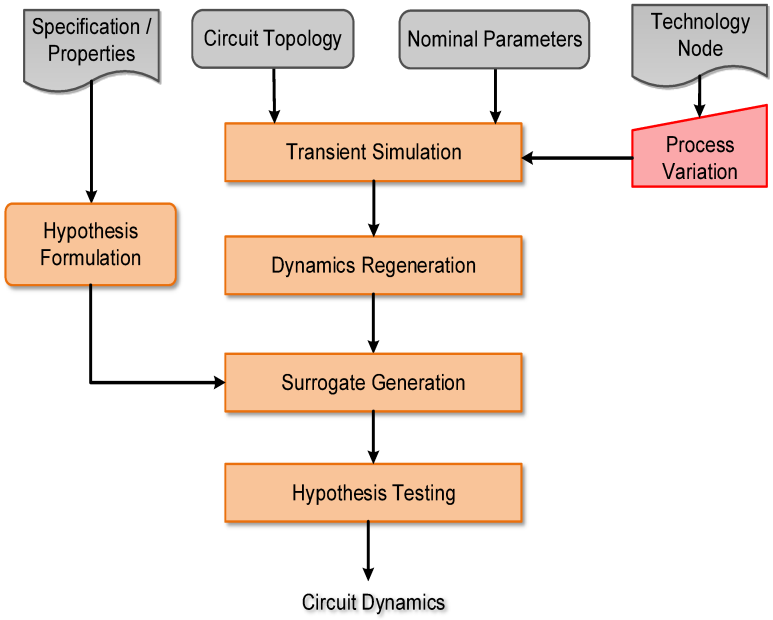

Figure 4.1: Surrogate based chaos/noise verification methodology

of the circuit behavior in light of process variations. Then, the surrogate verification scheme is deployed in the phase-space domain using a statistical proof by contradiction hypothesis testing procedure. In the sequel, we detail the different steps and methods of the proposed methodology.

SREs are the discrete version of analog differential equations. For the discrete digital components, the SREs are extended to Extended-SRE (E-SRE) [46] by expressing them with *if-else* logical formulas as follows:

$$X_i(n) = f_i(X_j(n-\gamma)), \forall i, j, n \in \mathbb{Z} \tag{4.1}$$

where $X_i(n) \in \mathbb{R}$ depicts the state variable and $\gamma \in \mathbb{N}$ denotes the time delay. f_i refers to a generalized If-formula $If(P, x, y) : B \times \mathbb{K} \times \mathbb{K}$ that satisfies the following two axioms:

$$If(true,\ x,\ y) \ = \ x$$

$$If(false,\ x,\ y) \ = \ y$$

In this thesis work, we are considering only thermal noise excitation that adheres to a Gaussian distribution with mean m, and standard deviation σ.

Definition 4.1.1 *(Chaos) The absence of a precise mathematical definition of the chaos phenomena makes it very challenging to be distinguished from circuit noisy behavior. Nevertheless, chaotic behavior can be characterized by the following features:*

1. *It is aperiodic but bounded.*

2. *It exhibits exponential sensitive dependence on initial conditions. Therefore, a very small initial condition discrepancy will exponentially change the behavior of the system over time which is known as the Butterfly Effect [62].*

3. *It is governed by one or more control parameters, a small change in which can cause the chaos to appear or disappear.*

4. *It has an unpredictable long-term behavior despite emerging from deterministic system.*

5. *It exhibits a complicated behavior wherein trajectories converge to a strange attractor that has a fractal dimension.*

First, we perform transient simulation of the obtained E-SRE AMS design model for specific environment constraints, namely the initial values of the voltage and current state variables and the simulation parameters (such as the total simulation time and the simulation step size). Thereafter, a dynamics regeneration method is adopted for

a *phase-space* verification of the circuit dynamics. In phase-space domain, the circuit state variables are displayed against each other, i.e., it leaves time as an implicit dimension not explicitly graphed. The subset of this phase-space domain toward which the circuit tends to evolve regardless of the initial conditions is called an *attractor*. This attractor is used to predict the chaotic behavior of an AMS circuit in order to consider them in the surrogates generation later. The non uniform embedded window [63] and the false nearest neighbor method [64] are used to establish optimal embedding parameters (d_e, τ) for the attractor reconstruction.

Next, we elucidate the property of interest ($\mathcal{P}$) that the circuit should comply with. The property to be verified is phrased as follows: "*Is the observed random like behavior of the AMS design due to noisy or chaotic behavior?*". Hence, we define a null hypothesis, denoted by H_0, which assumes that the circuit exhibits stochastic noise and an alternative hypothesis H_1 that assumes the circuits to be purely deterministic, i.e., chaotic. To verify the above-mentioned hypotheses, the idea is to generate artificial circuit outputs (called surrogates) which are realizations of what the circuit output would be if it was consistent with the property $\mathcal{P}$. Hence, these surrogates serve as a useful null model against which the real circuit output is verified. They are constructed from the circuit output so they are free from any chaotic process while preserving some features of the circuit output.

Thereafter, we determine the noise radius ρ which is the amount of noise that will obliterate the attractor of the surrogates. The best selection of this parameter is very important for the accuracy of the results. ρ is computed according to the suggestions in [65]. The parameters (d_e, τ, ρ) together with the hypothesis H_0 are then passed to a Surrogate Generation Method (SGM). A number of surrogates N_S is then generated using this method (more details will be given later in Section 4.1.1).

Those surrogates must preserve some deterministic features of the real output (such as periodicity) while satisfying the null hypothesis H_0. Therefore, chaotic behavior by fine scale dynamics will be altered by random noise with level ρ.

Finally, a single hypothesis testing technique is employed to verify the actual AMS circuit behaviors in order to verify the noisy behavior expressed with the null hypothesis H_0. If H_0 is rejected, significant differences between the original output and its surrogates in terms of Gaussian Kernel (GK) or Lempel-Ziv Complexity (LZC) measures (see Sections 4.1.2 and 4.1.3 for more details) are deduced depending on the noise distribution (i.e., Gaussian/non-Gaussian). The rejection of H_0 consequently implies the acceptance of the alternative hypothesis H_1 that the circuit behavior exhibits chaotic dynamics.

4.1.1 Surrogate Generation Method

We extend the surrogate data method, developed first in [65] to study the dynamics of human electrocardiogram (ECG), to verify AMS circuits behavior. It is a statistical proof by contradiction method to verify whether or not data belong to a particular class of system. Our surrogates generation procedure is summarized in Algorithm 4.1. The proposed algorithm requires: E-SREs model of the circuit for the state variables X with/without thermal noise in some or all circuit components denoted by *E-SRE(X)*, the noise radius ρ, the embedding dimension d_e, the embedding lag τ, and the number of surrogates to be generated N_S. The algorithm begins with state space reconstruction of the circuit dynamics (line 4). It consists of representing the dynamical features of the circuit output *E-SRE(X)* in an alternative domain namely an Euclidian space $\mathbb{R}^{d_e}$ where d_e is the embedding dimension. By doing so, the points in $\mathbb{R}^{d_e}$ form an attractor $\mathcal{A}$ (line 5) that gives intuition about the circuit dynamics.

Algorithm 4.1 Surrogate Generation Algorithm

Require: E-SRE(X), ρ, d_e, τ, N_S

1: $N \leftarrow length\ (X)$;
2: $\widetilde{N} \leftarrow N - (d_e - 1)\tau$;
3: $d_w \leftarrow d_e\tau - 1$;
4: $\{Z_t\}_{t=1}^{\widetilde{N}} \leftarrow embed\ (\text{E-SRE(X)}, d_e, \tau)$;
5: $\mathcal{A} = \{z_t/\ t = 1, 2, ..., \widetilde{N}\}$;
6: **for** $k = 1 \rightarrow N_S$ **do**
7: **for** $j = 1 \rightarrow N - d_w$ **do**
8: $i \leftarrow 1$;
9: $s_1 \in \mathcal{A}$;
10: **while** $i < n$ **do**
11: $d_j = \|s_i - z_j\|$;
12: $\omega_j = e^{-\frac{d_j}{\rho}}$;
13: $p_j \leftarrow \omega_j / \sum_k \omega_k$;
14: $P(s_{i+1} = z_t) \propto p_j$;
15: $s_{i+1} = z_j$;
16: $i \leftarrow i + 1$;
17: $\{(s_t)_k\} \equiv \{(s_1)_k, (s_2)_k, ..., (s_N)_k\}$;

Thereafter, the embedding points of neighboring trajectories in the obtained attractor are used to create a new attractor with noisy trajectories (lines 10-17). The algorithm chooses an initial condition s_1 randomly from the reconstructed attractor $\mathcal{A}$ (line 9). For the following noisy attractor point, a near neighbor $z_j \in \mathcal{A}$ is then chosen with a probability commensurate to the noise radius ρ (line 14). The introduction of this dynamical noise by the surrogate generation algorithm will obliterate any deterministic dynamics of the circuit while preserving periodicity. Hence, chaotic and stochastic circuit dynamics lead to distinct trends of their surrogates produced by this method.

4.1.2 Gaussian Kernel Test Statistic

Correlation dimension is an extension of the usual notion of dimension to objects with a fractional dimension. Hence, a correlation dimension between two and three

would represent an object which occupies more space than a plane, but less space than a sphere. Because strange attractors have a fractional dimension, correlation dimension is used as test statistic in the hypothesis testing. We use the Gaussian Kernel (GK) [66] test to measure the dimension d_c of the circuit attractor $\mathcal{A}$. GK is mathematically defined by Equation (4.2). It uses the Gaussian kernel function, given in Equation (4.3), that is more convenient for calculating the effect of Gaussian noise.

$$d_c = \lim_{h \to 0} \lim_{N \to +\infty} \frac{log\ \hat{T}_m(h)}{log\ h} \tag{4.2}$$

$$\hat{T}_m = \frac{1}{N} \sum_i \sum_{j \neq i} \left(\frac{1}{N-1} e^{\frac{\|x_i - x_j\|^2}{4h^2}} \right) \tag{4.3}$$

where h denotes the bandwidth, and N represents the number of estimation points. Our choice for this test can be justified by the fact that it has been proven to provide a rigorous estimation of correlation dimension even for a noise level that is 50% higher than an ideal signal [66].

4.1.3 Lempel-Ziv Complexity Test Statistic

The Lempel-Ziv Complexity (LZC) method, first defined in [67], is a nonparametric measure of complexity in the sense of Kolmogorov. It is able to capture randomness, i.e., the degree of redundancy (or patterns) that are similar in a signal without making any assumption about its distribution. Unlike the Gaussian Kernel (GK) test statistic described in the previous section, this measure has the advantage of handling stochastic circuit behaviors that do not follow a Gaussian distribution. It objectively and quantitatively estimates system complexity through the change process of inherent system structure.

Consider a circuit output $X = (x_1, x_2, ..., x_N)$ of length N that takes its values

in an alphabet A of finite size $\alpha = |A|$:

$$S_i = \begin{cases} 0 & \text{if} \quad x_i < T_d \\ 1 & \text{if} \quad x_i \geq T_d \end{cases}$$

The upper limit of the complexity counter is given by:

$$c(N) < \frac{N}{(1-\epsilon_N)\ log_\alpha(N)} \tag{4.4}$$

where α is the number of alphabets in the circuit output under verification (it is independent of the length of the output under verification N) and ϵ_N is given by the following equation:

$$\epsilon_N = 2\frac{1 + log_\alpha(log_\alpha(\alpha N))}{log_\alpha(N)} \tag{4.5}$$

The normalized LZC C_{LZ} is defined as:

$$C_{LZ}(N) = \frac{c(N)}{b(N)} \tag{4.6}$$

where $b(N)$ is given by the following equation:

$$b(N) = \frac{N}{log_\alpha(N)} \tag{4.7}$$

Ziv proved in [68] that if X is the infinite length output from an ergodic source with entropy rate h, then $\limsup_{n\longrightarrow\infty} C_{LZ}(n) = h$.

4.2 Applications

In this section, we report the results of the application of the proposed surrogate based dynamics verification approach on a Colpitts oscillator, a third order Σ-Δ modulator, and a PLL circuit. The type of hypothesis testing used is the one tailed test with the level of significance $\alpha = 5\%$.

4.2.1 Colpitts Oscillator

A Colpitts oscillator is a combination of a transistor amplifier and an LC circuit as shown in Figure 4.2. The Colpitts circuit behavior has been reported to exhibit chaotic behavior [69].

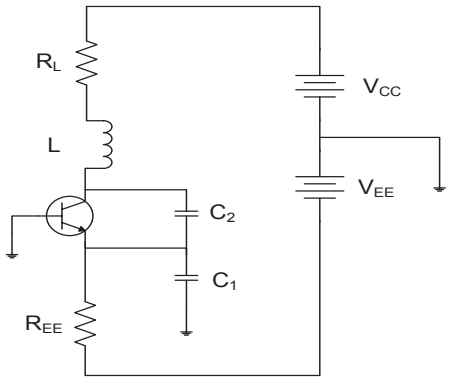

Figure 4.2: Colpitts oscillator

We model its behavior by the following E-SREs:

$$
\begin{aligned}
i_B(n) &= if(V_{BE} > V_{th}, \frac{V_{BE}(n) - V_{th}}{R_{ON}},\ 0) \\
i_c(n) &= if(true,\ \beta i_B(n),\ 0) \\
V_{CE}(n+1) &= if(true,\ V_{CE}(n) + \delta_t \frac{i_L(n) - i_c}{C_1},\ 0) \\
V_{BE}(n+1) &= if(true,\ V_{BE}(n) - \frac{\delta_t}{C_2}(\frac{V_{EE} + V_{BE}(n)}{R_{EE}} + i_L + i_B)),\ 1) \\
i_L(n+1) &= if(true,\ i_L(n) + \delta_t(V_{CC} - V_{CE}(n) + V_{BE}(n) - i_L(n)R_L),\ 0)
\end{aligned}
\tag{4.8}
$$

Table 4.1 summarizes the simulation and surrogate generation parameters for the Colpitts circuit. Figure 4.3 illustrates both the original and reconstructed attractor of the Colpitts oscillator behavior using the embedding dimension (d_e, τ) given in Table 4.1. The similarity of both attractors demonstrates the appropriate choice of embedding parameters.

Table 4.1: Simulation parameters of the Colpitts circuit

Parameter	Value	Parameter	Value
R_{EE}	0.904	R_L	35
C_1, C_2	54e-9	R_{EE}	400
R_{ON}	100	V_{CC}	5
V_{EE}	-5	V_{th}	0.75
β	94	d_e	2
τ	3	ρ	0.003
N_S	100	N	3600

The importance of an adequate selection of the noise radius ρ is shown in Figure 4.4. For instance, if ρ is too large ($\rho = 0.01$), the surrogate generation algorithm will introduce too much randomization and the surrogates will no longer resemble the circuit output V_{CE} (see Figure 4.4(c)). This resemblance can be measured using a pattern matching technique [70]. Conversely if ρ is too small ($\rho = 0.001$), the algorithm will introduce insufficient randomization, and surrogates will be identical to the output as shown in Figure 4.4(b).

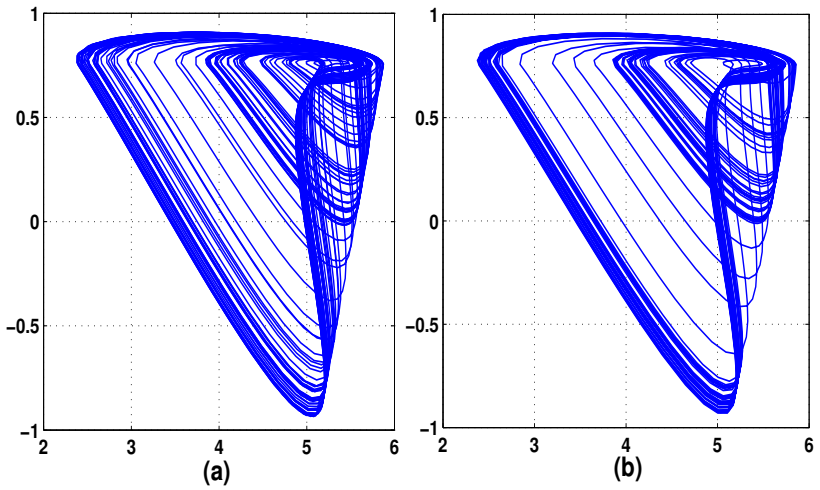

Figure 4.3: Original attractor of Colpitts output (a), reconstructed attractor (b)

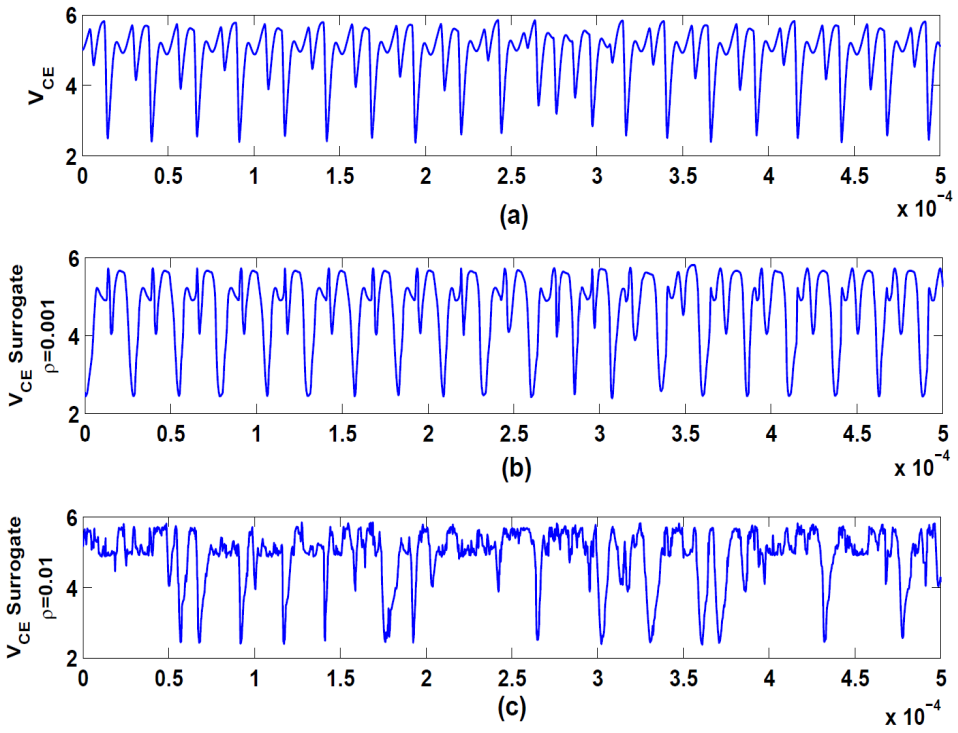

Figure 4.4: The V_{CE} output and its surrogate for different noise radius ρ

Figure 4.5 depicts the Gaussian Kernel correlation dimension d_c of the V_{CE} output (dashed line) and its corresponding 100 surrogates (dotted line). It can be observed that our approach successfully probes the chaotic behavior of the Colpitts circuit. For instance, the $d_c(V_{CE})$ is significantly different from those of the surrogates and so falls in the rejection region (see Figure 4.5). This leads to the rejection of the noisy dynamics hypothesis and consequently proves the chaotic circuit dynamics. Using our circuit dynamics verification technique, we were able to detect chaotic dynamics in the Colpitts oscillator with a confidence level of 95%.

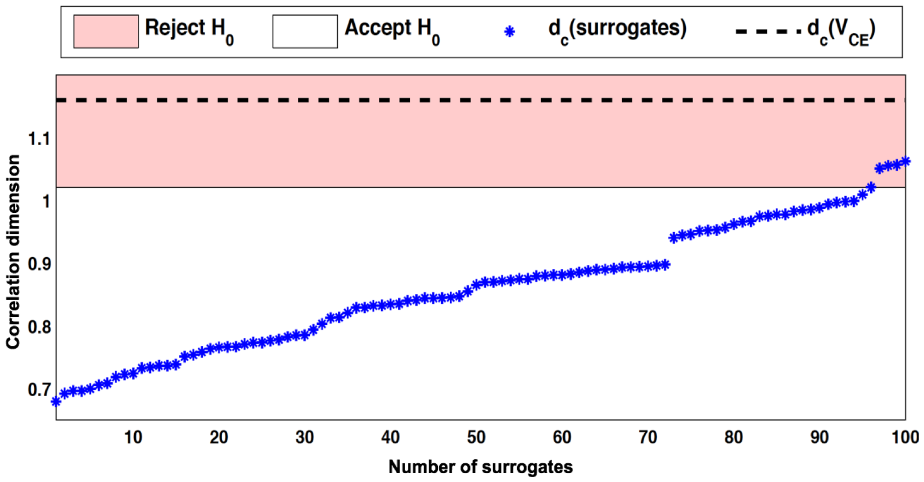

Figure 4.5: Analysis results for chaotic Colpitts circuit

4.2.2 Third Order Σ-Δ Modulator

We consider the third order Cascade of Integrator with Distributed Feedback (CIFB) structure Σ-Δ modulator depicted in Figure 4.6 and modeled with the system of E-SREs given by Equations (4.9).

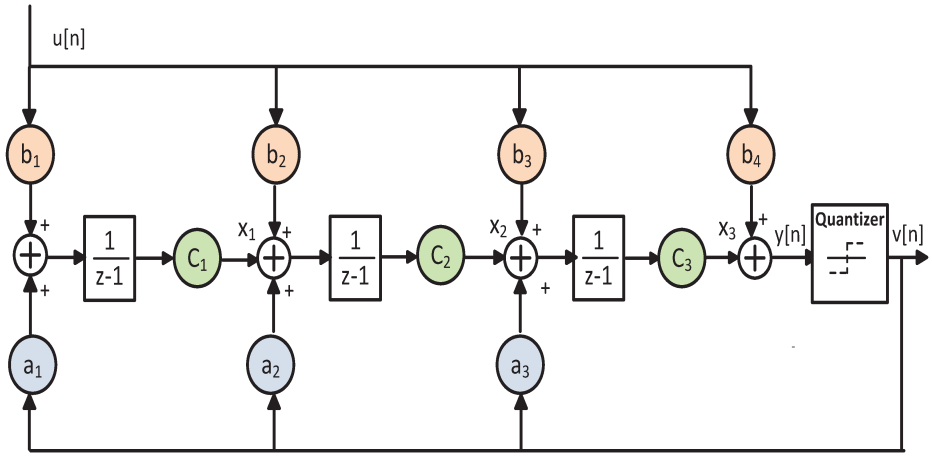

Figure 4.6: Third order Σ-Δ modulator

$$
\begin{aligned}
v(k+1) &= if(P_{th}(k), -a, a) \\
x_1(k+1) &= if(P_{th}(k), x_1(k) + b_1u(k) - a_1a, x_1(k) + b_1u(k) + a_1a) \\
x_2(k+1) &= if(P_{th}(k), c_1x_1(k) + b_2u(k) + x_2(k) - \\
&\qquad a_2a,\ c_1x_1(k) + x_2(k) + b_2u(k) + a_2a) \\
x_3(k+1) &= if(P_{th}(k), c_2x_2(k) + x_3(k) + b_3u(k) - \\
&\qquad a_3a,\ c_2x_2(k) + x_3(k) + b_3u(k) + a_3a) \\
\text{where } P_{th}(k) &= c_3x_3(k) + u(k) \geq 0
\end{aligned}
\tag{4.9}
$$

The following parameters of the circuit were computed using the Delta Sigma MATLAB toolbox [71]: $a = 2,\ A = B = [0.044\ 0.2881\ 0.7997]^t,\ C = [1\ 1\ 1]^t$. In [72], the author proved that the Σ-Δ modulator can reproduce chaos if it is fed by a chaotic input. This is a very important feature of Σ-Δ modulators in communication applications such as encryption and cryptography. Therefore, we will use our methodology to verify the Σ-Δ modulator given in Figure 4.6, with the chaotic input fed from the Colpitts Oscillator studied in Section 4.2.1. Figure 4.7 shows the time variation

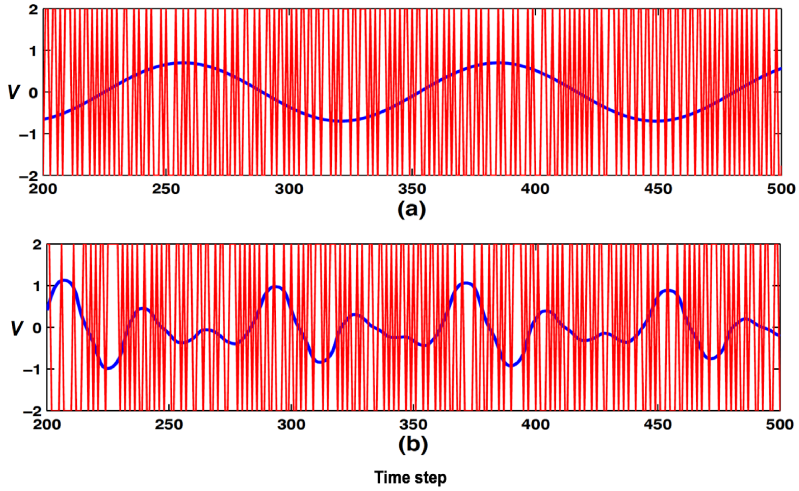

Figure 4.7: Quantized sinusoidal wave (a), and chaotic (b) inputs

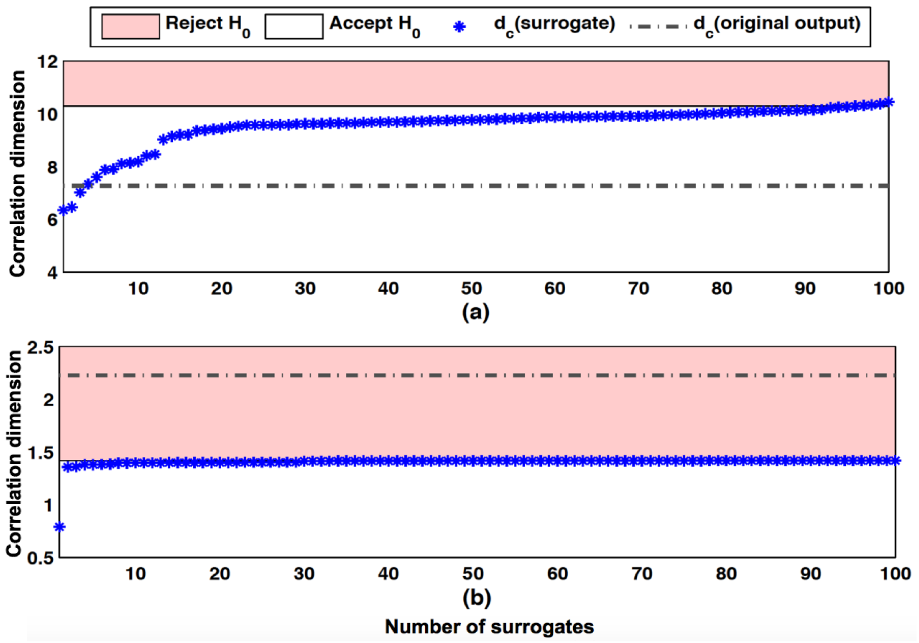

Figure 4.8: Chaos verification for noisy modulator (a), and modulator fed with chaotic input (b)

of the quantized output V of the Σ-Δ modulator for a sinusoidal (panel (a)) and a chaotic input (panel (b)).

By using GK correlation dimension, we verify the circuit using the proposed methodology in the presence of thermal noise that adheres to a Gaussian distribution and chaos. Our results shown in Figure 4.8(b) are in good agreement with the results in [72]. Indeed, the correlation dimension of the output V (dashed line) is very different from its corresponding surrogates (dotted line). This violates the hypothesis that the apparently random output is generated from a noisy modulator. In contrast, in the presence of thermal noise (Figure 4.8(a)), there was no apparent distinction between the two. Hence, the hypothesis H_0 holds and consequently the circuit exhibits noise. This, again, demonstrated the capability of the proposed technique in distinguishing chaotic and noisy dynamics in the Σ-Δ modulator circuit.

4.2.3 Phase Locked Loop

PLLs are widely used as modulators and demodulators in communication systems. In this section, we verify a third order PLL that serves as FM demodulator [73]. In this PLL, a multiplier Phase Detector (PD) and a resonant Low Pass Filter (LPF) are deployed as shown in Figure 4.9.

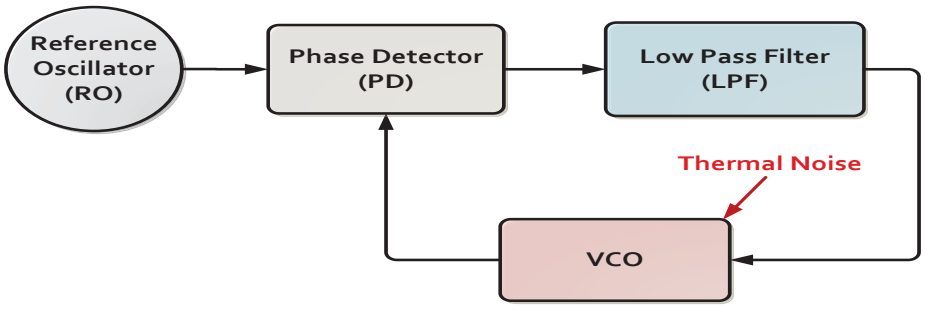

Figure 4.9: Conventional PLL block diagram

The PLL dynamics are governed by the following E-SREs:

$$
\begin{aligned}
\varphi(n+1) &= if(true,\ \varphi(n) + \delta_t\ f_n,\ 0) \\
\Psi(n+1) &= if(true,\ \Psi(n) - \delta_t\ m\ f_n\ sin(\varphi(n)),\ \pi) \\
x(n+1) &= if(true,\ x(n) + \delta_t\ (\Omega_n - k_n\ z(n)),\ 0) \\
y(n+1) &= if(true,\ y(n) + \delta_t\ (\sin(x(n) - \Psi(n)) + \\
&\qquad (g-2)\ y(n) - \frac{g-1}{g}\ z(n)),\ 0) \\
z(n+1) &= if(true,\ z(n) + \delta_t\ (g\ y(n) - z(n)), 1)
\end{aligned}
\tag{4.10}
$$

where the state variables φ, Ψ, x, y, and z stand for modulating signal, frequency of modulation, phase difference between PLL input and VCO output, PD output, and LPF output, respectively. As the control parameter m changes, the dynamic of the PLL changes and at the end culminating to a chaotic regime. For instance,

the circuit operates in a periodic regime for $m = 0$ while chaotic dynamics occur for $m = 10$. Figure 4.10 depicts the time domain behavior of the PD output y for periodic (panel(a)), chaotic (panel(b)), and noisy (panel(c)) behaviors.

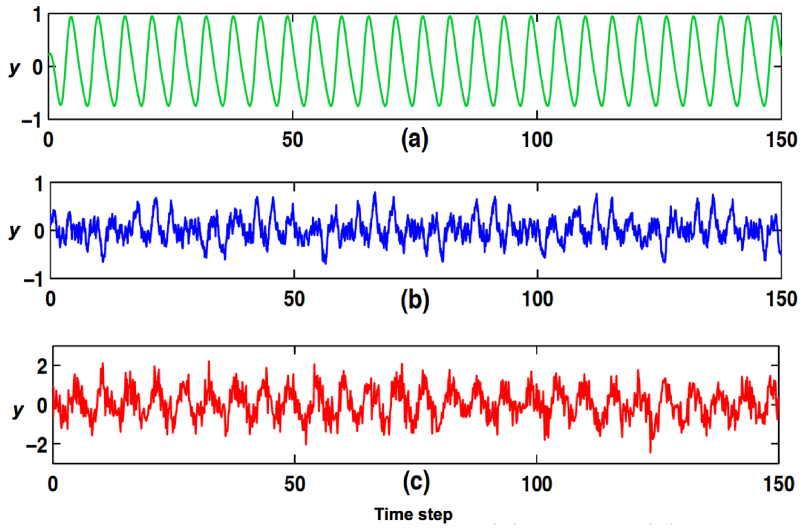

Figure 4.10: Time variation of Y during periodic (a), chaotic (b), and noisy (c) regimes

It can be remarked that the chaotic output reveals a similar behavior to the noisy output simulated with thermal noise in the VCO. This demonstrates the need to assess the real source of random-like behavior observed in nonlinear circuits during the design process. A phase diagram of the PLL attractor is depicted in Figure 4.11. The GK correlation dimension acquired from the PLL circuit output y (dashed line)

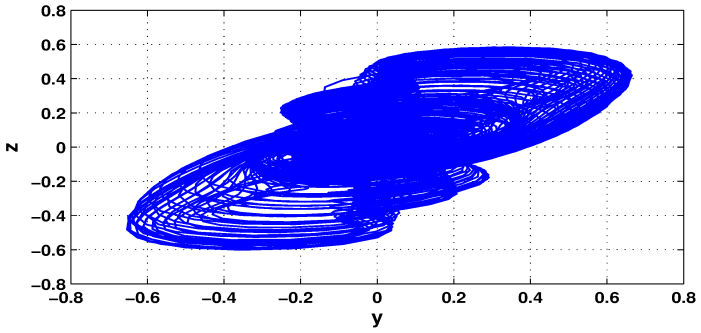

Figure 4.11: Attractor of the PLL circuit during chaotic regime

and 100 surrogates (dotted line) is shown in Figure 4.12 for the chaotic behavior (m=10) and in Figure 4.13 for the noisy behavior (m=0).

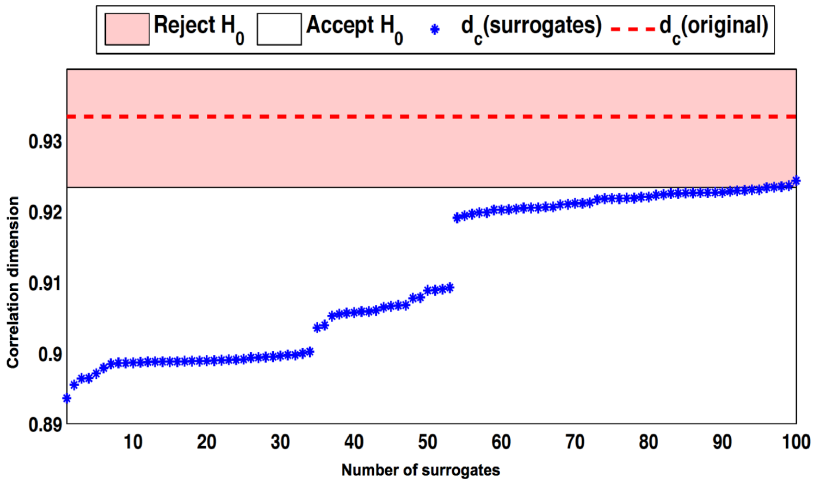

Figure 4.12: Verification of PLL in chaotic regime

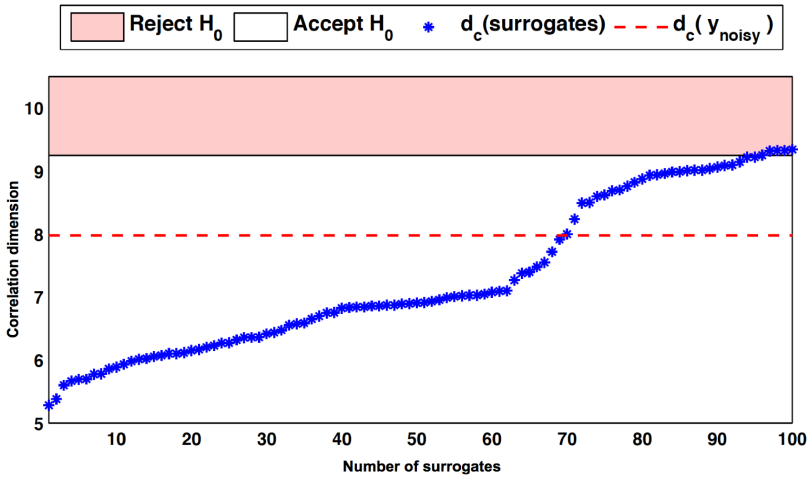

Figure 4.13: Verification of PLL in Noisy regime

A good qualitative agreement between the results of our methodology and the results presented in [73] is demonstrated; indeed, the correlation dimension of the original output (dashed line) is very different from its corresponding surrogates (dotted line) in the chaotic case. This violates the hypothesis that the apparently random output is generated from a noisy circuit and hence indicates the deterministic structure of

Table 4.2: Simulation parameters of the PLL circuit

Parameter	Value	Description
f_n	0.904	normalized frequency of the modulating signal
m	10	modulating index
Ω_n	1.2	normalized detuning
d_e	5	embedding dimension
k_n	0.6511	normalized loop gain
g	1.728	filter gain
τ	10	embedding lag
ρ	0.0170	noise radius
N_S	100	number of surrogates

the circuit output. Consequently, the proposed methodology was able to successfully distinguish the noise like behavior exhibited by deterministic chaotic circuit from the stochastic noisy PLL.

4.2.4 Comparison with Lyapunov Exponent Method

In order to demonstrate the efficiency of the proposed methodology, the Lyapunov Exponent (LE) measure was carried out for the previously analyzed circuits under the same simulation conditions and for the same circuits outputs. The results of chaos verification and simulation time are recapitulated in Table 4.3.

The obtained results using our approach are in good agreement with those obtained with the LE technique for the Colpitts circuit and Σ-Δ Modulator. However, a failure to discriminate the noisy behavior of PLL has been detected (see Table 4.3); Thermal noise in the VCO creates sensitivity to initial conditions of the PLL design that triggered the finding of a positive Lyapunov exponent. In fact, a maximum exponent $\lambda = +0.0154$ has been obtained while the circuit exhibits thermal noise in the VCO and not chaotic behavior. Moreover, a simulation time acceleration is found

using our methodology. Indeed, when adopting our approach, the simulation time was minimized from thousands of seconds to hundreds of seconds as shown in Table 4.3.

Table 4.3: Accuracy and simulation time comparison

	Colpitts Oscillator		3^{rd} order Σ-Δ Modulator		PLL	
	Our method	LE	Our method	LE	Our method	LE
Simulation Time [Sec.]	164.7	709.7	196.3	985.4	247.3	1213.4
Chaos\Noise Detection	√	√	√	√	√	×

×: Failure in detecting circuit dynamics.
√: Successfully detecting circuit dynamics.

4.2.5 First Order Σ-Δ Modulator

The block diagram of a first order Σ-Δ modulator is shown in Figure 4.14. It consists of a negative feedback loop with 1-bit quantizer and a discrete time integrator.

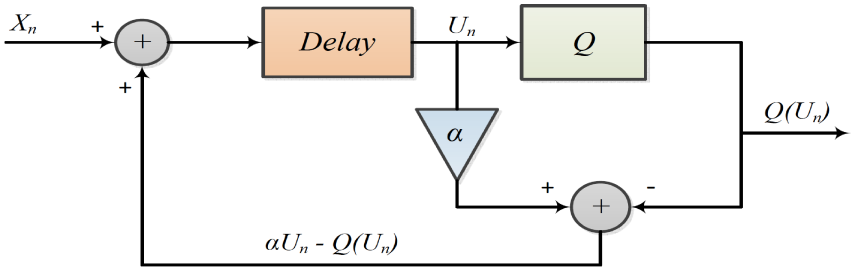

Figure 4.14: First order Σ-Δ modulator

The behavior of the circuit can be described by the following E-SRE:

$$U_n = \text{if } (U_{n-1} \geq 0, \alpha U_{n-1} + X_{n-1} - 1, \alpha U_{n-1} + X_{n-1} + 1), 0)$$

where X_n and α stand for the input signal and the modulator gain, respectively. The nonlinearity being introduced by the quantizer block Q gives rise to a chaotic behavior

if the gain α is in the range]1, 2]. However, if $\alpha \leq 1$, instead of chaos, the circuit exhibits a normal operation (i.e., the quantized output will be approximately equal to the input signal). We performed the verification of this circuit under two regimes: (1) chaotic regime with $\alpha = 1.14$; (2) noisy regime by introducing non Gaussian flicker noise to a non-chaotic output for $\alpha = 0.5$. The results of the application of our circuit dynamics verification methodology to the first order Σ-Δ modulator are recapitulated in Table 4.4. In the chaotic regime, both the Gaussian Kernel (GK) test statistic and LZC test statistic reject the null hypothesis H_0 of noisy circuit behavior.

Table 4.4: Results of verifying the first order Σ-Δ modulator

	GK test statistic	LZC test statistic
Chaotic regime	Reject H_0	Reject H_0
Noisy regime	Reject H_0	Accept H_0

Nevertheless, in the case of noisy regime, the GK test statistic falls short to discriminate the noisy behavior emanating from flicker noise which does not adhere to a Gaussian distribution while the LZC test statistic successfully discriminates it. Indeed, the null hypothesis H_0 is found consistent with the noisy assumption whereas the GK test statistic fails to do so. Consequently, our dynamics verification methodology presents two test statistic measures that are able to detect different types of noise depending on their distributions.

4.3 Summary

From a verification perspective, this chapter presented a methodology for the verification of analog circuit dynamics. More precisely, the proposed methodology serves to statistically assess chaos from noise in analog and mixed-signal designs. The circuit is

modeled using Extended System of Recurrence Equations. The verification approach is based on the univariate hypothesis testing and a surrogate generation method to decide whether to reject or accept the hypothesis that an unpredictable circuit behavior is emerging from noise. Depending on the type of noise, two test statistic measures, namely Gaussian Kernel and Lempel-Ziv Complexity, are proposed. The experimental results on several circuits show the robustness and effectiveness of the proposed methodology. Nevertheless, in reliability analysis, designers are more concerned about the failure probability (i.e., yield) of the circuit due to fabrication imperfections. To respond to this concern, we propose in the next chapters yield estimation techniques to verify compliance of the circuit performances to their desired specifications in light of process variation.

Chapter 5

Single Performance Yield Estimation

As stated in Chapter 1, a crucial step in the VLSI design flow is the verification of the circuit robustness to process variation. Upon ensuring that the circuit fulfills its intended behavior for the computed nominal process parameters, we propose in this chapter a semi-formal reachability analysis technique to estimate the yield rate for a single circuit performance. In contrast to methods that use solely forward reachability, our reachability analysis approach is carried out in an intertwined forward/backward manner in order to reduce wrapping effect. Subsequently, the circuit failure rate is estimated using a hypothesis testing based approach. We demonstrate the effectiveness of our proposed verification methodology on a Tunnel diode oscillator and a Phase Locked Loop (PLL) circuits.

5.1 Reachability Analysis based Yield Estimation

An overview of the proposed methodology for single performance yield assessment using intertwined forward/backward reachability analysis is shown in Figure 5.1. Given a nonlinear AMS circuit topology, a surrogate model of the circuit in the form of an SSRE (see Section 2.1.2) is generated. The proposed SSRE formalism features a sound treatment of noise. It actually allows a consistent consideration of the noise effect to which the circuit is incurred during the reachability analysis process. Then, parameter values from a certain distribution of the parameter space are derived using the efficient LHS technique.

Next, reachability bounds of the AMS circuit behavior for a continuous set of initial conditions, and under the derived circuit parameters are generated using first a forward reachability analysis technique. Then, the obtained forward reachable sets are corrected using a backward reachability scheme in order to reduce the over-bounding of the forward scheme. Then, an univariate hypothesis testing procedure is performed on the reachable bounds outputted from the backward reachability analysis.

The intertwined forward/backward reachability is computed using SSRE circuit model with parameters selected by the LHS procedure and for initial conditions that are defined within intervals (n-cubes) is based on multivariate global optimization methods. The SSRE is not solved for every initial condition value but it employs the reachability analysis algorithm to optimize the search for the global extremum. The output of this step is a refined reachability set generated from the backward reachability correction that includes all possible actual behaviors (trajectories) of the circuit transient behavior. The main advantage of the proposed verification scheme is its generality and scalability. In fact, it does not make any assumption about the nature

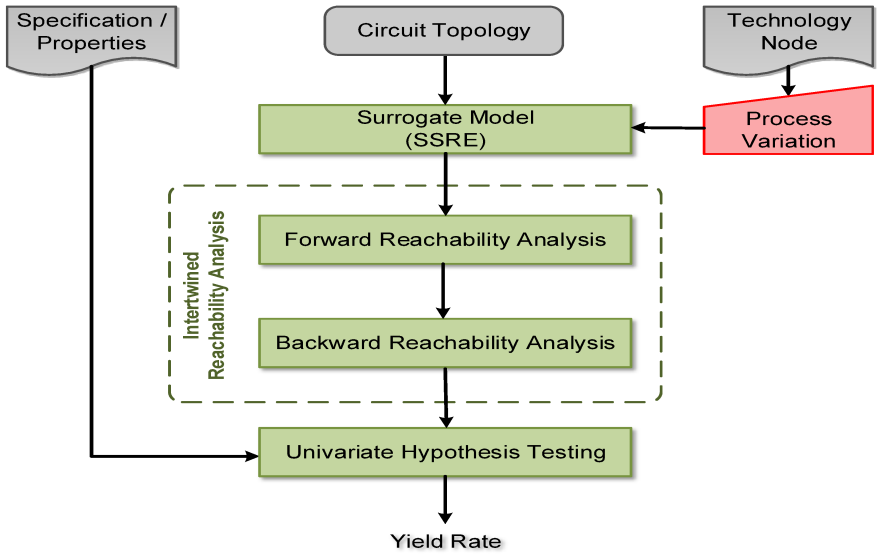

Figure 5.1: Proposed single performance yield estimation methodology

of the AMS circuit dynamics: it works for any AMS design with linear and nonlinear behavior. Next, appropriate null and alternative hypotheses are formulated from a certain SSRE specification of the AMS circuit under verification. For each selected circuit parameters in the reachability iteration, hypothesis testing based Monte Carlo (MC) technique is conducted to estimate the circuit parametric failure which refers to failures caused by the deviation between manufactured circuit parameter values and intended parameter values. Each time the null hypothesis H_0, which represents the desired circuit property/performance, is rejected, we draw a conclusion that the circuit fails to comply with its property and so we increment the number of circuit failures $N_{failure}$. Finally, the AMS circuit yield rate is computed based on the probability of failure $P_{Failure}$ as follows:

$$P_{Failure} = \frac{Nb.\ of\ Rejected\ H_0}{Total\ Nb.\ of\ MC\ Trials}$$

5.1.1 Latin Hypercube Sampling

To study parameter variation effects on the AMS circuits behavior, an optimal exploration of the parameter variation domain is very important in order to achieve a good accuracy and avoid non-informative verification runs. Traditional sampling techniques (e.g., Pseudo Random Sampling (PRS) [74], Fractional Factorial [75], Central Composite [76], etc.) only arrange parameter values at some specific corners in the parameter space and cannot handle multivariate stochastic parameters especially in terms of correlation. Consequently, when performing the verification, it cannot mimic the circuit behavior in a global circuit parameter space. We first look at PRS as applied in the estimation of circuit failure in order to justify the use of Latin Hypercube Sampling (LHS). It has been demonstrated that the LHS technique gives samples that could reflect the integral distribution more effectively with a reduced samples variance [77]. Figure 5.2 illustrates the differences while using Uniform Monte Carlo PRS and Gaussian Monte Carlo LHS of a random normal parameter of transistor width for 1000 trials. As it can be seen, the PRS approach has a poor space filling. Indeed, there are regions of the transistor width space that are not sampled enough and other regions that are heavily sampled; On the contrary, the LHS approach adequately samples the entire transistor width variation domain. The generated samples follow more closely the actual Gaussian distribution.

In the sequel, we explain the Latin Hypercube Sampling (LHS) main steps to generate a sample size N from n AMS circuit parameter variables $\xi = [\xi_1, \xi_2, \ldots, \xi_n]$ with the probability distribution function $f_\xi(.)$. The approach starts by the partitioning of the range of each circuit parameter variable into N nonoverlapping intervals on the basis of equally probability size $\frac{1}{N}$. One value from each interval is randomly selected w.r.t. the conditional probability density in the variation interval defined by

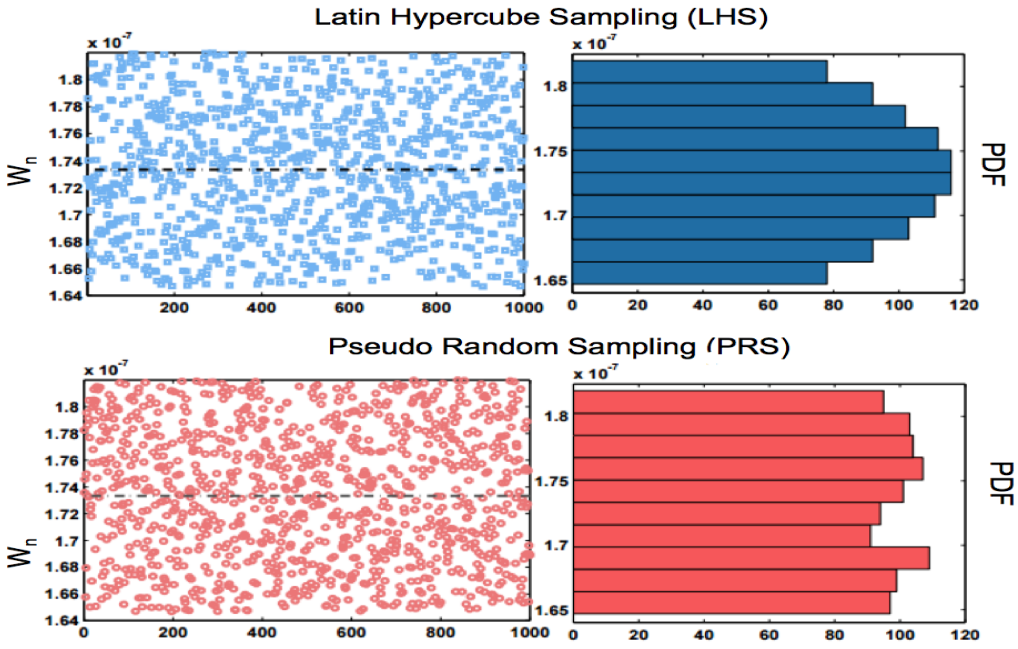

Figure 5.2: Sampling differences between Monte Carlo LHS and PRS

the technology library. The N values thus obtained for ξ_1, are paired in a random manner with the N values of ξ_2. These N pairs are combined in a random manner with the N values of ξ_3 to form N triplets, and so on, until a set of $N \times n$-tuples is formed according to the following equation:

$$\xi_{ij} = \frac{\pi_j(i) + U}{N}, 1 \leq i \leq N, 1 \leq j \leq n \tag{5.1}$$

where π_j are uniform random permutations U is a uniform distribution such that U and π_j are independent. The generated random samples follow the multiple stratification property given below:

$$\forall c = 0, \cdots, N-1, \forall j = 1, \cdots, n$$

$$prob\{1 \leq i \leq N | \frac{c}{N} \leq \xi_{ij} < \frac{c+1}{N}\} = 1$$

The choice of this sampling technique can be justified by its variance sampling reduction, which results in a better sampling selection and consequently a better verification coverage [78].

5.1.2 Intertwined Forward-Backward Reachability Analysis

The proposed intertwined reachability analysis approach is shown in Figure 5.3. The reachability analysis is conducted by iteratively applying a propagation algorithm which computes the next reachable set at time $t + \Delta t$ based on the current reachable set at time t.

Definition 5.1.1 *(Reachability Analysis) Reachable set (or bounds) is the collection of all possible trajectories or states of the AMS circuit transient behavior originated from an interval of initial conditions. Mathematically, this can be defined as follows:*

$$X_{Reachable\_set} = \{x \in \mathbb{R}^{N_x} \mid \underline{X_L} \leq x \leq \overline{X_U}\} \tag{5.2}$$

where $\underline{X_L}$ is the lower reachable bound of the reachable set (or region) and $\overline{X_U}$ is the upper bound of the reachable set.

First, the forward reachability analysis trajectories are calculated starting from the initial condition uncertainty region (in this case it has rectangular geometrical form) at each time step and projected to a reachable set as depicted in Figure 5.3 (a). Second, the backward reachable set is computed wherein the obtained forward reachable set is considered as the initial region of uncertainty. Trajectories starting from all points in the final backward reachable set is simulated in reverse time for the sake of screening out erroneous over-approximated reachable sets as illustrated in Figure 5.3 (b). The definition of reverse time dynamics of the SSRE model allows the forward/backward reachability exchange.

The detailed implementation of the intertwined reachability analysis approach is summarized in Algorithm 5.1. Given an interval system of stochastic differential equations (an SSRE whose initial conditions are intervals), the algorithm defines the region of uncertainty of the circuit output as a hypercube (n-cube) at time t_0 (lines

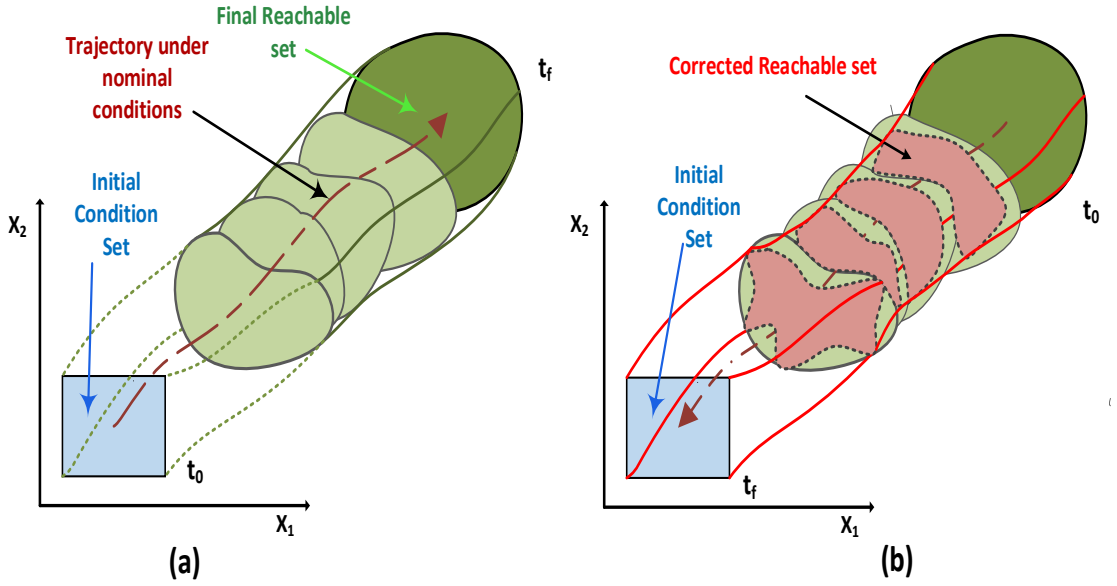

Figure 5.3: Intertwined reachability analysis concept

3 and 18). Hence, the reachability analysis problem at a given simulation time point t^* for each circuit output (or state space) is equivalent to finding the maximum and minimum bounds of the SSRE model. In the proposed algorithm, the reachability analysis problem is so cast into a constrained multivariable nonlinear global optimization problem. It was proven that under continuity condition, it is sufficient to compute the evolution of the external surface of the uncertainty region [79]. This means that to calculate the reachable bounds, it is sufficient to compute the trajectories emanating from the external surface of the region of the uncertainty region. The extreme functions (Max and Min) at a specific time t^* of the system equations $SSRE(t^*, j, X_{ext}), \forall j = 1, \ldots, N_x$, which bound the circuit behavior, are first computed using the forward reachability analysis. We use the MATLAB Optimization solver [80] based on trust regions (lines 1 to 15) to obtain these extreme functions of $SSRE(t^*, j, X_{ext}), \forall j = 1, \ldots, N_x$ by fixing the time variable to t^* and constraining the circuit transient behavior to evolve over the external uncertainty region (line

Algorithm 5.1 Intertwined Forward/Backward Reachability Analysis

Require: $SSRE$: AMS Circuit Model, X_0 : Interval of Initial Conditions, P : Circuit parameters, N_x : Number of state variables, t_0 : Initial time, t_f : Final time

1: **for** $t_1^* \leftarrow t_0$ *to* t_f **do**
2: **for** $j \leftarrow 1$ *to* N_x **do**
3: $X_{ext}(t_1^*) = Generate(X_0)$ ▷ external surface of the uncertainty region
4: $X_{max}(t_1^*, j) = -\infty$
5: $X_{min}(t_1^*, j) = \infty$
6: **for** *each state variable* $X_{ext}(j) \in X_{ext}$ **do**
7: $Const = UpdateConstar(j, SSRE, P, X_{ext})$
8: $Grad = UpdateGrad(j, t_1^*, SSRE, P, X_{ext}))$
9: $[X_{max}(t_1^*), X_{min}(t_1^*)] = Global\_Opt(SSRE, j, t_0, t_1^*, P, X_{ext}), Grad, Constr)$
10: $B_{L_{Forward}}(t_1^*) \leftarrow X_{min}(t_1^*)$
11: $B_{U_{Forward}}(t_1^*) \leftarrow X_{max}(t_1^*)$
12: $update\_forward(t_1^*, \Delta_t)$
13: **for** $t_2^* \leftarrow t_f$ *to* t_0 **do**
14: **for** $j \leftarrow 1$ *to* N_x **do**
15: $X_{ext}(t_2^*) = Generate(B_{L_{Forward}}(t_2^*), B_{U_{Forward}}(t^*))$ ▷ external surface of the approximate reachability bounds
16: $X_{max}(t_2^*, j) = B_{U_{Forward}}(t_2^*, j)$
17: $X_{min}(t_2^*, j) = B_{L_{Forward}}(t_2^*, j)$
18: **for** *each state variable* $X_{ext}(j) \in X_{ext}$ **do**
19: $Const = UpdateConstar_B(j, SSRE, P, X_{ext})$
20: $Grad = UpdateGrad_B(j, t_2^*, SSRE, P, X_{ext}))$
21: $[X_{max}(t_2^*), X_{min}(t_2^*)] = Global\_Opt_B(SSRE, j, t_f, t_2^*, P, X_{ext}), Grad, Constr)$
22: $B_{L_{corrected}}(t_2^*) \leftarrow X_{min}(t_2^*)$
23: $B_{U_{corrected}}(t_2^*) \leftarrow X_{max}(t_2^*)$
24: $update\_backward(t_2^*, \Delta_t)$

7). The computed optimization point is then passed to the SSRE model, which uses X_{ext} as initial conditions and generates a partial derivatives (gradient) values that are used to control the stability of the reachability analysis (line 8). The algorithm terminates if the optimization method considers $SSRE(t^*, j, X_{ext}), \forall j = 1, \ldots, N_x$ as an extremum which is the solution returned by the solver; Otherwise the gradient values are used to select new points from the external uncertainty region X_{ext} and the above described steps are repeated. Although this step guarantees the completeness

of the reachability set, the upper and lower obtained reachable sets are highly overbounded due to the wrapping effect. One way to tighten the reachability space is to conduct a backward reachability (lines 16 to 30). Starting from the final computed set (line 18), the backward optimization algorithm is now performed on the AMS circuit SSRE reversed in time in order to compute backward the reachability bounds and consequently, correct the overbounded forward reachability set.

5.1.3 Monte Carlo-Jackknife Statistical Technique

In the sequel, we describe Monte Carlo-Jackknife (MC-JK) technique that we developed in [81]. This technique will be used later on in Section 5.2 to compare the results of the yield estimation and to show the attractable advantages of the proposed reachability analysis based yield estimation.

The Jackknife technique [82] was originally developed as a nonparametric way to estimate and reduce the bias of an estimator of a population parameter. The bias of an estimator is defined as the difference between the expected value of this estimator and its true value. The Jackknife procedure works as follows: First, remove d (a parameter set by the designer) data points and calculate the statistic of interest. Second, calculate the pseudo-values according to Equation (5.3). Then, repeat this process, leaving out d data points at a time to build a distribution of the statistic. Finally, use that distribution to estimate the statistic and its uncertainty. For an estimator S, the i^{th} pseudo-value Jackknife of S was calculated as follows:

$$ps_i = NS - (N-1)S_i \tag{5.3}$$

where S_i is the estimator value for the sample with the i^{th} data point deleted. The Jackknife Confidence Interval (CI) of this estimate for 95% confidence level is then given by:

$$CI_J = \bar{ps} \pm 2\sqrt{\frac{\sigma_J}{N}} \tag{5.4}$$
$$\text{where} \quad \sigma_J = \sum \frac{(ps_i - \bar{ps})^2}{N-1}, \quad \bar{ps} = \frac{1}{N}\sum ps_i$$

Hence, Jackknife reduces the bias of parameter estimates as well as the variance. The detailed procedure for Monte Carlo-Jackknife (MC-JK) based hypothesis testing technique for AMS circuits is illustrated in Algorithm 5.2, where V_{out} represents the observed circuit output with process variation, M denotes the number of MC-JK samples, d is a parameter for the *Delete Jackknife Method* [83], α a chosen significant

Algorithm 5.2 Monte Carlo-Jackknife Verification Algorithm

Require: V_{out}, T_{obs}, α, *test*, M, d
1: $N \leftarrow length(V_{out})$
2: **for** $i \leftarrow$ 1 *to* N **do**
3: $\theta \leftarrow$ Delete Jackknife Method (d, V_{out})
4: $T_{JK}(i) \leftarrow$ Measure Test Statistic (θ)
5: **while** *test* = "*upper tail test*" **do**
6: $CV = quantile\ (T_{JK}, 1-\alpha)$
7: **if** $CV \geq T_{obs}$ **then**
8: *Accept* H_0
9: **else**
10: *Reject* H_0
11: **while** *test* = "*lower tail test*" **do**
12: $CV = quantile\ (T_{JK}, \alpha)$
13: **if** $CV \leq T_{obs}$ **then**
14: *Accept* H_0
15: **else**
16: *Reject* H_0
17: **while** *test* = "*two tailed test*" **do**
18: $CV_L = quantile\ (T_{JK}, \frac{\alpha}{2})$
19: $CV_U = quantile\ (T_{JK}, \frac{1-\alpha}{2})$
20: **if** $CV_L \geq T_{obs}$ **or** $CV_U \leq T_{obs}$ **then**
21: *Reject* H_0
22: **else**
23: *Accept* H_0

level and *test* stands for the type of test to be performed. The algorithm starts with drawing M samples from the circuit output V_{out} of size N by leaving out d samples of

the output at a time (line 3). The deviation between the output and H_0 is computed using a test statistic estimation T_{JK} for each Jackknife pseudo-sample.

Next, the Monte Carlo quantile procedure [84] is employed to measure the critical value by type of test: For an upper tail test (line 5)/lower tail test (line 11), the $1-\alpha/\alpha$ quantiles of the empirical distribution, respectively. In the case of two tailed test, both $1-\frac{1}{\alpha}$ and $\frac{\alpha}{2}$ quantiles define the lower and upper critical values (lines 18-19). Once the critical value is determined, the monitor decides about the satisfaction or violation of H_0.

5.2 Applications

As applications for our proposed methodology, we consider two circuits, namely a ring oscillator, a tunnel diode oscillator and a phase locked loop. In what follows, we estimate the parametric yield through carrying out the proposed method in light of process variation, jitter and initial conditions uncertainties. The obtained yield rates are compared with the MC-JK method and a forward only reachability scheme.

5.2.1 Tunnel Diode Oscillator

Oscillators are integral parts of today's Integrated Circuits (ICs) which require a time reference (clock). One main salient feature of a perfect oscillator is its ability to provide an accurate time reference even in an imperfect environment. A Tunnel Diode Oscillator (TDO) circuit is shown in Figure 5.4. It exhibits an oscillatory behavior when operating in the negative resistance region of the diode V-I characteristic (see Figure 5.5). It was reported that its oscillation property is affected by the temperature, the conductance $G = 1/R$ and the initial conditions [85].

Our goal is to verify the oscillation property in the presence of process variation in

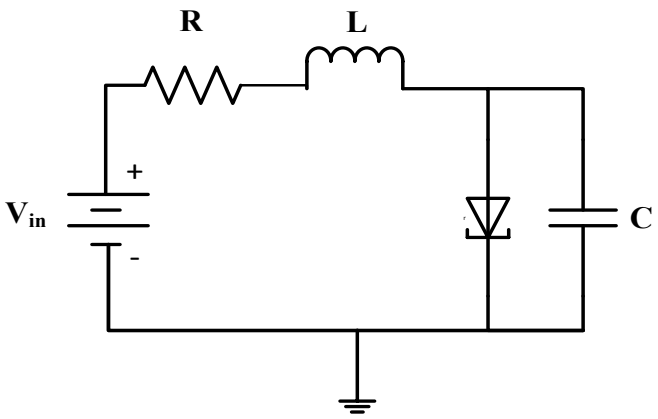

Figure 5.4: Tunnel diode oscillator schematic

$G = 1/R, L$, and C and under a range of initial conditions $X_0 = [X_{0_{min}}, X_{0_{max}}]$ lying in a specic continuous range of values at a nominal temperature ($T = 200K$). The component values R, L and C and the input voltage and current values have been chosen from [85]. The metric of interest in this experiment is the oscillation property with frequency f_{osc}. The desired specification for the TDO is:

$$H_0 : Oscillation \wedge f_{osc} \in [71, 74] \text{ MHz} \tag{5.5}$$
$$H_1 : Lock\_up \parallel f_{osc} \notin [71, 74] \text{ MHz}$$

The circuit was simulated for different conductance values G. Figure 5.6 depicts the output voltage V_c variation in the case of $G = 5m\Omega^{-1}$. It can be seen that the circuit, in this case, generates a periodic signal between *0*V and *0.5*V (Figure 5.6 (a)). Moreover, the state space representation given in Figure 5.6 (b) confirms the successful oscillatory behavior of the TDO circuit. Nonetheless, for a conductance value of $G = 4.13m\Omega^{-1}$, the TDO circuit fails to start-up and sustain oscillation (see Figures 5.6 (c),(d)). The voltage output actually settles to a fixed value which causes the circuit lock-up and hence violates the desired property given in Equation (5.5). Figure 5.7 shows a state space representation of the reachable set as well as

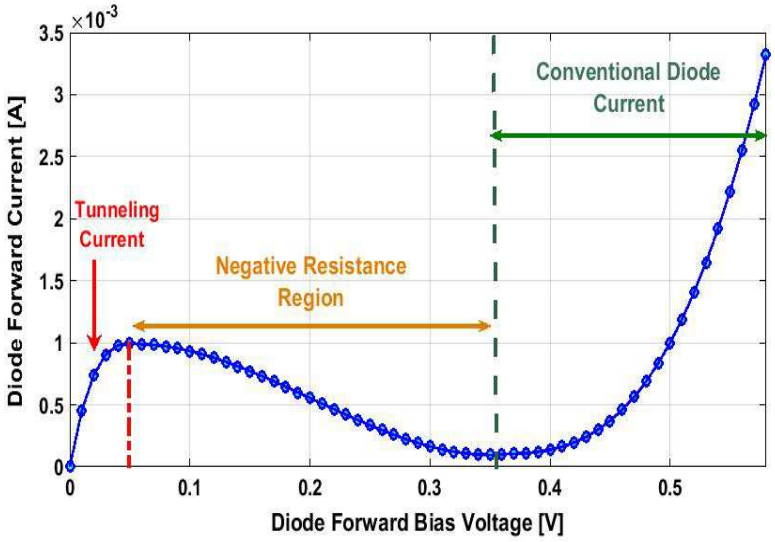

Figure 5.5: Tunnel diode V-I characteristic

the corrected backward reachable set in the case of lock up ($G = 4.13m\Omega$). As it can be noticed, the resultant state space reachable bounds settle to a fixed region which holds up the free stable oscillatory behavior. This confirms the results shown in Figures 5.6 (c),(d). The oscillation verification performance constraint is therefore violated and the verification fails in this case. The TDO is first verified using a variant of the Monte Carlo technique called Monte Carlo- Jackknife (MC-JK) [81], where the failure probability of the TDO property (see Equation (5.5)) is verified under process variation uncertainties. For the process variations in the circuits parameter, 1000 samples were drawn using LHS from the parameters space.

For a fair comparison, these same parameters points were passed to both the MC-JK method and our intertwined forward/backward reachability analysis method. The results of the yield rate estimation are summarized in Table 5.1 in the case of ($G = 5m\Omega$).

It can be noticed that our proposed methodology gives better yield estimation by detecting failures that were not detected by the Monte Carlo-Jackknife (MC-JK)

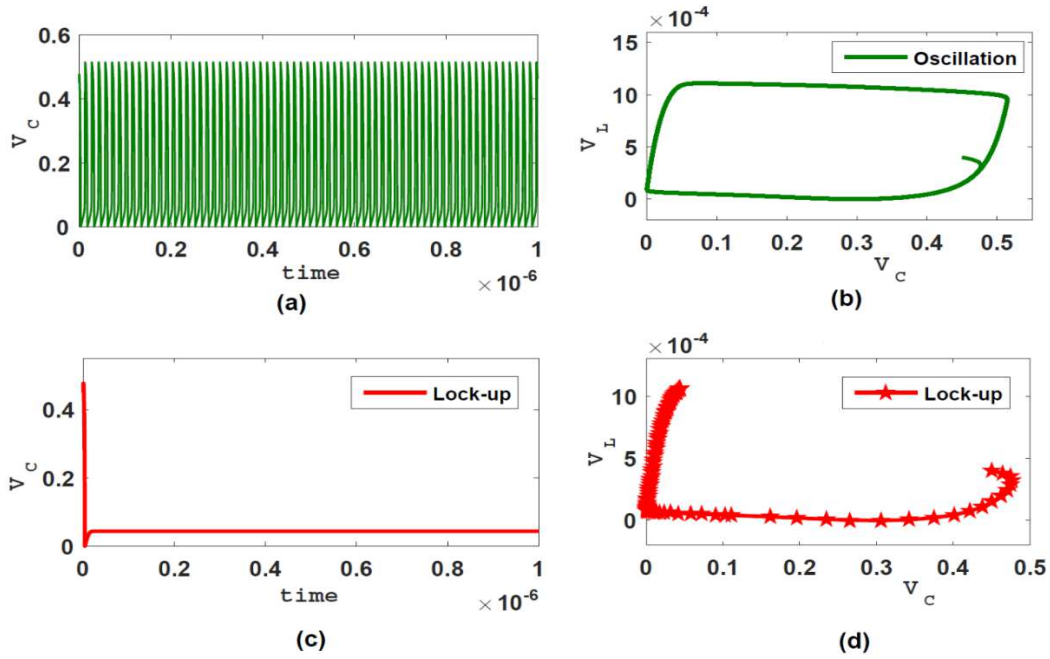

Figure 5.6: Tunnel diode oscillator output for different conductance G

Table 5.1: TDO yield estimation comparison with Monte Carlo-Jackknife method

	MC-JK [81] (%)	Our method (%)	Relative Error (%)
IC Variation Only	92.1	87.7	4.4
PV & IC Variations	88.6	83.3	5.3
Jitter & IC Variations	82.5	76.1	6.4
Jitter & PV & IC Variations	79.9	72.8	7.1

technique [81]. In this sense, the obtained parametric yield rates are over-estimated with up to 7% relative error in light of jitter, process variation and initial conditions uncertainties. In Table 5.2, we present the results of yield estimation for the same scenarios as in Table 5.1 yet for a forward only reachability scheme. The results show the better verification coverage offered by our proposed intertwined reachability technique.

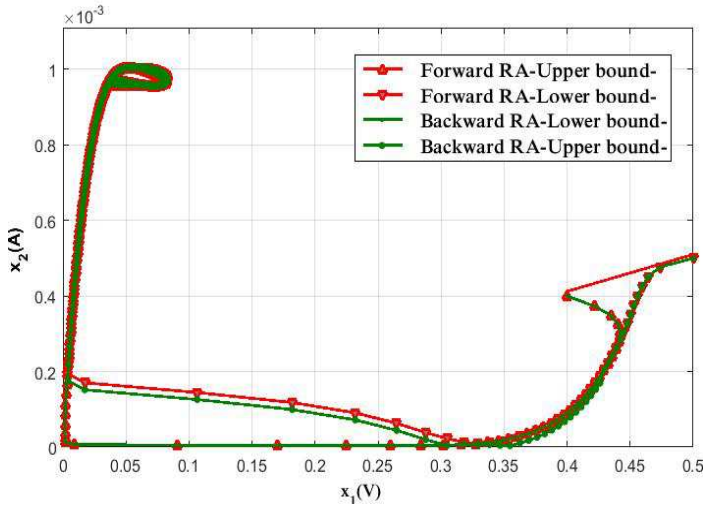

Figure 5.7: Intertwined reachability analysis in the lock-up case

Table 5.2: TDO yield estimation comparison with forward only reachability method

	Forward RA [86] (%)	Our method (%)	Relative Error (%)
IC Variation Only	86.1	87.7	1.6
PV & IC Variations	80.8	83.3	2.5
Jitter & IC Variations	73	76.1	3.1
Jitter & PV & IC Variations	68.1	72.8	4.7

5.2.2 PLL Frequency Synthesizer

The PLL based frequency synthesizer is a basic and essential block of modern communication systems. It is basically a feedback circuit that tries to reduce the phase error between the input and the reference signals. In this case study, we consider a simple frequency synthesizer, that generates an output signal whose frequency is N times the frequency of the reference signal. We consider for this application a *Sine wave* reference signal with a frequency of ω_0, the PLL output is a *Cosine wave* signal with frequency $N \times \omega_0$. Figure 5.8 shows a block based description of a second order PLL based frequency synthesizer. It consists of a reference oscillator, a Charge Pump (CP), a Low Pass Filter (LPF), and a Voltage Controlled Oscillator (VCO). In order

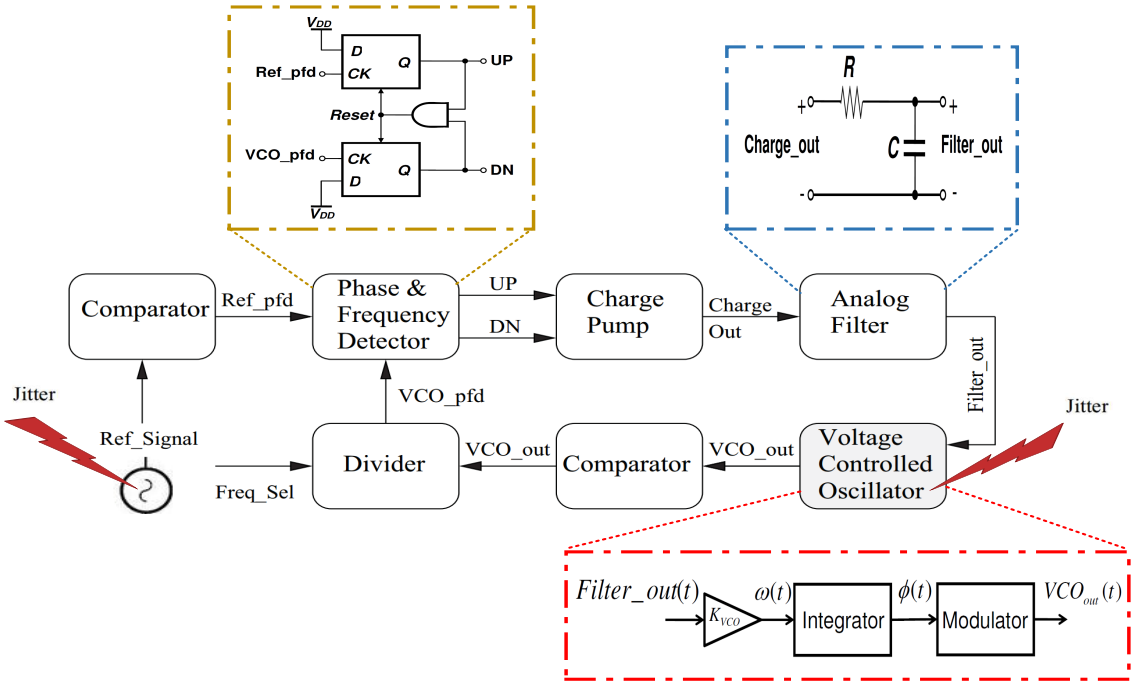

Figure 5.8: PLL design block diagram

to model this PLL using SSREs notation, we need to model each block separately and then link them according to the PLL architecture in Figure 5.8. The noise considered in this case study is the random temporal variation of the phase in the reference oscillator and the VCO block. It is well-known that jitter is the most dominant and critical noise metric in PLL because large jitter can modulate the oscillator signal both in frequency and amplitude. These modulation effects can cause a deviation in the phase from targeted locking range and hence results in a design failure. The efficient verification of PLL for a certain design specification has always been a challenge for circuit designers. We apply the proposed methodology to verify the locking property of the second order PLL design shown in Figure 5.8. The lock time property is a safety property that expresses how fast the frequency synthesizer switches from one frequency to another. The verification of this property is achieved by checking that the PLL reaches the proper DC value within the lock time parameter range which

is $\in [0.002, 0.0024]$ seconds. This property is defined within the ambit of an SSRE model in Equation (5.6), where the SSRE concatenation operator ($\wedge$) indicates that the two Boolean expressions hold simultaneously.

$$Property\_PLL = If(Filter\_out(Lock\_time_{min} + n) \in DC\_level\_range \wedge \quad (5.6)$$
$$Filter\_out(Lock\_time_{max} - n) \in DC\_level\_range, true, false)$$

The verification property is "*For a given confidence level α, and N Monte Carlo trials, what is the probability that the PLL meets the lock-time requirement?*".

In this case, the PLL has been designed with a lock-time in the range of [0.002, 0.0024] sec. Hence, the null hypothesis H_0 and the alternative hypothesis H_1 of Property (5.6) can be, respectively, expressed as:

$$H_0 : \quad lock\_time \in [0.002, 0.0024]$$

$$H_1 : \quad lock\_time \notin [0.002, 0.0024]$$

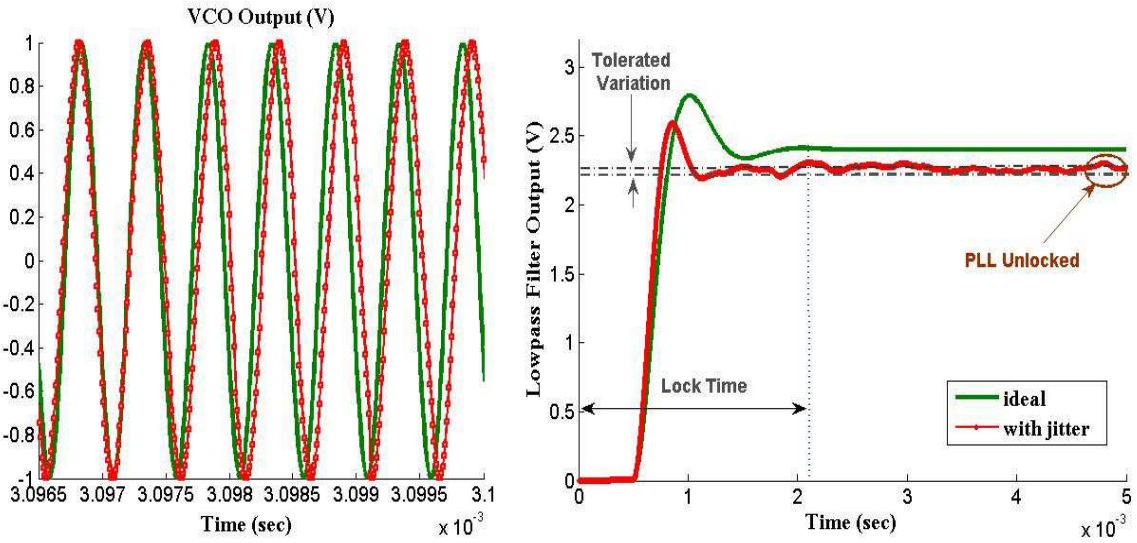

Figure 5.9: PLL output with and without jitter

Figure 5.9 depicts a comparison between the locking property of the PLL design whose parameter values are listed in Table 5.3 with and without jitter.

Table 5.3: PLL circuit parameters

Loop parameters	Value	Unit
VCO gain (K_{VCO})	$4\pi/5$	rad.MHz/V
Loop Filter resistance (R)	10	$K\Omega$
Loop Filter capacitor (C)	10	nF
Charge time parameter	1.0001	–
Divider Ratio (N)	2	–
Natural frequency	1	MHz
VCO operating frequency	1	MHz
Damping Ratio (ξ)	0.05	–
Charge Pump current (I_{CP})	0.25	mA
LPF DC level	2.5	V
Supply voltage (V_c)	5	V

A comparison of the same reachability algorithm without backward refinement [86] for the PLL design is given in Table 5.5. It can be remarked that in the case of jittery PLL (red dotted line in Figure 5.9), the low pass filter outputs do not stabilize to the tolerated DC level and keep fluctuating outside the tolerated range. As a result, the PLL locking property is violated and the verification fails.

From the above discussion, it becomes clear that the verification of the PLL with consideration of jitter is very important when performing reachability analysis. Now, we validate our proposed intertwined forward/backward reachability technique on the jittery PLL design for an entire range of initial conditions and with consideration of parameter variations. The derived forward and backward reachable bounds are shown in Figure 5.10, in which the forward reachability bound is painted in red and the backward reachability bound in green.

In the forward iteration, the reachable set is highly over-approximating the PLL behavior. By performing the backward correction, we were able to tighten up this over-approximation and trace back the circuit dynamics down to the initial condition.

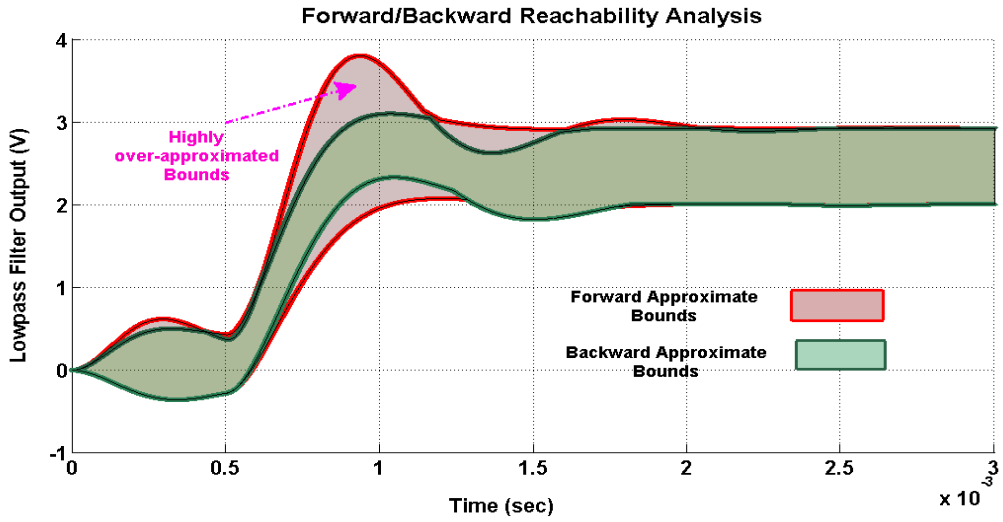

Figure 5.10: Intertwined forward/backward reachability analysis of PLL under jitter

The results of the PLL yield estimation using the Monte Carlo-Jackknife (MC-JK) [81] and our proposed intertwined reachability technique are summarized in Table 5.4. It is worth mentioning that our technique converges in one iteration only while Monte Carlo technique requires thousands of runs. From Table 5.4, it can be noticed that our proposed method finds a lower yield percentage compared to the statistical Monte Carlo scheme in [81]. This can be explained by the fact that our verification approach can weed out PLL locking failures that were not covered in [81]. In addition, the presence of combined jitter, initial conditions and process variations (columns $8-10$) have substantially decreased the PLL yield, meaning the PLL presents more probability of lock failure.

The presence of jitter alone has shown a lower yield rate. This can be justified by the high sensitivity of the VCO block to jitter. The failure of the PLL is not due to lock up (non oscillation) of the VCO but, due to either an "ugly" (i.e., fluctuates outside the tolerated region) or delayed oscillation. The Relative Error (RE) between our proposed approach and the MC technique (columns 4, 7 and 10) becomes more

Table 5.4: Verification results for the PLL lock-time property

N=	Jitter Only			Parameter Variation Only			Jitter & P.V		
	[81]	Our method	RE	[81]	Our method	RE	[81]	Our method	RE
	Yield (%)	Yield(%)	(%)	Yield(%)	Yield (%)	(%)	Yield (%)	Yield (%)	(%)
1000	82.4	74.1	8.3	84.7	79.2	5.5	80.6	71.5	9.1
	83.3	71.7	11.6	80.9	76.3	4.6	78.2	68.9	9.3
	81.7	69.8	11.9	79.2	72.7	6.5	77.5	67.3	10.2
5000	83.6	73.1	10.5	85.8	81.6	4.2	81.8	72.3	8.7
	80.2	72.3	7.9	81.9	77.8	4.1	78.2	70.1	8.9
	79.8	70.8	9	80.7	74.4	6.3	78.2	68.6	9.6
10000	81.7	69.9	11.8	83.6	79.7	3.9	80.2	66.1	14.1
	79.6	67.1	12.5	80.3	74.4	6.1	78.1	62.6	15.3
	78.1	65.9	12.2	81.9	71.8	10.1	76.8	60.1	16.7

RE: Relative Error

pronounced when the number of Monte Carlo trials is increased due to the high MC sampling variance. As stated before, we also performed a comparison between our proposed intertwined reachability analysis technique and the forward solely scheme in [86]. The results of the comparison for different uncertainty scenarios are summarized in Table 5.5. It can be seen that the yield estimate is the lowest under the combined jitter and process variation effects (columns 7-9 in Table 5.5). This confirms the importance of including jitter in the modeling and verification plan of the PLL design. As demonstrated, the proposed approach provides roughly 5% better accuracy in PLL parametric yield estimation, unlike the forward only reachability approach that highly over-approximates the reachable bounds and thus the yield rate.

Table 5.5: Comparison between reachability analysis schemes

Jitter Only			Parameter Variation Only			Jitter & P.V		
Forward [86]	Our method	RE	Forward [86]	Our method	RE	Forward [86]	Our method	RE
Yield (%)	Yield(%)	(%)	Yield(%)	Yield (%)	(%)	Yield (%)	Yield (%)	(%)
69.9	74.1	4.2	76.9	79.2	2.3	66.1	71.5	5.4
67	71.7	4.7	74.5	76.3	1.8	63.3	68.9	5.6
64.5	69.8	5.3	70.1	72.7	2.6	61.2	67.3	6.1

5.3 Summary

We have presented a novel methodology for modeling and verification of nonlinear analog and mixed-signal circuits by computing reachable sets of possible state-space trajectories in the presence of uncertainties. In contrast to methods that use solely forward reachability, the refinement of the reachable state space is carried out in an intertwined forward/backward manner. The resulting set, which contains all periodic and aperiodic time bounded behaviors of the circuit under parameter variation and initial condition disturbance, can be used to verify critical properties such as bounds on voltages, currents, and cycle time (frequency) of embedded designs. Statistical verification based on hypothesis testing is then conducted on the resultant corrected reachable sets for an accurate parametric circuit failure estimation. Experimental results show that our intertwined forward/backward reachability analysis can succeed in accurately estimating the circuit failure rate (a.k.a. yield) by reducing the high over-approximation of the forward scheme in the presence of noise and process variations. However, the proposed method does not handle yield estimation for multiple correlated circuit performances. In the next chapter, we present a multi-yield estimation approach that performs in a high dimensional process parameters space within a reasonable simulation time.

Chapter 6

Multiple Performance Yield Estimation

In this chapter, we focus on verifying multiple transient properties of analog and mixed signal circuits with dynamics described by a system of stochastic recurrence equations (SSREs). A critical yet challenging problem of yield estimation is to account for multiple circuit performance and environmental corners. Unlike the previous chapter where the verification is performed in the time domain, the yield estimation is carried out in the state space domain using a technique developed in the context of nonlinear dynamical system theory.

6.1 Statistical Runtime Verification

An overview of our proposed framework for parametric yield estimation is depicted in Figure 6.1. It comprises a structural verification scheme for yield assessment that consists of two major functional phases:

- After modeling the circuit as a System of Stochastic Recurrence Equation (SSRE)

(that has the form of Equation 2.4), the first phase runs a transient global sensitivity analysis routine. It aims to quantify the impact of process variability on circuit performances as well as to identify critical circuit parameters variation driving the circuit failure. It is conducted in two steps. In the first step, a parameter screening method is adopted to determine which circuit parameters have little impact on the desired performance metrics, such parameters are called non-influential parameters. Hence, a better verification coverage with a lower cost can be achieved through screening out non-influential parameters by setting their values to nominal ones. In the second step, a parameter prioritization method is employed. It is based on a variance based sensitivity analysis wherein sensitivity indices for the influential circuit parameters are derived. Based on the derived sensitivity indices, a prioritized list of influential parameters is generated. Using this prioritized circuit parameters list, we can improve the predictive capability of the yield estimation scheme by using this knowledge of how sensitive is the circuit performance to the variation in their parameters.

- The second phase is the statistical yield estimation scheme. The circuit performance verification is performed through a Joint Recurrence Verification (JRV) scheme. A novel verification metric is developed to score how close is the circuit behavior to the ideal one. The verification is conducted in the state space domain which allows simultaneous multiple performance/outputs verification. The yield rate is thereafter estimated based on a multiple hypothesis testing procedure on the derived performance quality metrics from the JRV scheme.

6.1.1 Transient Sensitivity Analysis

When dealing with the problem of large process variation spaces, a natural verification strategy is to first reduce the parameter variation space by some selection (screening

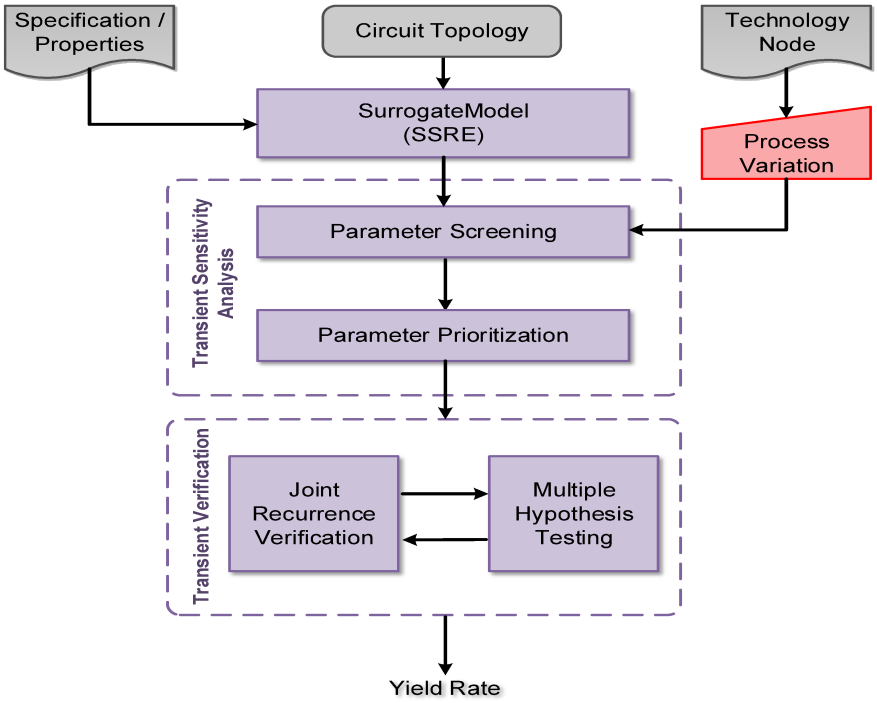

Figure 6.1: Proposed parametric yield estimation approach

or filtering) process, and then to verify the circuit properties on the reduced process parameters set. The main objectives at this step are twofold: First, how to identify the critical parameters or the group of circuit parameters related to the variation in circuit performances; Second, how to determine the interactions between parameters that strongly affect the yield. Our transient sensitivity is adapted from a combination of two techniques: Morris method [87] and Sobol method [88]. Morris is used for process parameter reduction wherein process parameters may be cut down to a subset of parameters that are significantly related to the yield. On the other hand, the Sobol method is deployed for prioritization and weighting of the reduced process parameters.

6.1.1.1 Screening Method

Whereas AMS circuits are subject to different process variations, not all of them are critical to the performances metric of interest. Therefore, only parameter variations

that have a significant impact on these performances should be considered for the yield estimation [89]. The key idea in this preliminary step is to relate the individual impact of parameter variations to the circuit performances variations and subsequently reduce the process parameters space by screening out the non-influential parameter variations in the desired circuit performance. The detailed procedure for Morris based process parameters screening of AMS circuits is given in Algorithm 6.1. The first step of the algorithm is to generate a hyperspace identified by a d-dimensional l-level grid of the parameter variation intervals $p_i = [lb(i), ub(i)] \forall i \in [1, d]$, where d is the number of process parameters. The distance between two consecutive levels is given by Δ (line 1). This hyperspace process parameter is then discretized through the scaled random sampling matrix referred to as the orientation matrix C (line 6) where $J_{(d+1,d)}$ is a $(d+1) \times d$ matrix with all ones, A_s is a $(d+1) \times d$ sampling matrix defined for process parameters in the hypercube $[0, 1]^d$, D^* is a d-dimensional diagonal matrix with elements ± 1 and finally, Pr^* is a $d \times d$ random permutation matrix, in which each column contains one element equal to 1 and all the others equal to 0, with no more than one ones columns in the same position. The influence of the parameter p_s is then evaluated by performing N^* times runs, where we only change a single process parameter at a time between two successive runs of the circuit performance g_k. This process generates a trajectory of N^* points in the parameter space for which several elementary effects at the different randomly selected values p_s are computed. Then, the Elementary Effect (EE), of the process parameter, p_s, on the circuit performance g_k, is calculated for each $s \in [1, d]$ (lines 5-8). Owing to the randomness of EE, we then characterize them using the mean μ^* and standard deviation σ statistics. Based on these statistics, the algorithm computes sensitivity indices (referred to as the Global Indices (GI)) in order to classify the parameters according to the Euclidian distance

Algorithm 6.1 Process parameters screening flow

Require: $P(d), G(m), l, LB, UB, N^*$

1: Compute the step size $\Delta : \Delta = \frac{l}{2(l-1)}$
2: Compute starting process parameter vector $p^* = LB$
3: **for** $s = 1 \rightarrow d$ **do**
4: **for all** $g_k \in G$ **do**
5: **repeat**
6: Calculate the sampling matrix C as follows:
7: $C = J_{(d+1,1)}LB + A_s(D(UB - LB))$ with $A_s = J_{(d+1,d)}p^* + \frac{\Delta}{2}[(2A - J_{(d+1,d)})D^* + J_{d+1,d}]p^*$
8: Compute the Elementary Effects: $E_{(s,k)} = \frac{g_k(C_i) - g_i(C_j)}{\Delta}$
9: **until** $r = N^*$
10: $\mu_k^* = \frac{1}{N^*} \sum_{r=1}^{N^*} \mid E_{(s,k)} \mid$
11: $\sigma_k^2 = \frac{1}{N^*-1} \sum_{r=1}^{N^*} (E_{(s,k)} - \mu)^2$, where $\mu = \frac{1}{N^*} \sum_{r=1}^{N^*} E_{(s,k)}$
12: $GI_s = \max_{k=1,\ldots,m} (\sqrt{\mu_k^2 + \sigma_k^2})$
13: $[P^n, P^i]$ = Assess parameter influence (GI_s)
14: **return** P^n, P^i

(line 12). Finally, the algorithm classifies the process parameter p_s (line 13) according to their influence on the desired circuit performance:

- *Non-influential parameters* having negligible effects on the circuit performances that exhibit a low sensitivity score GI.

$$P^n = \{p_1^n, \cdots, p_{\hat{d}_r}^n\} \subset P = \{p_1, \cdots, p_d\} \tag{6.1}$$

- *Influential parameters* having large linear/non-linear effects with/without interactions on the circuit performances that exhibit a high sensitivity score GI.

$$P^i = P - P^n \tag{6.2}$$

The proposed screening method will allow the removal of statistically insignificant process parameters (i.e., non-critical to the yield estimation) and thereby will reduce the yield analysis problem by the following ratio:

$$\frac{d - \hat{d}_r}{d} \tag{6.3}$$

6.1.1.2 Parameter Prioritization

In this section, we aim to assess how the variation in the circuit performance can be apportioned to the different sources of variations in both electrical and physical circuit parameters that were identified in the parameter screening step as influential parameters. To this end, novel measures should be introduced to quantify the circuit process parameters and the correlation thereof according to their influence on the AMS circuit output/performance. Consider P^i the set of $\hat{d}_p = d - \hat{d}_r$ influential process parameters which follow a certain distribution, and $f(x)$ a circuit performance of interest depending on these parameters. It is assumed that f is a second order random variable $f \in L_2(U^{\hat{d}_p})$. Therefore, f has a unique Sobol-Hoeffding decomposition as detailed in Section 2.2. Owing to the orthogonality of the Sobol-Hoeffding decomposition, the variance of the circuit performance can be decomposed as:

$$V(X) = V_X + \sum_{i=1}^{\hat{d}_p} V_i + \sum_{1 \le i \le j \le \hat{d}_p} V_{ij} + \ldots + V_{1,2,\ldots,\hat{d}_p} \tag{6.4}$$

where $V_i, V_{ij}, \ldots, V_{1,2,\ldots,\hat{d}_p}$ denotes the partial variance w.r.t a subset of the circuit parameters of the Sobol-Hoeffding circuit performance decomposition $X_i, X_{ij}, \ldots, X_{1,2,\ldots,\hat{d}_p}$ (defined in Equation 2.9), respectively.

$$\begin{aligned}
V_i &= V(E(X|p_i)) \\
V_{ij} &= V(E(X|p_i,p_j)) - V_i - V_j \\
V_{ijk} &= V(E(X|p_i,p_j,p_k)) - V_{ij} - V_{ik} - V_{jk} - V_i - V_j - V_k \\
&\vdots \\
V_{1,\ldots,\hat{d}_p} &= V(f) - \sum_{i=1}^{\hat{d}_p} V_{ij} - \sum_{1 \le i \le j \le \hat{d}_p} V_{ij} - \ldots - \sum_{1 \le i_1 < \ldots < i_{\hat{d}_p - 1} \le \hat{d}_p} V_{i_1,\ldots,i_{\hat{d}_p}-1}
\end{aligned} \tag{6.5}$$

Therefore, the Sobol-Hoeffding decomposition is a rich means of analyzing the respective contribution of individual or sets of parameters to circuit performance variability.

From the decomposition in Equation 6.4, sensitivity indices $(S_i, S_{ij}, \ldots, S_{1,\ldots,\hat{d}_p})$ can be naturally derived by normalizing the partial variances by $V(X)$ to get the relation:

$$1 = \sum_{1}^{\hat{d}_p} S_i + \sum_{1 \leq i \leq j \leq \hat{d}_p} S_{ij} + \ldots + S_{1,2,\ldots,\hat{d}_p} \tag{6.6}$$

where the order of the sensitivity indices S_i is equal to $|i| = Card(i)$. Whereas, a more abstract characterization is required to replace the $2^{\hat{d}_p} - 1$ contributions defined in Equation 6.6 which leads to an intractable number of contributions as $\hat{d}_p$ increases. To facilitate the characterization and hierarchization of the respective influence of each parameter p_i, we introduce new sensitivity indices: the main effect (also called first order term) and the Total Sensitivity Indices (TSI). The TSI of a parameter i, denoted by TSI_i, is defined as the sum of all sensitivity indices including all interactions effects involving parameter i.

$$TSI_i = S_i + S_{(i,\sim i)} = 1 - S_{\sim i} \tag{6.7}$$

where $S_{\sim i}$ is the sum of all the $S_{1,2,\ldots,\hat{d}_p}$ associated to the different process parameters excluding the parameter p_i. Thus, the circuit parameter variations priorities are defined according to their importance through their TSI values. As a rule of thumb, parameters with TSI greater than 0.8 are considered as "very high priority", between 0.5 and 0.8 "high priority", and between 0.5 and 0.3 "less priority" in the next yield analysis stage [90]. The circuit influential process parameters set (P^i) is therefore weighted according to the process parameters total sensitivity indices and denoted as weighted process parameters:

$$P^w = \{w_i p_i \mid w_(i) = \frac{TSI^i}{\sum_{j=1}^{\hat{d}_p} TSI_j}\} \tag{6.8}$$

6.1.2 Transient Verification

In the previous stage of the methodology, we have performed transient sensitivity analysis to characterize P^w as a set of weighted process parameters reflective of the influence of the process parameters in the circuit performances of interest. The objective of this stage is to verify the circuit transient behavior in order to estimate the yield in light of the joint effect of the weighted process variation and initial condition fluctuation. We make use of the defined weighted process variation parameters to generate a short and purposeful sampling scheme from the process variation space.

6.1.2.1 Joint Recurrence Verification

Recurrence Quantification Analysis (RQA) is a technique developed by the nonlinear dynamic theory community to verify complex nonlinear systems [91]. In this section, we propose a variant from RQA technique called Joint Recurrence Verification (JRV) technique for the multi-performances verification of AMS circuits influenced by process variation.

6.1.2.1.1 Joint Recurrence Verification Concept

A conceptualization of this technique is shown in Figure 6.2. It aims to find recurrent patterns between an ideal/golden circuit output and multiple non-ideal outputs due to process variation by verifying their occurrence in their respective state space domains. Thus, it permits to develop recurrence quantifiers for both temporal and frequency domain properties of the circuit. Unlike frequency domain analysis, JRV takes into account the initial conditions variation of the circuit. It also handles different natures of circuit behavior like transient and invariant behaviors. Moreover, it can detect state changes in drifting circuits without necessitating any constraining assumptions on the

output signal stationarity nor statistical distribution. It basically depicts the different

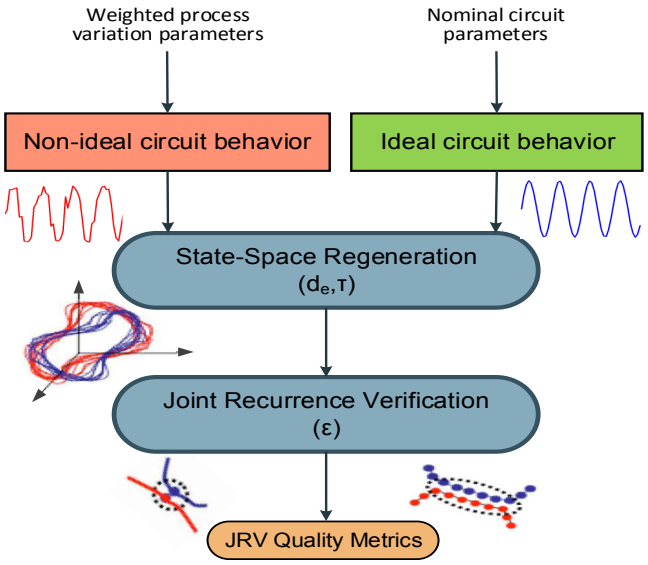

Figure 6.2: Joint recurrence verification scheme

occasions when similar circuits states are attained even at distinct times. Given the SSRE circuit model, we simulate the circuit under nominal design parameters and for the weighted process parameters in order to get a set of ideal/non-ideal circuit responses. Since the verification is conducted in the state space, we will need to regenerate the dynamics of both circuit responses in the state domain. These dynamics are thereafter verified using the JRV technique for a given radius threshold (ϵ); A distance matrix (called joint recurrence map), which represents the closeness of all possible state vectors pairs is then computed. The main advantages of the proposed approach upon existing quality matching techniques is its ability to automatically handle horizontal offset, frequency offset, and start-up delay.

6.1.2.1.2 Joint Recurrence Verification Implementation

The implementation of the JRV technique is summarized in Algorithm 6.2.

Algorithm 6.2 Joint Recurrence Verification based method

Require: P^w, $p_{nominal}$, G, IC

1: $x_{ideal} \leftarrow SSRE(p_{nominal}, mean(IC))$
2: $X_{non-ideal} \leftarrow SSRE(P^w, IC)$
3: $(\tau^i, d_e^i) \leftarrow Embedding\ dimension(x_{ideal})$
4: **State space representation**
5: $y_{ideal} \leftarrow Delay\_vector(x_{ideal}, d_e^i, \tau^i)$
6: $Y_{non-ideal} \leftarrow Delay\_vector(X_{non-ideal}, d_e^{ni}, \tau^{ni})$
7: **Joint Recurrence matrix computation**
8: $JR(i,j) \leftarrow \Theta(\varepsilon - \|y_{ideal}(i) - Y_{non-ideal}(j)^1\|) \cdot \ldots \cdot \Theta(\varepsilon - \|y_{ideal}(i) - Y_{non-ideal}(j)^k\|), \forall k \in \mathbb{R}^{\hat{d}_p^w}$
9: **JRV metrics computation**
10: $p^\epsilon(l) \leftarrow \sum_{m,n=1}^{N_c} \{(1 - JR_{m-1,n-1}) \cdot (1 - JR_{m+1,n+1}) \prod_{k=0}^{l-1} JR_{m+k,n+k}\}$
11: $RR = \frac{1}{N-k} \sum_{j-1=k} JR(i,j)$
12: $L_{max} = Max(p^\epsilon(l))$
13: $RP = -\frac{1}{\ln(T_{max})} \sum_{t=1}^{T_{max}} Y_{non-ideal}(t) \ln(Y_{non-ideal}(t))$
14: **return** $JRV_{metrics}$

From the transient sensitivity stage of the proposed methodology, the circuit process parameters are associated with different weights according to their TSI. Therefore, a sampling procedure that draws appropriate samples from this weighted process parameter set P^w is developed. It aims to minimize the simulation effort while achieving full coverage of the uncertain parameters space. Afterwards, non-ideal output sequences, denoted $X_{non-ideal}$, are generated from the drawn process parameter samples (line 2). Given these non-ideal circuit state space vectors $Y_{non-ideal}$ and the ideal state space vector y_{ideal}, we study the similarities/dissimilarities (i.e., recurring properties and patterns) of these two circuit outputs. To do so, a tolerance parameter called threshold radius ϵ is defined. This tolerance parameter specifies the maximum allowable deviation difference in terms of Euclidean distance between the two circuit outputs to be considered recurrent. The matching quality between these two sequences are then derived using the JRV technique. The circuit outputs are first generated in the multi-dimensional state space domain (lines 4-6). The embedding lag τ and the embedding

dimension d_e are computed using the Mutual Information function [92] and the False Nearest Neighbours function [64], respectively. Thereafter, the algorithm reconstructs the different state space circuit responses according to Taken's theorem [93] for the computed embedding dimensions. Next, the joint recurrence matrix (lines 7-8) is generated. It is computed as the Hadamard product of the recurrence matrix of the ideal circuit response and the recurrence matrix of the non-ideal circuit response in light of process variation (line 8). The recurrence matrix can be described by the following equation:

$$\Theta(i,j) = \begin{cases} 1 & \text{if } \|y_{ideal}(i) - Y^{k}_{ideal}(j)\| < \varepsilon \\ 0 & \text{else} \end{cases} \tag{6.9}$$

where Θ represents the Heaviside function. The obtained JR matrix locates the recurrent points whenever a similar state space behavior jointly occurs on both circuit output sequences x_{ideal} and $X_{non-ideal}$. In other words, it checks if the state space trajectories $y_{ideal}(i)$ at time i and $Y_{non-ideal}(j)$ at time j fall within the predefined threshold radius ϵ. The patterns between the two output sequences are revealed by recurrence points and diagonal lines in the JR matrix. The closer the two outputs are, the more diagonal lines occur in the recurrence matrix. Subsequently, the frequency distributions of the diagonal lines lengths in JR are computed for each diagonal parallel to the main diagonal $JR(i-j=r)$ for r equal to a constant (line 10). Finally, the interplay between the circuit outputs is characterized by the following measures (lines 11-13):

- The *recurrence rate* RR which reveals the percentage of matching (i.e., the probability of the occurrence of similar state) in both circuit outputs.

- The *maximum joint sequence* L_{max} that is the longest uninterrupted period of time that both circuits stay attuned.

- The *Recurrence periodicity RP* which reflects the periodicity of the circuit in the state space.

6.1.2.1.3 Radius Selection

How much recurrence we get in the JRV scheme depends on the value of the threshold parameter ϵ. If the selected ϵ is too small, there may be almost no recurrence points and the verification more likely fails. Conversely, if ϵ is selected too large, this will entail a large number of false recurrence points due to the tangential motion (i.e., counting every coordinate in state space as recurrent) and so the verification will be biased. Hence, the question that arises is, "*which values of* ϵ *one should consider*?". To this end, Algorithm 6.3 is proposed to determine the optimal ϵ value for any circuit output.

Algorithm 6.3 JRV threshold radius computation

1: $\mathcal{O} \leftarrow Compute\_Centroid(y_{ideal})$
2: $Distances = \sqrt{(y_{ideal}(:,1) - \mathcal{O}_1)^2 + (y_{ideal}(:,2) - \mathcal{O}_2)^2}$
3: $[maxRadius, maxRadiusIndex] = Max(Distances)$
4: $\epsilon_{optimal} = 0.05 * maxRadius$;
5: **return** $\epsilon_{optimal}$:Optimal Threshold Radius

The centroid is first computed using *Green's theorem* [94]. The threshold radius ϵ is then chosen 5% of the maximum possible distance from the centroid of the circuit output attractor up to the boundary of that attractor (coordinates of the farthest point from centroid) as recommended in the literature [91].

6.1.2.2 Multiple Hypothesis Testing

The goal of this step is to estimate the total yield rate for multiple performances in terms of the generated JRV metrics. On the one hand, the generated joint recurrence

verification quality metrics (RR, L_{max}, $RPDE$) gives an idea of how close the circuit behavior to the ideal one, yet, each metric reflects a different circuit performance. On the other hand, the JRV measures are correlated and clearly a separate verification of these measures is not adequate as demonstrated in Equation 2.18 (i.e., $P_{overlap}$ fraction will be omitted and so the yield rate is over-estimated). Therefore, we use a statistical inference procedure and extend the statistical runtime verification scheme proposed in [49], which regards the verification as a single hypothesis testing problem.

Our approach is based on a simultaneous statistical inference of the probability that a set of circuit performance specifications are met in the presence of process variation and/or initial conditions fluctuations with a certain level of confidence α. With such an approach, we do not need to estimate the overlay in an acceptance region expressed in the overlap yield $P_{overlap}$. Hence, the total estimated yield rate will be directly assessed. Furthermore, the proposed simple yet elegant multiple hypothesis scheme allows a direct accurate multiple performance yield computation in a convenient way by controlling the trade-off between computational burden and accuracy.

In the sequel, we detail the proposed multiple hypothesis testing procedure. When conducting the yield estimation, the number of null hypotheses, m, is known in advance and corresponds to the number of performance metrics of interest G. However, the number of true and false null hypotheses H_{0_j}, m_0 and m_1, respectively, have to be determined (see Table 2.2). When estimating the yield, Type II errors are not as disastrous as Type I errors. More importantly, when pursuing multiple performances verification, there is a potential increase in the chance of committing Type I errors $(1-\alpha)^m < (1-\alpha)$ since $\alpha \in [0,1]$. Hence, to guarantee an accurate yield estimation, the control of this type of error is needed. Also, the test statistics (formulated as JRV metrics) are dependent and correlated. Thus, we devise a scheme

which minimizes V while accounting for correlations between the tests. To do so, we implemented a hypothesis testing scheme based on controlling the errors committed by falsely rejecting null hypotheses H_{0_i} denoted by *False Discovery Rate* (FDR) [95]:

$$FDR = \mathbb{E}[\frac{V}{R} \mid R > 0]Pr(R > 0) \tag{6.10}$$

where V is the number of false positive, and R is the total number of rejected H_{0_i}.

The detailed FDR based AMS circuits yield estimation procedure is summarized in Algorithm 6.4.

Algorithm 6.4 FDR controlling procedure for yield rate computation

Require: $JRV_{metrics}$, G, α, $type\_test$
1: $\mathcal{H} \leftarrow$ set hypothesis$(G, JRV_{metrics})$
2: $N_{failure} \leftarrow 0$
3: **for** $i = 1 \rightarrow m$ **do**
4: **for** $j = 1 \rightarrow N$ **do**
5: $\mu_i \leftarrow$ mean$(JRV_{metrics}(j, i))$
6: $\sigma_i \leftarrow$ standard deviation $(JRV_{metrics}(j, i))$
7: $T_{obs}(i) \leftarrow$ compute test statistic$(JRV_{metrics}(:, i), \mu_i, \sigma_i)$
8: **for** $j = 1 \rightarrow N$ **do**
9: **for all** $H_i \in \mathcal{H}$ **do**
10: $(A(j), R(j)) \leftarrow$HT$(T_{obs}, type_test, JRV_{metrics}, \alpha)$
11: $R = \sum R(j) = V + S$
12: $p_i \leftarrow$ compute p-value (H_i)
13: $P \leftarrow sort(p_i)$
14: $l \leftarrow max\{p_i : P(i) \leq \frac{i}{m}\frac{\alpha}{\sum_{i=1}^{m} 1/i})\}$
15: **for all** $k = 1 \rightarrow l$ **do**
16: $H_{0_i} \leftarrow$reject hypothesis H_{0_k}
17: $R_{corrected}(j) \leftarrow R - l$
18: **if** $R_{corrected}(j) \geq 1$ **then**
19: $N_{failure} \leftarrow N_{failure} + 1$
20: $p_{failure} = \frac{1}{N}\sum_{k=1}^{N} N_{failure}$
21: $Yield \leftarrow 1 - p_{failure}$

First, we retrieve the metrics generated on the JRV stage. They are then used to define the null hypotheses that link them to the specification (line 1). This is followed by the computation of the standard score to determine the observed circuit JRV metric test

statistic T_{obs} (loop between lines 3 and 7) for each performance metric $g_i \in G$. The next step is the nonparametric FDR procedure as p-value adjustment repeated for N trials (loop between lines 8 and 19). We choose the p-value adjustment procedure because adjusted p-values permit a direct interpretation against a chosen significant level α and so eliminate the need for lookup tables or knowledge of complex hypothesis rejection rules. The adjustment procedure starts by defining the acceptance and rejection regions under the assumption of $H_{0_i} \in \mathcal{H}$ being true according to the type of test statistic (line 10). Then, the decision regarding whether each of the null hypotheses H_{0_i} holds or not is made. Thereafter, the FDR procedure is carried out in order to compute the false discovery proportion l. Afterwards, the number of actual rejections is corrected (line 17). Upon the rejection of one hypothesis H_{0_i} (i.e., violation of its corresponding performance metric g_i), we increment the probability of failure counter $N_{failure}$. Finally, the probability that the desired performances are satisfied in the presence of parameters variation is estimated as the percentage of samples with successful hypothesis over the total number of simulation runs. The parametric yield rate is thus defined in line 21 in terms of the probability of circuit failure.

6.2 Applications

In this section, we demonstrate the efficiency of the proposed parametric yield estimation approach described in this chapter on two benchmark circuits: A five stage-ring oscillator and a Phase Locked Loop (PLL).

6.2.1 Five Stage Ring Oscillator

We consider verifying a five-stage ring oscillator circuit as shown in Figure 6.3. The node voltages of each of the five inverters have been designed to oscillate at an operating frequency $f_{nom} = 4.5$GHz. The performance metrics of interest are the oscillation frequency and the start-up delay time measured using transient simulation (specifications are listed in Table 6.1).

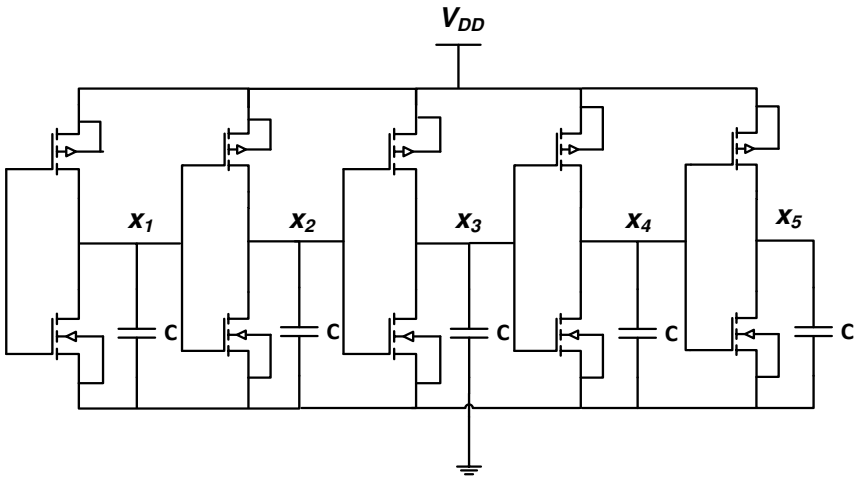

Figure 6.3: Five stage CMOS ring oscillator

The circuit performances are affected by process parameters as well as the operating conditions (V_{DD} and initial conditions). We consider process variations in the parameters of each NMOS and PMOS transistor. In addition, we take into account

Table 6.1: Specifications for five stage ring oscillator

Performance metric	Specification
Oscillation frequency	$f_{nom} \pm 2\%$
Start up time	$\tau_{start\_up} \leq 35$ ns

fluctuations in the power supply voltage V_{DD} and initial conditions. The process parameters, transistor width W, channel length L, threshold voltage V_{th}, and the gate oxide thickness T_{ox} are introduced into each transistor M_i, $i = 1, \ldots, 5$ which results in 40 process parameters in total for both NMOS and PMOS transistors. By considering variations in initial conditions $x_{\forall i=1..5}(0)$ and power supply voltage V_{DD}, the yield estimation problem rises to a 46-D problem. Consequently, our objective is to determine the yield of the circuit for these 46 random circuit parameters for the circuit specification given in Table 6.1. Figure 6.4 shows the transient simulation behavior of the five stage ring oscillator for different initial condition (IC) values . Comparing the different start-up delay time, it can be observed that initial conditions have a strong effect on the start-up delay time. Indeed, by sweeping the initial voltages in the node voltages of the five inverters, the start-up delay time changes remarkably, especially for $IC(x_i) = 1e^{-4}V$ whereby the start-up time performance constraint is violated.

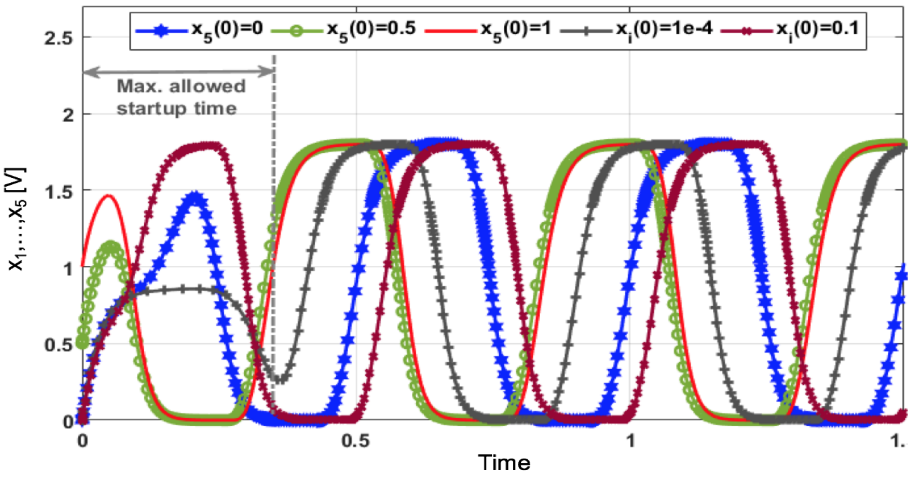

Figure 6.4: Start-up time dependency on the initial conditions

As a first step, we carry out our process parameters reduction and scoring scheme in order to estimate the impact of the joint effect of process variation and initial conditions variations on the ring oscillator frequency and start-up delay time. A Gaussian

distribution with mean m fixed to nominal value and 3σ variation is considered for each process parameter while a uniform distribution with 10% variation is adopted for initial condition variations. The Morris screening method was carried out for $l = 10$ and $N^* = 30$ to assess the sensitivity of the ring oscillator behavior to the above-mentioned process parameters. The highest mean μ^* value identifies the most important process parameters. The order of importance is considered through the μ^* ranking. In Figure 6.5, a graphical representation of the (μ, σ) Morris elementary effects is depicted to show the results for one of the five inverters process parameters. It can be observed in Figure 6.5 that the Morris elementary effects identified five important parameters out of eight for each inverter, which reduces the yield estimation problem from 46-D to 31-D (i.e., $5 \times 5 + 5 + 1$). Therefore, only these selected 31 parameters are chosen for the scoring scheme using the Sobol variance based sensitivity analysis and later on for the statistical transient verification scheme to estimate the yield rate. We carried out a Sobol global sensitivity analysis to relate the reduced set of parameter variations to the circuit performances variations.

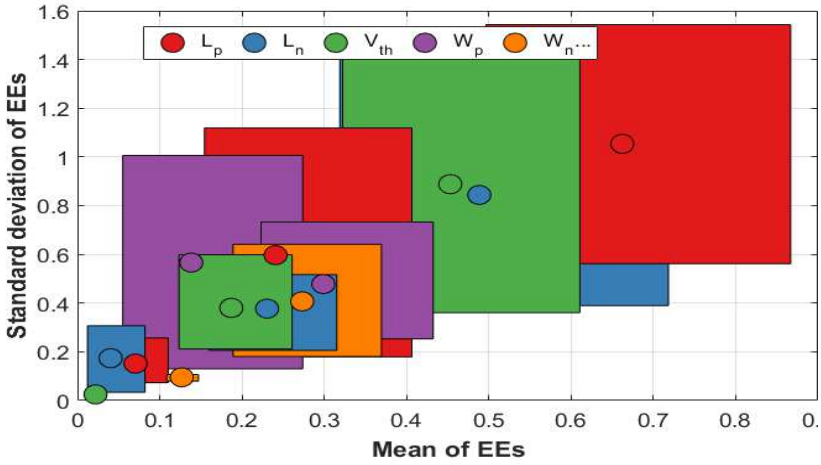

Figure 6.5: Process parameters screening for ring oscillator

For illustration purposes, we show in Figure 6.6 the main and total Sobol sensitivity indices on the ring oscillation frequency for one inverter parameters of the ring chain.

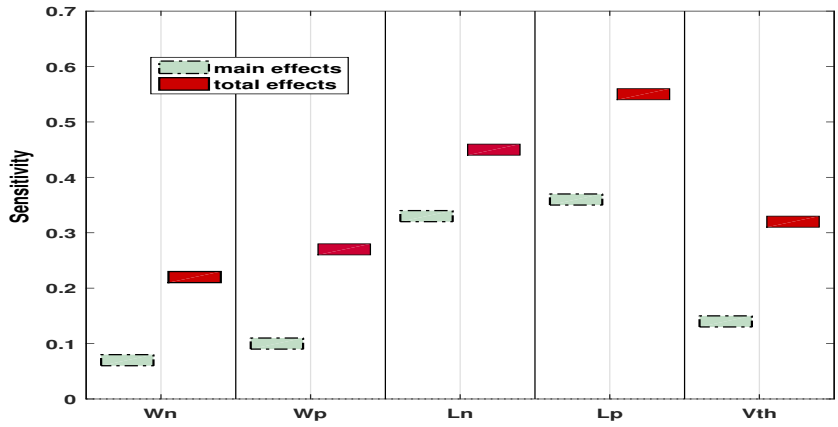

Figure 6.6: Process parameters prioritization for ring oscillator

The sensitivity analysis results are in good agreements with the Morris sensitivity in Figure 6.5. In fact, the variation in the sizes (width (W), and length (L)) of both PMOS and NMOS transistors and the threshold voltage (V_{th}) have an impact on the circuit oscillation frequency. To score the importance of each of these circuit parameters, the amount of variation that is explained by the main Sobol indices near one indicates that these parameters are more influential. Among all possible sources of process variations, the length gate L and threshold voltage V_{th} are the dominant parameters with the highest sensitivity indices 0.36 and 0.18, respectively. This can be justified by the random dopant effect [96]. Furthermore, a high correlation between parameters can be noticed through the gap between main and total effect indices. This is not surprising as the transistor threshold voltage fluctuation is directly related to the size of a transistor according to the following relation: $\sigma V_{th} \propto \frac{k}{\sqrt{WL}}$. The obtained indices will be used to guide the sampling selection in the JRV scheme in order to focus the verification on the parameters that affect the most the yield rate. The

JRV setup parameters are as follows: embedding dimension $d_e = 3$, embedding delay $\tau = 31$ and the tolerated radius $\varepsilon = 0.02$ ns. The relation between the performance of interest and the JRV metrics is shown in Figure 6.7.

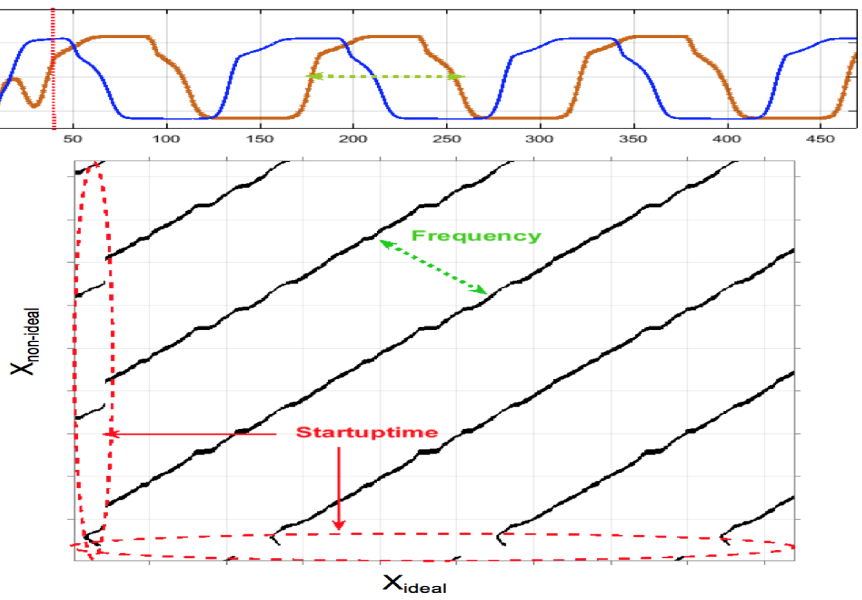

Figure 6.7: Relation JR matrix and circuit performances

The variation on the recurrence rate RR and maximum joint sequence L_{max} computed using the proposed joint recurrence verification scheme for transistors width variations are shown in Figures 6.8 and 6.10, respectively. Both the recurrence rate and the maximal joint sequence confirm the results reported in Figure 6.6. In fact, they both fluctuate significantly while varying the design parameters, especially in the case of threshold voltage variation V_{th}. More particularly, the maximal joint sequence increases linearly with the transistor width (Figure 6.8) and exponentially with the V_{th} (Figure 6.9). These obtained JRV schemes are used to assess the yield.

The accuracy and efficiency of the proposed multiple yield analysis methodology are compared with those of primitive MC, and its variants namely, LHS-MC and QMC based on $N = 1000$ simulation trials. The verification was carried out under the

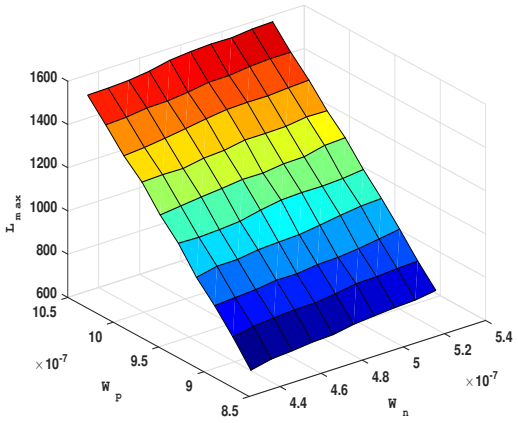

Figure 6.8: L_{max} variation with the transistors width

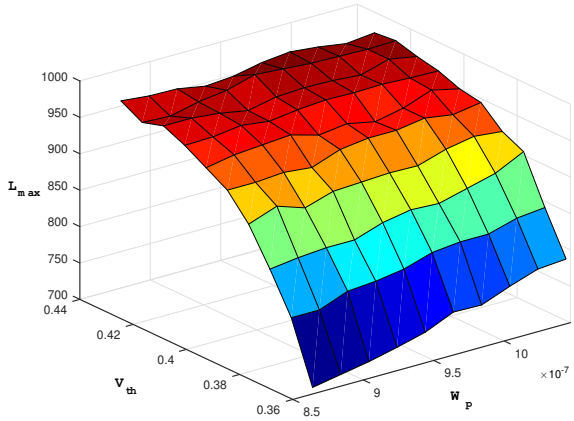

Figure 6.9: L_{max} variation with the PMOS transistor width and threshold voltage

confidence levels $\alpha = 0.05$ and for initial conditions following a uniform distribution model. The primitive Monte Carlo is considered as the base for the comparison in terms of speed-up and relative error. From Table 6.2, the results of the comparison show that the performance of the MC variants do not achieve significant improvement when compared to the primitive Monte Carlo analysis method. Indeed, QMC is able to reach the MC golden result with a 2.26 speedup, while the LHS-MC method is 1.93X faster than MC with approximately the same yield rate. This is due to the bad exploration of the process variation space during the sampling trials.

Table 6.2: Yield estimation results for ring oscillator

IC ranges	$x_i = 0.01, \forall i = 1, \cdots, n$					
	$x_5 \in [0, 0.5]$			$x_5 \in [0.5, 1]$		
	Yield rate	Error $\|.\|$	Speedup ratio	Yield rate	Error $\|.\|$	Speedup ratio
MC	0.887	–	1×	0.891	–	1×
LHS-MC	0.884	0.003	1.93×	0.889	0.002	1.98×
QMC	0.889	0.002	2.26×	0.896	0.005	2.32×
Our method	0.911	0.024	8.81×	0.925	0.034	9.76×

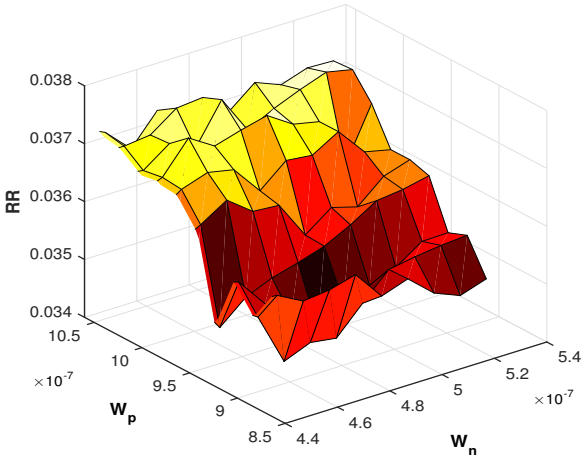

Figure 6.10: Recurrence rate while varying the PMOS and NMOS transistors width

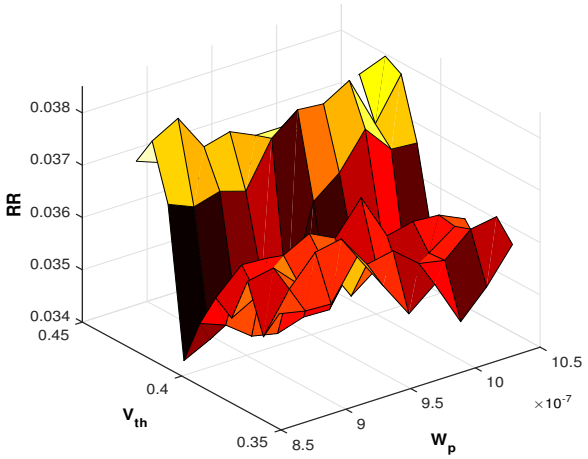

Figure 6.11: Recurrence rate while varying the PMOS transistor width and threshold voltage

Moreover, the ignorance of the high correlation effect between process parameters results in the ignorance of some special worst case combined effects. It can also be observed for the case of $x_5 \in [0.5, 1]$ (columns 5-7) that our proposed method reduces the runtime up to 9.76× in comparison with the conventional MC analysis, with no more than 3% relative error in estimated yield. It is also interesting to see that when the initial states get farther away from the equilibrium states, the circuit is subject to more failures and consequently, lower yield rates are obtained (columns 2-4). This can be explained by the direct dependency of the start-up time performance metrics on the initial conditions of the ring oscillator. For instance, when varying the initial conditions on the node voltages, the oscillation takes a longer time to settle when the initial conditions are too far from their DC values which is in good agreement with the results shown in Figure 6.4.

6.2.2 Phase-Locked Loop

Phase-Locked Loop based circuits (PLL) are key mixed-signal building blocks widely used in various applications. It is essentially a closed-loop feedback system with a challenging highly nonlinear behavior. A simplified block diagram of a PLL-based frequency synthesizer is depicted in Figure 6.12.

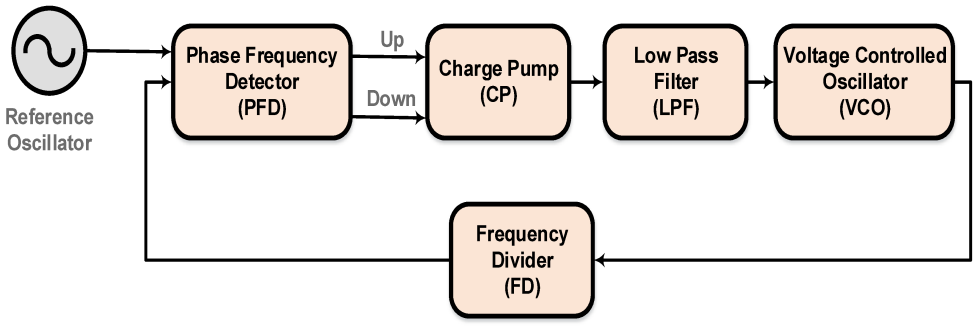

Figure 6.12: Conventional PLL frequency synthesizer

A formal rigorous yield analysis of PLL is a very challenging task. In practice, simulation is the common practice for the verification of the PLL to its desired performances [97]. However, several limitations of classical s-domain analysis based on a continuous-time approximation of PLL operability have been reported in [98]. For instance, classical linear analysis is not rich enough to describe many crucial and hidden dynamics due to the following two reasons: First, it does not comprehend the sampling nature due to the discrete-time operation of the Phase Frequency Detector (PFD). Therefore, it can result in a degraded performance particularly in terms of jitter peaking. Second, since s-domain analysis is a steady-state analysis it does not predict the nonlinear acquisition process of the PLL. In general, PLL designs need to satisfy the requirement of fast settling/locking time while maintaining a low-jitter in order to maximize the yield. The PLL design under verification needs to satisfy the

transient and invariant performance requirements given in Table 6.3 to avoid yield loss.

Table 6.3: Specifications for PLL design

Performance metric	Specification
Lock-time	$t_{lock} \leq 1.5$ ms
Period jitter	$J_{period} \leq 5.62$ ns
Stability	$\Delta_v \pm 0.05$ V

Apart from process variations, PLL circuits are also susceptible to the external (environmental) noise. Environmental noise sources (e.g., substrate or shot noise) seriously degrade the performance of a PLL circuit by inducing timing jitter and increasing the limit cycle. In this application, we consider the most dominant noise in PLL designs stemming from shot noise in the VCO block and manifesting itself as accumulation jitter (a.k.a. FM jitter) [99]. The noisy VCO output due to the intrinsic jitter is afflicted according to the following Equation:

$$Out_{VCO} = A\ cos(\omega_0 t + K_V \int_0^t \frac{Out_{LPF}(\tau)}{1 + J\theta \frac{K_V Out_{LPF}}{2\pi}} d\tau + \phi_0) \tag{6.11}$$

where J stands for the jitter deviation, K_V is the VCO gain, Out_{LPF} is the filter output, ϕ_0 is the initial phase, and θ a zero mean unit-variance Gaussian random process. We performed our JRV method on the PLL application for an embedding dimension $d_e = 3$ and an embedding lag $\tau = 15$.

Table 6.4: PLL yield estimation results for $\alpha = 0.05$

	Case I: without jitter			Case II: with VCO jitter		
	Yield rate	Error $\|.\|$	Speedup ratio	Yield rate	Error $\|.\|$	Speedup ratio
MC	0.9531	–	1X	0.8972	–	1X
LHS-MC	0.9543	1.2e-3	1.78X	0.8985	1.3e-3	1.82X
QMC	0.9547	1.6e-3	2.23X	0.8980	1.8e-3	2.46X
Our method	0.9559	2.1e-3	9.87X	0.8998	2.6e-3	11.53X

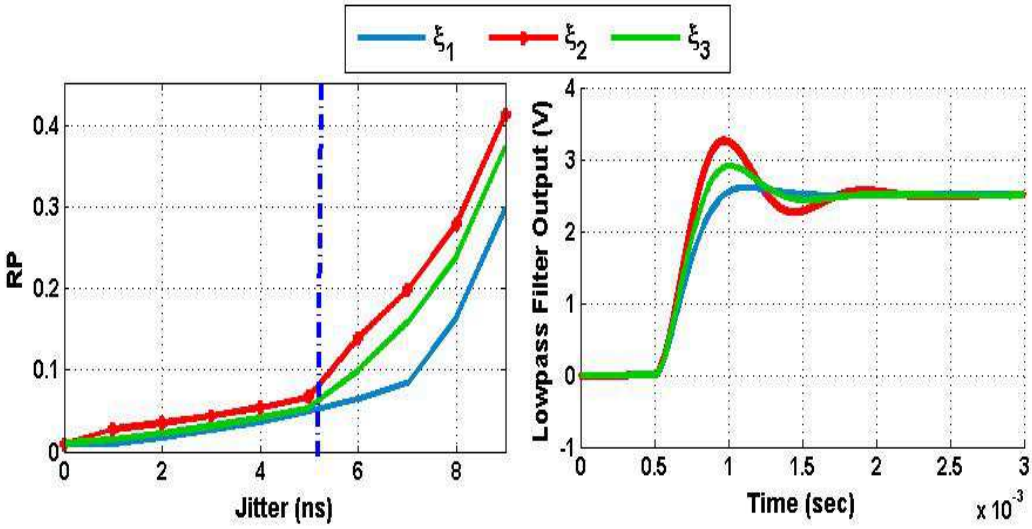

Figure 6.13: Recurrence periodicity for different damping factors

Table 6.5: PLL yield estimation results for $\alpha = 0.01$

	Case I: without jitter			Case II: with VCO jitter		
	Yield rate	Error $\|.\|$	Speedup ratio	Yield rate	Error $\|.\|$	Speedup ratio
MC	0.9386	–	1X	0.98806	–	1X
LHS-MC	0.9403	1.7e-3	1.58X	0.8825	1.9e-3	1.72X
QMC	0.9405	1.9e-3	2.17X	0.8826	2e-3	2.23X
Our method	0.9413	2.7e-3	9.16X	0.8817	2.9e-3	10.94X

Figure 6.13 plots the recurrence periodicity (RP) for different damping factors ($\xi_1 = 0.1$, $\xi_2 = 0.5$, and $\xi_3 = 0.707$, respectively). It can be noticed that a longer settling time is required for the PLL to achieve a lock while increasing ξ. This can be also seen through our JRV RP measure. In fact, for $\xi_3 = 0.707$ (red line in Figure 6.13) higher RP values are attained than those for $\xi_1 = 0.1$ and $\xi_2 = 0.5$. This means that the PLL presents less periodic outputs. In fact, the closer its value to 0, the closer the PLL is from its ideal behavior. In addition, the variation of the VCO jitter with the recurrence periodicity shows an exponential increase for values greater than $5.62ns$.

The resulting JRV metrics are employed in the multiple hypothesis testing scheme for different confidence levels $\alpha = 0.05$ and $\alpha = 0.01$. In this application, the three JRV metrics (RR, L_{max}, and RP) are employed in the multiple hypothesis testing scheme for different confidence levels $\alpha = 0.05$ and $\alpha = 0.01$. The obtained parametric yield results are shown in Tables 6.4 and 6.5 and compared to the MC method and its variants in light of process variation and jitter uncertainty. The presence of process variation alone has shown higher yields. However, the yield rates incorporating both jitter disturbance and process variations have shown lower rates (columns 5). It is obvious that the combined process variation/jitter effects will result in more PLL failures to satisfy its desired specifications due to the high sensitivity of the VCO to noise disturbances. The yield comparison for different confidence levels showed a slight dependency of the yield assessment results on the confidence level α. However, the yield accuracy would change to a very small degree (less than 0.003%) For instance, in the case $\alpha = 0.01$, slightly lower yield rates are obtained compared to those reported for $\alpha = 0.05$. In short, the hypotheses tests results can be slightly different for different confidence intervals and the accuracy would be compromised if the confidence level is too high or too low. Lower confidence level would increase the rejection; Higher confidence level, on the other hand, would increase the error margin and degrade the accuracy. A significant simulation-time saving (more than 10X reduction) resulting from using our proposed methodology has been remarked. The savings come from two distinct mechanisms. First, the sensitivity analysis approach (a) reduces the process parameters dimension space by fixing the non-influential parameters on the desired circuit performances to their nominal values; (b) prioritizes the parameter variation selections according to their influence on circuit performances; and (c) reveals hidden worst performances due to interactions between different parameters

variations. Second, the multi-performances yield estimation scheme is conducted simultaneously through a multiple hypothesis testing procedure. On the contrary, multiple single performances simulations runs are performed using primitive MC which results in an over-estimated yield due to the correlated PLL performances wherein rejection regions overlap. The relative yield estimation error with respect to the number of simulation runs of the primitive MC and the proposed method are compared in Figure 6.14. The relatively small number of the required simulations runs shows the efficiency of our approach, by which it was possible to have at least a 9 times computational cost gain without paying in terms of accuracy.

6.2.2.1 Discussion

To corroborate the process parameter reduction results obtained using the Morris sensitivity method, we perform a MC simulation on the reduced and non-reduced process parameters set. The aim of this experiment is to confirm that the non-significant parameters identified through the Morris method does not actually significantly affect the yield results.

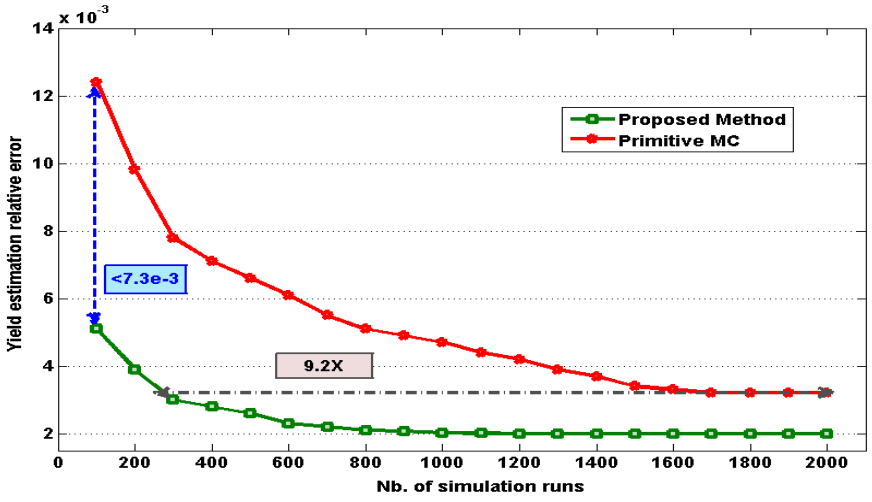

Figure 6.14: Effectiveness of our proposed approach

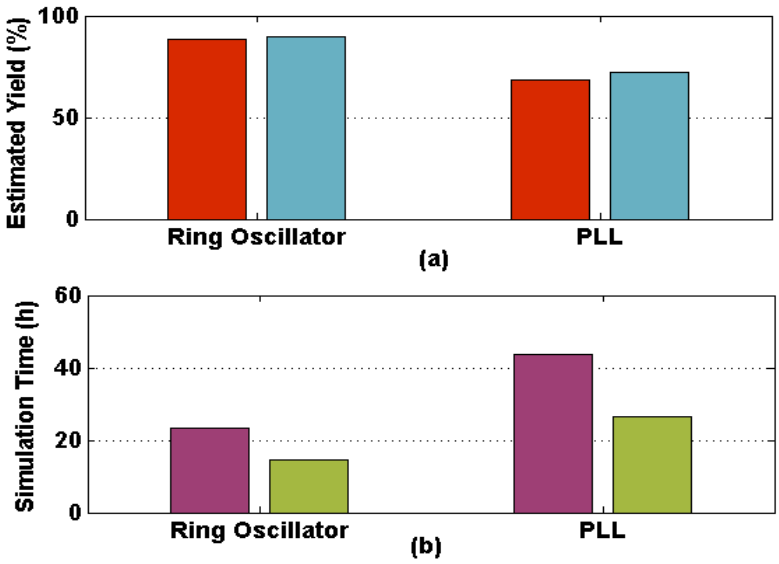

Figure 6.15: Effectiveness of the proposed screening method

Figure 6.15(a) compares the yield rate estimate using primitive MC simulations before and after process parameter reductions for ring oscillator and PLL design. The obtained yield analysis fully confirms the Morris results, since for both applications the estimated yield rate accounts for less than a maximum of 2% error rate. Hence, this confirms the capability and effectiveness of our proposed process parameters screening approach in identifying the actual non-significant parameters variation on the circuit performances of interest which substantially reduces the computational time. This is confirmed by Figure 6.15(b) wherein a notable simulation-time saving resulting from our parameter screening scheme is observed by removing redundant non statistically significant simulations as compared to the primitive MC without considering the reduction for both PLL and ring oscillator circuits.

6.2.3 Three Stage Ring Oscillator

In this section, we apply the proposed surrogate based optimization and verification methodology described in Section 1.3 on a three stage ring oscillator depicted in Figure 6.16. The circuit was first optimized in order to generate a fundamental oscillation

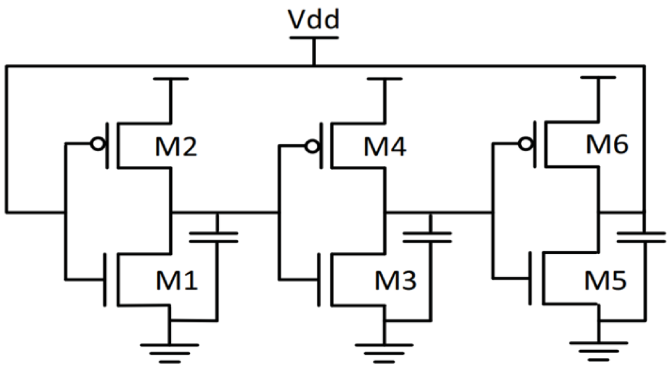

Figure 6.16: Three stage CMOS ring oscillator

frequency of 3.2 MHz. The lengths of all transistors are fixed to 65 nm. The proposed space mapping optimization engine is applied to compute the width of PMOS and NMOS transistors. Using the symmetry constraints, the computed optimal parameters are as follows: the width of all PMOS transistors is $W_{p_i} = 3$ μm and the width of all NMOS transistors is $W_{n_i} = 2.5$ μm. After the circuit optimization, we need to verify the circuit dynamics. More specifically, we want to ensure that for the computed optimal parameters, the circuit will not drift into a chaotic behavior when it is subject to process variation uncertainty.

The ring oscillator dynamics are governed by the following E-SREs:

$$
\begin{aligned}
x_1(n+1) &= if(true,\ x_3 - \frac{1}{C}\delta_t(I_n(x_3(n), x_1(n), gnd, p) - I_p(x_3(n), x_1(n), V_{dd}, p)), 1) \\
x_2(n+1) &= if(true,\ x_1 - \frac{1}{C}\delta_t(I_n(x_2(n), x_1(n), gnd, p) - I_p(x_2(n), x_1(n), V_{dd}, p)), 1) \\
x_3(n+1) &= if(true,\ x_3 - \frac{1}{C}\delta_t(I_n(x_2(n), x_1(n), gnd, p) - I_p(x_2(n), x_1(n), V_{dd}, p)), 1) \\
V_{out}(n+1) &= if(true, x_3(n+1), 0)
\end{aligned}
$$

where x_1, x_2, and x_3 stand for the state variables of the ring oscillator model that represent the node voltages in each inverter and V_{out} is the circuit output. The functions I_n and I_p model the nonlinear current generated by the NMOS and PMOS transistors, respectively, based on their gate, drain and source voltages. The verification is performed in the presence of process variation in transistor widths (both PMOS and NMOS) and threshold voltage. The surrogate based dynamics verification is applied on the three stage ring oscillator using the Gaussian Kernel correlation dimension d_c as test statistic of the hypothesis testing procedure. Figure 6.17 depicts the attractor of the circuit in the case of the optimal circuit parameters.

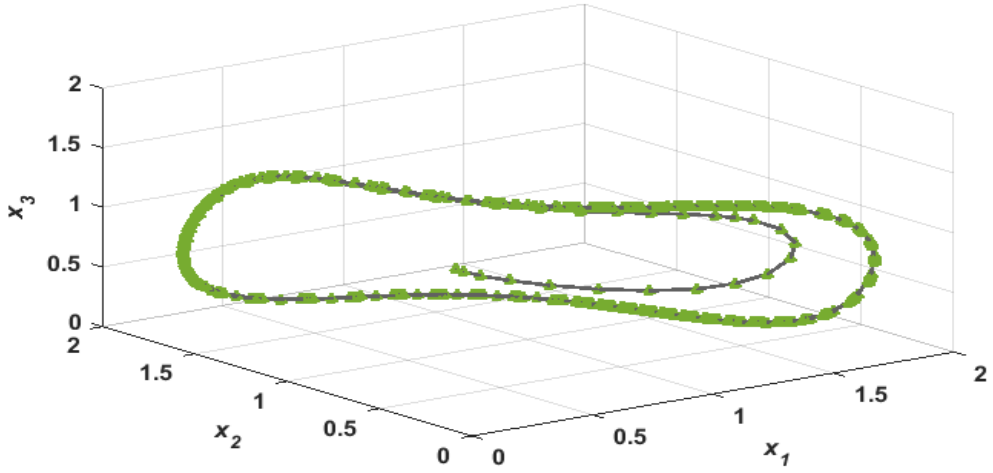

Figure 6.17: Attractor of the optimized ring oscillator circuit

We computed the embedding window, mainly the correlation dimension $d_e = 2$ using the false nearest neighbor (FNN) method and the embedding lag $\tau = 6$ using mutual information (MI) method, respectively. The result of the verification is shown in Figure 6.18 for 100 surrogates of the circuit outputs. An acceptance region (shown as the white region in Figure 6.18) and a rejection region (red region of Figure 6.18) of the noisy/chaotic dynamics are then defined from the obtained correlation dimensions d_c

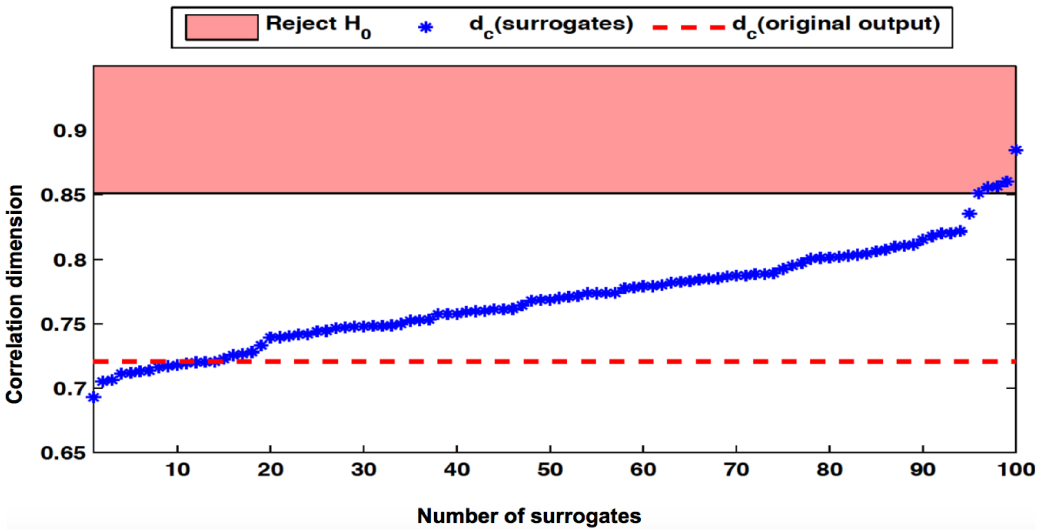

Figure 6.18: Results of the verification of the three stage ring oscillator circuit

using hypothesis testing for a confidence level of 95%. The circuit output is located in the acceptance region of noisy dynamics which proves the non-chaotic behavior of the circuit. In other words, the proposed surrogate dynamics verification method demonstrated that the ring oscillator circuit presents a chaos free dynamics. Thus, the optimized ring oscillator complies with the required dynamics of non-chaotic behavior.

The next step will be to verify the circuit robustness to process variation in terms of yield. To do so, we applied our surrogate based robustness verification method to analyze the effect of process variation and initial conditions uncertainties ($\forall x_i \in [0, 1]$) on the frequency of oscillation (f_{osc}) and the rise time (τ_r). First, the intertwined reachability analysis method is performed considering only the frequency of oscillation (f_{osc}) as the performance metric of interest. The results of the verification are compared with 1000 Monte Carlo simulation trials and summarized in Table 6.6. The yield rates computed using the Monte Carlo method are over-estimated when compared to the yield estimation using our reachability analysis method. For instance, our intertwined reachability analysis method offers a better verification coverage and

Table 6.6: Single performance verification of the three stage ring oscillator

	Intertwined Reachability Analysis	Monte Carlo	Relative Error
Initial Condition Variations	92.78%	94.61%	1.83%
Process Variation	86.13%	89.82%	3.69%
Jitter	83.52%	87.70%	4.18%
Process Variation and Jitter	79.84%	85.17%	5.33%
Process Variation, Jitter and Initial Conditions Variations	77.26%	84.35%	7.09%

hence gives more accurate yield estimation of the frequency of oscillation metric. However, Monte Carlo has a poor coverage and so fails to detect some cases where the required performance metric is not met. This results in a lower probability of failure and consequently higher yield. It can also be observed that in the presence of jitter, process variation, and initial condition uncertainties, the circuit presents the lowest yield.

We also verified the three stage ring oscillator in the case of two performance constraints using our statistical runtime verification technique based on the JRV method. The yield estimation results are depicted in Table 6.7.

Table 6.7: Multiple performances verification of the three stage ring oscillator

	Statistical Runtime Verification	Monte Carlo	Relative Error
Initial Condition Variations	90.94%	93.31%	2.37%
Process Variation	84.76%	89.22%	4.46%
Jitter	81.83%	87.61%	5.79%
Process Variation and Jitter	76.02%	83.13%	7.11%
Process Variation, Jitter and Initial Conditions Variations	74.21%	82.17%	7.96%

We validated the obtained yield against 1000 Monte Carlo simulation trials. It can be remarked that the proposed method for multiple performance constraints presents a

lower yield when compared to the yield estimated for a single performance constraint as shown in Table 6.6. Moreover, it can be noticed that the presence of jitter affects most the oscillation period and rise times. For instance, the estimated yield for jittery circuit is 5.81% less than the one estimated in the presence of process variation.

6.3 Summary

A critical yet challenging problem of yield estimation is to account for multiple circuit performances. In this chapter, we proposed a novel nonparametric statistical verification methodology to efficiently estimate the parametric yield for multi-performance constraints. Our proposed approach exploits the fact that circuit parameters variation has different impact on the circuit performance. Hence, a global sensitivity analysis classifies the circuit parameters according to their influence on the desired circuit performances. Based on this classification, an efficient Joint Recurrence Verification technique is performed on the most critical design parameters. The verification is conducted in the state space domain where new verification metrics are defined. A multiple hypothesis testing procedure is then performed based on the computed metrics. It enables a simultaneous yield analysis rather than multiple single-performance yield estimation with less run-time overhead. Experimental results showed that our methodology prevails over Monte Carlo technique in yield rate assessment. It has demonstrated up to 11.53X computational reduction capability while retaining accuracy.

Chapter 7

Conclusions

7.1 Conclusions

In contrast to the widely automated digital design flow, analog design is still predominantly manual relying on the designer's experience and expertise. Analog and mixed signal circuits verification is not automated at all, whereas the sizing step is partly automated in practice. For instance, although few commercial optimization tools exist, they are used only as a support tool, for example to fine tune a certain parameter of an already designed AMS circuit. The main encountered challenges are the following: the optimization was shown to be an *NP-hard* problem, the wide feasible design space whereof an exhaustive coverage of the design search space is unattainable, and therein the accuracy of the design solutions is not guaranteed. Furthermore, existing verification and yield estimation techniques rely mainly on simulation which is prohibitively expensive and a time consuming process. The aforementioned reasons show the need for robust tools that would automate the sizing and verification part of the analog design flow. The goal is to maximize the number of fabricated circuits whose performance satisfies a set of acceptability constraints dictated by the desired

specifications.

In the course of pursuing successful tape-out with sufficient design-for-manufacturability AMS design, this thesis proposes a novel methodology for nonlinear AMS circuit optimization and verification as well as the subtleties to implement it in practice. We proposed different new methods and algorithms to bypass certain limitations of existing methods.

The first contribution of this thesis is the development of a nominal sizing procedure that ensures an exhaustive coverage of the design space and outputs guaranteed optimum design solutions. To this end, we proposed a formally coupled equation based and simulation based approach inspired from equivalence checking technique. Given the circuit topology and the specification properties, the feasible design space is defined. Thereafter, a global sensitivity based approach is adopted to scout the defined design space and constrain the design space to regions where promising solutions might be expected to be found. Subsequently, these prominent design subspaces are passed to the nominal sizing step. The underlying nominal sizing approach employs a space mapping scheme between a surrogate and a detailed AMS circuit model to find the optimal design solution.

The second contribution of this thesis is the development of a typical qualitative verification approach to verify whether the circuit well-behaves in light of process variation. More importantly, the developed approach ensures that even the possible deviations in the circuit parameters do not drive the circuit into inappropriate dynamic (e.g., chaotic behavior). It is on a new verification strategy denoted by surrogate based method based on statistical proof by contradiction. The proposed method is robust and successfully discriminates noisy from chaotic behavior for different types of noise while traditional techniques such as Lyapunov Exponent method fail to do so.

The third contribution is the elaboration of a qualitative verification approach that enhances the capability to predict parametric yield estimation for nonlinear analog and mixed-signal circuits. Prior to performing multiple performances yield calculation, a single performance scheme is proposed based upon a geometrical computation of the reachable states using an intertwined forward/backward reachability analysis method. A non-parametric univariate hypothesis testing approach is then conducted on the resultant reachable behavioral bounds to assess the yield. Furthermore, a multi-performances yield estimation approach that combines the advantages of transient sensitivity analysis, joint recurrence verification, a method inspired from DNA matching, and multiple hypothesis testing techniques is developed.

In order to show the relevance in practice of the approaches presented in this thesis, we applied them on several analog and mixed signal circuits benchmarks, namely amplifier, oscillators, and phase locked loops. Comparisons of the obtained results with the existing approaches have demonstrated a significant computational reduction capability while retaining robustness in applicability. In summary, the proposed nonlinear AMS circuits optimization and verification methodology can be seen as a first step for a semi-formal optimization and verification approach and a basis for automatic analog designs generation. It offers a promising solution to reduce design cycle time while maintaining accuracy.

7.2 Future Work

This thesis lays the ground for a promising framework for the early optimization and verification of analog and mixed signal designs. Building on the proposed methodology and experimental results presented in this thesis, several enhancements and directions of further research can be explored and pursued. More features can be incremented

to scale and strengthen the capabilities of the proposed methodology in order to handle complex designs with a multitude of real imperfections and more stringent performances. In the sequel, we outline some future research directions:

- In its present form, the methodology considers only process variation. This spatial unreliability effects can be immediately detected right after fabrication. However, temporal unreliability effects vary with the time and the operating conditions (e.g., the operating voltage, temperature, switching activity). Consequently, they are extremely hard to detect and cannot be fixed nor recovered. An interesting extension of this work can be the integration of transient faults uncertainty such as aging effects (Negative-Bias Temperature Instability (NBTI)) [100] and transient effects (Single Event Transients (SET) [101], and of particular concern, Single Event Upsets (SEU) [102]).

- Another possible direction for future work refers to the improvement of the imperfections models by deriving them directly from transistor/layout level simulations as well as the integration of multi-stage nonparametric verification of multiple circuit performances. In addition, novel approaches from the nonlinear dynamical theory can be adopted to discriminate simple chaos from hyperchaos which have different application domains.

- Other global sensitivity analysis scheme such as Fourier amplitude sensitivity testing method can be explored for the class of linear AMS circuits. The research direction is to incorporate different transient sensitivity analysis methods based on the circuit classes in the *Spice* simulator in order to guide the selection process of Monte Carlo instances and consequently remove statistically insignificant parameters. By doing so, a significant reduction in the computational cost

through avoiding unnecessary simulation iterations as well as improvement in the simulation accuracy for a fixed number of runs can be achieved.

- In our circuit sizing methodology, we only consider optimization of circuit performances. However, analog IC designers not only call for optimized sized topologies but also need high robustness and yield in light of Process, Voltage, and Temperature (PVT) variations. This limitation can be addressed through: (1) extending the global sizing approach to handle regional sensitivity analysis to the circuit yield; (2) integrating design centering strategy in the space mapping procedure used for nominal sizing. In this case, the optimization process seeks the values of circuit parameters which not only optimize the circuit performance but also maximize the probability of satisfying the design specifications (i.e., both parametric and catastrophic yield maximization) in an integrating manner avoiding costly re-design iterations.

- Finally, it would be interesting to generalize the circuit surrogate models to handle more severe process variations. Of particular concern, local process variation (a.k.a mismatch) can be combined with global process variation. Subsequently, both process variation uncertainties can be considered to ensure that the AMS circuit under verification is still robust.

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[Cf2] I. Seghaier, and S. Tahar: Reliability Analysis of CMOS Rambus Oscillator

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