Feedback methods for inductorless bandwidth extension and linearisation of post-amplifiers in optical receiver frontends

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Abstract

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Marc-Alexandre Chan

Optical communication is increasingly important in today's telecommunications. It is not only a key component in long-haul infrastructure, but is also being brought into new applications within the datacentre, at the circuit board and integrated circuit level, and in next generation mobile networks. This thesis proposes feedback tuning approaches in order to address two challenges within optical receiver analog frontend circuits: a) the dynamic response of a prior bandwidth extension technique; and b) linearity optimisation.

To address dynamic response, we begin with a prior inductorless method of bandwidth extension using positive feedback loops. In a multi-stage post-amplifier with local positive feedback loops, we propose an approach which tunes each positive feedback gain separately, and we demonstrate that this achieves better dynamic response and eye opening than the prior equal-feedback-gain approach. We additionally present a root-locus analysis as a means of characterising dynamic response and suggest some design guidelines based on this analysis.

To address linearity optimisation, we propose the use of an interleaving negative-feedback post-amplifier topology, previously used only for bandwidth extension. We investigated the relationship between the feedback gains and linearity and developed a design approach for linearity optimisation. We designed and fabricated two 70 dB 6 GHz optical receiver circuits, making use of two different post-amplifiers, in order to compare different design approaches. We achieved a linearity of 0.08 dBVrms OIP3 (quasi-static) and a THD of 0.195% at 1 GHz.

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And gab about tech and society.

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For her patience, when I had none;
For her support, when I lost footing;
For each discussion held my mind
Open to the world beyond
The MOSFET.

Contribution of Authors

The work described in Chapter 3 of this thesis was co-published in the proceedings of the Midwest Symposium on Circuits and Systems 2015 [1] with Weihao Ni and Prof. Glenn Cowan (supervisor). All work performed by Ni is presented in Section 2.7 as part of the literature review. Work by the author is presented in Chapter 3, alongside comparisons to Ni's results. The text presented in that chapter was prepared specifically for this thesis.

Contents

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List of Abbreviations

BER Bit error rate

BW Bandwidth

CHA Cherry-Hopper amplifier

CMOS Complimentary metal oxide semiconductor (field effect transistor) technology.

dBVrms Unit of power: dB referenced to 1 V rms

ESD Electrostatic discharge

GaAs Gallium arsenide, a compound semiconductor used for electronics

GBW Gain bandwidth product. Also GBP

IIP3 Input-referred IP3

IMD3 Intermodulation distortion, third-order

InP Indium phosphide, a compound semiconductor used for electronics

IP3 Third-order intercept point, a measure of linearity

IRN Input-referred noise

ISI Inter-symbol inteference

LNA Low-noise amplifier, an RF front-end amplifier

MOSFET Metal-oxide semiconductor field effect transistor

NMOS n-channel MOSFET

OIP3 Output-referred IP3

OOK On-off keying

PA Post-amplifier

PAM Pulse amplitude modulation

PMOS p-channel MOSFET

PRBS Pseudo-random bit stream

QAM Quadrature amplitude modulation

QPSK Quadrature phase-shift keying

RF Radio frequency

rms Root mean squared

SiGe Silicon-germanium, a semiconductor alloy used for electronics

THD Total harmonic distortion

TIA Transimpedance amplifier

Chapter 1

Introduction

Optical links have found a wide variety of uses in the transmission of data and signals. One of the most notable is in digital communications: optical links form an essential part of long-haul communication networks, are increasingly important within datacentres and are beginning to find new application as an interconnect at a board or integrated circuit level. Other applications are also in common use or emerging, such as medical imaging, microwave photonic signal processing, and radio-over-fibre for next-generation mobile networks.

At each end of an optical link is typically an electrical system, so the signal must be converted from electrical to optical and back. The optical/electrical interface, or receiver, converts the received optical signal into an electrical current by means of a photodiode and then into a voltage and amplified by means of an analogue frontend circuit. This last circuit is the focus of this work.

One of the classic, and continuing, challenges of frontend circuit design is the need to handle increasing data rates. At a circuit level, the frontend must normally have a higher analogue bandwidth to handle higher data rates. A number of methods exist to extend bandwidth, which often comes at a tradeoff of poorer dynamic response (overshoot and ringing).

For some keying and modulation schemes used to transmit data, such as pulse amplitude modulation (PAM) or quadrature amplitude modulation (QAM), linearity is also a key challenge. Given the prevalence of on-off keying in optical communications, where linearity is less important, limited literature exists on linearity optimisation for optical receiver frontends in particular.

In this work, we propose the application of tuned-feedback approaches to both of these problems. It is well-known that feedback is effective for controlling both the dynamic response of a circuit and its linearity. Furthermore, typical frontend design favours identical amplifier stages for multi-stage frontends. Thus, in this work, we specifically explore the

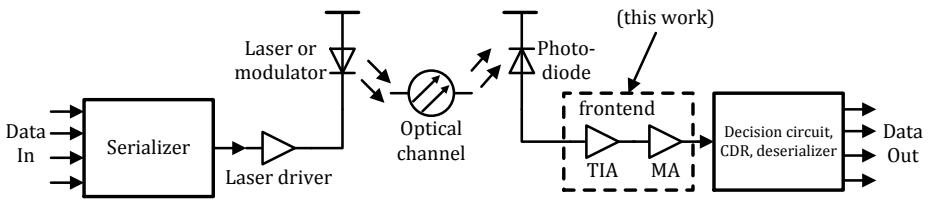


Figure 1.1: General architecture of an optical communication system. Adapted from [2:4].

possibility of using multiple feedback loops, where each feedback gain is tuned separately. We examine the behaviour of frontend circuits that are so tuned.

In the following chapter, we introduce core concepts of optical communication systems and the frontend circuit in general, qualitative terms. Subsequently, we define the scope and objectives of the study and summarise the research contributions of this work.

1.1 Optical communications systems

Optical communications are ideal for high-speed and long-distance links: compared to typical copper links, fibre optics exhibit very low loss over distance (0.15 dB/km to 0.2 dB/km) and high bandwidth (25 GHz to 50 GHz) [2:2]. Typically, the systems at each end of the link are electrical (computers, etc.), and so it is necessary to convert electrical signals to optical and back at each end.

A typical optical communication link block diagram is presented in Fig. 1.1. It consists of three major parts: first, the electrical/optical interface, which converts electrical data into an optical data stream. This is transmitted through an optical channel such as a fibre-optic cable, though other channels such as semiconductor waveguides exist. Finally, the optical/electrical interface converts the signal back into an electrical form usable by the system at the receiver side. The diagram assumes digital data represented as on-off-keyed (OOK) data streams.

The electrical/optical interface consists itself of a few components, shown as high-level blocks in the diagram. A serialiser converts a parallel input data stream into a single data stream. This signal is then handled by the laser driver, which modulates the current to the laser. In some systems, direct laser modulation may instead be replaced by a modulator driver into an optical modulator, which modulates the intensity of an always-on laser.

At the receive end of the optical channel, a photodiode converts light intensity into an electrical current. This small current must be converted to a voltage and amplified to a usable level, which is handled by the analog frontend: this component consists of a transimpedance amplifier (TIA), followed by one or more stages of post-amplifier (PA). The amplified signal

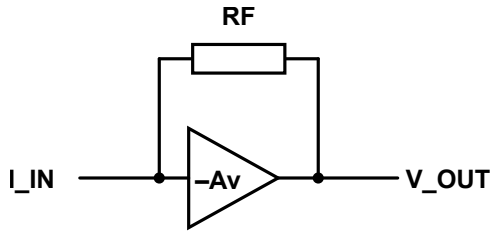


Figure 1.2: Shunt-feedback TIA topology.

can then be passed to a further block such as a decision circuit, clock-and-data-recovery circuit, deserialiser, etc. to recover the data and pass it onto the receiving system.

1.2 Optical receiver frontends

This thesis focuses entirely on the analogue frontend. One of the key design specifications of every optical receiver is its sensitivity, the minimum required input power to achieve a particular bit error rate (BER): good sensitivity requires low noise and high gain. Of course, the receiver's analogue bandwidth will critically impact the data rates it can support: it must be fast enough to amplify the high-frequency components of the signal. Optimising for low noise, high gain and high bandwidth, along with optical receiver-specific conditions and application-specific requirements, form the overall challenges of designing such a system.

1.2.1 Transimpedance amplifier

The transimpedance amplifier (TIA) takes as input the current from the photodiode and converts it to a voltage signal. The current is typically fairly small, requiring high gain—70 dBΩ or 80 dBΩ for the frontend overall is not unreasonable. The TIA's gain is expressed in ohms (Ω), a transimpedance gain, as it converts an input current to output voltage, and so the ratio of output to input is not dimensionless as in voltage amplifiers.

For the purpose of gain-staging to optimise noise, it is desirable for the TIA to have a high gain. However, sufficient bandwidth is important for high-speed systems, and the photodiode capacitance visible at the TIA's input often means the TIA has a dominant bandwidth-determining pole at its input; this may limit the gain that can be achieved while meeting bandwidth and data rate requirements. (With low-capacitance, high-speed photodiodes, however, this dominant input pole assumption may not be true.)

A typical shunt-feedback TIA topology is shown in Fig. 1.2, formed by any inverting voltage amplifier with a feedback resistor. The amplifier itself can make use of various topologies, yielding different performance characteristics. This category of TIA has the

advantage of a lower input and output resistance, yielding a faster circuit with higher output drive capability than open-loop TIAs [2:87].

1.2.2 Post-amplifier

The post-amplifier (PA) is a voltage-to-voltage amplifier that provide additional gain after the TIA, in order to amplify the received optical signal to a usable level. Given the TIA's dominant input pole, it may be challenging to obtain sufficient gain while meeting the bandwidth requirement on the TIA; thus, the post-amplifier can provide any gain the TIA is not capable of providing. The circuits used to implement the PA may be any suitable voltage-to-voltage amplifier.

1.3 Scope and objectives

In this work, we examined the application of new tuned-feedback design approaches for setting the gain of local feedback loops in multi-stage amplifiers in order to optimise a) dynamic response and b) linearity of optical receiver frontend circuits. These new approaches build upon topologies described previously in literature.

The two optimisation objectives above are examined separately. This work demonstrates that:

1. Dynamic response can be controlled and improved by the individual tuning of feedback gains, specifically in the context of a prior multi-stage post-amplifier design employing positive feedback, at the same bandwidth and test data-rate as the prior design.

2. The effect of such dynamic response control can be understood through root locus analysis. This analysis intends to move towards a systematic methodology and makes some design recommendations.

3. An interleaving-feedback topology described in literature can be repurposed for linearity optimisation by tuning the feedback gains. This topology is compared to non-feedback and non-interleaving-feedback designs to demonstrate linearity improvements.

We demonstrate the effectiveness of these approaches through the design of an optical receiver frontend circuit and comparison to a relevant reference design through simulation. Furthermore, for the linearity design, we designed and produced an integrated circuit with two variants to demonstrate the technique.

1.4 Contribution

This work develops and examines the idea of tuning multiple feedback loops in optical receiver frontend amplifier design, as applied to topologies and techniques where this design approach was not previously used. In particular:

1. The positive feedback technique was previously applied to a three-stage post-amplifier with one feedback loop per stage, and the bandwidth extension vs. dynamic response (overshoot/ringing) tradeoff was found to be a limiting factor. The proposed approach of independently tuning each feedback loop allows for improved performance for the same bandwidth extension and datarate that was previously found.

2. A root locus analysis is presented to provide insight into the dynamics of an amplifier circuit. The conclusions from this analysis may be useful to the designer in applying the above approach.

3. A design approach for linearity optimisation of an optical receiver frontend is proposed, making use of an interleaving feedback topology previously described for bandwidth extension. This topology's linearity is characterised and a design methodology focused on linearity optimisation is developed.

1.5 Thesis organisation

In Chapter 2, we review background related to the theory of bandwidth extension, dynamic response and linearity; technical background to the circuits involved; and existing approaches in literature.

Chapter 3 examines the dynamic response problem, starting from an existing design employing local positive feedback in a multi-stage post-amplifier. In this chapter, we demonstrate the concept with a design with improved dynamic response, discovered through simulation, and analyse the behaviour of the circuit when the feedback is tuned independently.

Chapter 4 then examines how a multiple-feedback topology, originally proposed in the literature for bandwidth extension, can be applied to the linearity problem and discusses the design of a receiver chip applying these concepts. Chapter 5 then presents and discusses overall chip simulation and measurement results.

Finally, Chapter 6 presents the overall conclusions to this investigation of feedback techniques.

Chapter 2

Background & literature review

This chapter provides an overview of the necessary background for the studies conducted in the subsequent chapters, and provides a brief overview of relevant recent literature in the same and related areas. In particular, we will overview background and literature for bandwidth extension of the PA; then we will provide general background and definitions on dynamic response metrics (pulse response, eye diagrams, etc.), followed by a section on linearity. Next, we will look at feedback theory in the two contexts in which feedback is used in the proposed designs. The subsequent sections introduce TIA and PA topologies used in this work. Finally, in the last three sections, we overview the positive feedback technique that is the basis of the first proposed design, and review literature on linearity in RF amplifiers, and review the linearity of optical receiver frontends in literature.

2.1 Bandwidth extension

In order to handle increasing data rates, an optical receiver's frontend circuits must have sufficient bandwidth to amplify the incident signals.

However, it is important to consider the contribution of additional high-frequency noise as well. There is therefore a tradeoff between intersymbol interference (ISI) at low bandwidth and noise at high bandwidth. A common rule of thumb suggests that bandwidth (in Hz) should be set to 70% of the data rate (in bits/s) [2:67].

A number of methods are well established in the literature. This section introduces a methods applied to post-amplifier (PA) design: we will start with general multi-stage amplifier theory, and then move on to the well-known inductive peaking method. From there, we will introduce various methods, both inductor-based and inductorless, in the more recent literature.

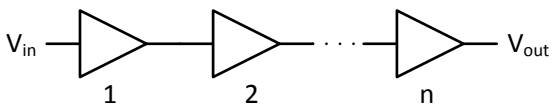


Figure 2.1: Multi-stage amplifier of n cascaded amplifier stages.

2.1.1 Multi-stage amplifiers and gain-bandwidth product optimisation

Multi-stage amplifiers are ubiquitous in transistor amplifier applications to achieve higher gain-bandwidth product (GBW). This is discussed, for example, by Säckinger in [3:176–178], in which analytical formulae for 1st-order and 2nd-order Butterworth amplifier stages are derived.

Given a design for a single amplifier stage, a cascade of identical amplifier stages increases the overall GBW (as shown in Figure 2.1). Säckinger gives a few sample equations relating the overall gain and bandwidth, the number of stages n and the per-stage gain and bandwidth. For a 1st-order stage,

$$A_{tot} = A_s^n \tag{2.1}$$

$$\mathrm{BW}_{tot} = \mathrm{BW}_s \sqrt{\sqrt[n]{2} - 1} \quad , \tag{2.2}$$

$$\tag{2.3}$$

whereas, for a 2nd-order Butterworth stage,

$$A_{tot} = A_s^n \tag{2.4}$$

$$\mathrm{BW}_{tot} = \mathrm{BW}_s \sqrt[4]{\sqrt[n]{2} - 1} \quad . \tag{2.5}$$

$$\tag{2.6}$$

We note the very high bandwidth dropoff for first-order systems (2, 3 and 4 stages yield 64%, 51% and 43% of the single-stage bandwidth, respectively) compared to second-order Butterworth systems (80%, 71% and 66% respectively). A cascade of second-order systems has a clear benefit over first-order for GBW extension.

In practical design terms, for a given target GBW, adding stages reduces the minimum GBW required of each individual stage at the cost of power and area. For example, to meet 100 V/V (40 dB) at 10 GHz bandwidth, two first-order stages would need 155 GHz GBW each, while four first-order stages would need only 73 GHz GBW each. Nonetheless, this effect is subject to diminishing returns; in fact, for realistic responses (e.g. Butterworth, as

opposed to brick-wall response), adding too many stages will even cause the overall GBW to decrease.

2.1.2 Bandwidth extension using inductive peaking

A number of methods in the literature use inductive peaking techniques in order to extend the bandwidth of the TIA and PA. As their name indicates, these methods use inductance—more accurately, the resonance between an inductive element and parasitic capacitances—in order to create a tuned peak in the frequency response that pushes the $-3\,\mathrm{dB}$ bandwidth higher.

Shunt peaking

The first method, shunt peaking, is a well-known method described by Razavi in [2:110–114], as well as in [4]. It makes use of an inductor placed in series with the load resistor of resistively loaded common source amplifiers and differential amplifiers; a common-source topology utilising the method is shown in Figure 2.2a. The following description is primarily based on Razavi's analysis.

Careful tuning is required to control overshoot in the pulse response of the circuit. Razavi gives the damping factor,

$$\zeta = \frac{R}{2}\sqrt{\frac{C_L}{L}} \quad , \tag{2.7}$$

which can be used to balance bandwidth extension and overshoot in design. Table 2.1 shows the tradeoff between these two quantities, assuming an ideal inductor. Razavi suggests that a 7.5% overshoot typically provides a reasonable compromise. Mohan et al. also demonstrate an analytical approach to designing for the desired flatness in the frequency response [4].

This method's primary drawback, and the drawback of inductive bandwidth extension methods in general, is the large area required for monolithic on-chip inductors. Additionally, the Q factor of such inductors is limited by parasitics, typically reducing the effective bandwidth extension down to 50% according to Razavi. It is possible to reduce the needed area by using active inductors, described in [2:138-139]. As an example, the circuit in Figure 2.2b has an equivalent inductance of

$$L = \frac{C_{GS}}{g_m}\left(R_S - \frac{1}{g_m}\right) \quad , \tag{2.8}$$

for $R_S \gg 1/g_m$ and g_m being the small-signal transconductance of M1. However, active inductors have drawbacks in terms of a large voltage headroom needed, as well as higher

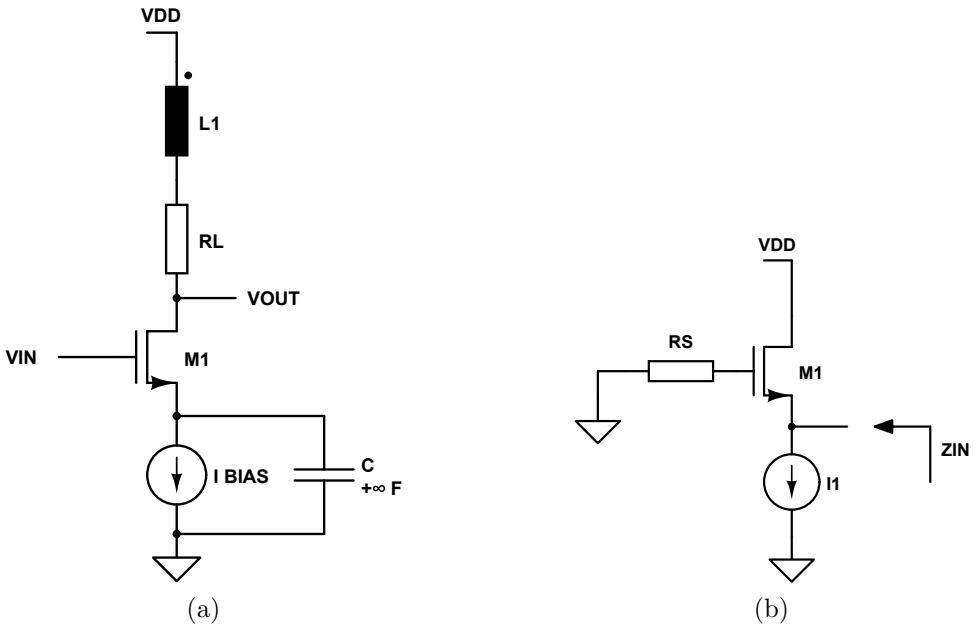


Figure 2.2: Inductive shunt peaking. (a) shunt peaking on a common-source amplifier using a monolithic inductor; (b) source follower-based active inductor.

Table 2.1: Shunt peaking overshoot vs. damping factor

Overshoot	ζ	BW ext.
5%	0.73	78%
7.5%	0.69	82%
10%	0.65	84%

Adapted from [2:112].

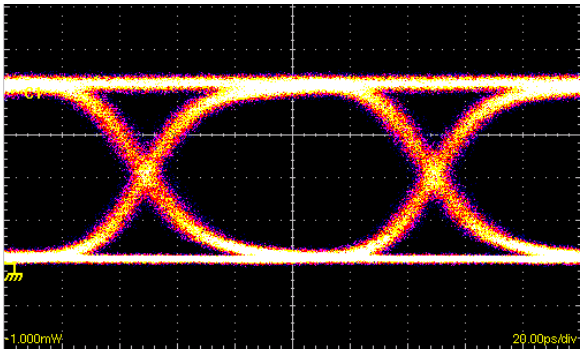


Figure 2.3: Typical eye diagram of OOK non-return-to-zero data, captured on oscilloscope. Constant-1, constant-0, 1-to-0 transitions and 0-to-1 transitions are all visible. From Wikimedia Commons [11], used under the CC-BY-SA 3.0 licence.

power consumption and noise contribution.

A number of methods are proposed in more recent literature[5–7], but all suffer similar concerns with the use of inductors. In order to improve area efficiency, it is desirable to achieve bandwidth extension without the use of inductors.

2.1.3 Inductorless bandwidth extension methods

The previous section discussed the foundations of inductive peaking-based bandwidth extension. However, as discussed, both monolithic and active inductors have significant drawbacks, whether that is large area or noise and power. Methods that achieve bandwidth extension without the use of explicit inductances are therefore highly desirable.

Feedback is frequently used in order to create similar peaking effects as inductive methods. A number of methods, such as [1, 8–10], are proposed in the literature. The feedback concepts and two of these methods are explored in detail in the following sections.

2.2 Pulse response, eye diagram and eye opening

For optical receivers intended for on-off-keyed (OOK) signal applications, the best performance metrics will evaluate the ability of the receiver to recover the original bit stream, i.e., distinguish bit values without errors. Fundamentally, we can represent binary data as a time-shifted sequence of square pulses in superposition, with a pulse duration related to the data rate. An amplifier's pulse response, in particular rise/fall time, settling time and undershoot/ringing, can all affect signal integrity of a datastream.

The eye diagram is the most direct measurement of performance in these applications, as it directly measures the usability of the output signal. This diagram is produced by inputting

a signal consisting of a long string of pseudo-random bits, and measuring the output signal; each output bit is then overlapped over each other in a single signal-vs.-time plot, as shown in Fig. 2.3. This representation shows a wide variety of possible bit transition sequences, providing a view of ISI, noise and dynamic response. The height and width of the 'eye' opening are related to recoverability of the bit stream.

2.3 Linearity

2.3.1 Definitions and measures

All active devices, and by extension all amplifiers, exhibit nonlinearity as input signal levels increase. In particular, for the purpose of this work, we are concerned with weak nonlinearities, which manifest when the output signal is not saturating (i.e. not near its maximum signal swing). We thus primarily consider harmonic distortion, represented by total harmonic distortion (THD), and intermodulation distortion, represented by the third-order intercept point (IP3).

In the most general terms, we can model an amplifier's low-frequency input/output transfer as a Taylor series [12]:

$$v_o = a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + \ldots , \tag{2.9}$$

where v_o and v_i are the output and input signals, respectively, and the coefficients a_n are

$$a_0 = v_o(0) \qquad \text{(Output DC bias); and} \tag{2.10}$$

$$a_n = \left.\frac{d^n v_o}{dv_i^n}\right|_{v_i=0} \qquad \text{for } n = 1, 2, \ldots \tag{2.11}$$

$$\tag{2.12}$$

a_1 represents the gain of the linear part of the output, with higher-order terms representing nonlinearities. If the input is a single tone, $v_i = A\cos(\omega t + \phi)$, then these higher-order terms will produce harmonics at multiples of the input frequency (2ω, 3ω, ...); if the input is the sum of two sinusoids $v_i = A\cos(\omega_1 t + \phi_1) + B\cos(\omega_2 t + \phi_2)$ (a two-tone test), then intermodulation products will result (e.g. the third-order term will produce signals at $2\omega_2 \pm \omega_1$, $2\omega_1 \pm \omega_2$, $3\omega_1$, and $3\omega_2$) [12]. These newly generated frequency components constitute nonlinear distortion.

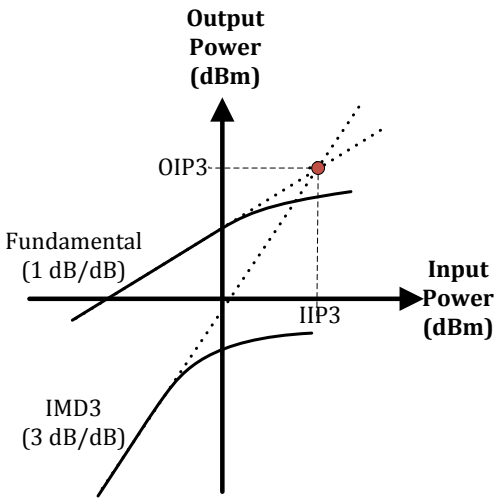


Figure 2.4: Power curves for determining IP3.

The primary metric of nonlinearity, for the purpose of this work, is the third-order intercept point (IP3) at frequency $2\omega_1 - \omega_2$ for some close input frequencies $\omega_{1,2}$. As discussed in [12], IP3 is a metric of intermodulation distortion which is independent of input power. As shown in Fig. 2.4, if we plot output vs. input power in logarithmic units, the linear response (proportional to v_i^2) has a slope of 1 dB/dB, i.e., the output is proportional to the input, up until the output saturates (top solid line). The third-order intermodulation product, however, is proportional to $(v_i^3)^2$ and has a logarithmic slope of 3 dB/dB (bottom solid line). If we extrapolate both these lines to their intersection point (as shown by the dotted lines), then we obtain two IP3 values, the IIP3 (input-referred IP3) and OIP3 (output-referred IP3), either of which represent the third-order nonlinearities of the system (higher is better).

Total harmonic distortion (THD) is also used to characterise linearity. For a given input tone, the THD of an amplifier is defined as the ratio of the total amplitude of harmonics to the fundamental signal amplitude:

$$\mathrm{THD} = \frac{\sqrt{V_{o2}^2 + V_{o3}^2 + \cdots}}{V_{o1}} \,, \tag{2.13}$$

where V_{on} indicates the amplitude of the nth harmonic at the amplifier output. Unlike the IP3, the THD varies with signal power, and will tend to increase as the output signal increases. Furthermore, since harmonics occur at multiples of the fundamental, at higher frequencies these harmonics may find themselves beyond the amplifier's bandwidth and be attenuated. While this may lead to a lower THD at higher frequencies, it does not fully characterise the amplifier's nonlinearities e.g. as may manifest as intermodulation distortion

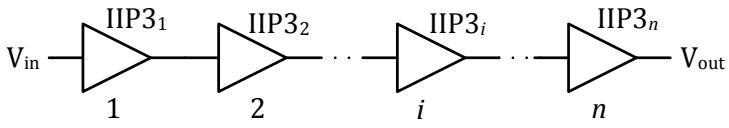


Figure 2.5: Multi-stage amplifier of n cascaded amplifier stages with weak nonlinearities.

in a two-tone test.

2.3.2 In short-channel MOSFETs

The proposed method primarily focuses on topology-level optimisation of linearity, independent of the linearity of the amplifier stages and the devices that constitute it. Nonetheless, this discussion of linearity would not be complete without considering the linearity of MOSFET amplifiers. A 1997 article by Soorapanth and Lee [13] discusses the RF linearity of the short-channel MOSFET, viewing its V-I characteristic as a two-port transconductance, and finds an expression for IIP3,

$$P_{\text{IIP3}} = \frac{8}{3}\frac{v_{\text{sat}}L}{\mu_1 R_S}V_{\text{ov}}\left(1+\frac{\mu_1 V_{\text{ov}}}{4v_{\text{sat}}L}\right)\left(1+\frac{\mu_1 V_{\text{ov}}}{2v_{\text{sat}}L}\right)^2 \tag{2.14}$$

where

$$\mu_1 \triangleq \mu_0 + 2\theta v_{\text{sat}}L\ . \tag{2.15}$$

Here, P_{IIP3} is the IIP3 in watts (not dBm), v_{sat} is the saturation velocity, L is the FET channel length, $V_{\text{ov}} = V_{\text{gs}} - V_{\text{th}}$ is the gate overdrive voltage, R_S is the input port impedance, μ_0 is carrier mobility (m^2/sV) and θ is mobility reduction (V^{-1}). This analysis assumed quasi-static nonlinearity, and so does not capture memory nonlinearities as the operating frequency approaches a MOSFET's transition frequency f_T.

The article identifies that IIP3 increases as the gate overdrive voltage increases. However, this increase in linearity comes with a tradeoff of increased power consumption and challenges with regard to voltage overhead with small supply voltages (such as the 1.5 V supply used by the GF 130 nm technology in this thesis). The article also observes that g_m is independent of IIP3 via the device width W, which does not appear in (2.14).

2.3.3 In multi-stage amplifiers

In a cascade of multiple amplifier stages shown in Fig. 2.5, all exhibiting weak nonlinearities, it is possible to calculate the overall IP3 and the IP3 contribution of each amplifier. If we want to refer the ith amplifier's IIP3 to the input, we can divide by the gain of all preceding

stages, in the same way as we refer noise across gain stages:

$$\mathrm{IIP3}_{i,\mathrm{in}} = \frac{\mathrm{IIP3}_i}{\prod_{j=1}^{i-1} G_j} \,. \tag{2.16}$$

Note that the IIP3 terms in this equation are all in watts (not dBm). The overall IIP3, as contributed by all stages, depends on the correlation between intermodulation distortion products (IM3). Since distortion products are deterministic and can be phase related, we can obtain two values: a worst-case lower bound for fully correlated distortion and an RMS value for uncorrelated distortion [12, 13]:

$$\frac{1}{\mathrm{IIP3}_{min}} = \frac{1}{\mathrm{IIP3}_1} + \sum_{i=2}^{N} \left(\prod_{j=1}^{i-1} G_j \cdot \frac{1}{\mathrm{IIP3}_i} \right) \tag{2.17}$$

$$\frac{1}{\mathrm{IIP3}_{rms}^2} = \frac{1}{\mathrm{IIP3}_1^2} + \sum_{i=2}^{N} \left(\prod_{j=1}^{i-1} G_j^2 \cdot \frac{1}{\mathrm{IIP3}_i^2} \right) \,. \tag{2.18}$$

As noted in [13], the IIP3 of later stages have a proportionally larger contribution to the overall IIP3, as the terms associated to each stage is multiplied by the total gain preceding that stage (this assumes $G_j > 1$ for all j). Additionally, a high gain in early stages also degrades IIP3, as that gain factor appears in all subsequent terms; this creates a tradeoff between noise optimisation (high early stage gain) and linearity optimisation. (However, high gain improves OIP3, given that the IP3 values are being referred in the other direction.)

2.4 Feedback

2.4.1 Closed-loop feedback in the Laplace domain

In order to study the dynamic response of an amplifier with feedback in this work, we will be considering the root locus in the Laplace domain as feedback gain is varied. It is therefore important to understand how the roots, in particular the poles, are affected by feedback.

For illustration, and for the case most relevant to this work, suppose we have an amplifier with an underdamped second-order response. The standard Laplace domain second-order transfer function is of the form

$$H(s) = \frac{a_0}{s^2 + \frac{\omega_n}{Q} s + \omega_n^2} \,, \tag{2.19}$$

where $H(0) = a_0/\omega_n^2$ is the DC gain ($H(0) > 0$ for an amplifier), ω_n is the natural frequency

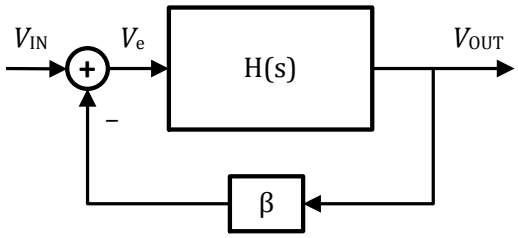


Figure 2.6: Negative feedback of an amplifier with a Laplace-domain transfer function $H(s)$.

of the system, and Q is the quality factor. In this case, two complex conjugate poles exist at

$$s = -\frac{\omega_n}{2Q} + \omega_n\sqrt{1 - \frac{1}{2Q}}\ . \tag{2.20}$$

Suppose now that this amplifier is placed in a negative feedback loop with a linear feedback gain $\beta > 0$, as shown in 2.6. Given the feedback equation,

$$H_{cl}(s) = \frac{H_{ol}(s)}{1 + \beta H_{ol}(s)}\ , \tag{2.21}$$

where $H_{cl}(s)$ is the closed-loop transfer function and $H_{ol}(s)$ is the open-loop transfer function, and substituting (2.19) for $H_{ol}(s)$, we find the transfer function

$$H\left(s\right) = \frac{a_0}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2 + \beta a_0}\ . \tag{2.22}$$

Thus, fitting (2.22) to the parameters of the standard second-order equation (2.19), we find the new parameters:

$$H_{cl}(0) = \frac{a_0}{\omega_n^2 + \beta a_0} \tag{2.23}$$

$$\omega_n' = \sqrt{\omega_n^2 + \beta a_0}\ ; \text{ and} \tag{2.24}$$

$$Q' = Q\frac{\omega_n'}{\omega_n}\ . \tag{2.25}$$

Furthermore, we can use these new parameters in (2.20) to find the new pole locations.

From these results, we see that, in negative feedback ($\beta > 0$), the gain decreases, the pole's natural frequency increases, and the quality factor increases. In positive feedback ($\beta < 0$), gain decreases, pole natural frequency decreases, and the quality factor decreases. In both cases, this is dependent on the β value. This demonstrates a level of control over

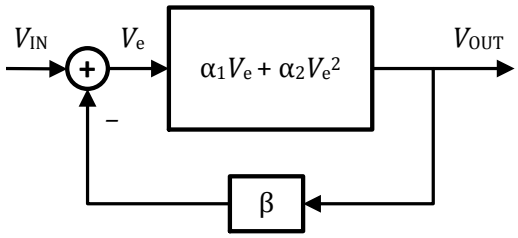


Figure 2.7: Negative feedback for a second-order weakly nonlinear system. Adapted from [14].

pole locations, and thus dynamic response, as a function of the feedback gain β; while these interactions may become more complex in a higher-order system, a root locus analysis of such systems, analytically as shown here or in simulation, allows similar insight into pole movement.

2.4.2 Linearity in closed-loop negative feedback

Negative feedback can be used, locally or globally, in order to linearise the response of an amplifier. This linearisation action may be considered similarly to the error-correction action of a closed loop control system: the error signal accounts for the distorted output signal and is thus corrected for. Razavi (2002) provides an example for second-order nonlinearities. Suppose we have an amplifier with weak second-order nonlinearity, having an open-loop transfer $V_{\text{out}} = \alpha_1 V_{\text{in}} + \alpha_2 V_{\text{in}}^2$, and a linear feedback gain $\beta > 0$, as shown in Fig. 2.7. If a sinusoidal input $V_{\text{in}} = A\cos(\omega t)$ is applied, we expect the output to be of the form

$$V_{\text{out}} = a\cos(\omega t) + b\cos(2\omega t)\ , \tag{2.26}$$

neglecting higher-order harmonics and phase shift. As derived in [14], the ratio of second-order distortion to the linear output b/a is found to be approximately,

$$\frac{b}{a} \approx \frac{\alpha_2 A}{2\alpha_1} \frac{1}{(1+\beta\alpha_1)^2}\ , \tag{2.27}$$

whereas without feedback, this ratio would be

$$\frac{b}{a} \approx \frac{\alpha_2 A}{2\alpha_1}\ . \tag{2.28}$$

Comparing (2.27) and (2.28), we see that second-order harmonic distortion ratio is reduced by a factor of $(1+\beta\alpha_1)^2$ relative to the fundamental. A similar approach could be used to

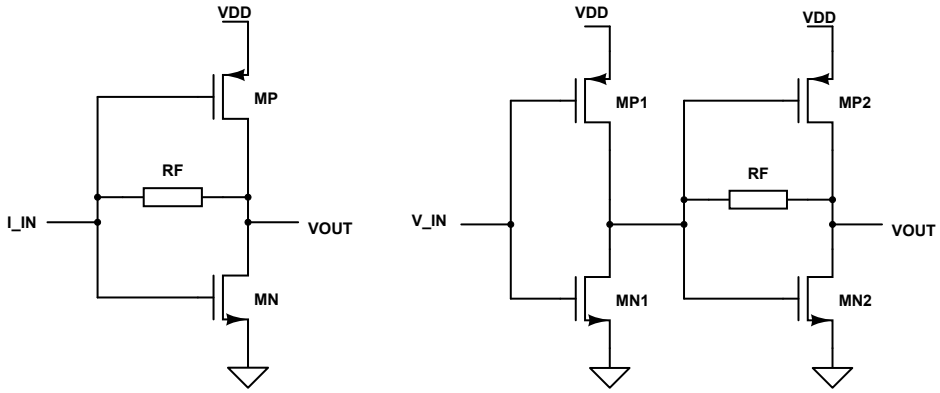


Figure 2.8: Inverter-based optical frontend circuits: (a) TIA; (b) Cherry-Hooper amplifier, used as PA stage.

derive the effect of negative feedback on higher-order harmonic distortion or intermodulation distortion. This linearisation effect will be the basis of the linearity optimisation described in this work.

2.5 Inverter-based transimpedance amplifier

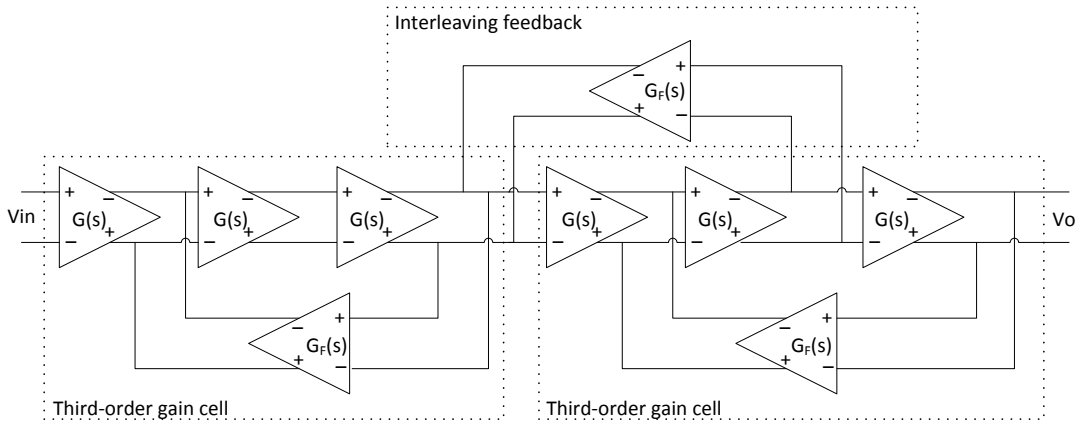
An inverter-based TIA is formed by a CMOS digital inverter with a feedback resistor, which biases it to operate as an amplifier, as shown in Fig. 2.8a. It is a shunt feedback-type TIA, similar to the common-source shunt feedback TIA (see [2:106-110]). The use of both NMOS and PMOS in these inverter amplifiers provides greater overall transconductance g_m for the same amount of bias current, and thus higher gain, as the two transistors both contribute additively to g_m [15]. These amplifiers also feature lower input-referred noise [16]. The TIA allows simple control over gain, $R_T \approx -R_F$ (by setting R_F), and bandwidth, $f_{-3\,\mathrm{dB}} \approx \frac{1}{2\pi g_m^{-}1 C_{in}}$ (by setting g_m).

This TIA's higher g_m and power efficiency, generally good bandwidth, and as its design simplicity make it suitable for state-of-the-art broadband communication applications.

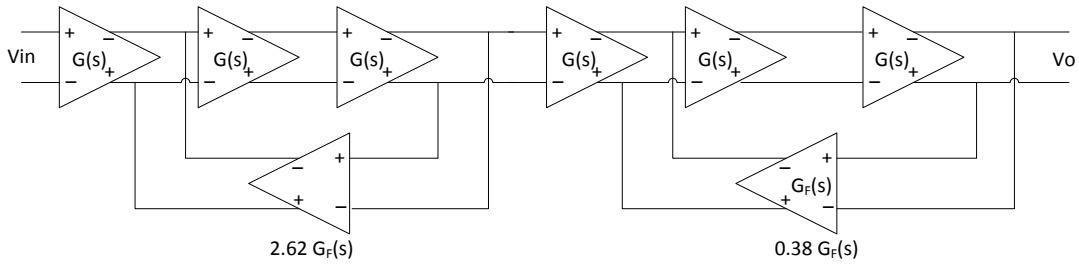
2.6 Post-amplifiers

2.6.1 Cherry-Hooper topology

The Cherry-Hooper amplifier (CHA), shown in Fig. 2.8b, is a two-stage amplifier, consisting of a transconductance stage (voltage-to-current) followed by a transimpedance stage



(a)



(b)

Figure 2.9: Block diagram of the third-order interleaving-feedback post-amplifier topology [8]: a) interleaving topology; b) theoretical equivalent without interleaving feedback.

(current-to-voltage). The local feedback in the second stage reduces the impedance seen at the intermediate node and output node, allowing the pole frequencies to become much higher than a common-source amplifier with load resistance equal to R_F [2:143-145].

In using inverter-based amplifiers for these amplifiers, we also obtain the properties discussed in Section 2.5. The Cherry-Hooper concept's properties combined with the inverter-based amplifier implementation makes the CHA a suitable PA for broadband applications.

2.6.2 Interleaving feedback topology

Huang, Chien and Lu (2007) proposed a fully differential PA topology which employs third-order gain stages with active local feedback, and interleaving feedback across different stages, as shown in Fig. 2.9a [8]. Each amplifier shown is itself a simple first-order differential pair

with inverting gain ($G(0) < 0$). With all feedback gains equal (shown as $G_F(s)$), they find that this topology provides for significant bandwidth extension while featuring excellent gain flatness in the frequency domain, significantly mitigating the peaking problems usually involved with bandwith extension techniques. This technique also trades off a modest amount of gain for bandwidth extension.

The article suggests that the interleaving feedback has "pole-splitting" behaviour. Taking the example of a two-stage amplifier, it is shown that the transfer function can be decomposed into two third-order stages with different feedback gains and without the interleaving feedback, as shown in Fig. 2.9b. In theory, this topology is equivalent to the interleaving feedback design, but presents greater complexity due to the differing feedback gains, as well as greater sensitivity to mismatch and process variation for the smaller feedback amplifier. In the context of the present thesis, the interleaving feedback may also present linearity advantages, as discussed in the next chapter.

A comparison of the interleaving architecture to a conventional architecture (third-order stages with local-only feedback) shows an 18% bandwidth extension, at a 2 dB reduction of voltage gain, a significant flattening of the gain near the cut-off frequency and improvement in simulated eye opening (reduced overshoot and ringing). Their implemented design in 0.18 µm using this technique achieves a gain of 42 dB at 9 GHz bandwidth, at 189 mW and 0.192 mm^2.

In this work, this topology is of interest not for bandwidth extension, but for its linearity properties. While these are not originally explored, we hypothesised that this topology would provide good linearity, depending on the feedback gain of each loop. Furthermore, an unbroken feedback path exists from the output to the input thanks to the interleaving feedback, which is expected to improve linearity even further compared to local per-stage feedback loops (such as the theoretical equivalent of Fig. 2.9b).

2.7 Positive feedback technique for bandwidth extension

A conference paper by Morita et al., very briefly mentions the use of positive feedback on the post-amplifier to extend receiver bandwidth [10], in the context of an optical I/O array chip design. The paper does not discuss the details of this technique or of the pre- and post-amplifier circuit design, and to the best of our knowledge, this technique is not discussed elsewhere in the literature.

Weihao Ni, a member of the same research group as the author, subsequently characterised positive feedback for the purpose of bandwidth extension [1] (co-published alongside parts of this work). He applied positive feedback to an inverter-based TIA and Cherry-Hooper PA stages, both discussed above. This reference design is similar to previous work within our research group [15, 17, 18], and represents a good state-of-the-art design for high-speed applications for the purpose of analysing and evaluating the technique's bandwidth extension.

We first discuss the reference design in Section 2.5. Then, we summarise the prior work, with further information available in [1]. In this summary, we discuss the key conclusions from theoretical analysis of a TIA and single Cherry-Hooper PA stage with positive feedback in Section 2.7.1, then describe the three-stage reference circuit and the three-stage PA with equal positive feedback in Section 2.7, both used as comparison points for the following chapters.

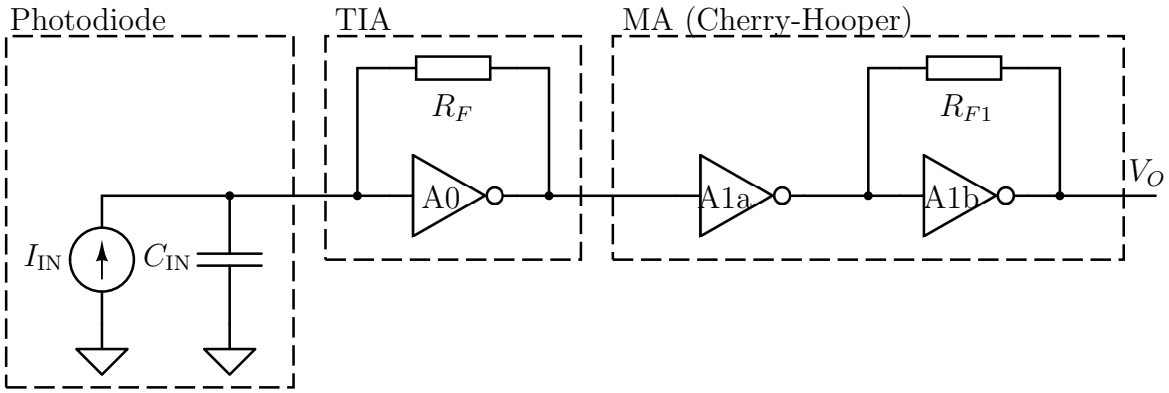
2.7.1 Single-stage PA

The reference design is formed of inverter-based TIA and inverter-based CHA PA stages. Fig. 2.10a shows this TIA, a single CHA1 stage. All inverters shown are CMOS inverters, with the forward inverters (A0, A1a and A1b) identical.

Positive feedback is then applied across the first half of the CHA1 stage, as shown in Fig. 2.10b. Note that, while CMOS digital inverters are used, the first inverter of CHA1 is biased into a linear region by the TIA output, and FB1 is biased into a linear region by the DC output bias of the first CHA1 stage. The bias currents are on the order of 4 mA, much larger than signal currents, and a linear amplified signal is expected at the output, not rail-to-rail digital signals.

FB1's gain is much smaller than the CHA1 forward amplifiers. In this situation, analysis shows that, qualitatively, FB1 acts equivalently to a negative resistance to ground at the CHA1 input node, as shown in Fig. 2.10c. This negative resistance acts on the TIA's transfer function: it presents in parallel to the TIA's output impedance, and thus the TIA's equivalent output impedance is increased, providing bandwidth extension compared to a circuit without FB1. Given a small FB1 gain, however, this negative resistance should not cause the TIA equivalent output impedance to become negative.

For the purpose of design and stability analysis, the feedback coefficient x is defined as the transconductance ratio of FB1 to the CHA first forward inverter, or equivalently the ratio of aspect ratios for the transistors in those inverters (assuming this quantity is the



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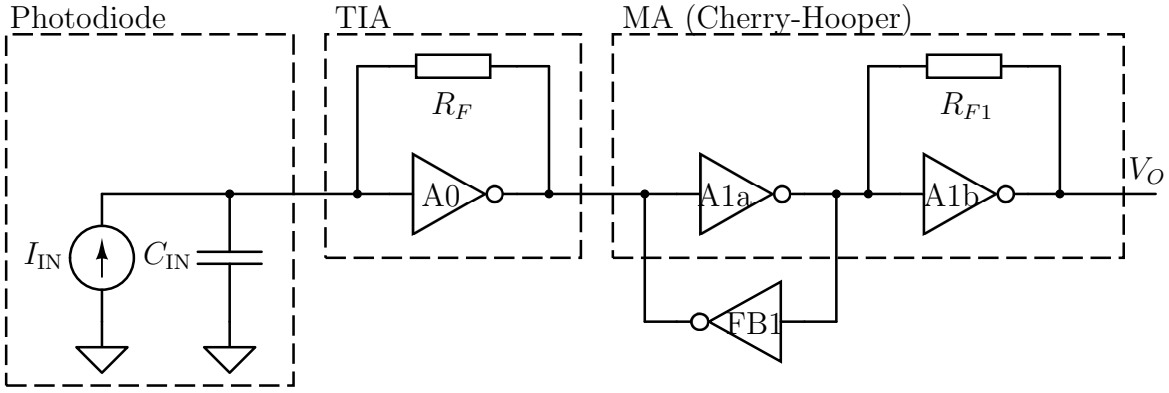

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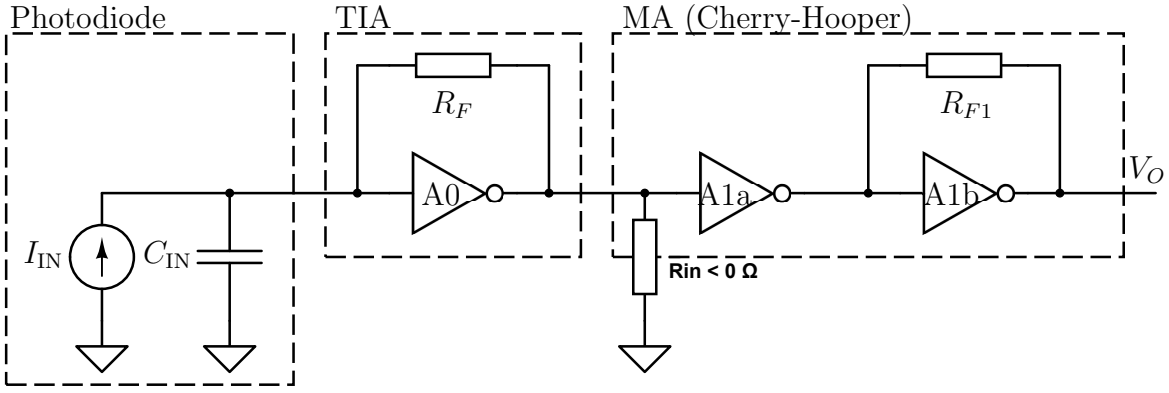


(c)

Figure 2.10: Circuits for positive feedback technique. (a) Reference circuit. (b) With positive feedback applied. (c) Equivalent negative-resistance model of positive feedback.

same for P- and NMOS). It is expressed by

$$x = \frac{g_{mfb}}{g_{m1a}} = \frac{(W/L)_{\mathrm{FB},N,P}}{(W/L)_{1N,P}} \quad . \tag{2.29}$$

Adding more feedback gain amounts to increasing the feedback coefficient x.

For the negative-resistance model to be valid, we find a stability criterion of $x < 1$; if this condition is not met, the CHA1-FB1 structure will act not as an amplifier with negative input resistance, but as a digital latch with exponential regeneration. Furthermore, a tradeoff exists between bandwidth extension and overshoot, similar to inductive methods; reducing overshoot requires $x << 1$.

The derivation of the above results is outlined below.

Outline of derivations

The input impedance of the CHA1 with FB1 can be modelled simply as a negative resistance, as obtained from small-signal analysis of the CHA1:

$$G_{in} = \frac{1}{R_{in}} = \left(\frac{1}{A} - \frac{A}{1+A}\right) g_{mfb} \tag{2.30}$$

where $A = g_m R_o$ is the gain of the forward inverters, and g_{mfb} is the total transconductance of the feedback inverter. When $A > 1$, $G_{in} < 0$, forming a negative resistance.

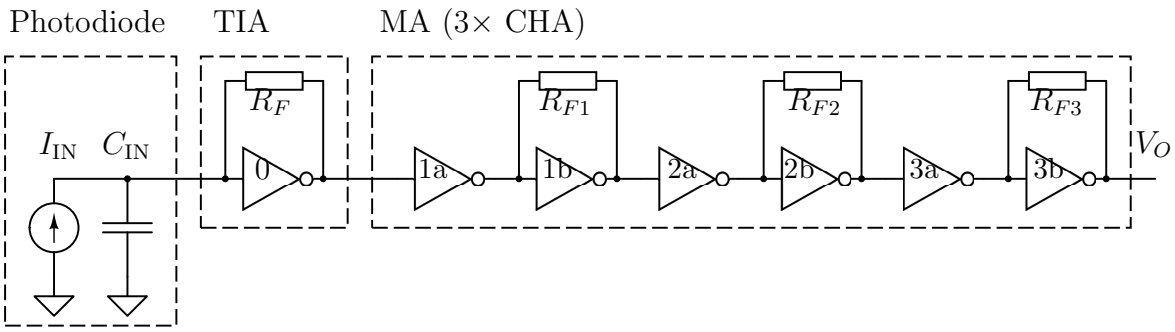
If we consider the small-signal equivalent circuit of the photodiode and TIA, loaded at the output by R_{in}, we can derive the transfer function at the TIA output. Its denominator is

$$\begin{aligned} D_{TIA}(s) = {} & s^2 \frac{R_F R_{o,tot}}{1 + g_m R_{o,tot}} \left(C_{IN}C_{OUT} + C_{IN}C_F + C_F C_{OUT}\right) \\ & + s \frac{1}{1 + g_m R_{o,tot}} \left(R_{o,tot}C_{OUT} + \left(R_{o,tot} + RF\right) C_{IN} + R_F \left(1 + g_m R_{o,tot}\right) C_F\right) + 1 \quad . \end{aligned} \tag{2.31}$$

where g_m is the total transconductance of the inverter A0, C_{IN} is the capacitance present at the TIA input, C_{OUT} is the capacitance at the TIA's output, and C_F is the TIA drain-gate capacitance. $R_{o,tot}$ is the overall output resistance of the TIA, encompassing A0's r_o parameter along with the CHA1/FB1 input impedance R_{in} from (2.30), given by the expression

$$G_{o,tot} = \frac{1}{R_{o,tot}} = g_o + G_{in} = \left(\frac{1+x}{A} - x\frac{A}{1+A}\right) g_{m1a} \quad , \tag{2.32}$$

where x is the feedback coefficient defined in (2.29).



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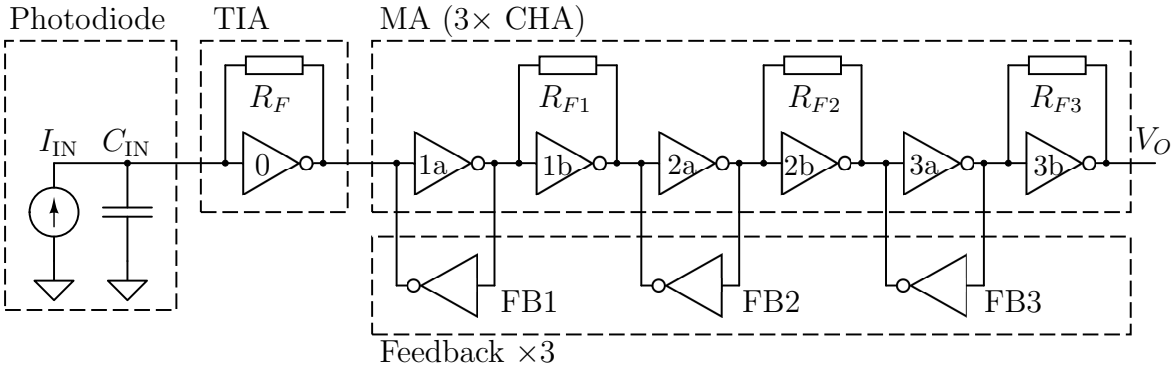


(b)

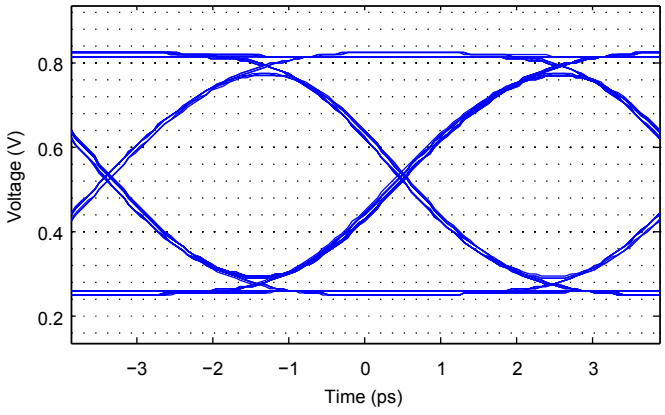
Figure 2.11: Inverter-based receiver topology with 3-stage PA. (a) Reference circuit. (b) With positive feedback applied, providing bandwidth extension.

If the TIA has a dominant input pole due to the typically large photodiode capacitance at C_{IN}, then from second-order dynamics, we know that the inverse of the bandwidth, $1/\omega_{-3\,\mathrm{dB}}$, is approximately equal to the coefficient of s in (2.31). Increasing x increases $R_{o,tot}$, which in turn will reduce this coefficient's value and increase the bandwidth. The transimpedance is also marginally increased, hence this method does create a gain/bandwidth tradeoff.

A tradeoff exists, however, with system stability. In (2.31), to maintain stability, all poles must be in the left half-plane, meaning the coefficients of s^2 and s must both be positive. Given (2.32), this requires $x < 1$; to ensure relative stability (low ringing), $x \ll 1$ is required.

2.7.2 Three-stage reference and positive feedback circuits

The positive feedback technique was applied to a reference design consisting of a TIA and 3 Cherry-Hooper PA stages, as shown in Fig. 2.11a. The forward amplifier transistors (NMOS and PMOS both) all have a width of 30 µm, width of 60 nm, in TSMC 65 nm CMOS. The TIA's gain, set via R_F, is set higher than the PA stages for a more noise-optimal design.



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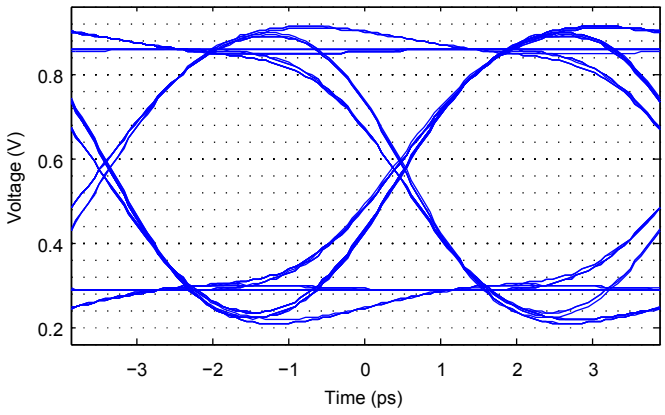


(b)

Figure 2.12: Eye diagrams for time-domain simulation of PRBS input at 26.1 Gbps. a) Reference circuit; b) Positive feedback circuit. Reproduced from [1], © 2015 IEEE.

The local positive feedback was applied to this design as shown in Fig. 2.11b, using inverters with transistor sizes 2.6 µm wide, 60 nm long. All three feedback inverters were identical, and so the feedback gain was identical for each of the three PA stages. To ensure the gain is equal to the reference design, the forward PA stage gain was reduced slightly (via the $R_{F1,2,3}$).

Between the reference and proposed positive-feedback circuits, the bandwidth is increased from 12.4 GHz to 18.3 GHz (48%), at constant transimpedance gain, with negligible frequency-domain peaking. Per the 70%-of-data rate rule of thumb, these designs were simulated at 26.1 Gbit/s for time-domain simulations.

This method is highly area-efficient, being inductorless, and increases power dissipation only marginally (+3.3%), as it only adds low-gain low-bias-current inverter amplifiers in the feedback paths. The variation in group delay significantly increases, which predicts a worse time-domain pulse response; this is corroborated by the 26.1 GHz eye diagrams (Fig. 2.12), where an improvement of 8% in vertical eye opening is observed, but a visibly less clean eye due to the over-/undershoot caused by ringing can be seen.

The stability and dynamic response issues observed with this technique motivated the investigations carried out in Chapter 2. The approach used there is applied to the same reference circuit.

2.8 Linearisation of RF amplifiers

In this section, we review literature surrounding the RF and microwave low-noise amplifier (LNA), as these circuits frequently must be optimised for both noise and linearity. The general approach found for multi-stage LNAs has been to optimise for gain and noise figure in the first stage, and optimise for linearity in the last stage, as follows from Section 2.3.3.

Park, Kim and Yu looked at a 2-stage LNA (topology not specified) in 0.35 µm CMOS with n-channel amplifying transistors [19]. They proposed a method of selecting device sizes and bias conditions to optimise for noise, linearity and power. They found that noise and linearity could be optimised independently via the first and second stage design, respectively. Higher W/L in the first stage led to lower noise, whereas a local minimum exists with respect to V_{gs} (around 1 V for their design). High overdrive voltage is preferred for linearity in strong inversion, as concluded previously in this chapter; they also observe that third-order intermodulation distortion is minimised at points where

$$\frac{d^2 g_m}{dV_{gs}^2} = 0 \tag{2.33}$$

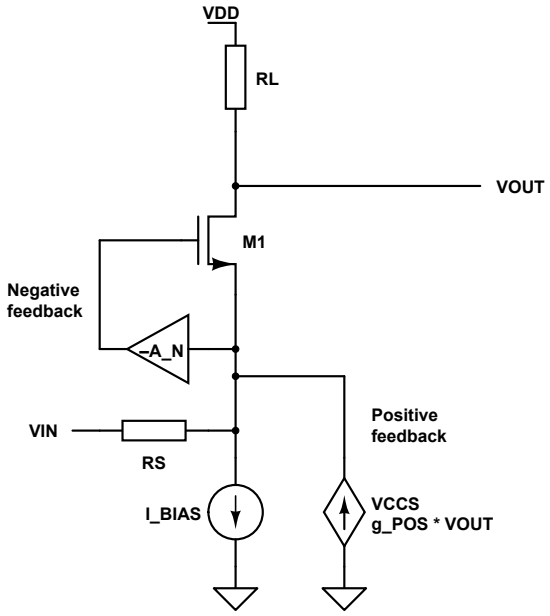


Figure 2.13: Hybrid positive-negative feedback LNA topology [22].

(i.e. the third derivative of the quasi-static voltage transfer function). Additionally, Guo and Huang applied a similar technique and further found, for their multistage cascode LNA topology, that the second stage's noise contribution is negligible beyond a certain device width, and that there exists a point of maximum linearity with respect to the common source transistor's width, when the bias current is held constant [20].

Rashtian et al. propose a method of gain control and noise/linearity optimisation via an adjustable body voltage which forward biases the body diode [21]. Using this principle, they designed a 60 GHz 4-stage cascode LNA with variable gain in 65 nm CMOS. Linearity optimisation is achieved by optimising only the last stage, similarly to above; the body voltage V_{SB} is adjusted such that $d^2 g_{mB}/dV_{SB}^2 = 0$, where g_{mB} is the transconductance with respect to the source-body voltage. This is analogous to (2.33), which can be understood from the V_{SB} behaviour as a "second gate", analogous to V_{GS}. They achieved a 1 dBm $\mathrm{IIP3}_{\mathrm{max}}$.

Woo et al. (2012) examine feedback techniques in LNAs and propose a new hybrid positive-negative feedback technique, applying it to a noise-and-linearity optimised LNA design [22]. The proposed design, based on a single-stage common-gate topology and shown conceptually Fig. 2.13, adds a negative feedback loop to a prior positive-feedback topology, which decouples Z_{IN} from effective g_m (simplifying input matching), allows higher G_m and increases Z_{OUT}. This improve gain and noise performance. Furthermore, their nonlinear analysis finds that 2nd order cancellation from a differential topology holds despite the positive feedback loop, and that the proper selection of positive feedback loop gain results in

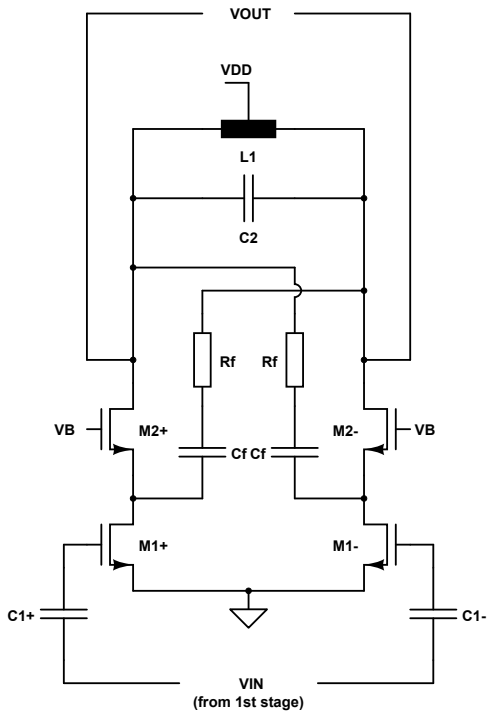


Figure 2.14: Negative feedback of third-order harmonics in a differential cascode LNA stage [23].

the cancellation of several terms in the 3rd-order Taylor series coefficient, thus improving IIP3. Whereas the input matching properties of this topology are not useful to the optical receiver frontend, the positive feedback result is of interest.

Yoon and Park (2014) rely on filtering and feeding back the third harmonic using an RC network in order to effect third-order cancellation [23]. Their design is based on a 2-stage, inductively loaded, differential cascode LNA. The second stage is optimised for linearity by introducing cross-coupled negative feedback of the third-order harmonic. This feedback loop is positioned at the output of the LNA and feeds back to the input of the common-gate stage of the cascode, filtered via an RC network (forming a high-pass filter), as shown in Fig. 2.14. They report an improvement of 3 dB in third-order harmonic. While included here for possible relevance to narrow-band optical communication applications, this technique cannot be used for the wide-band focus we are exploring in the present work.

As this overview has shown, LNA designs appear to primarily focus on the last stage of multistage designs to optimise linearity, utilise a variety of methods from bias point and transistor size optimisation to feedback techniques. While some of these techniques rely on narrow-band operation, others operate on quasi-static linearity or are otherwise not bound to a narrow-band assumption; LNA approaches to multi-stage and transistor-level optimisation and the hybrid positive-negative feedback technique may be applicable to a wide-band optical

amplifier.

2.9 High-linearity optical receivers

Literature exists in a number of application areas that require optical receivers with higher linearity than baseband 2-level communications applications. A few of these applications and a sample of related research is presented below. While the referenced works have characterised or analysed linearity in some way, we did not find works that specifically looked at design methodologies for linearity optimisation.

Xiao and Wang (2006) propose a 5.2 GHz narrow-band optical receiver frontend in 0.18 µm CMOS, targeted for radio-over-fibre applications [24]. This work makes use of an RF LNA design adapted to the optical receiver context; it consists of two stages, an inductive source-degenerated cascode LNA followed by a common-source LNA, with a series inductor matching network (via a length-adjusted bondwire) to optimise gain and input-referred noise. They achieved a transimpedance gain of 58.576 dBΩ, input-referred noise of 6.875 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ and an IIP3 > 5 dBm.

Peng et al. (2017) describe a receiver frontend design for 20 Gb/s PAM-4 applications in 0.18 µm CMOS [25]. This design makes use of a fully differential architecture, with two modified regulated cascode TIAs, and a two-stage differential post-amplifier with resistor shunt negative feedback around both stages. Linearity optimisation is not specifically discussed in this paper; however, we expect the negative feedback around these last two stages contribute to improved linearity, as discussed in Section 2.4.2. The results in [25] also show that using AGC achieves a higher linearity. Their design achieves a transimpedance gain of 51.7 dBΩ at 100 µA input, a bandwidth of 7.29 GHz, input-referred noise density of 23.6 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$, and THD as low as 2%.

Ahmed et al. (2018) have demonstrated a 34 Gbaud dual-polarisation 16QAM design in 0.13 nm SiGe using a fully differential architecture [26]. The design has a nominal 73 dBΩ gain, automatic gain control (AGC), and a 50 Ω output driver. At a 500 mVpp output level, it achieved a THD of 1.5%. This design's linearity is attributed to an AGC loop which controls both a variable-gain TIA and a variable-gain post-amplifier stage, in addition to fixed post-amplifier gain stages.

Chapter 3

Tuning the dynamic response of a positive-feedback receiver

In Section 2.7, the positive feedback technique for bandwidth extension was introduced. In that prior work, concerns of dynamic response were raised (overshoot and ringing). In particular, despite of the negligible (0.6 dB) peaking in the frequency domain, the pulse response of the positive-feedback circuit is underdamped, causing ringing in response to digital transitions and producing an unclean eye diagram. While a benefit to the technique is still visible, this dynamic response serves to limit it.

We considered whether any additional design variables could be harnessed to improve the receiver performance, while maintaining the same analog bandwidth (i.e. same bandwidth extension provided by the positive feedback method, compared to the reference circuit). In the prior work, identical positive feedback gain was applied to all 3 PA stages of the amplifier; if the feedback gain of each PA was allowed to be set independently, we hypothesised that the three feedback coefficients could be designed to better tune the dynamic response, at the expense of greater design complexity. Furthermore, we present a root locus analysis in order to characterise this tuning and develop recommendations for a design methodology.

3.1 Performance criteria

From the above overview on prior work by Ni, some performance criteria become apparent for this investigation.

3.1.1 Bandwidth

Since the headline of the technique under investigation is bandwidth extension, we will of course be concerned with the circuit −3 dB bandwidth. Since we are attempting to improve the positive feedback method, building on the prior work by Ni, our criterion is to maintain the same bandwidth extension previously reported. However, bandwidth alone does not determine performance at a given data rate: there exist further concerns about stability and dynamic response.

3.1.2 Dynamic response: frequency response, overshoot and eye opening

In addition to −3 dB bandwidth in the frequency domain response, the dynamic response can significantly affect performance. However, it is readily apparent, from the literature in Section 2.1 and 2.6.2, that many authors refer to the frequency response's bandwidth and flatness to gauge the speed and performance of optical receiver frontends. In the case of RF/microwave circuits, where signals are often viewed in the frequency domain, this is a reasonable approach; however, for transmission of OOK digital signals and similar, a broader view of the dynamic response is necessary. Filter design provides us a simple example of the inexact correlation between gain flatness and step response overshoot: the classic 2nd-order Butterworth filter is maximally flat in the frequency domain, and yet exhibits a small amount of overshoot in its pulse response.

The eye diagram is the primary metric for performance. For simplicity, we will only be looking at the maximum vertical eye opening; to account for clock jitter, we assume this opening is sampled over a particular time interval. That is to say, visually speaking, if we have a rectangle of a certain width (time interval), what is the maximum height (voltage) that could fit within the eye?

We will also be qualitatively considering the 'undershoot' of the ringing response visible in the eye diagram—that is, the first trough after the overshoot, which appears to particularly contribute to eye closure. This particular form of ISI seen in the time-domain is strongly related to variations in group delay, or equivalently, phase linearity in the frequency domain. In order to transmit a pulse without distortion, a constant group delay is needed within the amplifier's passband [27:388]—any variations in group delay value will tend to cause distortion.

Thus, overall, we will be characterising the dynamic response quality using the vertical eye opening and the group delay variation.

3.1.3 Other performance criteria

We will also be considering conventional performance criteria:

- **Noise** - In order to compare noise between the reference circuit (lower bandwidth) and positive-feedback circuits, we will examine the input-referred equivalent noise density in order to compare noise in a bandwidth-independent way, as well as considering total integrated input-referred noise.
- **Power dissipation** - DC power dissipation due to amplifier bias currents.

3.2 Brute-force search

In order to demonstrate the viability of an unequally tuned feedback circuit, we began with the positive feedback design defined in Section 2.7.2 and shown in Fig. 2.11b. In simulation, using the same TSMC 65 nm technology and toolkit, we varied the feedback coefficients $x_{1,2,3}$ with a three-variable parametric sweep (by varying the widths of the feedback amplifier transistors, at the same NMOS/PMOS ratio). 16 values from 0.02 to 0.20 were swept for each variable, producing a 4096-point sample set of the problem space.

We wanted to demonstrate improved dynamic response at the same bandwidth of 18.3 GHz, operating at 26.1 Gbps per the 70%-of-data rate rule of thumb. Thus, the candidates were filtered for approximately equal BW, simulated at 26.1 Gbps and sorted by eye opening. The candidates were then manually inspected for a candidate showing good overall performance improvement, presented in the next section.

3.3 Unequal feedback design

From the parametric sweep data set, an unequal-feedback design was selected that maximises the eye opening with a similar bandwidth to the equal-feedback design of 18.3 GHz. The PA feedback resistors are adjusted in order to match the gain of this design to the previous two circuits, and this circuit is simulated and compared to the reference and equal-feedback design. The design and simulation parameters are given in Table 3.1, corresponding to the schematic of Fig. 2.11b and the transistor-level diagram (TIA and first stage PA only) of Fig. 3.1. An output capacitance is added to the circuit output in order to model the next stage input, assumed identical to the PA stage input measured at at 68 fF in simulation.

The simulation results are summarised in Table 3.2. We note that this solution's feedback ratios are different from one another, with the first feedback ratio at the minimum sweep

Table 3.1: Design and simulation parameters

Par.		Ref.	Equal	Unequal	Unit
TIA feedback resistance	R_F	400.0	400.0	400.0	Ω
PA feedback resistance	$R_{F1,2,3}$	155.8	140.5	135.8	Ω
Forward amp MOS width (all)	$W_{n,p0,1,2,3}$	30	30	30	µm
Forward amp MOS length (all)	$W_{n,p0,1,2,3}$	60	60	60	nm
Feedback ratio 1	x_1	–	0.087	0.0200	
Feedback ratio 2	x_2	–	0.087	0.1427	
Feedback ratio 3	x_3	–	0.087	0.1120	
Photodiode cap.	C_{IN}	100	100	100	fF
Output cap. load	C_{OUT}	68	68	68	fF
Input (nominal)	I_{in}	±15	±15	±15	µA
Transimpedance	R_T	85.8	85.8	85.8	dBΩ
Target birate	R_B	26.1	26.1	26.1	Gb/s
(Bit period)	T_B	38.3	38.3	38.3	ps

Table 3.2: Positive feedback simulation results

Par.	Ref.	Equal	Unequal	Unit
Bandwidth	12.4	18.3	18.1	GHz
AC peaking	0.0	0.6	0.0	dBΩ
Group delay variation (to BW)	1.9	13.6	11.8	ps
Vertical eye opening	426.5	463.4	499.0	mV
Integrated output noise	21.0	28.1	27.2	mVrms
Ratio noise/eye op.	0.049	0.060	0.054	V/V
Input noise density	9.67	10.7	10.0	$\text{pA}/\sqrt{\text{Hz}}$
Power dissipation	32.9	34.0	34.1	mW

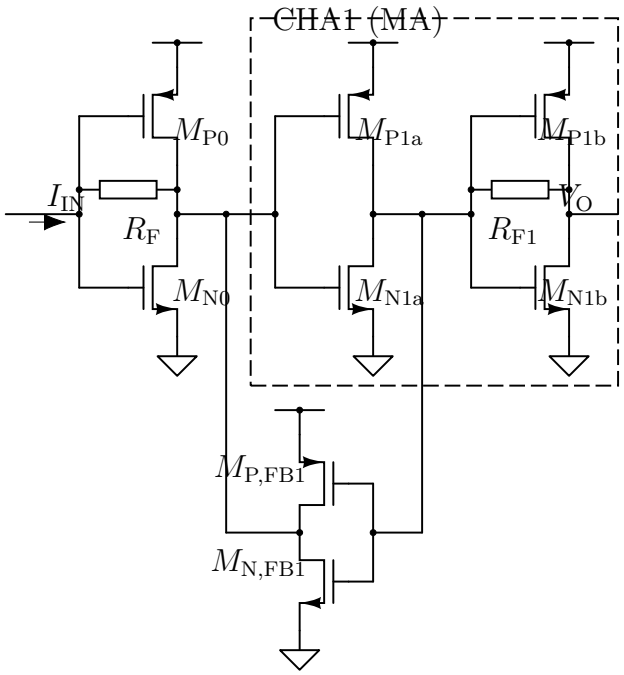


Figure 3.1: Transistor-level schematic of the receiver design (TIA and first of 3 PA stages only; remaining PA stages identical).

value—perhaps the interaction of FB1 with the TIA is more significant than FB2/FB3 interactions with the previous CHA stage, favouring low or possibly zero feedback on the first CHA stage.

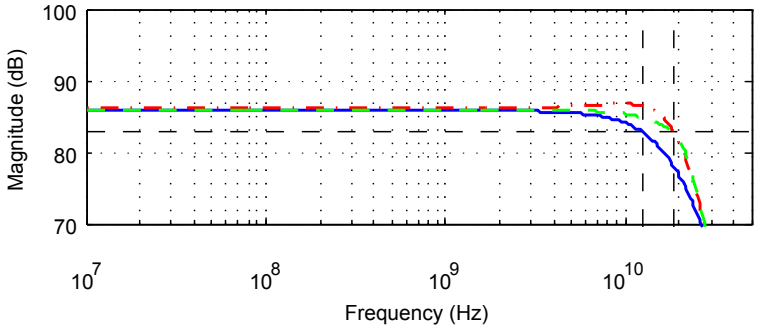
The frequency-domain response and group delay are shown in Fig. 3.2.

The time domain simulation was performed at $R_b = 26.1\,\text{Gbps}$, as explained earlier. The input is a $\pm 15\,\mu\text{A}$ pseudo-random binary sequence (PRBS) encoded as a non-return-to-zero on-off signal, with transitions smoothed through an ideal fourth-order filter of bandwidth $2R_b$ consisting of real repeated poles, to provide realistic rise and fall times at the input. Peak-to-peak signal voltages for the unequal circuit are 9.89 mV at TIA output, 38.8 mV at CHA1 output, 163 mV at CHA2, and 537 mV at CHA3. These signals are all present superposed onto a DC bias voltage of 530 mV to 570 mV, depending on the node.

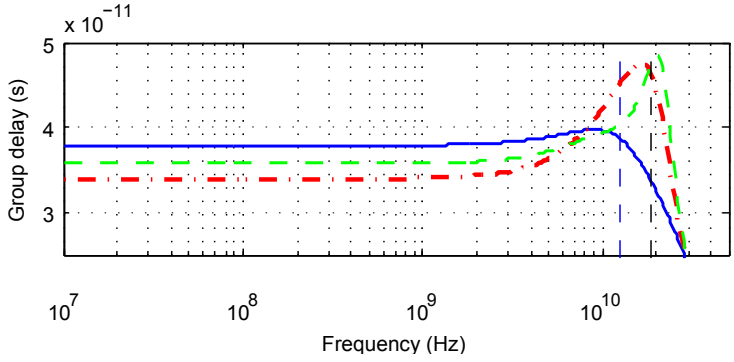
To measure the simulated eye opening, a clock jitter of 9.6 ps (25% of the bit period) is assumed. Consequently, the eye opening is measured as the maximum vertical distance that can fit within a 9.6 ps-wide interval.

The unequal-feedback circuit's performance is compared to the reference and to the equal-feedback circuit. As a reminder, both feedback circuits are based on the same reference design and matched in gain and bandwidth, with the primary performance metric being dynamic response in the time domain and hence eye opening.

Eye diagrams are shown in Fig. 3.3, with the reference and equal circuit eye diagrams

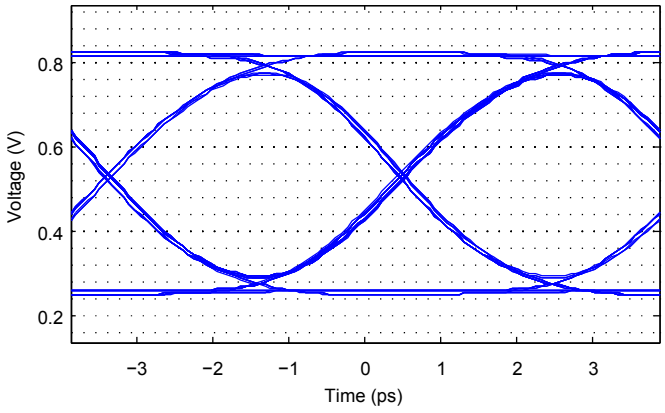


(a)

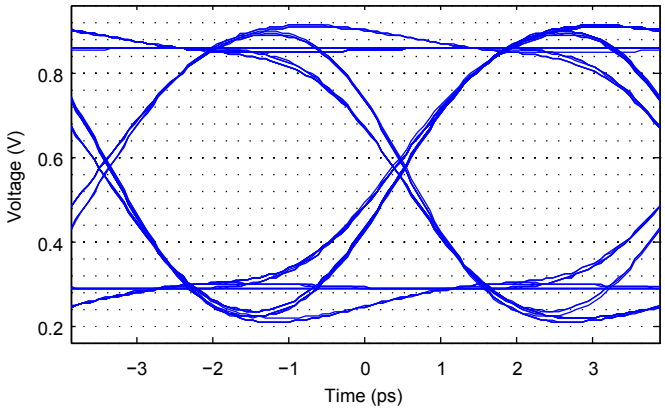


(b)

Figure 3.2: AC simulation results of all circuits. Solid trace: reference; dashed (red) = equal feedback; dot-dashed (green) = unequal feedback. Dashed vertical lines at 12.4 GHz and 18.1 GHz (circuit bandwidths). a) AC magnitude; b) group delay. Reproduced from [1], © 2015 IEEE.



(a)



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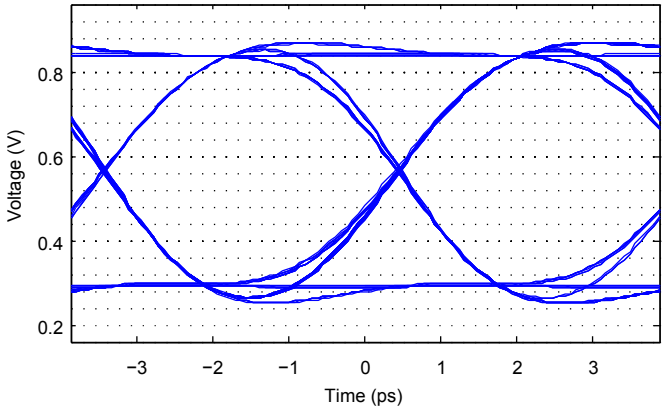


(c)

Figure 3.3: Eye diagrams for time-domain simulation of PRBS input at 26.1 Gbps. a) Reference circuit; b) Equal feedback circuit; c) Unequal feedback circuit. Reproduced from [1], © 2015 IEEE.

reproduced from Section 2.7.2 for convenience. The equal-feedback circuit improves the vertical eye opening by 8%, whereas the unequal-feedback circuit improves by 17%. Furthermore, the eye opening of 499.0 mV reaches about 90% of the maximum voltage swing of this circuit (approximately 560 mV). It is worth noting that, although overshoot is a typical measurement of pulse response, the eye diagram closure is primarily related to the subsequent undershoot present in underdamped systems (and a subsequent bit transition that occurs during this undershoot).

Variation in group delay, and the resulting phase distortion, is correlated to intersymbol interference and poor dynamic response. It is desirable to reduce group delay variation, or ideally maintain a constant or maximally flat group delay. Table 3.2 and Fig. 3.2b show that the equal-feedback circuit has a group delay that varies from 33.9 ps to 47.5 ps within the circuit's bandwidth, a variation of 36% of the bit period. In comparison, the unequal-feedback circuit has a group delay variation of 30.5% of the bit period; we also note that the group delay peak is narrower and at a higher frequency (around the bandwidth), at which the output magnitude is attenuated and less capable of causing meaningful waveform distortion. These observations on group delay agree with the eye opening results.

Total noise (integrated overall all frequencies, i.e., 0 GHz to 100 GHz in simulation) increases substantially relative to the reference circuit due to the higher circuit bandwidth. If we instead look at equivalent input noise density $v_n / \left(R_T \times \sqrt{\mathrm{BW}}\right)$, the equal-feedback circuit's noise power increases by about 22%, whereas the unequal-feedback circuit fares substantially better, increasing only by 7%. We also note that if we look at the ratio of noise to eye opening, while noise has still increased, it appears less severe than the absolute noise voltage alone.

Overall, we find that the unequal-feedback circuit performs better than the equal-feedback approach across all the performance metrics examined, at the expense of greater design complexity. Indeed, a computationally expensive brute-force approach was used to find this circuit candidate. In the following sections, we undertake a preliminary examination of the pole-zero perspective of system dynamics, in order to pave a path towards a systematic design methodology.

3.4 Pole-zero analysis of equal-feedback circuit

In order to better understand the dynamics of these circuits, we analysed the Laplace domain poles determined by simulation. The goal of this analysis is to develop a preliminary, qualitative understanding of the relationship between the pole locations, AC response and eye diagram (transient response), and of how these poles move as we increase the ratio of

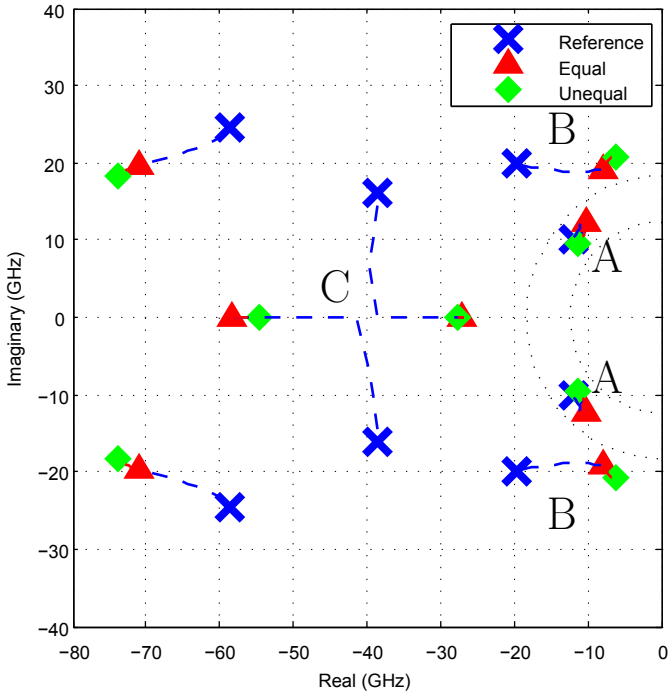


Figure 3.4: Pole plot for all 3 circuits. Dotted line shows root locus as x increases from zero (reference circuit) to equal circuit values. Reproduced from [1], © 2015 IEEE.

positive feedback in order to extend the bandwidth compared to the reference circuit.

Fig. 3.4 plots the poles for all three circuits. The dotted lines between the markers for the reference and equal-feedback circuits show the root locus of these poles as the feedback coefficients $x_1 = x_2 = x_3$ are increased simultaneously from 0 to 0.087. The two dotted circles are at radii 12.4 GHz and 18.1 GHz (i.e. the reference and feedback circuit bandwidths, respectively). No zeroes of significance to the passband exist.

In the reference circuit, the frequency-domain response is dominated by the "A" poles, at a natural frequency f_n of 15.6 GHz and quality factor $Q \approx 1/\sqrt{2}$. Neglecting other poles, this pole pair yields a response similar to a second-order Butterworth filter and a clean eye diagram (Fig. 3.3). We note, in particular, that some eye closure exists due to the high test data rate and that overshoot is minimal, as is expected from a Butterworth filter-like response.

The equal-feedback circuit has increased the "A" pole Q-factor slightly, possibly contributing some frequency-domain peaking. More significantly, the "B" poles at $f_n = 20.8$ GHz have moved horizontally towards the $j\omega$ axis, at a lower frequency and significantly higher Q-factor. The other poles have natural frequencies significantly higher than the bandwidth and are not considered significant to the passband. We understand the B poles to cause resonant peaking at a frequency above the original 12.4 GHz bandwidth figure, which serves

to extend the bandwidth. However, these poles also serve to increase the group delay variation (phase distortion) within the region of that bandwidth extension, as visible in Fig. 3.2b, causing ringing in the pulse response and resulting in a less clean eye diagram.

Considering the root locus more generally, the most significant effect of increasing positive feedback coefficient x appears to be on the "B" poles, which move horizontally, approaching the "A" poles' frequency while increasing in Q-factor. The bandwidth extension effected is similar to that of inductive peaking techniques. The "A" pole movement is relatively subtle, while "C" poles are at a higher natural frequency and assumed negligible in this analysis.

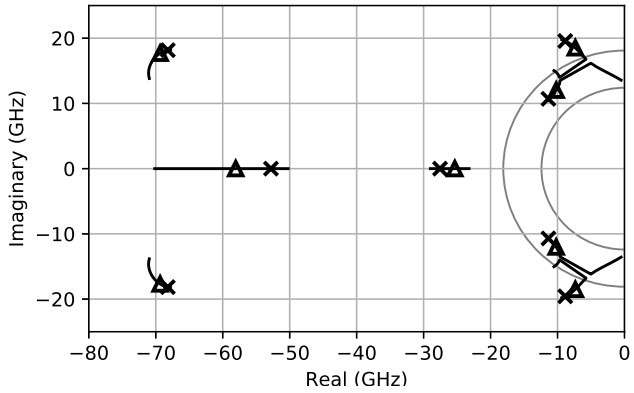
With the unequal feedback circuit, the poles are only subtly adjusted. The "B" poles move slightly higher in frequency and Q-factor, while the "A" poles reduce in Q-factor, returning nearly to the reference circuit's position. From an AC magnitude perspective, these changes appear to trade off some lower-frequency peaking from the "A" poles with more peaking from the "B" poles to effect the same bandwidth extension. From a group delay perspective, we can relate these poles to a flatter group delay curve, with the "A" poles contributing less at lower frequencies and allowing the group delay peak to be narrower and at a higher frequency.

This qualitative analysis gives us a first view into the dynamics of the system with respect to the x parameter, and how we can intuitively understand the results that were previously shown. We can interpret the "A" pole as determining the low-frequency response of the system (albeit still affected slightly by the positive feedback), with the "B" poles providing resonant peaking bandwidth extension due to the positive feedback, and other poles being nonsignificant. Proceeding with the idea of tuning the three feedback gains independently, the next section will examine the root locus for each of these individual gains.

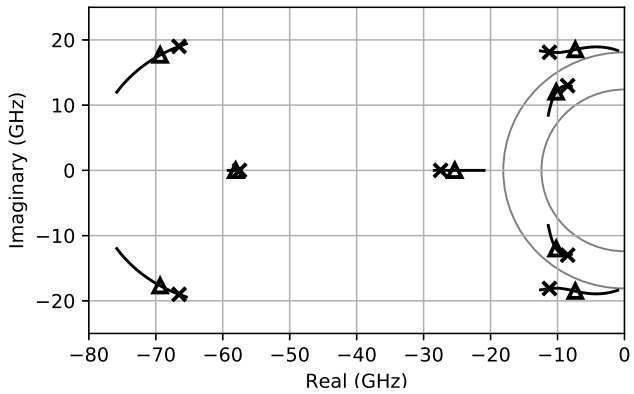
3.5 Root locus of unequal positive feedback

We have explored the possibility of tuning each of x_1, x_2 and x_3 independently in order to improve the dynamic response at similar bandwidth extension. In order to show a proof of concept, we used a brute-force three-parameter sweep to find a better-performing candidate; however, this does not provide insight useful to developing a design methodology based on this concept. In this section, we explore the root locus of the "A" and "B" poles of the system when each feedback parameter x is separately sweeped, using the data from our previous brute-force simulations.

Each stage of the reference circuit, shown in Fig. 2.11b, forms a second-order system. We can identify eight pairs of poles, which modelled ideally would correspond pairwise to each stage of the system (TIA + 3 PA stages). Introducing positive feedback provides



(a)



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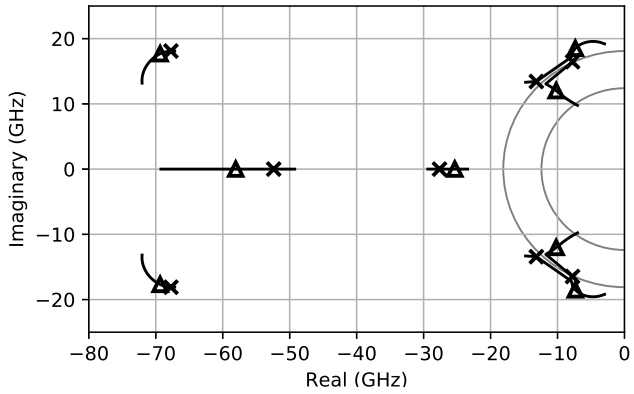


(c)

Figure 3.5: Root locus of receiver poles as each feedback ratio $x_{1,2,3}$ is independently varied. Circles have radii 12.4 GHz and 18.1 GHz (circuit bandwidths). × denotes $x_{1,2,3} = 0.0200$ (minimum), △ denotes $x_{1,2,3} = 0.0813$. a) $x_1 = 0.02$ to 0.25, $x_2 = x_3 = 0.08133$. b) $x_2 = 0.02$ to 0.25, $x_1 = x_3 = 0.08133$. c) $x_3 = 0.02$ to 0.25, $x_1 = x_2 = 0.08133$.

new parameters with which we can tune the dynamic response of the system, in addition to extending bandwidth. Naïvely, we might hope that each positive feedback ratio would correspond exactly to one pair of poles, providing a clear and simple tuning ability. However, from any stage's output, there exists a full feedback path to any previous signal node, via the positive feedback amplifiers and negative feedback resistors. This creates complex feedback interactions that affect every pole more strongly than parasitic C_{gd} would otherwise.

In order to understand what potential these positive feedback gains provide us in tuning the dynamic response of such a circuit, we examine the root locus as each feedback ratio $x_{1,2,3}$ is varied and the other two held constant. The reference design chosen is for values $x_{1,2,3} = 0.08133$, as this is the closest design to the equal-feedback circuit available in the brute-force data set.

Fig. 3.5 shows the root loci as each x is varied from 0.02 to 0.25, and the other two x values are held constant at 0.08133. For each pole, the reference point at minimum x and at the reference value of 0.08133 are shown; furthermore, circles are drawn at 12.4 GHz and 18.1 GHz (the circuit bandwidths) to provide a visual reference point. We will again focus on the "A" and "B" poles as discussed in the previous section.

We first examine the x_2 root locus (Fig. 3.5b). We previously established that the "B" poles provide bandwidth extension by resonant peaking, similar to inductive peaking methods; in this case, we can clearly see that increasing x_2 moves the "B" pole clearly horizontally, permitting this effect. Furthermore, the "A" poles slightly decrease in Q at almost constant pole frequency ω_p, which may further reduce overshoot. From these observations, increasing x_2 appears to be very beneficial to the dynamic response of the system. In fact, in our unequal-feedback design, it had the highest feedback gain.

The x_3 root locus (Fig. 3.5c) also appears useful. The "B" poles move diagonally, roughly increasing in Q at constant ω_p, also permitting the resonant peaking effect to extend bandwidth, without the reduction of the pole frequency seen with x_2. The "A" poles initially reduce in Q, but shortly before reaching $x_3 = 0.08133$ start moving radially inward, reducing pole frequency and potentially reducing passband flatness. It appears x_3 may be useful at bandwidth extension up to the point that the "A" poles move radially inward.

The x_1 root locus (Fig. 3.5a) suggest its useful effect is extremely limited. Between the $x_1 = 0.02$ to 0.08133 markers, very little movement of the "A" and "B" poles occur, followed by a very quick destabilisation of the "A" poles as Q increases suddenly. The "B" poles move lower in Q, failing to provide the bandwidth extension effect. Indeed, in the unequal-feedback design, this feedback value is minimum (0.02), and we suspect may preferably have been omitted entirely.

From this analysis, we can suggest preliminary design recommendations for this system.

It appears that x_2 and x_3 are the most important parameters to tune the dynamic response of our design, as both increase the Q of the "B" poles and decrease the Q of the "A" poles, as desired. x_2 tends to decrease the pole frequency of the "B" poles while x_3 does not affect it or slightly increases it, allowing some ability to tune both Q and pole frequency of the "B" poles. x_1's effect appears detrimental and should remain at 0 or small values.

This analysis focuses specifically on a single receiver system with feedback ratios $x_{1,2,3} = 0.08133$. These particular conclusions on the effect of each feedback parameter x may not be generalisable to cases where the technology, reference circuit design, or values of the non-swept feedback ratios differ significantly.

3.6 Discussion

The unequal-feedback design has proven to allow an improvement in overall dynamic response compared to the equal-feedback design, for the same bandwidth. These improvements may allow the positive-feedback technique to be pushed further, allowing further bandwidth extension and higher data rate for a receiver in a given semiconductor technology. Relative to the equal-feedback design, the use of unequal feedback has no significant impact on power consumption and silicon area, while improving both the eye opening and noise performance.

However, the main trade-off of unequal feedback is design complexity, introducing three design variables and greater complexity in how these variables affect the response. The equal feedback design, on the other hand, maintains a significant simplicity, with only one new design variable and consequently a straightforward understanding of the relative stability of the system, as discussed in Section 2.7.1. The pole-zero approach may help reduce that complexity: if we understand how these new design variables affect the pole zero approach, then we can potentially make use of filter design and control system knowledge to optimise the dynamic response. Ultimately, the goal would be to develop a straightforward sweep simulation-based design technique that allows for a quick, simple first design iteration while achieving the improved response possible from an unequal feedback design.

Chapter 4

Design of a high-linearity optical receiver frontend

In the previous chapter, we focused on optical communications applications that transmit OOK binary data. It is evidently possible to use other modulation methods over optical channels, and indeed to find other applications of optical signal transmission, such as pulse amplitude modulation (PAM) [25], quadrature phase-shift keying (QPSK)[28], or quadrature amplitude modulation (QAM) [26]. Additionally, we can find applications such as medical imaging [29], photonic microwave signal processing[30, 31], and radio-over-fibre [32, 33] that make use of optical signal transmission. OOK signals only requires the discrimination of two signal states (optical power values), and thus has little need for a highly linear optical receiver frontend; however, all of these examples require discrimination of multiple signal levels (e.g. PAM) or analog signal spectra. Thus, in these applications, the optical receiver frontend has a greater need for high linearity.

At the onset of this study, we did not find any literature which discussed the optimisation of linearity in optical receiver frontends, and only limited literature which reports linearity measurements (without discussing design optimisation). Thus, we investigate the design of a linearity-optimised wideband optical receiver, and design and fabricate two optical receiver circuits in GlobalFoundries (formerly IBM) 0.13 µm CMOS.

As discussed in Section 2.6.2, we hypothesized that the interleaving feedback topology proposed in [8] would provide better linearisation than cascaded second-[34] or third-order stages with only local feedback, as it provides a full feedback path from output to input thanks to the interleaving feedback paths. We also investigated the possibility that using different feedback gains, while introducing additional design complexity, could further improve performance. For this work, we originally had in mind a larger project consisting of

an integrated microwave signal processing chip with built-in electrical-optical and optical-electrical converters, for which we have primarily adopted a frequency-domain approach, but our methodology could easily be adapted to the other applications suggested previously.

Per the discussion in Section 2.3.3, both circuits focus on linearising the post-amplifier and make use of identical TIAs and other elements of the design. In particular, the two circuits compare two different approaches to setting the negative feedback gains of the same post-amplifier topology.

In the next section, we will briefly discuss the performance metrics for this chip. We will then define the architecture of the proposed designs and discuss design specifications for each block in this architecture, common to both circuits. In the remainder of this chapter, we will discuss the circuit topologies selected, investigations carried out to achieve the target specifications and research objectives, and design methods developed. The core of the work is the PA design and linearity optimisation, presented in section 4.4.

4.1 Performance metrics

For these designs, we are foremost interested in linearity. We have primarily referred to the IP3, given its common use in RF and microwave systems to characterise weak nonlinearities (e.g. in [24]); we are interested specifically in the third-order distortion, because the choice of a differential architecture suppresses even-order distortion, so the third-order distortion is generally the most significant distortion product.

We also later consider the THD, which has been used in [25, 26] for receivers for PAM-4 and 16-QAM applications, respectively.

Besides linearity, we are also interested in the noise performance of our system. In particular, we have generally looked at the equivalent noise density S_{vn}, defined as

$$S_{vn} = \frac{\overline{v_{n,o}}}{\sqrt{\mathrm{BW}}} \tag{4.1}$$

where $\overline{v_{n,o}}$ is the total rms output noise, integrated over all frequencies, and BW is the circuit bandwidth. We have also looked at the total output noise integrated in the range 1.0 GHz to 1.1 GHz, as representative of noise density in an assumed operational band around 1.05 GHz. We also briefly look at gain-bandwidth/linearity tradeoffs.

While the chip is designed to drive a 50 Ω transmission line in order to enable testing, our research and simulation results primarily focused on the TIA+PA system, excluding the output driver; we envisioned that this frontend could include further processing of the

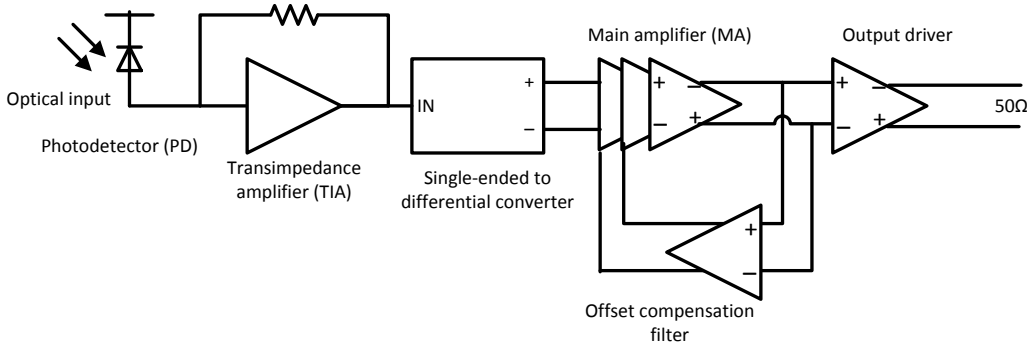


Figure 4.1: Proposed receiver architecture block diagram.

signal on-chip, rather than immediately exporting it off-chip. Furthermore, "system linearity" refers to the TIA+PA system without the output driver, unless otherwise noted. The shortcomings of the output driver are discussed in Section 4.6.

4.2 Architecture & specifications

The proposed system consists of a linear analog optical receiver frontend, shown in Fig. 4.1. It takes, as input, an electrical current from a photodiode (or from test equipment for characterisation), and outputs a differential RF electrical signal which drives two separate $50\,\Omega$ lines.

The system is analysed into blocks, designed separately. The first consists of a single-ended static-inverter-based TIA, followed by a passive single-ended-to-differential converter. This interfaces with a differential PA. An offset compensation filter is looped around the PA in order to reduce offset voltages due to mismatch and common-mode rejection. Finally, an output driver is used to drive the $50\,\Omega$ output lines, providing both impedance buffering and matching to allow measurement of RF signals.

The signal is converted to differential as soon as possible in the system. This decision was made in order to limit second-order nonlinear distortion in the system, allowing further optimisation efforts to focus on odd-order distortion (in particular third order).

The system-level specifications, excluding the driver, are shown in Table 4.1. These specifications are designed to demonstrate the utility of the proposed design methodology to a microwave photonics context, but they are not tailored to any specific application. This, for instance, is why bandwidth is specified in pre-layout simulation, as no application-bound constraint exists. While the system has largely been designed according to its wideband performance, it is occasionally assumed that the target application utilises a 100 MHz channel

Table 4.1: System specifications (excl. driver)

Specification	Value		Comment
Gain	65–70	dBΩ	
Min freq.	10	MHz	
Max freq.	5	GHz	pre-layout sim.
Power	75	mW	max; DC, amplifier bias only
C, photodiode, in	150	fF	
L, bond wire, in	1	nH	1 mm len., 1 mil dia.
C, on-chip, in	70	fF	Nom.: pads (≈ 35 fF), wiring, ESD
C, on-chip, out	200	fF	Max.: pads (≈ 35 fF), wiring, ESD
Z, out	50	Ω	driver, per o/p port (diff = 2x)
SNR out	20	dB	min, 1 GHz to 1.1 GHz
Dynamic range	25	dB	
Min input	3.56	µApp	Sinusoidal
Max input	112	µApp	
Max output	-10	dBm	differential
IMD3	-60	dBc	max, two-tone @ equal power
Max noise out	-55	dBm	from SNR + dyn. range

bandwidth at a carrier frequency above 1 GHz; for example, noise is specified according to this assumption.

4.2.1 Transimpedance amplifier

The TIA uses a single-ended inverter-based feedback topology, as in the previous circuit, designed to the target specifications in Table 4.2.

The TIA is the first gain stage of the system, and thus is the most significant contributor to system noise. For that reason, similar to the TIA designed in Part 2, the TIA must

Table 4.2: TIA specifications

Specification	Value		Comment
Gain	45	dBΩ	
Bandwidth	7.6	GHz	
Power	25	mW	DC amplifier bias
Noise, out	40	µVrms	max, 1.0 GHz to 1.1 GHz (system budget at TIA out)
Output DC bias	0.8	V	nom. Must be within PA input common mode range

provide a larger part of the overall transimpedance gain of the system to optimise noise performance; furthermore, the design's noise performance is optimised at a transistor level (see next chapter), as this provides the most benefit relative to later blocks in the system.

The TIA bandwidth is selected based on a rough approximation of overall bandwidth reduction for cascaded amplifiers. Specifically, we know that the TIA topology proposed is second-order and that the PA is sixth-order. Furthermore, we know that the overall bandwidth BW_{tot} of n identical cascaded second-order stages each with bandwidth BW_S is

$$BW_{tot} = BW_S \sqrt[4]{2^{1/n} - 1} \tag{4.2}$$

[3:178] from which we can obtain a $BW_S = 7.6\,\text{GHz}$ for $n = 2$ (if the PA were second-order), $BW_{tot} = 5\,\text{GHz}$. Of course, the stages are not identical or necessarily Butterworth, and the PA does not consist of second-order stages, so these numbers merely provide a rough target that was adjustable during circuit design.

The noise specification is selected to be roughly 50% of the total output noise. We assume that noise generated in the TIA and PA circuits are uncorrelated; given that uncorrelated noise adds in power, RMS noise voltages add according to

$$v_{n,out,rms} = \sqrt{v_{n,tia,rms}^2 + v_{n,ma,rms}^2} \tag{4.3}$$

where each voltage is referred to the PA output. If both noise components are equal, for a system noise target of $-55\,\text{dBm} = 1.12\,\text{Vrms}$, the TIA can contribute up to $792\,\mu\text{Vrms}$ at the PA output or $44\,\mu\text{Vrms}$ referred to the TIA output.

As previously discussed, the TIA as first gain stage has a lesser contribution to system nonlinearity compared to later stages, and this contribution was found to be minimal during preliminary investigation (see Section 4.3 for final design values). A linearity (IP3) target is therefore not specified.

4.2.2 Single-ended to differential converter

The TIA has a single-ended output and the PA has a differential input. In order to interface these two circuits, we simply set a DC common mode using a low-pass filter, designed in the next chapter. This block needed to meet the minimum system frequency given in Table 4.1.

4.2.3 Post-amplifier

The post-amplifier (PA) involves the majority of novel design efforts for this system. As the second cascaded block of the system, it is a more significant contributor to system

Table 4.3: PA specifications

Specification	Value		Comment
Gain	25	dBΩ	
Bandwidth	5.5	GHz	
Power	50	mW	
Noise, out	790	µVrms	1.0 GHz to 1.1 GHz (system budget at PA out)
OIP3	-	dBVrms	optimise at low freq.

Table 4.4: Offset cancellation and driver specifications

Specification	Value		Comment
Max output DC offset	80	mV	At PA output, with offset comp.
DC offset cutoff	10	MHz	
Driver gain	unity		
Driver bandwidth	10	GHz	minimum
Output impedance	50	Ω	per output pad

nonlinearity than the TIA, and so linearisation of this block is critical to achieving a highly linear overall frontend. In order to achieve this, this design develops a negative feedback-based approach to optimising for minimal memoryless nonlinearity in the PA.

The PA is fully differential in order to reduce even-order nonlinear distortion.

An approximate bandwidth target was determined as with the previous section, for a 6th-order section (cascade of three 2nd-order stages), per (4.2). Noise target was determined as in the previous section.

4.2.4 Offset compensation

A DC feedback loop is placed around the full post-amplifier block, in order to compensate for differential DC voltage offset in the PA. This block consists of a simple low-pass filter with gain, with specifications defined in Table 4.4.

4.2.5 Driver

The PA was designed independently and optimised for linearity, without consideration for driving an output line. A driver is required to allow for practical RF measurement of a fabricated chip, via standard 50 Ω transmission lines (100 Ω differential output). In the proposed architecture, the driver is connected open-loop to the output of the PA.

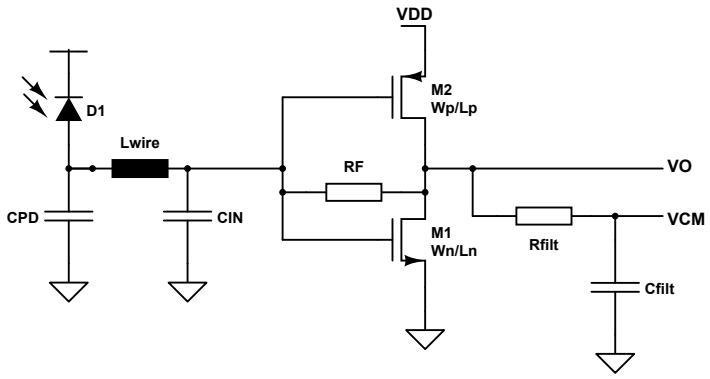


Figure 4.2: TIA circuit schematic with single-ended to differential converter.

Table 4.5: Design parameters of the transimpedance amplifier

Par.	Value	
$L_{n,p}$	120	nm
W_n	20	µm
W_p	80	µm
R_F	230	Ω
R_{filt}	10	kΩ
C_{filt}	15	pΩ

In order for this block not to interfere with measurement results, it should have close to unity gain, significantly higher bandwidth than the system, and linearity (IP3) on the order of—or better than—the system linearity (i.e., input-referred IP3 of the driver higher than output-referred IP3 of the TIA-PA cascade). These specifications are outlined in Table 4.4.

As the final stage of the fabricated chip, the driver is critical to overall measured linearity, but optimisation effort required for this block was underestimated. This is further discussed in Section 4.6, and remains an aspect of improvement for future work.

4.3 Transimpedance amplifier

4.3.1 Topology and circuit design

The TIA, shown in Fig. 4.2, uses the same inverter-based feedback topology previously discussed. The design parameters are shown in Table 4.5.

The core TIA design consists of M_1, M_2 and R_F. We will begin by motivating this particular topology.

As previously discussed, the TIA is not linearity-critical. Given this, a feedback TIA is

preferred over a shunt-resistor TIA as it removes the tradeoff between gain and noise [2:87], while its negative feedback topology helps mitigate nonlinearity introduced to the system. The inverter-based topology is selected largely for its simplicity, its low input and output impedances, as well as the higher total transistor transconductance g_m per unit of power, thanks to the use of a pair of P- and N-channel transistors, compared to single-transistor amplifiers.

The ratio of widths between M2 and M1 is selected in order to ensure that the TIA's DC output voltage is within the PA's common mode range, sacrificing the transconductance-per-unit-area optimisation from Part II. Performing DC analysis of Fig. 4.2, using the square-law MOSFET model, we find that the DC output is

$$V_o = \frac{\frac{\mu_p W_p}{\mu_n W_n}\left(V_{DD} - |V_{tp}|\right) + V_{tn}}{\frac{\mu_p W_p}{\mu_n W_n} + 1} \,. \tag{4.4}$$

Assuming $\mu_p/\mu_n = 1/3$ and $V_{tn} = V_{tp} = 365\,\text{mV}$, as approximated from simulation, we choose $W_p = 4W_n$ to obtain an output DC voltage around 805 mV per this model.

The component parameters were determined through parametric sweeps in simulation in order to meet the TIA performance requirements. With reasonable transistor widths, the R_F value was swept and selected in order to set the gain. Then, the transistor widths were swept to match the desired bandwidth; this step also sets the noise performance.

The photodiode D_1 and the input parasitics are also modelled in Fig. 4.2, and the values used for design are specified in the system specifications of Table 4.1. This model assumes a discrete photodiode die wirebonded to the receiver, and so consists of a photodiode capacitance C_{PD}, wirebond inductance L_{wire} and on-chip input capacitance C_{IN}. The C_{PD} is specified to a maximum of 150 fF, representative of current commercial photodiodes designed for 15 GHz to 25 GHz (e.g. GCS photodiodes DO190_32um_B1 and DO395_40um_Q8 [35]), with 1 nH of bondwire inductance.

4.3.2 Design of the single-ended to differential converter

As briefly mentioned in Section 4.2.2, the TIA output is interfaced to the differential PA input by generating a DC common-mode voltage. This is achieved with a simple first-order passive RC filter (R_{filt} and C_{filt}), also specified in Table 4.5, with a cutoff frequency set to 1 MHz, which is below the minimum system frequency.

Table 4.6: Simulation of the transimpedance amplifier

Parameter	Value		Comment
Gain	45.17	dBΩ	
Peaking	0.915	dB	with L1
Bandwidth	7.504	GHz	without L1, with ESD diodes
DC output	7.99	V	
Power	7.701	mW	
Lower cutoff	10	MHz	
DC rejection	156.0	dB	
Noise out	0.492	mV(rms)	total
	23.41	µV(rms)	1.0 GHz to 1.1 GHz
DC gain var	0.154	%	112 µApp input
OIP3	8.07	dBV(rms)	low-frequency
OIP3	3.32	dBV(rms)	at bandwidth

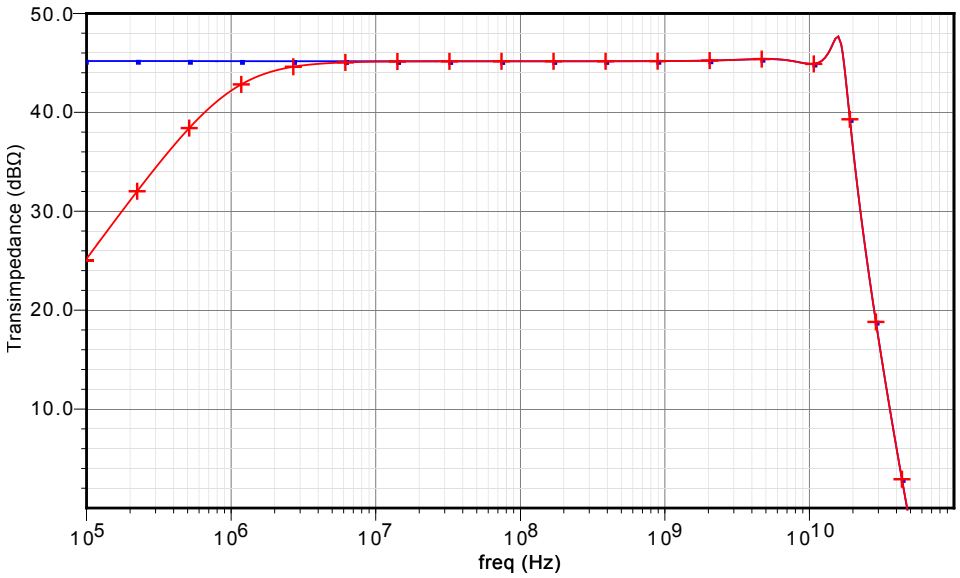
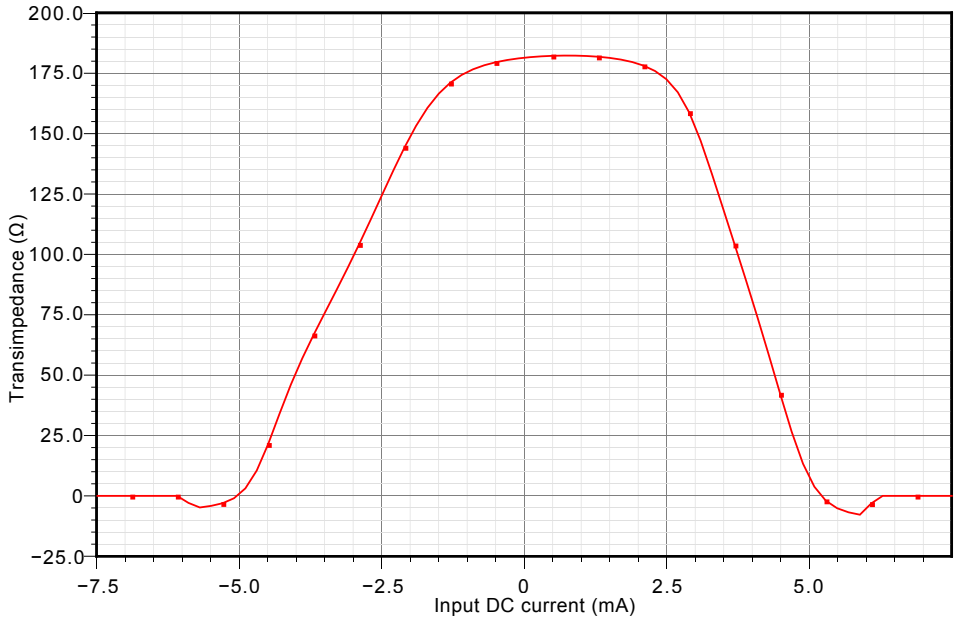
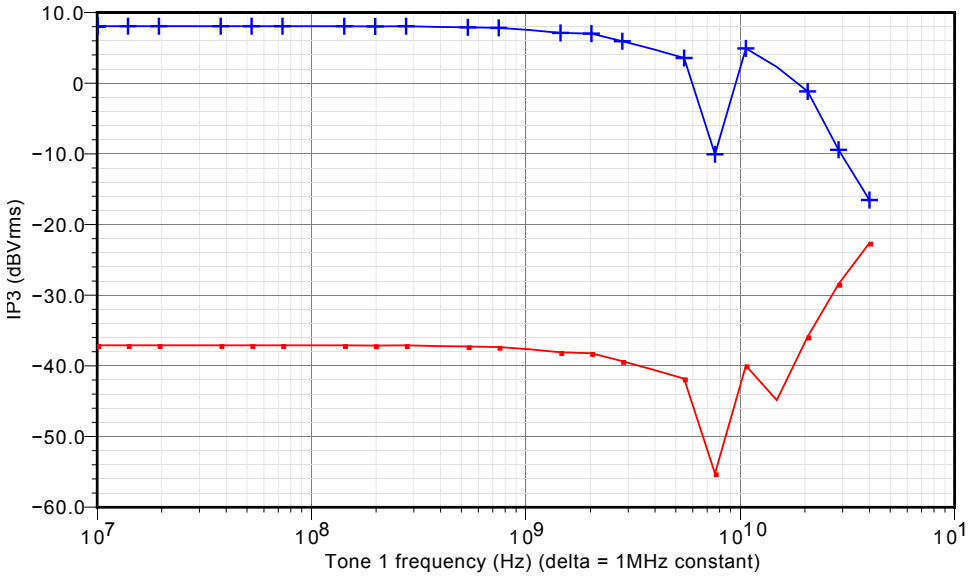


Figure 4.3: AC response of the TIA, single-ended output (blue, square) and differential output (red, +).



(a)



(b)

Figure 4.4: TIA linearity. a) Small-signal DC gain vs. input current. Flatter top is better. b) IP3 as a function of frequency (top: OIP3; bottom: IIP3).

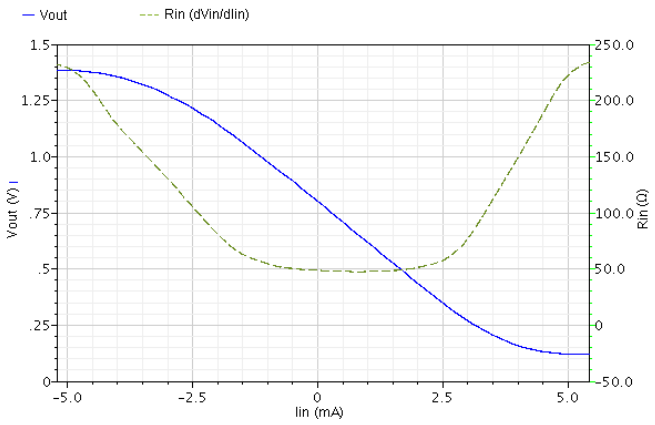


Figure 4.5: TIA DC transfer curve (solid line) and differential resistance (dashed line)

4.3.3 Simulation results

The schematic-level simulation results for the TIA are shown in Table 4.6. Fig 4.3, 4.4a and 4.4b show the AC simulation, DC sweep gain curve, and two-tone test IP3, respectively. Fig. 4.5 shows the DC transfer cuve and differential resistance $dV_{\text{in}}/dI_{\text{in}}$; this value is approximately 50 Ω, convenient for future electrical testing. These simulation results were run with the input parasitic values given in Table 4.1 along with the PA connected to the output as a load, unless otherwise noted.

The bond-wire inductance L_{wire} is observed to have two key effects. On one hand, it resonates with the input capacitances and creates peaking (here around 15 GHz, as seen in the AC simulation of Fig. 4.3). On the other hand, it also isolates C_{PD} and C_{IN}, which the parallel combination of which would reduce the frequency of the input pole and limit bandwidth. Through these effects, L_{wire} serves to extend the bandwidth of the TIA. While this peaking is minimal for the tested parasitics (3 dB without the ESD diode models, < 1 dB with them), it may be useful to further characterise its effects on performance and means of mitigating or making purposeful use of these effects (e.g. in [24] for narrowband applications).

The noise performance of 23.41 µVrms in the band of interest is well within the 40 µVrms budgeted in Table 4.2. A brief look at further minimising noise showed that increasing transistor width significantly reduces bandwidth due to added gate capacitance to the input node, while only marginally reducing noise power above 1 GHz.

As a figure-of-merit for this TIA design's noise performance, in particular compared to a passive shunt-resistor "TIA", we compare the total noise power contribution of the feedback resistor R_F to the overall TIA noise (i.e. R_F + amplifier noise). These results are summarised in Table 4.7, from simulations performed prior to adding the ESD protection diodes to the input. When it comes to broadband noise (integrated over all frequencies), the

Table 4.7: Noise figure-of-merit of the TIA

Par.	Value		Comment
Total noise	0.427	mV(rms)	all frequencies
R_F noise	0.200	mV(rms)	
R_F power contrib.	22.0	%	
Total noise	20.0	µV(rms)	to 1.0 GHz to 1.1 GHz
R_F noise	17.6	µV(rms)	total
R_F power contrib.	77.4	%	

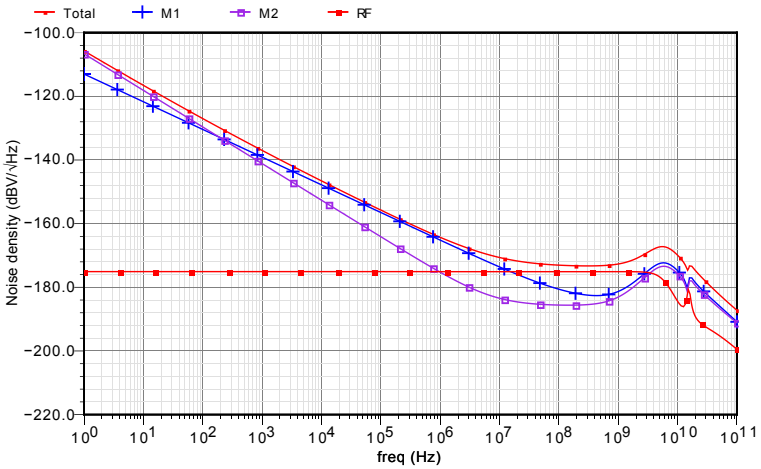


Figure 4.6: Output noise of TIA, and contribution of components.

feedback resistor R_F contributes a minority of the noise power, and this may suggest that this design's noise performance is highly sub-optimal. However, in the 1.0 GHz to 1.1 GHz band, we find it contributes 77% of the noise power, which appears more optimal.

Fig. 4.6 shows the TIA noise spectral density, along with the contributions of M1, M2 and RF to each. We observe that there is a peak around 3 GHz, contributed by the transistors, which contributes significantly to the overall output noise. Further optimisation of this TIA design may investigate how this high-frequency noise peak can be reduced.

The linearity of the TIA is relatively high due to the negative feedback, despite a lack of optimisation effort. Fig. 4.4a shows the small-signal gain as a function of DC input current (or the derivative of the function of output voltage vs. input current), and the flatness of this curve in the input signal swing (x-axis) is used as a qualitative representation of low-frequency linearity. We note a slightly flattened curve in a range in excess of the expected $\approx 65\,\mu\text{App}$ maximum input current (calculated from system specs: maximum $-10\,\text{dBm}$ output at $50\,\Omega$ and gain of $70\,\text{dB}\Omega$).

For more useful quantitative linearity analysis, the IP3 values are considered. At low

frequency, the TIA has an OIP3 8.0 dBV; this is over 15 dB higher than the unequal PA's IIP3 (i.e. both IP3 values are referred to the same node). Thus, the PA's nonlinearity dominates the overall linearity. Examining the IP3 at various frequencies in Fig. 4.4b, we see that the linearity is relatively flat below the GHz range, and begins to drop off as the -3 dB bandwidth edge of the TIA's AC response is approached.

4.4 Post-amplifier

4.4.1 Topology

The post-amplifier uses the interleaving feedback topology originally proposed in [8] and discussed in Section 2.6.2. It consists of two differential third-order stages with negative feedback, along with interleaving feedback in between the two stages (illustrated in Fig. 2.9a). Each amplifier unit, including the feedback amplifiers, consists of NMOS differential pairs with resistor loads; the full transistor circuit is shown in Fig. 4.7 (not shown: all NMOS body terminals tied to ground).

While originally proposed as a means of significant, stable bandwidth extension, in the context of this work we have chosen this topology for its negative feedback, which, in the general case, improves linearity, as discussed in Section 2.4.2. Furthermore, the interleaving feedback provides a full path from the output back to the input, allowing for some global feedback, which we hypothesise would further improve linearity compared to local-only feedback (this is further examined in the THD comparisons of Section 5.4). This topology was thus selected to explore its potential for linearity optimisation and how it may interact or form trade-offs with gain-bandwidth benefits described in the original paper. In particular, we explore the possibility of separately specifying the main feedback and interleaving feedback gains in Section 4.4.4.

In the remainder of this section, we will explore various properties of this topology, design techniques and decisions, followed by a presentation of the final design and simulation results.

4.4.2 DC linearity

In order to determine a design approach for the feedback loops, we first investigated the low-frequency linearity of the PA topology. In order to ensure results can be compared between each other and eliminate variation in linearity due to transistor parameter variation, the following parameters were fixed:

1. All transistors use the thin-oxide, low-threshold-voltage NMOS model.

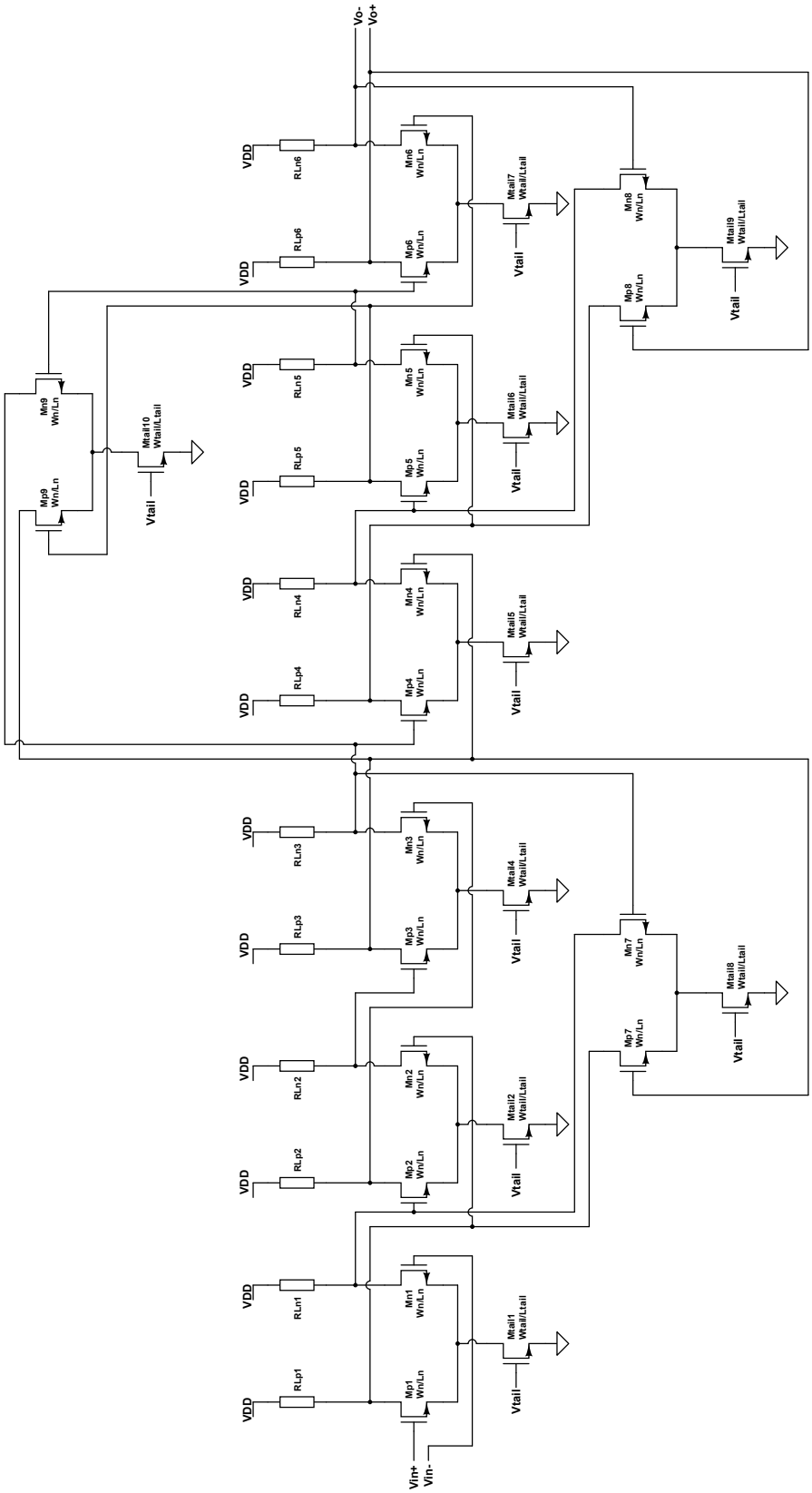


Figure 4.7: Transistor-level schematic of the third-order interleaving feedback PA.

2. The 6x forward amplifier cascade use fixed transistor parameters, equal to the final design values in Section 4.4.5.

3. The feedback amplifier transistors maintain constant channel length and overdrive voltage $V_{gs} - V_{th}$, equal to the final design values.

We first examine DC linearity by means of the DC transfer function. If we consider the output voltage vs. input voltage transfer function (both differential voltages), we expect that for a perfectly linear system, the curve would be perfectly linear within its signal input range, and that curve's derivative, which represents the DC small-signal gain at any given DC input, would be constant. We will examine the PA's DC small-signal gain in simulation as we vary the feedback gain, keeping all 3 feedback amplifiers' gains equal to one another.

In order to vary the feedback gain of each gain amplifier, recall that for a resistively loaded differential pair amplifier, the DC gain is given by[14]

$$|A_v| = R_L g_m = R_L \sqrt{2\mu_n C_{ox} \frac{W}{L} \frac{I_{tail}}{2}} \,. \tag{4.5}$$

Thus, in order to increase $|A_v|$ by some factor c, we can increase both the width W and tail current I_{tail} of the transistor by that same factor c:

$$R_L \sqrt{2\mu_n C_{ox} \frac{cW}{L} \frac{cI_{tail}}{2}} = cR_L \sqrt{2\mu_n C_{ox} \frac{W}{L} \frac{I_{tail}}{2}} = c\,|A_v| \tag{4.6}$$

Fig. 4.8 shows spectre simulations of this DC small-signal gain curves for increasing feedback gain (tallest curve has least gain), with the gain varied by varying feedback transistor width and tail current proportionally, as shown above. We note first the solid red curve (tallest), which has the least feedback; it has a smooth peak which falls sharply as input increases and the amplifier saturates. As feedback gain increases (going down: blue +, magenta square, etc. curves), several effects are observed: the gain decreases as expected from [8], thus we observe a lower peak and wider curve, as a larger input voltage is required to saturate the output.

As we increase the feedback further, a valley forms in this curve. The negative feedback effect can be intuitively understood. Consider the nonlinear gain curve of the forward system (appearing similar to the top curve of Fig. 4.8). If we open the loop and consider the output of the feedback amplifier, assuming it is ideally linear, then its output curve will be the inverse of the forward amplifier (scaled according to feedback gain). Feeding this back into the forward path flattens the curvature at small feedback gain, and starts to dip it further down and create a valley at higher feedback gain.

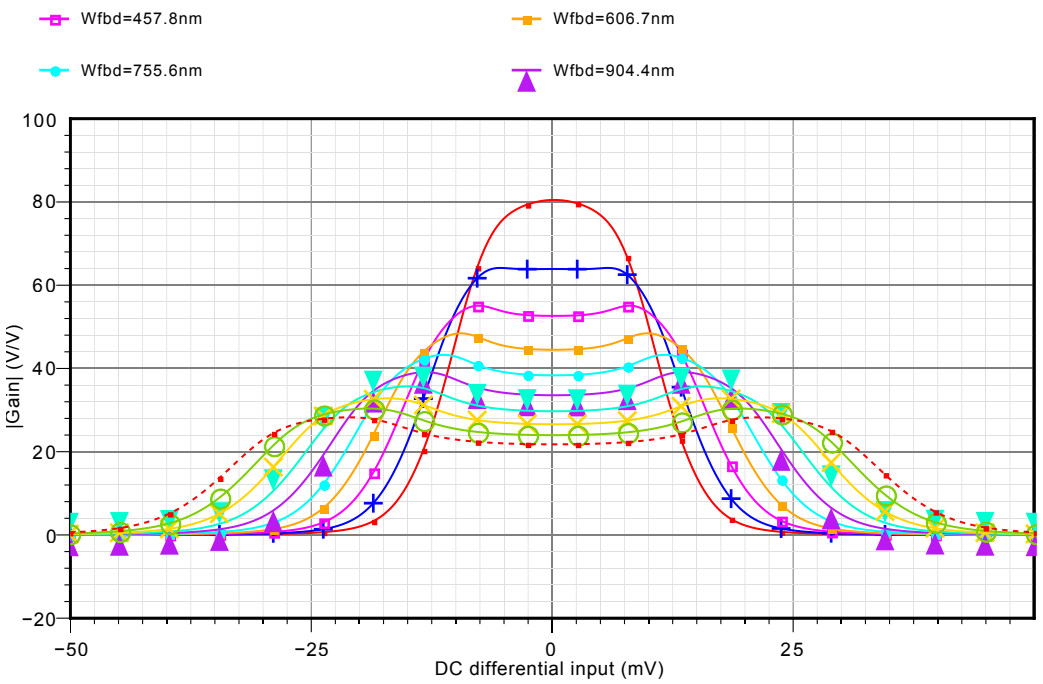


Figure 4.8: DC gain curves for increasing feedback gain, top to bottom. All three feedback gains are identical.

Similar behaviour is observed in the PA, compounded by the existence of multiple feedback loops, as shown in Fig. 4.9. For example, at the first stage output, we can clearly see a larger valley from the first feedback stage ($M_{p,n7}$ transistors), a hill from the interleaving feedback ($M_{p,n9}$ transistors) via the first feedback stage, and a further small valley from the last feedback stage ($M_{p,n8}$ transistors). The combination of these effects, with appropriate feedback gain, can optimise the PA's linearity significantly.

As a very simple linearity figure-of-merit, we will consider the percentage of DC gain variation from this curve, defined as

$$\text{gain variation} = \frac{\max A_v(V_{in}) - A_v(V_{in}=0)}{A_v(V_{in}=0)} \tag{4.7}$$

and further examine whether it corresponds to other measures, in particular intercept point at low frequency.

From Fig. 4.8, the feedback transistors with width of 308.9 nm has a nearly flat region. Thanks to its constant gain, this type of design minimises weak nonlinearity errors in DC applications. We also expect it to correspond to a minimisation of weak nonlinear distortion at low frequency, which we examine in the next section. Note that this concept of % gain variation and correspondence to low-frequency nonlinearity is reexamined in the final simulation results of the PA, in Section 4.4.5.

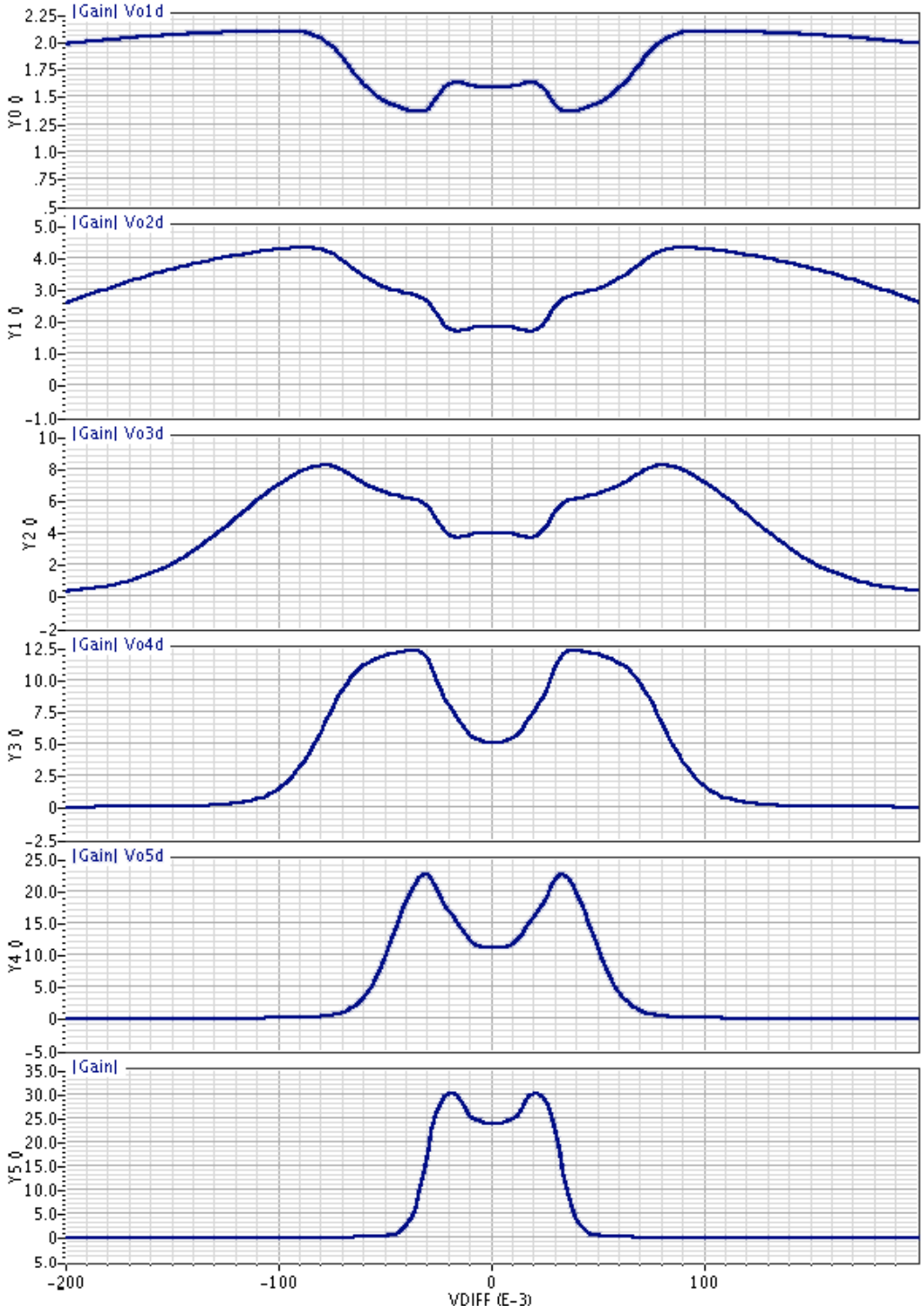


Figure 4.9: DC gain curves at the output of each forward amplifier of a PA design.

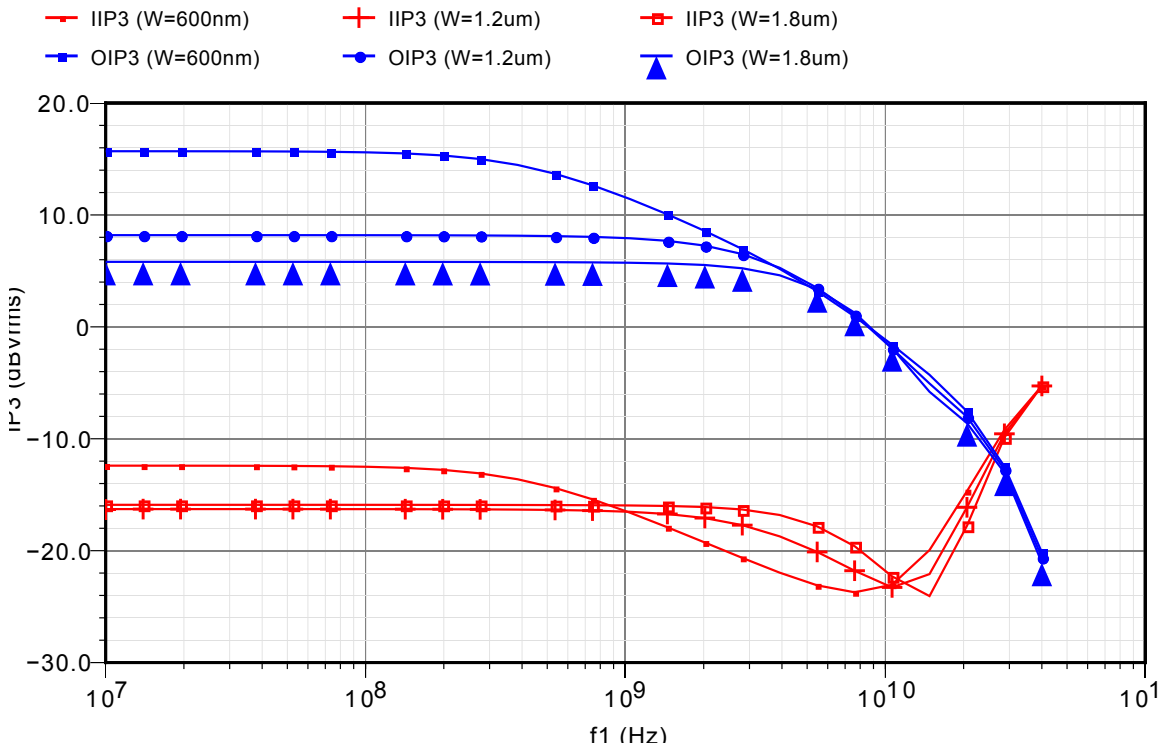


Figure 4.10: IP3 curves for increasing feedback gain, in dBV(rms). Top three curves: Output-referred IP3. Bottom three curves: Input-referred IP3.

4.4.3 RF linearity

For this PA design to be useful for RF/microwave applications, it is characterised in terms of third-order intercept point (IP3) with respect to input frequencies. To do so, a spectre PSS (periodic steady-state) simulation was performed on PAs with different feedback gains, similarly to the previous section. A two-tone test is performed with $f_2 - f_1 = 1\,\text{MHz}$ at an input of $-60\,\text{dBV(rms)}$ per tone, and the IIP3 and OIP3 are calculated from the simulation results.

Fig. 4.10 shows both the input- and output-referred IP3 for three different cases, all of them above the optimal feedback gain identified in the previous section ($W_{fbd} = 308.9\,\text{nm}$). Examining at the OIP3 values, we can very clearly see that, at low frequency, the linearity improves (OIP3 increases) as the feedback gain approaches that optimal value. However, the high-frequency OIP3 curve largely remains the same; this suggests that memory non-linearities (or frequency-dependent nonlinearities) are unaffected by the negative feedback, and eventually dominate the memoryless nonlinearities. It is possible to conclude that, for a given forward amplifier design, it is not possible to increase the IP3 at a given frequency beyond the value set by memory nonlinearities, and other considerations (e.g. transistor parameters) must be considered at this point.

Table 4.8: Effect of primary and interleaving feedback gain on performance

Parameter	Value		Comment
Gain	25.17	dB	
...change wrt primary FB	-2.8	dB/µm	400 nm to 600 nm
...change wrt interleaving FB	-1.2	dB/µm	3300 nm to 3500 nm
Bandwidth	6.80	GHz	
...change wrt primary FB	1.47	GHz/µm	400 nm to 600 nm
...change wrt interleaving FB	0.19	GHz/µm	3300 nm to 3500 nm
% gain variation	1.41	%	
...change wrt primary FB	12.37	%/µm	400 nm to 600 nm
...change wrt interleaving FB	0.595	%/µm	3300 nm to 3500 nm

4.4.4 Separately tuned feedback gains

We explored the possibility of setting the two types of feedback loops ("primary" feedback as part of the third-order stages of Fig. 2.9a; second type being the interleaving feedback) separately, instead of using equal gains. This is a departure from the original design in [8], where all feedback amplifiers are identical.

The following results, based on the final "unequal" feedback design of Section 4.4.5, which was designed to be reasonably optimal, demonstrate the behaviour. From that design, we varied the interleaving feedback gain by adjusting the $M_{p,n9}$ transistor widths by $\pm 100\,\text{nm}$ (and proportionally affecting the bias current) while keeping the primary feedback gain constant (transistors $M_{p,n7,8}$), and using the secant method, approximated the change in gain, bandwidth and % gain variation (from (4.7)) per micrometer of change in transistor width, which is proportional to the derivative with respect to feedback gain. (Recall that, per (4.6), transistor width in this situation is proportion to feedback gain).

Table 4.8 shows the results of this characterisation. We note firstly that the primary feedback has significantly more effort on gain, bandwidth and linearity (% gain variation) than the interleaving feedback. Suppose we are interested in the tradeoff between linearity and bandwidth. We find that, for the primary feedback adjustment, we have a ratio of $12.37\,\%/\mu\text{m}/1.47\,\text{GHz}/\mu\text{m} = 8.4\,\%/\text{GHz}$, whereas for the interleaving feedback adjustment, we have a ratio of $0.595\,\%/\mu\text{m}/0.19\,\text{GHz}/\mu\text{m} = 3.2\,\%/\text{GHz}$. Thus, in this local region, if we want to further extend bandwidth while minimising loss of linearity, an increase in interleaving feedback is preferred to the primary feedback.

Table 4.9: Design of post-amplifier

Par.	Forward (1–6)	Primary FB (7–8)	Inter. FB (9)	Units
Unequal feedback				
R_L	210	—	—	Ω
$W_{\text{n–p}}$	20.0	0.500	3.40	µm
$L_{\text{n–p}}$	120	120	120	nm
W_{tail}	165	4.00	27.2	µm
L_{tail}	480	480	480	nm
I_{SS}	3500	85	577	µA
g_m	11.64	0.270	1.93	µS
Equal feedback				
R_L	210	—	—	Ω
$W_{\text{n–p}}$	20.0	0.700	0.700	µm
$L_{\text{n–p}}$	120	120	120	nm
W_{tail}	165	5.60	5.60	µm
L_{tail}	480	480	480	nm
I_{SS}	3500	118	118	µA

4.4.5 Final design

Given the results of the investigations with unequal feedback gains, as demonstrated in Section 4.4.4, two separate PAs were designed, one with all 3 feedback gains equal, and one with them unequal as demonstrated in that section. The design values are given in Table 4.9. These circuits were designed with low-threshold-voltage transistors fixed to a 200 mV overdrive voltage, in order to achieve reasonably high baseline linearity with reasonable common-mode input range. All six forward amplifiers (circuit element subscripts 1–6 of Fig. 4.7) are identical. The primary feedback amplifiers (subscripts 7–8) are also identical between each other.

The forward amplifier stages (circuit element subscripts 1–6 of Fig. 4.7) were first designed, such that the overall gain of the 6 in cascade was around 35 dB to 40 dB (as the feedback would reduce this gain). Furthermore, the bandwidth of each stage, when loaded by an identical stage, was set somewhat above the target bandwidth by varying transistor sizes and load resistor value, given that it is possible to extend PA bandwidth up to the single-stage bandwidth easily using low values of feedback gain [8:Fig. 3a].

In order to design the unequal feedback variant, the primary feedback gain was selected to be slightly below the point of a fully flat DC gain curve. This follows from the prior results that the primary feedback more significantly degrades linearity for the same bandwidth

Table 4.10: Simulation results of post-amplifier designs

Parameter	Unequal	Equal	Units
Power	38.88	38.33	mW
Gain	25.17	28.34	dB
Peaking (AC)	0	0	dB
Bandwidth	6.80	6.39	GHz
Noise, out	4.67	6.36	mV(rms)
Noise, out, 1.0 GHz to 1.1 GHz	499	720	µV(rms)
% gain var	1.41	2.14	%
OIP3 10 MHz	17.25	22.67	dBV(rms)
OIP3 1 GHz	13.10	11.67	dBV(rms)
OIP3 at BW	3.02	2.24	dBV(rms)

extension, compared to the interleaving feedback. We then increase the interleaving feedback gain to obtain the desired bandwidth.

The equal feedback variant was then designed to the same bandwidth. It is thus possible to compare the two designs in order to evaluate the merit of the unequal feedback technique.

The schematic-level simulation results are given in Table 4.10 for both designs. Gain and bandwidth targets (Table 4.3) are both met.

The output noise in the 1.0 GHz to 1.1 GHz band is below the maximum 790 µVrms for both designs. The % gain variation is as defined at the end of Section 4.4.2.

The low-frequency OIP3 is better in the equal feedback case, while the % gain variation value is higher; we can conlude that this % gain variation value, while quick and convenient for sweep simulations, does not reliably correspond to weak nonlinearities, as it does not directly mesure the nonlinearity of the gain curve. Furthermore, this suggests that the unequal feedback technique may not provide significant advantages in linearity. Linearity at higher frequency is similar between the two designs, appearing to be limited by memory nonlinearities which are not addressed by this technique. Input-referred noise is approximately equal (note the difference in gain).

4.5 Offset compensation

The offset compensation filter is intended to compensate for any DC voltage offset that may occur at the output of the PA. In particular, it will compensate for transistor parameter mismatch (threshold voltage, etc.) and load resistor mismatch in the PA. DC from the TIA is not a concern, as the single-ended-to-differential converter of Section 4.3.2 will present any

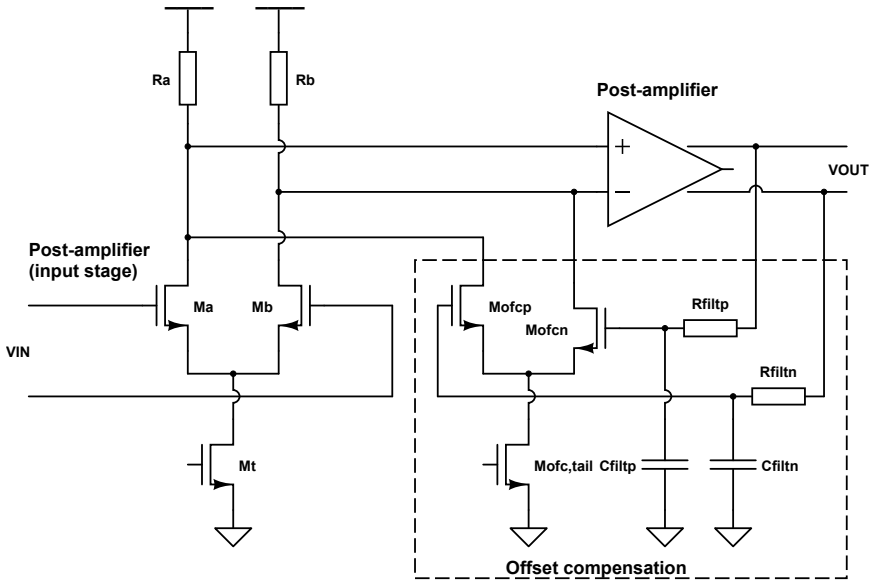


Figure 4.11: Schematic of the offset compensation, along with connections to the PA.

DC component as a common-mode voltage to the PA input, which will already be rejected at this stage.

The offset compensation is thus designed as a loop around the PA only, consisting of a low-pass filter and an amplifier, as shown in Fig. 4.11. The offset compensation works by first passing the PA's differential output through RC low-pass filters with a cutoff of around 1 MHz ($R_{filtn,p}$ and $C_{filtn,p}$). This isolates the differential DC signal at the output, which is amplified by the $M_{ofcn,p}$ transistors, and the loop is closed after the first PA forward path tranconductors ($M_{n,p1}$ transistors). Since this negative feedback loop operates only at low frequencies and DC, it does not interact significantly with the PA's signal feedback loops.

In order to analyse the offset compensation loop, assume we have some DC offset voltage reflected to the input. Then with the offset compensation, the closed-loop DC gain becomes

$$A_{dc,ofc} = \frac{A_v}{1 + \frac{g_{m,ofc}}{g_{m,fwd}} A_v} \tag{4.8}$$

where $A_{dc,ofc}$ is the closed-loop DC gain of the PA with compensation, A_v is the open-loop DC gain of the PA, $g_{m,fwd}$ is the transconductance of all forward amplifier transistors, and $g_{m,ofc}$ is the transconductance of the two offset compensation transistors. Given the standard deviation of the output offset voltage σ_{Vos} due to transistor mismatch, we can refer this value back to the input (σ_{Vos}/A_v) and then calculate the standard deviation of the closed-loop offset, given by

$$\sigma_{Vos,ofc} = \frac{\sigma_{Vos}}{1 + \frac{g_{m,ofc}}{g_{m,fwd}} A_v} \tag{4.9}$$

Table 4.11: Design parameters for offset compensation

Par.	Value		Comment
$W_{ofcp,n}$	6.80	µm	(equiv. - 2 parallel amplifiers)
$L_{ofcp,n}$	120	nm	
$W_{ofc,tail}$	54.4	µm	(equiv. - 2 parallel amplifiers)
$L_{ofc,tail}$	480	nm	
$g_{m,ofc}$	3.86	µS	
$R_{filtn,p}$	20	kΩ	
$C_{filtn,p}$	8.5	pF	

Table 4.12: Output offset voltage in Monte Carlo simulations ($n = 300$)

Case	μ (mV)	σ (mV)
Without offset comp.	5.58	101.0
With offset comp.	1.27	15.04

The maximum DC offset is specified as ±80 mV in Table 4.4. We will assume that DC offset due to random mismatch is normally distributed, and for the 3σ value to sufficiently define the maximum range of values. Then we have a target standard deviation $\sigma_{vos,ofc} = 27\,\text{mV}$. The unequal PA design was found to have $\sigma_{Vos} = 101.03\,\text{mV}$ (Monte Carlo simulation, $n = 300$), far in excess of the target. Given the unequal PA simulation results, specifically $g_{m,fwd}$ simulation value from Table 4.9 and PA gain from Table 4.10, we can calculate the necessary $g_{m,ofc}$ to meet the DC offset compensation target using Equation 4.9,

$$\begin{aligned} g_{m,ofc} &= \frac{g_{m,fwd}}{A_v}\left(\frac{\sigma_{Vos}}{\sigma_{Vos,ofc}} - 1\right) \\ &= \frac{11.64\,\mu\text{S}}{10^{25.17\,\text{dB}/20}}\left(\frac{101.0}{27} - 1\right) \\ &= 1.76\,\mu\text{S} \end{aligned}$$

To simplify layout work, we chose to use one of the differential amplifiers designed for the PA in Table 4.9. Two copies of the unequal feedback PA's interleaving feedback amplifier were paralleled to form the offset compensation amplifier. This provides a total transconductance of 3.86 µS, significantly above the 1.76 µS. (The single amplifier's transconductance was originally lower, but was adjusted to further optimise the PA, and this parallel offset compensation amplifier was retained through these design changes.)

Table 4.11 shows the final design values. Monte Carlo simulations ($n = 300$), with process variation and mismatch parameters considered in the models, were performed without and

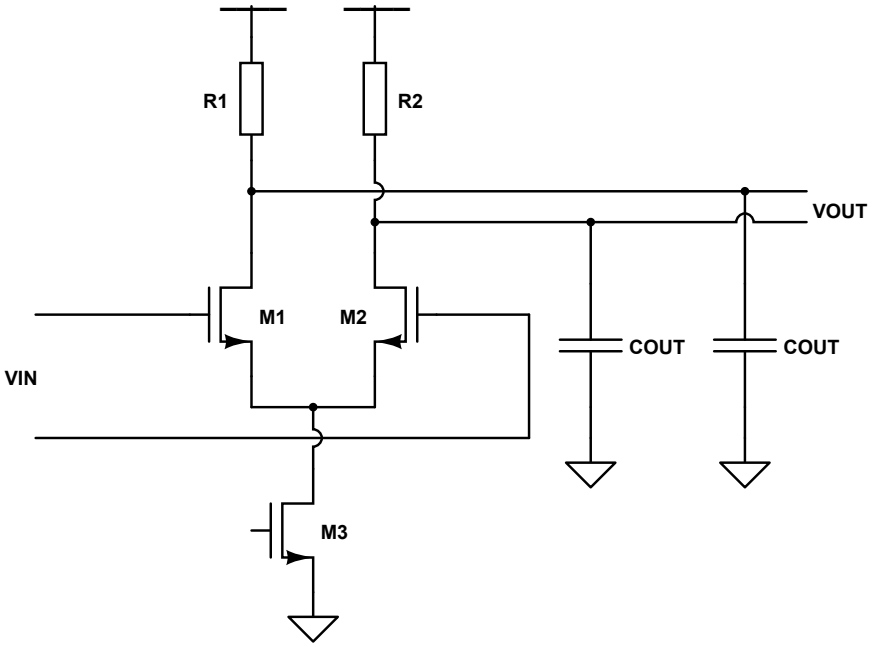


Figure 4.12: Schematic of the 50 Ω output driver.

with offset compensation to validate the design, as shown in Table 4.12. We find the σ_{Vos} value reduces to 15.04 mV, which is within 5% of the theoretical 14.40 mV obtained from 4.9 with $g_{m,pfc} = 3.86\,\mu S$.

We note briefly, in hindsight, that while this implementation was functional, a differential-mode filter would have allowed to obtain the same offset compensation performance in half the on-chip capacitor area. Specifically, the capacitors C_{filtp} and C_{filtn} to ground, shown in Fig. 4.11, could be replaced by a single capacitor of the same value as each individual capacitor.

4.6 Driver

The output driver is a simple differential pair, as shown in Fig. 4.12. In order to allow meaningful measurements with RF equipment, this driver is designed to drive two 50 Ω transmission lines off-chip, in order to provide the differential signal to off-chip equipment. In the course of design and in the simulation results below, an on-chip output capacitance C_{out} is set to 200 fF (pads, ESD, etc.), as defined originally in Table 4.1. The output line is modelled as a 50 Ω port, with a 10 MHz DC block in series. No further parasitics are modelled.

The design parameters for the driver are given in Table 4.13, with simulation results in Table 4.14. The 60 Ω resistive load is higher than the transmission line characteristic

Table 4.13: Design parameters of the output driver

Par.	Value	
$W_{1,2}$	40	µm
W_3	300	µm
I_{D3}	16.0	mA
L_{all}	120	nm
$R_{1,2}$	60	Ω
C_{out}	200	fF

Table 4.14: Simulation of the output driver

Par.	Value		Comment
Gain	-3.60	dB	
Bandwidth	33.74	GHz	without L1
Power	24.0	mW	
Return loss	24.3	dB	1 GHz
Noise out	260	µV(rms)	total
	13.4	µV(rms)	1.0 GHz to 1.1 GHz
DC gain var	0.548	%	200 mVpp input
IIP3	5.31	dBV(rms)	1 GHz
OIP3	1.71	dBV(rms)	1 GHz

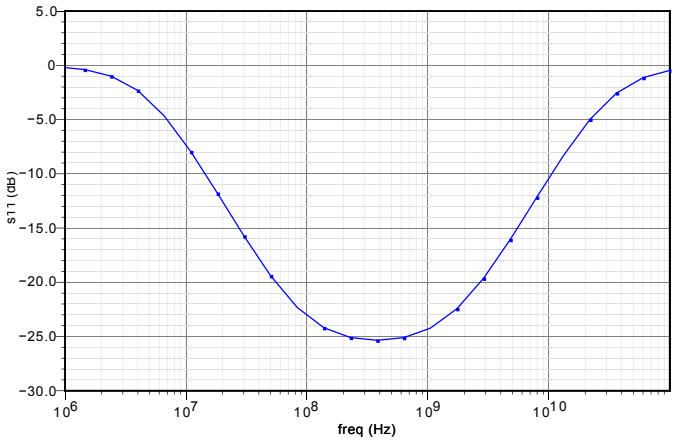


Figure 4.13: Return loss of the driver.

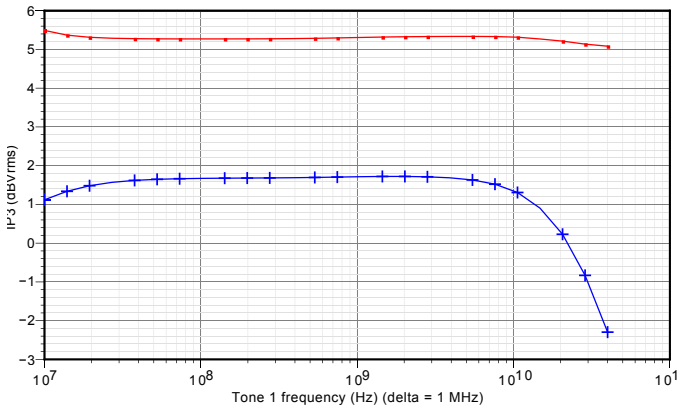


Figure 4.14: IP3 versus frequency of the driver. Top: Input-referred IP3. Bottom: Output-referred IP3.

impedance of 50 Ω in order to improve matching at higher frequencies, where this resistor is in parallel with the impedance of parasitic capacitances on-chip. The simulated return loss for this driver is shown in Fig. 4.13; it is below 15 dB in the range of 0.1 GHz to 5.0 GHz, with worse performance at low frequency due to the DC block and at high frequency due to the impedance of C_{out} and transistor capacitances.

Bandwidth is above 25 GHz, which is significantly above the system bandwidth and thus does not form a system bottleneck.

Obtaining a gain of approximately unity while still allowing sufficient output voltage swing in both directions was found to be challenging, given the constraint of a fixed 60 Ω resistive load. This is an expected limitation of small resistive loads for a differential amplifier, and a gain of −3.60 dB was deemed acceptable.

4.6.1 Linearity

From the initial driver design, which met the gain/bandwidth and line drive requirements, we attempted to improve the linearity by increasing the overdrive of the differential NMOS pair. The tail current source's overdrive was decreased in order to preserve the input common-mode minimum and ensure compatibility with the PA's output.

Fig. 4.14 shows simulated results for the driver's IP3 as a function of tone 1 frequency for a two-tone test (tone 2 being 1 MHz higher). The IP3 is very flat over the system's overall bandwidth, which simplifies calculations needed to remove the driver effect on linearity.

Nonetheless, the need for linearity optimisation of the output driver, despite its low gain, was underestimated for this design. At 1 GHz, the driver only achieves 5.31 dBV IIP3, in contrast to the PA's 13.1 dBV of OIP3 at the same frequency (i.e. both values are referred to the driver's input node). The driver nonlinearity dominates by 8 dB, limiting the ability

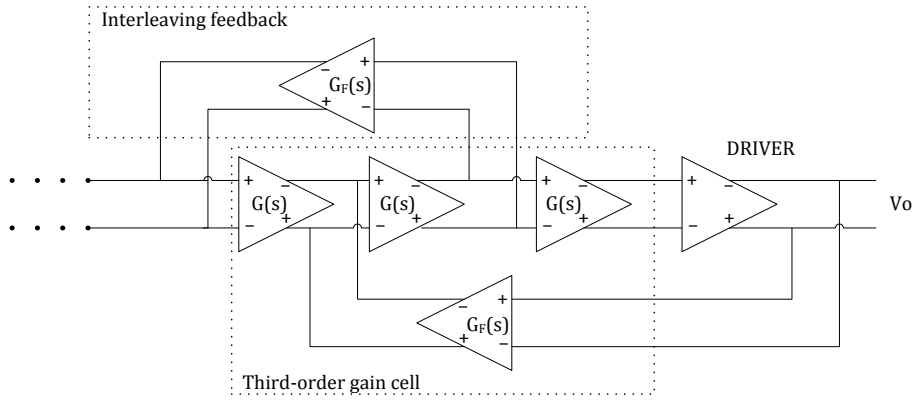


Figure 4.15: Inclusion of driver in a negative feedback loop.

Table 4.15: Comparison of PA with driver in open or closed loop

Par.	Open loop	Closed loop	Unit	Comment
Gain	23.8	24.1	dBΩ	
Bandwidth	7.70	7.62	GHz	
IIP3	-23.6	-24.5	dBV(rms)	1 GHz

to characterise the linearity of the system excluding the driver. Nonetheless, it is possible to attest whether the TIA-PA linearity exceeds that of the driver (i.e. if the driver appears to dominate the nonlinearity): in this case, the overall OIP3 will be close to the driver OIP3, while any TIA-PA linearity will degrade that value, as can be seen from (2.17). If the driver linearity is independently known and does not too strongly dominate, TIA-PA linearity can be calculated.

4.6.2 Linearity in a negative feedback loop

In the proposed design, the driver was connected open-loop, i.e., it was not included in any negative feedback loop. However, in high-linearity analogue applications, it is common to include a driver in a negative feedback loop (see e.g. many audio amplifiers, multi-stage op-amps in typical application).

Thus, we briefly explored this topology to improve the overall system linearity, inclusive of the driver. We first attempted to simply include the driver within the last feedback loop of the unequal-feedback PA, as shown in Fig. 4.15. The results of this attempt can be found in Table 4.15, which compares the performance of the PA and driver with the driver either outside and inside the loop. While we were expecting to see an improvement in input-referred linearity at the expense of gain from this simple change, given that all common-mode voltages

were compatible, we instead found that it slightly degraded linearity: IIP3 was reduced by about 1 dB. We also found a slight increase in gain, which is expected given the driver's sub-unity gain.

This is an unexpected outcome; however, due to time constraints from the chip tape-out deadline, this avenue was not pursued.

Further exploration of similar solutions, especially ones in which the PA is designed and linearity-optimised with an integrated driver stage, may provide even better linearity performance for applications that must drive a 50 Ω transmission line. Techniques such as source degeneration and other topologies for RF power amplifiers that exist in literature should also be considered, but were out of scope of the present work.

4.7 Chip-level considerations: I/O, testing, protection

This section covers some of the "boilerplate" chip-level considerations, such as input/output interfaces, ESD protection, and biasing. These elements are conventional and unrelated to the research goals, so their technical design is only briefly covered in this section. Furthermore, a datasheet-like manual for the fabricated chip is included in Appendix A, which shows the pad assignments and operation of the chip, along with preliminary simulation-based electrical characteristics.

Separate signal inputs are provided for the two circuits, with pads designed for a 100 µm-pitch GSGSG microwave probe or for wire-bonding. The differential output is common to all circuits, with a common pair 60 Ω loads to VDD, designed for a 80 µm-pitch GSSG microwave probe or wire-bonding. Furthermore, a copy of the output buffer is available for characterising it independently of the TIA-PA system, with a differential input with 80 µm-pitch GSSG pads, and the differential output also connected to the common output.

Several VDD and VSS supply pads are provided, internally connected, to ensure a low-impedance source, and are connected to all circuits on the chip. Amplifier bias currents are not generated on-chip but provided externally and distributed to the amplifiers via an NMOS current mirror. For each circuit, four bias current pins are provided, one each for the forward amplifiers, primary feedback amplifiers, interleaving and DC offset compensation amplifiers, and output driver (total of 8 bias current pins). This allows tuning of the interleaving feedback, permitting compensation of process variation and characterising the sensitivity of the high-linearity amplifiers to the feedback gains. Each bias current pin nominally expects 350 µA sunk into the pin, to be provided from a variable resistor connected to VDD or from a current source.

ESD protection consists of two pairs of clamp diodes, generated from p-cells provided

in the PDK, for each I/O pad. For all DC I/O pads, circuit and sizes used are according to the manufacturer's recommendations for HBM, MM and CDM protection, as provided in the technology documentation. For RF signal I/O, the minimum/RF ESD protection sizes are used instead. An RC-type clamp is used between VDD and VSS, also sized per recommended values.

4.8 Chip layout

Fig. 4.16 shows the full layout of the fabricated chip, with all pads and functional blocks in the layout labelled.

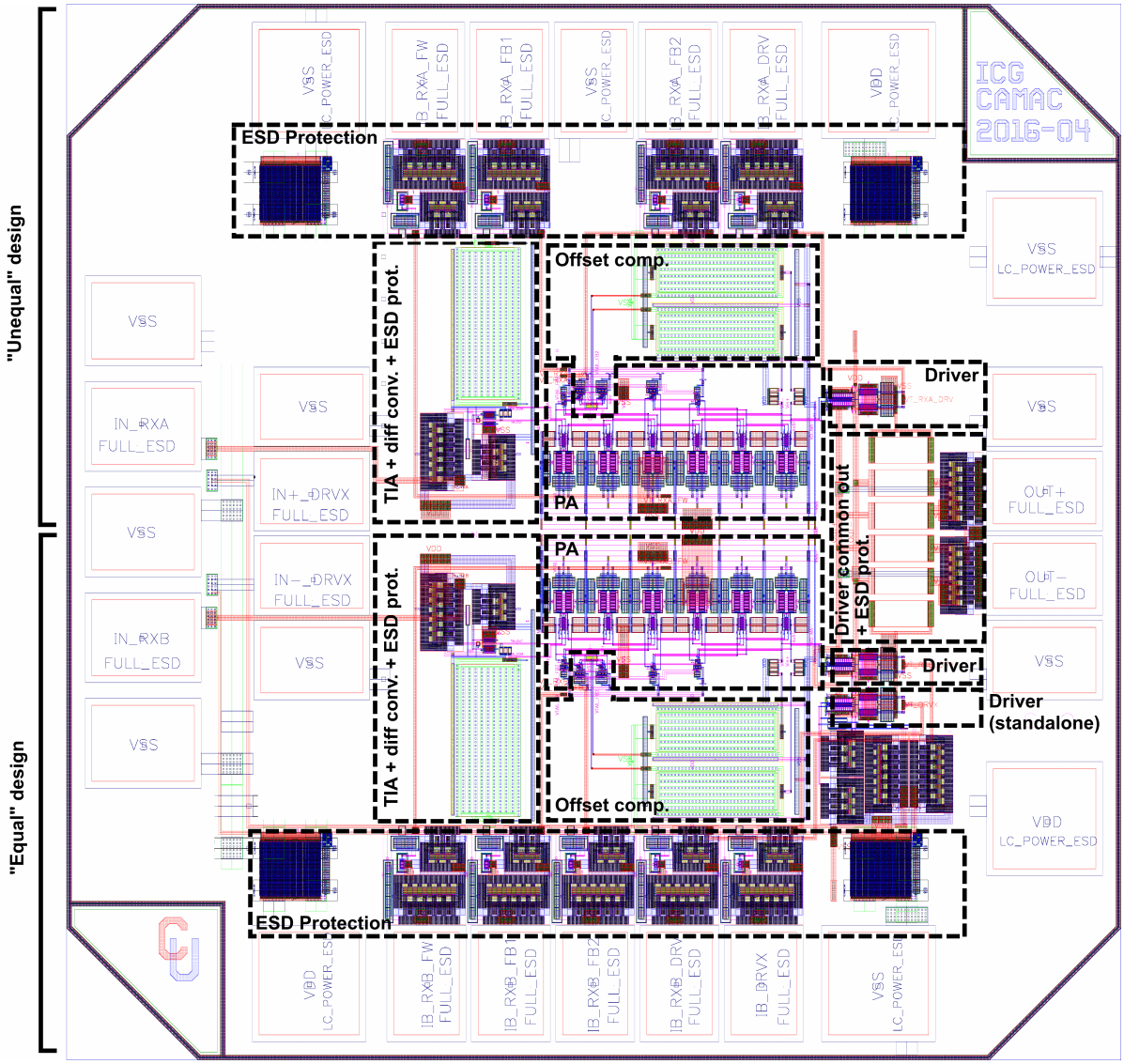


Figure 4.16: Layout of the fabricated chip.

Chapter 5

Simulation and measurement of the high-linearity receiver frontend

This chapter presents the overall system simulation and preliminary measurement results for the proposed design. We first discuss measurement considerations and the simulations that will be most useful for validating the fabricated devices to the models. The section that follows will then present simulation results for the overall system, with different measurement methods modelled (optical, electrical; single-ended/differential measurement of output). We will also provide simulation comparisons to relevant reference circuits without linearity optimisations in order to demonstrate the linearity improvements achieved by the proposed approach. Finally, we will compare key performance characteristics to other linear receiver designs in the literature.

5.1 Measurement considerations

Practical considerations of chip I/O and equipment access limit how the fabricated device can be characterised. As such, in order to validate the fabricated device's performance against the models, certain additional system simulations are useful.

The chip output is differential, intended to drive two separate $50\,\Omega$ transmission lines, which is standard for many RF cables and equipment I/O. However, three- or four-channel vector network analysers with a differential-mode feature, 5 GHz connectorised baluns, or other similar equipment may not be readily available. In this case, measurements may be made on a single-ended output, with the other output signal terminated with $50\,\Omega$ off-chip. Thus, we have characterised the single-ended output signals in these simulations alongside the differential, and validated that the values are as expected.

The device input is designed for a photodiode current. Initial validation of the device

Table 5.1: Full chip simulation results

Par.	Unequal	Equal	Unit	Comment
Gain	70.04	71.33	dBΩ	
Bandwidth	6.97	6.27	GHz	
Peaking	None	None	dB	
Min. freq.	7.9	8.1	MHz	
DC current	47.26	47.15	mA	amplifier bias + current steering
Power	70.89	70.73	mW	DC amplifier bias + current steering
Noise out	6.58	7.48	mV(rms)	total
	635	737	µV(rms)	1.0 GHz to 1.1 GHz
OIP3	0.71	0.08	dBV(rms)	100 MHz.
	0.72	-2.71	dBV(rms)	1 GHz
	-5.40	-5.57	dBV(rms)	10 GHz

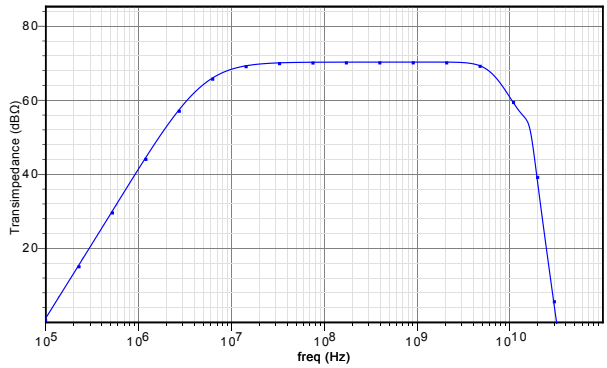
alone, however, can be performed electrically prior to integration testing with a photodiode and optical input. Conveniently, the TIA design has a DC input impedance of approximately 50 Ω, which is appropriate to a standard 50 Ω RF signal source. S-parameter simulations were thus performed for a 50 Ω input source to correlate results.

5.2 Schematic simulations

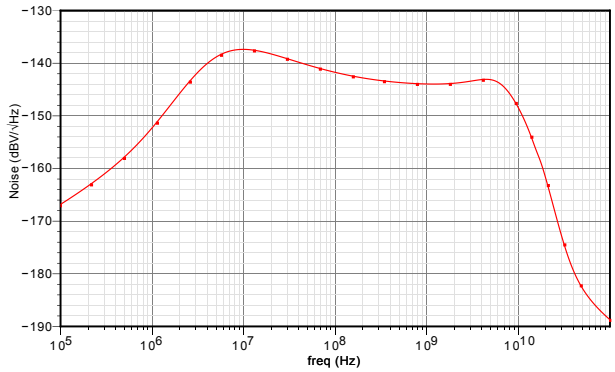
The following simulations were performed using schematic simulation of the system. This includes parasitic elements available in the device models, as well as the estimated pad and ESD diode capacitances from Chapter 4.2 (included as ideal capacitors), but notably does not include wiring capacitances.

Most simulations were carried out with an input current of 17.0 µA (rms), or an equivalent −48.38 dBm for electrical simulations with a 50 Ω port source. This yields a differential output at the maximum specified of 200 mVpp. For IP3 measurements, at each frequency point, a 3-point input sweep from approximately 1.26 µA to 40.0 µA (rms) is performed to calculate the IP3.

Table 5.1 shows the simulation results, with plots for the AC, output noise spectrum, and IP3 vs. frequency given in Fig. 5.1 (unequal) and 5.2 (equal). Simulations were performed with a wirebonded photodiode model input, as used in the TIA simulations. It is important to note that bandwidth may be affected (extended) by the inductive peaking effect of the bondwire inductance between the photodiode and TIA; variation in system bandwidth, parasitic capacitances and bondwire inductance may alter the measured bandwidth.



(a)



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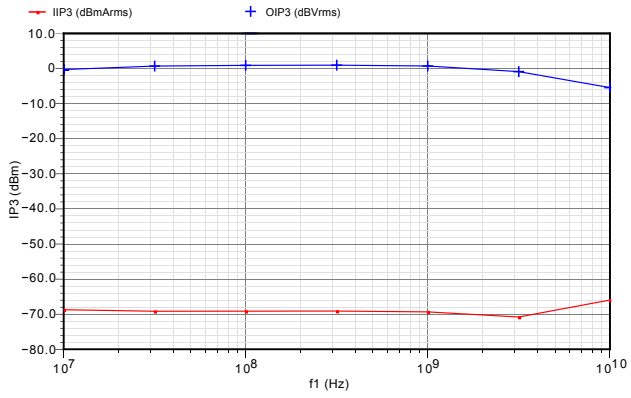
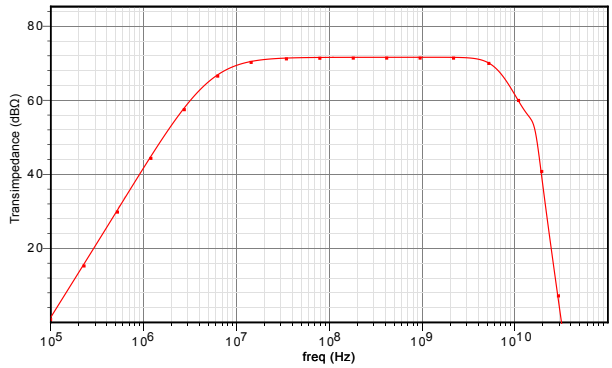
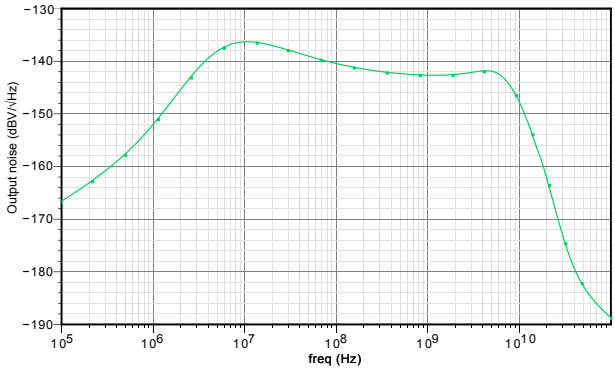


(c)

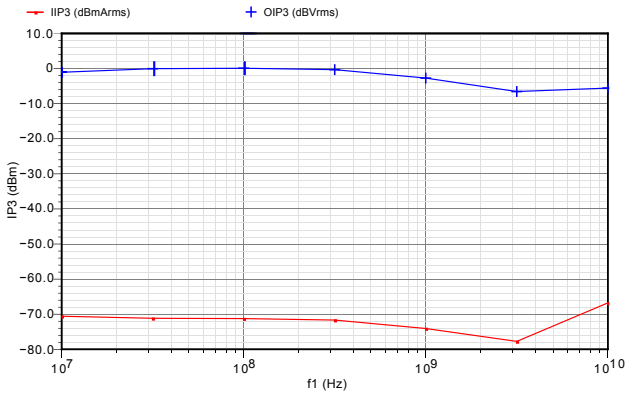
Figure 5.1: "Unequal" circuit full-chip simulation. a) AC response; b) Output noise spectrum; c) IP3.



(a)



(b)



(c)

Figure 5.2: "Equal" circuit full-chip simulation. a) AC response; b) Output noise spectrum; c) IP3.

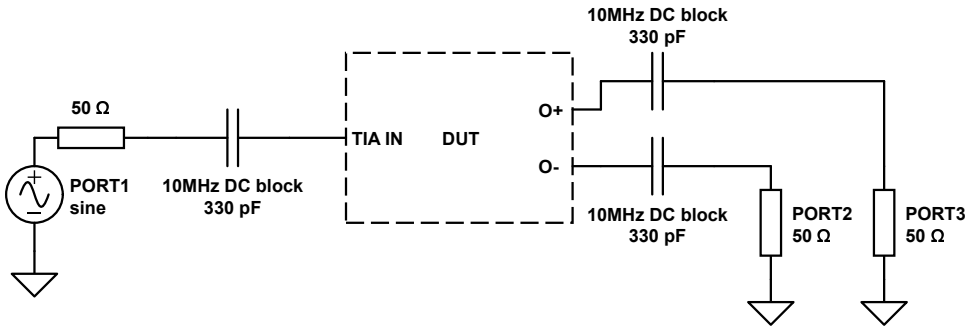


Figure 5.3: Electrical simulation model.

Results mostly correspond to the PA simulation results. The two designs perform very similarly. The low-frequency OIP3 are roughly equal (limited by the driver); we do not see the equal design's significant improvement in linearity. The unequal circuit marginally outperforms the equal circuit in high-frequency OIP3 and bandwidth. Noise performance is nearly identical (when input-referred; note the gain difference).

In the electrical test configuration, the gain's numerical value is expected to reduce by about 34 dB, due to a change of units from the input stimulus from current to power (dBm at $Z_o = 50\,\Omega$). This can be derived knowing that, with a current input, the transimpedance gain is

$$G_{(dB\Omega)} = 20\log\frac{V_{out}}{I_{in}} = 20\log V_{out} - 20\log I_{in}\ . \tag{5.1}$$

Given the power relationships to voltage and current,

$$\begin{aligned} P_{out(W)} = V_{out}^2/R \quad &\rightarrow \quad 10\log P_{out(W)} = 20\log V_{out} - 10\log R \quad \text{and} \\ P_{in(W)} = I_{in}^2 R \quad &\rightarrow \quad 10\log P_{in(W)} = 20\log I_{in} + 10\log R \quad , \end{aligned}$$

we can substitute into (5.1) to obtain the relationship between the gains in these two measurement scenarios,

$$G_{(dB\Omega)} = G_{(dB,RF)} + 20\log R \tag{5.2}$$

where $G_{(dB\Omega)}$ is the transimpedance gain (photodiode current input), $G_{(dB,RF)} = 10\log P_{out} - 10\log P_{in}$ is the RF gain, and $R = 50\,\Omega$ is the RF characteristic impedance of the I/O ports and transmission lines. Substituting R, we see that the transimpedance gain is numerically $20\log 50 \approx 34$ dB higher than the electrical gain.

The bandwidth is expected to decrease, as the system will not benefit from bandwidth extension provided by bondwire inductive peaking when directly probed. IIP3 is not expected to change significantly (OIP3 may change due to change in gain vs. frequency).

In order to validate the expected values in a measurement context, simulations of the

Table 5.2: S-parameter (electrical) simulations of unequal-feedback design

Par.	Diff out	1-ended out	Unit	Comment
R_{in}		48.7	Ω	DC $\partial V/\partial I$ at 0V bias.
s_{11}		-42.2	dB	Minimum at 794 MHz.
		-7.2	dB	Maximum in-band at 10 MHz.
s_{22}		-27.0	dB	Minimum at 316 MHz.
		-7.2	dB	Maximum in-band at 10 MHz.
s_{21} gain	36.08	30.06	dB	In-band. Difference −6 dB
s_{21} BW	4.73	4.73	GHz	No difference.
OIP3	-0.06	-6.06	dBV(rms)	100 MHz. 1-ended follows gain.
	-0.95	-7.01	dBV(rms)	1 GHz
	-5.43	-11.4	dBV(rms)	10 GHz

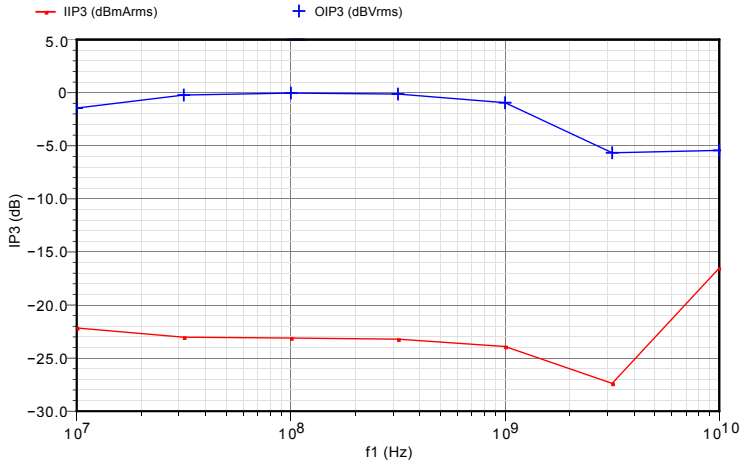


Figure 5.4: Electrical testing simulation IP3 versus frequency. $\Delta f = 1\,\text{MHz}$.

unequal-feedback design are shown in Table 5.2. These simulations were performed using simplified models of the expected electrical test environment, as shown in Fig. 5.3.

The comments column remarks on the observed differences between the differential and single-ended output measurements; these differences are as expected from theory.

The gain is as predicted from (5.2) (when $R = 50\,\Omega$), and bandwidth is reduced due to the removal of bandwidth extension from the bondwire inductance. The IP3, shown with respect to frequency in Fig. 5.4, is slightly lower than expected (but within 2 dB).

Having identified the relationships, expected measurement results and potential deviations between these measurement cases, it is possible to measure the fabricated chips with available equipment and validate its performance against simulation models.

Table 5.3: Post-layout full chip simulation results

Par.	Unequal	Equal	Unit	Comment
Gain	69.42	70.7	dBΩ	
Bandwidth	3.56	3.50	GHz	
Peaking	None	None	dB	
Min. freq.	7.6	7.2	MHz	
DC current	45.77	45.65	mA	amplifier bias + current steering
Power	68.66	69.48	mW	DC amplifier bias + current steering
Noise out	4.69	5.29	mV(rms)	total
	601	697	µV(rms)	1.0 GHz to 1.1 GHz
OIP3	0.66	-0.05	dBV(rms)	100 MHz.
	0.03	-0.59	dBV(rms)	1 GHz
	-11.5	-11.3	dBV(rms)	10 GHz

5.3 Post-layout extracted simulations

The results of full-chip post-layout simulation are shown in Table 5.3, with AC and IP3 figures for the unequal and equal circuits in Fig. 5.5 and 5.6, respectively.

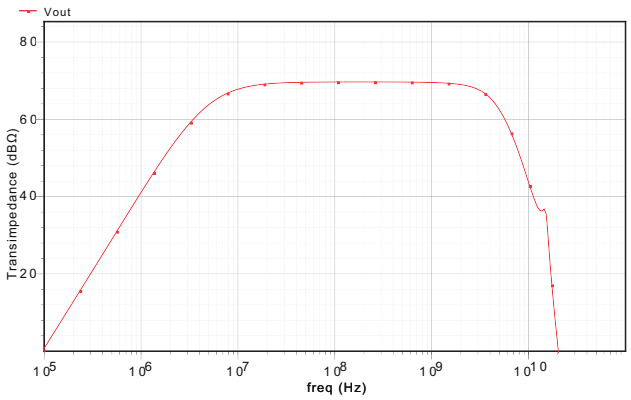
The results largely align with the full chip schematic-level simulation results, with the expected exception that bandwidth is reduced due to parasitic capacitances. Two other differences are notable: output noise appears to have decreased, following both a decrease in gain and the decrease in bandwidth (for total noise), and OIP3, while similar at low frequency, appears to drop off much more quickly at high frequency in post-layout (see 10 GHz values).

5.4 Post-amplifier linearity enhancement: comparisons

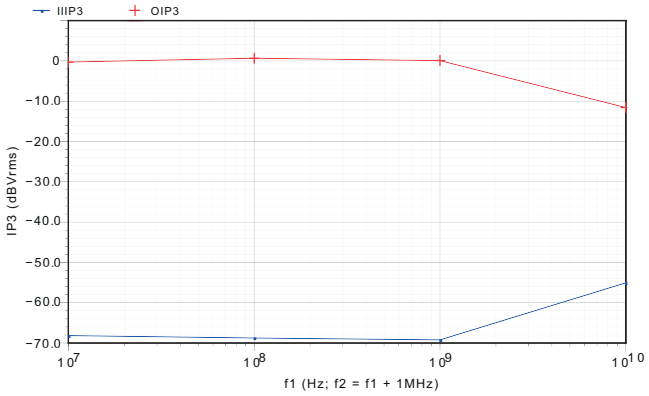
In this section, we will refocus on our PA design's linearity, in order to provide a comparison to relevant reference circuits that demonstrate the achieved improvements. Furthermore, we will consider a different metric, the total harmonic distortion (THD), which is relevant to compare this design to some designs found in literature in Section 5.6.

We will compare our equal feedback design ("equal", as shown in Fig. 2.9a) to two reference designs:

1. The "reference" design consists of the same PA forward path with no feedback paths at all.

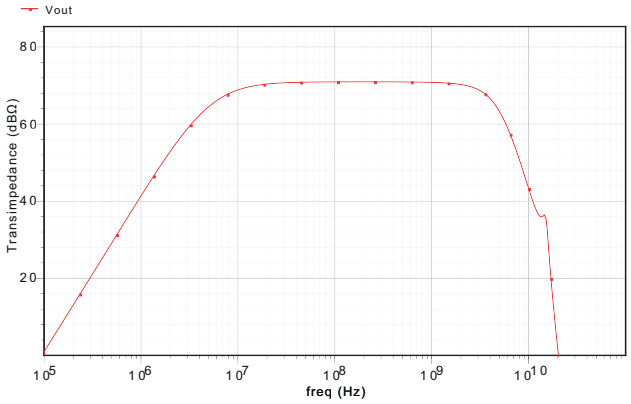


(a)

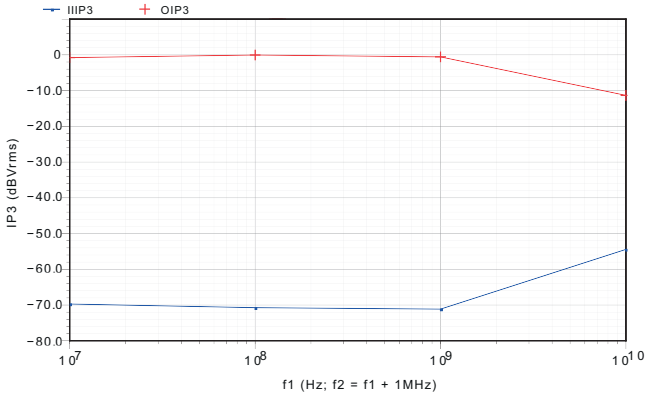


(b)

Figure 5.5: "Unequal" circuit post-layout simulation. a) AC response; b) IP3.



(a)



(b)

Figure 5.6: "Equal" circuit post-layout simulation. a) AC response; b) IP3.

2. The "equivalent" design has the same forward path as "equal" and removes the interleaving feedback, as shown in Fig. 2.9b. The two feedback amplifiers are set to gains 2.62 and 0.38 times that of the equal feedback design, respectively, as shown in Fig. 2.9b; this theoretically achieves the same transfer function, and thus same gain and bandwidth, as the equal feedback design, though the differences in loop gains and feedback paths are expected to change circuit linearity (see Section 2.6.2).

Comparison to these reference circuits allows a demonstration of how the addition of feedback and interleaving feedback have achieved linearity improvement.

All three PA designs are adjusted to equal gain ($(74.8 \pm 0.1)\,\mathrm{dB}$) by adjusting the load resistors equally, and they are simulated with the same TIA designed earlier and no output buffer. With these two reference circuits, we aim to show linearity optimisation relative to a simple amplifier cascade and specifically benefits of interleaving feedback over simple negative feedback at each third-order stage.

The basic performance parameters of all three circuits are given in Table 5.4. We can make a few observations on these amplifiers' performance. First, adding interleaving negative feedback to the reference has provided a 43% GBW extension, though we were not optimising for bandwidth as in [8]. The equivalent design, contrary to theory, shows a slightly lower bandwidth at 90% of the "equal" circuit. The proposed "equal" design has slightly higher integrated noise than the reference, but performs better in terms of average noise density, considering the bandwidth extnesion.

Table 5.5 shows the linearity performance of these three circuits, from both an IP3 and THD perspective. As previously, we also compare a low-frequency and 1 GHz measurement to attest for the effect of memory nonlinearities. From the IP3, we see that the equal design performs significantly better (over 12 dB) at low frequency. At 1 GHz, the linearity of all three circuits are much closer, as expected from previous results. It is noteworthy that the equivalent circuit, despite negative feedback, has a worse linearity than the reference circuit at this frequency.

The THD values were calculated from the first 7 harmonics, with output set to 200 mVpp and 500 mVpp. The THD simulation at low frequency show very high (sub-0.2%) linearity up to 500 mVpp output. The equal design shows the best performance, with clear reduction in THD from the reference and a more modest improvement from the equivalent design. The THD of all three designs is plotted in greater detail in Fig. 5.7a.

At 1 GHz, we see the effect of memory nonlinearities: THD has degraded overall, and while the equal design is still the most linear, the equivalent design is almost as linear. Detailed results are plotted in Fig. 5.7b.

Table 5.4: Comparison of frontend designs

Param.	Equal	Ref.	Equiv.	Units
Gain	74.84	74.83	74.77	dB
Bandwidth	6.94	4.86	6.25	GHz
Noise [a]	9.71	9.53	9.81	mVrms
Noise density [b]	117	137	124	nVrms/$\sqrt{\text{Hz}}$

[a] Output referred, integrated over all frequencies.

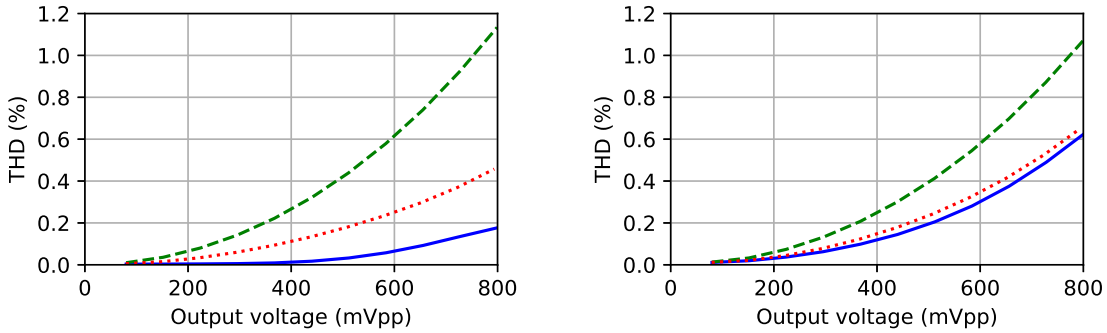
[b] Average: $\overline{v_{n,\text{out}}}/\sqrt{\text{BW}}$

Table 5.5: Linearity of optical frontend designs

Parameter	Equal	Ref.	Equiv.	Units
OIP3 50 MHz	18.7	4.03	6.40	dBV(rms)
OIP3 1 GHz	1.78	0.72	-0.41	dBV(rms)
THD 50 MHz [a]	0.004	0.066	0.028	%
THD 1 GHz [a]	0.031	0.060	0.037	%
THD 50 MHz [b]	0.030	0.421	0.174	%
THD 1 GHz [b]	0.195	0.395	0.235	%

[a] 200 mVpp output (−10 dBm).

[b] 500 mVpp output.



(a) (b)

Figure 5.7: Total harmonic distortion of frontend designs vs. output voltage. Dash green: "reference". Solid blue: "equal". Dotted orange: "equivalent". a) At 50 MHz; b) At 1 GHz.

5.5 Fabricated chip measurements

This section presents the preliminary measurement results for the two fabricated circuits. All measurements were conducted electrically, with 50 Ω sources and transmission lines at RF signal I/O ports. Signal measurements were all single-ended, with the second port of the differential pair connected to a DC block followed by a 50 Ω termination, as shown in Fig. 5.8a.

Two-tone tests for IP3 measurements were conducted using two signal generators and a Mini-Circuits ZN2PD2-14W-S+ power splitter/combiner to superpose the signals, as shown in Fig. 5.8b; this power combiner's response was calibrated out of the measured results. The two tones were fixed at 100 MHz apart.

An error in the measurement setup was not originally detected when these measurements were conducted: the bias current for the output driver may have been incorrect, and may have varied between circuit measurements, due to an error in current mirror ratios in the layout. Only the driver bias current is affected by this error. Therefore, these measurements are considered preliminary.

Optical measurements have not yet been conducted.

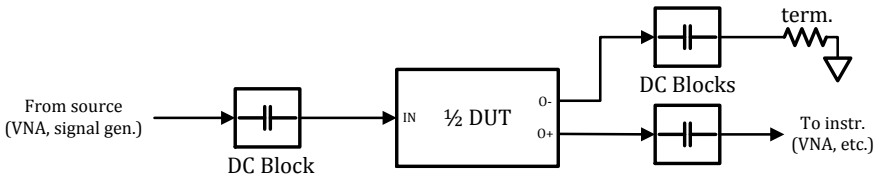
Table 5.6 shows the summarised test results, with s-parameter sweeps and OIP3 shown in Fig. 5.9, 5.10 and 5.11. Gain is as expected for electrical measurements; however, significant high-frequency peaks are observed in the "unequal" circuit. These were found to vary between two tested chips and from probe landing to probe landing. Bandwidth was, contrary to simulations, higher in the "equal" circuit, but this conclusion may be muddied by the observed peaking.

Low-frequency OIP3 is around 3 dB less than expected (but measured at a higher frequency than simulations, at 550 MHz), and degrades more with frequency than expected from simulations. Significant variation over frequency raises some doubts over the accuracy of these results, potentially due to calibration or other measurement setup issues with the two-tone test.

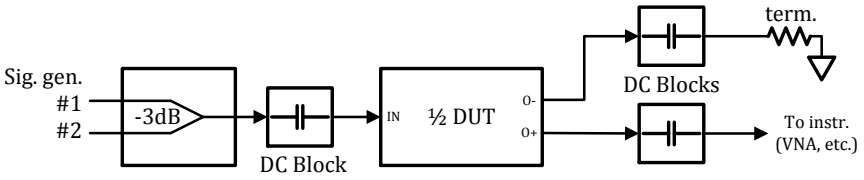
5.6 Comparison to designs in literature

Table 5.7 compares the "equal" design (post-layout simulation results) proposed in this work to a selection of other receiver designs in the literature, for various applications. The results in this table, where relevant, are taken from simulation results at 1.0 GHz to 1.1 GHz.

The proposed design performs very favourably in THD, with similar noise performance, relative to [26] and [25]. This is achieved in a smaller area than the latter design, and is



(a)



(b)

Figure 5.8: General test configurations for RF measurements. a) Single-tone measurements. b) Two-tone measurements.

Table 5.6: Electrical chip measurements

Parameter	Equal	Unequal	Unit	Comment
DC current	51	49	mA	
Bias current	350	350	µA	±1, nom. all bias pins
Common mode out	0.977	0.969	V	
Diff. offset out	-0.022	-0.066	V	
Gain, passb.	31.5	28.6	dBΩ	electrical, 80 MHz
Peaking	0	6.44	dB	
$f_{3\,\mathrm{dB,lower}}$	7.47	4.54	MHz	
BW	2.72	1.99	GHz	
OIP3	-2.8	-2.8	dBVrms	550 MHz
	-6.7	-8.1	dBVrms	1.2 GHz
$s_{11,\mathrm{max}}$	-14.26	-12.01	dB	0.1 GHz to 1 GHz
	-1.59	-3.98	dB	1 GHz to BW
$s_{22,\mathrm{max}}$	-1.37	10.07	dB	

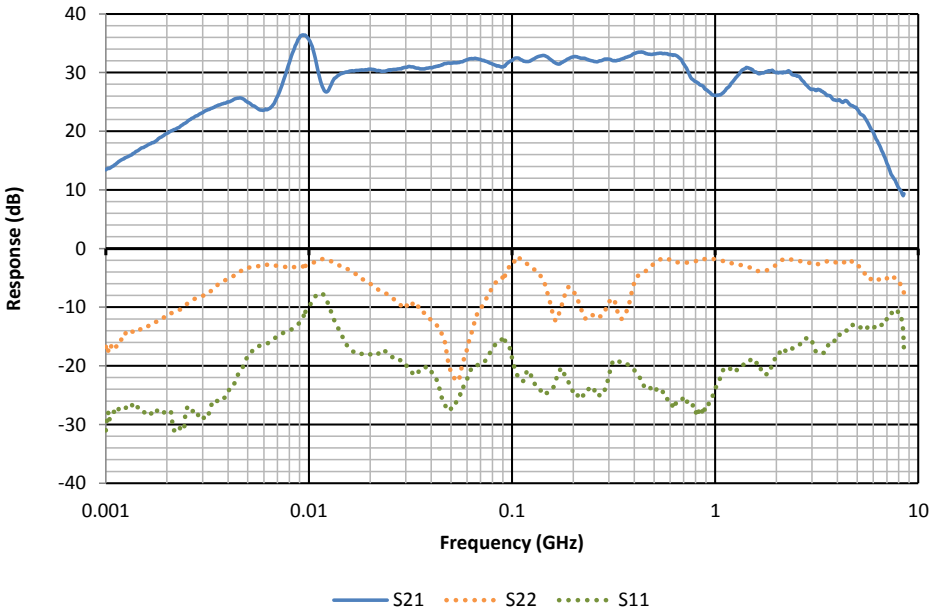


Figure 5.9: s-parameter measurements of "equal" circuit. Input = −44 dBm.

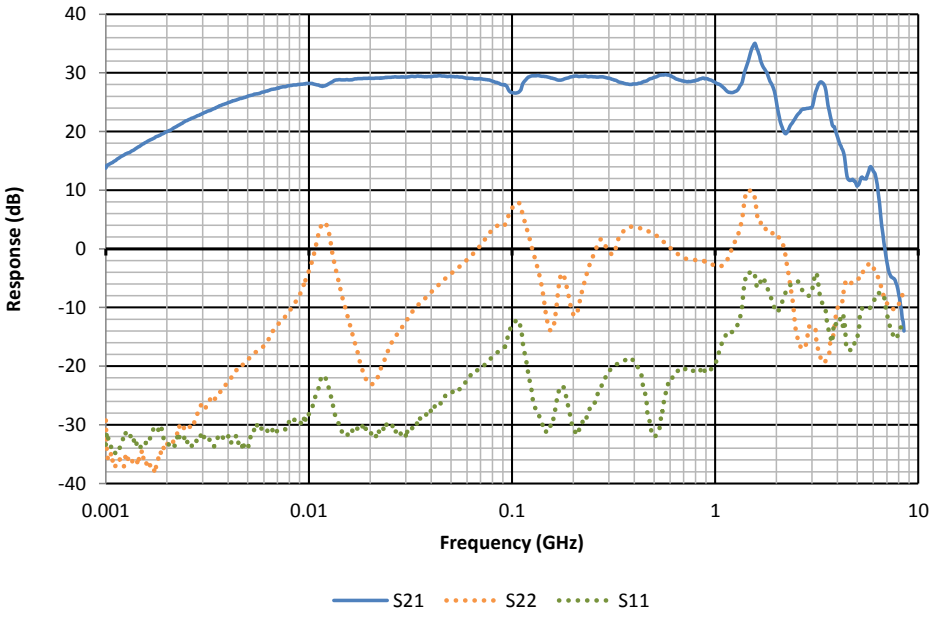


Figure 5.10: s-parameter measurements of "unequal" circuit. Input = −44 dBm.

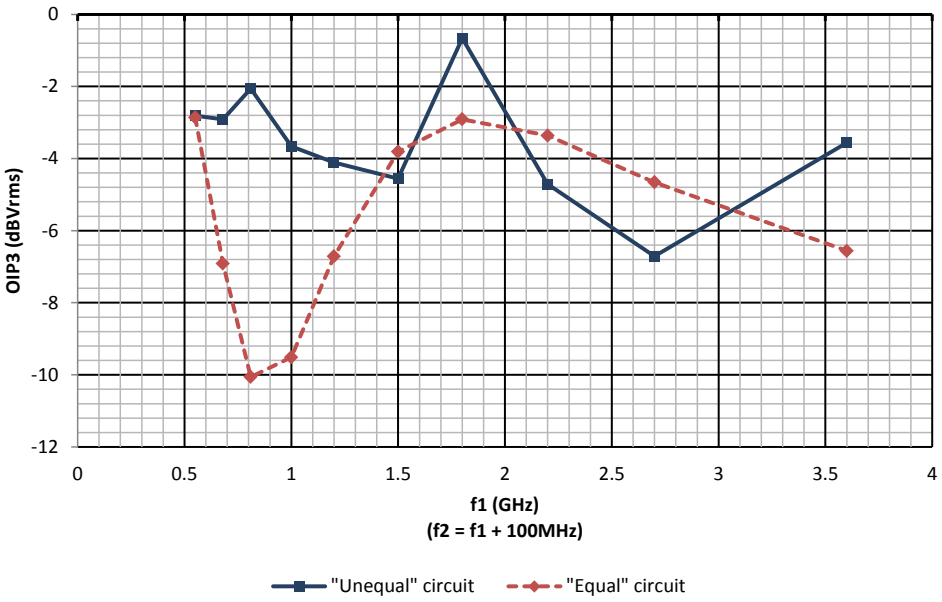


Figure 5.11: Measured OIP3

Table 5.7: Performance comparison

Parameter		unit	This work	[26]	[24]	[25]
Technology			0.13 µm CMOS	0.13 µm SiGe	0.18 µm CMOS	0.18 µm CMOS
Application			PAM, QAM, QPSK, etc.	34 GBaud DP-16QAM	radio-over-fibre, 5.2 GHz	20 Gb/s PAM-4
Topology			diff., w/input 1-ended	fully differential	LNA (cascode + com. source)	diff. RGC TIA + diff cascode MA
Inductors?			no	yes	yes	no
Gain	A_0	dBΩ	70.7	73.0	58.6	51.7
BW	$\omega_{-3\,\mathrm{dB}}$	GHz	3.50	27	4.6 – 7.4	7.3
IRN	$S_{i,in}$	pA/$\sqrt{\mathrm{Hz}}$	20.3	20	6.875	23.6
IIP3		dBm	−26.2	–	> 5	–
THD		%	0.195	1.5	–	< 2%
@ V_{OUT}		mVpp	500	500	–	≈ 130
Power/ch.	P	mW	68.48	313	n/a	37.8
Area/ch.	A	mm^2	0.15	1.12	n/a	0.31

between these two designs on power dissipation.

The proposed design does not compete with the LNA-style narrowband design of [24] in either IIP3 or noise performance. Nonetheless, as a wideband design, the proposed receiver is more versatile, capable of receiving baseband modulation like PAM, and avoids the use of on-chip inductors (area) and the need for impedance matching (design complexity) which is featured in the LNA-style design.

Chapter 6

Conclusion

The increasing demand in data throughput via optical communications and development of new applications for optical links continues to push the boundaries of circuit design for optics. In the course of this work, we have proposed multiple tuned-feedback design approaches to address two challenges: dynamic response in a bandwidth-extended design, and linearity optimisation for emerging applications such as radio-over-fibre.

In Chapter 2, we overviewed the theory and literature that forms the foundation of this work.

In Chapter 3, we investigated improvements to dynamic response of an optical receiving when using positive feedback for bandwidth extension. In particular, we proposed that using separate feedback gains would allow optimisation of the dynamic response compared to the prior approach of using identical feedback on each post-amplifier stage. Compared to a design using this prior approach, we demonstrated a 7.7% eye opening improvement via a brute-force simulation search of the design space.

Furthermore, we presented a root-locus analysis in order to understand the effect of tuning separate feedback gains on the dynamic response. A preliminary root-locus analysis of the prior all-equal feedback approach yielded an initial interpretation that corresponded to the prior understanding of the peaking behaviour of this technique; a root-locus analysis as each feedback gain is independently varied further provided insight into the different effect of each gain, providing design guidance for this approach. In this way, we have shown the usefulness of root-locus analysis to optimising dynamic response of amplifiers.

In Chapter 4, we turned our attention to linearity optimisation, which has not been previously examined for optical receiver frontends in the literature, to our awareness. We proposed that an interleaving-feedback PA topology, originally for bandwith enhancement, could be repurposed to optimise linearity, and we developed an approach to tuning the feedback to do so. We found that proper selection of the feedback values in the PA could improve

IP3 by over 14 dB in simulation at low frequency, but that memory nonlinearities limit the maximum possible optimisation as frequency increases. We designed two optical receiver frontends using slightly different approaches, fabricated in 130 nm CMOS, to demonstrate the proposed technique.

In Chapter 5, we simulated the chip designed in the previous chapter to confirm overall results, achieving 0.08 dBVrms OIP3 (quasi-static) and a THD of 0.195% (1 GHz). We concluded, in particular, that the RF output driver is a key limiting factor in our designed chip when it comes to linearity optimisation. Nonetheless, through simulation we establish the linearity benefits both relative to non-optimised reference circuits and to optical receiver frontends reported in literature. The proposed circuits compare favourably to other wideband receiver designs.

6.1 Further work

A number of avenues for further investigation were identified in the course of this work:

1. Development of a robust, systematic design methodology should be investigated based on the design guidelines presented in Chapter 3's root-locus analysis.

2. Further study of amplifier dynamics from a pole-zero/root-locus perspective: an exploration of how to "design" an amplifier's dynamic response, possibly by relating the root positions to the pole-zero plot of well-behaved filters (e.g. Bessel, Gaussian) or control system theory.

3. Linearity optimisation at a transistor level. This work's linearity focus was primarily on a topology level, and did not consider how transistor linearity could be improved (i.e. via overdrive voltage, sizing).

4. Linearity optimisation of an RF output driver. This would be important to the measurement of the proposed linearisation technique, and may be useful to applications where the output of the frontend is driven off-chip (e.g. to an off-chip analog-to-digital converter). This could include more linear driver topologies (e.g. source degeneration, local negative feedback), or alternative PA designs or architectures capable of directly driving a 50 Ω transmission line (e.g. tapered forward path).

5. A greater exploration of LNAs, in particular ultra-wideband designs, for methodologies in the RF field that could be applied to wideband optical receiver frontend design.

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Appendix A

Chip documentation

RXLINMFB (ICGCAMAC)

The RXLINMFB (CMC: ICGCAMAC) investigates a design for high-linearity optical receiver frontend circuits for microwave photonics applications. It uses a typical feedback-inverter transimpedance amplifier (TIA), followed by a differential postamplifier (PA) design consisting of two gain stages with interleaving feedback loops based on [1]; the feedback is tuned to minimise nonlinear distortion to the maximum possible extent.

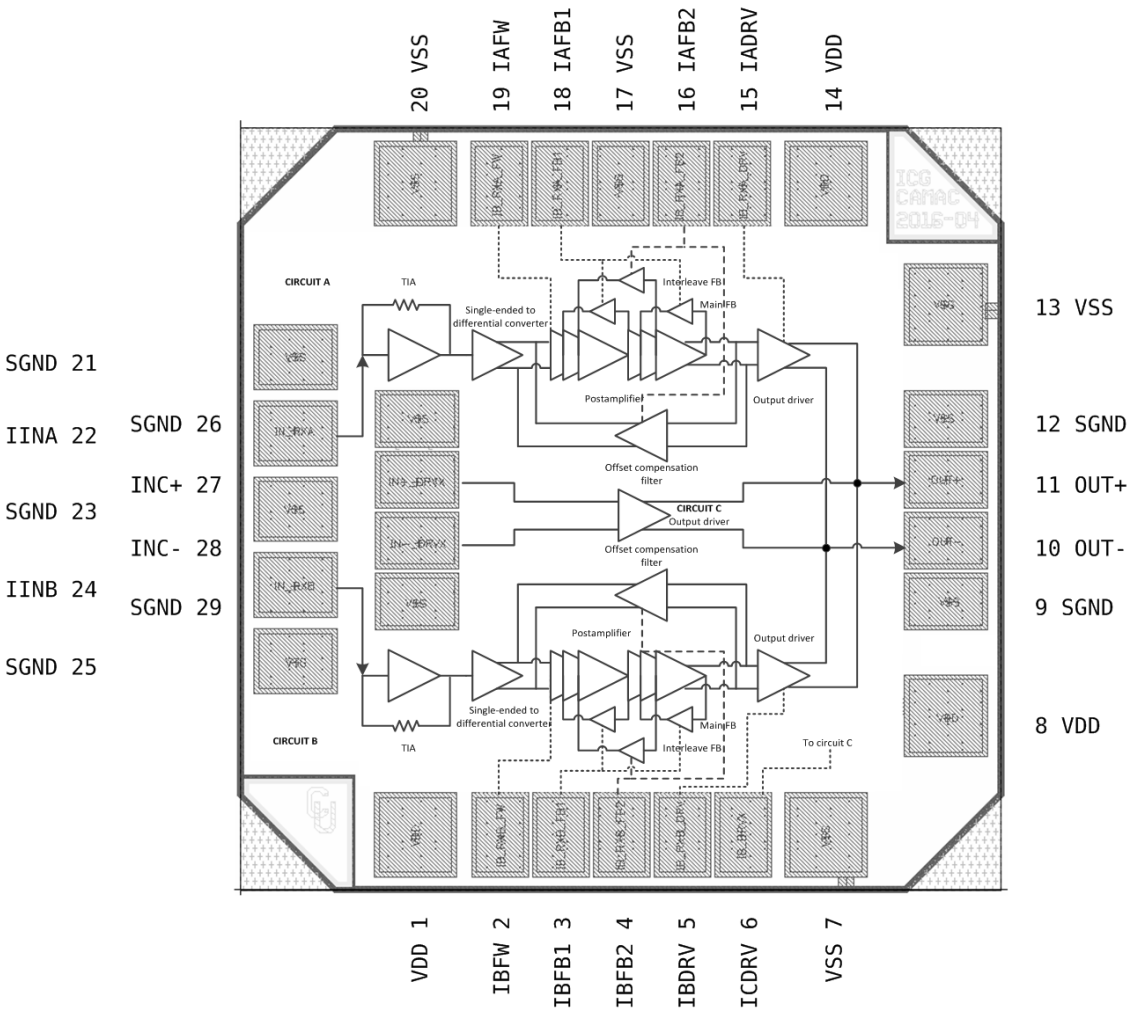
The RXLINMFB has two frontend circuits. Circuit B uses equal feedback gain for all feedback amplifiers in the postamplifier. Circuit A attempts to optimise linearity vs. bandwidth tradeoffs by using different gain values for the interleaving feedback than the gain stage feedback.

The RXLINMFB also has an independent driver (circuit C) in order to characterise the bandwidth and linearity of the output driver separately from the TIA-PA

Main features:

- 1.5V supply
- 50mW per circuit quiescent current
- Tunable dynamics via bias current inputs
    - Separate currents for forward amplifiers, main feedback, interleaving feedback, and output drivers
- Each circuit can be disabled by grounding the bias currents
- Input (circuit A, B)
    - Self-biasing around 0.5 to 0.8V
    - Matched to 50Ω for distant photodiode or electrical characterisation
- Input (circuit C only) is unterminated input - bare gates
- Output
    - Differential output of the sum of all circuit outputs A, B, C
    - 60Ω on-chip termination at output provides >20dB return loss (0.06–3GHz)
    - Output drivers can drive -10dBm into 50Ω
- Input and output compatible with microwave probes

Pinout



Electrical Parameters

DC parameters

		Condition	Min	Typ/Nom	Max	Unit
V_{DD}	Supply voltage			1.5	1.6	V
I_{DD}	Supply current, quiescent	$V_{DD} = 1.5V$ $I_{BIAS} = -350\mu A$ (all pins)		27.5		mA
I_{BIAS}	All bias pins.			-350		µA
V_{BIAS}	FW, FB1, FB2 pins	$I_{BIAS} = 350\mu A$		336		mV
V_{BIAS}	DRV pins	$I_{BIAS} = 350\mu A$		477		mV

AC parameters

TBD after testing

Operation

Circuit description

Circuits A and B are highly linear optical frontend circuits. They take a current input, intended for use with an external photodiode, and output an amplified voltage.

Each circuit consists first of a transimpedance amplifier (TIA), using the feedback inverter topology\addcite. The signal is passed into a passive RC-based differential converter.

The next stage is a two-stage differential post-amplifier (PA). This circuit uses third-order amplifier stages, consisting of three cascaded forward differential amplifiers with a negative feedback amplifier around the last two amplifiers. Between each third-order stage, further negative feedback is applied interleaved with the first feedback amplifiers.\addcite

This stage is followed by an output buffer capable of high-linearity output at around -10 dBm, to a 50Ω-matched differential output. The output buffer consists of a simple differential pair biased for driving 50Ω, and may have limited linearity despite being designed to maximise that linearity within that constraint. Other topologies may have been more linear.

Subcircuits

- Circuit A is designed to use different FB1 and FB2 feedback gains to optimise linearity, gain and bandwidth.
- Circuit B is designed with equal FB1 and FB2 feedback gains at matched gain/bandwidth, in order to compare performance.
- Circuit C is the output buffer alone for characterising the linearity of this stage. This circuit permits the analysis of the effect of the output buffer on output linearity.

Biasing

Circuit current biases are derived from an external current, instead of internal current references and mirrors. This simplifies the circuit design to focus on the research components, and also allows some adjustment of amplifier gains at runtime.

All bias inputs are designed to take a 350µA current each (sunk into the pin), supplied externally, which may be adjusted to within a certain extent to adjust transconductances (keep in mind that all amplifiers are resistively loaded, so this will affect the internal DC output voltage and dynamic range). The typical drive voltage is given in Electrical Parameters. This bias current can be supplied via a bias resistor tied to VDD (approx. 3.0kΩ for DRV pins, 3.3kΩ for other pins; an adjustment potentiometer is highly recommended), or via an active current source.

The TIA is self-biasing and its bias current cannot be adjusted.

Individual bias currents are made available for different parts of the PA and output driver. The forward amplifiers (FW), main feedback amplifiers (FB1), and interleaving feedback amplifiers (FB2) can all be independently adjusted (FB2 also affects the DC offset feedback loop). Furthermore, the output buffer bias (DRV) can also be adjusted.

Feedback amplifier adjustment allows for adjusting and characterising the linearity and bandwidth of the system. This can be used to compensate for process or temperature variations and to characterise the linearity with respect to feedback gains, which could be interesting for adaptive high-linearity systems.

Testing

Probing

The high-speed inputs and outputs are designed for compatibility with common RF probes.

Inputs for circuits A, B have pads 100µm in pitch. When used individually, GSG probes can be used; if both inputs need to be used simultaneously, dual GSGSG or GSGGSG probes should be used.

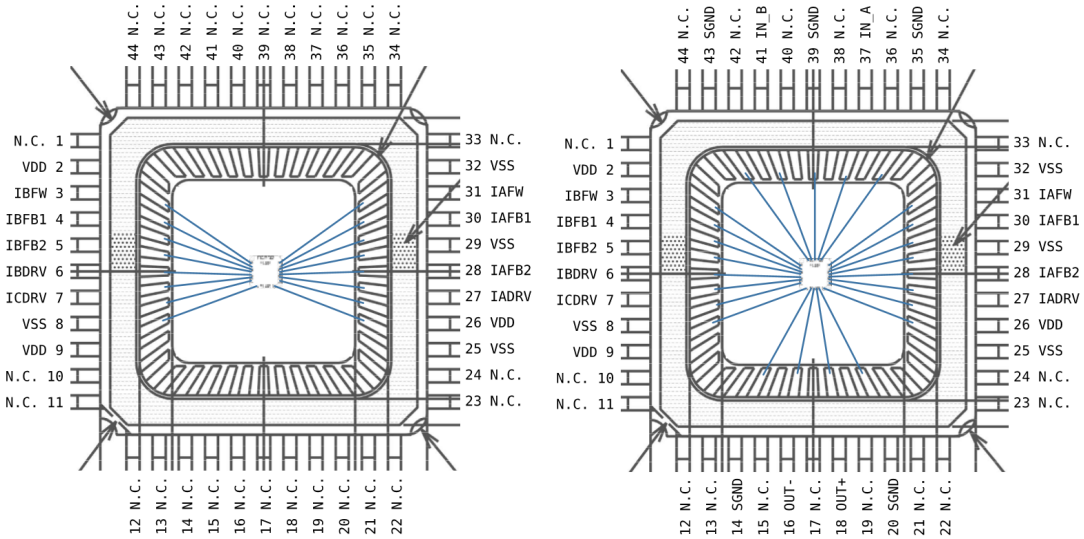
Input for circuit C is differential with pads with pitch 80µm for use with dual GSSG probes.

Output is differential with pads with pitch 80µm for use with dual GSSG probes.

The pads have a top layer of aluminium. Nickel alloy probe contacts are recommended.

Packaging

The chips have been packaged in CQFP44 packages. Two variants were packaged: one only has DC pads wirebonded and is suitable for microwave probing. The other has DC and signal pads wirebonded to the package.



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