Design Approach for a Three-Phase Voltage Source Inverter with Low Harmonic Distortion for a Wide Range of Operating Conditions

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ABSTRACT

Design Approach for a Three-Phase Voltage Source Inverter with Low Harmonic Distortion for a Wide Range of Operating Conditions

Karin Rezende Feistel

DC-AC power electronic converters, or inverters, are frequently used in AC motor drives, in AC grid interfaces of renewable energy sources and energy storage units and to supply AC power to loads in stand-alone systems. They are usually of the Voltage Source Inverter (VSI) type and are expected to operate either at a constant frequency and voltage magnitude or within a small range. Passive Low-Pass Filters (LPF) are employed to attenuate the switching harmonics providing outputs voltages with low Total Harmonic Distortion (THD_V), in the order of 1% to 3%. This is a well-established commercial technology.

This research work concerns a three-phase 6-switch VSI that is expected to provide an extremely low THD_V for the output voltage, about 0.5%, with a wide range for the voltage magnitude, 10% to 100% of rated voltage, and frequency in the range of DC to 1 kHz . In such a case, the design of the output LPF becomes more complicated, mostly considering that the load can also vary in a wide range. The target application for this inverter is the emulation of AC rotating machines. Usually linear power amplifiers are employed in this application but they are very expensive, mostly in the power range of tens to hundreds of kVA.

This Thesis proposes an approach for designing a second-order LC LPF for the demanding conditions stated above. The VSI is controlled with Sinusoidal Pulse-Width Modulation (SPWM) and an algorithm that considers the magnitudes of the voltage components of the VSI and the attenuation/amplification of the LPF is developed. It computes suitable values for L and C that allow the system to provide the required fundamental component and THD_V with the VSI operating in the linear SPWM mode. Then, a voltage control loop is designed for the VSI and an assessment of the converter losses and efficiency is carried out. The performance of the proposed system is verified by means of simulation with MATLAB and PSIM.

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I would like to dedicate this work to my mother and father, without whom this would to be possible at all. You, together with Amy, were the pillars who kept me together. And Luccas, there are no words that can describe what your support meant to me. Thank you.

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Nomenclature

A	Ampere
AC	Alternating Current
dB	Decibel
DC	Direct Current
ESR	Equivalent Series Resistance
EUT	Equipment Under Test
ξ	Damping Factor ratio
f_{res}	Resonant Frequency
f_1	Fundamental Voltage
f_{sw}	Switching Frequency
Hz	Hertz
IGBT	Insulated-Gate Bipolar Transistor
LPA	Linear Power Amplifier
LPF	Low Pass Filter
m_a	Modulation index
PHIL	Power Hardware-in-the-Loop
PI	Proportional Integral
PM	Phase Margin
PWM	Pulse Width Modulation
RMS	Root-Mean-Square value
T_d	Dead-Time
TF	Transfer Function
THD_V	Total Voltage Harmonic Distortion
SPWM	Sinusoidal Pulse Width Modulation
V	Voltage
VD	Voltage Drop
VSI	Voltage Source Inverter
V_{LL}	Line-to-Line Voltage
W	Watts

Chapter 1 Introduction

1.1 Introduction

Nowadays, the continuous growing demand of electricity results in an energy production must be done in an effective way. Power converters are a group of electrical circuits that convert electrical energy from one level of voltage or current or even frequency to another, through semiconductors-based electronic switches [1]. Thus, they enable technology development for industrial processes powered by electric system, transforming its development in an essentiality.

In the family of converters, there are rectifiers, inverters, step up/down (choppers) and voltage regulators. Specifically on the inverter group, a few types of them are well known in the industry and literature, such as two-level, three-level and the multi-level inverters. The two-level converter is considered the simplest drive to a feed a three-phase load [2] and it can generate a variable frequency and amplitude voltage waveform by modifying a time average of their two voltage levels [3]. Multilevel inverters can be used to several power conversions in high power applications and they provide more than two voltage levels. In theory, the desired output voltage can be synthetized from the multiple voltage levels with lower distortion, lower switching frequency, higher efficiency and lower voltage devices [4]. Three-level inverters, for example, have certain advantages over conventional two-level ones. They can synthetize double the voltage level using devices of similar voltage rating; for a given switching frequency, they can have double bandwidth; they have higher quality of the output signal regarding the total harmonic distortion (THD_V) levels [5]. Those are some of the reasons for the importance and the increasing of the use of the three-level inverters in several modern applications.

1.2 Types of Converters

Modern developments in power electronics switching devices allowed a better performance of high-frequency switching operation as pulse width modulation (PWM) inverters for several applications. Among the most common used converters, there is the Half-Bridge, the Full-Bridge and the Voltage Source Inverter (VSI).

1.2.1 Half-Bridge Converter

Half-Bridge inverters are commonly used to converter DC to AC. It has only two switching devices and the pulse generation technique is usually Sinusoidal Pulse-Width Modulation

(SPWM). The combination of these two switches in series is also referred as an inverter (or voltage source inverter) leg. It has only two voltage levels, and it switch devices operates alternatively. It requires double input voltage to produce the same level of output when compared to a Full-Bridge Converter. It can be observed in Fig.1.1.

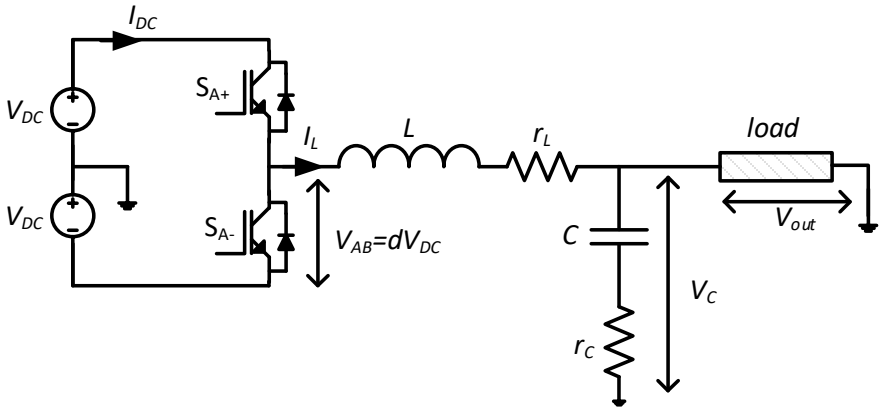


Fig. 1.1 Single-phase Half-Bridge Inverter

1.2.2 Full-Bridge Converter

Each Full- Bridge Converter corresponds to two voltage source phase legs with the line-to-line voltage is the converter output so it is capable of generate three voltage levels. For each leg, there is only two possible switching states, completing four possible switching states, where two have the same output voltage [3]. If two or more of these converters are connected in series, they can produce different levels of output voltage, characterizing than, a multi-level system.

1.2.3 Voltage Source Inverter

Three-phase Voltage Source Inverter (VSI) is a well know robust topology and one of the most widely used power electronics solution for DC/AC power conversion nowadays. It is used in applications such as variable speed drives, active power filter, uninterruptable power supplies, and electric drive applications among others [6]. In these types of applications, VSIs should be able to generate a fixed or variable frequency and voltage from a DC voltage supply in order to control, for example, the flux and the speed of a machine. Two main uses for VSI recently are in as a grid-tied converter for renewable sources, such as solar and wind. There are straightforward control strategies for synchronization with the grid and the controlled active and reactive power injection on the grid. Another important use of the VSI is as a power amplifier in Power Hardware-in-the-Loop (PHIL) application, where the VSI is selected due to its wide range of output in terms of

frequency and voltage. The VSI can be realized in many configurations, as is possible to observe in the literature. In [7], the two-level three-phase VSI is presented as a composition of three identical single-phase half-bridges.

Modulation techniques are necessary to control the converter to generate, in the output, the desired frequency and voltage levels [8]. While using Pulse-Width-Modulation (PWM) techniques, the generated output signal contains some undesired harmonics due to the high frequency switching in which these systems usually operate, which ends up deteriorating the performance of the system and quality of the output. Better performance of VSIs, such as higher efficiency and smaller output current ripple can be reached with a Sinusoidal Pulse-Width Modulation (SPWM) scheme, an established technology, followed by an output *LC* Low-Pass Filters (LPF), which is implemented to mitigate or reduce the high-frequency harmonics and it is shown in Fig.1.2. This topology is commonly used in isolated microgrids (usually with an additional inductor at the connection point) and in UPS systems. Usually it operates with voltage control mode with the capacitor voltage and inductor currents being the controlled states [9]. The *LC* filter in the output leads to an output voltage waveform that normally presents some considerable level of Total Harmonic Distortion (THD_V), usually in a level of 2-3%, which this work will aim to reduce to a value much smaller than that. This is a result of the relationship between its resonant frequency (f_{res}), and the switching frequency (f_{sw}) the former usually around 10% of the latter, also well above the frequency of the fundamental voltage component (f_1) [10-12]. In order to tune this relation between f_{res} and f_{sw}, the values of the filter components can be modified, but it is important to keep in mind that as larger the inductance, more expensive, heavier and bulkier the system can get [13].

Power semiconductors are one of the most vulnerable elements in a power converter, because its losses are the main responsible for the increase of temperature, one of the main stress sources in this system. Switching losses represent one of the most important limitations to the VSI applications, when operating in high power systems [14]. Power loss reduction and temperature stress reduction are very important targets to aim in modern power converters [6], in other words, reducing switching losses to improve efficiency is an important issue for power converters, independent of the control technique [15]. VSI are not immune to several other problems such as

overvoltage in long cables, conducted and irradiated electromagnetic interference, which will not be considered in this work.

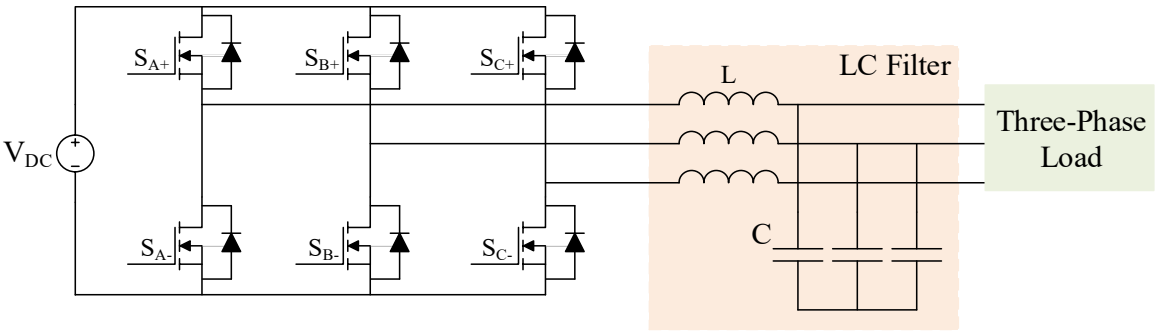


Fig. 1.2 Three-phase VSI with output LC-filter

1.3 Switching Techniques

The conversion from DC power to three-phase AC power is performed mainly by the fast switching of the semiconductors. Semiconductors switches temporarily connects, at high repetition rates, the DC terminals to the three-phase load. The power that will flow in each phase of the load and the desired sinusoidal waveform of the output (either voltage and or current) depends on the variation of the duty cycle of these switches. This variation is achieved by employing modulation techniques [16]. On the literature, several switching techniques or strategies are used in VSI applications. Between the most used techniques, it can be pointed out the Square Wave Modulation, Pulse Width Modulation, Sinusoidal Pulse Width Modulation and Space Vector Pulse Width Modulation.

1.3.1 Square Wave Modulation

This type of modulation is the one of the most simple and basic switching schemes and is the basic operation of the three-phase VSI [17]. Although the frequency can be controlled, this technique uses constant duty cycle, with positive and negative half periods. That limits the ability to control the output voltage, since it will be only a function of the DC bus.

1.3.2 Pulse Width Modulation

Pulse Width Modulation (PWM) is a modulation technique that uses high frequency pulses to produce low frequency output signals. It is a carrier-based method that is usually the preferred approach in most applications, due to the low harmonic distortion waveform characteristics with

a defined spectrum, the ability to achieve higher switching frequencies and the simplicity of its implementation [18].

The carrier-based PWM uses the per-carrier cycle volt-second balance methodology to generate the desirable inverter output-voltage waveform, and can be as a triangle intersection or as direct digital technique. The carrier signal can be a high frequency triangular waveform while the modulation signal may vary its shape. A variety of PWM methods appears in the literature, each of them resulting from a unique placement of the voltage pulses.

In the sinusoidal PWM (SPWM), there are two waves, the modulation sinusoidal one and a triangular one, that will be compared and the intersections will define the switching instants, as can be observed in Fig. 1.3. If the peak of the modulation is less than the peak of the carrier, the output will follow the shape of the first.

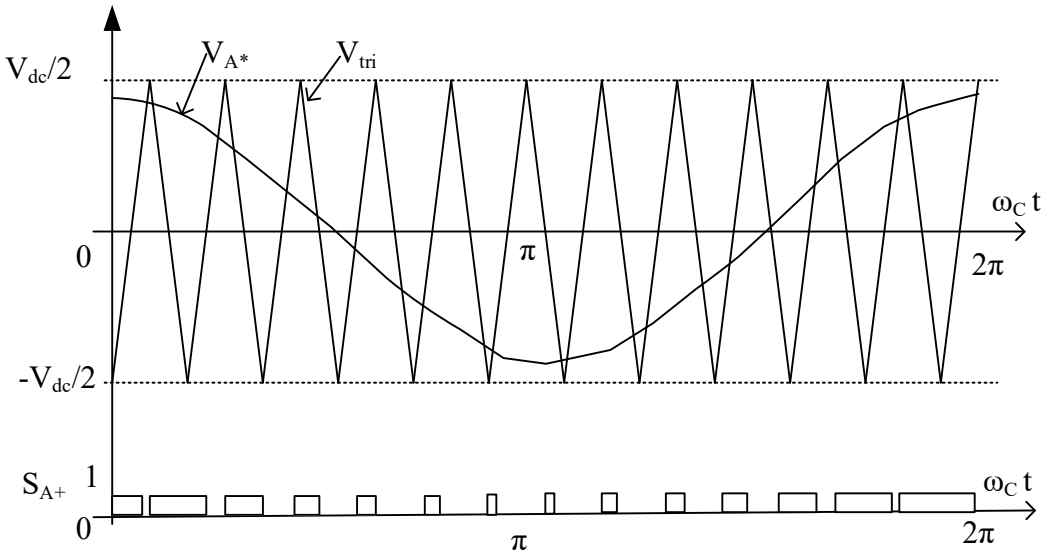


Fig. 1.3 Single-phase SPWM technique

1.3.3 Space Vector Pulse Width Modulation

Space Vector PWM (SVPWM) differs from the previous one by not using a carried-based modulation signal but it generates switching signals base on pattern possibilities and instantaneous required output voltages, as can be observed in Fig.1.4. For a three-phase VSI, for example, there are eight possible switching patterns and each of them determines a voltage space vector. In

SVPWM methods, the voltage reference is provided using a rotational reference vector, in which the magnitude and frequency of the fundamental component are controlled by the same characteristics of the reference voltage vector [1]. For SVPWM, the time length of the inverter states in the direct digital technique are pre calculated for each carrier cycle by making use of the space vector theory, and the voltage pulses are directly programmed [18]. It has constant switching frequency, a well-defined harmonic spectrum, among others. As a voltage-type modulator, SVPWM may compromise the output current causing some drawbacks to controllers [5]. It lacks in over-current protection and it is more computational intense when compared to the SPWM.

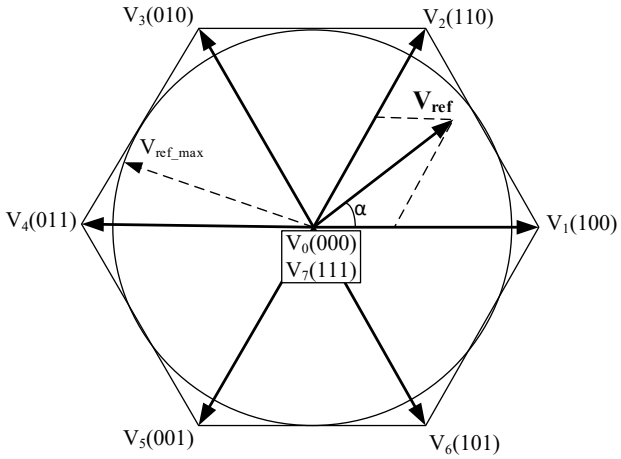


Fig. 1.4 SVPWM

1.4 Filter topologies

Output filters in switching devices are extremely important, since they reduce the harmonic content generated by the high frequency semiconductor switching. In the literature, it is possible to find several types of filters, where the simplest variant is an inductor connected to the output of the converter [19]. Combinations with capacitors as *LC* or *LCL* are also very common, and can be observed in Fig. 1.5.

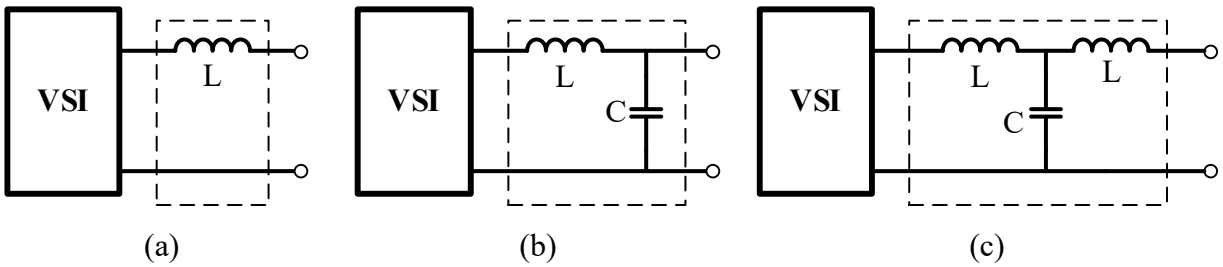


Fig. 1.5 Basic filter topologies (a) *L* filter, (b) *LC* filter and (c) *LCL* filter

The *L* filter is a first order filter that is applicable for converters with high switching frequency, where its attenuation of 20 dB/decade is adequate. When used alone, the inductance decreases the dynamics of the whole system. That is the reason that, when necessary, a capacitance is added.

Hence, the *LC* filter, a second order one, has better dynamics, and by that, better damping than the previous one. It is simple to design and it adapts very well to a variety of systems. This will be the filter chosen to be designed by this work. Its transfer function (TF) is represented by (1.1). The design of this filter is always a compromise between the capacitance and the inductance values, since they will affect the filter volume, output current and voltage ripple.

$$F(s) = \frac{1}{s^2 L_f C_f + s L_f + 1} \tag{1.1}$$

The *LCL* filter allows lower switching frequency for the converter's operation and provides good decoupling between the filter and the grid impedance, when used in grid-tied applications. In another hand, it can bring resonances and unstable states to the system, since it is vulnerable to oscillations and it may magnify frequencies around the cut-off frequency. Therefore, it calls for a precise design according to the parameters of a specific system. As the system under study has a wide range of several parameters, a simpler filter, the *LC* filter, was chosen to be designed.

1.5 Thesis Objective

Emulation of any system is defined as when a model is extracted of an equipment or a controller and it is used on a power amplifier to verify the behavior of certain parts or even the entire system. Emulation of an electric machine plays a very important role in modern power electronics, and industry, because it allows equipment that are under development to be tested under transitory and steady state conditions, inside its limits of operation, and under conditions that would be unsafe to be physically tested. This is a great strategy for growing industries that sometimes need to test solutions very fast, such as electric vehicles and airplane industries. The electric machine emulation needs an equipment for power amplification, usually a linear power amplifier (LPA) due to its fast response (high bandwidth) and ability to generate high quality

output waveforms. Even though the LPA has its advantages, it is very costly, especially for high power applications. Therefore, it is necessary to evaluate a cheaper solution with similar output quality. A high-frequency switched power amplifier is an alternative for the LPA replacement.

This work aims to develop a DC-AC converter of a switched power amplifier based on a 6-switch VSI that can deliver a voltage waveform with variable magnitude (22 to 220 V range) and frequency (0 to 1 kHz range) with very low levels of THD_V. The computation of the efficiency of the switch and operation in closed loop voltage control will be evaluated. Hence, at first, it will be proposed a design procedure for a LPF suitable for a three-phase SPWM-VSI operating with wide frequency range (where the ratio f_{sw}/f_1 can be as low as 20 and f_{res}/f_1 as low as 2); voltage magnitude varying from 10% to rated voltage; output power varying from no-load to full (rated) power or current and voltage waveform with $THD_V \leq 0.5\%$. It is important to observe that the variable load has significant impact on the damping factor (ξ) [20]; so high values of ξ, read heavy loads, can lead to high attenuations, which will affect the voltage drop of the fundamental component on the inductive elements of the LPF if $f_{res} >> f_1$ is not respected [10]. The opposite is valid, where light loads, with low damping, may cause amplifications to the fundamental component. It is important to observe that deliver full (rated) power to a load with low voltage would require an over-design of switches and inductors in terms of current ratings. Therefore, a maximum current will be defined, and as the voltage magnitude decreases the maximum output power achievable will decrease proportionally to the voltage decrease.

Therefore, it should be clear that one of the main objectives of this work is to propose a design procedure for an output filter for the VSI that will make possible to achieve an extreme low THD_V value on the output voltage, as can be observed in Fig. 1.6.This procedure will be simulated and its results will be compared with the ones proposed by the designed methodology. Non-ideal situation will be evaluated as the dead time effect on the output voltage magnitude, and the switching losses will be considered further in the study.

As the final objective of this work, is achieve an optimal filter design for a three-phase VSI to emulate an AC-machine. One of the results of that is that the motor terminal voltage oscillates at the system resonant frequency, that is small in the VSI, but it faces no impedance by the LPF. This results in a considerate amount of resonating current circulating between the inverter and the filter and causes the motor voltage to oscillate at the resonant frequency. By generating a control

loop, this issue tends to disappear. That brings the necessity of test the system under closed loop control.

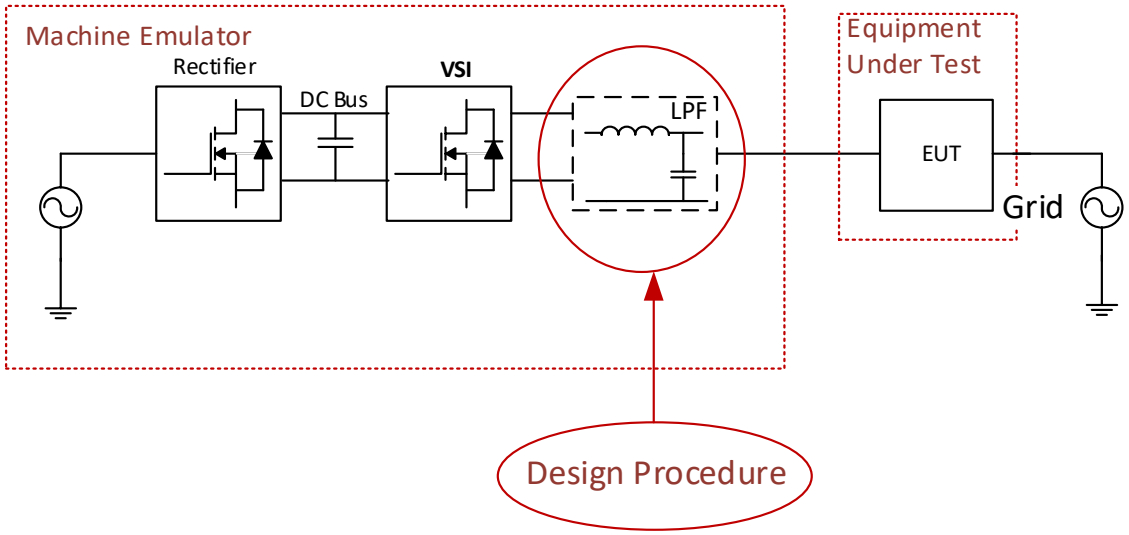


Fig. 1.6 Overall system Objective

The VSI can operate in voltage or current control mode, and inexact design of the inner loops reduces the performance of the overall control system, may even interfering with the outer loop, usually characterized by slower dynamics [9]. According to [21], any control loop, voltage or current, should at least achieve zero steady-state error, accurately track the command reference, rejecting any disturbance and compensate for low-order harmonics. Therefore, a closed-control loop will be designed and tested for the entire range of operation of the system. It will consist in voltage control loop that has the objective of to track the command signals and guarantee fast dynamic disturbance ejection in the bandwidth range. When this loop is unable to achieve its goals, the system performance damages.

1.6 Thesis Outline

The thesis is organized in five chapters, as follows.

Chapter 2 will propose a filter design for an ideal 6-pack VSI, as well as lossless L and C. It will be verified, by means of simulations, the impact of the voltage drop across the switches and

the impact of the dead time in the switching scheme, in order to consider a system closer to reality. The quality of the THD_V will depend on the design of the LPF for all potential values of the modulation index, m_a. It is important to verify whether the designed filter can attenuate the switching harmonics to achieve the closest value to the unitary gain for the fundamental component. If not, the m_a value should be redefined or adjusted. A verification of the proposed design filter procedure will be performed and therefore, after the LPF design procedure finds the most suitable values of inductance and capacitance for the system in which the desired output voltage, in magnitude and frequency, a control loop needs to be design.

Chapter 3 will present the design of the control strategy that best suits the restrictions of the system. Therefore, in order to avoid variations on the fundamental component, the closed loop control will automatically adjust the modulation index, m_a, ensuring the THD_V levels across the load, inside the desired level of $THD_V \leq 0.5\%$. The closed loop control only regulates the fundamental component and will take in consideration the wide range of voltage variation present in the system, leading to the possible necessity of a control with a feedback loop, as will be further discussed in this chapter. The performance of the control loop considered will be evaluated.

Chapter 4 will present an estimation of the 3-phase VSI efficiency and an analysis of the losses of the system. At first, it will be used a well-known software, to estimate the losses and them, its computation will be made by means of simulation. The results between them will be compared and evaluated. The efficiency of the designs from the previous chapters is then evaluated and finally, a power density estimation is performed.

Chapter 5 concludes this research and presents some alternatives and suggestions for future works.

Chapter 2 LPF Proposed Design Procedure

2.1 Introduction

The utilization of a Voltage Source Inverter to feed an AC drive topology is common in the production lines. Once the VSI has great range of variation on the output voltage, usually passive filters and pulse width-modulation techniques are used with the objective of mitigate problems as bearing and insulation failure of the motor windings, and other concerns, such as electromagnetic compatibility or interference [22]. To preserve the lifetime of the machine, it is preferable to operate it with sinusoidal voltages, and a LC filter is used to smooth the VSI output voltage.

The system under study, a VSI with a LC filter in the output, has as final purpose to be used as an emulator of a rotational AC machine, and for that, same assumptions and parameters will be used for the design, presented in the next sections. After the parameter definition, the procedure for the design of the filter is divided in two main analysis; first, a fundamental voltage and modulation index compensation analysis, and later, a harmonics analysis will be performed. With these purposes, it will be possible to verify if the output voltage waveform harmonic level is inside the expected, by analyzing the THD_V. The system can be observed in Fig. 2.1.

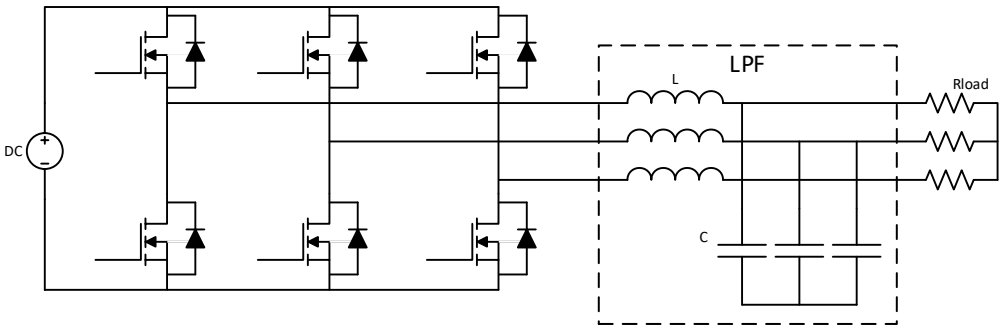


Fig. 2.1 VSI System with Output LC Filter

2.2 Design Constrains

This research work is a part of a bigger project that aims to emulate an AC machine. The chosen design constraints are determined based on the limits of operation of those machines that are to be emulated, in terms of frequency, voltage, current and power. Since the objective of this

work is to present a high quality on the VSI's output, compared to an LPA's output, the chosen THD_V level will be targeted as below 0.5%, for all the range of operation.

The design procedure that will be proposed for the filter will be constrained by a parameters specifications in the following range of values: V_{dc} = 400 V, f_{sw} = 20 kHz, 0 Hz ≤ f_1 ≤ 1 kHz, V_{oh}/V_{o1} ≤ 0.25%, 22 ≤ V_{LL} ≤ 220V, P_{rated} = 5 kW and I_{Lmax} = 15 A. The values of L and C that meet the specifications are to be calculated. Some initial values are assumed, as a resonant frequency 10% of the switching one, that means f_{res} = 2 kHz, and a filter capacitance with a value of C = 5 μF. The filter inductance is calculate from (2.1) as L = 1.3 mH. These values (L, C, f_{res}) will be used as an initial parameter and later changed if the imposed conditions are not reached.

$$L = \frac{1}{C(2\pi f_{res})^2} \tag{2.1}$$

From (2.2), the minimum value of the load, expressed as R_n ($R_{min,n}$) and so P_{rated}, is computed for all output voltage values (n) while respecting the rated output power and current. The line voltage will be defined from 10% to 100% of the rated value, with a repetitive 5% increase.

$$R_{min,n} = \frac{V_{LL,n}^2}{P_{rated}} \tag{2.2}$$

The damping for each output voltage, and consequently value of load, can be estimated, since the load resistance values will lead to the largest values of ξ_n (ξ_{max}), calculated from (2.3) [10].

$$\xi_n = \frac{1}{2R_{min,n}}\sqrt{\frac{L}{C}} \tag{2.3}$$

It is possible to plot the gain of the transfer function of the LPF and the load in the frequency domain by (2.4), as can be observed in Fig. 2.2. The gains for each of the fundamental components in the output voltage range can now be estimated, considering the system operating with maximum/rated power. It can be observed that for fundamental components below 100 Hz there

is no significant attenuation or amplification of the signal. On the next interval, from 100 to 1000 Hz, different results are obtained, since there are attenuation and amplification of the fundamental components, depending on the load and output voltage.

$$G_{LPF,n}(\omega) = \frac{\frac{1}{LC}}{(j\omega)^2 + \frac{1}{RC}(j\omega) + \frac{1}{LC}} \tag{2.4}$$

It should be noticed that the gain at the fundamental frequency should be unitary and if different from that, it must be compensated to the closest value to the unity as possible. If the gain is lower than unitary, the fundamental component is being reduced, while if higher the same component would be amplified, and both results are undesired. This compensation can be made by varying the original modulation index (2.5) to values below one, otherwise, it can lead to low frequency harmonics, due to effects of over modulation.

$$m_{a,n} = \frac{V_{LL,n}}{\left(\frac{\sqrt{3}}{2\sqrt{2}}\right) V_{dc}} \tag{2.5}$$

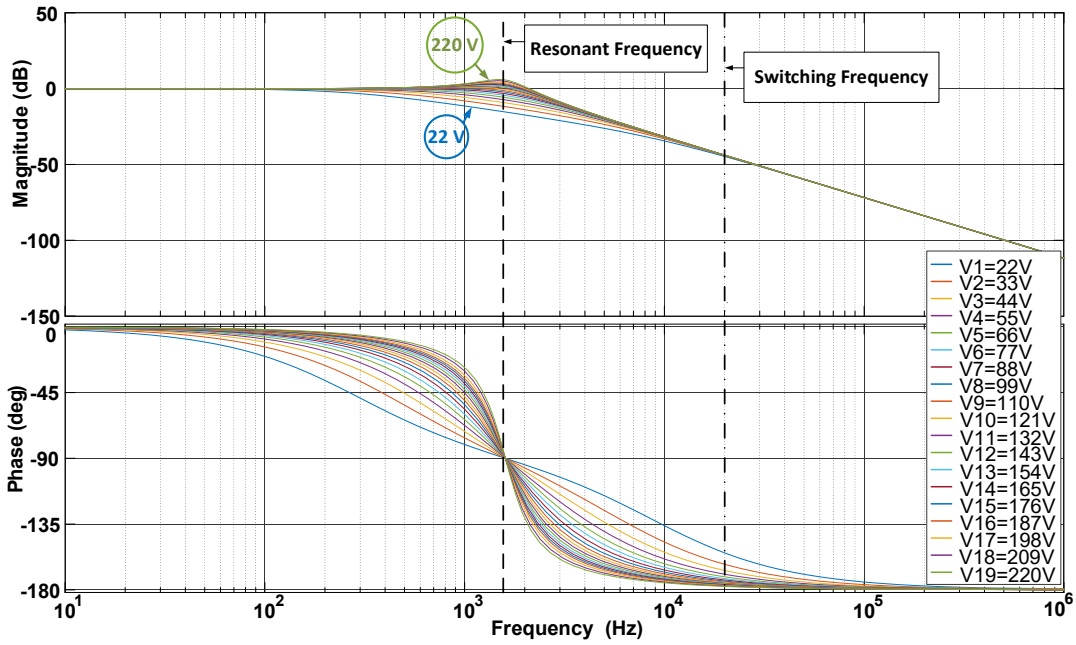


Fig. 2.2 Bode plot for the LPF with maximum output power in the specified output voltage range.

This variation, $m_{a,n,crt}$, calculate by (2.6), where $m_{a,n,crt}$ is the compensated $m_{a,n}$, *att* is the attenuation of the LPF and $m_{a,n}$ is the original modulation index, at these frequencies and outputs the desired voltage value across the load.

$$m_{a,n,crt} = \left(\frac{1}{att}\right) m_{a,n} < 1 \tag{2.6}$$

When $m_{a,crt}$ is less than the unity, then the initial values of the filter inductance and capacitance can be accepted, once the gain provided by the filter is compensated, ensuring a fundamental voltage close to its desired voltage [10]. The influence of the modulation index compensation in the output voltage system and an evaluation of the fundamental voltage will be performed in the next section.

In order to clarify how the load, voltage and current changes with the minimum and maximum output voltage, Table 2.1 and 2.2 presents the output current, load and power values for ten different outputs varying from 22 to 220V, and an additional column at the end represents the case for no load. The original modulation index, based on (2.5) is also presented for all the range. The current load, I_{load}, represents the current output on the load only and it does not consider the current flowing through the damping resistor. The load power, P_{load}, represents the power consumption by the load (R_{load}) only. The damping resistor (R_{dp}) is always in parallel with the load, resulting in output resistor (R_{out}). The power consumption by the damping resistor is expressed as P_{dp}, while the total output power is expressed as P_{out}. Observe that for the last current, there is zero current on the load, since just the damping resistor is connected, so the current shown in that line, within parenthesis, represents the current flowing on it. The first column (in light blue) in Table 2.1, in which the output voltage is 22 V, is consider on the scope of this work as light-load condition. The last but one column in Table 2.2 (in light green), with 220 V, is used as the rated load condition, while the last (in light orange) is the no-load condition.

Table 2.1 – System parameters: Output Voltage, Current, Power and Loads for 22 to 110V output

V_{out} (V)	22/Light-Load	44	66	88	110
I_{load} (A)	15	15	15	15	15
P_{load} (W)	571.6	1,143.2	1,714.7	2,286.3	2,857.9
R_{load} (Ω)	0.8468	1.6936	2.5403	3.3871	4.2339
R_{dp} (Ω)	150	150	150	150	150
P_{dp} (W)	3.2267	12.9067	29.04	51.6266	80.6667
R_{out} (Ω)	0.8420	1.6747	2.4980	3.3123	4.1177
P_{out} (W)	574.8034	1,156.06	1,743.77	2,337.934	2,938.55
m_a	0.0898	0.1796	0.2694	0.3593	0.4491

Table 2.2 – System parameters: Output Voltage, Current, Power and Loads for 132 to 220V output

V_{out} (V)	132	154	176	198	220/Rated-Load	220/No-Load
I_{load} (A)	15	15	15	14.58	13.12	(0.84)*
P_{load} (W)	3,429.5	4,001.0	4,572.6	5,000	5,000	0
R_{load} (Ω)	5.0807	5.9275	6.7742	7.8408	9.6800	0
R_{dp} (Ω)	150	150	150	150	150	150
P_{dp} (W)	116.16	158.1067	206.5067	261.36	322.666	322.666
R_{out} (Ω)	4.9142	5.7021	6.4815	7.4513	9.0932	150
P_{out} (W)	3,545.621	4,159.144	4,779.121	5,261.376	5,322.668	322.666
m_a	0.5389	0.6287	0.7185	0.8083	0.8981	0.8981

*current on the damping resistor only

2.3 Fundamental Voltage Analysis and m_a Compensation

It is possible to observe in Fig. 2.3 that low voltages and high frequencies can lead to an attenuation on the fundamental frequency since the gain of the designed LPF is calculated to the maximum output power at various fundamental frequencies. For instance, for f_1 = 1 kHz, V_{LL} = 22 V, rated current (15 A) and P_{load} = 571W, one gets ξ = 7.01 and a gain of 0.1087 (-19.3 dB), as opposed to the ideal unitary, demonstrating that the fundamental voltage component is highly attenuated.

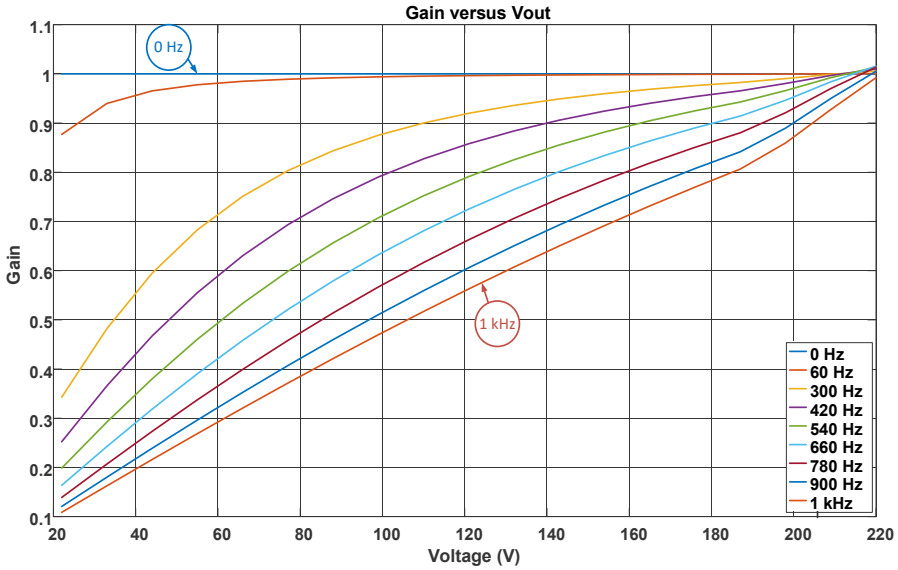


Fig. 2.3 LPF gain for various values of fundamental components in the specified output voltage range and maximum power/current.

It should also be noted that when operating with high power and voltage, this filter might still attenuate the fundamental voltage component. The modulation index should be increased but always respecting the restrictions imposed by the SPWM linear operation, i.e. being kept less than one. From Fig. 2.3, it can be seen that for voltage outputs below 210 V, the fundamental component is being attenuated for all range of frequencies. Above that limit, the fundamental component suffers small amplification, for a reduced range of frequencies.

In Fig. 2.4, it is demonstrated how the modulation index is varied and compensated through the application of the corrected $m_{a,crt}$. It is presented its behavior for a fundamental frequency of 60Hz and 1 kHz, consistently keeping its maximum magnitude bellow or equal to the unity. The computation of the harmonics magnitude should now be estimated and analyzed. On the top, for 60 Hz, is possible to see that the attenuation on the fundamental is low, as the gain is almost unitary in the whole range. That leads to a compensated m_a not very much different from the original (red and yellow lines respectively). There is a significant difference for 1 kHz where there is heavy attenuation of the fundamental. Here, the effort of the compensation is higher, leading to a completely different behavior for the original and compensated m_a (red and yellow).

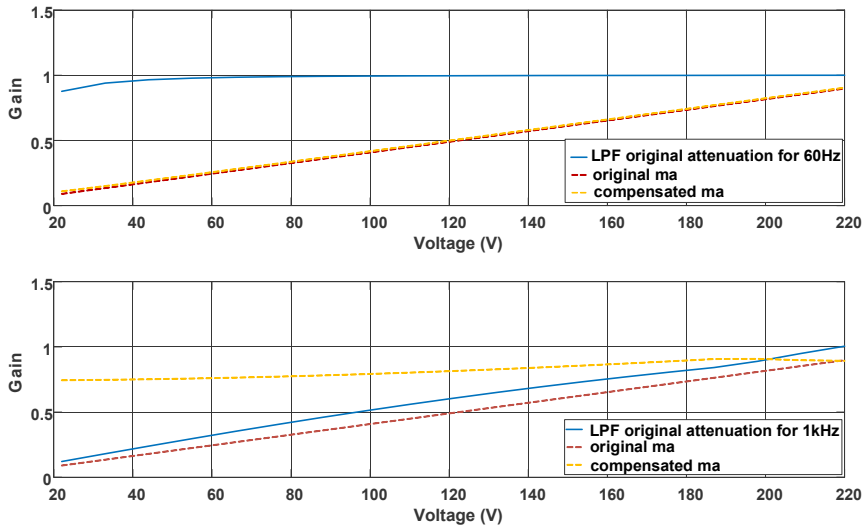


Fig. 2.4 Correction curve for m_a for frequencies of 60 Hz and 1 kHz.

2.4 Harmonic Analysis

The analysis of the harmonics magnitude should be presented, because it allows the identification of the most dominant harmonic in the output of the VSI. With that harmonic amplitude and the gain of the implemented LPF, as defined previously, it is possible to verify whether the converter output THD_V levels are accordingly with the desired condition of 0.5%. If this analysis is negative, then the filter parameters will be changed, until the proposed design approach converges to parameters that satisfy the requirements.

Therefore, it is necessary to develop a procedure to predict the attenuation area of a LPF for a three-phase VSI operating with SPWM in various conditions was developed [10]. The output voltage waveform, while using SPWM, contains many harmonics that can be divided in two categories: 1) Switching frequency (and its harmonics) at frequencies $f = mf_c$, m = 1,2,3 and 2) Sideband harmonics of the carrier frequency at frequencies $f = mf_c+nf_1$, n = 0,1,2,3,4. It was chosen to be used the Bessel Function (2.7), where R is the load condition, for the first side band, m = 1 and n = 0,2,4, and the magnitude of the harmonics given by (2.8), where J_n (order,x) and manipulating the equation using the case of M = 1, sideband (m = 1) and element (n = 2).

$$M = \frac{2R}{C_m} = 1 \tag{2.7}$$

$$h_{mag} = \frac{2}{m\pi} J_n\left(\frac{m\pi M}{2}\right) \tag{2.8}$$

That leads to (2.9), where m is a multiple of m_f (1 to 4), n is the shifting of the harmonics in the f_{sw} (0 to 7) and M is the modulation index. Equation (2.9) allows the computation of the magnitudes of the harmonics with any m_a desired in the frequencies from m_f to $4m_f$ and its respective sideband frequencies.

$$H(m,n,M) = \frac{4}{m\pi} J_n\left(n, \frac{m\pi M}{2}\right) \tag{2.9}$$

Next, it is necessary the computation of the dominant harmonic in terms of magnitude and frequency for each modulation index and at which frequency it appears. With this data, it is possible to apply the attenuation values provided by the LPF and observe the behavior of the system and a restriction regarding the maximum acceptable level of THD_V can be determine, as presented in (2.10).

$$V_{dom\_in} \cdot gain \leq V_{1_{out}} \cdot 0.25\% \tag{2.10}$$

This represents a magnitude in which the gain times the dominant harmonic is smaller than 0.25% of the fundamental voltage amplitude. This restriction guarantees the system to operate with a Total Harmonic Distortion (THD_V) smaller than 0.5%, since the dominant harmonics always appears in pairs.

2.5 Impact of the Load on the Gain Curve of the LPF

In Fig. 2.5, it is possible to observe the gain values of the system for maximum and minimum output power conditions. Three regions can be observed.

I. Regardless the load conditions, there is no attenuation on the output fundamental component. This region is limited between 0 and 100 Hz. This represents only 10% of the output range of the VSI.

II. This region is extremely sensitive to the load conditions and it is the region where most of the voltages outputs in terms of frequency are placed, summing up the remaining 90% of the output range. This represents the main reason for the compensation of the modulation curve index. This region is limited between 100 Hz and 20 kHz.

III. The harmonic content attenuation in this region is not highly influenced due to the load conditions. This region begins in 20 kHz.

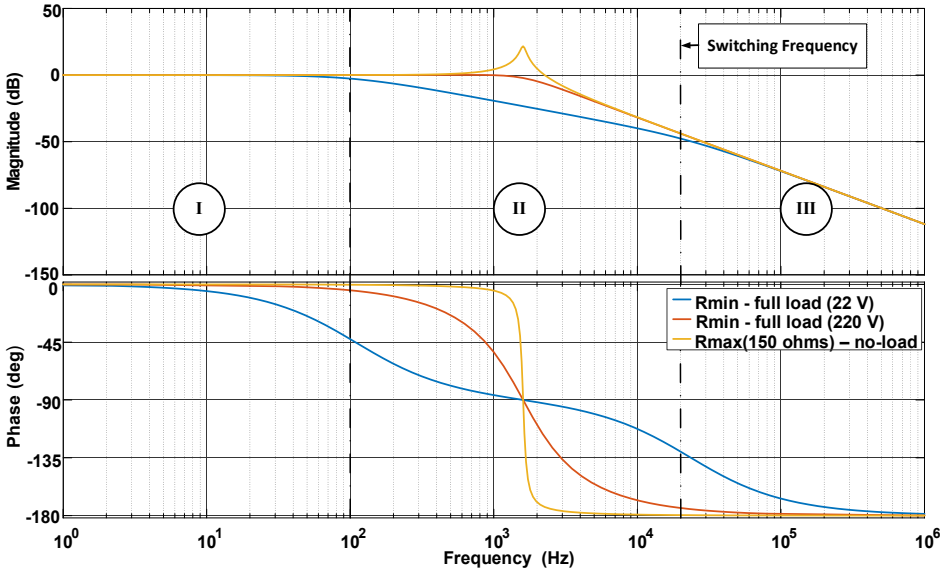


Fig. 2.5 Bode plot for the LPF with maximum and minimum output power in the specified output voltage.

The low damping curve, no-load condition, presents a high gain at the resonant frequency. It will reduce the modulation index but would not lead to a m_a >1. In order to make a more detailed analysis, three load cases will be considered, a no-load condition, and two full-load conditions, one with 100% of the rated output voltage and the other one with 10% of it. Those three cases will be discussed during the performance analysis of the proposed design procedure.

2.6 Influence of the values of L and C in the PWM Inverter

There is more than one combination of filter inductance and filter capacitance for a given f_{res}. By increasing the inductance, the current ripple of a PWM inverter is expected to decrease. In the other hand, the capacitance will be decreased and by that, increases the sensitiveness of the AC output voltage to the load current disturbances [12] - [20] and the output voltage ripple. As higher the inductor filter is, more expensive and heaviest the system will be. In addition, more voltage stress will be applied on the switches and the inductor voltage drop will reflect in a loss of the output power of the converter. Taking this information in consideration, the proposed design will suggest some values of capacitance and inductance that will try to satisfy the conditions predetermined for the system. So, after analyzing the gain of the fundamental component, if the modulation index is higher than expected, that means that the damping factor should be reduced, and that will be done, automatically by the design, by the change of the filter capacitor and inductor values. It is possible now, to present the complete design procedure for the system under study.

2.7 LPF Design Procedure Flowchart

In this section, it will be presented a flowchart for the LC-LPF procedure design proposed and discussed in the previous sections. In order to verify its performance, at first, the same parameters previously presented will be put under test, although it can be applied for other systems specifications later on. The complete procedure presented on the Flowchart will allow the inverter to operate with a THD_V in a range equal or below 0.5%. As can be observe in Figure 4, it is essentially iterative, and it will pursue the filter parameters that includes the switching and resonant frequencies, that suit better the restriction imposed. It is important to observe that the whole procedure is analyzing, during all the steps, all the load conditions (from 22 to 220 V) and all the frequency range (0 to 1 kHz).

In order to achieve its objective, the procedure was divided in two main blocks, the "Fundamental Voltage Analysis", in blue, and the "Harmonic analysis", in pink. The former, utilizes the transfer functions computed from the filter for the loads under consideration. Then, it calculates the gain of the fundamental component for each load at each frequency. As pointed in [10] each condition has its own gain curve, which in some cases, as for 1 kHz, the fundamental voltage is highly attenuated, demonstrating the necessity of the application of the $m_{a,crt}$ in order to certificate that no application and/or attenuation is applied to the fundamental component. If the compensation curve applied is not enough for compensate the attenuation presented, it suggests the application of a high damping in the system. When that is the case, the filter inductance should be decreased and consequently increasing its capacitance (2.3), and these changed filter values are now re-applied in the "Parameters Definition" block, when the test restarts until it converge to a correct compensated m_a leading to the required fundamental voltage on the output.

Once the values for L and C are found ensuring that the fundamental component is correctly compensated, the "Harmonics Analysis" can be initiated, where (2.9) is applied to compute the harmonic content and generate a list with the harmonics magnitudes. The next step is, for each load condition, determine if the dominant harmonic detected is inside the THD_V limit determined by (2.10) for all the range of operation. For that the harmonic has to be multiplied by the attenuation of the filter at the same frequency at it occurs. If it is not, the resonant frequency should be decreased in order to increase the filter attenuation for the same switching frequency harmonic. If this action is not sufficient to make the inverter to operate with low THD_V values, then the last

action taken by the procedure should be increase the switching frequency. This changed frequencies values are once again inserted in the "Parameters Definition" block in which the complete procedure will be tested again. The procedure will keep repeating itself until it converts to a solution for the case presented to it in the beginning. The complete flow-chart can be observed in Fig. 2.6.

2.8 LPF Design Procedure Performance Verification

The proposed design procedure performance will be evaluated by two approaches. First, with the software MATLAB, were the code presented Figure 2.6 was developed. It is expected to provide different values for L, C, f_{res} and f_{sw}, from the values inputted as initial parameters, leading to a squared green area at the end of it, representing that the complete range of operation of the system under test respects the restriction imposed by Equation (2.10). Once that is achieved, the complete system is inserted in PSIM environment, in order to investigate its accuracy with the parameters proposed by the procedure.

2.8.1 Design Procedure Algorithm Verification

Initial input parameters are provided to the system, as presented in Section 2.2. Tables 2.1 and 2.1 present the fixed parameters on the first four lines (V_{LL}, f_1, P_{rated}, V_{dc}). These are strictly determined by the user or designer of the system. The next four (f_{sw}, f_{res}, $C_{initial}$ and $L_{initial}$) are the variables of the system and they must be determined by the designer as arbitrary values initially, since the objective of the proposed solution is to converge to a solution. The last lines represent the increments and decrements on the switching and resonant frequency, and on the capacitance. The inductance will be changed accordantly with the new value of the capacitor and (2.1). The filter capacitance will have an increment, of 5% in its value (when necessary), representing a magnitude increment of 1 μF, when the reduction of the damping factor is necessary. For the resonant frequency steps, it was considered a decrement of 100 Hz, until it reaches a minimum value of 1.5 kHz. This limitation is necessary due to a possibility of an unacceptable increase on the damping factor. When f_{res} is smaller than that, it can lead to an increase on the gain values that may influence the frequency values that are being synthetize. These parameters can be observed in Table 2.3.

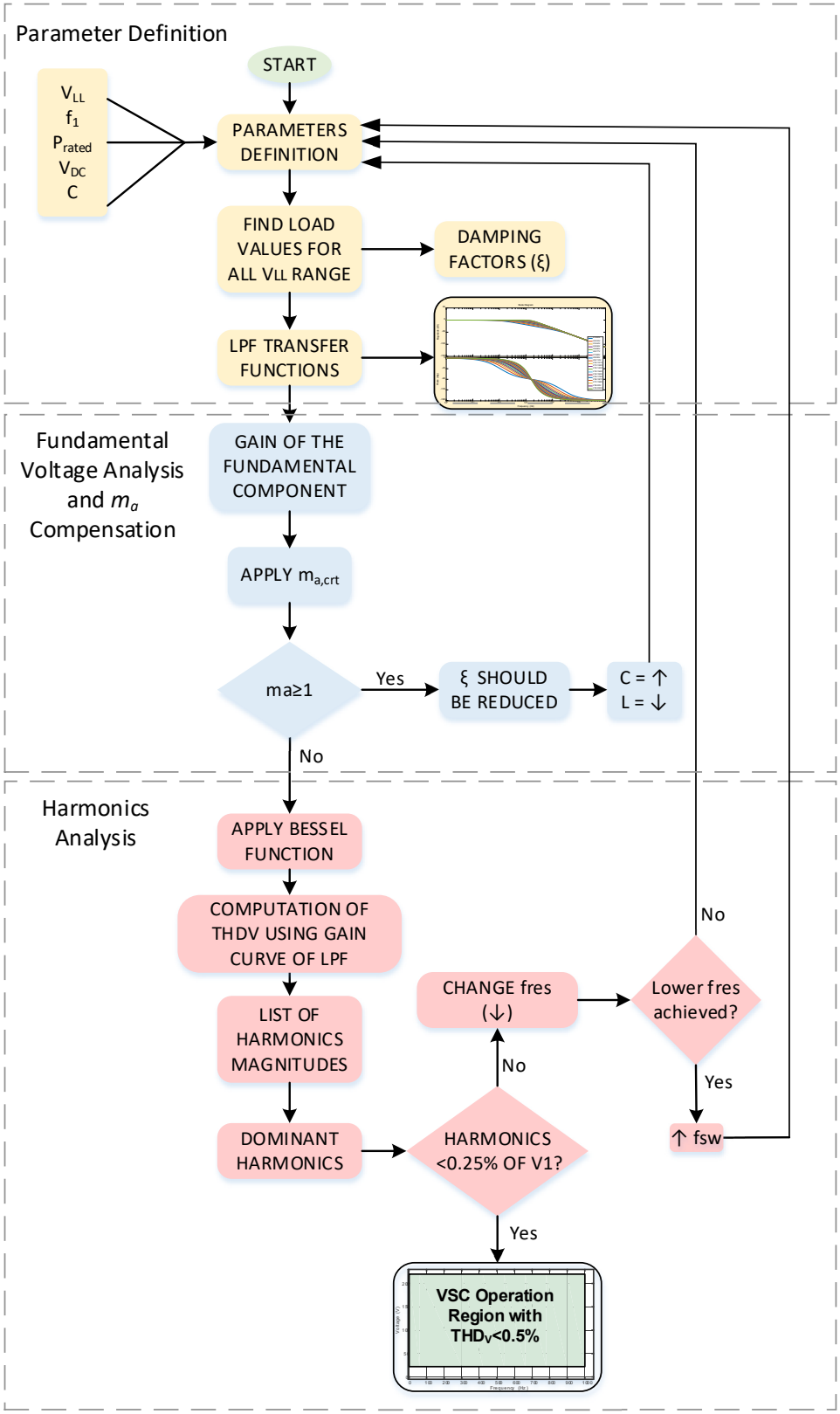


Fig. 2.6 Flowchart of the LPF Design Procedure

Table 2.3 Fixed and initial system parameters

Parameter	Value
V_{LL}	22 – 220 V
f_l	0 – 1 kHz
P_{rated}	5 kW
V_{dc}	400 V
f_{sw}	20 kHz
f_{res}	2 kHz
$C_{initial}$	5 µF
$L_{initial}$	1.3 mH
f_{sw} *increment*	1 kHz
C increment	1 μF
f_{res} *decrement*	100 Hz

To illustrate the output of the procedure the first run will be without any loops or corrections. It has the objective of showing what would be the output for the initial set of conditions as shown in Table 2.1 and 2.2. The values for the filter capacitor and inductor were 5 µF and 1.3 mH, and switching and resonant frequency were 20 and 2 kHz. The results are presented in Fig. 2.7. As it is demonstrated, the red area corresponds to the region in which the THD_V levels are higher than 0.5%. It is a considerable range, since it comprehends almost all conditions of light-load. This represents that the arbitrary parameters previously defined, did not cover all the restrictions of the system, in other words, they were not the proper ones for the case in study. The green area in the figure demonstrates the region in which the system operates within the levels imposed by (2.10).

Therefore, it is clear that the initial parameters do not achieve the expected quality imposed by the constraints. With the objective to find parameters that, allow the complete system to operate with the THD_V below the targeted value, all the loops and corrections are allowed. After running for a few times, the procedure will come up with a set of optimal parameters, as can be observed in Table 2.4. The capacitor value was changed to 9 µF, the switching increased to 30 kHz and the resonant frequency decreased to its lower limit value of 1.5 kHz. It should be observed that as

higher the f_{sw}, higher the losses i.e. lower the efficiency, but at the same time, lower the volume of the passive elements [6]. An evaluation of the losses will be presented in Chapter 4, so by this time, the switches are considered as ideal.

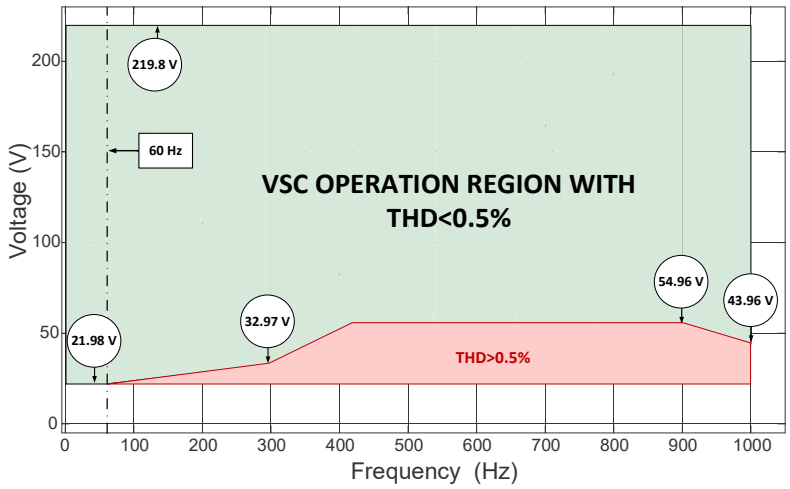


Fig. 2.7 Performance of the Design Procedure for initial conditions.

With these parameters, the complete system should be able to operate in all its range of output voltage and fundamental frequency with THD_V<0.5%. Fig. 2.8 shows the resulting area of operation with the new system parameters.

Table 2.4 - Parameters Proposed by the Design Procedure

Parameter	Value
f_{sw}	30 kHz
f_{res}	1.5 kHz
C_{final}	9 µF
L_{final}	1.3 mH

By analyzing the proposed algorithm, it can be seen how the design procedure properly works. First, it is verified if the fundamental is not being attenuated or amplified and, if the correction does not exceed the linear limits. Then, the harmonics are computed and compared to the imposed restriction from Equation (2.10).

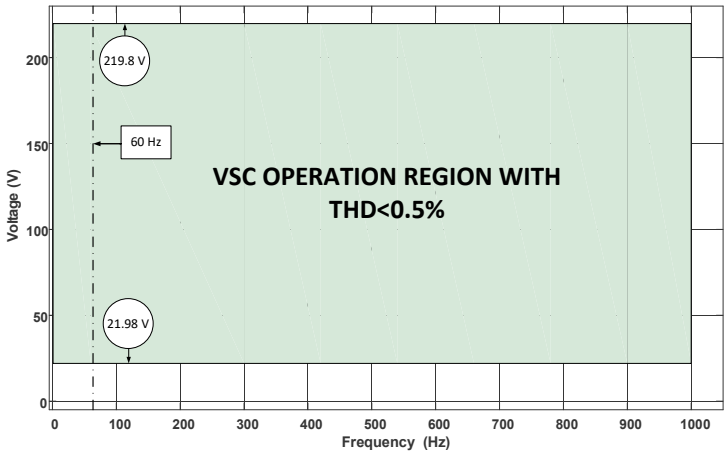


Fig. 2.8 Optimal Performance of the Designed Procedure

If the expected THD_V value is not achieved, the design modifies the filter values (C and L), the resonant frequency and the switching frequency and them, it proposes new parameters values inside the input range defined by the designer. The algorithm just stops when the parameters reach values that will satisfy the imposed conditions for the entire range of operation desired, or it will inform the user that the design is not possible to be reached with the specifications provided.

2.9 Simulation Verification of the Designed Algorithm

The software used to verify if the procedure found a correct solution for the system, by looking at the actual THD_V levels at the output signals, was PSIM, and the complete system can be observed in Fig. 2.9. The well-known SPWM modulation was chosen as open-loop control technique for this performance verification. Three cases will be evaluated, a no-load, a rated-load and a light-load condition. For all the cases, two situations were evaluated, first, for a fundamental frequency of 60 Hz, and then, for f_l=1 kHz. No losses in the filter components will be considered at this point. For all scenarios on this section, three cases will be evaluated regarding the switches: an ideal case, a case with dead time and a case with conductive resistance on the switches (called voltage drop case). First, the last two cases will be detailed.

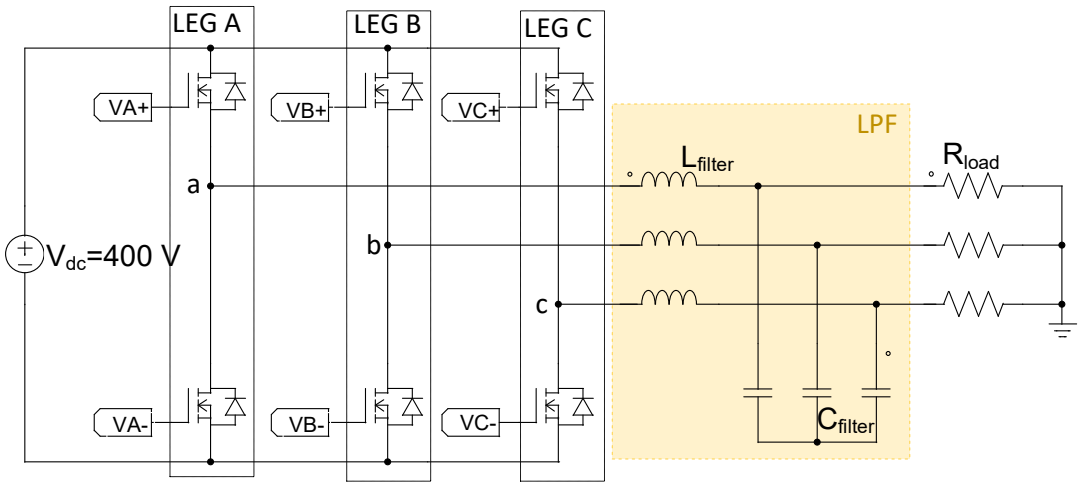


Fig. 2.9 Simulated VSI System

2.9.1 Dead-Time Effect

In the following simulations that will be presented, at first the switches were considered as ideal, to match the calculations and which makes possible the switches to instantaneously changes from on to off state and the other way around. In reality, this does not occur, and the switches present a certain delay period in which they change from one status to the other. To take this delay period in consideration, the insertion of a dead time or blanking time is essential. Therefore, the dead time (T_d) is a period of time introduced between the turn-on and turn-off of the switching devices in order to prevent short-circuit across the input [23]. It is one of the most impacting nonlinearity introduced in the system since it guarantees the safe operation of the inverter. In the other hand, it generates distortions in the output voltage and may result in a temporary loss of control [25]. When T_d is applied, both switches of an inverter's leg are off, and so, the current will find its path through one of the anti-parallel diodes, see Fig. 2.10, and its direction will dictate the output voltage polarity. The dead time is adjust to a few nanoseconds or microseconds, and it depends on the technology of the switch used, i.e., higher switching frequencies requires faster switching devices that allow T_d to be smaller [23]-[24]. In Fig. 2.11 an ideal, and complementary, switching is show on the first two lines (a and b). The next two lines (c and d) show the same signals with the inclusion of the dead time.

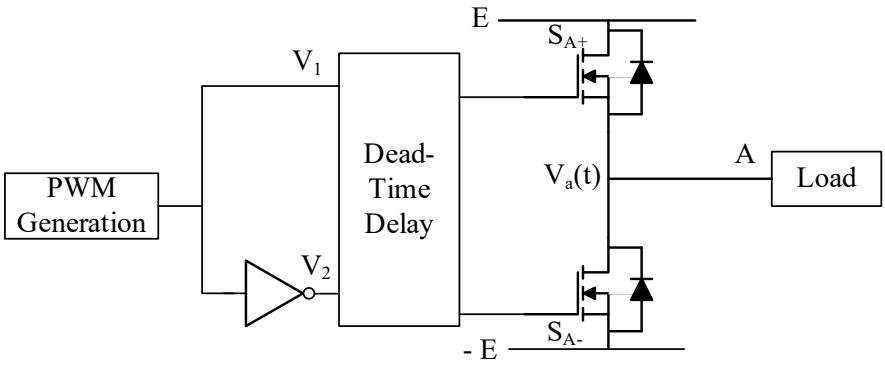


Fig. 2.10 PWM generation for the VSI, with only one leg shown

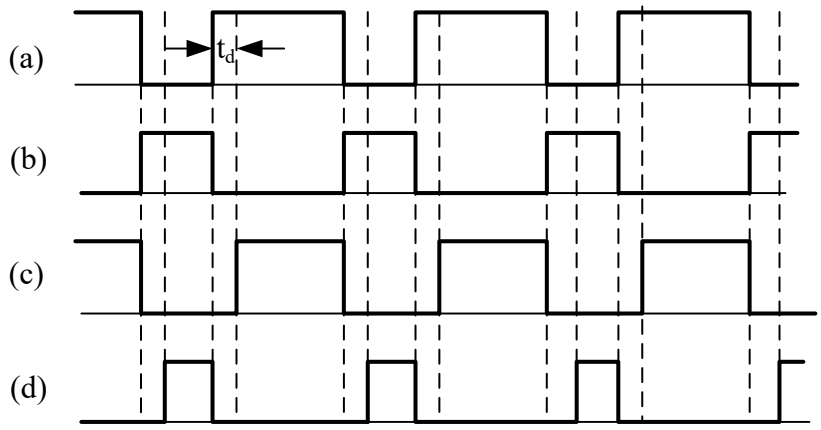
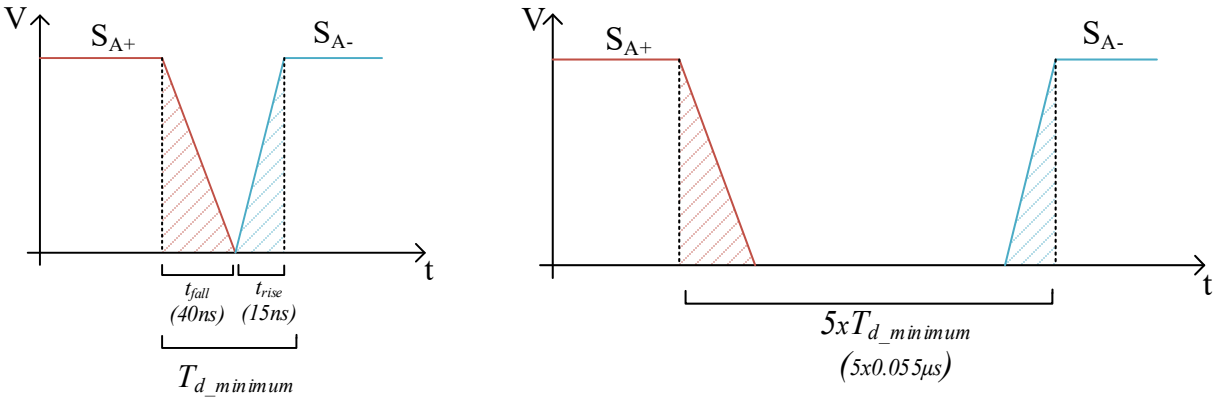


Fig. 2.11 PWM gate signals and dead time distortion

For the calculation of the dead time, it was considered an IGBT module, from SEMIKRON, the SK20GD066ET, which the datasheet can be observed in the Appendix section. The same module that will be used in the next chapters. This component have an IGBT pack in which each switch device has a rise and fall time that was used as base to determine the dead time period, Equation 2.11.

$$T_{d,min} > t_{rise} + t_{fall} \tag{2.11}$$
$$T_{d,min} > 55\ ns$$

Considering that in real systems there are other types of parasitic capacitances present that may lead to additional delays in the switching states, it was considered a safety margin of five times the minimum dead time calculated, which leads to a $T_d = 0.25\mu s$ [26]. Fig. 2.12 demonstrates the dead time chosen. Although the five times margin may seem excessive, the result represents only 0.15% of the switching period ($1/T_s$ – 1/30 kHz).



(a) (b)

Fig. 2.12 (a) Minimum dead time and (b) Selected dead time

2.9.2 Dead-time Compensation

Since the dead time occurs in every sampling of the PWM cycle, it increases the magnitude error of the output fundamental component, which claims to a compensation technique to be applied. There are several techniques in the literature, most of them based on the polarity of the current [27]-[28] and the accuracy of the compensation voltage [25]. Generally, the compensation of the dead time can be performed by adding to the reference voltage the average of the estimated voltage error [29]. A simple way to compensate the created dead time is by compensate for the average loss, or gain, voltage per carrier period. Using part of a methodology presented by [30], it is possible to observe the presence of an error from the non-ideality of the switching, here called ΔV, which is defined as (2.12), where V_{dsw} is the voltage drop across the switch. Three sinusoidal references, in phase with each one of the phases are added to the reference with its peak value corresponding to ΔV.

$$\Delta V = \frac{T_d + t_{rise} - t_{fall}}{1/f_{sw}}(V_{DC} - V_{dsw}) + \frac{V_{dsw}}{2} \tag{2.12}$$

Using the resulted ΔV it is possible to make use of the pulse-based dead time compensator technique [26 - 31], which adjust the pulse command of the modulation technique to compensate the voltage distortion caused by the dead time. The volt-variation presented by (2.12) then, is inserted in the reference voltage command, resulting in the compensation of the T_d. Although this is not the most accurate method, it performed well in the cases tested. Fig. 2.13 presents the waveforms a light-load condition, output voltage of 22 V, at 60 Hz of fundamental frequency, in which is possible to observe the compensation method working. The red curve shows an ideal condition, the green curve, the same load condition with the inserted dead time, and the blue curve is the compensated dead time output voltage waveform, very similar to the ideal one, verifying that the compensation method showed satisfactory results for its simplicity. The dead time, and its compensation, are kept constant, no matter the output voltage. The dead time for the light-load, hence lower output voltage (22V), plays a major role, and any voltage drop is more impacting since the lower output voltage. Alternatively, a result for rated load could be presented, but the level of impact of the insertion of T_d would be as relevant as in this condition.

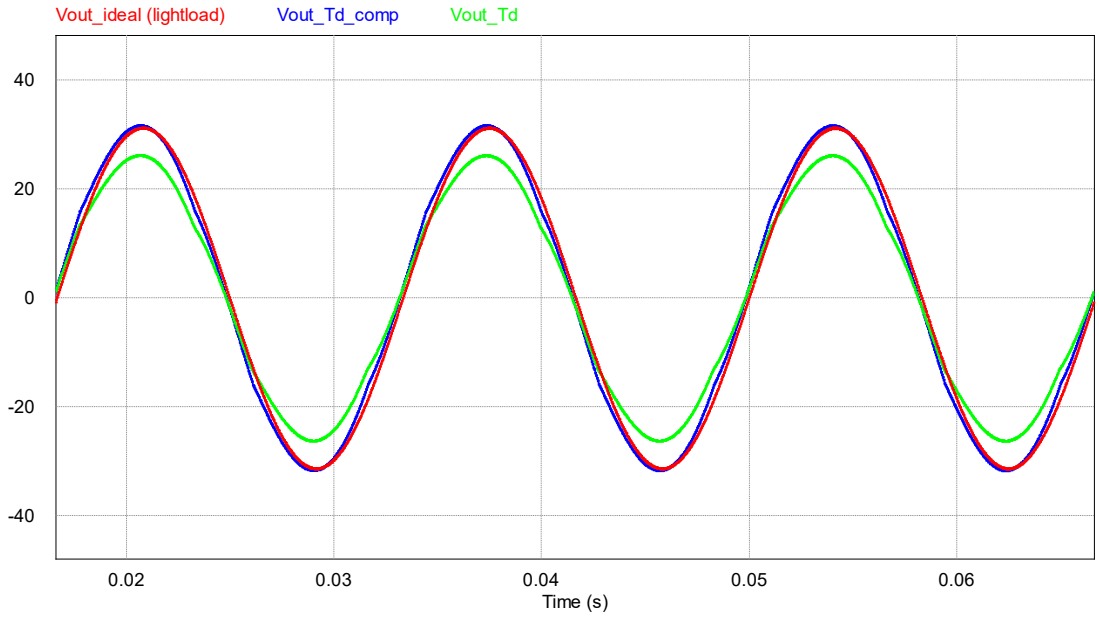


Fig. 2.13 Dead-time compensation

2.9.3 Voltage Drop

The Voltage Drop (*VD*) on a power device is nonlinear since it depends on the current magnitude and it is difficult to compensate it fully [25]. To evaluate the impact on the conduction losses, or *VD*, on the switches it is necessary to consider that, when conducting, the switch can be modeled as a series internal resistor. Using the same IGBT module, the series conductive resistance between the collector and emitter of each switch is 37 mΩ. The voltage drop on each switch is defined by Equation (2.13). Where R_{ds_on} is the series (parasitic) conductive resistance on the switch and $i_{sw,k}$ is the *rms* current on the switch.

$$VD_{sw,k} = R_{ds\_on} i_{sw,k} \tag{2.13}$$

2.9.4 Simulated Conditions

Hence, in the following subsections it will be presented comparative simulations of the system with the designed parameters for the ideal case, represented, always, by the red curve. In addition, it will be observed the effect of the compensated dead time on the output voltage magnitude, represented by the blue curve and at least, a *VD* is considered, always represented by the green curve. Three load conditions will be presented, and the details of the output voltage, power, load (resistances) and current can be found in Table 2.1 and 2.2.

2.9.4.1 No-load Condition

If a low power condition is considered, the output resistance value becomes large and the damping factor, small. The system tends to become very oscillatory what can make it difficult to obtain good transient responses in closed loop mode [10]. To avoid this oscillatory behavior and ensure a minimum damping to the system a resistor will be inserted in parallel with the output of the system. Therefore, even if this condition refers to the no-load condition, this damping resistor, R_{dp} is connected to the output. As mentioned in Section 2.2 and Tables 2.1 and 2.2, for this condition the damping resistor will be considered as the load of the system, and all a small current (0.84 A) will flow throughout it. For this condition, the output voltage will be set as 220 V, there will be no load connected to the system, hence no load current or power. The damping resistor (150Ω) will be connected to the output of the system and it will consume 322 W, entirely computed as a loss for the system, reducing the overall efficiency.

It has to be large to avoid high power losses. In this application it has been selected as 150 Ω, for $\xi_{min} = 0.05$, and $P_{loss} \leq 322$W, 6.4% of the rated VSI power. So, for this condition, the parallel resistor (R_{dp}) is presented as a situation in which $load = R_{max}$, which will represent the no-load condition. Fig. 2.14 demonstrates the situation in which the $f_1 = 60$ Hz, where the red curve represents the ideal components, the blue one the influence of the already compensated dead time and the green one, the voltage drop effect. Fig. 2.15 is a zoon in from one peak of one cycle of Fig. 2.14, so the effects of dead time and voltage drop can be better perceived. Considering the dead time insertion, an error of 2.7% is introduced in the voltage magnitude, before its compensation, with reflected in an increase of the THD_V value from the ideal scenario to 0.55%. When f1 = 1 kHz, a similar behavior can be observed due to the increase of the THDV value, when the switches are considered ideal the THDV = 0% so small that can be neglected, when the dead time is inserted the $THD_V = 0.065\%$. Although there is an error introduced and an increase in the THD_V in both situations, the restriction (2.10) was respected. The influence and impact of *VD* in the switches, for both fundamental frequencies, was very small and did not had any significant influence on the THD_V. The summary of the THD_V levels can be observed in Table 2.5.

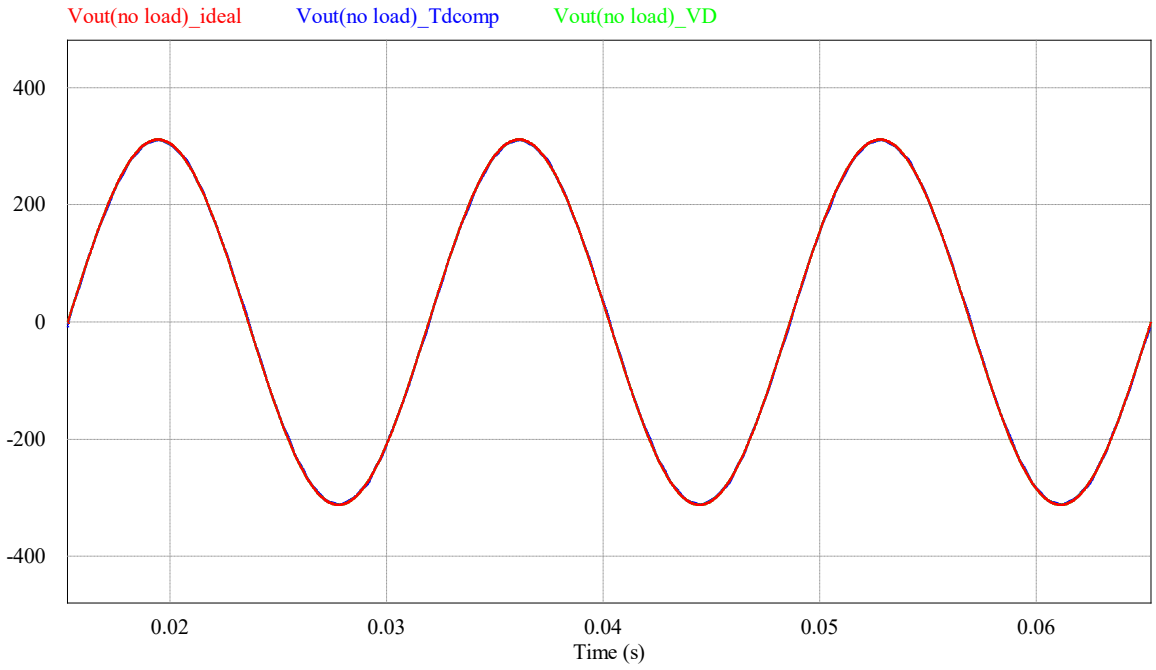


Fig. 2.14 VSI system output for no-load, V_{LL}=220V, f_1=60 Hz

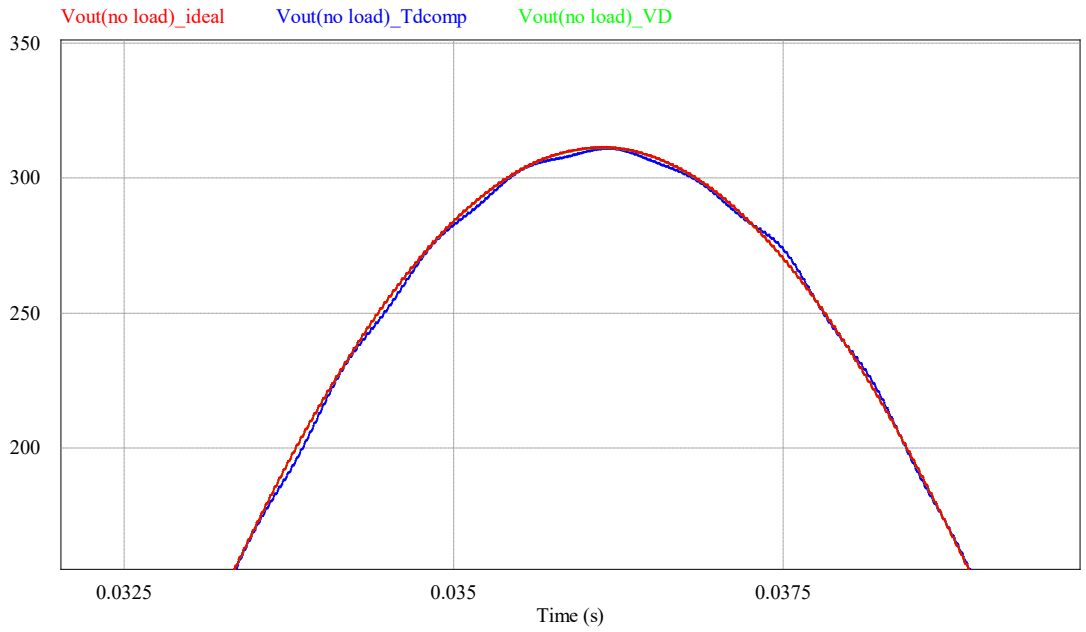


Fig. 2.15 VSI system output for no-load, V_{LL}=220V, f_1=60 Hz, zoomed in

Table 2.5 No-load condition resulting THD_V levels

Power	$m_{a,n,crt}$ ($m_{a,n}$)	f_1 (Hz)	V_{RMS} (V)	V_{peak} (V)	THD_V (%)	Condition
no-load	0.8977 (0.8981)	60	220	311	0	*ideal*
			219.6	311	0.552	T_d
			220	311	0	*VD*
	0.4901 (0.8981)	1k	220	311	0	*ideal*
			220	311	0.065	T_d
			220	311	0.052	*VD*

Also in Table 2.5, the original and compensated values of $m_{a,n}$ are presented. As in Fig. 2.5, for the case of no-load condition (orange line) there is an amplification for fundamental voltages at 1 kHz, and the effect of the *att* variable reduces significantly the corrected $m_{a,n}$, while for 60 Hz, there is a small variation. When reducing the applied $m_{a,n}$ both fundamental and harmonics are reduced, which is shown on the overall THD reduction, when the nonlinearities are included.

2.9.4.2 Rated-load Condition

In this condition, the load represents a stage in which it will have the maximum load applied to the system under normal operation. Two fundamental frequencies were also evaluated, f_1=60 Hz and f_1 = 1 kHz, and an output voltage of 220 V. For the gains applied at the fundamental frequencies, either Fig. 2.4 or Fig. 2.5 (red line) can be used as a reference. It is notable that for rated-load, the amplification (or even attenuation) on the fundamental frequencies is very small, when compared with the case previously presented for no-load. The load connected to the system for this condition is a 9.68 Ω, which is responsible for the rated power of 5 kW. The damping resistor is still connected to the output, and consumes around 322 W. The load current, 13.12 A is limited due to the limited output power of the system.

Figure 2.16 represents this case, in which the THD_V = 0% for the lower fundamental frequency, and ideal switches, red curve, and THD_V = 0.58% with the dead time insertion, an introduced error of 2.11%. When f_1 = 1 kHz, the THD_V = 0.107% for ideal switches and THD_V = 0.13% with T_d. It can be said that the restriction (2.10) was respected. Regarding the voltage drop, it can be seen that the decrease on the output voltage magnitude was very minimal, which did not had influence in the THD_V when the fundamental frequency was set as 60 Hz. When f_1 = 1 kHz, the VD influenced a little more on the V_{out}, and it increased the THD_V for 0.1%, but also respecting the restriction from (2.10). The VD effect can be observed in the green line. Also in this condition, a zoom-in peak is shown, in other to better observe the effects of both dead time and voltage drop in the output voltage magnitude, as can be seen in Figure 2.17. The resulting THD_V levels can be observed in Table 2.6.

Table 2.6 Rated-load condition resulting THD_V levels

Power	$m_{a,n,crt}$ ($m_{a,n}$)	f_1 (Hz)	V_{RMS} (V)	V_{peak} (V)	THD_V (%)	Condition
rated-load (220 V)	0.9101 (0.8981)	60	220	311	0	*ideal*
			220	311	0.571	T_d
			217	310	0	*VD*
	0.8980 (0.8981)	1k	220	311	0.107	*ideal*
			220	310	0.131	T_d
			219	310	0.108	*VD*

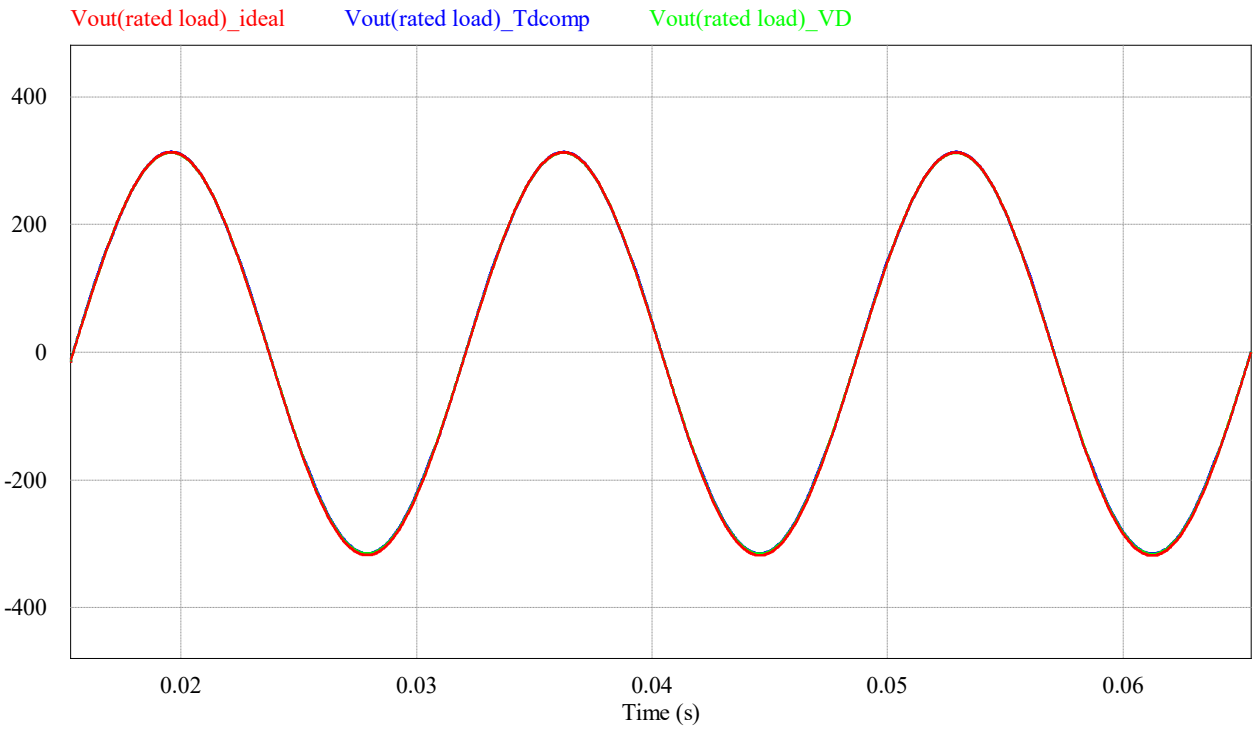


Fig. 2.16 VSI system output for rated-load, VLL=220V for f1=60 Hz

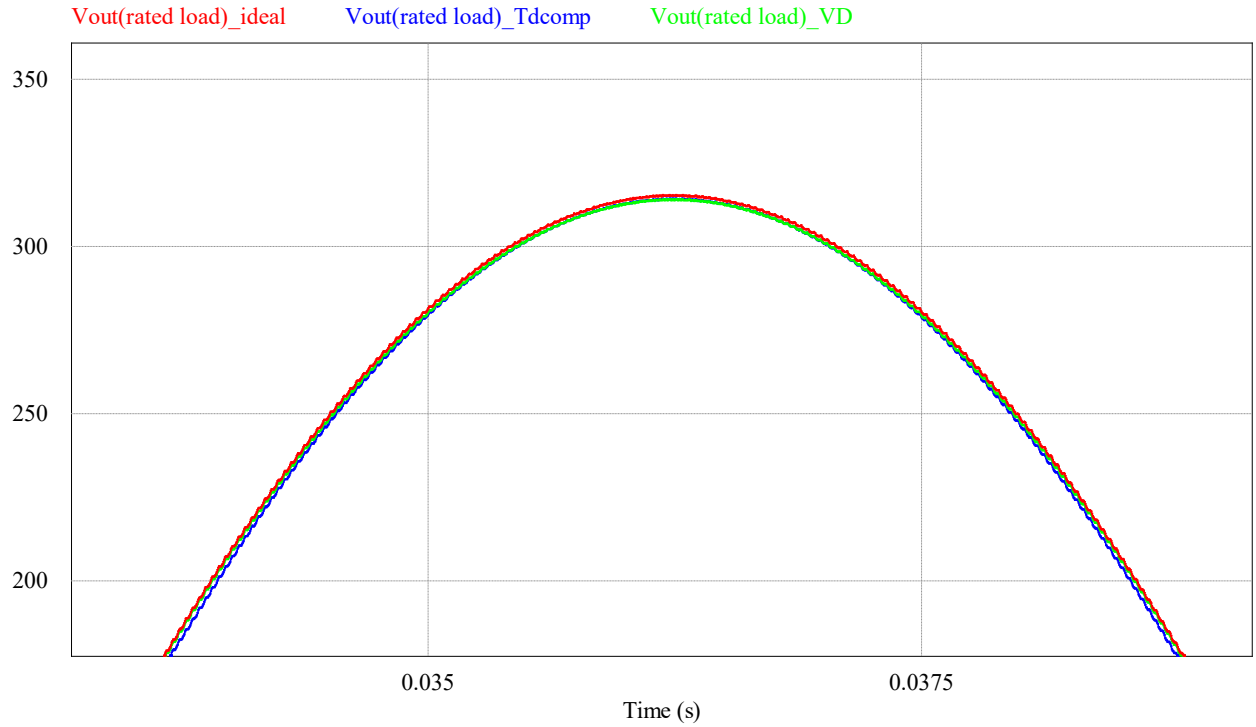


Fig. 2.17 VSI system output for rated-load, V_{LL}=220V for f_1=60 Hz, zoomed in

2.9.4.3 Light-load Condition

To verify the system for this load condition, it is considered the minimum operational load that can be applied to it under normal operation. The case was once again tested for the minimum and maximum fundamental frequency values, and Figures 2.18 and 2.19 represent it. For the gains applied at the fundamental frequencies, either Fig. 2.4 or Fig. 2.5 (blue line) can be used as a reference, for this light-load condition (22 V). The attenuation on the fundamental frequencies varies significantly here. For smaller frequencies a small attenuation happens, as oppose for higher frequencies. As shown in Table 2.7, the effort of the compensated $m_{a,crt,n}$ is very high. Increasing the modulation index brings the disadvantage of increasing the harmonics as well and this is visible, since ideal and VD conditions have higher THD_V. With this, it is possible to conclude that for rated-load the system have smaller variations, in terms of the gains due to the filter, but any condition other than that proves the necessity of corrections on the modulation index. The load connected to the system for this condition is a 0.8465 Ω, which is responsible for an output power of 517 W. The damping resistor is still connected to the output, and consumes around 5 W. The load current, 15 A is limited due to the limited output current of the system.

The first figure presents a THD_V = 0% for the lower fundamental frequency, and ideal switches, red curve, and THD_V =1.6% with the dead time insertion. When f_1 = 1 kHz, the THD_V = 0.85% for ideal switches and THD_V = 0.84% with T_d. The dead time influenced strongly on the phase of the signal.

The voltage drop in this scenario did not decrease the quality of the output voltage, since the reduction on the magnitude was almost insignificant and similarly to the previous load, it did not interfered in the THD_V value for f_1 = 60 Hz, and when f_1 = 1 kHz, it has the level of 0.83%, but the *VD* reduced more significantly the magnitude or peak of the voltage. This is the only case in which the THD_V levels were higher than the 0.5% imposed as a restriction, but are kept still in a low range. Even though the output voltage kept its good quality of the signal, represented by a very (but not extremely) low THD_V. The main cause of this is the nonlinearities inserted by the dead time and VD. The dead time used is an added value to the sinusoidal reference, but constant for all range of operation. The voltage drop is directly dependent on the current, and, since the current is the same for all operating conditions below 180 V, similar voltage drops occurs. As an example, the impact of 1 V drop at 22 V output represents 4.5% reduction, while in 180 V represents only 0.55%. Since these values do not vary during the operation of the VSI, the losses

affect the system heavier at lower voltages. Additionally, these nonlinearities were not considered when modeling the system, and this constitutes one of the main areas for future works. These cases are expecting to be corrected with the insertion of a closed control loop that will be further discussed in Chapter 3, and more results will be presented. All the THD_V values can be observed in Table 2.7. In red, are the values that surpass the desired THD_V values.

Table 2.7 Light-load condition resulting THD_V levels

Power	$m_{a,n,crt}$ ($m_{a,n}$)	f_1 (Hz)	V_{RMS} (V)	V_{peak} (V)	THD_V (%)	Condition
light-load (22 V)	0.1038 (0.0898)	60	22	31	0	*ideal*
			22	31	1.6	T_{dcomp}
			21.2	30.3	0	*VD*
	0.8937 (0.0898)	1k	22	30.9	0.849	*ideal*
			22	31.4	0.843	T_{dcomp}
			22	31.2	0.832	*VD*

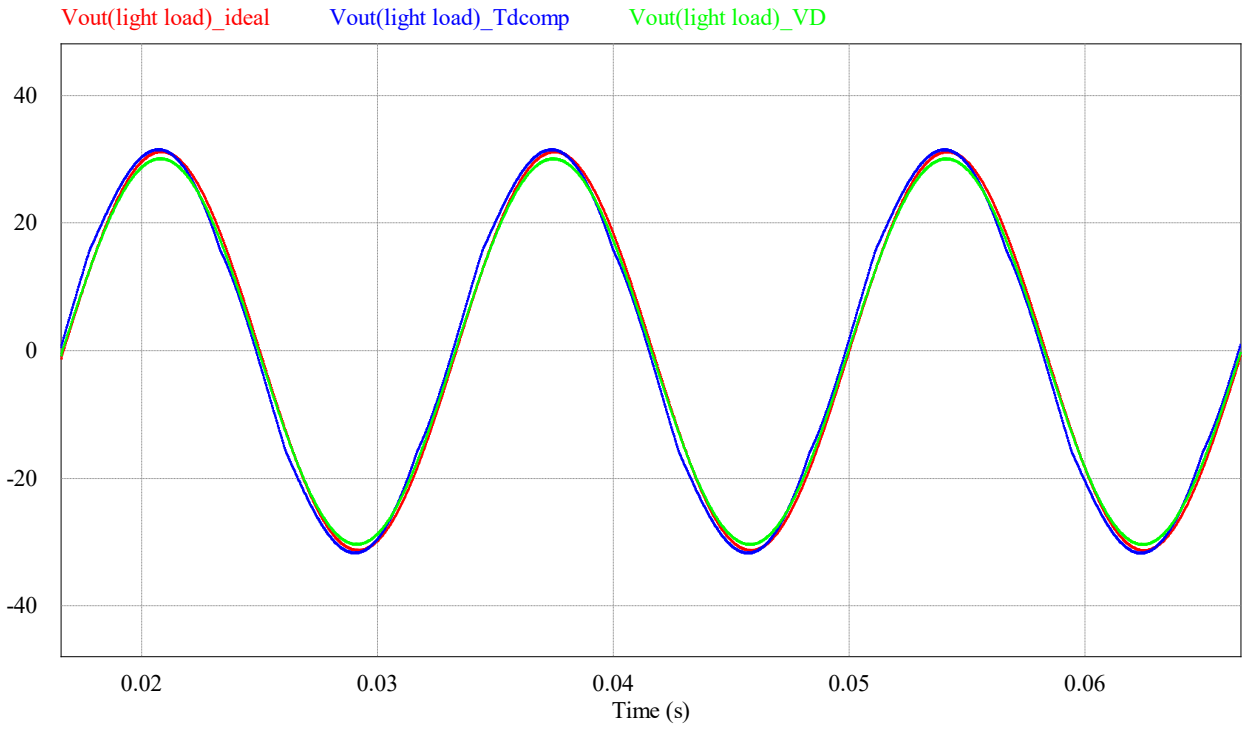


Fig. 2.18 VSI system output for light-load V_{LL} = 22 V for f_1 = 60 Hz

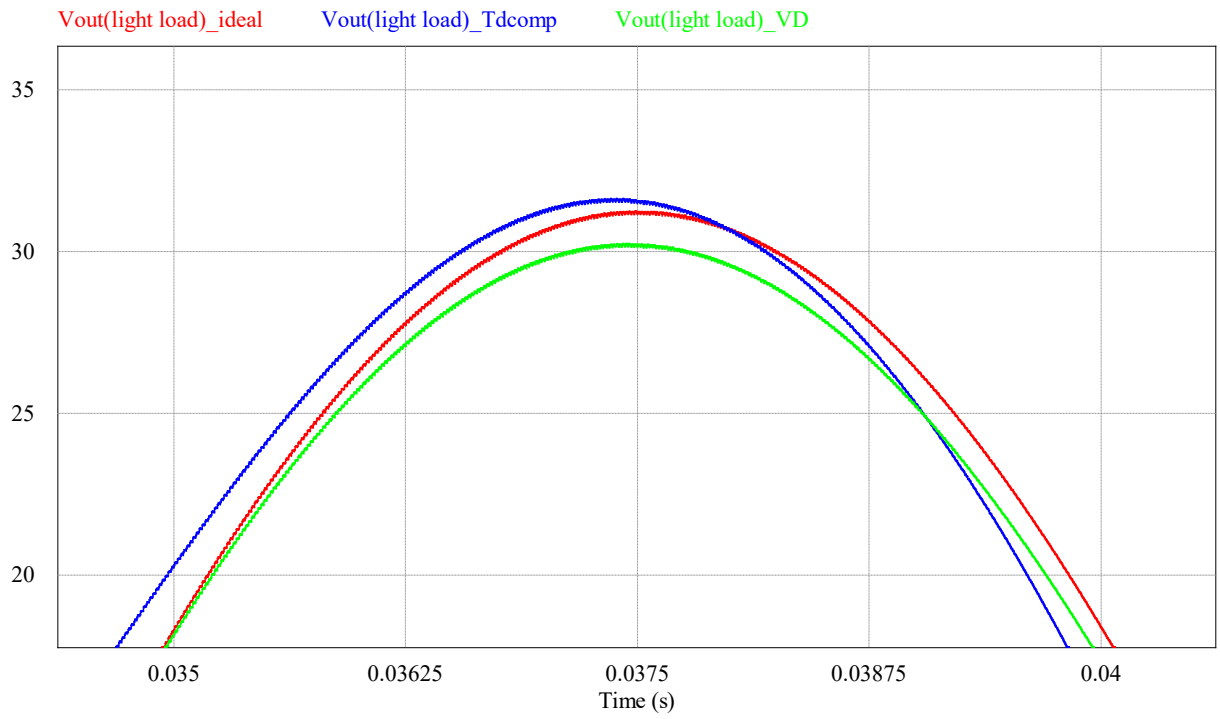


Fig. 2.19 VSI system output for light-load, V_{LL} = 22 V for f_1 = 60 Hz, zoomed in

2.10 Conclusion

In this Chapter, the main issues concerning the design of a second-order *LC* LPF for a VSI operating with SPWM with a wide range of output power, voltage and frequency with low harmonic distortion were discussed. Then, a systematic procedure for designing such a filter was described. The performance of the proposed approach was verified by means of mathematical modeling and simulation. It was taken in consideration if the load influences in the performance in the output filter.

The proposed procedure to design a *LC* filter, able to attenuate the undesired harmonics maintaining the fundamental voltage component unharmed, was presented and verified. In this procedure, the input parameters were analyzed and put to test under the necessary conditions of operation, as maintaining the corrected amplitude modulation inside the limitations (<1) and assuring a low level of THD_V for the system. It was presented the performance of the design procedure algorithm in a 3-phase VSI system. The entire fundamental frequency spectrum was analyzed and the most relevant load conditions were taken in consideration. The nonlinearities of the system were considered. A voltage drop in the switching devices of the VSI was measured and for the cases simulated it did not showed any significant decreased in the output voltage magnitude.

The necessary insertion of a dead time added an error in the output voltage magnitude that affects mostly the efficiency of the VSI. The error on the amplitude, caused by the utilization of the dead time, was compensated through a simple methodology that added the average error to the reference voltage, presenting satisfactory responses.

For most case scenarios, after the alterations proposed by the design procedure were made, the harmonic content was kept in extremely low levels. Although for the last scenario, which presented a light-load, the THD_V was slightly higher than the level proposed by Equation (2.10), it was still an extremely low harmonic level, smaller than 2%. The level presented was very low and maintained a high quality signal in the output of the system. These verifications were made using an open-loop control; the next chapter will discuss a control technique that will better suit this system and its restrictions, aiming to reducing all the harmonic levels to inside the desired range.

Chapter 3 Control Algorithm Utilized for a Three-Phase VSI

3.1 Introduction

The VSI can be realized in many configurations, as is possible to observe in the literature. This chapter presents the design of a control algorithm that will be used to control the three-phase Voltage Source Inverter with an output *LC* filter. The derivation of the equation models will be performed, followed by the design of a voltage closed loop control that will be verified in three different load scenarios, as was performed in the previous chapter. Some variations will be applied in the reference voltage and in the load, to verify the dynamic behavior of the system. In all this scenarios, the harmonic content is expected to be smaller than 0.5%, in the output voltage signal.

3.2 Derivation of the Control Equation Models

In order to calculate the control equations of the VSI, some known equations that represents the behavior of the system in *abc* coordinates, will be presented and properly transfer to *dq* coordinates using Park's transformation. The final controller for the three-phase VSI will consist of a voltage control loop. In the grid connected three-phase inverter, *dq* transformation in synchronous reference frame is used to simplify the control algorithm. As the input signals are transformed to *dq* frame, these signals are transformed to DC quantities. Due to this, signals are easily regulated to their reference values by using PI controller. The control of voltages and currents transformed from *abc* to *dq* frame variables makes it simpler to control active and reactive power. Depending on the transformation matrix used for controlling the system, function of d and q components can be interchanged. Fig. 3.1 presents the overall system.

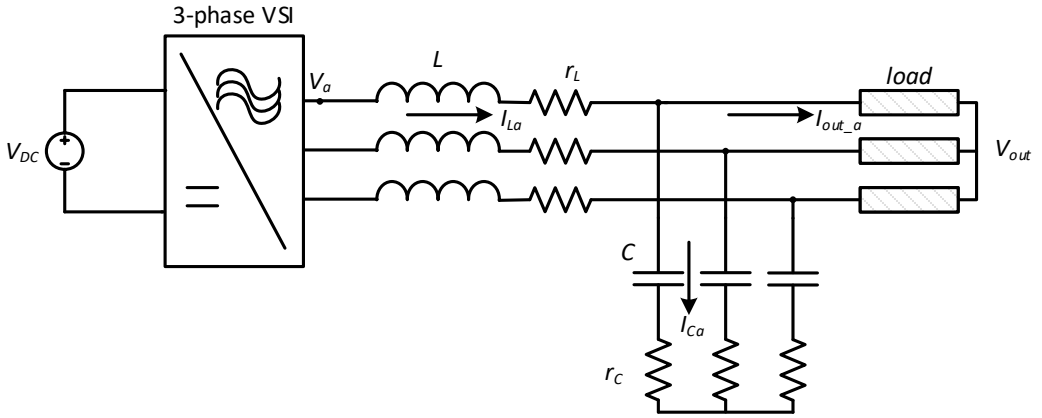


Fig. 3.1 Overall 3-phase VSI system

Equation 3.1 describes the filter inductor's current per phase.

$$\frac{di_{La}}{dt} = \frac{V_a - r_{La}i_{La} - V_{out\_a}}{L_a} \tag{3.1}$$

Where i_{La} is the inductor's current, V_a is the output switched voltage, L_a is the filter inductor value, and V_{out_a} is the system output voltage. Hence, for the three-phase system, and from (3.1), there is (3.2) and (3.3) [6].

$$\frac{d}{dt}\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} = \frac{1}{L} \times \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} - \frac{r_L}{L} \times \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} - \frac{1}{L} \times \begin{bmatrix} V_{out\_a} \\ V_{out\_b} \\ V_{out\_c} \end{bmatrix} \tag{3.2}$$

Equation (3.3) describes the capacitor's voltage.

$$\frac{d}{dt}\begin{bmatrix} V_{out\_a} \\ V_{out\_b} \\ V_{out\_c} \end{bmatrix} = \frac{1}{C} \times \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} - \frac{1}{CR} \times \begin{bmatrix} V_{out\_a} \\ V_{out\_b} \\ V_{out\_c} \end{bmatrix} \tag{3.3}$$

Where i_{La}, i_{Lb} and i_{Lc} are the inductor's currents per phase, V_a, V_b and V_c are the output switched voltages, L and C are the filter inductance and capacitance values, respectively, R is the load value and V_{out_a}, V_{out_b} and V_{out_c} are the system output voltages. Subsequent, the model of the inverter, presented by Equation (3.4), should be transform from *abc* coordinates to *dq0* coordinates [32], known as Park's transformation. For this modeling, the capacitor ESR is so small that can be neglected. According to [6], it is possible to describe the Park's transformation matrix through the matrix presented by (3.4).

$$\begin{bmatrix} x_q \\ x_d \\ x_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \sin(\omega t) & \sin\left(\omega t - \frac{2}{3}\right) & \sin\left(\omega t + \frac{2}{3}\right) \\ \cos(\omega t) & \cos\left(\omega t - \frac{2}{3}\right) & \cos\left(\omega t + \frac{2}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \times \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{3.4}$$

Where ω is the angular frequency ($\omega = 2\pi f$), (3.4) can be rewritten as (3.5).

$$\begin{bmatrix} x_q \\ x_d \\ x_0 \end{bmatrix} = T \times \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{3.5}$$

Where T is the matrix represented in (3.6).

$$T^{-1} = \begin{bmatrix} \sin(\theta) & \cos(\theta) & 1 \\ \sin\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \sin\left(\theta + \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \tag{3.6}$$

Deriving (3.5), yields to (3.7).

$$\frac{d}{dt}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \left(T^{-1} \times \begin{bmatrix} x_q \\ x_d \\ x_0 \end{bmatrix}\right)$$

$$\frac{d}{dt}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \frac{d}{dt}(T^{-1}) \times \begin{bmatrix} x_q \\ x_d \\ x_0 \end{bmatrix} + T^{-1} \times \frac{d}{dt}\begin{bmatrix} x_q \\ x_d \\ x_0 \end{bmatrix} \tag{3.7}$$

That leads to (3.8).

$$T \times \frac{d}{dt}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = T \times \frac{d}{dt}\left(T^{-1} \times \begin{bmatrix} x_q \\ x_d \\ x_0 \end{bmatrix}\right)$$

$$T \times \frac{d}{dt}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = T \times \frac{d}{dt}(T^{-1}) \times \begin{bmatrix} x_q \\ x_d \\ x_0 \end{bmatrix} + \frac{d}{dt}\begin{bmatrix} x_q \\ x_d \\ x_0 \end{bmatrix} \tag{3.8}$$

That can be represented as (3.9).

$$T \times \frac{d}{dt}(T^{-1}) = \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{3.9}$$

Applying the previous equations on the inductor's current and capacitor's voltage equations, there is (3.10) and (3.11) that represents the variables *abc* in the coordinates where they are expressed in the direct, quadrature and zero axis.

$$\frac{d}{dt}\begin{bmatrix} i_{Lq} \\ i_{Ld} \\ i_{L0} \end{bmatrix} = \frac{1}{L}\begin{bmatrix} V_q \\ V_d \\ V_0 \end{bmatrix} - \frac{r_L}{L}\begin{bmatrix} I_{Lq} \\ I_{Ld} \\ I_{L0} \end{bmatrix} - \frac{1}{L}\begin{bmatrix} V_{out_q} \\ V_{out_d} \\ V_{out_0} \end{bmatrix} - \begin{bmatrix} -\omega I_{Ld} \\ \omega I_{Lq} \\ 0 \end{bmatrix} \tag{3.10}$$

$$\frac{d}{dt}\begin{bmatrix} V_{out_q} \\ V_{out_d} \\ V_{out_0} \end{bmatrix} = \frac{1}{C}\begin{bmatrix} I_{Lq} \\ I_{Ld} \\ I_{L0} \end{bmatrix} - \frac{1}{CR}\begin{bmatrix} V_{out_q} \\ V_{out_d} \\ V_{out_0} \end{bmatrix} - \begin{bmatrix} -\omega V_{outd} \\ \omega V_{outq} \\ 0 \end{bmatrix} \tag{3.11}$$

3.2.1 Block Diagram

With the discussed equations, it is possible to draw the block diagram of the equivalent circuit of the three-phase VSI in *dq0* coordinates, as can be observed in Fig. 3.2. It is possible to observe the coupling effect that exist between the *d* and *q* signals. This effect has no influence in the zero signal.

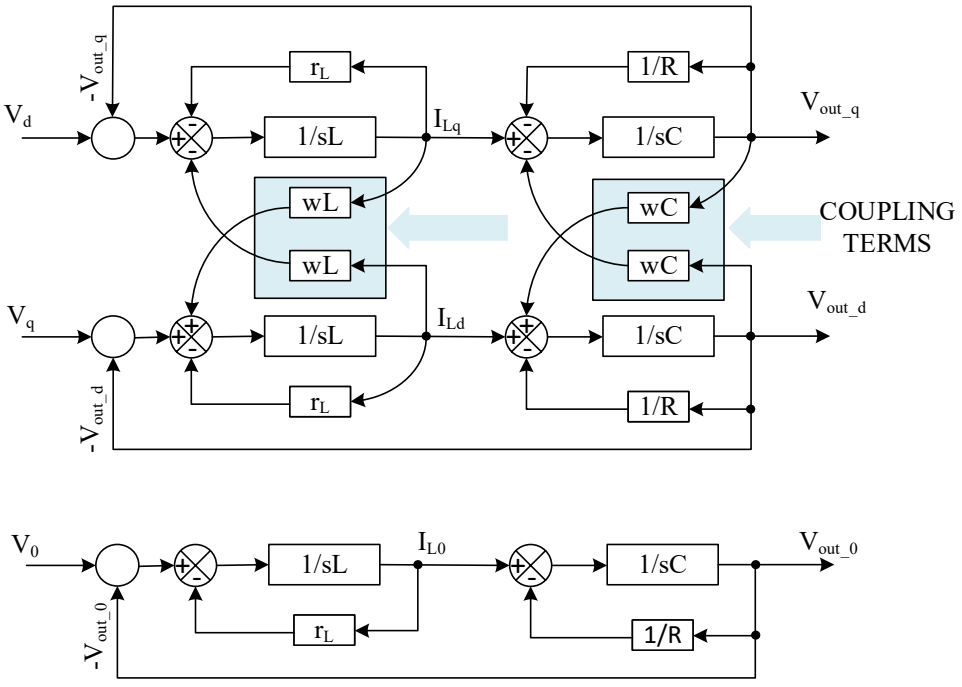


Fig. 3.2 Equivalent circuit of the three-phase VSI in *dq0* coordinates

The control loop can then, be designed and implemented in the simulation software PSIM in order to verify its performance under the restrictions impose to the system as will be discussed in the next sections.

3.2.2 Transfer Function of a three-phase VSI

All the state-space equations were mathematically developed and are well known in the literature. From Fig. 3.2, it is possible to observe the coupling effect between the *d* and *q* coordinates, while there is no such effect in the zero coordinate. It is possible then, to derivate the

VSI transfer function from the diagrams presented in Fig. 3.2, not including the coupling terms [6]. Choosing the last diagram, V_{out_0} / V_0, and performing some straightforward mathematical calculations, there is the following block diagram, in Fig. 3.3.

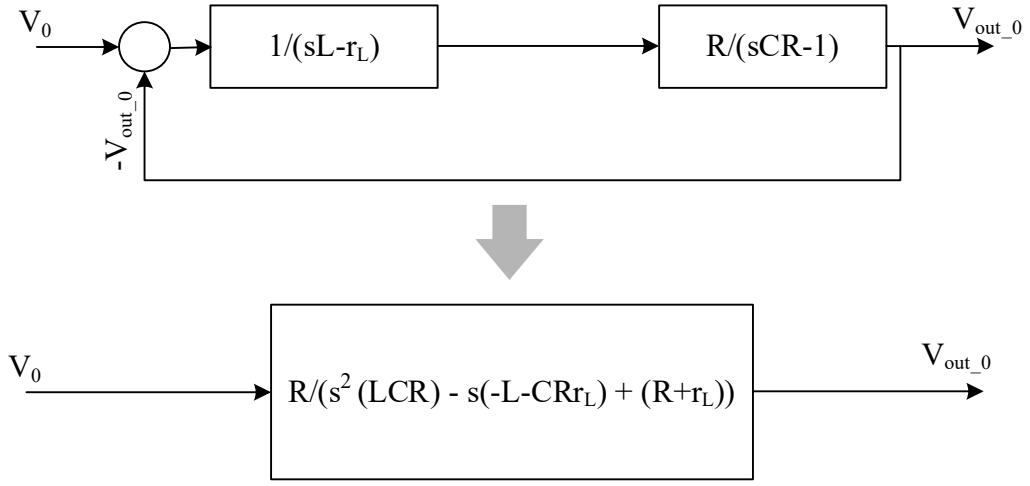


Fig. 3.3 Diagram form 0 coordinate simplification

The simplification of this diagram leads to the Open Loop Transfer Function (OLTF), of a three-phase VSI, that can be written as (3.12).

$$G(s) = \frac{V_{out}}{V} = \frac{R}{s^2(LCR) - s(-L - r_L CR) + (r_L + R)} \tag{3.12}$$

The capacitor ESR, considered was r_C= 1 mΩ (although neglected here) and the filter inductor resistance was r_L = 5 mΩ [6]. The Bode plot of the OLTF is presented in Fig. 3.4. It is important to realize that, once the coupling terms are not considered, there is three similar transfer functions, V_{out_d} / V_d, V_{out_q} / V_q and V_{out_0} / V_0, and they have the same Bode diagrams as presented in Fig. 3.4.

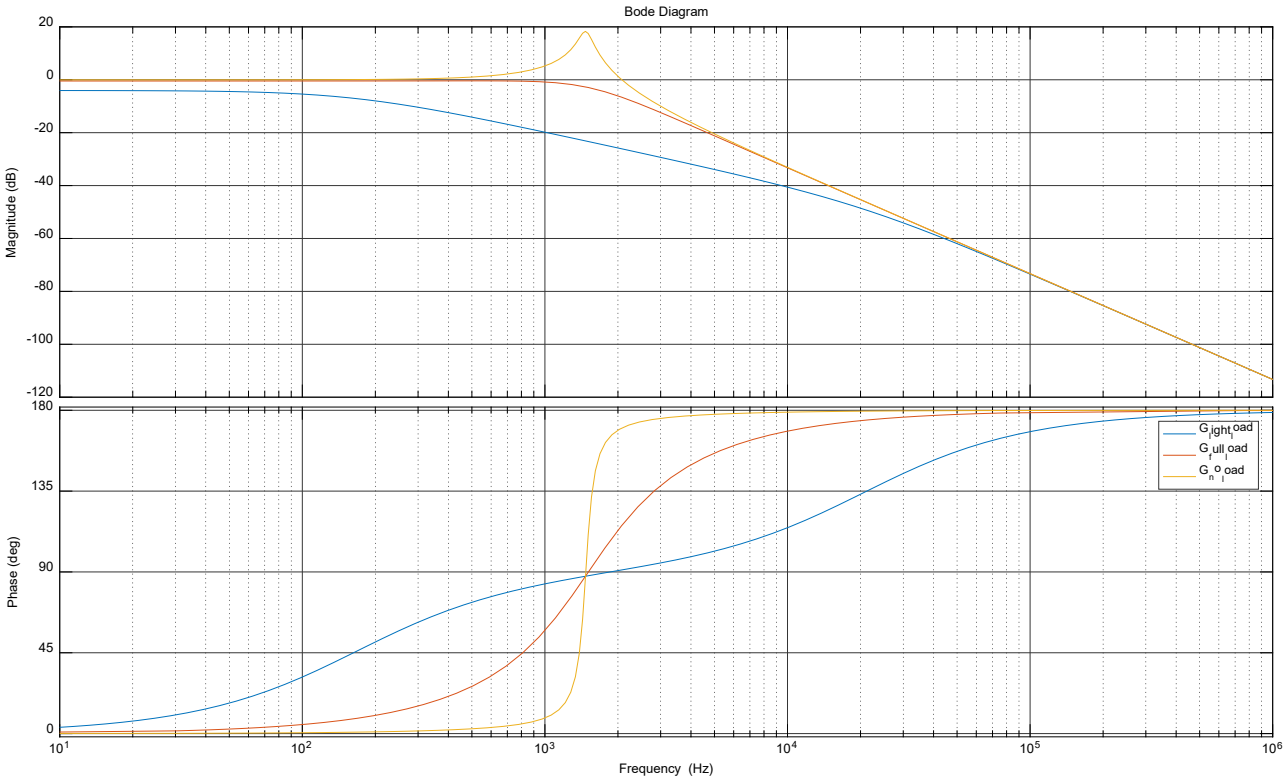


Fig. 3.4 Bode diagram for light (blue), rated (red) and no-load (yellow) conditions

By analyzing the OLTF plots of the Bode diagram of the inverter for three load conditions light-load in red (V_{out} = 22 V), rated-load in blue (V_{out} = 220 V) and *no-load* condition in orange, it was possible to observe the response of the plant system to each of the load conditions and verify the worst case, which for this system operation under no-load condition and a fundamental frequency of 1 kHz, in which the frequency is very high and the load condition is too small. At this condition, the system presented the highest dumping factor. For an appropriate inverter stability margin, the controller should be design for the worst conditions that it is intended to operate, that it is this load scenario.

3.3 Design of the Closed Control Loop

For the purpose of this study, the scenario of operation condition were V_{out}= *no-load* will set the parameters for the controller design, in order to avoid oscillatory transient responses. A PI-control type 3 was selected to allow getting enough phase margin (*PM*) and large negative slop at high frequencies. The TF of the PI-type 3 is well known and presented by Equation 3.13.

$$G_{PI3}(s)=\frac{K_{PI}}{s\tau}\frac{(1+s\tau)^2}{(1+sT_p)^2} \tag{3.13}$$

To determine all the parameters for this TF, at first, it is determined the phase margin (*PM*) and the crossover frequency (f_x) of the system as PM = 60^0 and a crossover frequency between 10 to 20% of the switching frequency, f_x =4 kHz. Using the Bode diagram of the converter's plant, the magnitude and phase can be obtained at the selected crossover frequency $|G(f_x)|$ = -16.4 dB as the magnitude, which corresponds to *Gain* = 6.06; and a phase of $<(G(f_x))$ = -177^0. Then, the phase lead of the controller can be determined from (3.14) to (3.18). All the controller parameters can be observed in Table 3.1.

$$(< GC(f_x)) = PM - (180^o + (<(G(f_x))) = 60 - (180^o + (-177)) = 57^o \tag{3.14}$$

The boost angle is then, calculate: boost = (< GC(fx))+90^0 = 147^0. And K can be found.

$$K = tan\left(\frac{boost}{4} + 45°\right) = 6.9 \tag{3.15}$$

Considering $w_m = f_x \times 2\pi = 4\,kHz \times 2\pi = 25132$ rad/s and to determine the time constant τ, there is the following equation.

$$\tau = \frac{K}{w_m} = \frac{6.9}{25132} = 274\,\mu s \tag{3.16}$$

It is known that the time constant *Tp* can be found according to (3.17).

$$T_p = \frac{1}{K \times w_m} = \frac{1}{6.9 \times 25132} = 13.8\,\mu s \tag{3.17}$$

Finally, the KPI can be written as follows.

$$K_{PI} = \frac{Gain}{K} = \frac{6.06}{6.9} = 0.88 \tag{3.18}$$

Table 3.1 Controller Parameters

Controller	Cross-over Frequency	Phase Margin	K_{PI}	T_p	τ
PI – type III	4 kHz	60^0	0.88	13.8µs	274µs

Through the observation of the Bode diagram, Fig. 3.5, it is possible to observe that the crossover frequency and the PM are according to the designed after the compensation by the controller. The blue curve represents the plant for no-load condition in open loop and the orange curve is the controller plant, with the PI controller already in action.

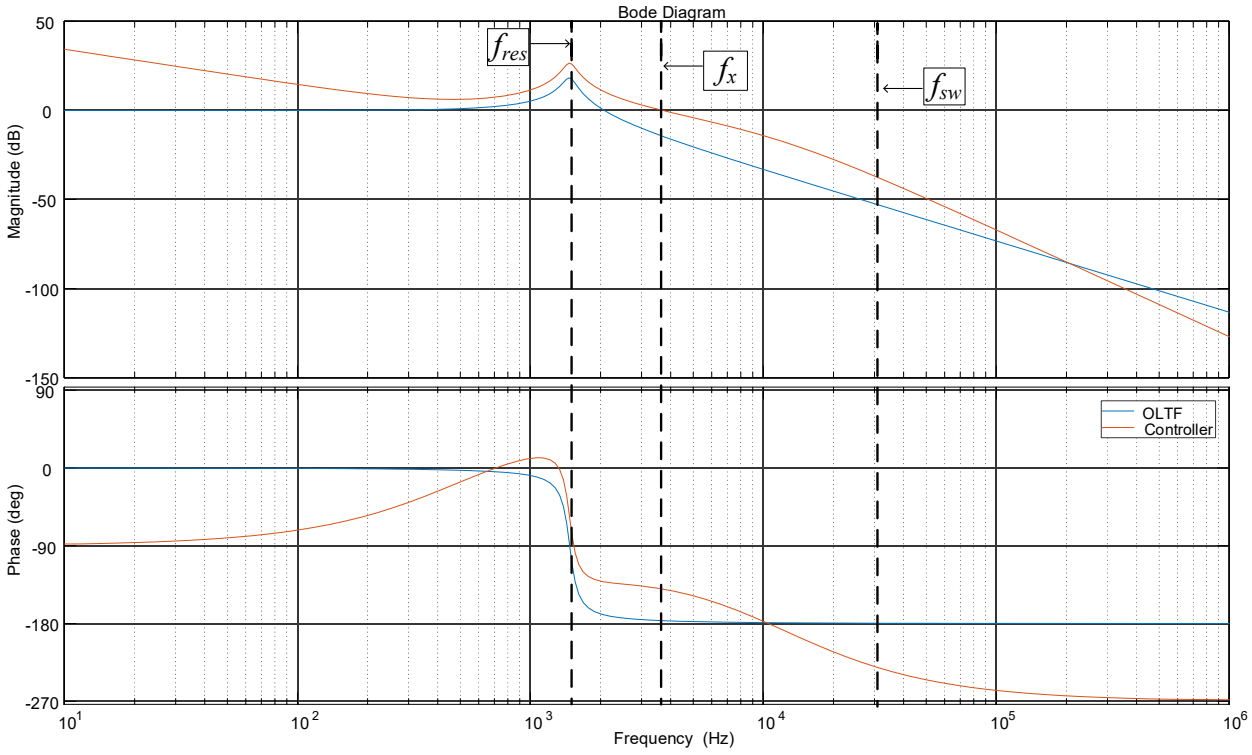


Fig. 3.5 Bode diagram of the OLTF (blue) and of the OLTF x Controller (Red)

An important characteristic of the whole system is that it is going to be controlled to match a three-phase voltage reference. Although internally there is a control loop, the desired and evaluated signal at the output will be the load voltage. It is also valid to mention that only balanced (between the phases) signals will be studied.

A theta reference angle needs to be defined in order to synchronize all the systems transforms previously discussed [2], since it makes the system to operate in the same angle reference. This angle is generated based on the conversion of the reference desired voltage signals, which are transformed from *abc* to *dq* with a grounded (zero) angle reference, similar to an *abc*-α-β transformation. This first transformation generates two orthogonal (90° phased) signals. By applying a negative gain on the second and later applying the arc tangent conversion is possible to find the theta angle. This first result is given in degrees, so a gain of 17.45m (2π/360) is inserted in the output theta generation as demonstrated in Fig. 3.6. As said before, this theta will synchronize all the subsequent systems and it is solemnly related to the frequency of the reference signal. Fig. 3.7 shows the behavior of theta for a 60Hz and 1 kHz signal. The peak of the signal reaches always the same value of 2π.

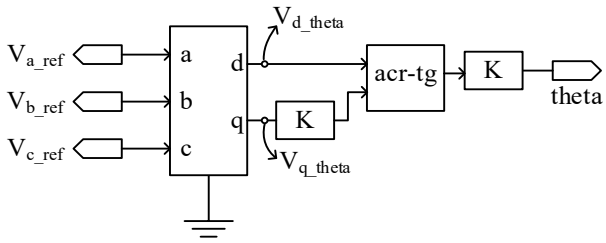
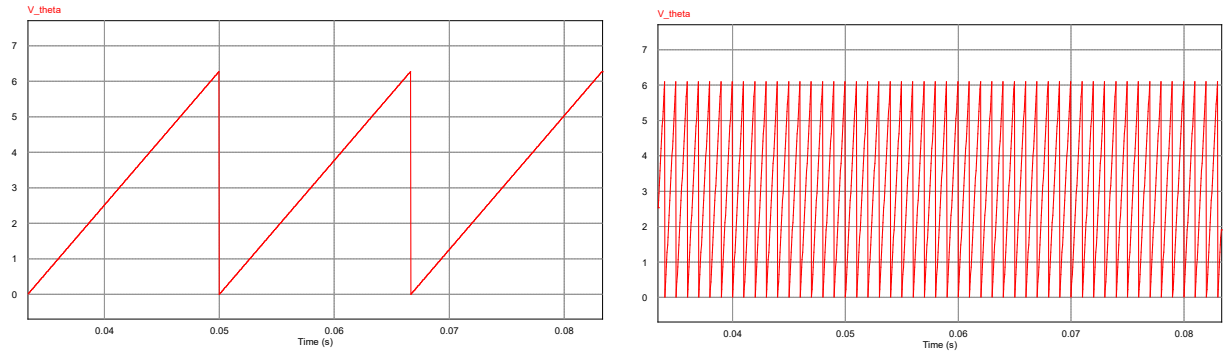


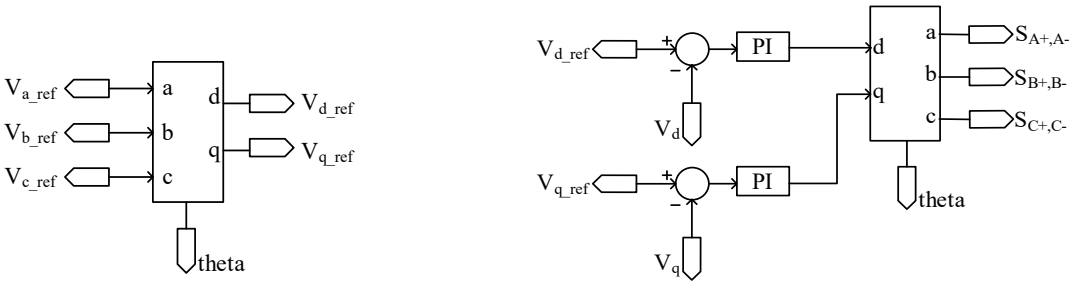
Fig. 3.6 *Theta* reference generation



(a) (b)

Fig. 3.7 The theta angle used for synchronizing all the subsystem with *abc*-dq-*abc* control for (a) 60Hz and (b)1 kHz reference signal

It is important to mention that all measured signals, as the output voltages, are sensed and initially processed as *abc* signals. All of them are transformed to *dq*. All reference signals are denoted by * or by the termination *_ref*. The reference signals for the control loop are generated based on the desired *rms* voltage values considering a balanced three-phase system. In Fig. 3.8, it is possible to see the generation blocks of the voltage generation. The theta angle from Fig. 3.6 is applied in the *dq* transformation block and this data will go through the PI controller designed after being compared to the actual measured voltage signal. The output of the PI controller will create the voltage signal that, after transformed back from *dq* to *abc*, will command the SPWM for the inverter switching.



(a) (b)

Fig. 3.8 (a) Voltage reference generation (b) Voltage Controller

In Fig. 3.9, it is possible to observe the configuration of the complete control loop previously designed and presented. The control loop has the load voltage as feedback signal. The overall system and each of the voltage controllers will be presented separately to facilitate the comprehension of the control loop.

3.4 Performance Verification of the Control Designed For the 3-Phase VSI

Three main cases will be considered for this verification, no-load, rated-load and light-load condition. The parameters used for the simulation will be the same as presented on Section 2.9.4. Each of these will operate with two different fundamental frequencies, 60 Hz and 1 kHz, and the THD_V values of the voltage output will be evaluated in order to verify if they are inside the desired levels. This Section will evaluate the steady-state results of the system mainly on the ability to keep the output in accordance with the reference and with the desired high quality, or low THD_V,

at the output. In the next Section, dynamic results will be presented in order to evaluate the stability of the system and how fast it can track references and load step variations.

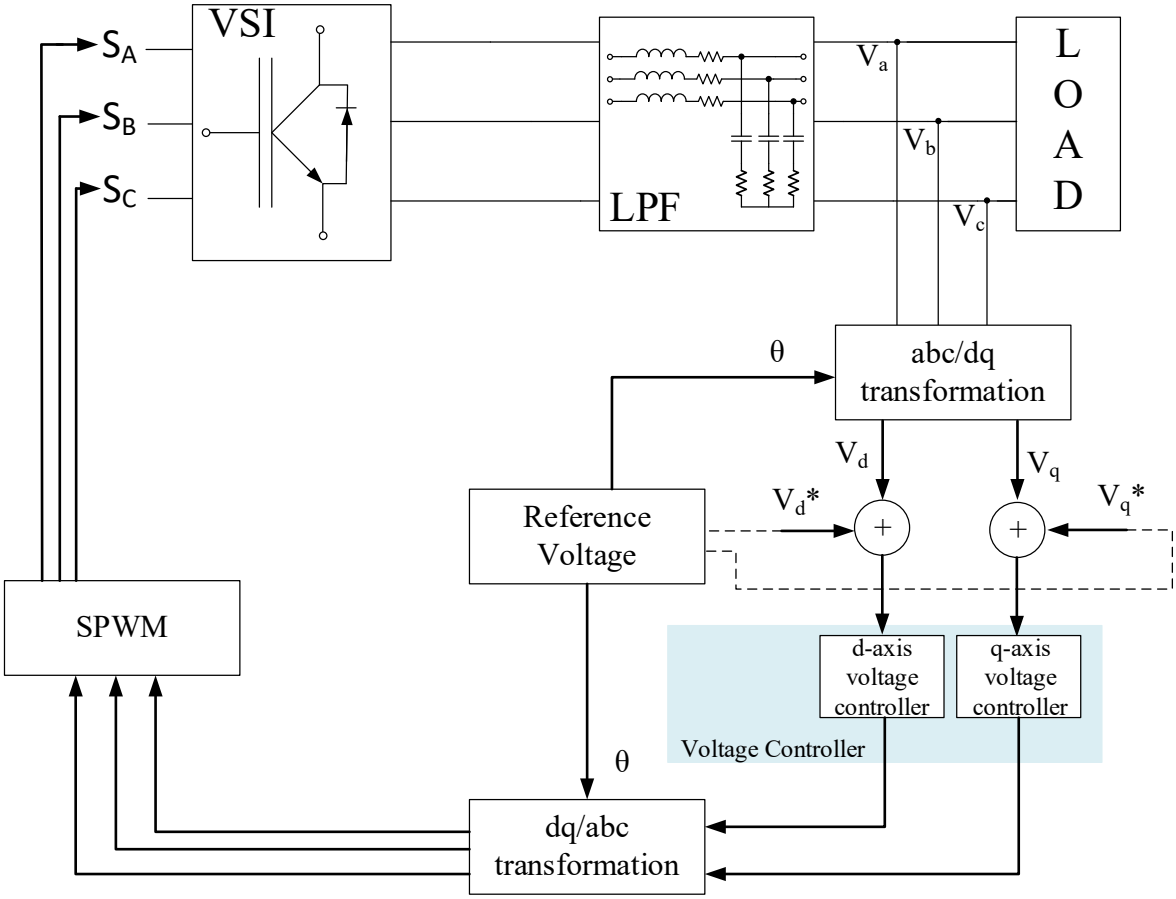


Fig. 3.9 Overall control system

Fig. 3.10 and Fig. 3.11 represents the complete system that will be simulated at the power and signal level, respectively. The system is built to test the system both in steady state and in dynamic conditions. For the initial three main cases, no step is applied on the reference or in the load and this will only be evaluated at Section 3.5. Fig. 3.11 gathers all the blocks previously presented related to the *abc*/*dq* and *dq*/*abc* transformations, the proposed controller, the references generator and lastly the PWM control signals for the switches with the proposed dead time. The values used on the PI is from Table 3.1, and the load, voltage and current values follow Tables 2.1 and 2.2. It is possible to observe the connection of the damping resistor R_{dp}, in parallel with the VSI output.

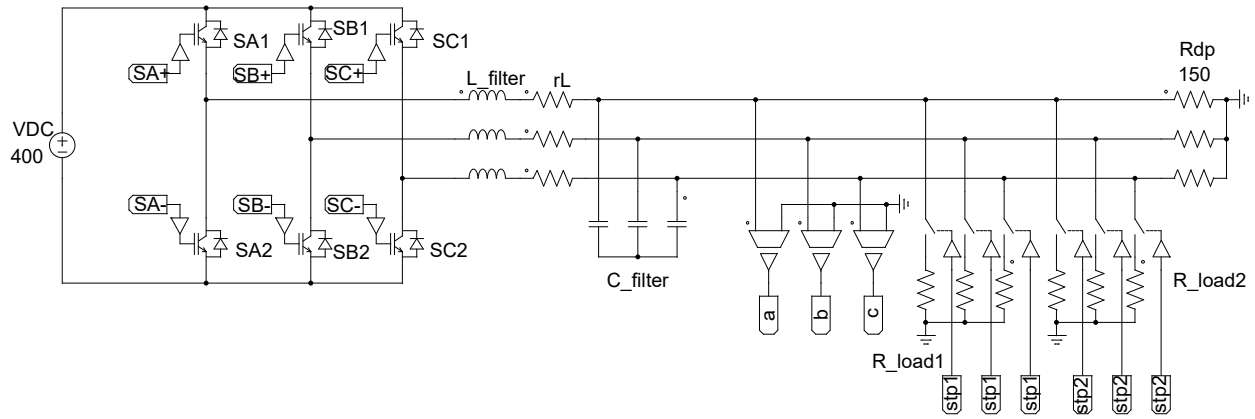


Fig. 3.10 Complete simulated system at PSIM – power level

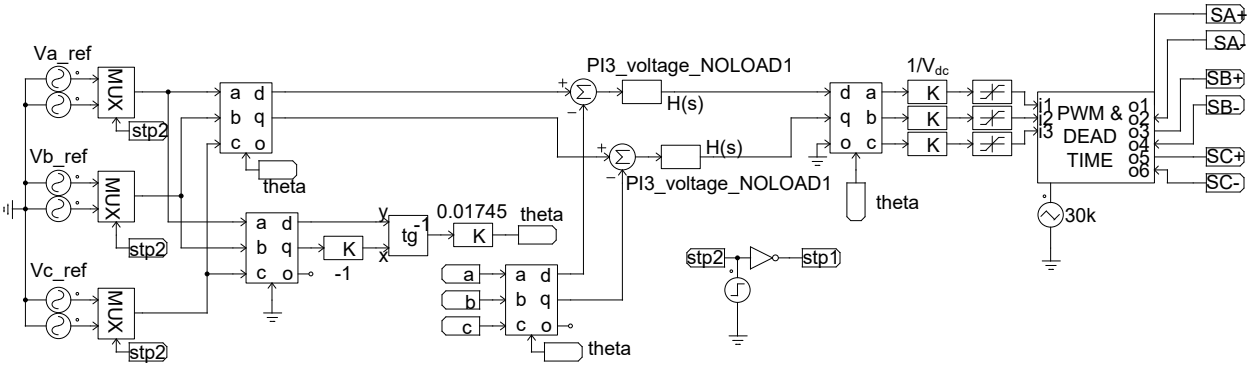


Fig. 3.11 Complete simulated system at PSIM – signal and control level

For all the scenarios that will be simulated, two graphs for each condition will be presented. The first graph shows, for the fundamental frequency of 60 Hz, the line-to-line voltages across all the three phases. In red, the phases AB, in blue, the phases BC and in green, the phases CA. The second graph, for the same frequency, presents in red, the reference voltage of phase A, in blue, the actual phase voltage in the same phase and in green, the load current in that phase. In most of the cases, the actual measured voltage followed the reference with high accuracy, and that is why sometimes, it is not possible to differentiate them in the graph. For the maximum fundamental frequency, 1 kHz, the first graph will show the same three-phase output voltages as the previous frequency analyzed and the second graph will present the modulating signal, in blue, and the triangular carrier one, that compared, will generate the SPWM pulsing signals.

3.4.1 No-load Condition

For this condition, a minimum load is connect to the system (150 Ω) and the output voltage can assume any values inside its limits of operation. A condition with an output voltage of 220 V and fundamental frequency of 60 Hz is presented and the results can be observed in Fig. 3.12. Fig. 3.13 represent the same load condition, but with f_1=1 kHz. It is important to mention that the controller could track the reference and provide an accurate output. The control signals are also in the same range values, which confirms that the control technique utilized was appropriated. The designed controller was able to output the signal and provide to the VSI system the expected responses, with a THD_V smaller than 0.5%, for an output voltage between 22 and 220 V when the fundamental voltage frequency varies between 60 Hz to 1 kHz. When the fundamental voltage frequency was 60 Hz and V_{out} = 220V the THD_V = 0.15%. For f_1 =1 kHz and V_{out} = 220V the THD_V = 0.18%.

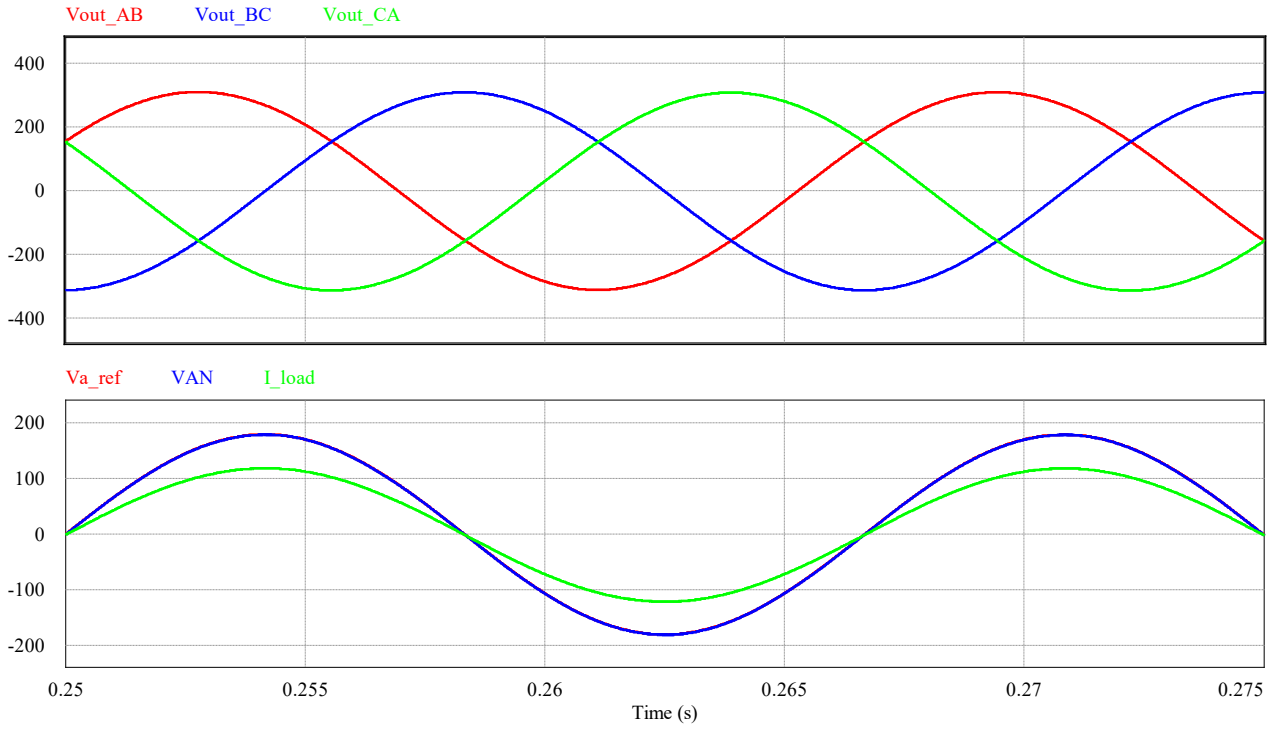


Fig. 3.12 No-load condition, V_{out} = 220 V, f_1 = 60 Hz, THD_V = 0.15%

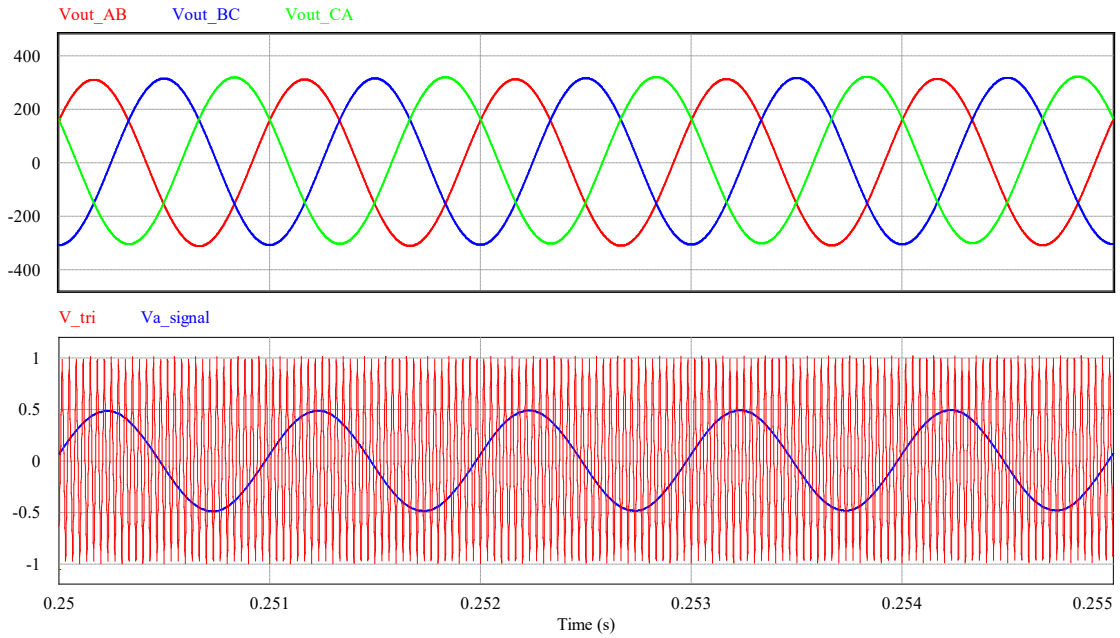


Fig. 3.13 no-load condition, V_{out} = 220 V, f_1 = 1 kHz, THD_V = 0.18%

3.4.2 Rated-load Condition

The same analysis is now made for and output voltage of 220 V, for f_1 = 60 Hz and later, 1 kHz. The results can be observed in Fig. 3.14 and 3.15. For f_1 = 60 Hz, THD_V = 0.24% and for f_1 = 1 kHz, THD_V = 0.22% both values were lower than 0.5%, demonstrating an output signal with high quality and low disturbances.

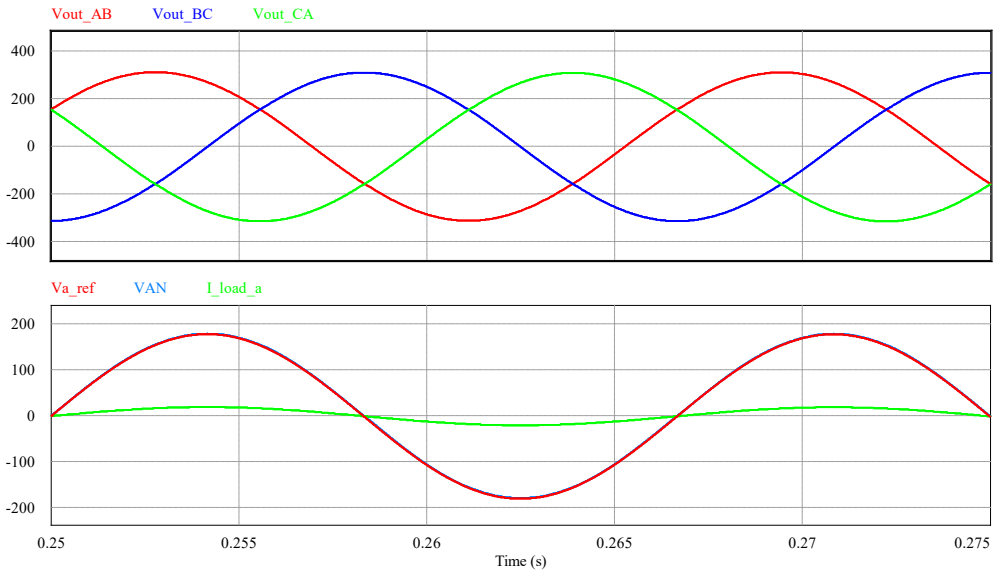


Fig. 3.14 Rated-load condition, V_{out} = 220 V, f_1 = 60 Hz, THD_V = 0.24%

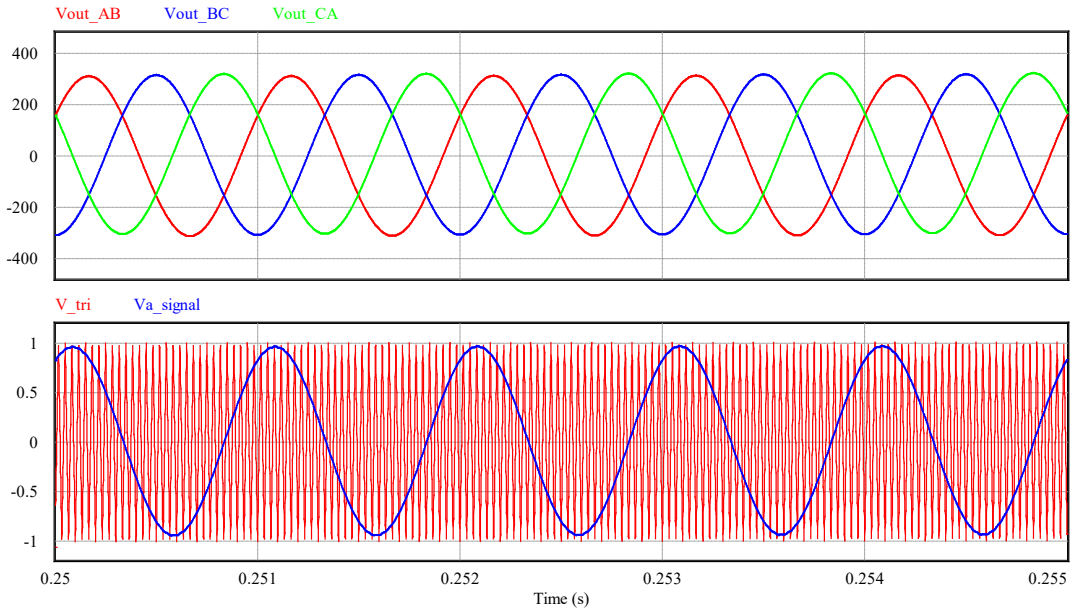


Fig. 3.15 Rated-load condition, V_{out} = 220 V, f_1 = 1 kHz, THD_V = 0.22%

3.4.3 Light-load Condition

A similar analysis is performed for the light-load condition, in which the THD_V levels for a fundamental frequency of 60 Hz was equal 0.16%, and for f_1 = 1 kHz, THD_V = 0.48%, both inside the restriction used to design the LPF (THD_V < 0.5%). This represents the high quality of the output voltage signal.

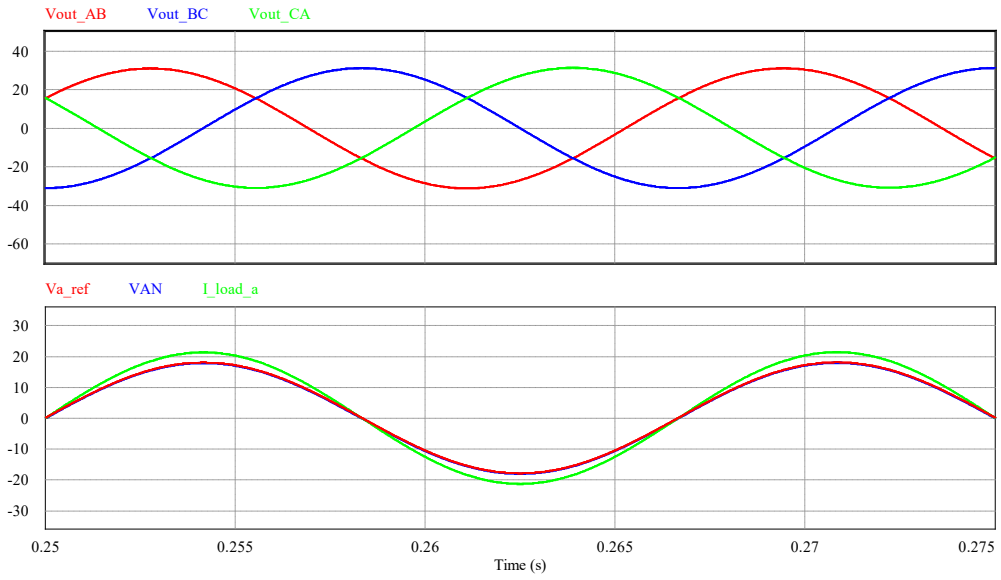


Fig. 3.16 Light-load Condition, V_{out} = 22 V, f_1 = 60 Hz, THD_V = 0.16%

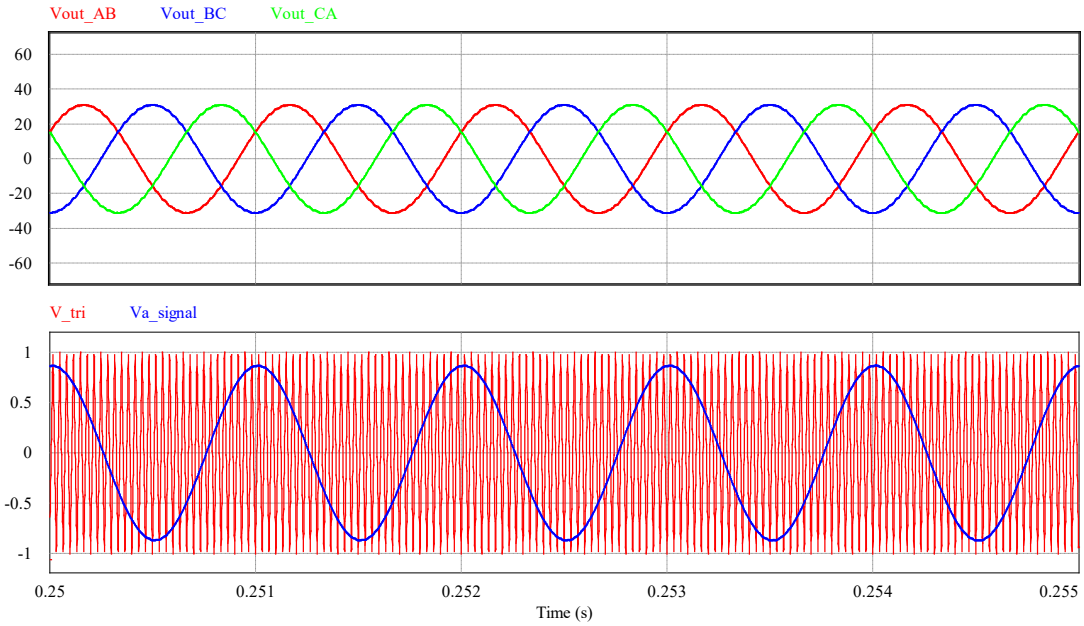


Fig. 3.17 Light-load Condition, V_{out} = 22 V, f_1 = 1 kHz, THD_V = 0.48%

3.5 Load and Reference Voltage Variation

For this scenario, a voltage step was given to the controller from 22 V to 220 V at 0.16666s both set at a fundamental frequency of 60 Hz. Since the system contains only the voltage control loop, the load had to be adjusted at the same time. The result can be observed in Fig. 3.18. It is possible to observe the performance of the controller in tracking and outputting the line phase AB (in red) for the reference given by the blue line. The current, presented on the lower graph, initially at the light-load condition reaches the VSI limit, at 15 A. Once the step is applied, the output power limitation acts on the system and reduced the current to 13.12 A.

The controller presented a fast response during the voltage transient, in which it takes about a quarter of a cycle to return to steady state. Similar results were found for both fundamental frequencies, 60 Hz and 1 kHz.

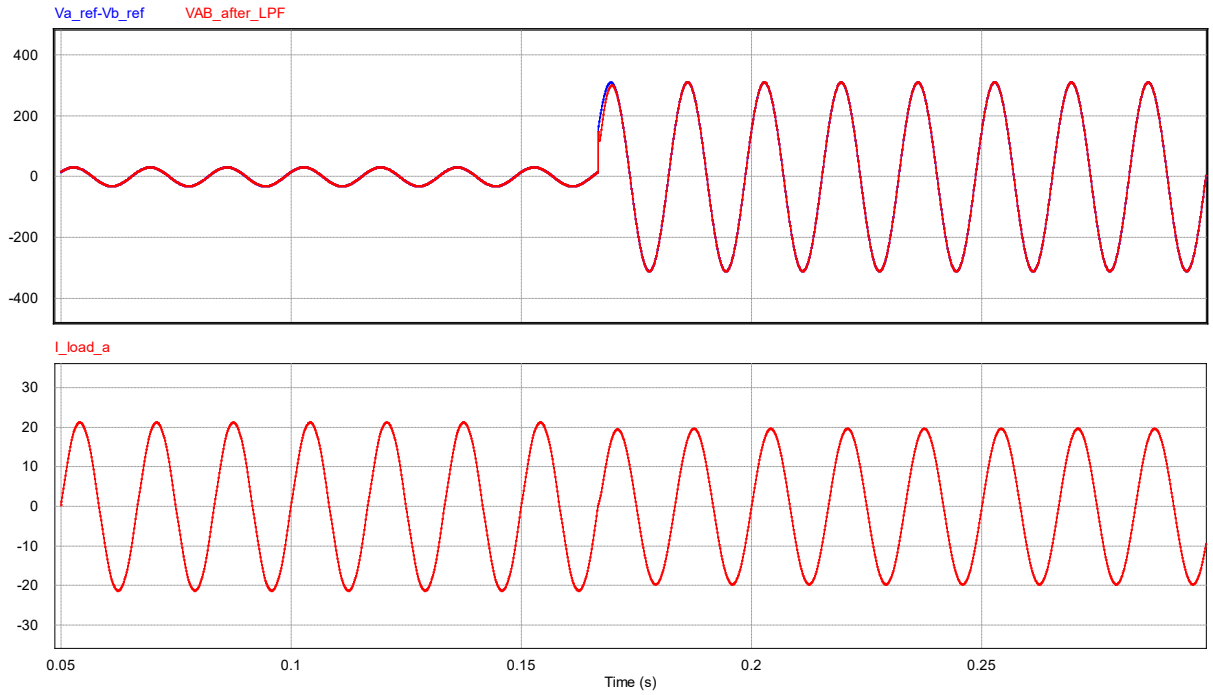


Fig. 3.18 Line voltage output for a varying load condition and f_l=60Hz

Another approach to evaluate the controller dynamic performance is to monitor the reference and sensed/output combined magnitude of the direct and quadrature variables for the reference and output voltage. This makes it possible to look at a single signal, initially converter from *abc* to *dq* and later to a single magnitude signal as shown in Equation (3.19) and (3.20).

$$V_x = \sqrt{\left({V_d}^2 + {V_q}^2\right)} \tag{3.19}$$

$$V_x^* = \sqrt{\left(V_d^{*2} + V_q^{*2}\right)} \tag{3.20}$$

Next, it is possible to observe the dynamic response of the voltage controller, for the output voltage variation and load variation, in Fig. 3.19. The blue curve represents the reference voltage in *dq* coordinates, as in (3.20), while the red one is the actual voltage output, given by (3.19). It is possible to see a small transient response with a small settling time and without any overshoot.

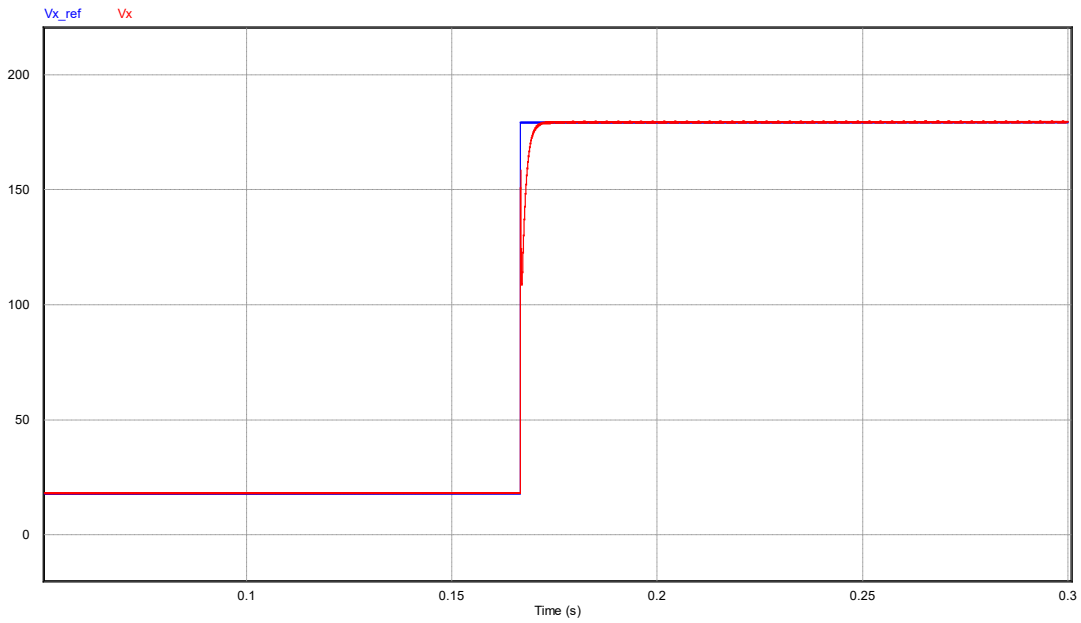


Fig. 3.19 Output voltage variation, from light to rated load and f_1 = 60 Hz

3.6 Filter Capacitor Current Influence

Considering a condition in which it is considered an ESRC = 1 mΩ for the C_{filter}. The current expected to be flowing through the capacitor, can be calculated as follows.

$$I_C = \frac{V}{X_c} = V_\varphi \omega C_{filter} \tag{3.21}$$

$$I_C = 127 \times 2\pi \times f_1 \times 9\mu$$

Therefore, for the minimum and maximum fundamental voltage frequency, there is, respectively.

$$I_{C\_60} = 0.43\ A \qquad I_{C\_1k} = 7.18\ A$$

When f_1 = 60 Hz, the measured value for I_{C_60} = 0.5 A, very close to the expected, and can be observed in Fig. 3.20. For f_1 = 1 kHz, the measured value was very close to the expected, I_{C_1k} = 7.1959 A, as can be observed in Fig. 3.21.

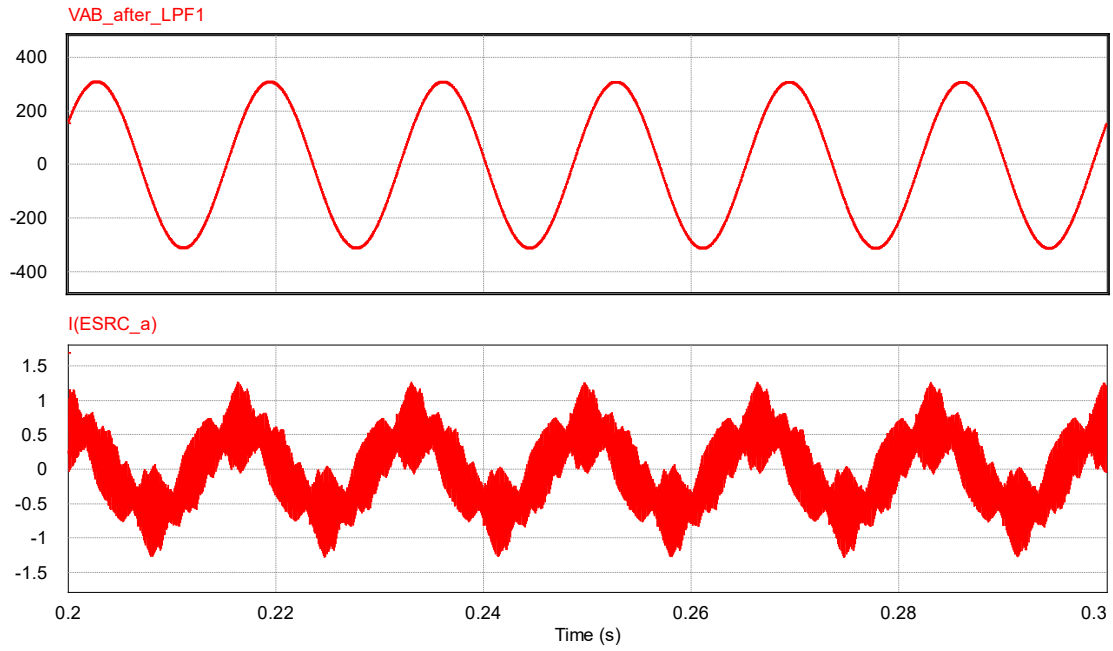


Fig. 3.20 Filter Capacitor current I_{C_rms}= 0.5 A for V_{out} = 220V and f_1 = 60 Hz

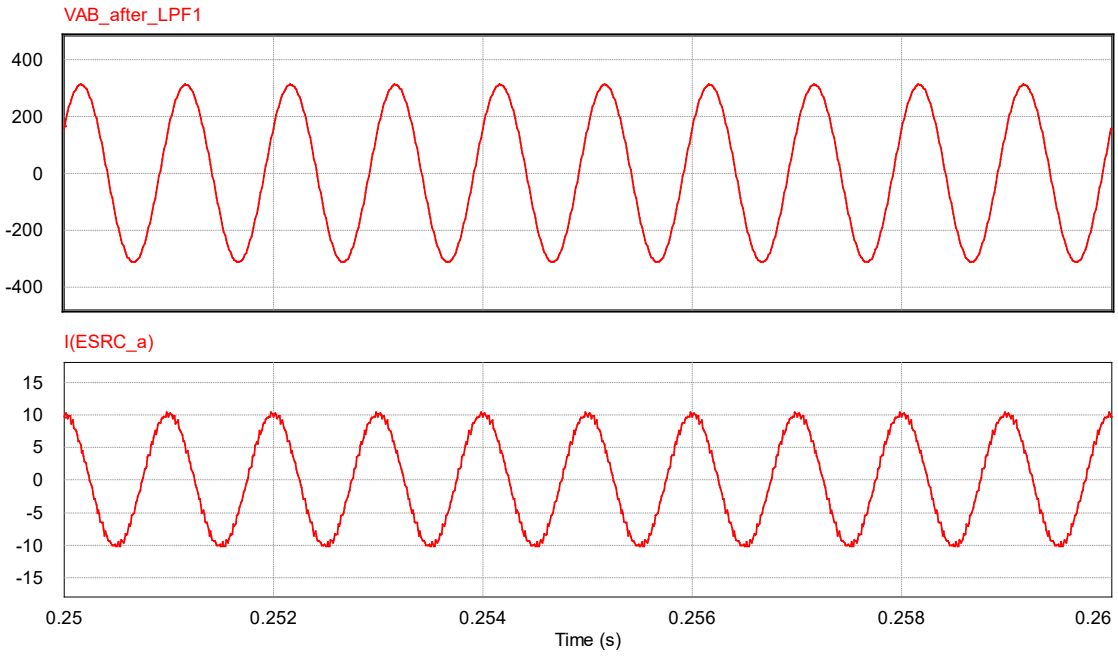


Fig. 3.21 *Filter Capacitor current* I_{C_rms}= *7.1959 A for* V_{out} = *220V and* f_1 = *1 kHz*

Two changes were made here, that make this simulation different from the previous sections. The filter inductor and capacitor were considered as real ones, with parasitic resistances of r_L = 0.5 Ω and r_C = 0.1 Ω, respectively. Although the current in the filter capacitor, for a

fundamental voltage frequency of 1 kHz can be considered high, 7.18 A, the output THD_V levels did not showed any concerning increase. For an output voltage of 220 V, f_1 = 60 Hz, THD_V = 0.13%, and for output voltage of 220 V, f_1 = 1 kHz, THD_V=0.3%, still inside of the restriction levels imposed in this study.

For an output voltage of 22V and f_1 = 60Hz, the expected current in the capacitor is $I_{C\_60} = 0.043\ A$ and the measured one was $I_{C\_60} = 0.083\ A$, the double. The THD_V level was 0.45%. For a f_1 =1 kHz, the expected current was $I_{C\_1k} = 0.718\ A$. And the measured was $I_{C\_1k} = 0.715\ A$. The THD_V = 0.26%. These results are for a rated-load condition. For light-load condition, V_{out} = 22V and f_1 = 1 kHz, I_{c_1k} = 0.75, THD_V = 0.94%, higher than the desired value, but still considered a very low THD_V value.

3.7 Conclusion

A controller was designed to the VSI with an output *LC* filter system under discussion. After the mathematical development of the controller transfer functions, a *dq0* model control was mathematically designed. A Proportional Integrative controller was used and could provide satisfactory results for both steady state and dynamic performance. The performance of the controller was evaluated, through simulations in several load conditions. For all the simulations presented, the THD_V levels were smaller than the restriction imposed in the previous Chapter, of THD_V < 0.5%. The higher value was for a V_{out} = 22 V and a f_1 = 1 kHz that presented a THD_V = 0.48%, and it is the worst condition of operation of the system.

Some tests varying the load were performed, and the results were satisfactory, since the control was able to follow the changes with fast response and inside the limitations imposed, maintaining the current smaller than 20 A, regardless of the load variation. The output voltage was maintained at the desired level as well. Overall, this section could show that the proposed methodology for the filter could reach *L* and *C* values capable to output a high quality output, which was ensured also by the designed controller.

Chapter 4 Efficiency of the Designed System

4.1 Introduction

When the efficiency of a power converter system is discussed, the losses calculation comes directly to mind. Power loss reduction in power converters is one of the main targets in this field to obtain higher efficiency and enhance the devices lifetime, together with the reduction of the temperature stress [42]. The latter is mostly increased by conduction losses and leakage current losses, both considered static losses, which will vary depending on the device technology and switching losses that can be modified with the switching frequency. The maximum achievable switching frequency is strongly dependent on the thermal characteristics of the switches of the VSI system.

This chapter will discuss the major losses present in the system under study where it will be considered switching, conduction losses, and the losses in the passive components that together compose the output filter. The total losses of the inverter system will be estimated and so the efficiency of the system can be evaluated.

4.2 System Losses

The switching losses, which includes the turn-on, turn-off, reverse recovery and driving stages are an important source of the losses in the inverter, and should be computed. The switches also have intrinsic parasitic capacitances that varies accordingly to the physical size of the switch, if the size increases the capacitance also increases [43] – [45]. At each switching cycle, this capacitance stores and consumes energy. The losses are, then, proportional to the switching frequency, the parasitic capacitances values and the size of the device.

By analyzing the strategies to make these losses smaller presented in the literature [15] - [23], [32]-[33], [38], it can be observed that a tradeoff between switching losses and output current quality occurs. It can be summarized that the switching losses depend on the value of the current and voltage to be switched in the device as on the number of commutations. Then, the main idea behind some others strategies is to reduce the number of commutations of the power electronics devices during the modulation cycle [34], whereas there is a compromise between the number of commutations and the *rms* value of the output current ripple when the switching frequency changes that must be considered.

Some strategies to reduce switching losses are well-known in the literature, as soft-switching techniques (reducing voltage or current of the switch during commutation), the use of advanced gate drives that will vary the switching time interval or even modulation and switching frequency variation techniques (changes the number of commutations in the fundamental period of the output current) [8], [39]. Although all these techniques have the benefit of cooperate with the reduction of switching losses, they also have some detriments, as for the soft switching and advantage gate drives strategies, they reduce the reliability of the system by adding extra complexity through hardware and control. This section is focused on the estimation of the system losses under a regular and continuous SPWM modulation. Other modulation techniques will not be applied. Another strategy is to vary the switching frequency by lowering it, which would reduce the switching losses, but in the other hand, will reduce the output current quality, which may increase the losses in the output [44]. That explains the decision made on Chapter 2, when the parameters of the system are not sufficient to achieve the imposed objectives, the switching frequency is increased and not decreased, as was presented in the Flowchart from Fig. 2.6.

4.2.1 Switches Losses from SEMISEL Software

To estimate the switching and conduction losses present in the designed system, at first, it was used an online application provided by Semikron, known as SEMISEL, where the specifications of the desired system are inserted (V_{in}, V_{out}, I_{out}, P_{out}, f_{sw}, among others) and a device that will be able to operate accordingly with the chosen conditions is suggested. For the case under study, it was the SEMITOP SK20GD066ET*, which is represented by Fig. 4.1 with the main parameters presented in Table 4.1. The datasheet can be observed in the Appendix. Another input for the system is the profile and the size of the heatsink to be used with the switches. The type of cooling is also taken into account and it can assume the following configurations: natural-cooled and air-forced.

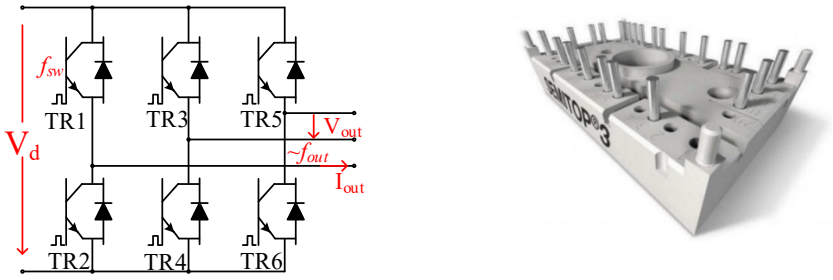


Fig. 4.1 *Semikron Device SK20GD066ET**

Table 4.1 Main parameters of Semikron module SK20GD066ET

Parameter	Condition	Value
V_{CES} – Forward Voltage	Tj = 25°C	600 V
I_C – Forward Current	Tj = 175°C	30 A
V_{GES} – Gate Emitter Voltage		± 20 V
I_F – Diode Forward Current	Tj = 175°C	31 A
r_{ce} – Parasitic Series Resistance	Tj = 25°C	37.5 mΩ
	Tj = 150°C	52.5 mΩ
*All other parameters are found in the Appendix and on the datasheet of the module SK20GD066ET		

The application also provide a calculation of the losses and temperatures with rated current, considering both 60 Hz and 1 kHz as fundamental components of the desired outputs, maintaining a fixed switching frequency of 30 kHz, as is presented Table 4.2. Where P_{cond} is the conduction loss in the IGBT transistor and in the reverse diode, respectively; P_{sw} is the switching losses in the same both devices; and P_{total} is the total loss for the switching and conduction part of the system.

Table 4.2 SEMISEL/Semikron provided loss estimation

Type of Loss	*Calculated Loss (W)*
P_{cond_tr}	8.76
P_{sw_tr}	11
P_{tr}*	19
P_{cond_d}	1.25
P_{sw_d}	1.03
P_d*	2.29
P_{total}**	130

*for one switch
**for the six-pack of switches

For the application to provide a correct output, a heatsink has being selected so that the chosen switch does not exceed its maximum junction temperature. For the SK20GD066ET* this value should not exceed 175°C. After a few simulations, the Semikron P14/120 was chosen. Fig.4.2 shows the profile of the heatsink. Table 4.3 presents its details. A forced air-cooling was considered with the rate of 80 m^3/h.

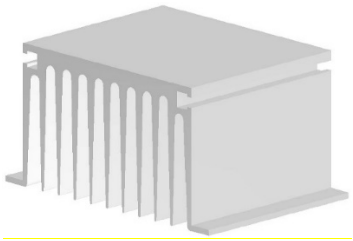


Fig. 4.2 Profile of Semikron P14/120 Heatsink

According to these, the estimated losses from the switches would be a total of 130 W, considering rated current condition, which corresponds to less than 3% of the total power of the system. The SEMISEL application also takes in consideration elements e.g. ambiance temperature, a predefined heatsink that fits the application and different types of cooling.

Table 4.3 Cooling Device Characteristics

Cooling	
Ambient Temperature	40 *ºC*
Number of switches per heat sink	6
Number of parallel devices on the same heat sink	1
Additional power source at this heat sink	0 W
Predefined SK-Heat Sink	P14_120
Correction factor	1
Forced Air Cooling, Flow Rate:	85 m^3/h
$R_{th(s-a)}$	0.110 K/W

From the SEMISEL software, it is also provided a curve of the characteristic temperature during an overload situation in order to guarantee that the selected device will not surpass a secure temperature of operation, as can be observed in Fig. 4.3. The green curve represents the evolution for the junction temperature of the IGBT's transistor initially during a 25% overload for 10 s and later for rated conditions, and the blue curve shows the same temperature analyses for the IGBT's diode. Both temperatures were below the maximum junction temperature of the module, of 175°C, so the chosen profile of heatsink has a thermal resistance small enough for the system. Table 4.4

presents the temperature magnitudes for each part of the device and for the curve with small boxes, the case temperature, witch stays around 55° even with the overload condition.

Table 4.4 Estimate Temperatures for rated current condition and overload

Part of the Device	Case/Junction Temperature for Rated Current Average values (^oC)	Case/Junction Temperature for Overload Condition Average Values (^oC)
T_{case}	54	55
$T_{transistor}$	92	106
T_{diode}	60	62

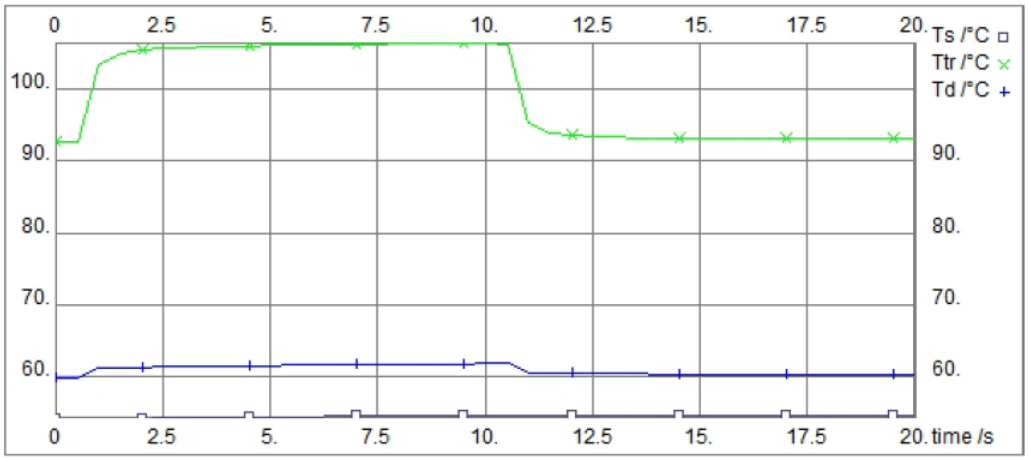


Fig. 4.3 *Temperature Characteristic during overload*

4.2.2 Computation of System Losses using PSIM

The next step is to simulate the system with the parameters given by the SK20GD066ET datasheet, to verify if the losses presented will be similar to those found with the SEMISEL software. For this verification, some values were added, and they will bring the simulated system closer to a real system, increasing its fidelity. The values are the saturation voltage (V_{sat}), IGBT conductive resistance (R_{cond}), diode forward voltage (V_{fwd}) and resistance of the diode (R_d). Those can be seen as a combination of parameters that can simulate the switching and conduction losses of the inverter.

In addition to the parameters added to the IGBT, the ESR from filter capacitor and the parasite resistance from the filter inductor are included. The minimum load is consisted as a

damping resistor that is always be connected to the system and it will be seen as a loss in the system for any other operational point.

4.2.3 Rated load and fundamental frequency condition

In Fig. 4.4 and 4.5, it is possible to observe the input and output power of the system, and the losses that occur in intermediate components as switches, capacitors and inductors. The first condition chosen to be demonstrated is the one with rated-load, with a fundamental frequency of 60 Hz. Even though, other limit conditions will be presented, e.g. for light-load and higher frequency, load conditions were verified and the results will be presented in Table 4.4. In Fig. 4.4 (a), the red curve represents the actual curve of the input power, given by the input current and the V_{DC} voltage, while the blue curve is the average of the red curve over the fundamental period. As the system is balanced, the output power is calculated considering three times the single-phase voltage and current. Once again, in red, the actual waveform of the output power and in blue its average, as presented in Fig. 4.4 (b). It is possible to observe an average value of 5.43 kW for the input and 5 kW for the output power.

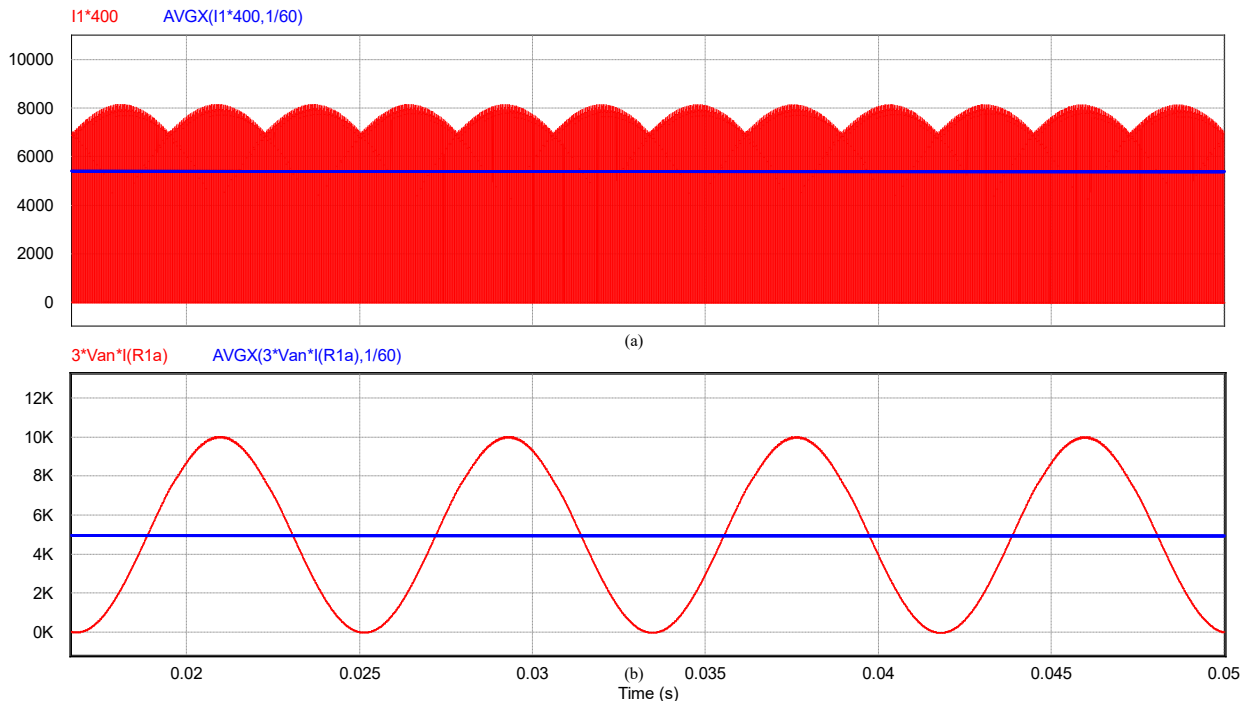


Fig. 4.4 Results for Rated-load condition, f_1=60Hz, (a) Input Power and (b) Output Power

Fig. 4.5 is divided in three representations, the first presents the losses in all the six switches, losses here considered as switching and conducting losses. The second and third representations are the resistive losses on the passive filter components, *C* and *L*, respectively. In red, there is the actual waveform of the dissipated power and in blue, the average of each waveform over the fundamental period. The filter capacitance losses are so small that can be considered neglectable while the filter inductance has an impact of around 3% on the total losses of the system.

As a result, from the difference from the input to the output power, there is 430 W, which represent the losses on the system. The switching losses shown in Fig. 4.5 (a) adds up a value of 105 W, both *L* and *C* parasitic resistive losses add up another 3W approximately. The remaining 322W are losses on the *damping* resistor, responsible for providing the minimum load for the system in the case that no load is connected. Fig. 4.6 show the distribution of losses for a 60Hz output with rated-load (220V) and light-load (22V).

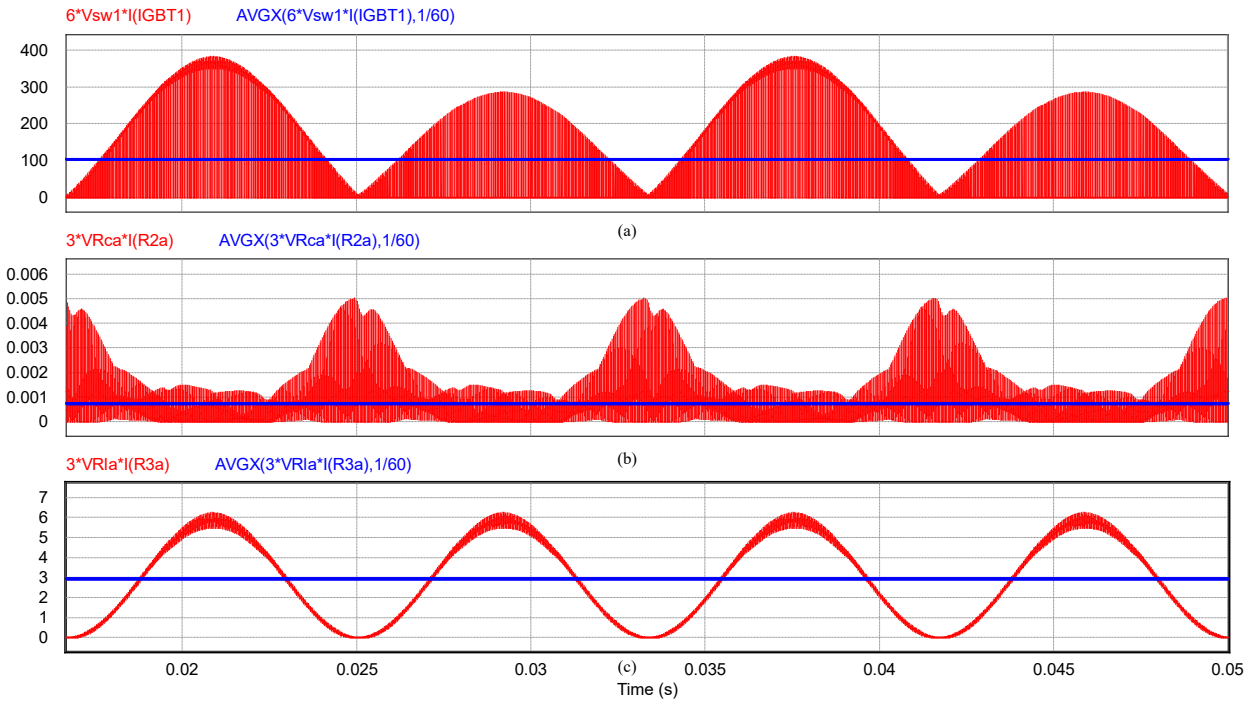


Fig. 4.5 Results for Rated-load condition, f_l=60Hz, (a) switch losses; (b) resistive losses in the filter C and (c) resistive losses in the filter L

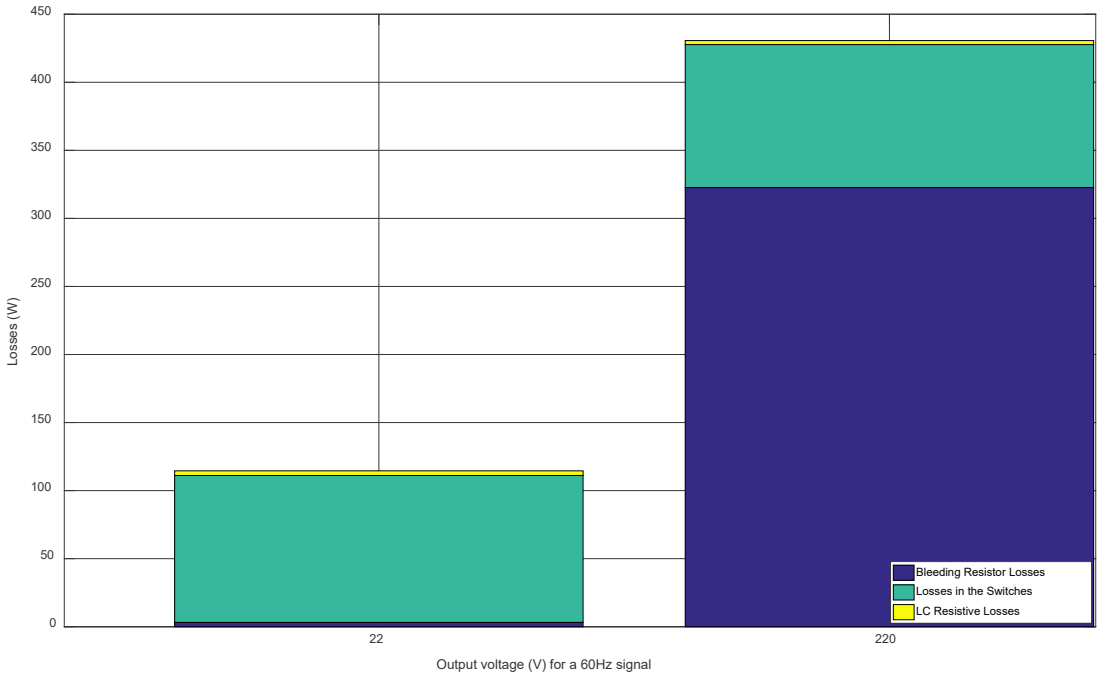


Fig. 4.6 *Distribution Losses for* f_1*=60 Hz and* V_{out}*=22 and 220 V*

4.2.4 Rated load-condition and high fundamental frequency

The same representations are now presented for a fundamental frequency of 1 kHz, since there is the concern about maintaining the system in similar efficiency levels during all operational range of this study. In Fig. 4.7 it is presented the input and output power, at the average level of 5.5 kW and 5 kW, respectively (blue curve). Fig. 4.8 indicates the losses in the switches and in the filter components, respectively, and similar assumptions can be made, as the filter capacitance almost does not influence in the total loss estimation.

In this second condition, the difference from the input to the output power is 448 W, representing the total losses on the system. The switching losses shown in Fig. 4.8 (a) adds up to 121 W, both *L* and *C* parasitic resistive losses add up another 4 W approximately. The remaining 323 W are losses on the *damping* resistor, responsible for majority of the losses in the system for this condition as well. Fig. 4.9 show the distribution of losses for a 1 kHz output with rated-load (220V) and light-load (22V).

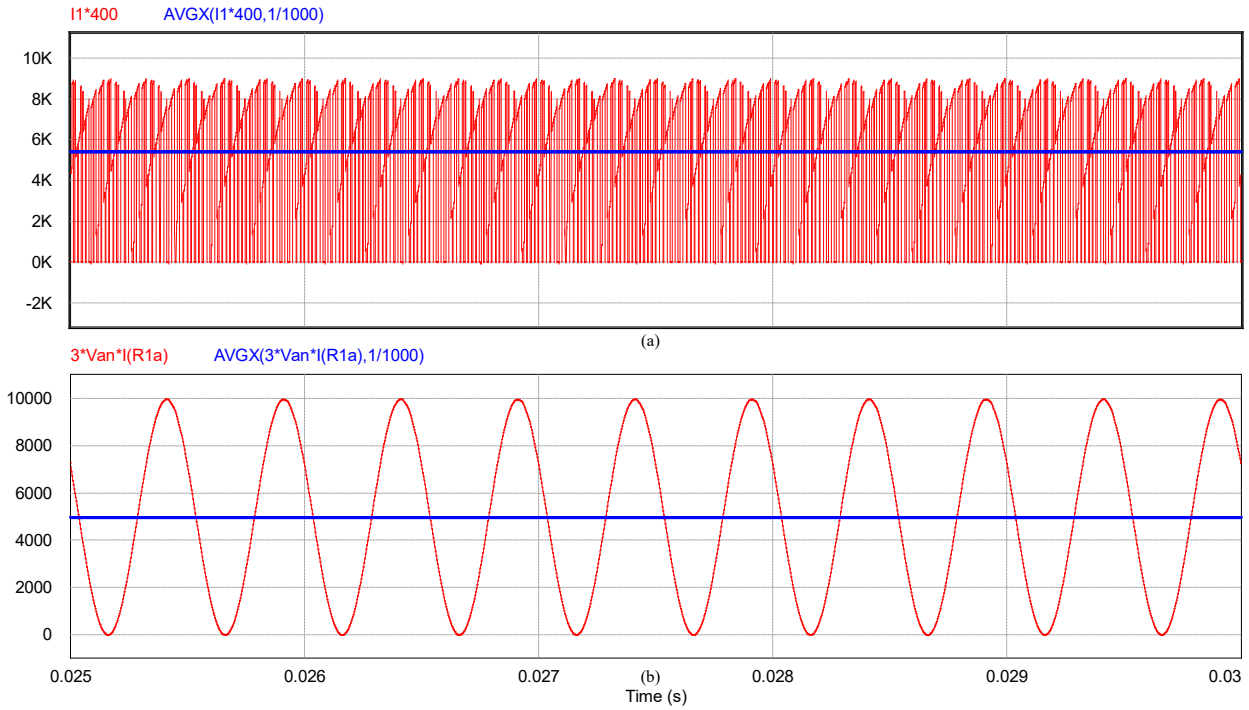


Fig. 4.7 Results for Rated-load condition, f_1=1 kHz, (a) Input Power and (b) Output Power

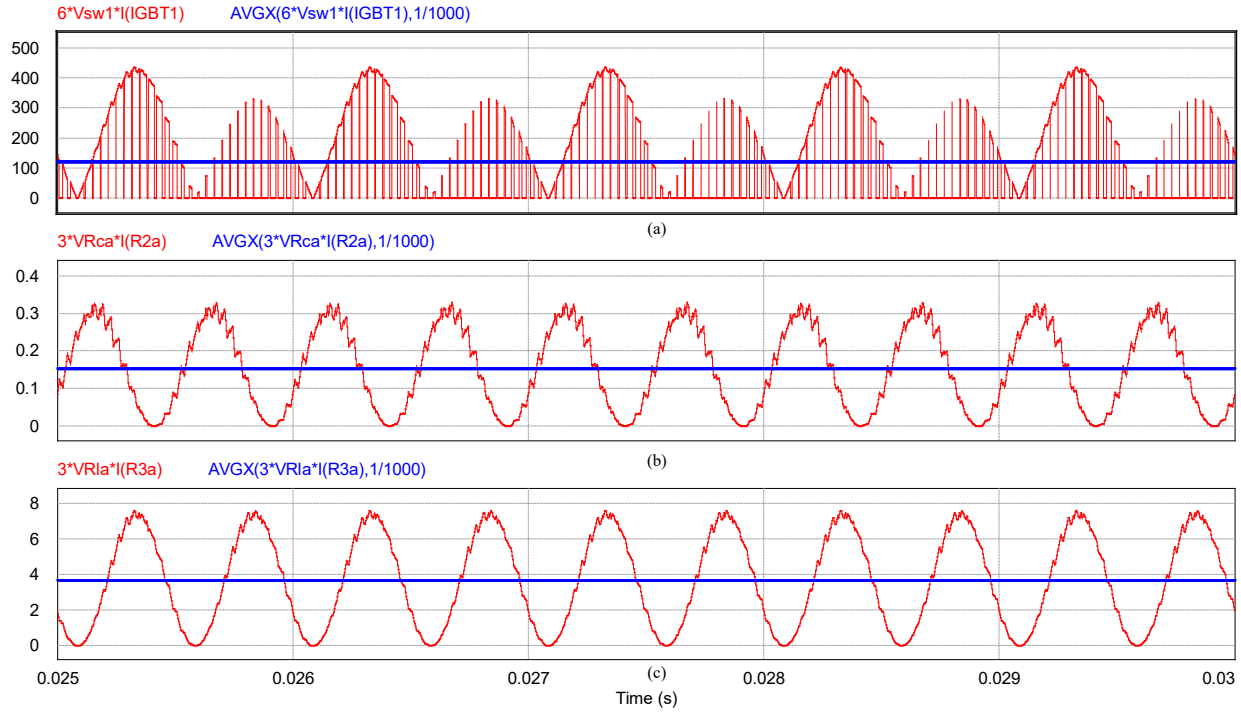


Fig. 4.8 Results for Rated-load condition, f_1=1 kHz, (a) switch losses; (b) resistive losses in the filter C and (c) resistive losses in the filter L

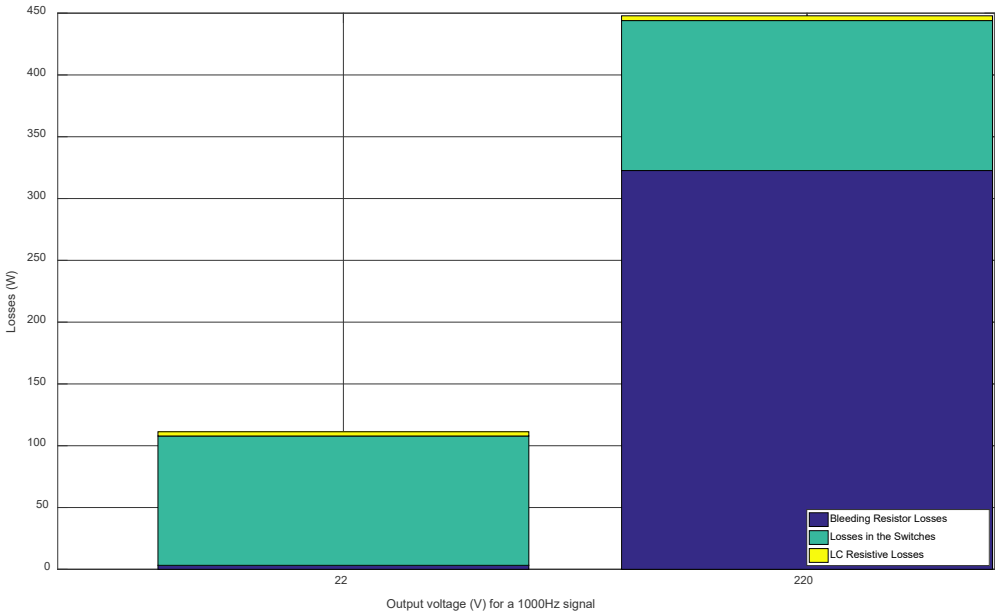


Fig. 4.9 *Distribution Losses for* f_1*=1 kHz and* V_{out}*=22 and 220 V*

4.2.5 PSIM and SEMISEL Comparison

The models used in SEMISEL presented slightly higher losses magnitudes and that should be because they are more accurate since they take in consideration more variables while the models in PSIM consider only the transistor and diode resistance and its saturation/drop voltages. SEMISEL also includes the parasitic capacitances between collector, emitter and gate and the required energy spent to turn-on and off the switches. Nevertheless, the PSIM models are very reliable and presented results that can be considered accurate and according to the estimated by the application from Semikron. For both conditions under study, SEMISEL outputted 130 W of losses, considering both switching and conduction losses. PSIM on the other hand outputted a 105 W for the 60 Hz output and 121 W for the 1 kHz output, an error/difference of 20% and 7% respectively.

4.3 Efficiency of the designs

As could been observed in the previous section, the damping resistor has an important impact on the losses of the system, when the system is operating near to the rated-load. As the load decreases in direction of lighter loads, the switching and conduction losses are the main responsible for the losses. This affects the system output efficiency, which has its values represented in Table 4.4, for the rated, half-load and light-load conditions.

Table 4.5 Total System Efficiency

V_{out} (V)	f_1 (Hz)	Switching/conducting losses (W)	Output Filter losses (W)	**Damping Resistor Losses (W)**	Total system efficiency (%)
220	60	105.03	2.94	322.68	92.07
	1 k	121.34	3.87	322.66	91.78
110	60	114.37	3.56	80.65	93.50
	1 k	118.40	3.76	80.66	93.37
22	60	107.91	3.41	3.22	83.31
	1 k	104.66	3.42	3.22	83.70

Fig. 4.10 presents the overall system efficiency when operating from rated to light-load condition, for the fundamental frequencies of 60 Hz and 1 kHz. It can be observed that the system presents a slightly higher efficiency when operation in lower frequency. The peak efficiencies for both curves are reached around 50-60% of the load.

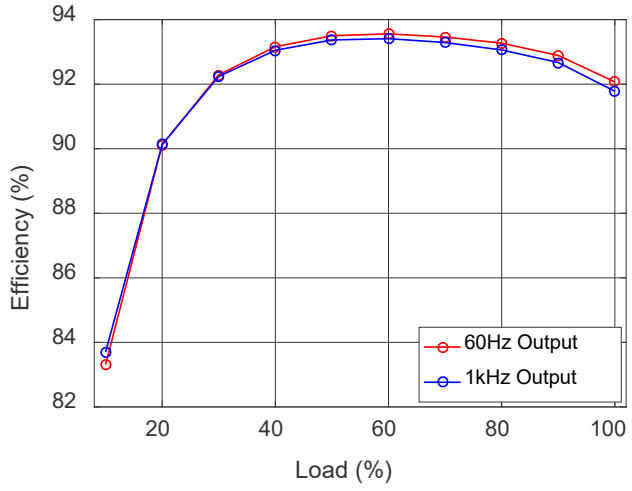


Fig. 4.10 *Overall System Efficiency*

4.4 Power Density Estimation

Power density is a concept that is highly impacted by the evolution of components (new technologies, smaller, for higher frequencies and with lower losses) and new switching techniques [40]. As presented in [36] and shown in Fig. 4.11, the tendency in the future is a reduction in every one of the aspects of Losses, Volume, Weight and Costs.

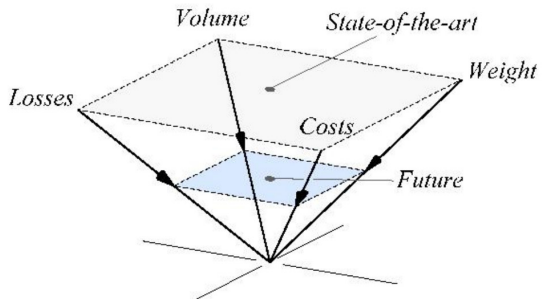


Fig. 4.11 Development trends in power electronic converters [36]

Each one of these categories is related to one of the called Figures of Merit [37], usually used to evaluate and compare power electronic converters. Power Density is defined as the ratio between the output power and the volume and it is expressed as kW/dm^3 [41]. Specific power is the relation between the output power and the weight (kW/kg). Relative cost is the ratio between the output power and the overall cost (kW/$) and lastly the Relative Losses is the ratio between the output power and the converter losses (W/W or %).

In this section, a brief study on power density will be presented. For that, the components previously used in this study will be arranged in a layout as presented in Fig. 4.12. The heatsink is the dark grey block and the PCB is the green block. The IGBT pack is the one in light grey. Inductor are represented by the yellow block, while the capacitors are shown in the blue blocks. Lastly, the red blocks represent the damping resistor. Each component will be detailed in Table 4.5.

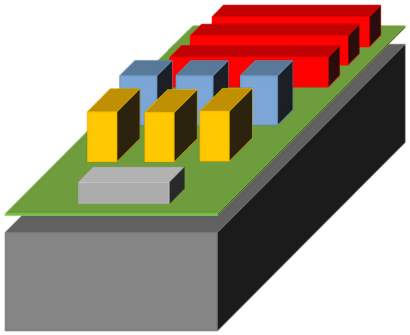


Fig. 4.12 *Suggested Layout*

Considering an output power of 5kW, the power density reaches approximately 1.4kW/dm^3. Comparing to the converters under study in [36], this is a low power density, but a few reasons can be used to explain. First, the suggested layout is only a preliminary version for a future setup. The heatsink was extended up to the end of the layout to dissipate the power from the damping resistor but this project is not optimal since it was not model. Secondly, usually converters have control strategies that can keep the system stable for no-load conditions so there is no need for the damping resistor. Just an estimative of removing them and the reducing the heatsink only for the IGBT pack would almost triple the power density.

Table 4.6 Component Characteristics for Power Density Estimation

Components	*Part number*	*Dimensions (dm x dm x dm)*	*Volume (dm^3)*	*Total Volume (dm^3)*
Switches Pack	SK20GD066ET	0.31*0.5*0.16	0.0248	0.0248
Inductor (unit)	B82747S4203A20	0.6 (diameter) x 0.28	0.079166	0.237497
Capacitor (unit)	B32676G6106K000	0.41 x 0.28 x 0.4	0.04592	0.13776
Damping Resistor (unit)	HSC150150RJ	0.98 x 0.47 x 0.26	0.119756	0.359268
Heatsink	P14/200	1.45 x 0.75 x 2.5	2.71875	2.71875
PCB	Custom	1.45 x 2.5 x 0.03	0.10875	0.10875
Total				3.5775

4.5 Conclusion

The importance of estimate the losses of power converter are clear since they will define the efficiency of the converter system. Through the analysis of the results provided by the software SEMISEL and the simulations performed by PSIM, it could be verified the good performance of the system with the parameters proposed by the designed LPF procedure. For rated conditions of load and fundamental frequency, the system operated with an efficiency of 92.07%. For a condition of light-load and high frequency, the system still provides a magnitude of above 83% of efficiency. The damping resistor is the main responsible for the losses when the system operates in rated load and the same is valid for the losses in the switches when operating with lighter loads. If the damping resistor is removed, the losses in the system can be reduced considerably. The overall system efficiency could go up to 98% with this measure, although a study to ensure the stability of the system without load has to be evaluated.

Chapter 5 Conclusion and Future Work

5.1 Conclusion

In this work, the main issues concerning the design of a second-order LC-LPF for a VSI operating with SPWM with a wide range of output power, voltage and frequency with extremely low harmonic distortion were discussed. Then, a systematic procedure for designing such a filter was described. The performance of the proposed approach was verified by means of mathematical modeling and simulation, the latest, through MATLAB software. It was also taken in consideration how the load influences the performance of the LC-LPF. It was verified that the load has a significant impact on the calculation of the attenuation of the LC-LPF, depending on the region that it is being analyzed. The load heavily affects the damping factor and light and heavy loads push the gains of the transfer functions up and down.

The proposed procedure to design a LC-LPF was still able to provide the desired voltage to the load by changing the modulation index and magnitude of the fundamental component that is applied to the LPF. While eliminating higher frequencies harmonics the LC-LPF sometimes promoted gains and attenuation for the fundamental component of the output, so a strategy to apply a compensated modulation amplitude index was also develop. On this study, the input parameters were analyzed and put to test under the necessary conditions of operation with the objective of assuring a low level of THD_V. Each case was simulated considering three scenarios, an ideal one, one considering a dead time insertion between switches places on the same inverter leg and lastly one considering a conductive resistance in each switch, what generated voltage drops on the switches while conducting. It could be observed the different responses of the system for each imposed situation. While the insertion of the switch resistance hardly affected the output, the input of dead time affected the system lowering the voltage level by 3% and introducing certain phase to output when compared to the ideal system.

Although the harmonic levels in the case of light-load and higher frequency, was slightly above the imposed restriction, the content of THD_V presented in the output voltage is still very low, since it is less than 1%. In addition to that, these nonlinearities or losses were not included and considered for the procedure of the filter design. The ideal case on the other hand had always respected the limits. Therefore, it can be said that the proposed design procedure accomplish its

purpose for the parameter definition presented, demonstrating its great capability to be implemented for other conditions outlines.

The next chapter had as objective to design a control loop that would be suitable for all the conditions of operation and that would bring the output harmonic levels to the desired magnitude and the fundamental automatically for the right value, correcting any gain or attenuation caused by the filter. It came the necessity of a *dqo*-model control that was mathematically developed and designed, considering a simple voltage controller. The design of the entire controller was presented containing voltage loop control, using PI blocks to compensate the error. After the design of the controller, a performance evaluation was made, in which three main load cases were evaluated, light, rated and minimum load condition. For these conditions, the THD_V levels were kept under the imposed restriction of 0.5%, demonstrating the capability of the controller designed to respect the low harmonic content level desired. The control also showed satisfactory response to load and voltage and current variations. A methodology for evaluation the variation of the voltages due to the steps using a single variable, *Vx*, was used as the combined magnitude of *Vd* and *Vq* both for sensed and reference voltages. The designed control presented good results while operating in a 3-phase VSI system with the LPF previously designed.

A complete chapter was developed regarding the system losses estimation. Initially the study of the losses was performed by a software provided by Semikron to calculate the switching and conduction losses. This losses were compared to the ones found in PSIM, were the resistive components and threshold voltages were inserted to the switches. In addition to that, the resistive losses on capacitors, inductors and on the minimum load (damping resistors) were evaluated on PSIM. A peak efficiency around 94% was reached around 50 to 60% of the load, for a line voltage output of around 110V. If the damping resistor could be removed the efficiency could go up to 98%, since it was observed that the damping resistor was the main responsible for the losses during rated operation and that by removing it from the system would increase the overall system efficiency.

A power density study was performed on a suggested layout of the converter, to evaluate the ratio between the output power of the system with its volume. This was an initial study with the objective of identifying design bottlenecks that could be improved in order to achieve higher power densities.

5.2 Future Work

As a future work the main contribution should be the experimental validation of the system, what would verify the efficacy of the proposed filter design procedure for low THD_V outputs. In addition, the proposed procedure can be expanded for a larger limit of operation. An important improvement for the system it would be if it could automatically detect the optimal increments for the capacitor, the inductor, the resonant and switching frequency. Also, the proposed procedure could include other topologies than the 3-phase VSI.

Others modulation techniques should be studied and their relation with the losses of the system can bring more benefits to the system. Although this system has some very singular restrictions, since it presents a very wide range of output power and mostly switching frequency, these techniques would have to be carefully evaluated. The one that was mostly presented in the literature and seems to better fit this system, at first, would be the discontinuous SPWM followed by a Variable Switching Frequency (VSF). Therefore, as a next step in this research, it would be the study and performance evaluation of the application of this two, and other more in the future, modulation techniques in the system under study, to verify which one presents the most relevant results regarding losses reduction and converter efficiency.

In the power density analysis, it was suggested a first layout that is only a preliminary version for a future setup. The heatsink was extended up to the end of the layout to dissipate the power from the damping resistor but this project is not optimal since it was not model. Therefore, this is an important study to be made in the future.

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APPENDIX

A.1. Resistance values used in simulation in Chapter 2.

Table A1. Resistance values for all the output voltage range.

Resistance #	Resistance value (Ω)	Output voltage (V_{LL})
R_1	0.8468	22 V
R_2	1.2702	33 V
R_3	1.6936	44 V
R_4	2.1170	55 V
R_5	2.5403	66 V
R_6	2.9637	77 V
R_7	3.3871	88 V
R_8	3.8105	99 V
R_9	4.2339	110 V
R_{10}	4.6573	121 V
R_{11}	5.0807	132 V
R_{12}	5.5041	143 V
R_{13}	5.9275	154 V
R_{14}	6.3509	165 V
R_{15}	6.7742	176 V
R_{16}	7.1976	187 V
R_{17}	7.8408	198 V
R_{18}	8.7362	209V

A.2 Matlab Code for the LPF design

```
clear all
close all
clc

%%%%%%PARAMETERS DEFINITION:

%INPUT PARAMETERS:
Vdc = 400;
Vll = [22:11:220];
Prated = 5000; %output power
%incrementation of the switching frequency
fsw_initial = 29000; %switching frequency
fsw_inc = 1000;
fsw_final = 30000;
Vfsw = [fsw_initial:fsw_inc:fsw_final];

%determination of the cut off frequency of the filter(start with one decade
bellow the fsw)
fi = 1600; %initial frequency value
finc = -100; % 5% of increment
ffinal = 1500; %final value of fres that can be applied
Vfres=[fi:finc:ffinal];

kk=1;
while kk<length(Vfsw)+1;
        fsw=Vfsw(kk);
ff=1;
while ff<length(Vfres)+1;
    fres=Vfres(ff);
    sprintf('Currently testing the system for a fres of (%f k)and a fsw of
(%f k)',0.001*fres, 0.001*fsw)
Ci = 8e-6; %initial value for Capacitance
Cinc = 1e-6; %incrementarl value for Capacitance
Cf = 100e-6; %final value of Capacitance
VC=[Ci:Cinc:Cf];

aa = 1;
while aa<length(VC)+1;
    C=VC(aa);
    L = 1/(C*(2*3.1415*fres)^2); %the L of the LC filter is given by:

%DEFINITIONS:
Ir=15; %rated current = maximum inductor current
LineVoltage = transpose (Vll);
Vlim=(Prated/(sqrt(3)*Ir));
tri = 1; %1 for 3-phase systems, 0 for 1-phase.
f1_g =[1 60 300 420 540 660 780 900 1000]; %group of fundamental frequency

%TO FIND THE LOAD RESISTANCES FOR THE DIFFERENT VALUES OF V_LL:
icur=1;
while icur<length(Vll)+1;
    if Vll(icur)<Vlim;
```

```
        I(icur)=Ir;
    else
        I(icur)= (Prated/(sqrt(3)*Vll(icur)));
    end
    P(icur)=(sqrt(3)*Vll(icur)*I(icur));
    R_initial(icur) = ((Vll(icur))/(I(icur)*sqrt(3)));
    R(icur)=((R_initial(icur)*150)/(R_initial(icur)+150));
    icur=icur+1;
end

Resistance = transpose(R);

%TO COMPUTE THE BODE PLOT:
ll=1; %Resistor counter
% figure;
while ll<length(R)+1;

%the damping factor is defined as:
E(ll)=((1/(2*R(ll)))*(sqrt(L/C)));
DampingFactor = transpose(E);

 %the transfer funtion of the LC filter is gien by: Gn = (1/LC)/(s^2 +
(1/RC)s + (1/LC))
 A = [0 0 (1/(L*C))];
 B = [1 (1/(R(ll)*C)) (1/(L*C))];
 Gn = tf(A,B);

%  opts = bodeoptions;
%  %opts.MagUnits = 'abs'
%  opts.FreqUnits = 'Hz';
%  bodeplot (Gn,opts)
%  hold on;
%  grid on;

 %varying the frequency in intervals of 60Hz:
 fl=[1:1:1000000]; % this interval must be "big" enough
 wl=fl*2*3.1415;
 [MAG2(:,ll),PHASE2(:,ll)] = bode(Gn,wl);

 ll = ll+1;

end

%
%legend('R1=0.847','R2=1.270','R3=1.694','R4=2.117','R5=2.540','R6=2.964','R7
=3.387','R8=3.811','R9=4.234','R10=4.657','R11=5.081','R12=5.504','R13=5.927'
,'R14=6.351','R15=6.774','R16=7.198','R17=7.841','R18=8.736','R19=9.680');
%
legend('V1=22V','V2=33V','V3=44V','V4=55V','V5=66V','V6=77V','V7=88V','V8=99V
','V9=110V','V10=121V','V11=132V','V12=143V','V13=154V','V14=165V','V15=176V'
,'V16=187V','V17=198V','V18=22V','V19=220V');
% set(gca,'FontSize',22)


%%%%%%%%FUNDAMENTAL VOLTAGE ANALYSIS/m_a COMPENSATION:
```

```
%m_a theoretical:
ii=1;
jj=1;
while ii<length(I)+1 & length(Vll)+1
    ma_new(ii)=(Vll(jj)/245);  % to find the ma to each line voltage
    ii=ii+1;
    jj=jj+1;
end

%FREQUENCIES IN WHICH THE HARMONICS WILL APPEAR:
zz = 1; %fundamental frequency counter
while zz < length(f1_g)+1;

f1 = f1_g(zz);
mf = fsw/f1;

%real frequency of the 16 lines of harmonics - definition of in which
frequencies the harmonics are appearing
d1 = round((mf*f1),0);
d2 = round((mf-2)*f1,0);
d3 = round((mf-4)*f1,0);
d4 = round((mf-6)*f1,0);
d5 = round((2*mf-1)*f1,0);
d6 = round((2*mf-3)*f1,0);
d7 = round((2*mf-5)*f1,0);
d8 = round((2*mf-7)*f1,0);
d9 = round((3*mf)*f1,0);
d10 = round((3*mf-2)*f1,0);
d11 = round((3*mf-4)*f1,0);
d12 = round((3*mf-6)*f1,0);
d13 = round((4*mf-1)*f1,0);
d14 = round((4*mf-3)*f1,0);
d15 = round((4*mf-5)*f1,0);
d16 = round((4*mf-7)*f1,0);

d = [d1, d2, d3, d4, d5, d6, d7, d8, d9, d10, d11, d12, d13, d14, d15, d16];
%it organizes the frequencies, in lines

 mm = 1; %counter of the harmonic frequencies from 'd'
 ll = 1; %Same resistor counter
 while mm<length(d)+1;
     ll=1;
     while ll<length(R)+1
 %frequency desired (for example: m_f-2 or 2m_f+1, etc..)
 gain(mm,ll) = round(MAG2(d(mm),ll),4);
 g_fund(zz,ll) = MAG2(f1,ll); %to observe if the V1 is attenuated or not to
all the load conditions and all fundamental frequencies
 g_ma(zz,ll) = (1/g_fund(zz,ll)); % to determine the gain that should be
applied in ma to be unitary for every freq and Vll
 ma_crt(zz,ll) = ma_new(ll)*g_ma(zz,ll);

 MX=max(ma_crt(:));

 dd(zz,ll)=round(100*ma_crt(zz,ll));
```

```
 ll=ll+1;
     end
  mm=mm+1;

 end

 %%%%HARMONIC ANALYSIS

n = 0; %the shifting of the harmonic in the multiple of the switching
frequency, varys from 0-2-4-6
n2 = 1; %the shifting of the harmonic in the multiple of the switching
frequency, varys from 1-3-5-7
m = 1; %multiple of mf, varys from 1-3
m2 = 2; %multiple of mf, varys from 2-4
M = 0.01; %M=ma M = 0.36 = modulation index
Mi=0.01; %initial ma
i=1;

 while m<5 & m2<5
    while n<7 & n2<8
        while M<1.01 %maximum ma value
            H(i) = abs((4/(m*3.1415))*(besselj(n,(m*3.1415*M)/2))); %Bessel
function for odd m
            G(i) = abs((4/(m2*3.1415))*(besselj(n2,(m2*3.1415*M)/2)));
%Bessel function for even m
            i = i+1;
            M = M+Mi; %how the ma will vary (ex.:0.2-0.4-0.6-0.8-1.0)
        end
        M = Mi; %need to be reset at each loop
        n = n+2;
        n2 = n2+2;
    end
    n = 0;
    n2 = 1;
    M = Mi;
    m = m+2;
    m2 = m2+2;
 end
 H;
 G;

 n_ma = 100; %number of collums of m_a (ex.: Mohan's has 5 collums)-dependend
on the chosen M (ex:M=0.01,n_ma=100)
 %P1=0 if 3-phase
 P1 = H(1:n_ma); %how to "print" %0 if tri-phase
 P2 = H(n_ma+1:2*n_ma);
 P3 = H(2*n_ma+1:3*n_ma);
 P4 = H(3*n_ma+1:4*n_ma);

 Q1 = G(1:n_ma);
 Q2 = G(n_ma+1:2*n_ma); %0 if tri-phase
 Q3 = G(2*n_ma+1:3*n_ma);
 Q4 = G(3*n_ma+1:4*n_ma);
```

```
 %P5=0 if 3-phase
 P5 = H(4*n_ma+1:5*n_ma); %0 if tri-phase
 P6 = H(5*n_ma+1:6*n_ma);
 P7 = H(6*n_ma+1:7*n_ma);
 P8 = H(7*n_ma+1:8*n_ma);

 Q5 = G(4*n_ma+1:5*n_ma);
 Q6 = G(5*n_ma+1:6*n_ma); %0 if tri-phase
 Q7 = G(6*n_ma+1:7*n_ma);
 Q8 = G(7*n_ma+1:8*n_ma);

  if tri == 1 %for 3-phase
     P1 = P1*0;
     P5 = P5*0;
     Q2 = Q2*0;
     Q6 = Q6*0;
 end

 line = [0.01:0.01:1];


 K = [line;P1;P2;P3;P4;Q1;Q2;Q3;Q4;P5;P6;P7;P8;Q5;Q6;Q7;Q8]; %list of
harmonic amplitudes

if tri == 1
    K_LL = K*0.61237;
    K_VDC = K_LL*Vdc; %real magnitude values of the harmonics
else %for 1-phase sytems
    K_F = K*1;
    K_VDC = K*(Vdc/2);
end

uu = 1;
while uu<(n_ma+1);
    [m(uu),p(uu)] = max(K_VDC(2:end,(uu))); %m=maximum value and p=position
of the max value (to know the freq in which it happens)
    uu = uu+1;
end

mti
=[m(9),m(14),m(18),m(23),m(27),m(32),m(36),m(41),m(45),m(49),m(54),m(58),m(63
),m(67),m(72),m(76),m(81),m(85),m(90)];
pti
=[p(9),p(14),p(18),p(23),p(27),p(32),p(36),p(41),p(45),p(49),p(54),p(58),p(63
),p(67),p(72),p(76),p(81),p(85),p(90)];

gain;
zz;

con = 1;
while con<20
    if dd(zz,con)>=100
        mti_dd(zz,con)=0;
        pti_dd(zz,con)=0;
```

```
    else
        mti_dd(zz,con) = m(dd(zz,con));
        pti_dd(zz,con) = p(dd(zz,con));
    end
     v_dom_aff(con)=mti(con)*gain(pti(con),con);

    if pti_dd(zz,con)==0
        v_dd(zz,con)=0;
    else
       v_dd(zz,con)=mti_dd(zz,con)*gain(pti_dd(zz,con),con);
    end

    con=con+1;
end



Tti = 0.0025*Vll; %original = 0.0025

cont = 1;
while cont<20
    if v_dd(zz,cont) <= Tti(cont)
        XX(cont) = 1; %print "1" if the confition is respected
    else
        XX(cont) = 0; %print "0" if not respected
    end
    cont = cont+1;
end

YY=transpose(XX);

BB(:,zz) = YY;
zz=zz+1;
end

if MX<1
    aa=length(VC)+1000;
   sprintf('Choosen Capacitor (%f u) is correct. Frequency analysis
pending',1000000*C)

else
    aa=aa+1;
    sprintf('Choosen Capacitor (%f u) not correct',1000000*C)
end

end
aa=1;
Sum=sum(sum(BB));
if Sum==171
    ff=length(Vfres)+1000;
    kk=length(Vfsw)+1000;
    ms = msgbox(sprintf('Suggested Resonant Frequency of (%f k),at a
Switching Frequency of (%f k) with a Capacitor of(%f u) for values of the LPF
that ensure to the VSI an operation, in the designed conditions, with
THDv<0.5 percent.',0.001*fres,0.001*fsw,1000000*C))
```

```
    %sprintf('Suggested Resonant Frequency of (%f k), at a Switching
Frequency of (%f k) with a Capacitor of (%f u) for values of the LPF that
ensure to the VSI an operation, in the designed conditions, with THDv<0.5
percent.',0.001*fres,0.001*fsw,1000000*C)
    break
else
    ff=ff+1;
   sprintf('Chosen Resonant Frequency (%f k) not enough',0.001*fres)
if ff==length(Vfres)+1;
    kk=kk+1;
    sprintf('Chosen Switching Frequency (%f k) not enough', 0.001*fsw)
end
end
end
end



ll=1;
while ll<length(R)+1;

%the damping factor is defined as:
E(ll)=((1/(2*R(ll)))*(sqrt(L/C)));
DampingFactor = transpose(E);

 %the transfer funtion of the LC filter is gien by: Gn = (1/LC)/(s^2 +
(1/RC)s + (1/LC))
 A = [0 0 (1/(L*C))];
 B = [1 (1/(R(ll)*C)) (1/(L*C))];
 Gn = tf(A,B);

 opts = bodeoptions;
 %opts.MagUnits = 'abs'
 opts.FreqUnits = 'Hz';
 bodeplot (Gn,opts)
 hold on;
 grid on;

 ll = ll+1;
 end

%
%legend('R1=0.847','R2=1.270','R3=1.694','R4=2.117','R5=2.540','R6=2.964','R7
=3.387','R8=3.811','R9=4.234','R10=4.657','R11=5.081','R12=5.504','R13=5.927'
,'R14=6.351','R15=6.774','R16=7.198','R17=7.841','R18=8.736','R19=9.680');
legend('V1=22V','V2=33V','V3=44V','V4=55V','V5=66V','V6=77V','V7=88V','V8=99V
','V9=110V','V10=121V','V11=132V','V12=143V','V13=154V','V14=165V','V15=176V'
,'V16=187V','V17=198V','V18=209V','V19=220V');
set(gca,'FontSize',22)


%NO-LOAD AND FULL-LOAD CONDITION GRAPHIC:
Rmin_min=0.8468; %fullload to 22 V
A1 = [0 0 (1/(L*C))];
B1 = [1 (1/(Rmin_min*C)) (1/(L*C))];
```

```
Gn1 = tf(A1,B1);

Rmin=9.68; %fullload to 220 V
A2 = [0 0 (1/(L*C))];
B2 = [1 (1/(Rmin*C)) (1/(L*C))];
Gn2 = tf(A2,B2);

Rmax=150; %noload
A3 = [0 0 (1/(L*C))];
B3 = [1 (1/(Rmax*C)) (1/(L*C))];
Gn3 = tf(A3,B3);

figure
opts = bodeoptions;
 %opts.MagUnits = 'abs'
 opts.FreqUnits = 'Hz';
 bodeplot (Gn1,opts)
 hold on;
 bodeplot (Gn2,opts)
 hold on;
 bodeplot (Gn3,opts)
 grid on;
 legend('Rmin - full load (22 V)','Rmin - full load (220 V)','Rmax(150 ohms)
- no load');
 set(gca,'FontSize',22)

xma = ma_new;

i = 1;
while i<length(xma)+1
    Y(i,:) = xma(i)*400*0.612*BB(i,:);

    i=i+1;
end

Y(~Y) = nan;

j = 1;
while j<length(f1_g)+1
    [mx(j),px(j)] = max(Y(:,j));
    [mi(j),pi(j)] = min(Y(:,j));

    j=j+1;
end


%to plot the "Restriction Respected Area"
V_ma_dw = mi;
V_ma_up = mx; %ex.: here =215V

% "Restriction Respected Area"
load count.dat
plot(count)
figure
```

```
F = [f1_g,fliplr(f1_g)]; %#create continuous x value array for plotting
V_ma = [V_ma_dw,fliplr(V_ma_up)]; %#create y values for out and then back
fill(F,V_ma,[0.839215695858002 0.909803926944733 0.850980401039124]) %#plot
filled area
grid on
xlim([-5 1050])
ylim([-5 230])
xlabel('Frequency  (Hz)')
ylabel('Voltage (V)')
title ('Restriction-Respected Area')
set(gca,'FontSize',22)

%Power x Voltage
% figure
% plot(Vll,P)
% hold on
% stem (Vll,P)
% grid on
% xlim([0 230])
% ylim([0 5500])
% xlabel('Voltage (V)')
% ylabel('Power (W)')
% title ('VxP relation respecting Ilmax')
% set(gca,'FontSize',22)

%Voltage x Rmin
% figure
% plot(Vll,R)
% hold on
% stem (Vll,R)
% grid on
% xlim([0 230])
% ylim([0 10])
% xlabel('Voltage (V)')
% ylabel('Rmin (ohms)')
% title ('VxRmin relation respecting Ilmax')
% set(gca,'FontSize',22)

% Voltage x Damping Factor
% figure
% plot(Vll,E)
% hold on
% stem (Vll,E)
% grid on
% xlim([0 230])
% ylim([0 10])
% xlabel('Voltage (V)')
% ylabel('Danping Factor')
% title ('Damping Factor relation respecting Rmin')
% set(gca,'FontSize',22)

%Voltage x Gain
figure
plot(Vll,g_fund)
hold on
%plot(Vll,ma_new,'--')
```

```
grid on
% xlim([0 230])
% ylim([0 1.1])
xlabel('Voltage (V)')
ylabel('Gain')
title ('Gain versus Vout')
legend('0 Hz','60 Hz','300 Hz','420 Hz','540 Hz','660 Hz','780 Hz','900
Hz','1 kHz');
set(gca,'FontSize',22)

figure
title ('ma Correction')
subplot(2,1,1)
plot(Vll,g_fund(2,:))
hold on
grid on
plot(Vll,ma_new,'--')
plot(Vll,ma_crt(2,:),'--')
% xlim([0 230])
% ylim([0 1.1])
xlabel('Voltage (V)')
ylabel('Gain')
legend('LPF original attenuation for 60Hz','original ma', 'compensated ma')
set(gca,'FontSize',22)

% subplot(2,2,2)
% plot(Vll,g_fund(3,:))
% hold on
% grid on
% plot(Vll,ma_new,'--')
% plot(Vll,ma_crt(3,:),'--')
% % xlim([0 230])
% % ylim([0 1.1])
% xlabel('Voltage (V)')
% ylabel('Gain')
% legend('LPF original attenuation for 420Hz','original ma', 'compensated
ma')
% set(gca,'FontSize',18)
%
% subplot(2,2,3)
% plot(Vll,g_fund(6,:))
% hold on
% grid on
% plot(Vll,ma_new,'--')
% plot(Vll,ma_crt(6,:),'--')
% % xlim([0 230])
% % ylim([0 1.1])
% xlabel('Voltage (V)')
% ylabel('Gain')
% legend('LPF original attenuation for 780Hz','original ma', 'compensated
ma')
% set(gca,'FontSize',18)

subplot(2,1,2)
plot(Vll,g_fund(8,:))
hold on
```

```
grid on
plot(Vll,ma_new,'--')
plot(Vll,ma_crt(8,:),'--')
% xlim([0 230])
% ylim([0 1.1])
%xlabel('Voltage (V)','fontsize',14)
xlabel('Voltage (V)')
ylabel('Gain')
legend('LPF original attenuation for 1kHz','original ma', 'compensated ma')
set(gca,'FontSize',22)
```

A.3 PSIM simulated system

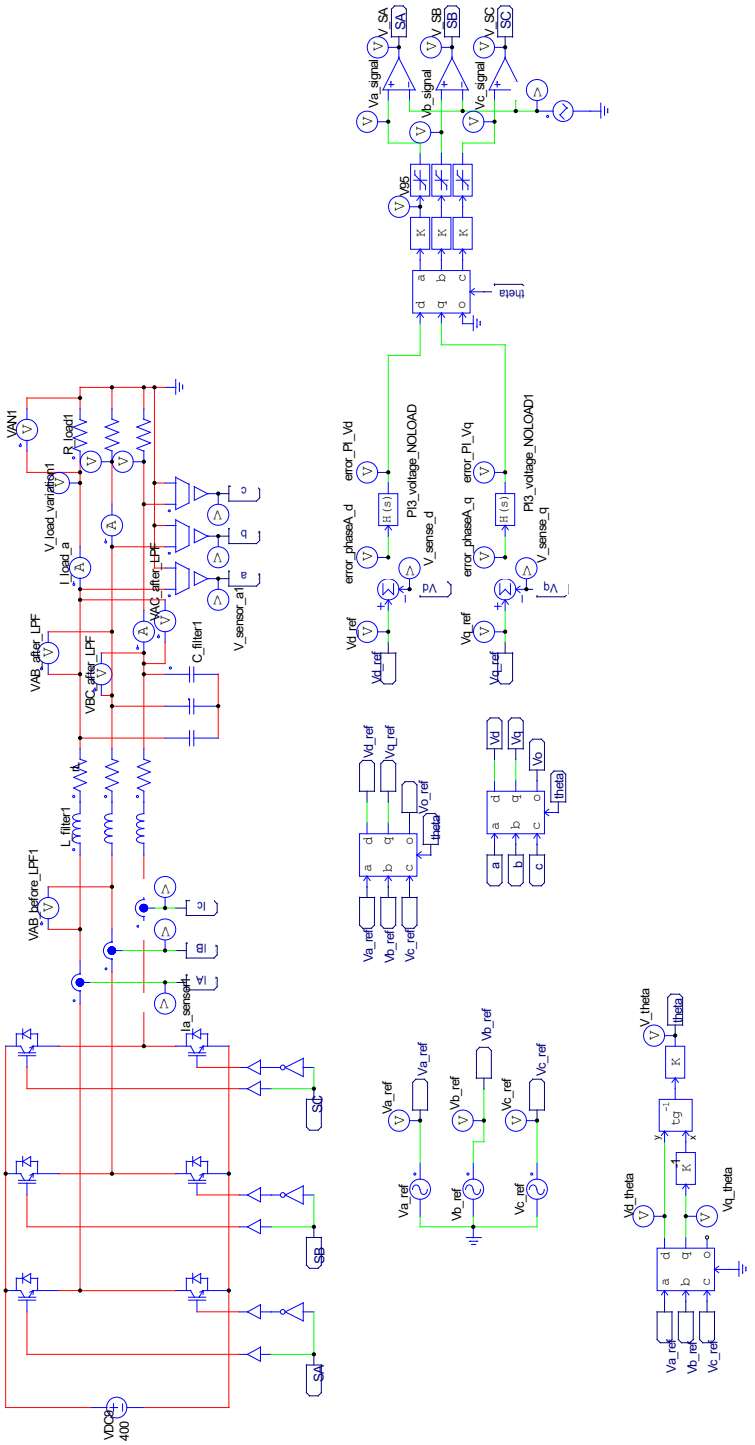
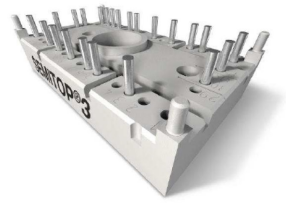


Figure A. 1 Closed Loop Control System simulated in PSIM

A.4 Datasheet of SK20GD066ET

SK20GD066ET



SEMITOP® 3

IGBT Module

SK20GD066ET

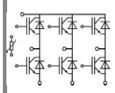
Target Data

Features

- Compact design
- One screw mounting
- Heat transfer and isolation through direct copper bonded aluminium oxide ceramic (DCB)
- Trench IGBT technology
- CAL technology FWD
- Integrated NTC temperature sensor

Typical Applications*

- Inverter up to 6,3 kVA
- Typ. motor power 4 kW

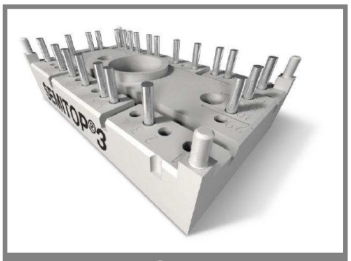


GD-ET

Absolute Maximum Ratings			T_s = 25 °C, unless otherwise specified	
Symbol	**Conditions**		**Values**	**Units**
IGBT				
V_{CES}	T_j = 25 °C		600	V
I_C	T_j = 175 °C	T_s = 25 °C	30	A
		T_s = 70 °C	25	A
I_{CRM}	I_{CRM}= 2 x I_{Cnom}		40	A
V_{GES}			± 20	V
t_{psc}	V_{CC} = 360 V; $V_{GE} \leq$ 20 V; V_{CES} < 600 V	T_j = 150 °C	6	µs
Inverse Diode				
I_F	T_j = 175 °C	T_s = 25 °C	31	A
		T_s = 70 °C	24	A
I_{FRM}	I_{FRM}= 2 x I_{Fnom}		40	A
I_{FSM}	t_p = 10 ms; half sine wave	T_j = 150 °C	95	A
Module				
$I_{t(RMS)}$				A
T_{vj}			-40 ... +175	°C
T_{stg}			-40 ... +125	°C
V_{isol}	AC, 1 min.		2500	V

Characteristics			T_s = 25 °C, unless otherwise specified			
Symbol	**Conditions**		**min.**	**typ.**	**max.**	**Units**
IGBT						
$V_{GE(th)}$	V_{GE} = V_{CE}, I_C = 0,29 mA		5	5,8	6,5	V
I_{CES}	V_{GE} = 0 V, V_{CE} = V_{CES}	T_j = 25 °C			0,0011	mA
		T_j = 125 °C				mA
I_{GES}	V_{CE} = 0 V, V_{GE} = 20 V	T_j = 25 °C			300	nA
		T_j = 125 °C				nA
V_{CE0}		T_j = 25 °C		0,9	1,1	V
		T_j = 150 °C		0,8	1	V
r_{CE}	V_{GE} = 15 V	T_j = 25°C		27,5	37,5	mΩ
		T_j = 150°C		42,5	52,5	mΩ
$V_{CE(sat)}$	I_{Cnom} = 20 A, V_{GE} = 15 V	T_j = 25°$C_{chiplev.}$		1,45	1,85	V
		T_j = 125°$C_{chiplev.}$		1,65	2,05	V
C_{ies}				1,1		nF
C_{oes}	V_{CE} = 25, V_{GE} = 0 V	f = 1 MHz		0,071		nF
C_{res}				0,032		nF
Q_G	V_{GE}= -7V...+15V			225		nC
$t_{d(on)}$				16		ns
t_r	R_{Gon} = 15 Ω	V_{CC} = 300V		15		ns
E_{on}	di/dt = 3300 A/µs	I_C = 20A		0,34		mJ
$t_{d(off)}$	R_{Goff} = 15 Ω	T_j = 150 °C		166		ns
t_f	di/dt = 3300 A/µs	V_{GE}=±15V		40		ns
E_{off}				0,63		mJ
$R_{th(j-s)}$	per IGBT			1,95		K/W

SK20GD066ET



SEMITOP® 3

IGBT Module

SK20GD066ET

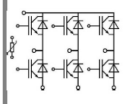
Target Data

Features

- Compact design
- One screw mounting
- Heat transfer and isolation through direct copper bonded aluminium oxide ceramic (DCB)
- Trench IGBT technology
- CAL technology FWD
- Integrated NTC temperature sensor

Typical Applications*

- Inverter up to 6,3 kVA
- Typ. motor power 4 kW



GD-ET

Characteristics

Symbol	Conditions		min.	typ.	max.	Units
Inverse Diode						
$V_F = V_{EC}$	I_{Fnom} = 20 A; V_{GE} = 0 V	T_j = 25 °$C_{chiplev.}$		1,45	1,7	V
		T_j = 150 °$C_{chiplev.}$		1,45	1,7	V
V_{F0}		T_j = 25 °C		1	1,1	V
		T_j = 150 °C		0,9	1	V
r_F		T_j = 25 °C		22,5	30	mΩ
		T_j = 150 °C		27,5	35	mΩ
I_{RRM}	I_F = 30 A	T_j = 150 °C		32		A
Q_{rr}	di/dt = 3300 A/µs			2		µC
E_{rr}	V_{CC}= 300V			0,2		mJ
$R_{th(j-s)D}$	per diode			2,46		K/W
M_s	to heat sink		2,25		2,5	Nm
w				30		g
Temperature sensor						
R_{100}	T_s =100°C (R_{25}=5kΩ)			493±5%		Ω

This is an electrostatic discharge sensitive device (ESDS), international standard IEC 60747-1, Chapter IX.

* The specifications of our components may not be considered as an assurance of component characteristics. Components have to be tested for the respective application. Adjustments may be necessary. The use of SEMIKRON products in life support appliances and systems is subject to prior specification and written approval by SEMIKRON. We therefore strongly recommend prior consultation of our personal.