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A MODIFIED ASYMMETRICAL PULSE-WIDTH MODULATED SERIES RESONANT DC/DC CONVERTER

Simmi Mangat

A Thesis

in

The Department

of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements
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ABSTRACT

A Modified Asymmetrical Pulse-Width Modulated Series Resonant DC/DC Converter

Simmi Mangat

Telecommunication and computer systems require power supply topologies that offer high efficiency and high power density at ever-increasing switching frequencies. There are many resonant topologies that can offer this, but the asymmetrical pulse-width modulated (APWM) resonant DC/DC converter is a simple topology that operates at a constant frequency and with near-zero voltage switching losses. However, the range of input voltage where high efficiency is maintained is narrow. After a certain limit, zero voltage switching is lost and the voltage stress on the resonant inductor becomes too high. A modified APWM resonant DC/DC converter topology is proposed that employs an auxiliary network. Steady-state analysis and computer simulations are performed and show how this simple auxiliary network compensates the original topology by improving the efficiency and reducing the resonant inductor voltage stress. A prototype of the modified topology is constructed and experimental analysis supports the theoretical results. Operating curves and a design example help to realize optimum values of the major components. To further improve the performance, the use of MOSFETs as synchronous rectifiers in place of diode rectifiers is proposed. Two examples of synchronous rectifier topologies that are applicable to the converter under study are investigated. Computer simulation shows the feasibility of employing synchronous rectification with the modified APWM series resonant DC/DC converter.

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LIST OF ACRONYMS

PWM	Pulse-Width Modulation
DC	Direct Current
EMI	Electro-Magnetic Interference
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
FET	Field-Effect Transistor
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
APWM	Asymmetrical Pulse-Width Modulated
SR	Synchronous Rectification
BJT	Bipolar Junction Transistor
RMS	Root Mean Square
IC	Integrated Circuit
CMOS	Complementary Metal-Oxide Semiconductor
VLSI	Very Large Scale Integration

LIST OF PRINCIPAL SYMBOLS

v_{gs}	gate-source voltage of a MOSFET
v_{ds}	drain-source voltage of a MOSFET
f_s	switching frequency in Hertz
ω_s	switching frequency in radians/second
D	duty cycle
C_s	resonant capacitor
L_s	resonant inductor
V_{in}	input voltage to converter
S_1, S_2	main power MOSFETs of converter
C_1, C_2	capacitors across main power MOSFETs
D_1, D_2	diodes across main power MOSFETs
i_s	resonant current
n	harmonic number
I_{S_1}	peak value of the fundamental component of i_s
v_{ds_1}	drain-source voltage across power MOSFET S_1
v_{ds_2}, v_s	drain-source voltage across power MOSFET S_2
θ_n	phase difference arising from asymmetrical duty cycle
ϕ_n	phase difference between v_s and i_s
I_o	DC output current

V_o	DC output voltage
Q	quality factor of resonant tank
C_{1a}, C_{2a}	auxiliary capacitors
L_a	auxiliary inductor
T_x	main power transformer
DR_1, DR_2	diodes of output diode rectifier
C_o	output filter capacitor
R_L	load resistance
R_{eq}	equivalent load resistance seen by resonant tank
v_{gs1}, v_{gs2}	gate-source voltage of MOSFETs S_1 and S_2
T_s	switching time period
V_1, V_2	voltage across C_{1a} and C_{2a} respectively
v_r	voltage across primary of main transformer
n_{T_x}	transformer turns ratio
f_r	resonant frequency
ω	ratio between switching frequency and resonant frequency
Z_{in}	impedance of resonant tank
v_{C_s}	voltage across resonant capacitor
v_{L_s}	voltage across resonant inductor
v_{L_a}	voltage across auxiliary inductor
i_{L_a}	auxiliary inductor current
I_a	peak of the auxiliary inductor current

i_{sw}	current through power MOSFETs S_1 and S_2
i_d	input current
t	time in micro seconds
$i_{C_{2a}}$	current through auxiliary capacitor C_{2a}
M	ratio between the output and input voltages
I_d	input DC current
P_o	output power of the converter
r_{DS1}, r_{DS2}	on-state resistances of S_1 and S_2
r_C	parasitic resonant capacitor resistance
r_L	parasitic resonant inductor resistance
r_{DS}	average parasitic resistance of main power MOSFETs
r	total parasitic resistance of resonant circuit and main power MOSFETs
P_r	total conduction power loss in resonant circuit and main power MOSFETs
V_F	forward voltage drop of a diode
R_F	on-state resistance of a diode
K	the ratio between the auxiliary inductor and resonant inductor
ΔV_{in}	voltage ripple across capacitors C_{1a} and C_{2a}
ΔV_o	output voltage ripple
$V_{DS\_S1,S2}$	drain-source breakdown voltage of S_1 and S_2
SR_1, SR_2	synchronous rectifier MOSFETs
v_{SR1}, v_{SR2}	voltage across SR_1 and SR_2 respectively
i_{SR2}	current through SR_2

I_{SR}	peak forward current of each rectifier MOSFET
I_{SRrms}	RMS value of the current through each rectifier MOSFET
V_{SR}	peak reverse voltage of each rectifier MOSFET
V_{R1}	amplitude of the fundamental component of the transformer input voltage
V_{R1rms}	RMS value of V_{R1}
P_{Req}	input power of the synchronous rectifier
r_{DS_SR}	drain-source resistance of synchronous rectifier MOSFET
P_{rDS}	power loss in the forward resistance, r_{DS} of each rectifier MOSFET
P_{SR}	total power loss of the synchronous rectifier
η_{SR}	efficiency of the synchronous rectifier
T_{sense1}, T_{sense2}	current-sense transformers
Q_1, Q_2, Q_3, Q_4	bipolar junction transistors used in current-sense transformer topology
i_{pri}	constant sinusoidal current source represented as resonant current in current-sense transformer topology
T_{main}	main transformer in current-sense transformer topology
i_{sec1}, i_{sec2}	secondary currents of T_{main}
V_{cc}	DC voltage source for current-sense transformer topology
L_{m1}	magnetizing inductance of sense transformer in current-sense transformer topology
i_{m1}	magnetizing current of L_{m1}
i_{sensep}	primary current of the sense transformer
L_m, $L_{m,\,min}$	minimum value for the magnetizing inductor
V_{be}, V_{be1}, V_{be2}	base-emitter voltages of BJTs

$\tau_{v_{ds}}$	propagation delay through drain-source voltage comparator used in adaptive control scheme
$\tau_{v_{gs}}$	propagation delay through gate-source voltage comparator used in adaptive control scheme
τ_{timer}	propagation delay through timer used in adaptive control scheme
τ_{driver}	propagation delay through driver used in adaptive control scheme
C_{int}	integrating capacitor used to set timing interval in adaptive control scheme
I_{PUMP}	charge pump used to charge and discharge C_{int}

Chapter 1

Introduction

1.1 GENERAL INTRODUCTION

With the advancement of telecommunication and computer systems, the distributed power architecture and point-of-use power supplies are becoming essential. While operating at a constant frequency, these supplies are required to produce high efficiency, high power density and low switching losses. Furthermore, operation at high frequencies not only increases the power density, but also reduces component size. Currently, there is a wide variety of power converters on the market, but the designer must select those converters which satisfy their design requirements. For example, with operation at high frequencies, some topologies show better performance than others.

1.2 SWITCH-MODE AND SOFT-SWITCHING CONVERTERS

In many PWM DC/DC converter topologies, the controllable switches are operated in switch mode where they are required to turn the entire load current on and off during each switching cycle. Under these conditions, the switches are subjected to high switching stresses and high switching power losses. Fig.1.1 illustrates the general switching characteristics of a switch-mode converter. Fig.1.1a shows the switch gating control signal, $v_{gs}(t)$, and Fig.1.1b shows the switch drain-source voltage, $v_{ds}(t)$, and drain current,

$i_d(t)$, waveforms during both turn-on and turn-off of the switch. Fig.1.1c illustrates the instantaneous power dissipation, $p(t)$.

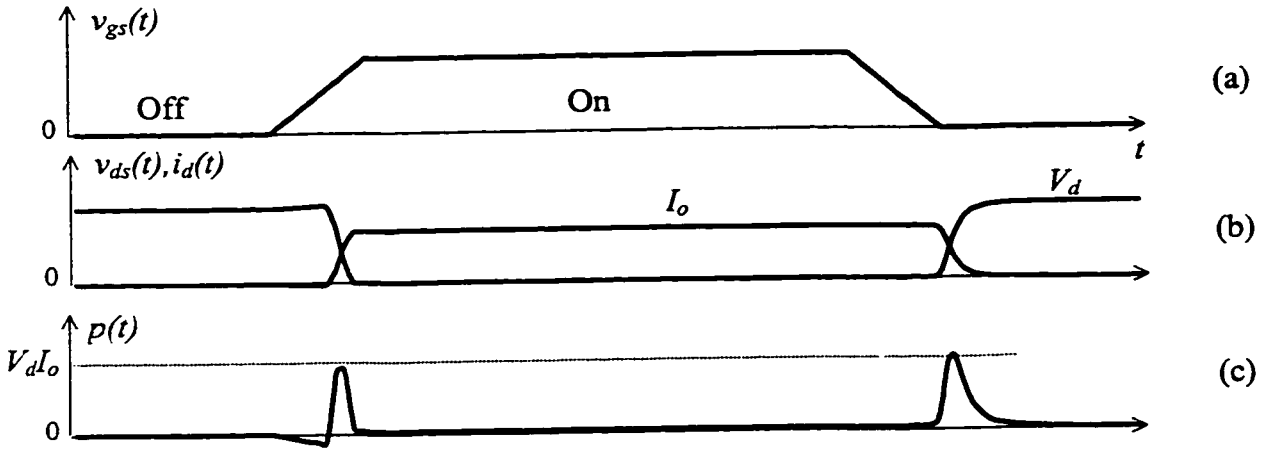


Fig. 1.1 Generic Switch switching characteristics: a) control signal, b) switch current and voltage, c) instantaneous switch power loss

It is obvious from this plot that a large instantaneous power dissipation occurs in the switch during the turn-on and turn-off intervals. There are f_s such turn-on and turn-off transitions per second. The average switching power loss P_s in the switch due to these transitions can be given by:

$$P_s = \frac{V_d I_o f_s}{2} \cdot \left(t_{on} + t_{off} \right) \tag{1-1}$$

This is an important result because it shows that the switching power loss in a semiconductor switch varies linearly with the switching frequency and the switching times. For converter operation in the megahertz range, this is not a suitable choice. The switch stresses can be reduced by connecting simple dissipative snubber circuits (consisting of diodes and passive components) in series and parallel with the switches in

the switch-mode converters. These dissipative snubbers, however, shift the switching power loss from the switch to snubber circuit and therefore do not provide a reduction in the overall switching power loss. To realize high switching frequencies in converters, the switching losses can be minimized if each power switch in the converter changes its status when the voltage across it and/or the current through it is zero at the switching instant. This is done with the combination of proper converter topologies that exhibit the desired characteristics and are often termed soft-switching converters.

The main advantages gained by using soft-switching converters are:

1) very low switching losses and stresses;

2) improved converter efficiency;

3) reduced need for cooling means;

4) achievement of higher switching frequencies.

Many of the topologies that utilize these zero-voltage and/or zero-current switching techniques require some sort of inductive-capacitive resonance, hence the name "resonant converters". Resonant converters are an important category of soft-switching converters and will be discussed in the next section.

1.3 RESONANT CONVERTERS

The operation of resonant converters is quite different from the operation of PWM converters. First, the switches in a resonant converter create a square-wave AC waveform from the DC source. An LC circuit tuned close to the switching frequency then removes the unwanted harmonics from this square-wave. By changing the switching frequency, the resonant current and hence the load current and voltage can be controlled. These LC

networks have voltage and current waveforms that vary sinusoidally during each switching period. These sinusoidal waveforms mean the absence of high *di/dt* current changes usually associated with square-wave converters. This results in low levels of electromagnetic interference (EMI). There are many categories of resonant converters, which will be examined briefly. The first ones that will be discussed are the load-resonant converters.

1.3.1 Load-Resonant Converters

There are three basic configurations of load-resonant converters: series, parallel and series-parallel [1]. These are shown in Fig.1.2.

Fig.1.2a shows the series-resonant converter. One of the main advantages of the series resonant converter is that the resonant capacitor on the primary side acts as a DC blocking capacitor. This helps in reducing power losses in the main transformer. Also, leakage inductance associated with the main transformer can be grouped together with the resonant inductor. This is possible due to the series arrangement of the resonant components. The future trend is to operate converters at higher frequencies and reduce the output voltage to one volt or less. The advantages of operation at high frequencies include a faster response time of the converter and increased bandwidth. Series resonant converters are suitable topologies for high frequency operation because of their lower power losses. In topologies where the resonant capacitor is in parallel with the transformer, however, the leakage inductance cannot be grouped with the resonant inductor and power losses increase as the frequency increases. Another advantage is that the currents in the power devices decrease as the load decreases. This in turn reduces the power loss in the devices and maintains a high efficiency at low load. At no-load,

however, the output voltage shows poor regulation. The output filter capacitor must carry high ripple current (equal in magnitude to almost 50% of the output DC current). This point, however, is becoming less of a problem because of advancements in capacitor design.

Fig.1.2b shows the parallel-resonant converter. The main advantage of this converter, unlike the previous one, is that the output voltage can be regulated under no-load conditions as long as the operating frequency is above resonance. Another advantage is that the DC filter at the output is inductive, therefore, DC output capacitors capable of carrying very high ripple currents aren't needed. The main disadvantage, however, is that the current carried by the power MOSFETs and the resonant components is relatively independent of the load. The result of this is that the conduction losses in the MOSFETs and the reactive components stay relatively fixed as the load decreases so that the light-load efficiency of the converter suffers. Also, unlike the series resonant converter, leakage inductances in the transformer cannot be grouped with the resonant inductor. Power losses in the transformer are thus increased.

Fig.1.2c shows the series-parallel converter. It is seen that the load is connected in parallel with only part of the capacitance, for example, one-third of the total capacitance, and the other two-thirds of the capacitance appears in series. This topology attempts to combine the advantages of both series and parallel converters while eliminating their disadvantages. With proper selection of C_{r_1} and C_{r_2}, DC current will be blocked by the series resonant capacitor as well as having no-load output voltage regulation. Also, the resonant current will change with a change in the load resistance.

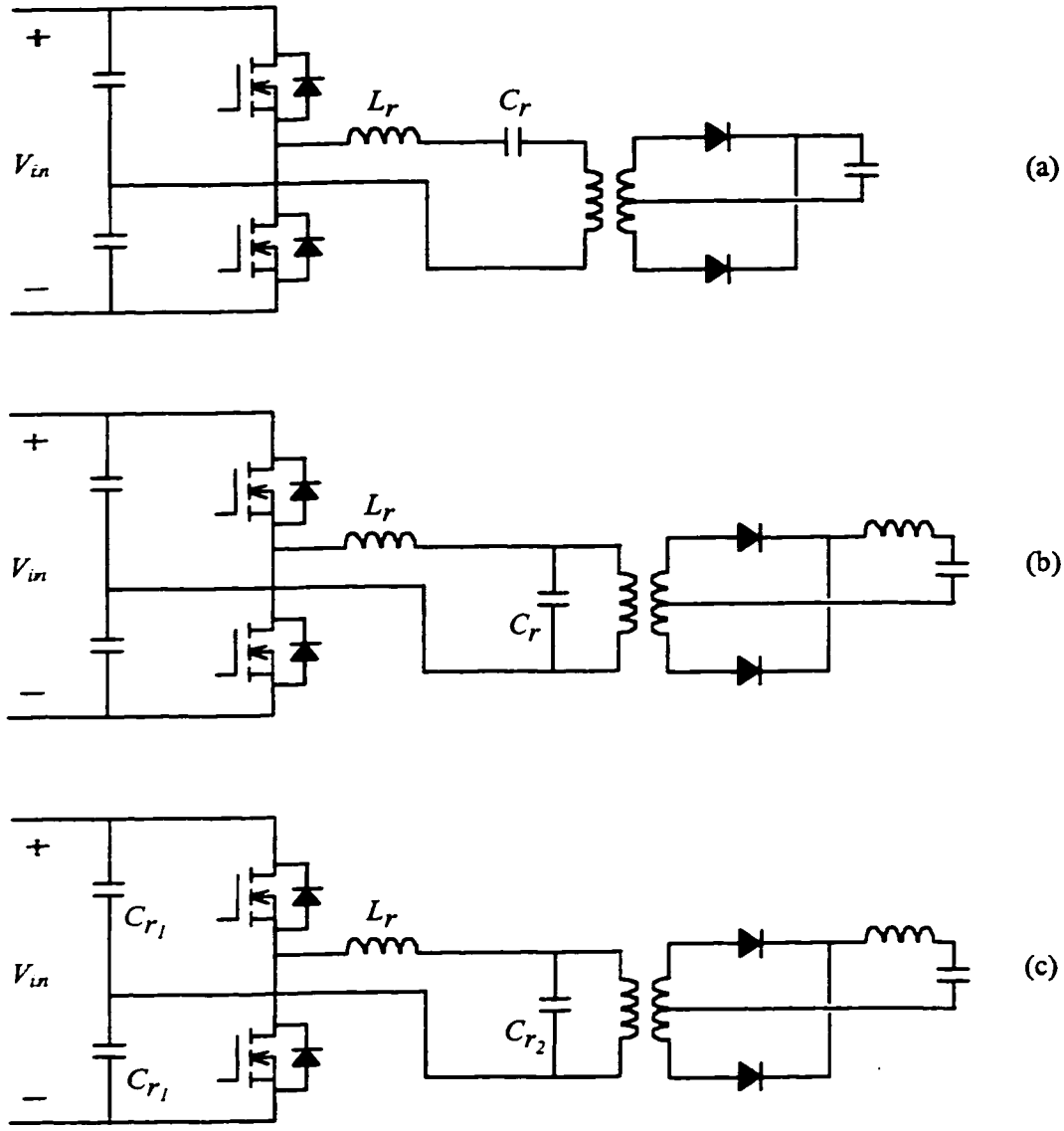


Fig.1.2 Load-Resonant Converters: a) series, b) parallel, c) series-parallel

1.3.2 Resonant-Switch Converters

With this approach, resonant elements are inserted into the switch network to shape the switch voltage and current to provide zero-voltage and/or zero-current switchings. During one switching cycle, there are both resonant and nonresonant operating intervals.

Therefore, these converters are often termed quasi-resonant converters. There are two categories of resonant switch converters: zero-current switching (ZCS) where the switch changes its state at zero-current and zero-voltage switching (ZVS) where the switch changes its state at zero-voltage [2, 3]. Fig.1.3 shows both topologies.

In a ZCS resonant-switch topology, the current produced by LC resonance flows through the switch, thus causing it to turn on and off at zero current. Since the switching losses are minimized and the EMI is reduced, very high switching frequencies can be attained. A drawback to this topology is that the switch must conduct a peak current that is much higher than the load current. The conduction losses in the switch would then be higher than in a similar switch-mode design.

In a ZVS resonant switch topology, the resonant capacitor produces a zero-voltage across the switch, at which instant the switch can be turned on or off. At other instants however, the switch must withstand a peak voltage that is much higher than the input voltage. This requires a switch with a very high voltage rating.

In general, ZVS is usually preferred over ZCS at high switching frequencies. This has to do with the internal capacitances of the switch. When the switch turns on at zero-current but at a finite voltage, the charge on the internal capacitance is dissipated in the switch.

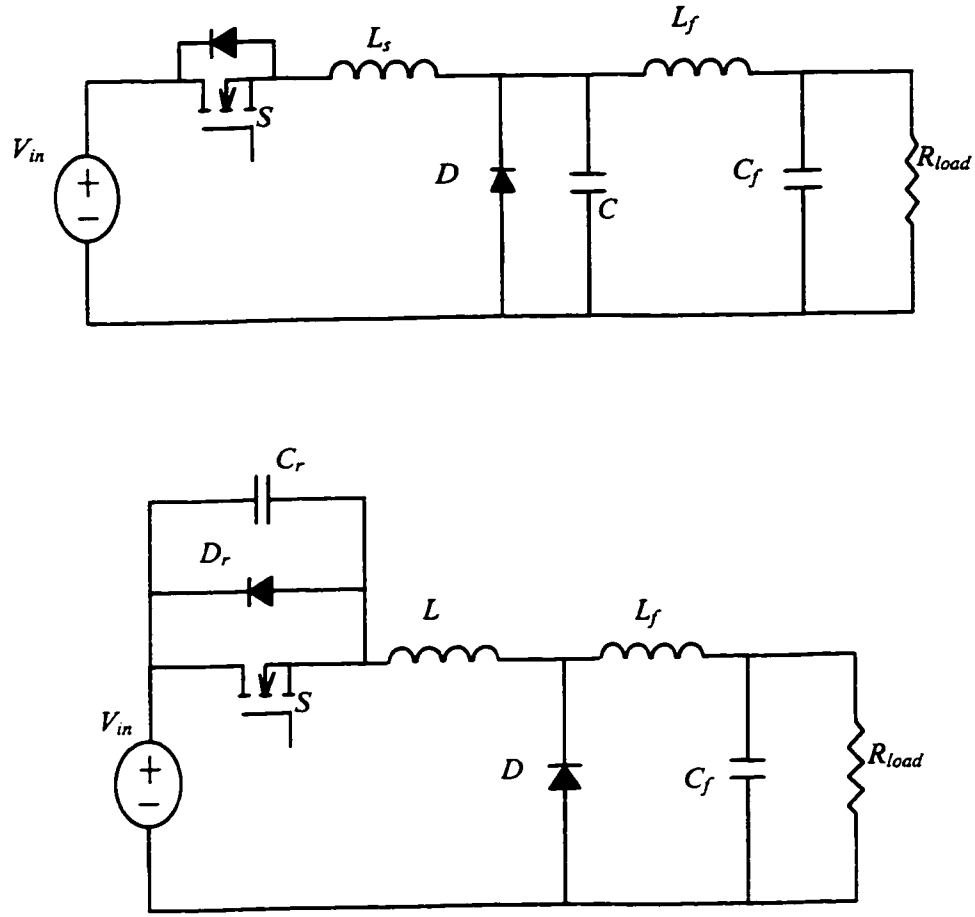


Fig.1.3 DC/DC Resonant-Switch Buck Converters: a) ZCS, b) ZVS

1.3.3 Multi-Resonant Converters

The main limitation of the quasi-resonant-converters is their high voltage and current stresses. The multisonant switch concept overcomes these problems [4]. Fig.1.4 shows a ZVS multisonant buck converter. With the capacitor in parallel with diode, *D*, a new resonant circuit arrangement is formed. The voltage stress across the switch is significantly reduced and the resonant circuit absorbs all major parasitic reactances. By limiting the switching frequency range, the parasitic oscillations found in the ZVS quasi-resonant type are better controlled.

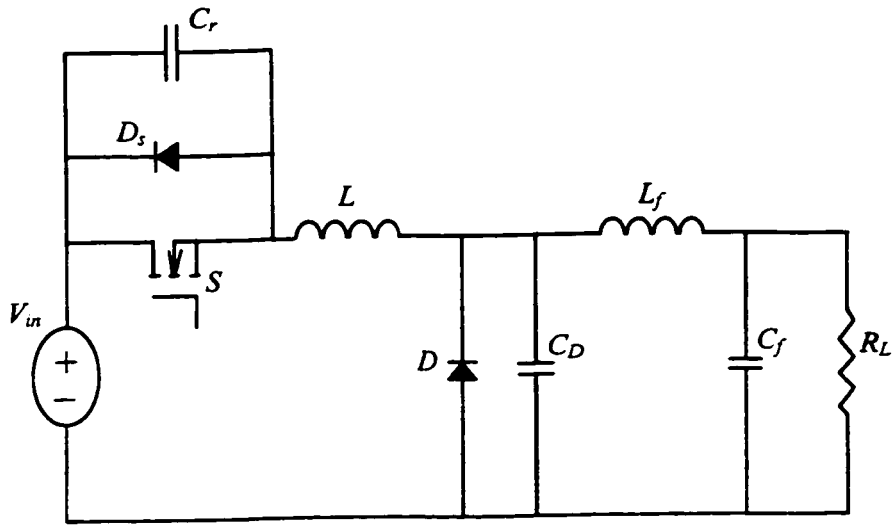


Fig. 1.4 ZVS Multiresonant Buck Converter Topology

1.4 ASYMMETRICAL DUTY CYCLE

There have been many resonant converters discussed in the literature [5-10]. Some offer near-zero switching losses, but only with the variation of the operating frequency can their output voltages be controlled. This becomes difficult when the power supply has to be maintained at a constant switching frequency. Using the asymmetrical duty cycle, it is the variation of the duty cycle D, which controls the output voltage and not the switching frequency. This is unlike the converters mentioned above which switch only at a fifty percent duty cycle. By varying D from 0 to 0.5, the voltage at the output changes from minimum to maximum. This will be explained further in Chapter 2.

1.5 ASYMMETRICAL PULSE WIDTH MODULATED RESONANT DC/DC CONVERTER

Many constant frequency resonant converter topologies have been reported in the literature [11-19]. They show reduced switching losses and can operate at high frequencies, but their circuits are complex and include many components that make them less cost-effective. By combining the resonant converter which shows lossless switching and smaller component size at high frequencies with the asymmetrical duty cycle control, the Asymmetrical Pulse-Width Modulated (APWM) Resonant DC/DC Converter is achieved [20, 21]. This converter is shown in Fig.1.5. This circuit consists of the following functional blocks: a chopper, a series resonant tank, a high-frequency transformer, a rectifying circuit and an output filter. The chopper converts the DC input voltage to a high-frequency unidirectional voltage waveform, v_s at its output. The series resonant circuit converts the unidirectional voltage v_s into the resonant current i_s. Not only does C_s form the resonant circuit along with L_s, but it also serves to block the DC component of v_s from the transformer. The rectifying circuit converts the resonating current i_s into unidirectional current I_o at its output. The output filter removes the high-frequency ripple out of I_o and provides an essentially ripple-free and constant output voltage V_o across the load. As S_2 is switched off, the resonant current is negative, thus forcing C_2 to charge up to V_{in} and C_1 to discharge into the resonant circuit. As C_1 reaches zero volts, the negative resonant current forces D_1 to conduct. Therefore, when the gate signal is applied to S_1, it is able to switch on under zero-voltage conditions.

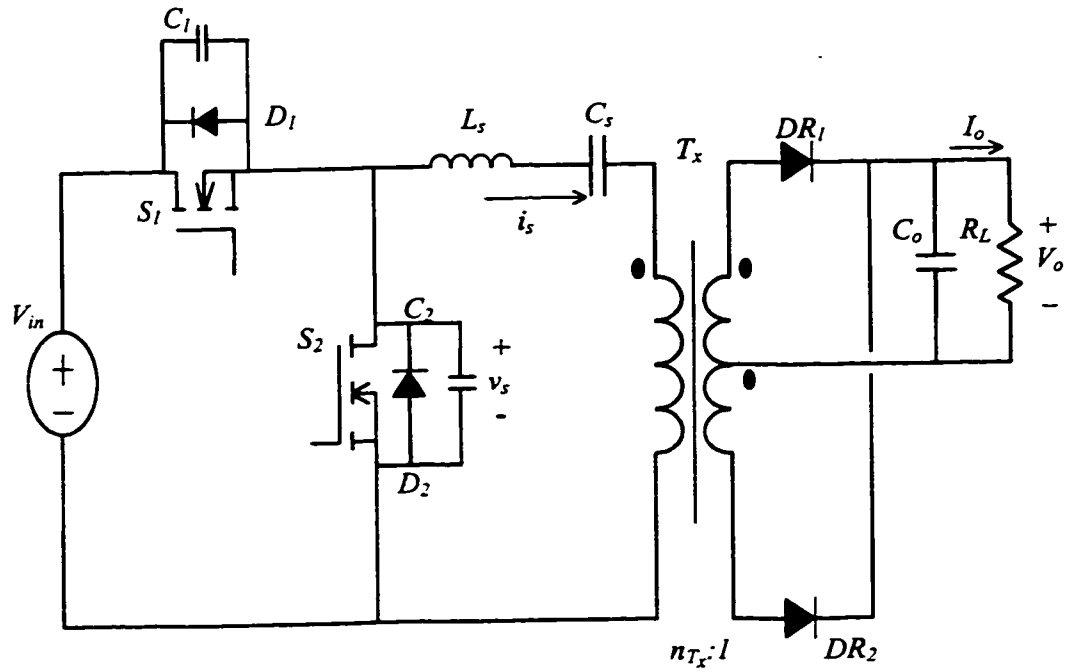


Fig.1.5 Asymmetrical Pulse-Width Modulated DC/DC Converter

The current that was flowing through D_1, now begins to flow through switch S_1. A similar occurrence happens as S_1 is switched off. This time the resonant current is positive, thus forcing C_1 to charge up to V_{in} and C_2 to discharge into the resonant circuit. As C_2 reaches zero volts, the positive resonant current forces D_2 to conduct. Therefore, when the gate signal is applied to S_2, it is able to switch on under zero-voltage conditions. The current that was flowing through D_2 now begins to flow through switch S_2.

This circuit offers near-zero switching losses while operating at constant and very high frequencies. Its component count is low, making operation at low to medium power levels feasible.

1.6 LIMITS OF ORIGINAL CIRCUIT

For all its merits, the APWM Resonant DC/DC Converter has its limits as well. Ideally the converter should operate between 35 and 80 V. The input voltage range in which ZVS is achieved is narrow, however. This compromises the efficiency, which decreases beyond 60V. The reason for this is that as the input voltage increases, the rails at which the switches swing across also increase. The current across the switch is insufficient to properly discharge the MOSFET capacitance, therefore, the switch turns on under non-zero conditions.

Another disadvantage is the voltage stress across the resonant inductor. This increases as the input voltage increases. As it will be shown, operation with ZVS will work only for a limited range of resonant components and resonant frequencies. The aim here is to keep the resonant tank impedance at a minimum. This may not be possible if ZVS is to be achieved. The consequence of this is that the inductor voltage will have notably higher frequency harmonics and thus higher core losses. This will increase the cost as the resonant inductor will be more difficult to manufacture.

The original topology employs a diode rectifier in the output stage. The trend in computer power supplies is a reduction of output voltage levels, from 5V to 3.3V and lower (less than one volt). As the output voltage is reduced, the diode conduction loss remains relatively constant, thereby making it the largest source of power losses in the entire circuit. Even with advanced diodes like the low turn-on Schottky diode, the diode junction contact limits what can be done to reduce the forward voltage drop of diodes.

1.7 SYNCHRONOUS RECTIFIERS

A solution to the problem of diode rectifiers is the MOSFET. Its ability to conduct current in the reverse direction makes it possible to employ a MOSFET where a diode would otherwise be required. Fig.1.6a shows how the MOSFET source and drain connections for synchronous rectification (SR) and Fig.1.6b shows the current-voltage characteristics [22]. When employed as a synchronous rectifier, the source and drain connections of the MOSFET are reversed as shown. The device can now block negative voltage and conduct positive current, similar to the *i-v* characteristics of a diode. The MOSFET must be controlled such that it operates in the on state when the diode would normally conduct and in the off state when the diode would be reverse-biased. To achieve such control, the design must focus on the generation of the gating waveforms.

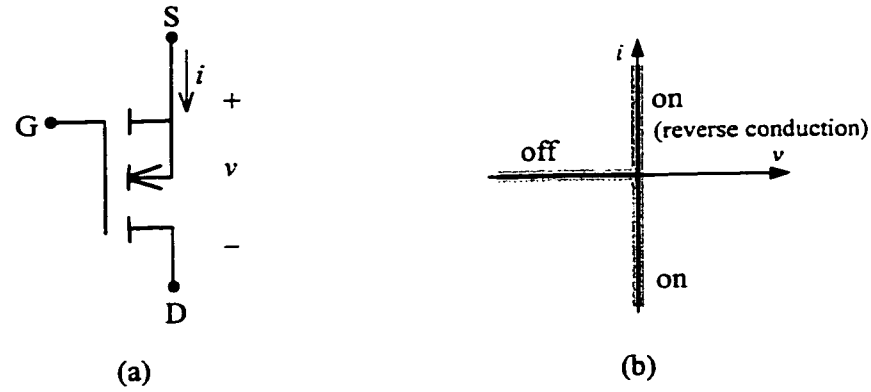


Fig. 1.6 MOSFET Characteristics as a Synchronous Rectifier: a) circuit symbol b) ideal switch characteristics

Many examples have been presented in the literature offering unique approaches for synthesizing the required gate signal:

1) deriving the gating waveforms from auxiliary windings on the main power transformer as shown in Fig.1.7a [23]

2) driving a cross-couple pair of MOSFETs directly from the voltage appearing on the main transformer secondary as shown in Fig.1.6b [24-26]

3) sensing the MOSFETs' drain current and/or drain-source voltage using either current-sense transformers or current-sensing MOSFETS in order to determine the proper gating waveforms [27-30]

4) using integrated circuits to monitor the MOSFET drain-source voltage in order to determine the proper gating waveforms [31, 32]

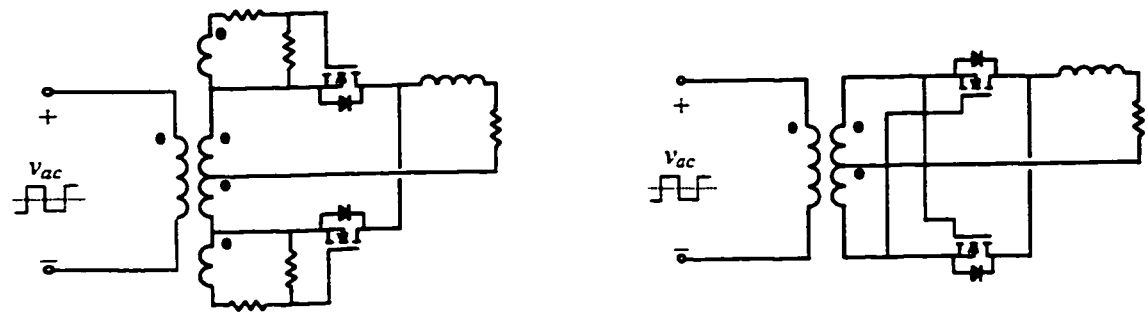
In many applications, the synchronous rectifiers are used in a voltage-fed inductor-loaded configuration. The gate drive signals can then be derived from either an auxiliary winding or from the secondary of the main transformer itself. When the rectifier is current-fed and capacitor-loaded as is the case with APWM series resonant converter, the MOSFET gating signals can no longer be easily derived as in the previous case. From the synchronous rectifier topology examples given above, only the last two are suitable for the converter under study.

1.8 OBJECTIVES AND SCOPE

One of the two objectives of this thesis is to propose and analyze a modified topology that is based on the APWM resonant DC/DC converter. The advantages that the modified topology has over the original one include:

1) wider range of input voltage;

2) stress reduction on the resonant inductor;



(a) (b)

Fig. 1.7 Synchronous Rectifier Topologies: a)using auxiliary windings of the main transformer b)cross-coupled gate-drain connection

3) reduced losses in the rectifying circuit;

4) higher efficiency;

A performance comparison will also be made between the original and proposed topologies.

The other objective is to investigate the use of synchronous rectifiers for the proposed topology. It will be shown that diode rectifiers create relatively high power losses, thus lowering the overall efficiency of the proposed converter. In using synchronous rectification in the output stage, the goal is to reduce power losses and increase efficiency.

The scope of this thesis is limited to the steady state analyses, simulation results, experimental results and design of the proposed topology. This topology is suitable for low power applications (between 30 and 35W), high switching frequencies (0.5-1MHz) and DC input voltage in the range of 35 to 80V. The output voltage is maintained at 5V. Also included within the scope of this thesis is the investigation of the use of synchronous

rectifiers. Some examples of SR topologies suitable for current-fed topologies will be investigated.

1.9 SUMMARY

The contents of the thesis are as follows:

In Chapter 2, the modified APWM resonant DC/DC converter is described and its principle of operation is explained. Theoretical analysis is done and compared with both a computer simulation model and an experimental prototype. Comparisons are also made between the original and modified topologies.

In Chapter 3, performance curves are presented that aid in determining essential component values. Theoretical analysis is also presented which will also help determine other component values.

In Chapter 4, basic analysis of the synchronous rectifier is presented, including power loss analysis. Two examples of synchronous rectifier topologies that are applicable to the converter under discussion are investigated. Their principles of operation are examined as well as studying both their advantages and disadvantages. Computer simulation results are also given.

In Chapter 5, a summary of the thesis is given as well as the overall conclusions and contributions. Suggestions for future work on this topic are also proposed.

Chapter 2

Modified Asymmetrical Pulse-Width Modulated Resonant DC/DC Converter

2.1 INTRODUCTION

In examining previous constant frequency resonant converter topologies, many offer high power densities and reduced switching losses, but only for medium to high power levels. The APWM resonant DC/DC converter has been shown to exhibit near-zero switching losses while operating at constant and high frequencies. However, its drawbacks result in poor performance at higher input voltages. A solution to this problem is necessary.

This chapter presents a new topology that will overcome the previously mentioned drawbacks. In combination with an additional network, a modified APWM resonant DC/DC converter is evolved.

Section 2.2 will present a detailed description of the modified topology as a series of functional blocks. Section 2.3 examines the operating principle by looking at the events occurring in one switching cycle. Section 2.4 performs the steady-state analysis of the converter by examining each functional block separately. Section 2.5 presents an analysis of the diode rectifier, particularly a power loss analysis. Section 2.6 presents the results from computer simulation of the converter in steady state, whereas section 2.7 will show the actual experimental results from the construction of a prototype. Section 2.8 will

present a comparison between the original topology and the modified one that is the subject of this thesis. Section 2.9 will summarise the key points of this chapter.

2.2 CIRCUIT DESCRIPTION

Fig.2.1 shows the APWM resonant DC/DC converter along with the additional network [33]. This network is shown within the dashed lines. The circuit can be broken down into functional blocks including the compensating network (C_{1a}, C_{2a} and L_a), a chopper, a series-resonant tank (L_s, C_s), a power transformer (T_x), a rectifying block (DR_1, DR_2), the output filter, C_o, and the load R_L. The chopper consists of the two switches (S_1, S_2), the two snubber capacitors (C_1, C_2) and two-anti parallel diodes (D_1, D_2). With the presence of the compensating network, the switch currents are the sum of the resonant current and the auxiliary current.

This circuit consists of two switches, S_1 and S_2. These are controlled by two complementary gating signals, v_{gs1} and v_{gs2}, respectively. The gating signal of S_1 has a duty cycle of D and that of S_2 is 1-D. When S_1 is on, the power from the source is transferred to the load and the output of the chopper sees a positive voltage of V_{in} from the source. When S_2 turns on, the input side is separated from the rest of the power circuit and the output of the chopper sees the voltage across S_2 which goes to zero volts. The energy from the resonant components now freewheels through S_2 and supplies power to the load. By varying D, we can control the output voltage.

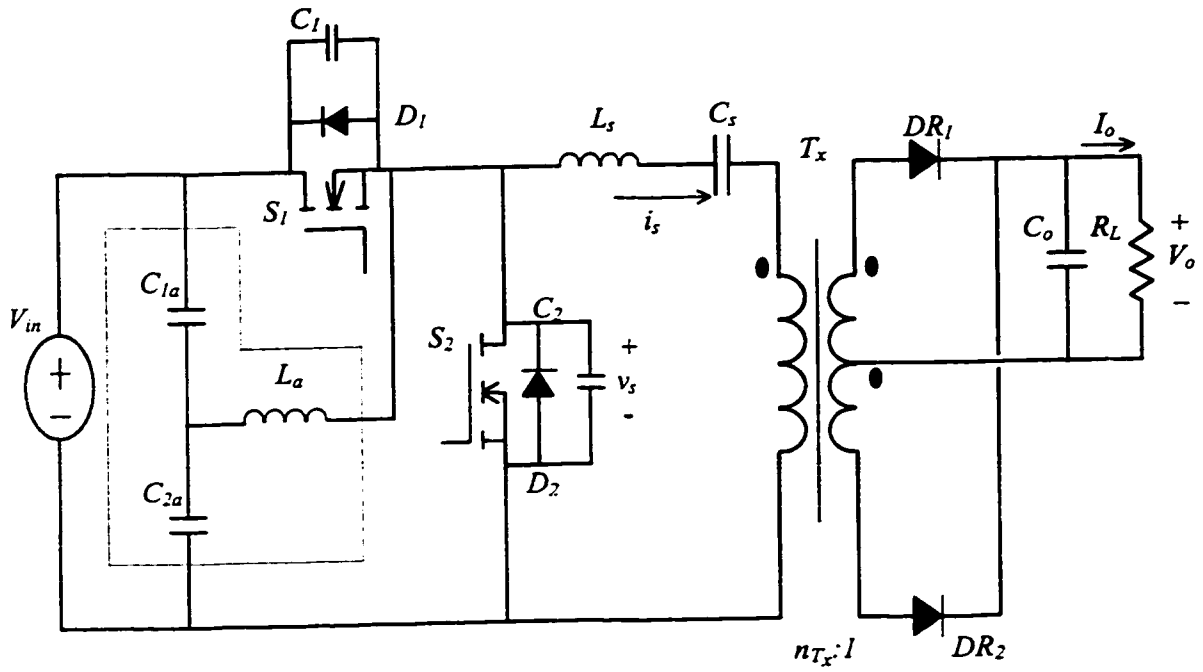


Fig.2.1 Asymmetrical Pulse-Width Modulated DC/DC Converter with Compensating Network

2.3 PRINCIPLE OF OPERATION

There exist four intervals within each switching time period, T_s. For each interval, the operation of the converter is described below.

Interval I: Prior to this interval S_2 was switched on. At the beginning of this interval the gate drive to S_2 is removed and this switch turns off. The currents flowing through the auxiliary inductor and the resonant branch are negative, thus forcing the discharging of C_1 and the charging of C_2. This charging-discharging process is complementary, i.e. as C_1 discharges from V_{in} to 0, C_2 charges from 0 to V_{in}. At any given moment throughout the cycle the total charge in both C_1 and C_2 is V_{in}. In order to maintain this, the voltage across L_a changes from $-V_2$ to V_1, where V_1 is the voltage across C_{1a} and

V_2 is the voltage across C_{2a}. In order to maintain the volt-second balance across the auxiliary inductor, V_1 and V_2 are given as follows:

$$V_1 = (1-D)V_{in} \tag{2-1}$$

$$V_2 = DV_{in} \tag{2-2}$$

Once C_1 has fully discharged and C_2 has fully charged, the negative currents force the conduction of diode D_1. The voltage across S_1 is now set at zero volts.

Interval II: At the beginning of this interval, gating signal v_{gs_1} is applied to the gate of S_1 to switch it on. The current previously flowing through D_1 now flows through S_1. The switch thus turns on under zero voltage. The voltage across L_a remains constant at V_1. Since C_2 maintains its charge, the voltage across S_2 is set at V_{in} during this interval. Power flows from the input DC source to the resonant circuit and to the output load.

Interval III: At the beginning of this interval, the gate drive to S_1 is removed and this switch is turned off. The currents flowing through the auxiliary inductor and the resonant branch are positive thus forcing the charging of C_1 and the discharging of C_2. The voltage across L_a changes from V_1 to $-V_2$. Once C_1 has fully charged and C_2 has fully discharged, the positive currents force the conduction of diode D_2. The voltage across S_2 is now set at zero volts.

Interval IV: At the beginning of this interval gating signal v_{gs2} is applied to the gate of S_2 to switch it on. The current previously flowing through D_2 now flows through S_2. Therefore, zero voltage switching is achieved at turn-on. The voltage across L_a remains constant at $-V_2$. The voltage across S_2 is set at zero volts during this interval since C_2

maintains its charge of zero volts. To maintain a constant supply of power to the output load, the energy stored in the resonant components during interval II now flows through S_2.

2.4 STEADY STATE ANALYSIS

This section will present the steady-state analysis of the circuit in Fig.2.1. It is first useful to introduce the assumptions prior to the analysis.

2.4.1 Assumptions

In presenting the analysis, the following assumptions will be made:

1) The semiconductor switches and diodes are ideal.

2) The effect of the capacitors across the switches is negligible.

3) The diode rectifier incurs zero losses

4) An AC equivalent resistance at the primary of the transformer represents the output rectification stage.

5) The delay time between the two switches is neglected.

In order to simplify the analysis, the circuit will be broken down into functional blocks as was shown in Fig.2.1. Since the analysis of the resonant tank will depend on the output stage, it will be examined first, followed by the analysis of the resonant tank and finally the switch network and the compensating network. Fig.2.2 shows the key waveforms of the proposed topology. These curves are based on the equations developed in the following pages.

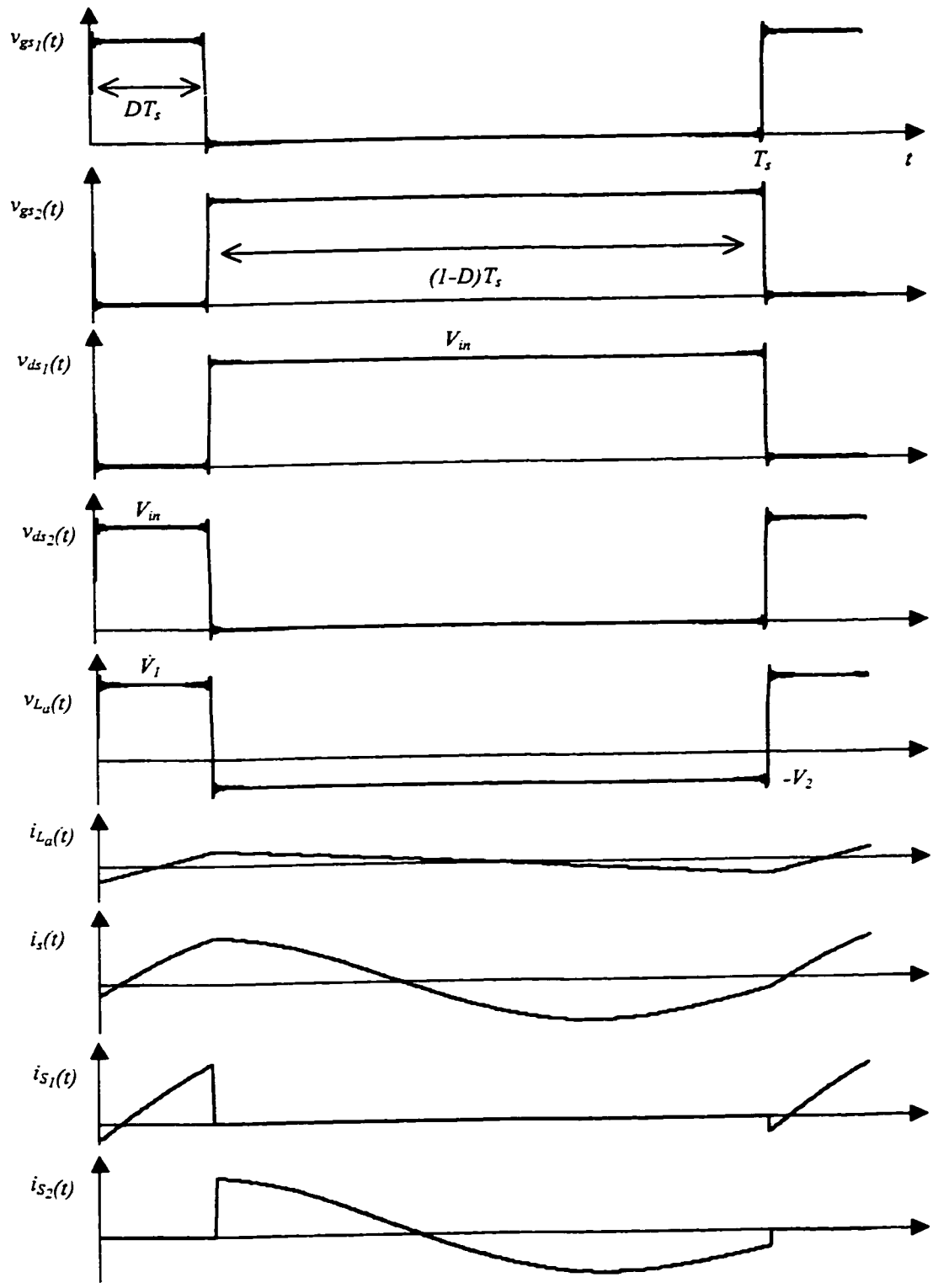


Fig.2.2 Ideal Waveforms of the APWM DC/DC Converter with Compensating Network

2.4.2 Output Stage

The purpose of the analysis here is to show how the entire output stage can be modeled as a resistance. This will then help in doing the analysis for the resonant network. The output stage consists of the rectifier network, the output filter and the load. The rectifier is driven by the nearly sinusoidal resonant tank current $i_s(t)$. A large capacitor C_o, then removes the higher harmonics so that only negligible harmonics are present at the load. For this part of the analysis, the power losses through the diode rectifier will be neglected, but will be examined in detail in section 2.5. This way, it can be approximated that the load (represented by a resistance R_L) has a DC voltage V_o across it and draws a DC current I_o. The input to the output stage is the output of the resonant tank, $v_r(t)$, namely an AC square-wave voltage where the positive and negative rails are proportional to V_o. It is also the voltage seen across the primary of the main transformer, T_x. We can express this waveform using Fourier series:

$$v_r(t) = \frac{4 n_{T_x} V_o}{\pi} \sum_{m=1,3,5,\ldots} \frac{1}{m} \sin(n\omega_s t - \varphi_s) \tag{2-3}$$

where φ_s represents the phase shift of $i_s(t)$, n_{T_x} represents the transformer turns ratio and ω_s is the switching frequency. Now if we consider only the first harmonic, Eq.(2-3) reduces to:

$$v_{r_1}(t) = \frac{4 n_{T_x} V_o}{\pi} \sin(\omega_s t - \varphi_s) \tag{2-4}$$

Likewise, the resonant current can also be expressed using Fourier series:

$$i_s(t) = \sum_m \frac{I_S}{m} \sin(n\omega_s t - \varphi_s) \tag{2-5}$$

where φ_s is the phase shift which takes into account the resonant components as well as the duty cycle, D. Its exact value will be shown in the following pages. If we consider only the fundamental harmonic, this current can be expressed as:

$$i_{s_1}(t) = I_{S_1} \sin(\omega_s t - \varphi_s) \tag{2-6}$$

where I_{S_1} is the peak of the fundamental component of the resonant current. At the output stage this current is half-wave rectified and then averaged by C_o to produce an essentially DC current. This is shown below where only the first harmonic is considered:

$$I_o = \frac{2n_{T_s}}{T_s} \int_0^{T_s/2} I_{S_1} \left|\sin(\omega_s t - \varphi_s)\right| dt = \frac{2n_{T_s}}{\pi} I_{S_1} \tag{2-7}$$

This current is proportional to I_{S_1}. Substitution of Eq.(2-7) into Eq.(2-6) and then division of Eq.(2-4) by Eq.(2-6) gives an expression for an equivalent resistance that is proportional to the output load:

$$R_{eq} = \frac{v_{R_1}(t)}{i_{S_1}(t)} = \frac{8n_{T_s}}{\pi^2} \frac{V_o}{I_o} = \frac{8n_{T_s}^2}{\pi^2} R_L \tag{2-8}$$

This result leads to the conclusion that the tank network is damped by an effective load resistance R_{eq} that is equal to approximately 81% of the actual load resistance R_L. The above analysis can be summarised by Fig.2.3.

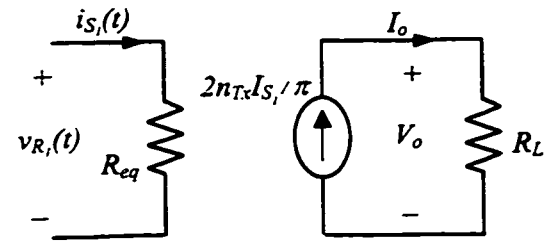


Fig.2.3 Equivalent Model of the Ideal Output Stage

The DC component of the output voltage can be expressed as

$$V_o = I_o R_L = \frac{2 n_{T_x} I_{S_1} R_L}{\pi} \tag{2-9}$$

This result demonstrates that the DC output voltage V_o is directly proportional to the peak of the resonant current, I_{S_1} and, therefore, can be regulated against load and line variations by varying I_{S_1} in such a way that the product of I_{S_1} and R_L remains constant. It will be seen in the following section that the resonant current is dependent on the duty cycle, D, therefore, the output voltage V_o is also a function of D.

2.4.3 Resonant Tank Network

The two gating functions, v_{gs_1} and v_{gs_2}, as shown in Fig.2.2, control the switch network. As explained earlier in section 2.3, when S_1 is turned on the input DC source is seen across S_2 and acts as a power source for the resonant circuit. At time $t = DT_s$, however, S_1 turns off and S_2 turns on, therefore, the voltage across S_2, namely v_{ds_2}, becomes zero volts. Therefore, v_{ds_2} or v_s, can be represented by its Fourier series in one switching cycle T_s as:

$$v_s(t) = V_{in} \cdot D + \sum_{n=1,3,5,\ldots} \frac{\sqrt{2} V_{in}}{n\pi} \left[\sqrt{1-\cos 2n\pi D} \cdot \sin\left(n\omega_s t + \theta_n\right) \right] \tag{2-10}$$

where,

$$\theta_n = \tan^{-1}\left[\frac{\sin 2n\pi D}{1-\cos 2n\pi D}\right] \tag{2-11}$$

It is shown that Eq.(2-10) includes both the DC and AC components where $V_{in} \cdot D$ represents the DC component. The resonant capacitor C_s will block the DC component from the transformer, so that only the AC component will pass through the transformer. Fig.2.4 shows the equivalent model that will be used to solve for the resonant current. Eqs. (2-8) and (2-10) have already defined R_{eq} and $v_s(t)$ respectively. It is also useful to define some terms given below:

$$f_r = \frac{1}{2\pi\sqrt{L_s C_s}} \tag{2-12}$$

$$\omega = \frac{f_o}{f_r} \tag{2-13}$$

$$Q = \frac{2\pi f_r L_s}{R_{eq}} = \frac{1}{2\pi f_r C_s R_{eq}} \tag{2-14}$$

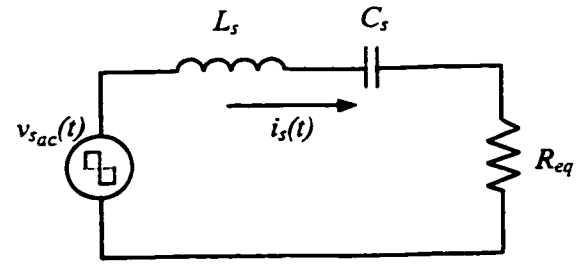


Fig.2.4 Equivalent Model of the Series Resonant Tank

Eq.(2-13) uses the resonant frequency f_r as a base value. The resonant current is essentially the voltage at the input of the resonant tank, Eq.(2-10), divided by the tank impedance. This is shown here:

$$i_s(t) = \sum_n \frac{\sqrt{2}V_{in}}{n\pi|Z_{in}|}\sqrt{1-\cos 2n\pi D}\cdot \sin(n\omega_s t + \theta_n - \phi_n) \tag{2-15}$$

where,

$$|Z_{in}| = R_{eq}\sqrt{1+Q^2\left(n\omega - \frac{1}{n\omega}\right)^2} \tag{2-16}$$

$$\phi_n = \tan^{-1}\left[Q\left(n\omega - \frac{1}{n\omega}\right)\right] \tag{2-17}$$

From Eq.(2-15), the peak value of the fundamental resonant current, I_{S1} can be given as:

$$I_{s_1} = \frac{\sqrt{2}V_{in}\cdot\sqrt{1-\cos(2\pi D)}}{\pi\cdot R_{eq}\sqrt{1+Q^2\left(\omega - \frac{1}{\omega}\right)^2}} \tag{2-18}$$

The time-varying voltages across the resonant capacitor and the resonant inductor are given by:

$$v_{C_s}(t) = -\sum_n \frac{\sqrt{2}QV_{in}}{n^2\omega\pi|Z_{in}|}\sqrt{1-\cos 2n\pi D}\cdot\cos(n\omega_s t + \theta_n - \phi_n) \tag{2-19}$$

$$v_{L_s}(t) = \sum_n \frac{\sqrt{2}\omega QV_{in}}{\pi|Z_{in}|}\sqrt{1-\cos 2n\pi D}\cdot\sin(n\omega_s t + \theta_n - \phi_n) \tag{2-20}$$

$$v_{L_r}(t) = \sum_n \frac{\sqrt{2}\omega Q V_{in}}{\pi |Z_{in}|} \sqrt{1-\cos 2n\pi D} \cdot \sin(n\omega_s t + \theta_n - \phi_n) \qquad (2\text{-}20)$$

2.4.4 Switch and Compensating Network

The switch currents are functions of both the resonant and auxiliary currents. The auxiliary inductor generates the auxiliary current. To solve for this current, the voltage across the auxiliary inductor v_{L_a}, must first be derived. As explained earlier, when S_1 is on, v_{L_a} is set at V_1 and when S_2 is on, v_{L_a} is set at $-V_2$. The Fourier series of this waveform is given as:

$$v_{L_a}(t) = \sum_n \frac{\sqrt{2} V_{in}}{n\pi} \sqrt{1-\cos 2n\pi D} \cdot \sin(n\omega_s t + \theta_n) \qquad (2\text{-}21)$$

As expected, this result is the same as the AC component of v_s. By integration of Eq.(2-21), the auxiliary inductor current, i_{L_a} can be found:

$$i_{L_a}(t) = \sum_n \frac{\sqrt{2} I_a}{(n\pi)^2 D(1-D)} \sqrt{1-\cos 2n\pi D} \cdot \sin(n\omega_s t + \delta_n) \qquad (2\text{-}22)$$

where,

$$I_a = \frac{D(1-D)V_{in}}{2 f_s L_a} \qquad (2\text{-}23)$$

$$\delta_n = \tan^{-1}\left(\frac{\cos 2n\pi D - 1}{\sin 2n\pi D}\right) \qquad (2\text{-}24)$$

I_a represents the peak of the auxiliary current. The current through the switches is then the sum of the resonant current and the auxiliary current:

$$i_{sw}(t) = \sum_n \frac{\sqrt{2}V_{in}}{n\pi}\sqrt{1-\cos 2n\pi D}\left[\frac{1}{|Z_{in}|}\cdot \sin(n\omega_s t + \theta_n - \phi_n) + \frac{1}{2n\pi f_s L_a}\cdot \sin(n\omega_s t + \delta_n)\right]$$

(2-25)

It should be noted that Eq.(2-25) is valid only when the switches are on (during intervals II and IV for S_1 and S_2 respectively). When the switches are off, the current is zero. To complete the analysis, the input current $i_d(t)$ will also be presented. The value of this current depends on which switch is on. During interval II when S_1 is on ($0 \le t \le DT_s$), the input current is:

$$i_d(t) = i_s(t) + i_{C_{2a}}(t) \qquad (2\text{-}26)$$

where i_{C2a} is equal to half of the auxiliary current. The auxiliary current divides equally among the two compensating network capacitors, C_{1a} and C_{2a}. With this in mind $i_d(t)$ becomes:

$$i_d(t) = \sum_n \frac{\sqrt{2}V_{in}}{n\pi}\sqrt{1-\cos 2n\pi D}\left[\frac{1}{|Z_{in}|}\cdot \sin(n\omega_s t + \theta_n - \phi_n) + \frac{1}{4n\pi f_s L_a}\cdot \sin(n\omega_s t + \delta_n)\right]$$

(2-27)

During interval IV when S_2 is on ($DT_s \le t \le T_s$), the input current is:

$$i_d(t) = i_{C_1}(t) = \sum_n \frac{\sqrt{2}V_{in}}{4(n\pi)^2 f_s L_a} \sqrt{1-\cos 2n\pi D} \cdot \sin(n\omega_s t + \delta_n) \qquad (2\text{-}28)$$

Fig.2.5 illustrates an equivalent circuit for the switch network. It models the input current as well as the auxiliary and resonant currents.

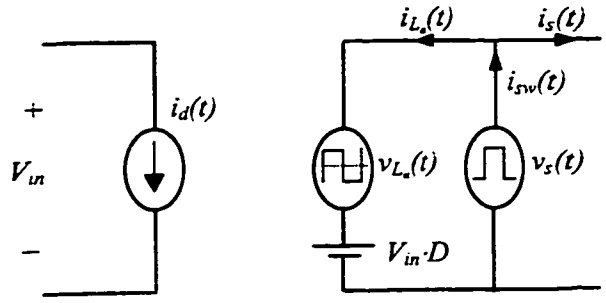


Fig.2.5 Equivalent Model of the Switch Network including the Compensating Network

2.4.5 Modified APWM Series Resonant Converter

Fig.2.6 shows the equivalent circuit of the entire modified APWM series resonant converter. It is a combination of Figs.2.3, 2.4 and 2.5.

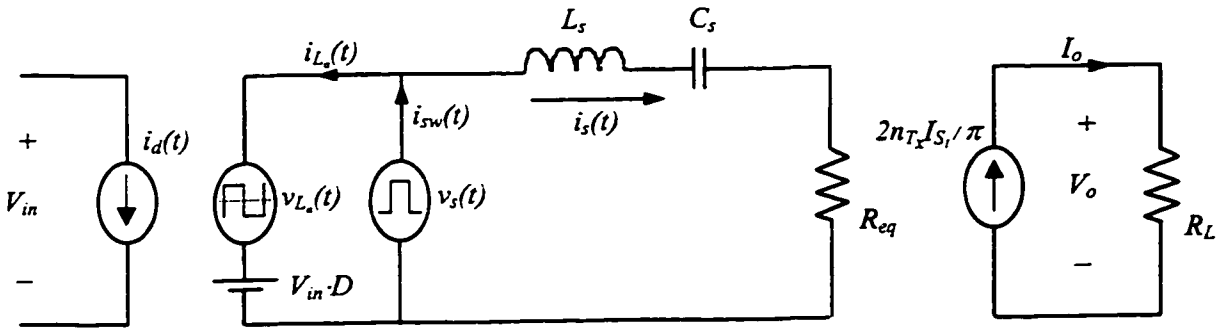


Fig. 2.6 Equivalent Model of the Asymmetrical Pulse-Width Modulated DC/DC Series Resonant Converter with Compensating Network

From Eqs. (2-9) and (2-18), we can form the voltage conversion ratio M. This is the ratio between the output and input voltages:

$$M = \frac{V_o}{V_{in}} = \frac{2\sqrt{2}\, n_{T_s} R_L}{\pi^2} \cdot \frac{\sqrt{1-\cos(2\pi D)}}{\sqrt{R_{eq}^2 + Q^2\left(\omega - \frac{1}{\omega}\right)^2}} \tag{2-29}$$

This is plotted in Fig.2.7.

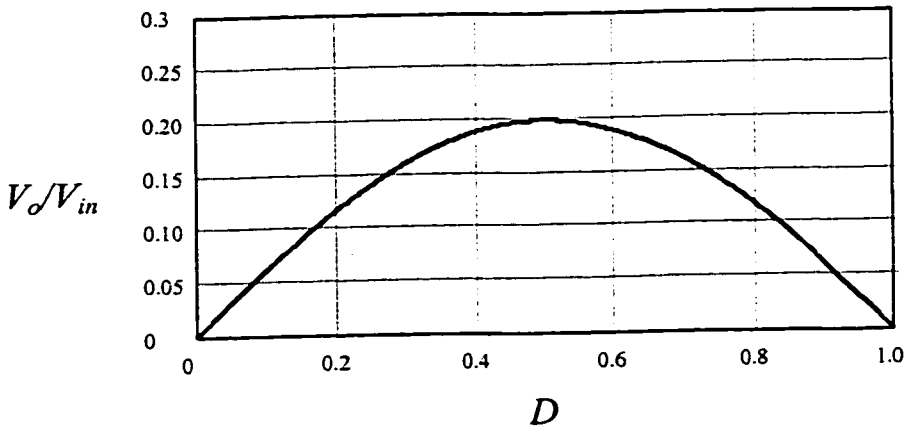


Fig.2.7 Output Voltage Normalized to V_{in} as a Function of Duty Cycle for Q=4.8 and ω=1.1

For a lossless converter, the input power is equal to the output power, i.e. $V_o I_o = V_{in} I_d$, or:

$$\frac{V_o}{V_{in}} = \frac{I_d}{I_o} = M \tag{2-30}$$

With Eqs. (2-7) and (2-29) the output power of the converter is given by:

$$P_o = V_o I_o = V_{in} M \cdot \frac{2 n_{T_s}}{\pi} \cdot I_{s_1} \tag{2-31}$$

Using Eq.(2-31), the current drawn from the inverter is given by:

$$I_{s_1} = \frac{P_o}{V_{in}} \cdot \frac{\pi}{2n_{T_x}} \cdot \frac{1}{M} \tag{2-32}$$

Eq.(2-31) shows that for a given P_o and V_{in}, the current I_{s1} drawn from the inverter is inversely proportional to the voltage gain, M.

The above equations demonstrate the analysis for a lossless converter. When determining the efficiency, however, the losses throughout the circuit must be taken into consideration. Fig.2.8a shows the equivalent circuit of the inverter including the parasitic resistances [34]. The power MOSFETs are modeled as ideal switches in series with the on-resistances r_{DS1} and r_{DS2}. The equivalent series resistance of the resonant inductor is r_L and the equivalent series capacitance is r_C. In Fig.2.8b, the DC voltage source V_{in} and the switches are modeled by a square-wave voltage source, v_s, and the averaged parasitic resistance of the MOSFETs as:

$$r_{DS} = r_{DS1} D + r_{DS2} (1-D) \tag{2-33}$$

The total parasitic resistance r is given by:

$$r = r_{DS} + r_L + r_C \tag{2-34}$$

The previous equation shows the sources of power loss in the inverter. This gives rise to the total conduction power loss in the resonant circuit and the two switches:

$$P_r = \frac{I_{S_1}^2 (r_{DS} + r_L + r_C)}{2} = \frac{I_{S_1}^2 r}{2} \tag{2-35}$$

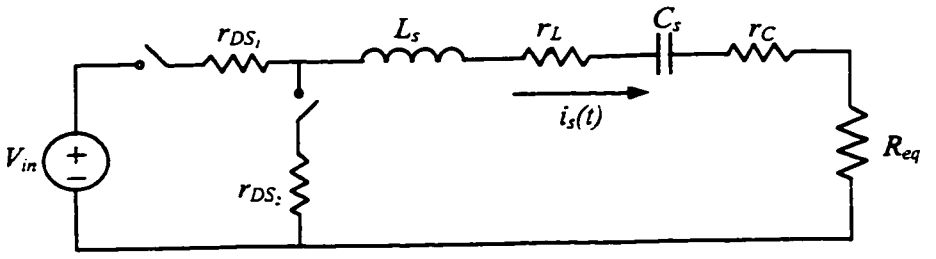
The output power of the inverter or the input power to the rectifier is given by:

$$P_{R_{eq}} = \frac{I_{S_1}^2 R_{eq}}{2} \tag{2-36}$$

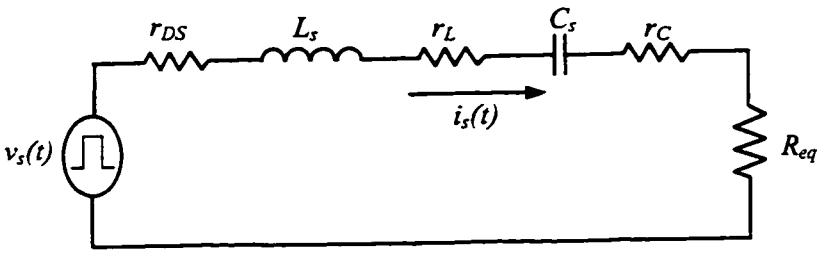
Under the assumption of ZVS, the efficiency of the inverter is given by:

$$\eta_l = \frac{P_{R_{eq}}}{P_{R_{eq}} + P_r} = \frac{R_{eq}}{R_{eq} + r} = 1 - \frac{1}{1 + \frac{R_{eq}}{r}} \tag{2-37}$$

It can be seen that the inverter efficiency depends on R_{eq}/r and as R_L increases, R_{eq} increases; thus maintaining high efficiency at light loads.



(a)



(b)

Fig.2.8 Equivalent Models of the Converter including Parasitic Resistances: a)parasitic resistance of each element, b)combination of switch parasitic resistance

2.5 DIODE RECTIFIER ANALYSIS

For an ideal diode, the forward voltage drop is zero. In practice, when a diode is forward-biased, it can be represented as a small voltage source, V_F, in series with a constant resistance R_F. The voltage source V_F represents the diode threshold voltage and R_F represents the diode forward resistance. Fig.2.9a shows the center-tapped diode

rectifier where the resonant current is represented as a current source i_s [35]. Fig.2.9b shows the model for $i_s > 0$ and Fig.2.9c shows the model for $i_s < 0$. Fig.2.10 gives the waveforms of the diode rectifier. The currents through DR_1 and DR_2, (i_{DR_1} and i_{DR_2}, respectively) are given by:

$$i_{DR_1} = \frac{\cos(x) - \sin(x)}{2} + \sum_{n,even} \frac{1}{\pi}\left[\frac{\cos(x)}{1-n} + \frac{\cos(x)}{1+n}\right] \cdot \cos(n\omega_s t) - \sum_{n,even} \frac{1}{\pi}\left[\frac{\sin(x)}{1+n}\right] \cdot \sin(n\omega_s t) \quad (2\text{-}38)$$

and,

$$i_{DR_1} = \frac{\sin(x) - \cos(x)}{2} + \sum_{n,even} \frac{-1}{\pi}\left[\frac{\cos(x)}{1-n} + \frac{\cos(x)}{1+n}\right] \cdot \cos(n\omega_s t) + \sum_{n,even} \frac{1}{\pi}\left[\frac{\sin(x)}{1+n}\right] \cdot \sin(n\omega_s t) \quad (2\text{-}39)$$

where $x = \phi - \theta$. The waveforms are shown in Fig.2.10.

The current flowing through the output load of C_o and R_L is given by:

$$i_{CR} = i_{DR1} + i_{DR2} = n_{T_x} |i_s(t)| = n_{T_x} I_{S_1} |\sin(\omega_s t) + \theta + \phi| \quad (2\text{-}40)$$

The average current through each diode is $I_{D(av)} = I_o/2$. The power dissipated in each diode due to V_F is:

$$P_{V_F} = V_F I_{D(av)} = \frac{V_F I_o}{2} \quad (2\text{-}41)$$

and due to R_F is

$$P_{R_F} = R_F I_{D,rms}^2 = \frac{\pi^2 I_o^2 R_F}{16} . \tag{2-42}$$

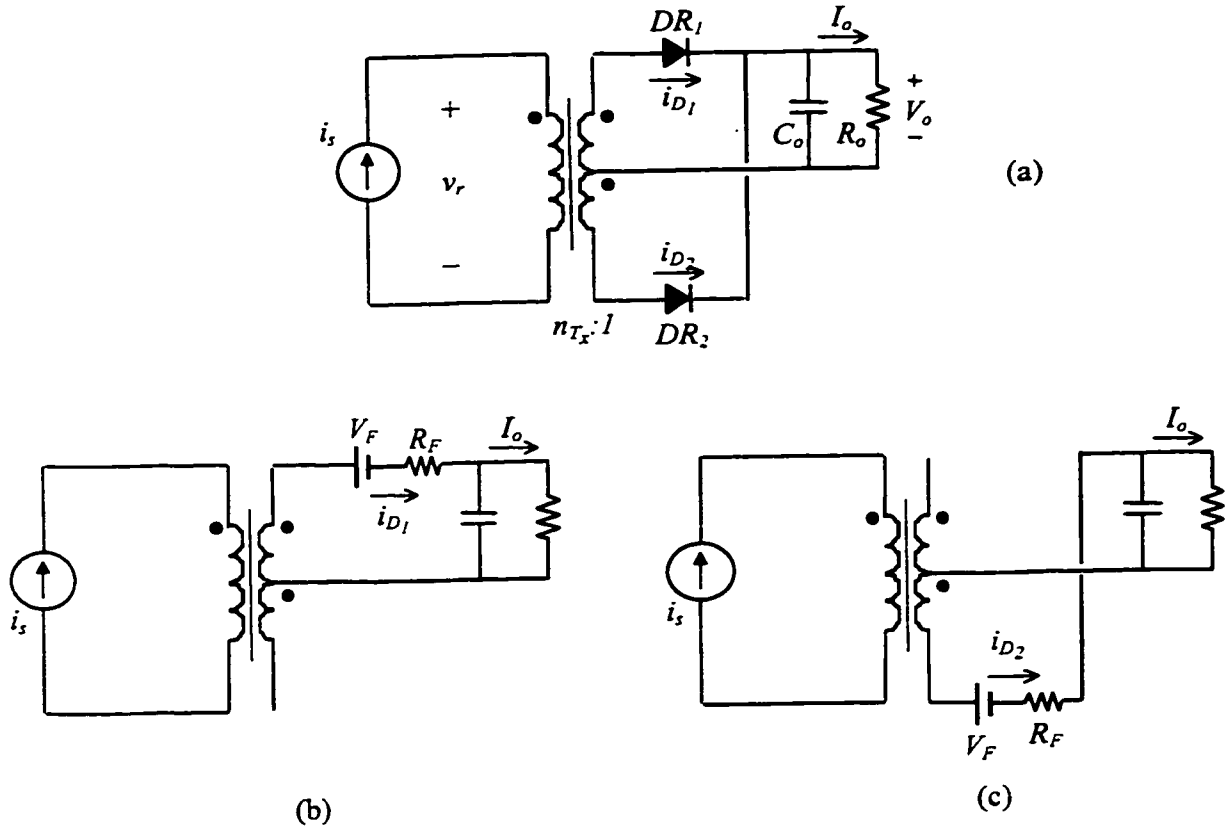


Fig.2.9 Center-Tapped Rectifier: a)circuit b)model for $i_s > 0$ c) model for $i_s < 0$

Therefore, the total power loss in one diode is:

$$P_D = P_{V_F} + P_{R_F} = \frac{V_F I_o}{2} + \frac{\pi^2 I_o^2 R_F}{16} = I_o^2 R_L \left(\frac{V_F}{2V_o} + \frac{\pi^2 R_F}{16 R_L} \right) \tag{2-43}$$

and the total power loss of the diode rectifier is:

$$P_c = 2P_D = I_o^2 R_L \left(\frac{V_F}{V_o} + \frac{\pi^2 R_F}{8 R_L} \right) . \tag{2-44}$$

It is also useful to include the efficiency of the output rectifier. It is given as:

$$\eta_R = \frac{P_o}{P_i} = \frac{P_o}{P_o + P_c} = \frac{1}{1 + \frac{I_o R_L}{V_o}\left(\frac{V_F}{V_o} + \frac{\pi^2 R_F}{8 R_L}\right)} \qquad (2\text{-}45)$$

2.6 SIMULATION RESULTS

The performance of the modified APWM series resonant converter depicted in Fig.2.1 was analyzed using a standard electronic simulation software (MicroSim Pspice). The circuit is a 5V, 30W converter operating with an input voltage of 80V at 500kHz. Schottky diodes were used in the output rectifier for their low forward voltage drop characteristics. This circuit was simulated under steady-state operating conditions. Fig.2.11 shows the key waveforms similar to the theoretical waveforms shown in Fig.2.2. As discussed in section 2.2, these simulation results indicate the deadtime and the operating intervals. They show good comparison with the theoretical waveforms. At the beginning of interval III, S_1 is switched on under zero-voltage switching. Similarly for S_2, interval I shows turn-on at ZVS.

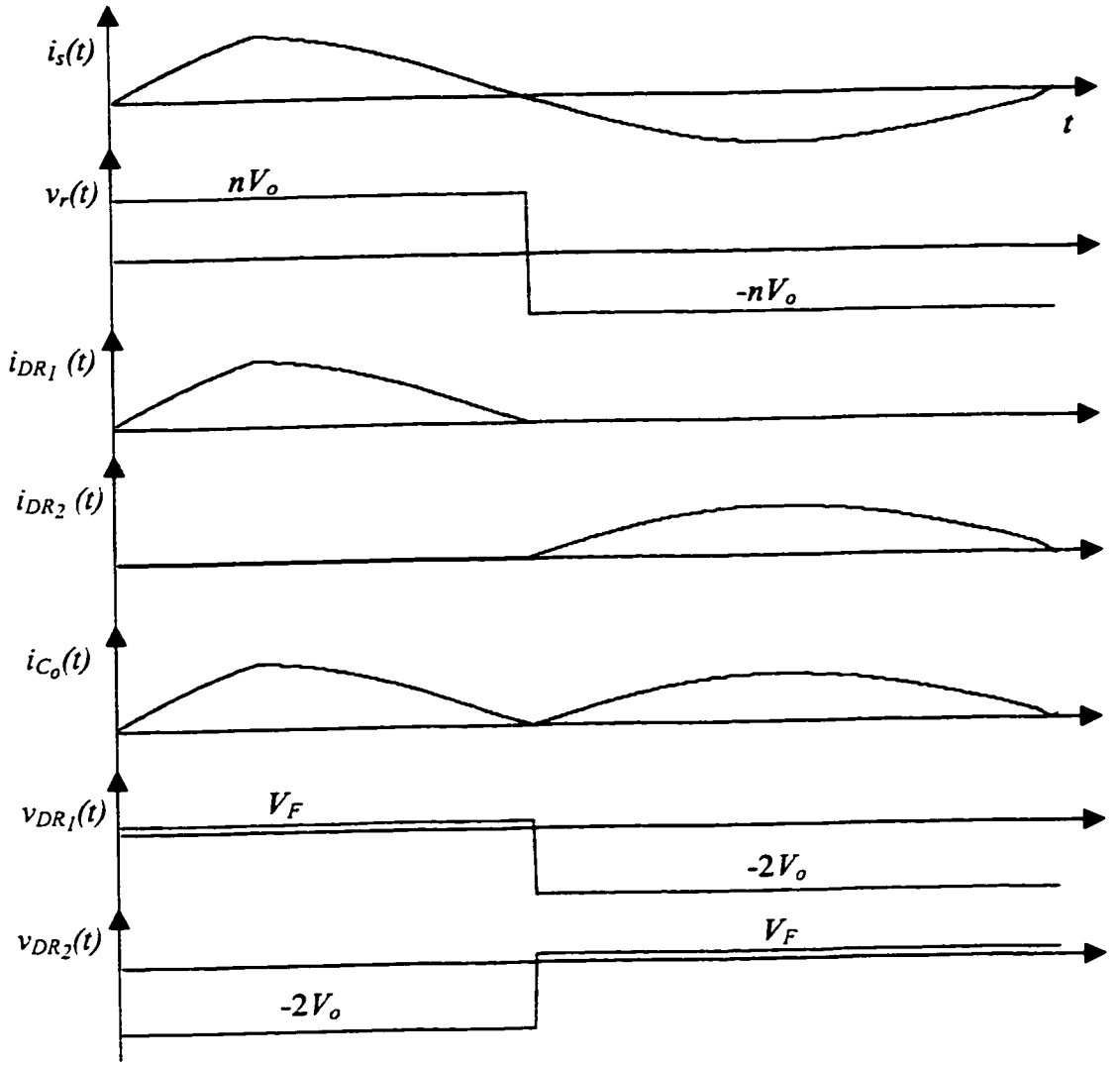


Fig.2.10 Diode Rectifier Waveforms from Circuit in Fig.2.9

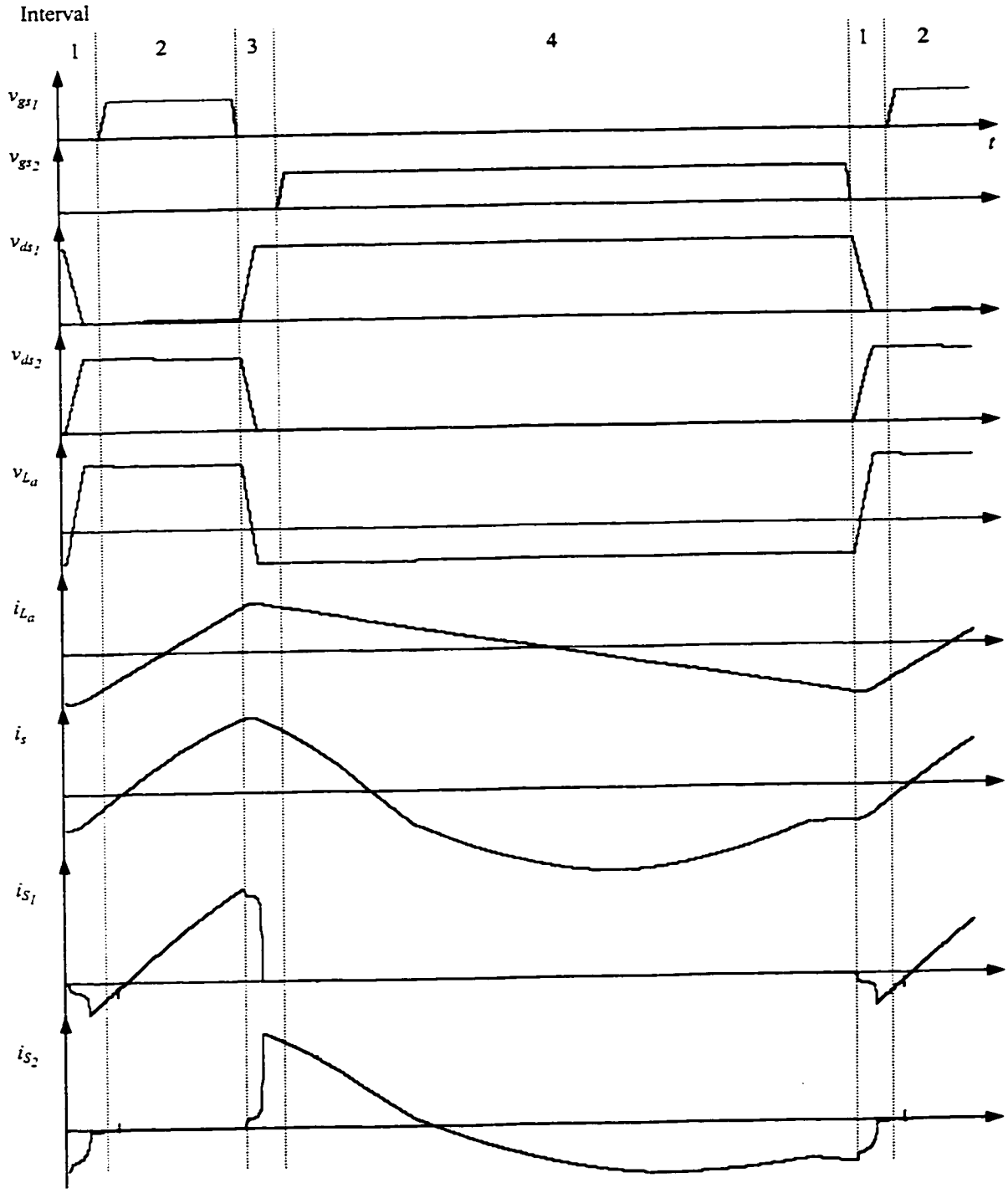


Fig.2.11 Simulation Results of APWM Series Resonant DC/DC Converter with Compensating Network

2.7 EXPERIMENTAL RESULTS

To verify this modified topology, a 30W converter with a 5V output was constructed. The switching frequency was 500kHz. The input voltage was 40V, operating at 70% full load. In the resonant circuit, the following values were used: the resonant capacitor was 44nF, the resonant inductor was 3μH and the transformer turns ratio was 2.5 to 1. The value of the auxiliary inductor used was 3μH, therefore, K was equal to 1. The capacitors in the auxiliary circuit (C_{1a}, C_{2a}) were chosen as 2.2μF. Schottky diodes (MBR2545) were used as part of the diode rectifier. Fig.2.12 shows the voltage and current waveforms of the auxiliary inductor (v_{L_a} and i_{L_a} respectively). Fig.2.13 shows the resonant tank current, i_s. Fig.2.14 shows the voltage and current waveforms of S_1. Fig.2.15 shows the voltage and current waveforms of S_2. The experimental results match the results from both the theoretical and computer simulation analyses. The main goal of the modified topology is to achieve ZVS for higher input voltages. Fig.2.16 demonstrates this for S_1 and Fig.2.17 demonstrates this for S_2 [33]. The input voltage was set at 80 V at full load. On both figures, the dotted vertical line shows that the drain-to-source voltage reaches zero before the gate signal is applied.

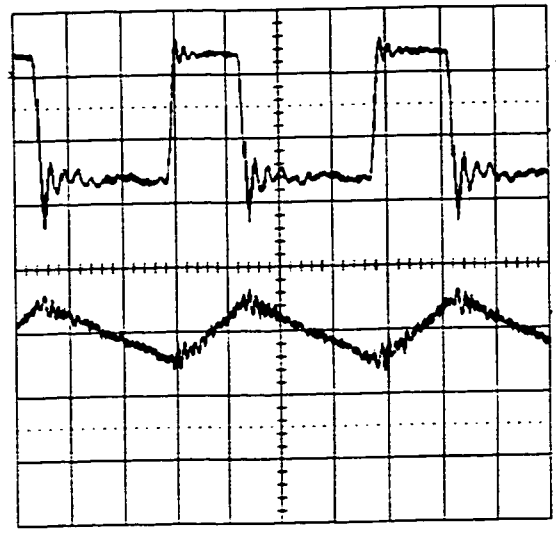


Fig.12 Voltage and Current Waveforms of Auxiliary Inductor from Experimental Analysis: top trace, v_{L_a} (20V/div);bottom trace, i_{L_a} (5A/div); time scale is 0.5μs/div; f_s=500kHz; V_{in}=40V; V_o=4.5V P_o=21W

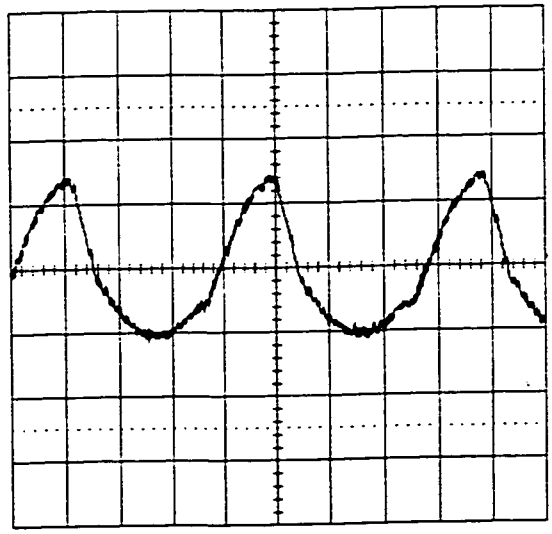


Fig.2.13 Resonant Current Waveform from Experimental Analysis: (5A/div), time scale is 0.5μs/div; f_s=500kHz; V_{in}=40V; V_o=4.5V; P_o=21W

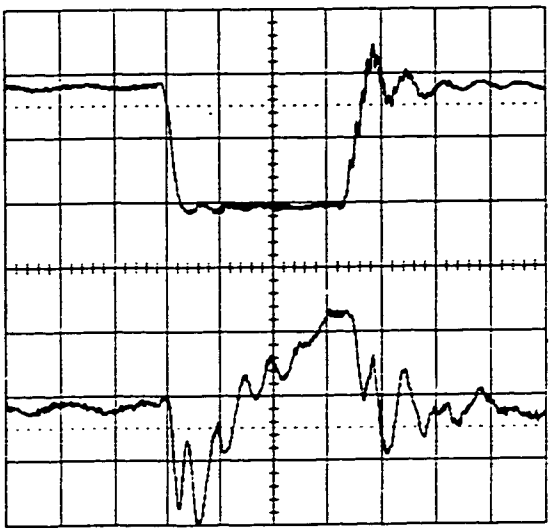


Fig.2.14 Voltage and Current Waveforms of S_1 from Experimental Analysis : top trace, v_{dS_1} (20V/div); bottom trace, i_{S_1} (5A/div); time scale is 0.2μs/div; f_s=500kHz; V_{in}=40V; V_o=4.5V; P_o=21W

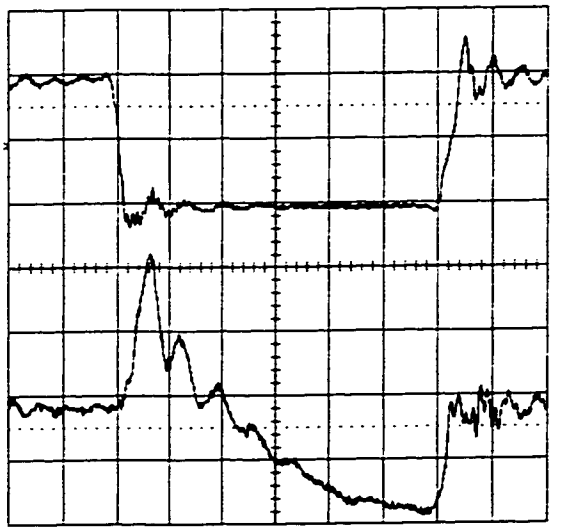


Fig.2.15 Voltage and Current Waveforms of S_2 from Experimental Analysis: top trace, v_{dS_2} (20V/div); bottom trace, i_{S_2} (5A/div); time scale is 0.2μs/div; f_s=500kHz; V_{in}=40V; V_o=4.5V; P_o=21W

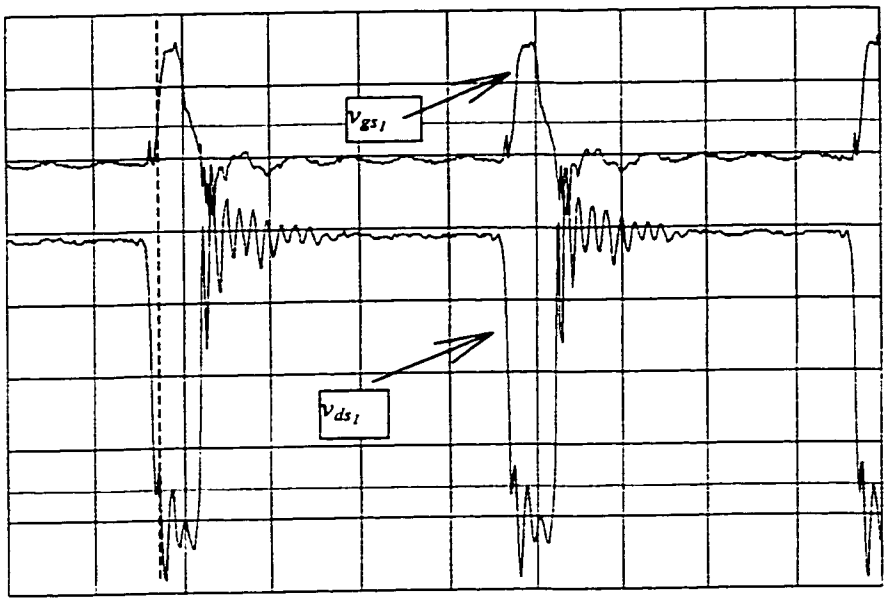


Fig.2.16. Waveforms at Turn-On of Switch S_1 at V_{in}=80V from Experimental Analysis. Top trace: gate signal (5 V/div, 5 μs/div). Bottom trace: drain-to-source voltage (20 V/div, 5 μs/div). V_{in}=80V; f_s=500 kHz; V_o=4.8V; P_o=30W.

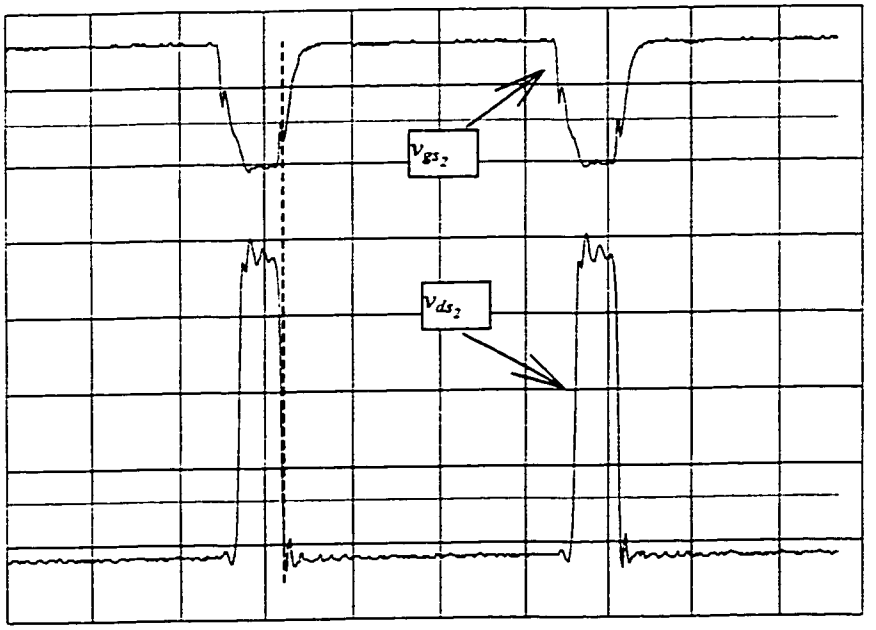


Fig.2.17 Waveforms at Turn-On of Switch S_2 at V_{in}=80V from Experimental Analysis. Top trace: gate signal (5 V/div, 5 μs/div). Bottom trace: drain-to-source voltage (20 V/div, 5 μs/div). V_{in}=80V; f_s=500 kHz; V_o=4.8V; P_o=30W.

2.8 COMPARISON BETWEEN ORIGINAL AND MODIFIED TOPOLOGIES

The mode of operation described in section 2.3 is similar to the operation of the original APWM resonant DC/DC converter, yet at higher voltages, ZVS is lost while this new topology maintains it. For example, at V_{in} = 80 volts, Fig.2.18 shows that ZVS is lost for S_1 in the original circuit [33]. Notice that for S_1 to achieve ZVS, the resonant current (which is also the current that flows through the switches) at the turn-off of S_2, must have enough negative current in order to discharge C_1, thus ZVS is lost. With the addition of the auxiliary branch, however, it supplies the additional current to the switch in order to discharge C_1 and achieve ZVS. The current through this auxiliary branch acts as a compensation for the resonant current when the input voltage increases, whereas, earlier the original APWM was limited to a narrow range of input voltage.

Fig.2.19 shows the efficiency, η, of the modified topology and the original one in relation with the input voltage [33]. It is easily seen that overall, the modified topology has a higher efficiency than the original design. This is more evident at higher voltages where the efficiency of the original design begins to fall after 55V. The main reason for this is the loss of ZVS and soft switching at higher voltages. The efficiency of the modified topology however is consistent at 81% throughout the whole input voltage range with a variation of about 1% with the efficiency of the original topology. The variation increases up to 3% above an input voltage of 55V at which point the original topology begins to show reduced efficiency.

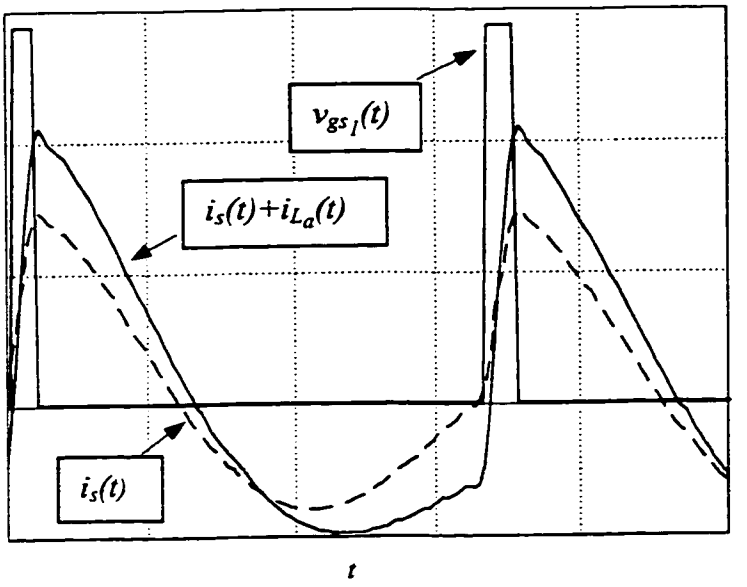


Fig. 2.18 Waveforms of Original and Modified APWM Resonant DC/DC Converter with K=1, Q=2.5

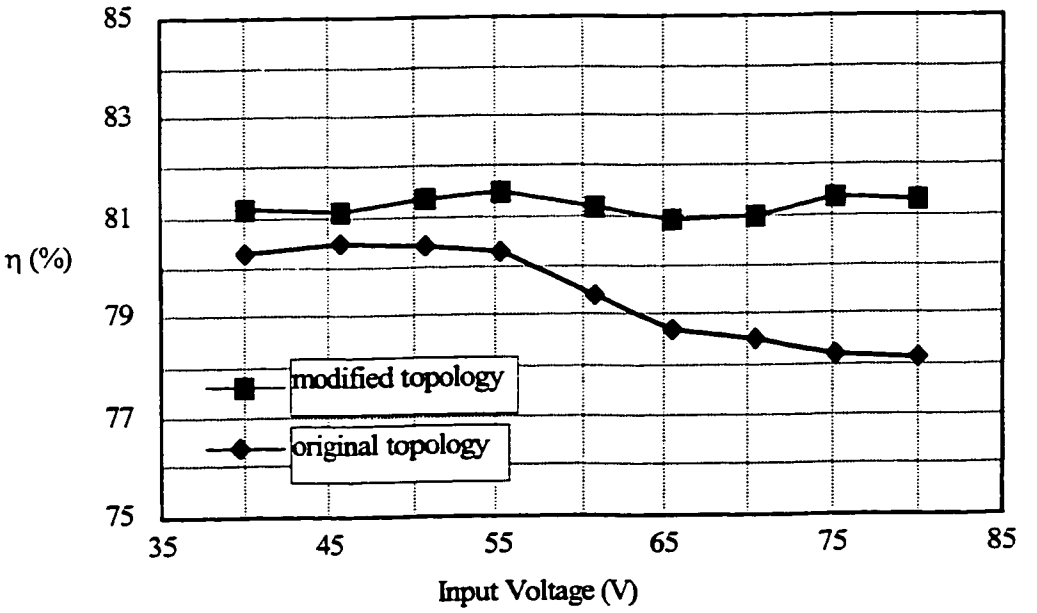


Fig.2.19 Efficiency, η, of Original APWM resonant DC/DC Converter and Modified Topology with Variation of Input Voltage

Fig.2.20 shows the efficiency, η, of the modified topology and the original one in relation with the load current [33]. It can be seen that the modified topology shows about 2% higher efficiency than the original converter.

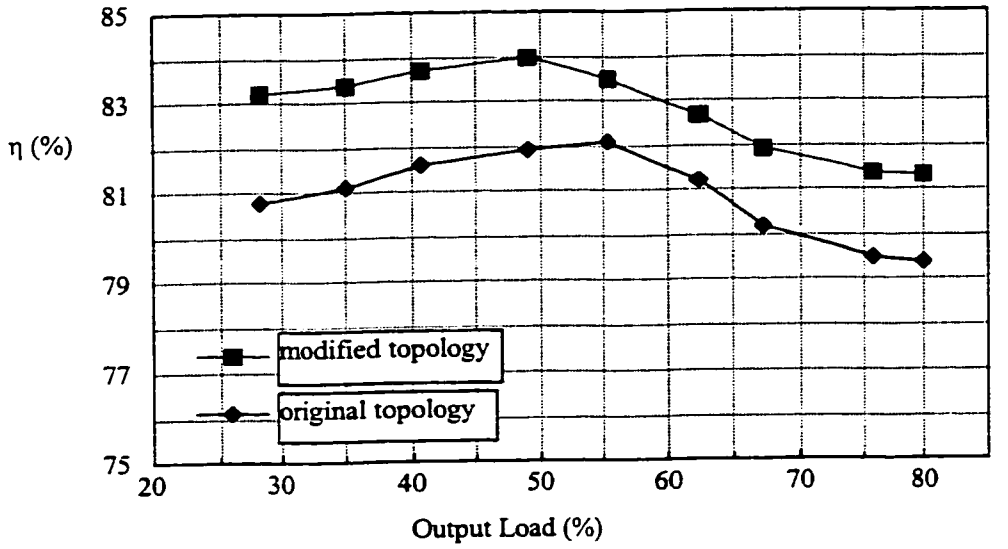


Fig.2.20 Efficiency, η, of Original APWM Resonant DC/DC Converter and Modified Topology with Variation of Output Load

2.9 CONCLUSIONS

This chapter has presented the modified APWM series resonant DC/DC converter. Steady-state analysis was done and compared favourably with the results of computer simulation. They have also shown the benefits of this modified topology including ZVS over a wider input voltage range due to the compensating nature of the auxiliary network. The diode rectifier was analyzed and it was found that its losses are due to the forward voltage drop of the diode as well as its on-state resistance. A prototype of the converter was built and experimental results showed not only the presence of ZVS at input voltage of 80V, but an improved efficiency performance as well.

Chapter 3

Design of Modified Topology

3.1 INTRODUCTION

It was shown in the last chapter how the performance improved with the addition of the compensating network. With proper selection of components, the design can achieve optimum results. Using the equations developed in the last chapter, performance curves are realized to determine the best parameter values. A design example of the converter is given to illustrate the selection of the major components. The design is based on the required specifications such as, input voltage range, switching frequency, duty cycle range, etc.

The breakdown of this chapter is as follows. Section 3.2. presents performance curves based on the currents flowing through the main power MOSFET switches. These curves will be referred to in the design example and will help to determine optimum values. Section 3.3 begins by outlining the design specifications. A design example follows and it demonstrates the selection of the major components, including the resonant components, output capacitor, transformer turns ratio, etc. Lastly, section 3.4 draws the conclusions from this chapter.

3.2 PERFORMANCE CURVES

3.2.1 Definition of *K*

It will be useful in the design analysis to relate the auxiliary inductor to the resonant inductor. This will be done with use of a variable *K*:

$$K = \frac{L_a}{L_s} \tag{3-1}$$

Using Eq.(2-14) and Eq.(2-22) the auxiliary current peak I_a, can be rewritten as:

$$I_a = \frac{D(1-D)V_{in}\,\pi}{K\omega Q} \tag{3-2}$$

This equation will be used to plot the design curves.

3.3.2 Turn-off current I_2 of Switch S_2

In order to achieve ZVS for S_1, the current at the turn-off of S_2 must be negative. Using Eq.(2-15) and Eq.(2-22) and solving them at $t = T_s^-$ just before S_2 is about to switch off, the current through S_2 is given as:

$$I_2 = \sum_n \frac{\sqrt{2}}{n\pi} \cdot \sqrt{1-\cos 2n\pi D} \cdot \left[\frac{V_{in}}{Z_{in}} \sin(\theta_n - \phi_n) + \frac{I_a \sin(\delta_n)}{(n\pi)D(1-D)} \right] \tag{3-3}$$

Figs.3.1-3.3 show the plots of Eq.(3-3) as a function of *D* with various values for Q, ω, and *K*. Fig.3.1 is for *K*=0.1, Fig.3.2 is for *K*=1 and Fig.3.3 is for *K*=2. Operation with ZVS is achievable over the range of *K* values listed. The current through the auxiliary inductor and hence the current through the switches is inversely proportional to the value of the inductor, i.e. as the value of *K* (or L_a) decreases, the amount of current present increases.

3.2.3 Turn-off current I_1 of Switch S_1

In order to achieve ZVS for S_2, the current at the turn-off of S_1 must be positive. Using Eq.(2-15) and Eq.(2-22) and solving them at $t = DT_s^-$ just before S_1 is about to switch off, the current through S_1 is given as:

$$I_1 = \sum_n \frac{\sqrt{2}}{n\pi} \cdot \sqrt{1-\cos 2n\pi D} \cdot \left[\frac{V_{in}}{|Z_{in}|} \sin(2n\pi D + \theta_n - \phi_n) + \frac{I_a \sin(2n\pi D + \delta_n)}{(n\pi)D(1-D)} \right] \tag{3-4}$$

Figs.3.4-3.6 show the plots of Eq.(3-4) as a function of D with various values for Q, ω and K. Fig.3.4 is for K=0.1, Fig.3.5 is for K=1 and Fig.3.6 is for K=2. From these graphs, it is apparent that ZVS in S_2 is lost for high values of K. However, if K is too small, then the current through L_a and hence the switches becomes too big. This results in conduction losses. It is important that the right value of K is chosen for operation with ZVS and low conduction losses.

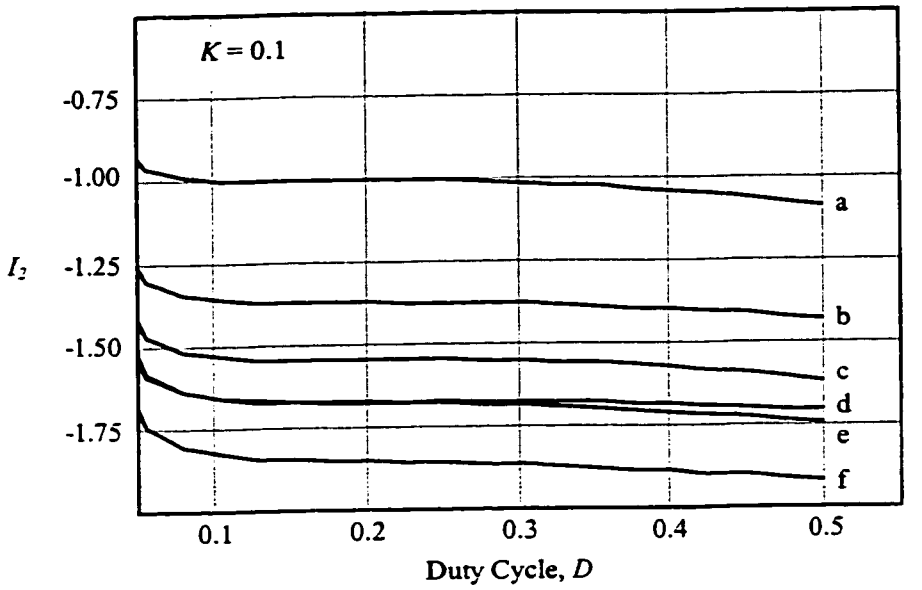


Fig.3.1 Current through S_2 at turn-off, I_2, as a function of D for $K = 0.1$
a:Q=2.5, ω=1.1; b:Q=2.5, ω=1.3; c: Q=1.5, ω=1.1; d: Q=2.5, ω=1.5; e: Q=1.5, ω=1.3; f: Q=1.5, ω=1.5

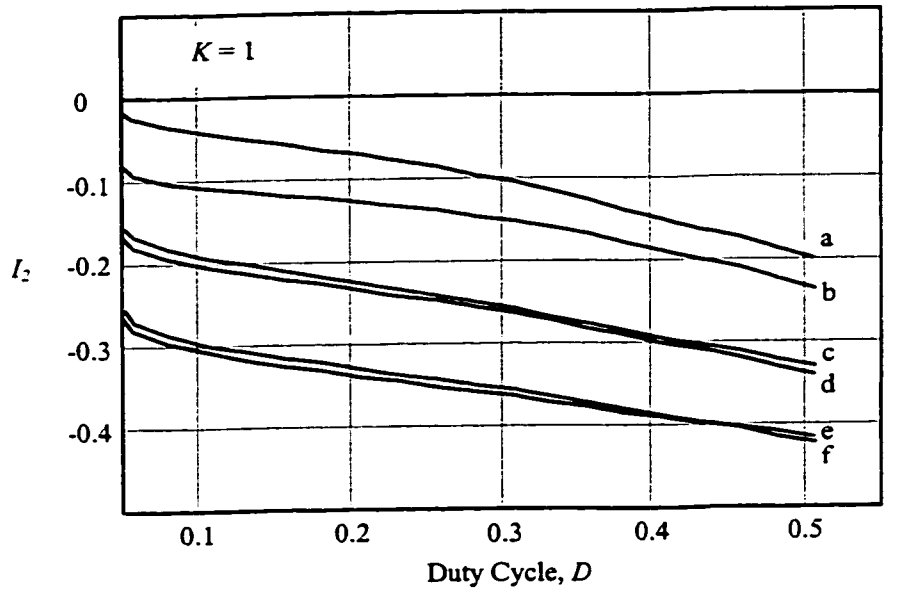


Fig.3.2 Current through S_2 at Turn-Off, I_2, as a Function of D for $K = 1$
a:Q=2.5, ω=1.1; b:Q=1.5, ω=1.1; c: Q=2.5, ω=1.3; d: Q=1.5, ω=1.3; e: Q=2.5, ω=1.5; f: Q=1.5, ω=1.5

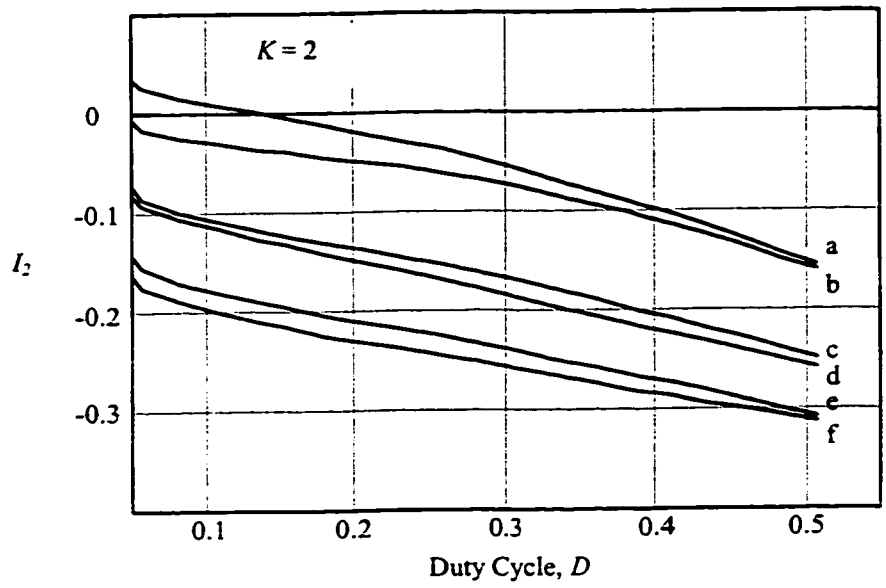


Fig.3.3 Current through S_2 at Turn-Off, I_2, as a Function of D for $K = 2$
a:Q=2.5, ω=1.1; b:Q=1.5, ω=1.1; c: Q=1.5, ω=1.3; d: Q=2.5, ω=1.3; e: Q=1.5, ω=1.5; f: Q=2.5, ω=1.5

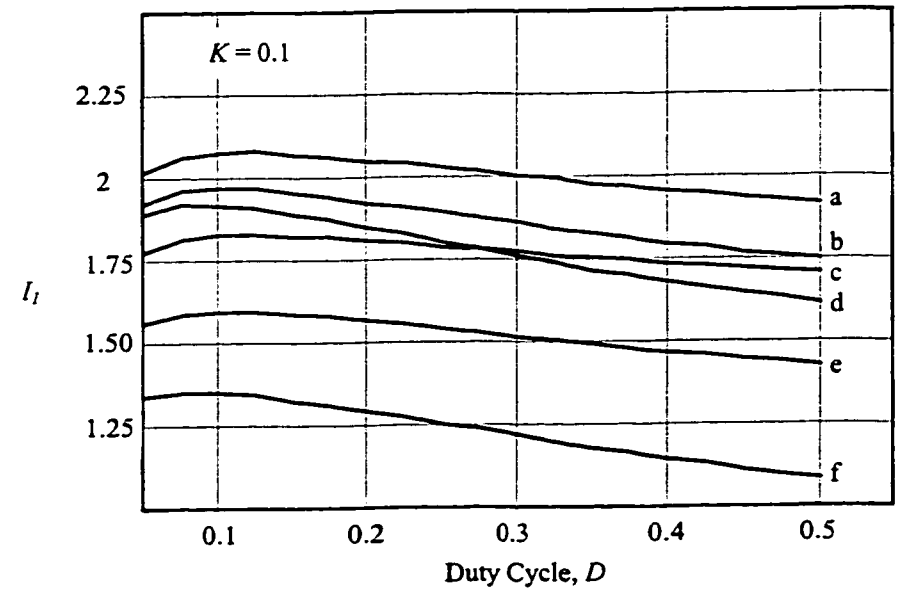


Fig.3.4 Current through S_1 at Turn-Off, I_1, as a Function of D for $K = 0.1$
a:Q=1.5, ω=1.5; b:Q=1.5, ω=1.3; c: Q=2.5, ω=1.5; d: Q=2.5, ω=1.1; e: Q=2.5, ω=1.3; f: Q=1.5, ω=1.1

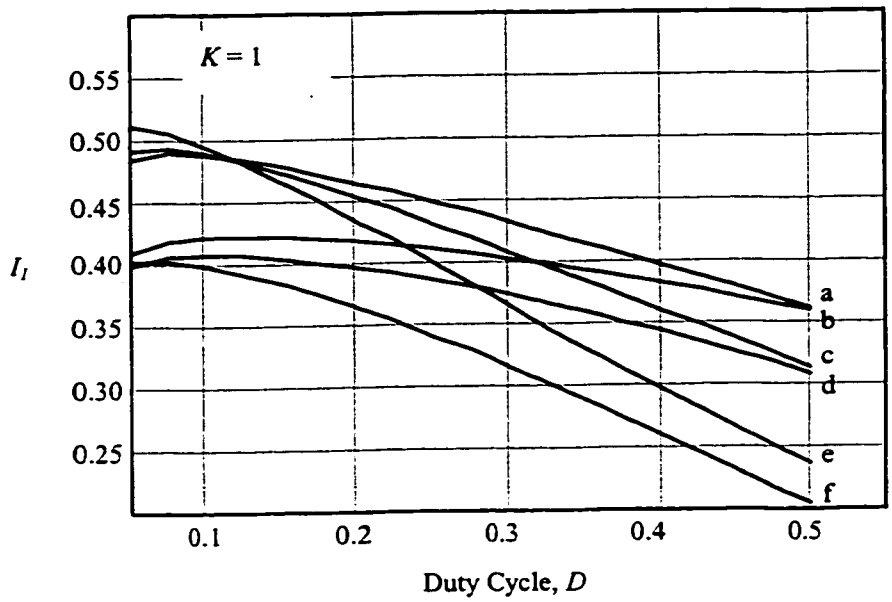


Fig.3.5 Current through S_1 at Turn-Off, I_1, as a Function of D for $K = 1$
a:Q=1.5, ω=1.5; b:Q=2.5, ω=1.5; c: Q=1.5, ω=1.3; d: Q=2.5, ω=1.3; e: Q=1.5, ω=1.1; f: Q=2.5, ω=1.1

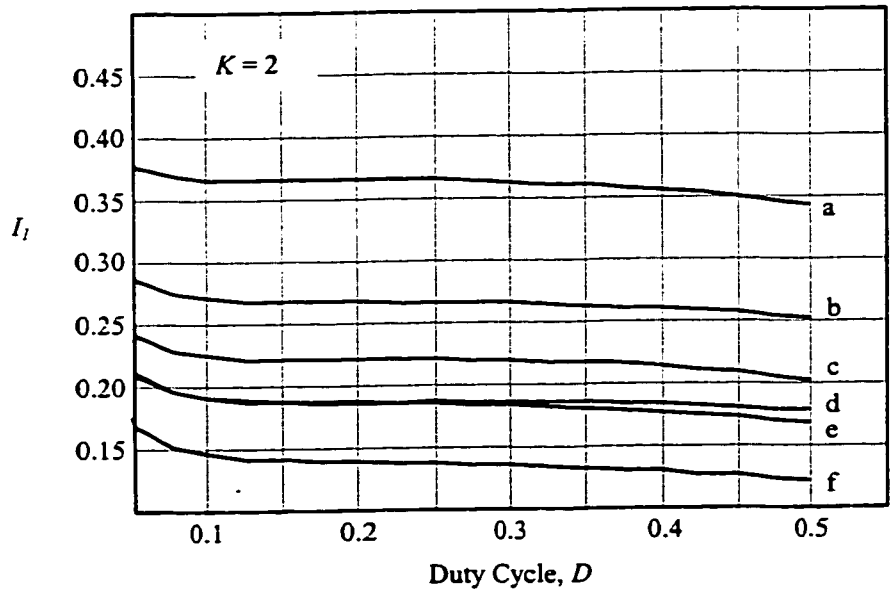


Fig.3.6 Current through S_1 at Turn-Off, I_1, as a Function of D for $K = 2$
a:Q=2.5, ω=1.5; b:Q=1.5, ω=1.5; c: Q=2.5, ω=1.3; d: Q=1.5, ω=1.3; e: Q=1.5, ω=1.1; f: Q=2.5, ω=1.1

3.3 DESIGN EXAMPLE

To better illustrate the process of determining component values, an example is presented.

3.3.1 Design Specifications

The specifications for this design are as follows:

1) full load output power, $P_o = 30\text{W}$;

2) output voltage, $V_o = 5\text{V}$;

3) switching frequency, $f_s = 500\text{kHz}$;

4) input voltage range, $V_{in} = 35\text{V} - 80\text{V}$;

5) duty cycle range, $D = 0.0 - 0.5$;

6) voltage ripple across capacitors C_{1a} and C_{2a}, $\Delta V_{in} = 0.05 V_{in}$;

7) output voltage ripple, $\Delta V_o = 0.05 V_o$;

8) deadtime between main power switches, $\Delta t = 100\text{ns}$.

3.3.2 Determination of K, Q, and ω

It is evident from Figs.3.1 to 3.6 that the values of Q and ω chosen affect the amount of current passing through the switches. The chosen parameters should ideally present a low amount of current, but, not at the expense of losing ZVS. Overall, the best results occur for Q=1.5 and ω=1.1. This shows that this circuit can operate at frequencies very close to the resonant frequency. The voltage across the resonant inductor v_{L_s} was given in Eq.(2-20). The curves for $v_{L_s}(t)$ are shown in Fig.3.7 [33] with Q=2.5 which was the optimum value of Q for the original topology [20] and Q=1.5. As seen from Fig.3.7, the auxiliary inductor voltage of the original circuit will have notably higher frequency harmonics and

thus higher core losses at Q=2.5 compared to the modified topology with Q=1.5. The significant reduction in core losses of the modified topology will make the resonant inductor much easier to manufacture. The best value for the auxiliary inductor is K=1. This means that the auxiliary inductor and the resonant inductor can have the same value and, therefore, lower production costs.

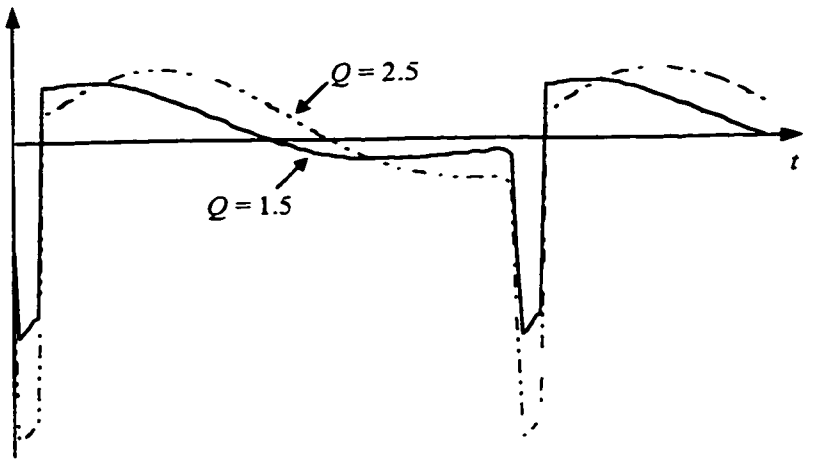


Fig.3.7 Voltage across Resonant Inductor for Q=2.5 (original circuit) and Q=1.5 (modified circuit)

3.3.3 Transformer Turns Ratio

Some curves are presented to demonstrate the determination of the transformer turns ratio n_{T_x}. Using Eq.(2-29), Fig.3.8 plots the input voltage as a function of duty cycle, D. The optimum values for Q and ω described in section 3.3.2 are used. There are four curves, each one representing a different n_{T_x} value. In examining the curve for n_{T_x} = 4, it is apparent that having an input voltage of less than 40V will not give an output of 5V. The curve for n_{T_x} = 1 shows a steep curve. The range of D is very narrow (about 0.05 at 80V and 0.1 at 35V) so that the value of D must be very precise. There is not much room for

error. The curves for $n_{T_x} = 2$ and $n_{T_x} = 3$ show better results. For the specifications given earlier, the value for the transformer turns ratio n_{T_x} should be: $2 \leq n_{T_x} \leq 3$.

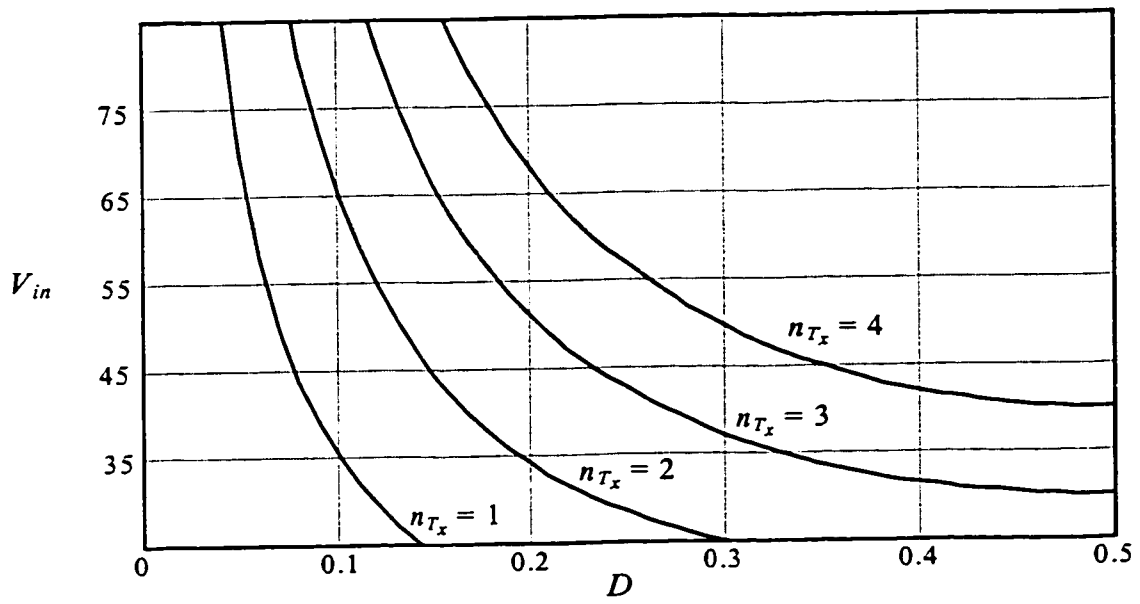


Fig.3.8 Input Voltage as a Function of Duty Cycle for Different Values of Transformer Turns Ratio, n_{T_x} for a Constant Output Voltage of 5V

3.3.4 Auxiliary Inductor and Resonant Components

The optimum values for K, Q and ω given in section 3.3.2 will be used to solve for the auxiliary inductor and the resonant components. To begin with, the equivalent resistance has to be calculated. Based on the results of the last section, a suitable value for the transformer turns ratio n_{T_x} is 2.5. Substitution of this value in Eq.(2-8), R_{eq} becomes 4.22Ω. To solve for the resonant inductor, Eq.(2-13) and Eq.(2-14) give $L_s \approx 2.2\mu H$. Since K=1, L_a has the same value as L_s. Using Eq.(2-12) to determine the value of C_s results in $C_s \approx 56nF$.

3.3.5 Capacitors C_{1a} and C_{2a}

The equations that will be developed here are based on the auxiliary inductor current of Fig.2.2. The total charge developed across C_{1a} and C_{2a} in one cycle is given by:

$$\Delta Q_{chg1} = \left(\frac{DT_s}{2} + \frac{(1-D)T_s}{2} \right) \cdot I_a = \frac{T_s}{2} \cdot I_a \tag{3-5}$$

where I_a is the peak of the auxiliary inductor current and was given in Eq.(2-23). Since this charge is transferred to two capacitors of the same value, the following can be stated:

$$2C_{1a} \cdot \Delta V_{in} \geq \frac{T_s}{2} \cdot \frac{D(1-D) \cdot V_{in}}{2 f_s L_a} \tag{3-6}$$

where ΔV_{in} is the voltage ripple across capacitors C_{1a} and C_{2a}. With the specification for this voltage ripple given in section 3.3.1, the value of C_{1a} becomes :

$$C_{1a} \geq \frac{D(1-D)}{0.4 f_s^2 L_a} \tag{3-7}$$

To find the minimum value of C_{1a} that can be used in the circuit, the maximum value of D should be used in Eq.(3-7). Using $D = 0.5$ gives C_{1a}, $C_{2a} \geq 1.1\mu F$.

3.3.6 Capacitors C_1 and C_2

So far in the analysis, it has been assumed that the deadtime between the switches was zero. Since the capacitors charge and discharge during the deadtime, this time becomes non-trivial. It must be assumed that no current flows through the switches during the deadtime. An approximation of the charge stored in C_1 and C_2 is given by:

$$\Delta Q_{chg\,2} \approx \frac{\Delta t}{2} \cdot \left(I_a' + I_{s1}' \right) \tag{3-8}$$

where I_a' represents the peak of the auxiliary current when the deadtime is taken into account. Eqs.(2-22) and (2-23) make the assumption of no deadtime. I_a' is defined as:

$$I_a' = \frac{DD'}{D + D'} \cdot \frac{V_{in}}{2 f_s L_a} \tag{3-9}$$

where D' is the amount of time S_2 is on. It is defined as:

$$D' = 1 - D - \frac{\Delta t}{T_s} \tag{3-10}$$

I_{s1}' is the peak of the fundamental component of the resonant current including deadtime. Modifying Eq.(2-18), I_{s1}' is defined as:

$$I_{s1}' = \frac{\sqrt{2} V_{in} R_{eq}}{\pi |Z_{in}|} \cdot \sqrt{1 - \cos 2\pi D'} \tag{3-11}$$

Since this charge is transferred to two capacitors of the same value, the following can be stated:

$$2C_1 \cdot \Delta V_{in} \geq \frac{\Delta t \cdot V_{in}}{2} \cdot \left(\frac{DD'}{2 f_s L_a (D + D')} + \frac{\sqrt{2} R_{eq} \cdot \sqrt{1 - \cos 2\pi D}}{\pi |Z_{in}|} \right) \tag{3-12}$$

L_a was found to be 2.2μH and $|Z_{in}|$ can be found by using Eq.(2-30) and the values for Q, ω and R_{eq}, which were determined earlier. Using the maximum value of D ($D = 0.5$) will give the minimum values of C_1 and C_2. This results in $C_1, C_2 \geq 37$nF.

3.3.7 Main Power MOSFETs, S_1 and S_2

As seen in Fig.2.2, when each switch is off, it must withstand the input voltage. This means that the drain-source breakdown voltage rating of each switch, $V_{DS\_S1,\ S2}$ must be:

$$V_{DS\_S_1,S_2} \geq V_{in,max} \tag{3-13}$$

Since the switch current is the sum of the resonant and the auxiliary currents, the maximum current that can flow through each switch is given by $I_{D\_S1,\ S2}$:

$$I_{D\_S_1,S_2} = I_{S_1} + I_a \tag{3-14}$$

where I_{S1} and I_a were given in Eqs.(2-18) and (2-23) respectively. For the specifications outlined earlier, $V_{DS\_\ S1,\ S2}$ must be greater than 80V and $I_{D\_S1,\ S2}$ is equal to 21A. Along with the voltage and current ratings, MOSFETs which have a low on-state resistance should be chosen.

3.3.8 Output Capacitor

To determine the value of C_o, the current through this capacitor must first be determined. Assuming that only the fundamental component is taken into account, this current is a half-wave rectified sinusoid proportional to the resonant current. The stored charge in one half cycle is given by:

$$C_o \Delta V \geq = \int_0^{T_s/2} I_{s1} \sin\left(\omega_o t + \theta_n - \phi_n\right) dt \tag{3-15}$$

The definitions of θ_n and ϕ_n were given in Eq.(2-11) and Eq.(2-17) and are solved for D = 0.5. The definition of I_{s1} is given in Eq.(2-18) is in terms of V_{in}. To put it in terms of V_o,

the voltage conversion ratio can be used. This was given in Eq.(2-29). With the design specifications given earlier, $C_o \geq 15.6\mu F$.

3.3.9 Output Rectifier

The object of the output rectifier, is to convert bipolar current and voltage into unipolar waveforms. The goal of the designer is to achieve this with as little power dissipation as possible. When selecting a diode, the voltage and current ratings must be taken into account. For the rectifier diode, the peak forward current and the peak reverse voltage are given as:

$$I_{D,pk} = nI_{R1} = \frac{\pi I_o}{2} \tag{3-16}$$

$$V_{D,pk} = 2V_o \tag{3-17}$$

In examining the families of rectifier diodes, it is generally the Schottky diodes which show the smallest voltage drops.

3.4 CONCLUSIONS

This chapter has used the equations that were developed in Chapter 2 and then performance curves were derived to determine the optimum values for the major components of the converter. A design example was presented, outlining the specifications and the development of equations to determine the major component values. It was realized that with the addition of the auxiliary network, the converter can be designed for a low value of Q which reduces the resonant tank impedance. Also, both the resonant and auxiliary inductors can be designed to have the same value.

Chapter 4

Use of Synchronous Rectification

4.1 INTRODUCTION

It was demonstrated in the last chapter that the power losses of the diode rectifier are quite considerable. The use of the Schottky diode alleviates the problem to a degree, but the rectifier is still the greatest source of power losses in the converter. When used in a proper configuration, MOSFETs can be used as a diode without the diode's constant voltage drop. With the advanced technology in MOSFET design, the on-resistance is very low, thus the power losses are also very low. Since the MOSFET now acts as a diode and not as a switch, the roles of the source and drain become reversed. Fig.4.1 shows the synchronous rectifier, where the resonant current is modeled as a current source on the primary side. When the power MOSFET is used for synchronous rectification, it is configured so that the current normally flows through the channel from source to drain (in the direction of the body diode). The forward blocking direction of the MOSFETs is the reverse blocking direction of their body-drain diodes, so that the MOSFET is maintained in the OFF state while the diode is reverse biased. When the body-drain diode is forward biased, the MOSFET is turned on. To guarantee that the two MOSFETs do not turn on simultaneously and create a transformer short circuit, a deadtime is usually introduced between the two gate signals.

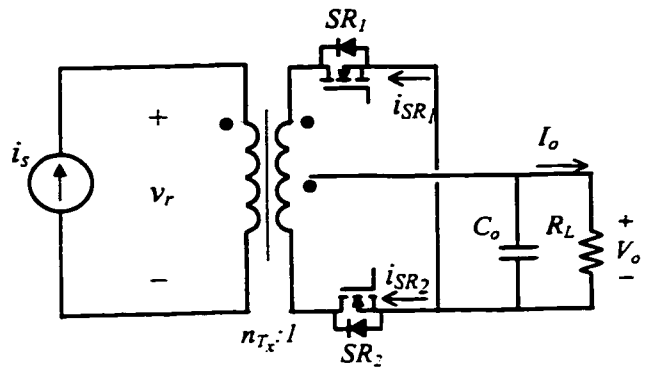


Fig.4.1 MOSFET used as Synchronous Rectifier

The synchronous rectifier topologies can either be self-driven or externally driven, where separate driver integrated circuits (IC) are required.

Section 4.2 will present a theoretical analysis of synchronous rectification, including power loss analysis. It is similar to the analysis of diode rectifiers presented in Chapter 2. Section 4.3 discusses the selection of synchronous rectifier topologies for the modified asymmetrical pulse-width modulated series resonant DC/DC converter. A couple of examples of synchronous rectifiers that can be applied to series-resonant converters will be presented in Sections 4.4 and 4.5 including simulation results. Section 4.6 will examine the advantages and disadvantages associated with each one. Section 4.7 completes the chapter with some conclusions.

4.2 BASIC ANALYSIS

Some basic analysis will be presented with the assumption of no dead time. It will also be assumed that when the MOSFET is on, it can be modeled by an equivalent on-resistance r_{DS_SR} and as an open circuit when it is off. This is shown in Fig.4.2a when SR_1 is off and SR_2 is on and in Fig4.2b when SR_1 is on and SR_2 is off [34].

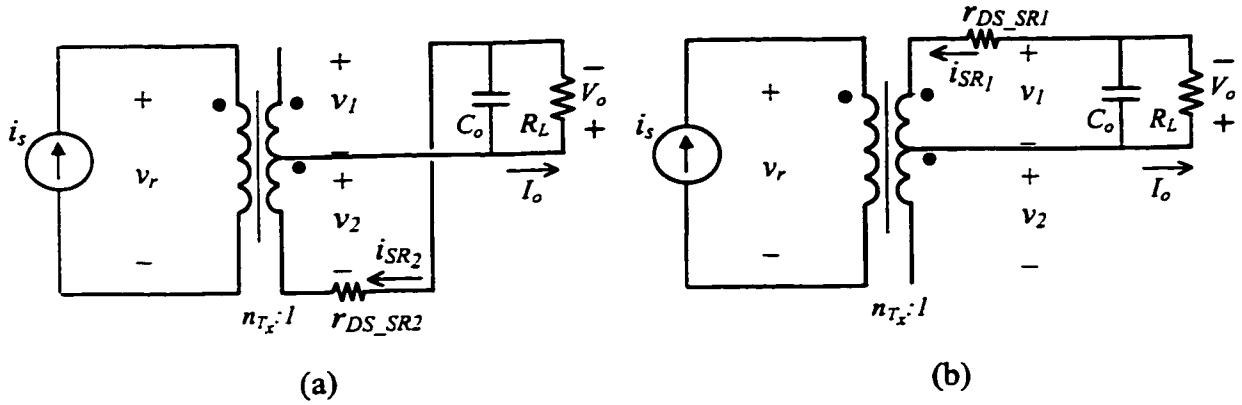


Fig.4.2 Equivalent Models of Synchronous Rectifiers: a)SR_2 is on, b)SR_1 is on

For the first half of the cycle, $0 < \omega_s t < \pi$, the resonant current is positive and SR_2 is switched on. The voltages across the secondary sides of the transformer are:

$$v_1 = v_2 = V_o \tag{4-1}$$

and the voltage across SR_1 is:

$$v_{SR_1} = -v_1 - v_2 = -2V_o \tag{4-2}$$

The current through SR_2 is:

$$i_{SR_2} = n_{T_x} i_s(t) \tag{4-3}$$

where n_{T_x} is the turns ratio of the transformer. For the second half of the cycle, $\pi < \omega_s t < 2\pi$, the resonant current is negative and SR_1 is switched on. The voltages across the secondary sides of the transformer are:

$$v_1 = v_2 = -V_o \tag{4-4}$$

and the voltage across SR_2 is:

$$v_{SR_2} = v_1 + v_2 = -2V_o \tag{4-5}$$

The current through SR_1 is the same as given in Eq.(4-3). From Eq.(2-7), the peak forward current of each rectifier MOSFET is:

$$I_{SR} = n_{T_x} I_{S_1} = \frac{\pi I_o}{2} \tag{4-6}$$

and the peak reverse voltage of each rectifier MOSFET is:

$$V_{SR} = 2V_o \tag{4-7}$$

Using the transformer turns ratio, n_{T_x} and (2-4), the amplitude of the fundamental component of the transformer input voltage is:

$$V_{R1} = \frac{4n_{T_x} V_o}{\pi} \tag{4-8}$$

and its RMS value is:

$$V_{R1rms} = \frac{V_{R1}}{\sqrt{2}} = \frac{2\sqrt{2}n_{T_x} V_o}{\pi} \tag{4-9}$$

Since the rectifier input current is approximately sinusoidal, the power to the input of the synchronous rectifier contains only the fundamental component. The input power can be expressed as:

$$P_{R_{eq}} = \frac{{I_{S_1}}^2 R_{eq}}{2} = \frac{\pi^2 {I_o}^2 R_{eq}}{8{n_{T_x}}^2} \tag{4-10}$$

The RMS value of the current through each rectifier MOSFET is:

$$I_{SRrms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{SR_1}^2 \, d(\omega t)} = \frac{n_{T_x} I_{S_1}}{2} = \frac{\pi I_o}{4} \tag{4-11}$$

From this result, the power loss in the forward resistance r_{DS_SR} of each synchronous rectifier MOSFET is:

$$P_{r_{DS\_SR}} = r_{DS\_SR} I_{SRrms}^2 = \frac{\pi^2 I_o^2 r_{DS\_SR}}{16} = \frac{\pi^2 r_{DS\_SR}}{16 R_L} P_o \tag{4-12}$$

where P_o is the DC output power. The total power loss of the synchronous rectifier is:

$$P_{SR} = 2 P_{r_{DS\_SR}} = \frac{\pi^2 r_{DS\_SR}}{8 R_L} P_o \tag{4-13}$$

The power loss that has been presented here is the conduction loss. The MOSFETs are turned on and off at the zero crossings of the resonant current so the switching losses compared to the conduction losses are quite negligible.

Taking the power loss in the transformer into consideration, the input power to the rectifier circuit is:

$$P_{R_{eq}} = \frac{P_o + P_{SR}}{\eta_{Tx}} \tag{4-14}$$

where η_{Tx} is the efficiency of the transformer. The efficiency of the synchronous rectifier then becomes:

$$\eta_{SR} = \frac{P_o}{P_{R_{eq}}} = \frac{\eta_{Tx} P_o}{P_o + P_{SR}} = \frac{8 R_L \eta_{Tx}}{8 R_L + \pi^2 r_{DS\_SR}} \tag{4-15}$$

4.3 SELECTION OF SYNCHRONOUS RECTIFIER TOPOLOGIES

The selection of a suitable synchronous rectifier topology depends on the topology of the converter. A popular choice for self-driven synchronous rectification is shown in Fig.1.7(a) and shown again in Fig.4.3. The secondaries of the main transformer are used to drive the synchronous rectifiers. This method, however, is only suitable for voltage-fed, inductor-loaded topologies. In this case, the voltage across the primary of the main transformer is fixed and not dependent on the output stage and can therefore be used as a gating signal for the synchronous rectifiers. The APWM series resonant DC/DC converter is a current-fed, capacitor-loaded topology. In this case, the MOSFET gating signals cannot be derived from the primary of the main transformer because these voltages also depend on the state of the rectifier itself. Initially, when SR_1 is on, a positive voltage is seen across both the primary and secondary of the main transformer. The voltage across the transformer will only change when SR_1 is turned off and SR_2 is turned on. However, this will never happen if the gating signals of the synchronous rectifiers depend on the polarity of the transformer.

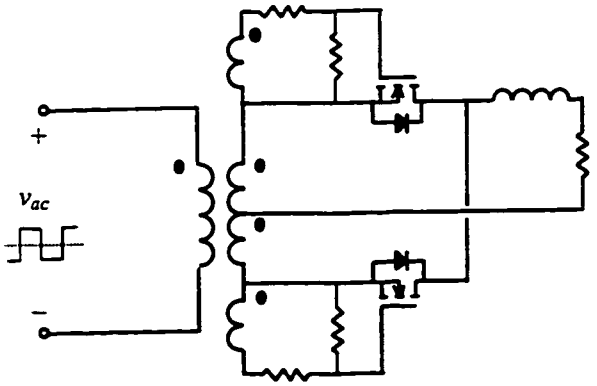


Fig.4.3 Voltage-Fed Topology with Synchronous Rectfication

Another problem with this circuit is that there will always be an overlap between the conduction of SR_1 and SR_2 due to the finite turn-on and turn-off times which will lead to a short-circuit condition during this overlap period. For current-fed topologies then, using the secondary voltages as gating signals for the synchronous rectifiers is not preferable. Instead, these topologies must rely on the current through the transformer, which is fixed, to derive the gating signals. Also, there must be a deadtime between the two MOSFET gating signals in order to prevent the simultaneous turn-on of both switches. In examining the output rectifier waveforms of Fig.2.10, the MOSFETs switch when the resonant current crosses zero. A topology is needed that can sense this approaching current transition and switch the MOSFET on or off before the resonant current actually crosses zero, thus creating a deadtime between the switches. Therefore, the synchronous rectifier topologies that can work with current-fed configurations are those that involve sensing the resonant current (or the secondary currents of the main transformer) and switching the MOSFET as the current approaches zero.

If the synchronous rectifiers are externally driven, then the main issue is that of timing. Care must be given to ensure that both switches are not turned on at the same time. The turn-on and turn-off of the switches must be carefully monitored to prevent switching errors.

4.4 CURRENT-SENSE TRANSFORMER TOPOLOGY

4.4.1 Circuit Description and Principle of Operation

The first one is depicted in Fig. 4.4 [27]. It consists of two synchronous rectifier MOSFETs (SR_1, SR_2), two current-sense transformers (T_{sense1}, T_{sense2}), four bipolar junction transistors (Q_1 to Q_4), two diodes (D_1, D_2) and two capacitors ($C_{V_{cc}}$, C_o). The resonant current is represented as a constant sinusoidal current source, i_{pri}. The secondary currents of T_x are represented by i_{sec1} and i_{sec2}. Each sense transformer, T_{sense1} and T_{sense1}, has a transformer turns ratio of *1:N:N*. Diodes D_1 and D_2 along with capacitor $C_{V_{cc}}$ develop a bootstrap voltage V_{cc} from the secondary of the main transformer T_x for the collector supply of the totem-pole bipolar junction transistors (BJTs). With reference to the polarities of the secondaries of the main transformer, when I_{pri} is negative, D_1 becomes forward-biased and D_2 becomes reverse-biased. Sensing the incipient conduction of the body-drain diode, T_{sense1}, turns on Q_1, which in turn pulls up the output voltage of the totem-pole to V_{cc}. The emitter of Q_1 will then provide fast charging of the gate capacitance of SR_1. Fig. 4.5 shows the equivalent circuit of T_{sense1}, including the magnetizing inductance, L_{m1}. The leakage inductance is neglected.

As i_{sec1} flows, the magnetizing current i_{m1} builds up until it surpasses i_{sec1}, thus forcing the reversal of the primary current of the sense transformer i_{sensep}. The definition of i_{sensep} is:

$$i_{sensep} = i_{sec1} - i_{m1} \tag{4-16}$$

When this occurs, Q_1 is turned off and Q_2 is turned on. Transistor Q_2 will then provide the fast discharging of gate capacitance of SR_1 and provide a low resistance to ground. SR_1 is

turned off and i_{sec1} goes to zero. The magnetizing current i_m starts to decrease as well. The waveforms for this circuit are shown in Fig.4.6. There is a dead time between drive pulses, which is inherent in the circuit design. Ideally, each BJT totem-pole inverter switches (as explained above) when rectifier current equals its associated sense transformer magnetizing current.

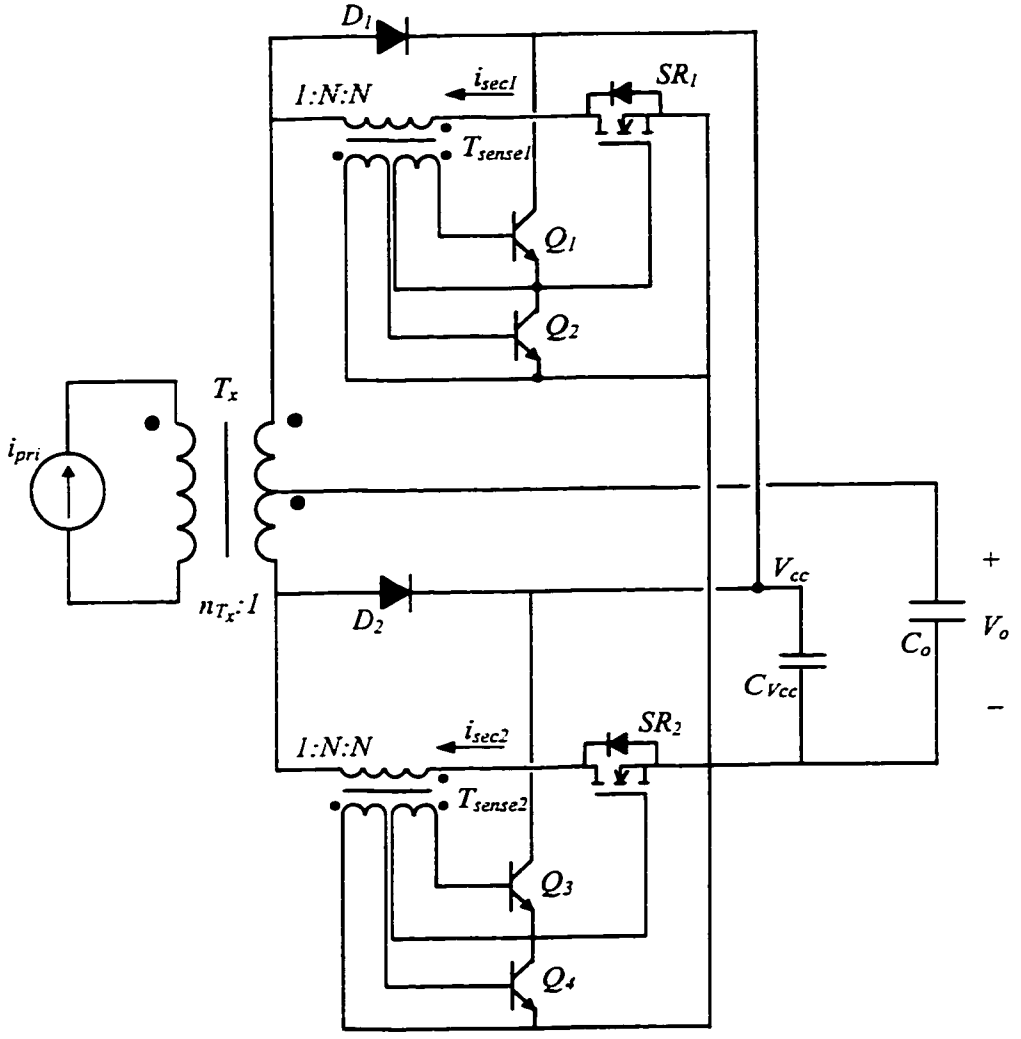


Fig. 4.4 Current-Sensing Transformer Approach

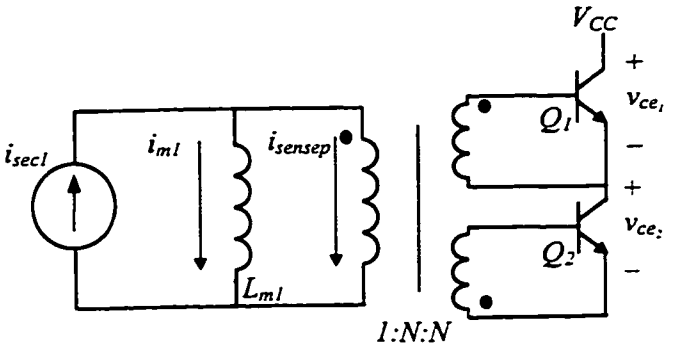


Fig. 4.5 Equivalent Circuit Seen by the Sense Transformer, T_{sense1}

This is seen in Fig.4.7. To insure against premature gate-drive transitions, the magnetizing current i_m must be in continuous mode. To determine the minimum value for L_m, the boundary between the continuous and discontinuous modes is examined. At this boundary, i_m goes to zero at the end of the switching period, T_s. The maximum DC current that can flow through each main transformer secondary is $I_o/2$. The voltage across the magnetizing inductance is given by V_{be}/N (assuming that $V_{be} = V_{be1} = V_{be2}$). With this in mind, the minimum value for the magnetizing inductor is given by:

$$L_{m,\min} = \frac{V_{be}}{N} \cdot \frac{1}{I_o/2} \cdot \frac{T_s}{4} \tag{4-17}$$

or,

$$L_m > \frac{V_{be} T_s}{2 N I_o} \tag{4-18}$$

where T_s is the switching period.

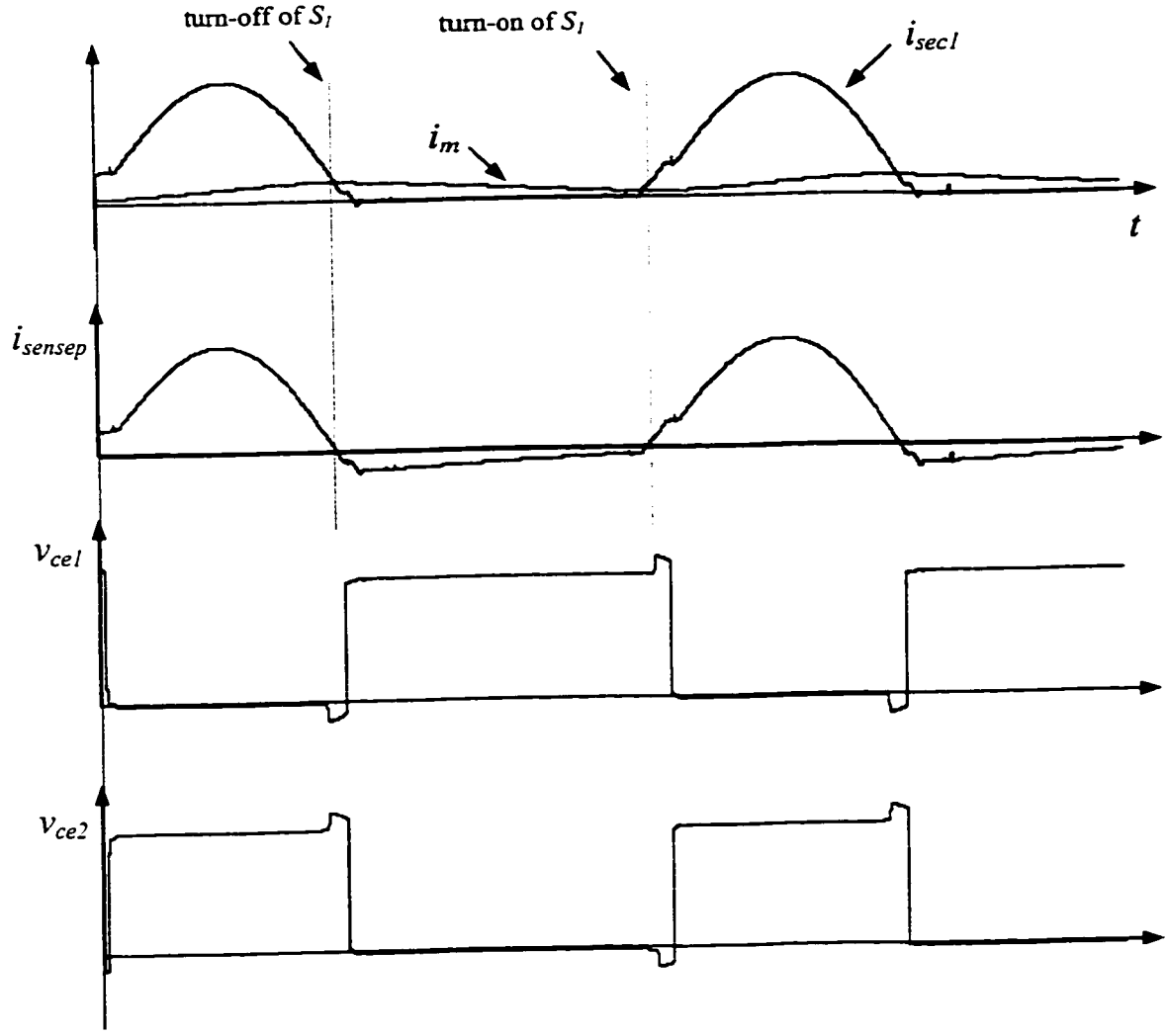


Fig.4.6 Key Waveforms of the Equivalent Circuit Seen by the Sense Transformer, T_{sense1}

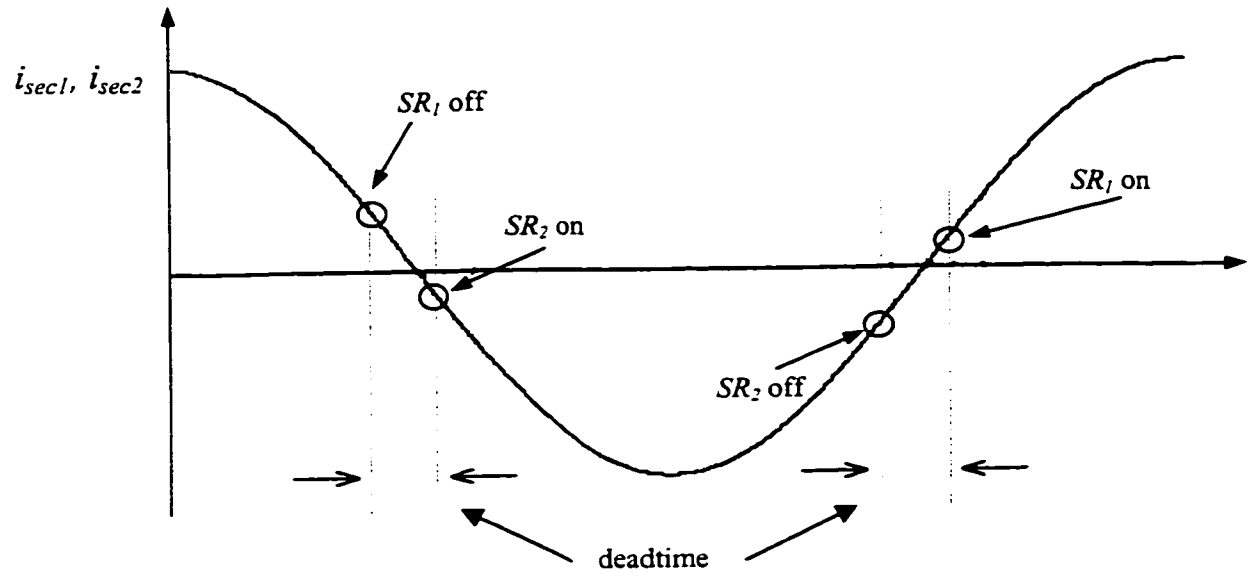


Fig.4.7 Unrectified Secondary Current of Main Transformer Showing Deadtime Intervals

4.4.2 Simulation Results

Computer simulations were performed using the circuit shown in Fig.4.4. The test was based on the series resonant topology, therefore, the primary side current is represented as sinusoidal current source as shown in Fig.4.4. The circuit is designed for operation at 100kHz with a 30W power output and 5V output DC voltage. The turns ratio for the main transformer is 2.5:1 as determined in the previous chapter and the sense transformer turns ratio are both set at 1:1. Assuming a base-emitter voltage drop of 0.7V, the minimum value of the magnetizing inductor was found to be 0.6μH. For the current simulation, a value of 7μH for was used.

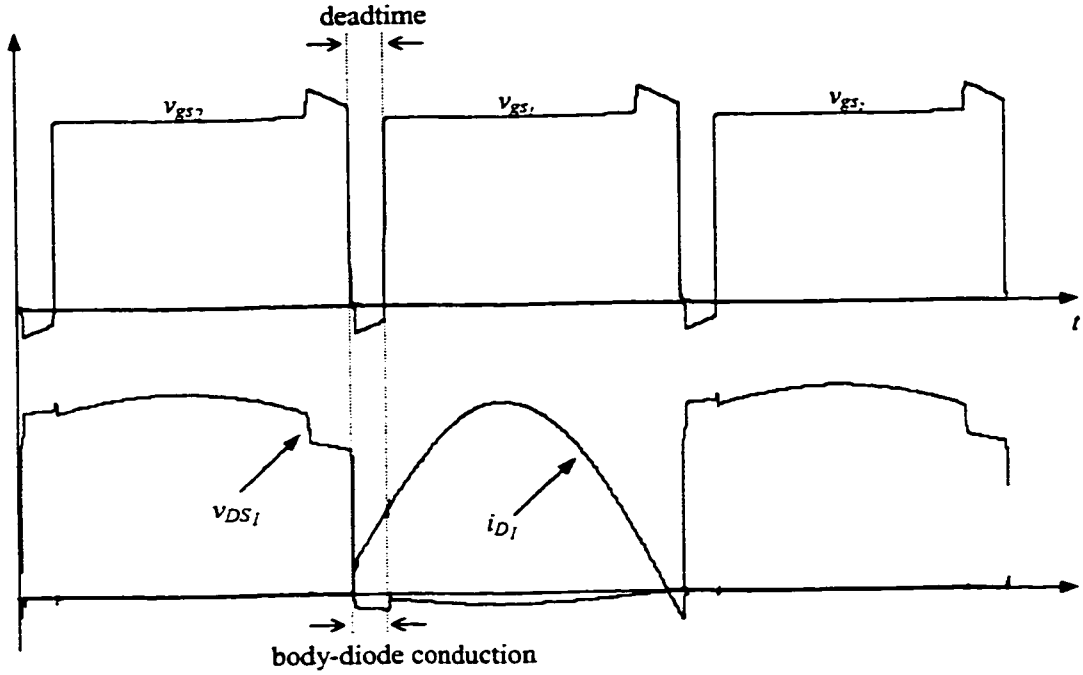


Fig.4.8 Simulation Results for Current-Sense Transformer Topology: upper set of curves show gating signals and bottom set show current and voltage across the switch

At this frequency, the simulation shows favourable results. The deadtime between the two gating pulses ensures that there is no overlap and no chance that both switches will turn-on simultaneously. Just before the switch is turned on, current flow is through the body diode of the MOSFET, thus guaranteeing zero voltage switching at turn-on. With ZVS at turn-on, the switching losses are almost negligible and so the only power losses present originate from the conduction losses. Advancements in MOSFET technology have made the production of MOSFETs with on-resistances in the miliohms possible so that even the conduction losses are almost negligible as well.

4.5 ADAPTIVE TIMING CONTROL

4.5.1 Principle of operation

With this type of control, discrete ICs are used to drive the gate signal to achieve precise timing. The goal here is to represent the function of an ideal diode. When the drain-source voltage goes to zero, the MOSFET will turn on and when the drain current goes to zero, the MOSFET will turn off. The drain current can be monitored by examining the voltage-drop across the MOSFET that is due to the on-state resistance. An important issue that is often raised when justifying the use of synchronous rectifiers in place of diode rectifiers is the timing. This is especially crucial as the operating frequencies are increased. The turn-on and turn-off of the switch has to be exactly on time, otherwise the inherent body diode will begin conducting, in turn creating conduction losses. In most cases, this could pose a problem since the external gate drive circuit will naturally have propagation delays. With the adaptive timing control system, the delays are effectively cancelled out. This system has two separate feedback loops. One determines the timing for the MOSFET turn-on and the other for the turn-off. Fig.4.9 shows the block diagram of the turn-on loop [32]. It consists of two comparators, an edge comparator, two MOSFETs, a charge pump, an integrating capacitor, a one-shot timer, a latch and a gate driver. Ideally, the MOSFET should be switched on as soon as the drain-source voltage is zero. Propagation delays through the control circuit prevent this from happening. In this scheme, as soon as the comparator senses that the drain-source voltage has crossed zero, it initiates the gate turn-on for the following cycle of operation. An error signal is developed during each cycle and used in an adaptation loop to asymptotically eliminate timing error

in periodic steady-state operation. Fig.4.9 shows two comparators. The first is the turn-on comparator and detects when the drain-source voltage of the synchronous rectifier v_{ds_SR} crosses zero. The second one is a gate threshold comparator that is used to indicate when the MOSFET is fully enhanced by comparing the gate-source voltage of the synchronous rectifier v_{gs_SR} to the nominal gate threshold voltage. As soon as v_{ds_SR} crosses zero, the turn-on comparator detects this event and after a time $\tau_{v_{ds}}$, corresponding to the comparator propagation delay, the output of the comparator goes high, triggering the one-shot timer. At the end of the programmed timing interval τ_{timer}, the timer output sets the latch. The voltage stored on the integrating capacitor determines the timing interval. The gate drive buffer circuitry then starts charging up the gate input capacitance of the synchronous rectifier MOSFET. After a delay. τ_{driver}, which corresponds to the delay of the gate driver, v_{gs_SR} will reach its threshold value and the MOSFET will turn on. The gate-threshold comparator monitors this event and produces a positive-going edge after interval $\tau_{v_{gs}}$, corresponding to the delay through the comparator. For ideal steady-state operation, the MOSFET must be turned on as soon as its drain-source voltage crosses zero. This can be achieved by adjusting τ_{timer} according to:

$$T_s = \tau_{v_{ds}} + \tau_{timer} + \tau_{driver} \tag{4-19}$$

The delays through the logic circuitry are effectively compensated by the adjustment of τ_{timer}.

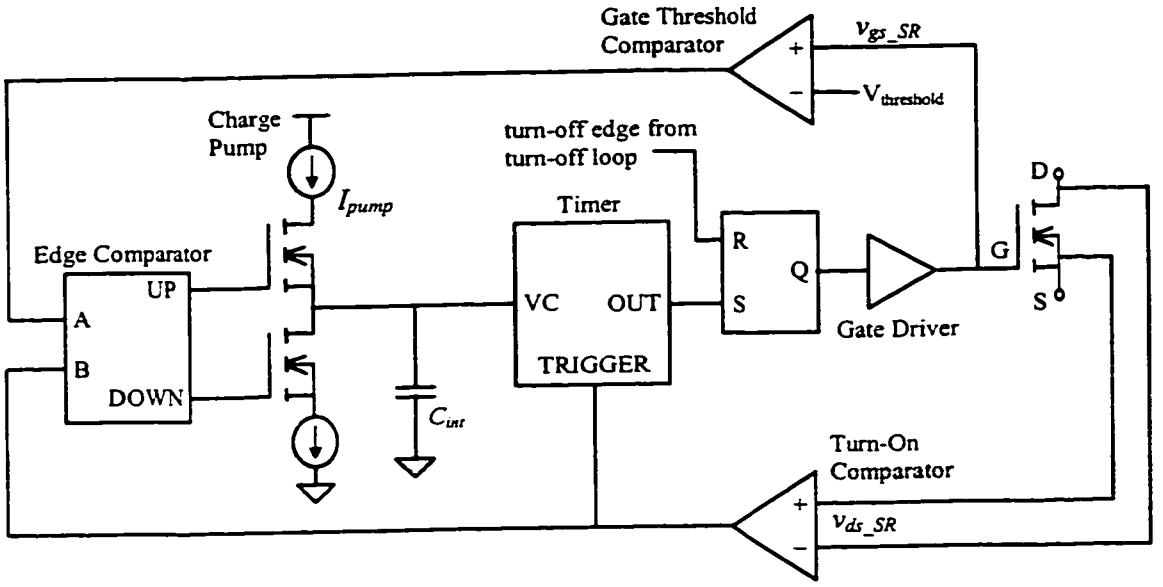


Fig. 4.9 Turn-On Loop Circuitry for Synchronous Rectification with Adaptive Timing Control

The operation outlined above is heavily dependent on the timing interval of the one-shot timer. If the timer output is too early or too late the MOSFET turn-on will be directly affected. The adaptive control system takes care of this problem with the addition of the edge comparator. When the synchronous rectifier MOSFET is switched on too early, the gate-threshold comparator output edge will lead the turn-on comparator edge. In reference to Fig.4.9, when B leads A, the DOWN output is active for the duration of the time lag between them. The bottom MOSFET of the charge pump turns on and acts like a sink for the integrating capacitor, therefore reducing its charge. The timing interval of the one-shot timer, τ_{timer} is controlled by the charge stored on the integrating capacitor. The charge on the capacitor is inversely proportional to the length of the timing interval so that as the charge on the capacitor is reduced, the timing interval is increased so that the MOSFET won't be turned on too early at the next cycle. For the case of late turn-on, the situation is

slightly different. If the drain-source voltage has crossed zero, but the timer hasn't completed its timing interval, the circuit will not wait for the timing operation to be completed. Instead, that timing interval is aborted and the latch is automatically set. The timer is retriggered to begin a new timing cycle. In this situation, the turn-on comparator edge will lead the gate threshold comparator edge, therefore activating the UP output. The upper MOSFET of the charge pump turns on, thus allowing I_{PUMP} to charge up the integrating capacitor. This increased rate of rise of voltage on the capacitor has the effect of reducing the timing interval of the timer for the next cycle of operation.

Another independent adaptation loop effects the turn-off timing of the synchronous rectifier by resetting the output latch at the appropriate time. This loop has an edge detector, charge pump, integrating capacitor and timer similar to those of the turn-on loop. The turn-off comparator, however, needs to detect the zero-crossing of the current through the synchronous rectifier. It does this by monitoring the small voltage drop developed across the synchronous rectifier's on-state resistance.

This synchronous rectifier can be integrated into a single package. Having the two power MOSFETs each with its own independent control and drive circuitry on a single chip using a CMOS process results in low power dissipation. Other advantages include the use of a gate drive level of 3.3 volts or less, which significantly reduces gate drive losses. This is due to the low gate threshold of the device. The control over source inductance is also much better compared to using discrete MOSFETs with separate control/driver circuitry.

4.5.2 Simulation Results

The simulation results using this method are shown in Fig.4.10. The frequency of operation is 500kHz. Before the switch is gated on, the current flows through the body-diode, and ZVS is achieved when the switch turns on. The deadtime between the gating signals can be realized through the propagation delays of the ICs and can therefore be controlled.

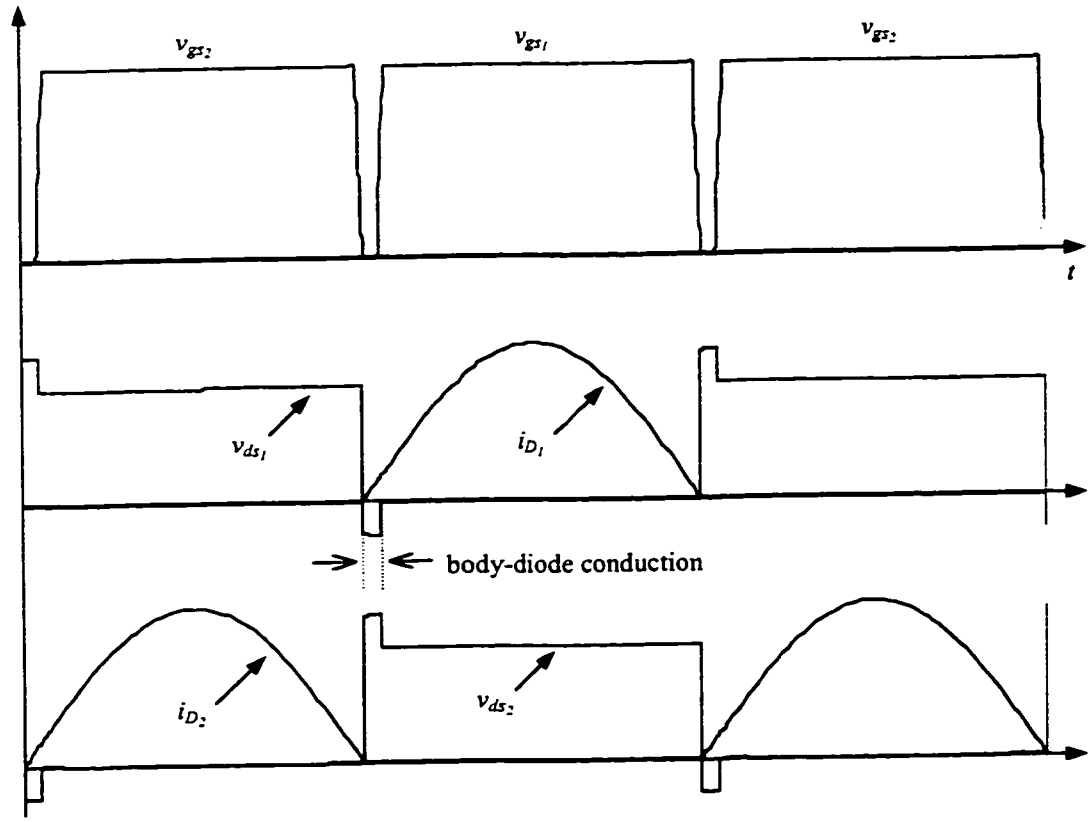


Fig.4.10 Simulation Results of Adaptive Control Method: top waveforms show gating signals; middle waveforms show current and voltage through top switch and bottom waveforms show current and voltage through bottom switch

4.5 COMPARISON OF SYNCHRONOUS RECTIFIER TOPOLOGIES

The operating principles of the synchronous rectifier topologies have been examined, yet the study wouldn't be complete without a comparison of their advantages and disadvantages:

Current-Sensing Transformer

Advantages:
- simple design requiring few components
- no external control or driver circuitry required

Disadvantages:
- transformer losses increase as frequencies increase
- leakage inductance from current-sensing transformer in series with MOSFET may cause problems with current commutation

Adaptive Timing Control

Advantages:
- synchronous rectifier including power MOSFET and gate/driver circuitry can be packaged together on a single chip, thus reducing losses otherwise caused by discrete components
- adaptive control scheme solves problems associated with timing delays
- suitable for high frequency operation
- very good accuracy

Disadvantages:
- packaging of synchronous rectifier on a single chip is costly
- more complex design and more components required
- additional voltage source necessary to power up logic gates

- under light load conditions, the small voltage drop across synchronous rectifier may be only a few tens of millivolts which may make its detection difficult

With the advancement of micro-technology, some of the aforementioned disadvantages may not be so problematic in the future. Microfabrication of transformers and inductors for high frequency operation is now possible and losses normally associated with transformers at high frequencies wouldn't be such a concern. This technology involves the use of thin-film metal alloys in place of ferrites as the material of choice. VLSI technology is becoming more and more widespread, resulting in lower costs for the production of ICs.

4.6 CONCLUSIONS

The use of synchronous rectification in the output stage has been presented here. This goal is to replace diode rectifiers and thus reduce power losses. Since a MOSFET can be represented as a resistance in its on state, and, unlike a diode, it doesn't have a fixed voltage drop across it.

Two possible SR topologies were presented. The current transformer method senses the drain current through a sense transformer which in turn controls a pair of BJTs. This pair acts as a switch producing a pulse waveform that is fed to the gate of the MOSFET turning it on and off. Since this topology is essentially controlled by the state of the converter itself, this topology is said to be self-driven. Its simplicity in design with no external driving circuit necessary makes it a good topology. The effect of leakage inductances at high frequencies, might cause problems, however.

The second method uses external circuitry to develop gate signals for the *next* switching period. This ensures that the propagation delay times through the logic gates do not cause unnecessary delays in the gating signals. Separate turn-on and turn-off loops sense the drain-source voltage of the synchronous rectifier and use it to control the timing of the gating waveform. It also corrects for timing errors associated with its one-shot timer. The design is more complex and more components are required which lead to increased cost.

Chapter 5

Conclusion

5.1 SUMMARY

In the telecommunication and computer industry, power supply topologies that offer high power density and low power loss while operating at high frequencies are essential. Resonant-mode topologies satisfy these requirements. With many of them, however, their output voltage is controlled by varying the switching frequency. This becomes a problem when constant frequency operation is required. The topologies that do offer constant frequency operation often suffer from complex circuitry and a high component count. The development of the Asymmetrical Pulse-Width Modulated Series Resonant DC/DC Converter offers a simple topology with near-zero voltage switching losses, even with operation at high switching frequencies. The range of input voltage where high efficiency is maintained is narrow, however. Above this range, ZVS is sacrificed and the efficiency drops. Also, the voltage stress across the resonant inductor increases as the input voltage is increased. It is in overcoming these limitations that have lead to the development of an auxiliary network.

In Chapter 2, the modified topology has been presented and analyzed. The operating principle was presented by dividing the operation of one switching cycle into four intervals and looking at each interval separately. Steady-state analysis was presented by examining one functional block at a time. For further verification, computer simulations were done and an experimental prototype was built. A comparison between

the original topology and the modified one was presented and it is seen that the auxiliary network compensates for the shortage of current in the resonant tank and thus results in ZVS at higher input voltages.

In Chapter 3, the design of the major components was presented. The design was based on theoretical equations and design curves. From these, optimal values were chosen.

In Chapter 4, synchronous rectification, an alternative to diode rectifiers was presented. Two types of synchronous rectifier topologies that are applicable to the modified topology under study were presented and analyzed including the current-sense transformer topology and the adaptive control scheme. These topologies were then tested using computer simulation.

5.2 CONCLUSIONS AND CONTRIBUTIONS

The modified topology has been analyzed, designed and a prototype was built. Not only did it overcome the limitations of the original topology, but also the concept is simple and not many extra components are required. It offers zero-voltage switching over an input voltage range of 35 to 80 volts. Based on experimental results from the prototypes, its overall efficiency is 2% higher than that of the original and up to 4% higher in the input voltage range of 60 to 80 volts. Due to the compensating feature of the auxiliary network, its design can be optimized to have a lower value of quality factor, thereby providing a lower voltage stress across the resonant inductor.

With a diode rectifier in the output stage, the power loss is quite significant. The use of MOSFETs in synchronous rectification can reduce this power loss. For current-

fed topologies, the gating signals must be developed from the secondary currents of the main transformer and not their voltages, for proper rectifier operation.

The current-sense transformer topology offers a simple design with no external driving circuits necessary. Being self-driven, synchronization is inherent in the design. At high frequencies, however, leakage inductances associated with the sense transformers may be problematic.

The adaptive control scheme offers accurate timing by developing gating signals for the next operating cycle. It also has the ability to correct timing errors associated with its one-shot timer. Its design is more complex requiring many components. This is a big disadvantage in terms of cost.

The principal contributions of this thesis are as follows:

1) A modified APWM resonant DC/DC converter topology was proposed and analyzed. It was shown that this modified topology has several advantages over its original counterpart including improved performance at a wider range of input voltages, reduction of losses in the resonant inductor and reduction of losses in the output rectifier. The combination of these improvements increase the efficiency overall.

2) Prototype converters of the original and proposed topologies were built. Their frequency of operation is 500kHz and they have a power level of 30W. Experimental results were obtained from these and were compared against each other. The modified topology shows a marked improvement over the original.

3) Two synchronous rectifier topologies were investigated and their operating principles were explained. Computer simulation showed the feasibility of applying these topologies to the converter under study.

5.3 SUGGESTIONS FOR FUTURE WORK

The following suggestions can be examined for future work on this topic:

(i) Building the prototype converter on printed circuit board (PCB) and optimizing the magnetics to further improve the overall efficiency.

(ii) Implementing the current sense transformer and/or the adaptive control scheme in the prototype of the modified APWM resonant converter topology and investigate its performance under high frequencies.

(iii) Research other possible alternatives in the area of synchronous rectification to reduce the power loss in the output stage.

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Appendix

Frequency Characteristics of a Series Resonant Converter

The equations defining Q and ω were given in (2-13) and (2-14). Q represents the quality factor of the resonant tank. It's a normalized measure of the tank's selectivity, i.e. its ability to select a desired frequency and reject all others. The resonant tank impedance of (2-16) is plotted against the normalized frequency, ω for different values of Q and this is shown in Fig.A.1a. It is seen that as the value of Q increases, the sharper the curve becomes. Fig.A.1b shows the plot of the phase difference between v_s and i_s versus ω. When ω is equal to 1, the phase difference is zero and Z_{in} is a pure resistance. The current leads the voltage when $\omega<1$ and the capacitor impedance dominates over the inductor impedance. The voltage leads the current when $\omega>1$ and the inductor impedance dominates over the capacitor impedance. From (2-16), the admittance of the resonant tank can be derived:

$$|Y_{in}| = \frac{1}{|Z_{in}|} = \frac{1}{\sqrt{1 + Q^2\left(n\omega - \frac{1}{\omega}\right)^2}} \qquad \text{(A-1)}$$

Fig.A.2a shows a plot of the harmonic spectrum of v_s. It contains the fundamental plus odd harmonics. This voltage is applied to the input of the resonant tank. Fig.A.2b depicts the plot of the resonant tank response which essentially a plot of Eq.(A-1). Fig.A.2c shows the spectrum of the resonant current. The resonant frequency, f_r, is tuned close to the

fundamental component of v_s, so that the resonant current exhibits negligible response at the harmonics of v_s.

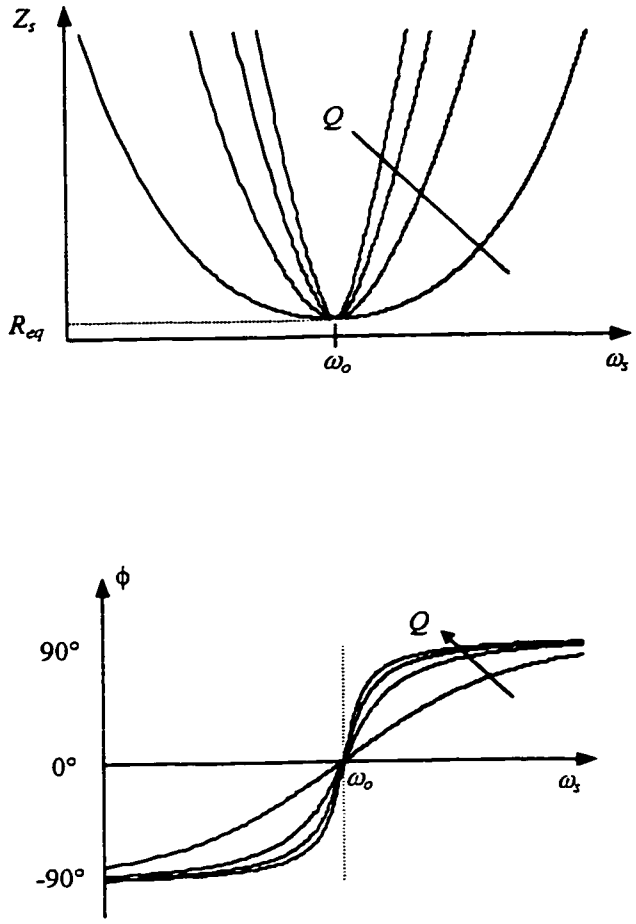
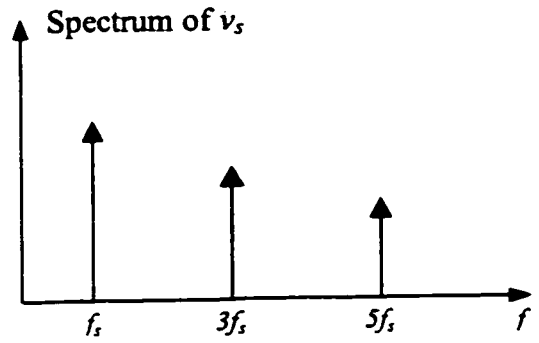
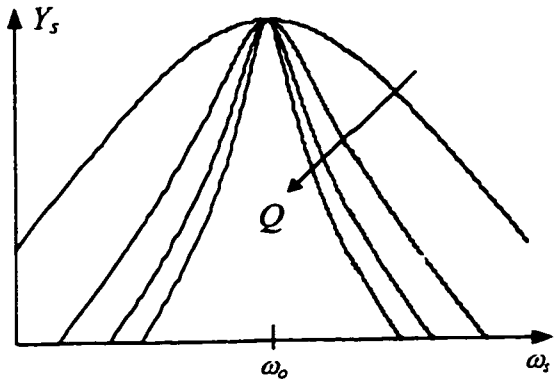


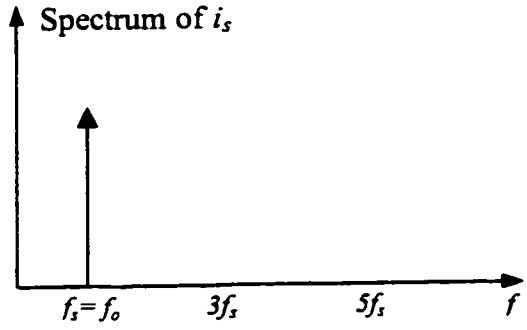
Fig.A.1 Frequency Characteristics of Series-Resonant Circuit: a)impedance vs. frequency, b)phase difference vs. frequency



(a)



(b)



(c)

Fig.A.2 Resonant Tank Response: a)spectrum of v_s, b)admittance vs. frequency of resonant tank for different values of Q, c)spectrum of i_s