Shunt Connected Power Conditioner with Energy Storage for a Hydrogen Fuel Cell System Supplying a DC Nanogrid

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Abstract

Shunt Connected Power Conditioner with Energy Storage for a Hydrogen Fuel Cell System Supplying a DC Nanogrid

Muhammad Ali Akbar

DC power distribution systems (especially DC nanogrids) are becoming a great area of interest for researchers that can lead to a better integration of distributed energy resources (DERs) and supplying local loads in a more efficient way compared to AC systems. As a power source for DC power distribution systems, the use of renewable energy source is increasing every day. When considering renewable energy sources, one can think of the most popular ones like photovoltaics (PV) and wind energy, but another environment friendly power source that is gaining popularity is the hydrogen fuel cell (FC). DC nanogrids for Net-Zero Energy Homes (NZEHs) are expected to include a number of Distributed Energy Resources (DERs). FCs are an interesting choice as supplemental/dispatchable power sources because they can operate as co-generators supplying electricity and heat for NZEHs. The output voltage of the FC changes with the electric power demanded by the load (if the hydrogen injection in the FC is kept constant). Besides, if there is an instant change in the load current demand, it can also damage the FC. Therefore, to protect the FC and supply the load with a regulated voltage, a DC-DC converter is often employed as an interface for the FC. In such a case, load demand variations will lead to variations in the output power of the FC, which is at the maximum power point, when it is supplying a given amount of power at a given current.

This thesis discusses the realization of a control scheme that enables a FC system to operate at the maximum power point by using an Energy Storage System (ESS) based on a super capacitor (SC) and another power electronics interface as supporting unit. The output of the ESS is connected in shunt with the output of the FC system to the DC (load) bus. The ESS is current controlled to force the FC system to supply a constant current. In this way, the FC will supply an ideal, maximum power point, current even as the power demand by the electric load varies. Besides, the

ESS can also provide the load with more power than the rated value of the FC system. Moreover, an additional control scheme is also implemented in the ESS to keep the voltage at the SC within safe and useful values.

Finally, the proposed scheme is verified with hardware experiments. Experimental results with power electronics interfaces showing the voltage regulation in the DC (load) bus, FC current control and the regulation of SC voltage are presented. It is demonstrated that the FC can be operated at its maximum power point, using a SC-based ESS with injected current and SC voltage control loops.

This thesis is dedicated to the Almighty

my strength and power, who led me in the right way for

Success.

To my parents and family for their love and support

and

to my teachers who showed me the right path.

ACKNOWLEDGMENTS

In the name of ALLAH (God) Almighty, the Most Compassionate, the Most Merciful, all praises and thanks be to HIM. This is by the grace of God.

Then, I would like to express my deep gratitude to my advisor, Professor Luiz A. C. Lopes for his support and valuable guidance throughout this work. His character, positive attitude and intelligence has greatly impacted my life. His passion for research, broad knowledge of power electronics and easy to understand ways of delivering his knowledge, were very beneficial for me and it influenced my perception of engineering in general. Whatever I have learned from him during this period, will be beneficial for my career.

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Nomenclature

PEM: Proton Exchange Membrane

ESS: Energy Storage System

RES: Renewable Energy Source

FC: Fuel Cell

SC: Super Capacitor

NZEHs: net-zero energy homes

PEMFC: Proton Exchange Membrane Fuel cell

HEV: Hybrid Electric Vehicle

PWM: Pulse Width Modulation

EMI: Electromagnetic Interference

RFI: Radio Frequency Interference

ADC: Analog to Digital Converter

DERs: Distributed Energy Resources

HV: High Voltage

LV: Low Voltage

AC: Alternating Current

ADC: Analog-to-Digital Converter

DC: Direct Current

Chapter 1 Introduction

Demand of energy is increasing every day and there is a great concern over using fossil fuel as the source of energy, as a result, the use of renewable energy sources (RESs) is increasing every day. When renewable sources of energy are considered, one can think of sources like photovoltaics (PV) and wind energy, but another fuel source that is gaining popularity is hydrogen Fuel Cell (FC) which has zero emission and is environment friendly. With the development of Proton Exchange Membrane (PEM) fuel cells, the output and reliability of FCs has been greatly improved. Recent advancements in power electronics and controls led to the implementation of nanogrids, where multiple RES are integrated with energy storage units. Nanogrids can be controlled as a local grid but at a very small scale, roughly less than 50 kW [1]. Microgrid is higher in scale as compared to nanogrids and there can be multiple nanogrids in a microgrid, which can also be connected to the existing utility grid. The idea of connecting the utility grid with a nano or microgrid is becoming popular considering its benefits. Nanogrids are considered vital for future smart homes and smart commercial buildings which will lead on to net-zero energy homes (NZEHs), a concept that is very popular these days. The idea of NZEHs is that, by incorporating distributed energy resources (DERs), buildings/homes will be able to produce the amount of energy they consume in a given period of time, typically a year. To achieve clean energy in future smart homes, RESs and energy storage systems (ESS) are to be integrated together to form a nanogrid. Due to the need of clean energy sources, fuel cells are being considered to be integrated into NZEHs, automobiles, and airplanes as the main or a supplemental power source. With time, the reliability and safety of FC Systems (FCSs), which concerns the FC and a power electronics interface has increased significantly. Many big automobile companies are also investing in the development of hydrogen based economy, the greatest examples are Toyota Mirai and Kenworth truck. Recently, a Toyota Mirai traveled 480km with 5kg tank of hydrogen, which is significantly higher than what is achieved with “standard” batteries [2]. There is still an ongoing debate on whether batteries are the best choice for electric vehicles (EVs), or fuel cells, considering the infrastructure required and cost per kg. Shell also demonstrated on-site hydrogen production plant technology in one of their gas stations in UK. FCSs are also being used in (Unmanned Aerial Vehicles) UAVs to increase their flight time from hours to days, the only byproduct one get from FCs is pure water that is why FCSs are considered very environment friendly. FCSs are being used

in modern NZEHs commercially, products like “VITOVALOR” by Viessmann Manufacturing Company are getting popular in the market as it powers the house heating system through the heat produced by the fuel cell as well, which is better than the old systems in terms of cost effectiveness, efficiency, size and environment friendly byproducts [3]. Some other power companies like “Bloom Energy” are also implementing fuel cell based small scale power supply systems for commercial buildings [4]. A standalone DC distribution system has a clear advantage over AC systems as, most RESs supply inherently DC and most appliances these days work on DC and require an AC-DC converter inside. All such appliances can directly be supplied through DC nanogrid and this will eliminate the need of AC-DC converters and make the system more simplified. Moreover, DC systems provide higher efficiency, they are cost effective and simpler compared to their AC counterpart.

The implementation of a nanogrid or a microgrid may require RESs with Energy Storage Systems (ESSs), if they are to be used “off-grid”. These RESs and ESSs are connected to the nanogrid through power converters to make the system more reliable and control the power flow. The power converters which connect RESs with the DC bus can be unidirectional because one doesn’t need any power flowing backwards to the RES. On the other hand, for ESSs, bi-directional power converters are required, so that the storage elements can supply power whenever needed and can absorb power when required. Different types of storage elements can be used for the support of RESs depending upon their properties. Figure 1.1 shows the structure of a DC nanogrid for a future home, which contains power generation units (photovoltaic solar cells, wind turbine), local energy storage units, a hybrid electrical vehicle interface and house loads. The system is also connected to the local grid [5]. It is a dual DC bus system with a higher bus voltage level (380V) to drive high power loads and a lighter bus voltage level (48V) in order to drive low power loads. The higher DC bus voltage level is chosen as 380V to match the industry standard intermediate DC voltage in consumer electronics. A lot of research is being carried out to decide the voltage levels for the DC bus. In this Thesis, the aim is to consider the lower voltage DC bus as 48V in a DC nanogrid. However, it can further be extended to any potential level which is required.

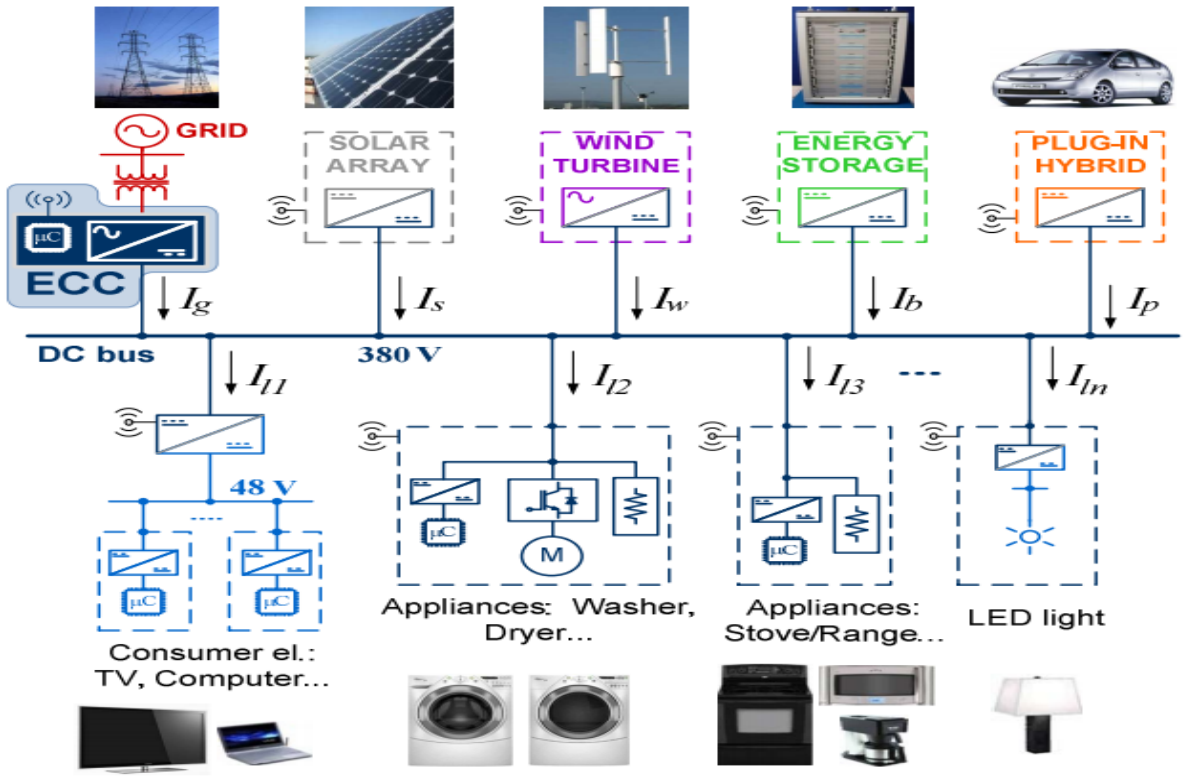

Figure 1.1 Configuration of a DC nanogrid [5]

This Thesis mainly focuses on the application of a FCS in a DC residential nanogrid. Standalone fuel cell (only) power supply systems may not be the best choice because FCs have poor dynamic response due to the flow regulator needed to maintain the air in the cathode terminal. Moreover, whenever there is a sudden change in the load in a nanogrid, it will result in a sudden spike in current demand which can damage the fuel cell. ESSs can also be used to support the FCS in such scenarios. ESSs, (systems that include a power interface and that are connected at the output of the FCS) can also act as a backup system for a nanogrid with a FCS as a power source because the electrode assembly membrane of FC can also fail, it can suffer internal gas leakage and cell flooding/drying.

As a support unit in a nanogrid, whenever the load demand changes instantly, the ESS can provide support to the FCS by supplying/absorbing high currents for short periods of time. In this way there won't be any sharp change in the fuel cell current. The selection of storage units/medium plays an important role in the design of the nanogrid. Therefore, before the selection of a storage unit for a nanogrid, one should consider their properties. Figure 1.2 shows that hydrogen fuel cells can deliver high power for long periods but they have very low specific power. Super capacitors

can provide high specific power but hey have limited specific energy storage capacity. Moreover, they can be charged quickly. Batteries, on the other hand, have low specific power but they have more energy capacity than super capacitors.

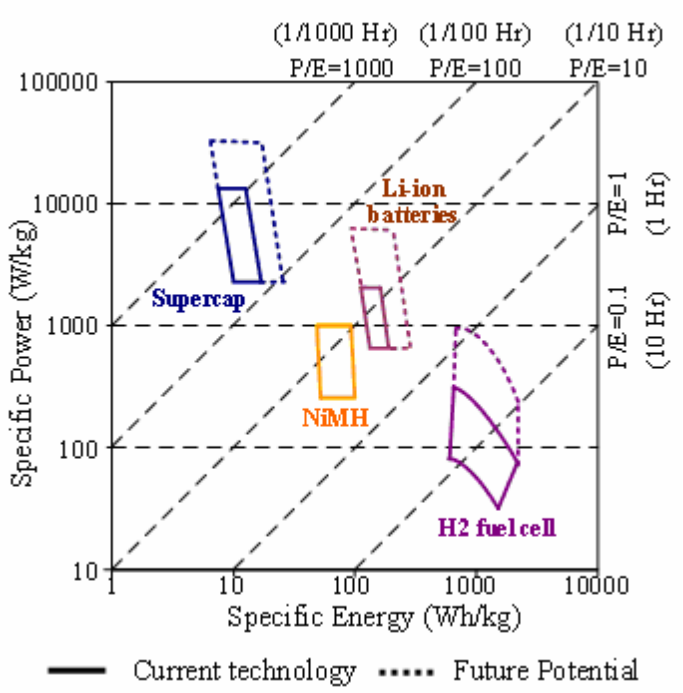

Figure 1.2 Power and energy comparison of super capacitor, battery and fuel cell

More research work has been carried out on the application of fuel cells and storage units in automobiles then on the implementation of DC nano/micro grids with fuel cell as a power source. Considering automobiles, hybridization of FCs with super capacitors has good performance. Super capacitors can effectively assist the FCS to meet the transient power demand because it can be charged and discharged at high currents, and on the other hand high current charges and discharges reduce the life time of batteries. Nonetheless, for automobiles FC/battery/super capacitor hybrid is a more practical answer because the startup time for PEM fuel cell is around 5-10 min, in which case, the battery provides its higher specific energy than the super capacitors [6]. Researchers have used different control strategies to interface super capacitors with the DC bus, as a storage unit, by using bi-directional converters. The condition to ensure good operation is that the DC bus voltage regulation should be faster than the storage device voltage regulation. The voltage of super capacitor is controlled by the current delivered by FCS [7]. The FC net power is mainly dependent

on the air and hydrogen flow rate and pressure, and heat and water management. Some researchers used advanced control on the air flow regulator to operate the fuel cell at its maximum power point (MPP) [8]. Considering the research work done in this area, this thesis presents the implementation and experimental verification of a DC nanogrid using super capacitor as a supporting unit for the FCS. The voltage in the DC (load) bus should be constant, therefore the output voltage of the fuel cell system should be regulated. One knows that, in order to make the fuel cell operate at it maximum power point, the current at the output of its interface converter should be constant. For that, one employs an ESS, where a Super capacitor is connected to the DC bus though bi-directional power electronic converter. Whenever there is a change in output load, the, ESS should provide/absorb the mismatch between the variable load current and the "ideal" current of the FCS. Thus, the super capacitor converter has to be current controlled, with a faster control loop than the voltage control loop in the super capacitor.

Using battery or super capacitor systems as supporting units for FCSs have their own pros and cons. A typical Lithium battery can store 10-30 kWh, and can be charged or discharged in 10 to 20 minutes. Batteries have shorter life span, fewer charge and discharge cycles as compared to super capacitors, low power density and depth of discharge. A lot of researchers are working to improve the reliability of batteries. Super capacitors, on the other hand, present high power density, longer life span, more charge/discharge cycles as compared to batteries, fast charging and discharging and fast transient response. Fast transient response and fast charge/discharge cycles make super capacitors able to supply and absorb high power for short periods, whenever the load increases or decreases. The combination of the fast and large transient response of super capacitors to support the slow transient response of fuel cells is the most practical choice for DC nanogrids.

1.1 Problem statement and proposed solution

The hydrogen gas injected into a fuel cell can be controlled by the hydrogen injection controller. The maximum power point of a fuel cell depends upon its output current, which changes with the output load. Any changes in the output load changes the fuel cell current. That is why it is hard to keep the fuel cell in the maximum power region/point. At the same time, the output voltage of the fuel cell is not regulated. Regulation of the voltage in the DC bus is a usual requirement for a DC

nanogrid. Moreover, recall that whenever there is an instant change in the load, the output current of the fuel cell will change very fast, which is not good for the performance of FCs, and that can be damaging. These are the major problems faced by power system designers: To make the FC operate at its maximum power point, by using power electronic interfaces and at the same time keeping the fuel cell un-damaged by avoiding sudden current spikes. In order to use FCS efficiently as a power source in a nanogrid, ideally one needs to make the FCS operate at its maximum power point, which may vary for every fuel cell. This Thesis provides a control scheme which forces the FCS to operate at the maximum power point by using super capacitor based ESS as supporting unit. In this Thesis and experimentation, "Horizon-PEM-Fuel cell-H-2000" [9] fuel cell is used along with a commercial power electronics interface designed for FC applications. In Figure 1.3, one can see the power and current (P-I) curve of the fuel cell. It is evident that the fuel cell (rated) output power is around 2000W at 70A and it is about the maximum power point of this fuel cell. For an efficient and cost effective fuel cell power supply system, one should operate the fuel cell close to this point.

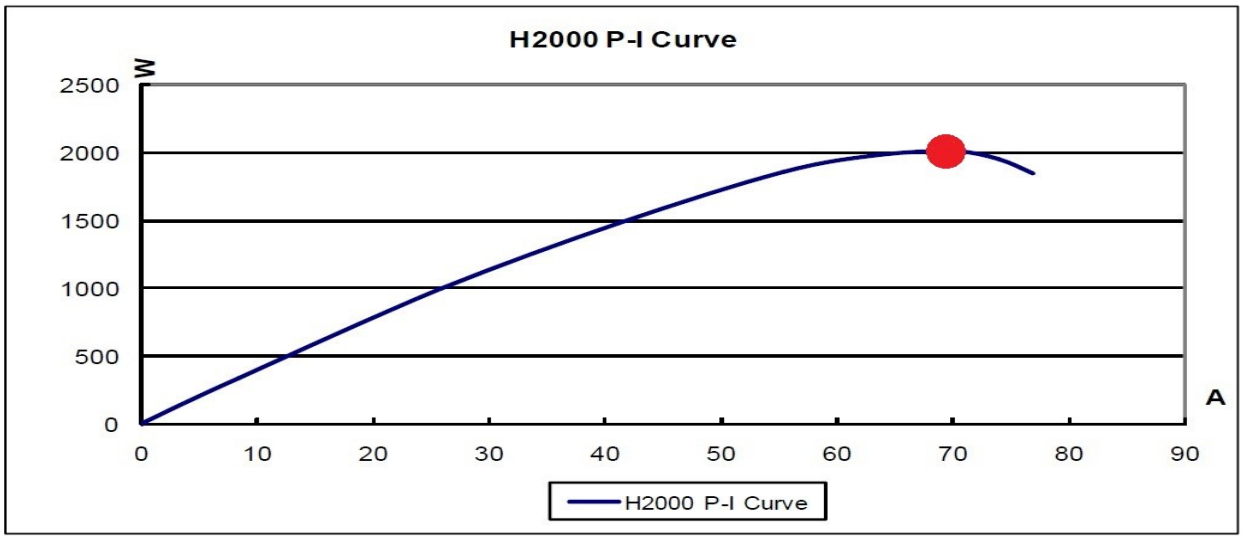

Figure 1.3 Hydrogen Fuel cell P-I Curve

In Figure 1.4, one can see that when the current reaches 70A, the output voltage at this point is 28.8V. This is the ideal operating point for the fuel cell. This Thesis discusses the implementation of a control strategy which forces the fuel cell to keep operating at 70A/28.8V by using a super

capacitor as storage unit of an ESS, which is connected in shunt at the output of the FCS which corresponds to the DC (load) bus.

The ESS consists of a bi-directional DC-DC converter with an injected current control loop, to force the output current of the FCS to be constant, as the power demanded by the load varies. Also, it includes a SC voltage control loop, which guarantees that the SC is not damaged by over-voltage and will also have some energy left, a minimum voltage, to supply a given amount of power support to the FCS.

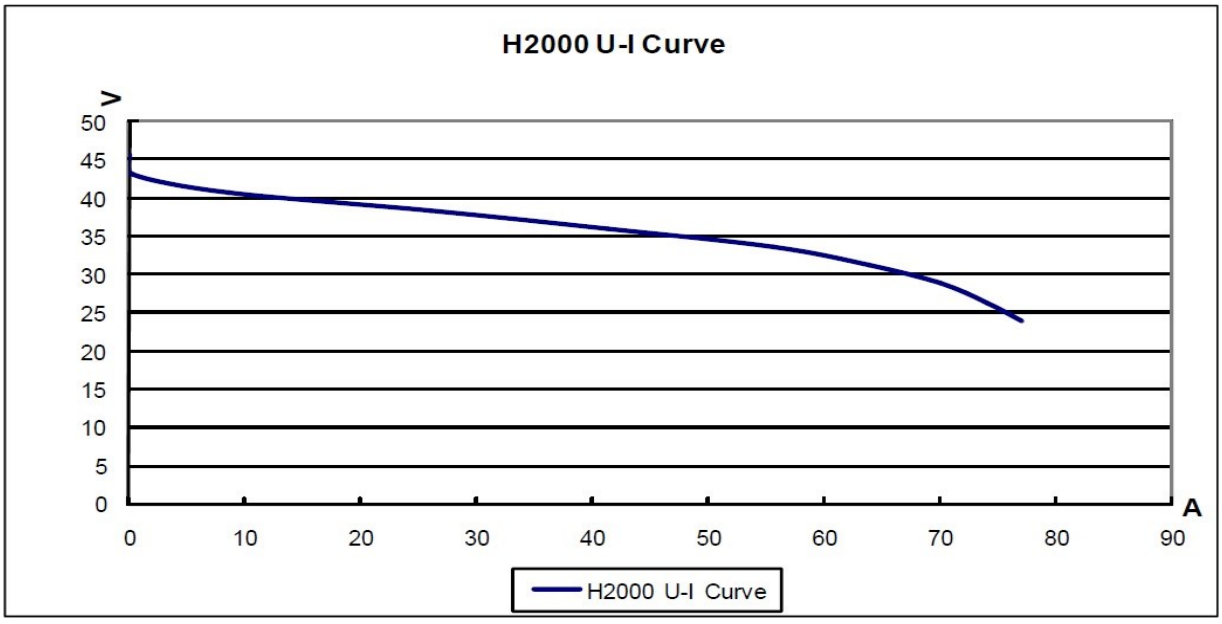

Figure 1.4 Hydrogen Fuel Cell V-I Curve

Super capacitors which are used in this project are Maxwell 165F super capacitors with usable specific power of 3300W/kg [10].The maximum voltage that this super capacitor can reach is 51V. In case when the load increased above the rated value, the extra required current would be supplied by the super capacitor. Due to which, the voltage in super capacitor decreases, and it should not discharge below a certain point. Contrary to this, when the required load is less than the rated current (e.g. 70A), this extra current should charge the super capacitor, due to the current control loop. The control scheme that was developed in this work, also prevents the super capacitor from charging and discharging beyond a certain point therefore ensuring the safety of the super capacitor. However, in this case the FCS will not operate exactly at the point of maximum power point.

1.2 Contributions of the research work

This Thesis focuses on an ESS as a power conditioner for a FCS that allows the FC to operate with a constant current, around the point of maximum power. The interface, power electronics converter and control logic, used in the SC-based ESS is developed in house.

The main contributions of this work are as follows:

1) Design and implementation of an injected/output current control scheme for the ESS, to control the output current of the FCS.

2) Design and implementation of an input voltage control loop to prevent the SC used as storage medium from over charging and discharging below a certain limit.

3) Experimental verification of the proposed power conditioner.

1.3 Outline of the Thesis

The remaining Chapters of this Thesis are structured as follows:

Chapter 2, discusses the setup of the commercial unidirectional power converter of the FCS, for voltage regulation in the DC (load) bus, the design and assembly of a class-C bi-directional DC-DC converter for the ESS.

Chapter 3, presents the voltage regulation characteristics in the DC bus, due to the FCS, design of the output current control loop and input (SC) voltage control loop of the ESS, explanation of the final system schematic and simulation results.

In Chapter 4, the implementation of the prototype of the proposed system including both power converters, source and storage elements is discussed. The performance of the proposed control scheme is verified through experimental results which are presented and discussed in this Chapter.

Chapter 5 highlights the outcomes with the conclusion of the Thesis and suggests future work that can be conducted related to the project.

Chapter 2 Power Converters Assembly and Implementation

The system to be realized consists of a commercial (Zahn – Model CH6390-SU) unidirectional DC-DC converter for the fuel cell, which is referred as FC Converter in the Thesis, whose main task is to regulate the magnitude of the voltage supplied to the load. Recall that the output voltage of the fuel cell varies with its output current and this project requires the DC bus voltage to be regulated at 48V. A bi-directional DC-DC converter is used to interface the ESS (super capacitor) to the load bus. The main task of bi-directional DC-DC converter is to supply the mismatch between the load current and the ideal current to be supplied by the FC Converter, so that the current from the fuel cell corresponds to that where the FCS has its maximum power. Thus, there is no incompatibility between the control goals of the two converters. The bi-directional DC-DC converter will also prevent the overcharging and discharging of the super capacitor beyond a point defined in the control loop.

2.1 FC Converter Implementation

The voltage in the DC bus (load bus) should be regulated in this system. As previously mentioned, to achieve voltage regulation in the DC bus a unidirectional DC-DC FC Converter has been used. In Figure 2.1, the power circuit of FC Converter is presented. This converter uses Half H Bridge or class C configuration, where there are two MOSFETs which control the power flow in the forward direction. The switching frequency for the FC Converter is exactly 31,250 Hz. From Figure 2.1 one can see that, if the input voltage for the converter is 28.8V at 70A input current, assuming that there are very few losses in the converter, then the input and output powers should be the same. For a DC bus voltage regulated at 48V the output current should be 42A in this case.

In the FC Converter, there is a closed loop control for voltage regulation, to supply the load with regulated voltage magnitude. In Figure 2.2, the control circuit diagram can be seen for the FC Converter. There, one can see that the load is connected to a voltage sensing circuit which then passes through a differential amplifier, giving the load voltage. A reference signal which is

connected to a variable resistor is mentioned as resistor voltage reference, this is the reference signal corresponding to 48 V at the load.

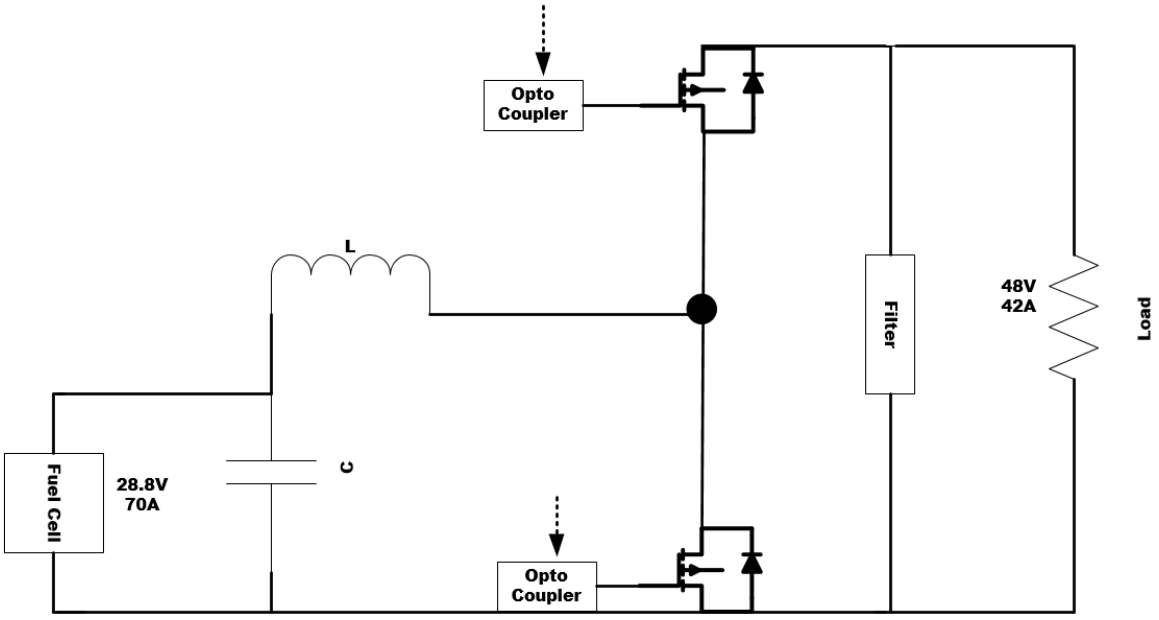

Figure 2.1 FC Converter Power Circuit

By adding the two signals mentioned above, one can find the error between the desired and actual value of the output voltage of the converter. This error is then passed through the compensation circuitry which gives us a current reference for the input side (boost) inductor current. The input current is measured through a Hall sensor. The measured value of current is called feedback current. Then the current reference and feedback current are compared to get the error that will be then passed into another compensator circuit. After that stage one will get a pulse width modulation (PWM) reference signal which will produce the gating signals for the MOSFETs. As mentioned earlier that FC Converter operates at 31250Hz switching frequency. A signal generation circuit is implemented in the FC Converter. A crystal controller oscillator generates a saw tooth waveform which is needed in pulse width modulation. The switching circuitry (comparator) will be fed with the output of the signal generator (saw tooth) and PWM reference from the output of compensator, which will produce the gating signals for the MOSFETs. The gating signals generated from the switching circuit control the opto-couplers, used for isolation, connected to the gate terminal of each MOSFET. These opto-couplers turn the MOSFET on and off depending upon the input gating signal.

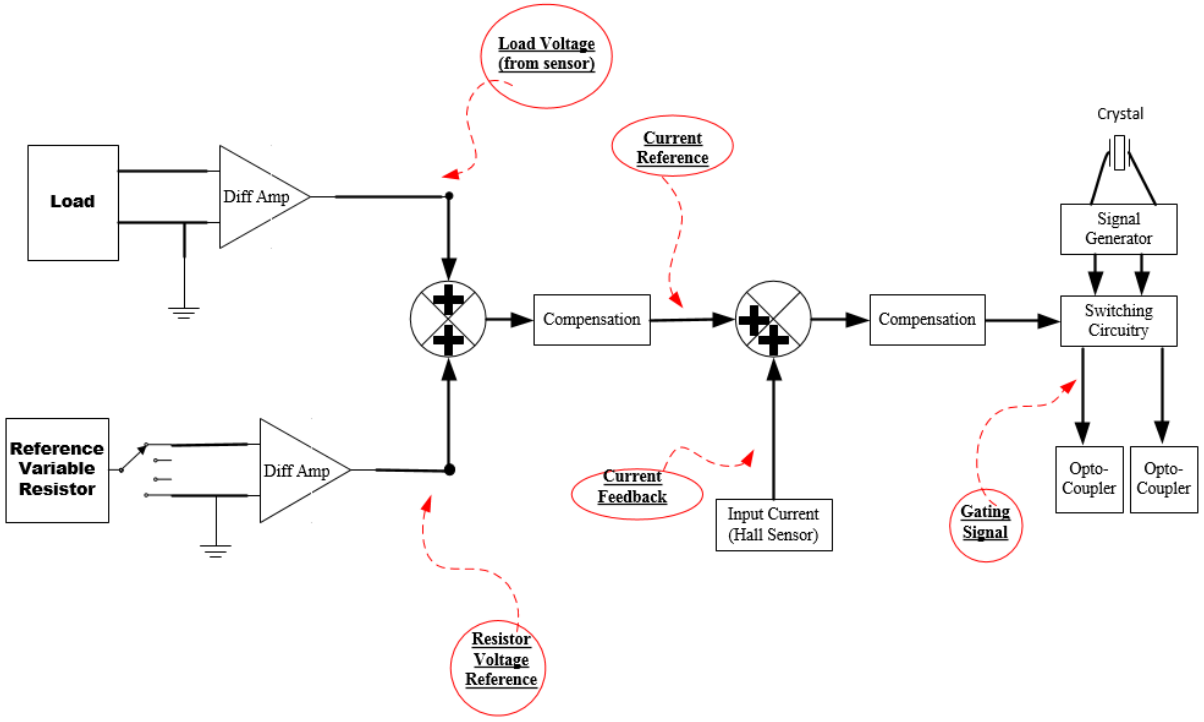

Figure 2.2 FC Converter Control Circuit

By the controlled switching of these MOSFETs, one will control the inductor current in order to regulate the DC bus voltage at 48V. In Figure 2.1 it can be seen that the Fuel cell output terminals are connected to the FC Converter, the output of the fuel cell passes through an inductor which provides boost functionality and limits the current ripple in the fuel cell. At the output terminals of the FC Converter, there is another CLC filter which filters the switching harmonics at the output voltage, thus making the output voltage ripple negligible.

In order to make the output voltage of the FC Converter regulated at 48V, the reference variable resistor has to be adjusted, shown in Figure 2.2. Once the output voltage is set to 48V, then by the action of the PI controller and PWM, the input voltage of converter can vary but it will not have any effect on the output voltage of the FC Converter. Which means that even if the fuel cell output voltage changes, it will not affect the voltage in the DC bus. In the same way, if the load in the DC bus changes, it will only change the output current not the voltage, in steady-state conditions.

In addition to the power and control circuitry, the FC Converter also uses additional circuitry for protection and to avoid overheating. Power transistors are attached to an aluminum case and to the same aluminum case where there is a thermistor attached, which provides the thermal feedback. Whenever the temperature rises above 60 degrees, a fan is turned on to reduce the temperature. In an event of excessively high ambient temperature the FC Converter will automatically reduce the current to the load, to hold the transistor temperature to a safe level. In such a case, the converter will not be able to regulate the load voltage at rated (48 V) value.

Besides, for protection, there is a "disable" mode in FC Converter as well. In single quadrant or unidirectional operation the disable mode prevents the flow of current from the source to the load. In two quadrant or bi-directional operation, the disable mode will prevent the current flow from source to load by clamping the reference output voltage to a near zero value. However, it allows the reverse current to flow from the load to the source. In this project FC Converter is used, only in single quadrant or unidirectional mode, to prevent any current flowing back to the fuel cell.

2.2 Bi-directional DC-DC Converter Implementation

The voltage in the DC bus (output) will be regulated by FC Converter that is why any changes in the load will not affect the DC bus voltage. Whenever there is a change in output load, the current demand will change and the output current of FCS will also change, accordingly. As discussed in chapter 1, FCS should operate at its maximum power point. At the maximum power point, the fuel cell should be supplying 70A current at 28.8V output voltage (Figure 1.4). Therefore, the fuel cell output current should be 70A, in order to operate at the maximum power point (Figure 1.3). The ESS cannot control this current directly. However, by forcing the current delivered by the FC converter to be 42 A, the FC current is indirectly adjusted to the desired 70 A. Moreover, if there is an instant change in load, the FCS has a very poor dynamic response and needs a supporting unit/element with fast transient response to supply the load for short duration of peak power demand or load change until the FCS slow dynamic response catches up.

The supporting element should be able to absorb and supply the power whenever needed, for that a super capacitor and respective interface converter is used in this project. Because of the fast transient response of super capacitors, they can provide more power in short time intervals, until

the FCS slow dynamic response catches up. For this project, the ESS is interface with the DC bus at the same point where FC Converter is connected to the DC bus for the support of the fuel cell. In order to interface the SC with the DC bus, a power converter is needed because the DC bus is at 48V and the super capacitor voltage level drops as it supplies power to the load. Since the voltage regulation in the DC bus will be achieved by the FC Converter, one cannot have the second power converter to regulate the load voltage but for load current control, thus indirectly the fuel cell current.

The required power converter should be suitable for current control and later on, one needs to control the voltage levels in the super capacitor. One have to consider that the converter should be DC to DC and that it should support bi directional power flow. The converter used in this project is a new realization of an existing 4-switch Texas Instrument (TI) DC-DC converter "LM5170EVM-BIDIR Evaluation Module*"* [11] that was designed for a similar application. For bi-directional current flow, a class-C converter would be sufficient, the TI converter consisted of two half bridges with an inductor between them. This converter presents additional features, such as the capability to operate with a DC bus voltage lower than the supercapacitor voltage, what can happen during severe load transients. Therefore, this solution/alternative was retained.

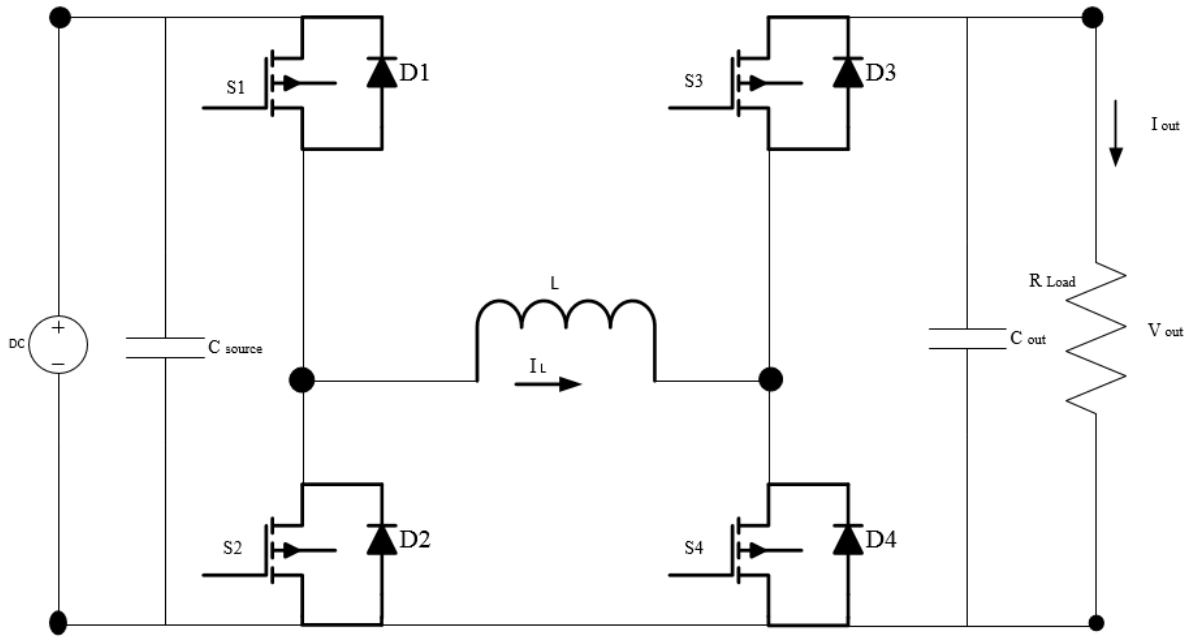

Figure 2.3 4-switch DC-DC Converter

In Figure 2.3 the converter circuit diagram is shown, presenting four switches (S1, S2, S3 and S4) connected in two half bridges, and can operate in two quadrants. For this project, S1 is always kept ON and S2 is always kept OFF to make it a class-C converter which is the essential feature required for this project.

2.2.1 Switching Scheme

For the 4-switch converter to operate in class-C mode, S1 should always be ON and S2 should always stay OFF. In Figure 2.4 and Figure 2.5, one can see the current/power flow in the converter while it is operating in class-C mode with respect to the duty cycle ($D_{OFF} = 1 - D_{ON}$).

1) D_{ON}: The switches S1 and S4 are turned ON, and conducting, while S2 is always OFF and the gating signal of S3 is the complement of S4. (Figure 2.4)

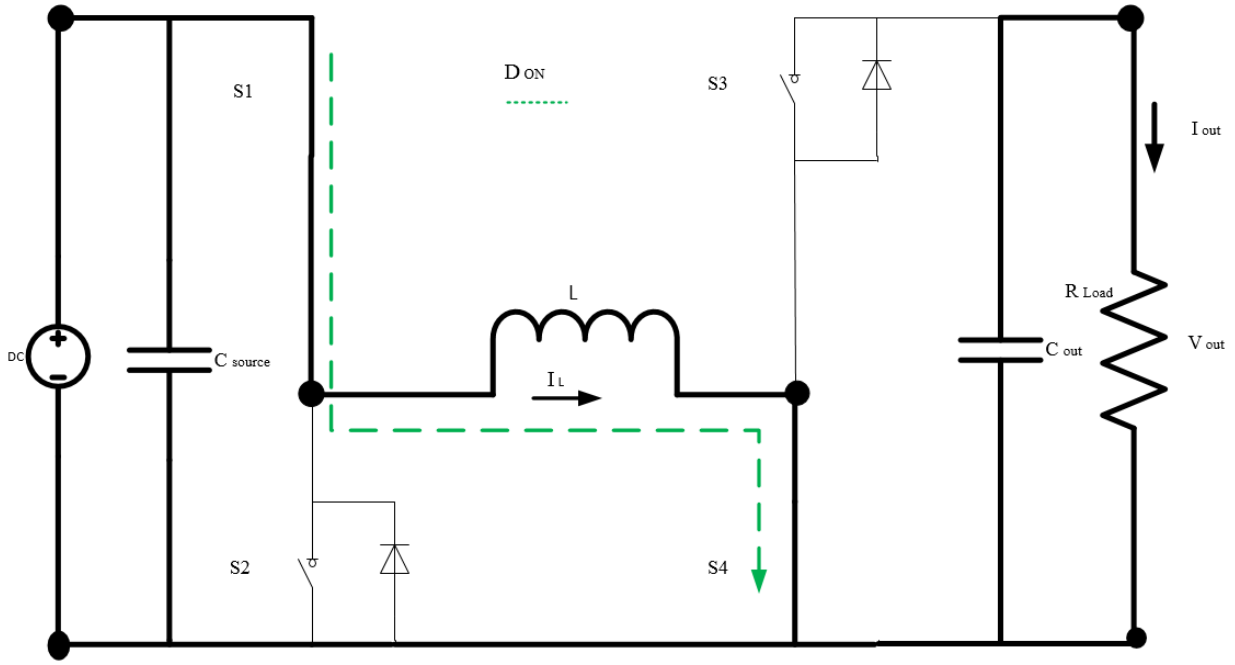

Figure 2.4 DC-DC Converter in *DON* state

2) D_{OFF}: The switches S1 and S3 are turned ON, with D3 conducting, while S2 is always OFF and S4 is the complement of S3. (Figure 2.5)

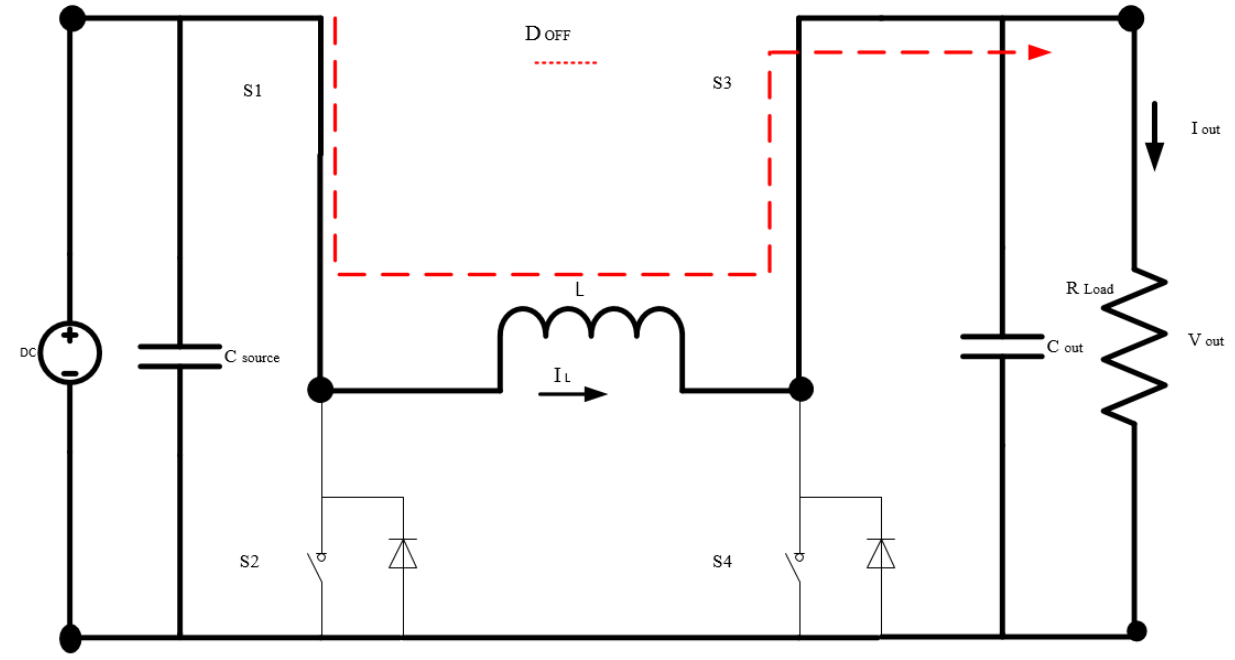

Figure 2.5 DC-DC Converter in *DOFF* state

In case of D_{ON} the inductor will charge, its current will increase, while in case of D_{OFF}, the inductor will discharge across the load. "D_{ON}" is shown by the green dotted line while "D_{OFF}" is shown by red dotted line.

In Figure 2.6 one can see that S1 is always ON and S2 is always OFF. S3 is the complement of S4. When S4 is ON the inductor charges and the inductor current rises. When S4 is OFF the inductor discharges across the load and the inductor current decreases.

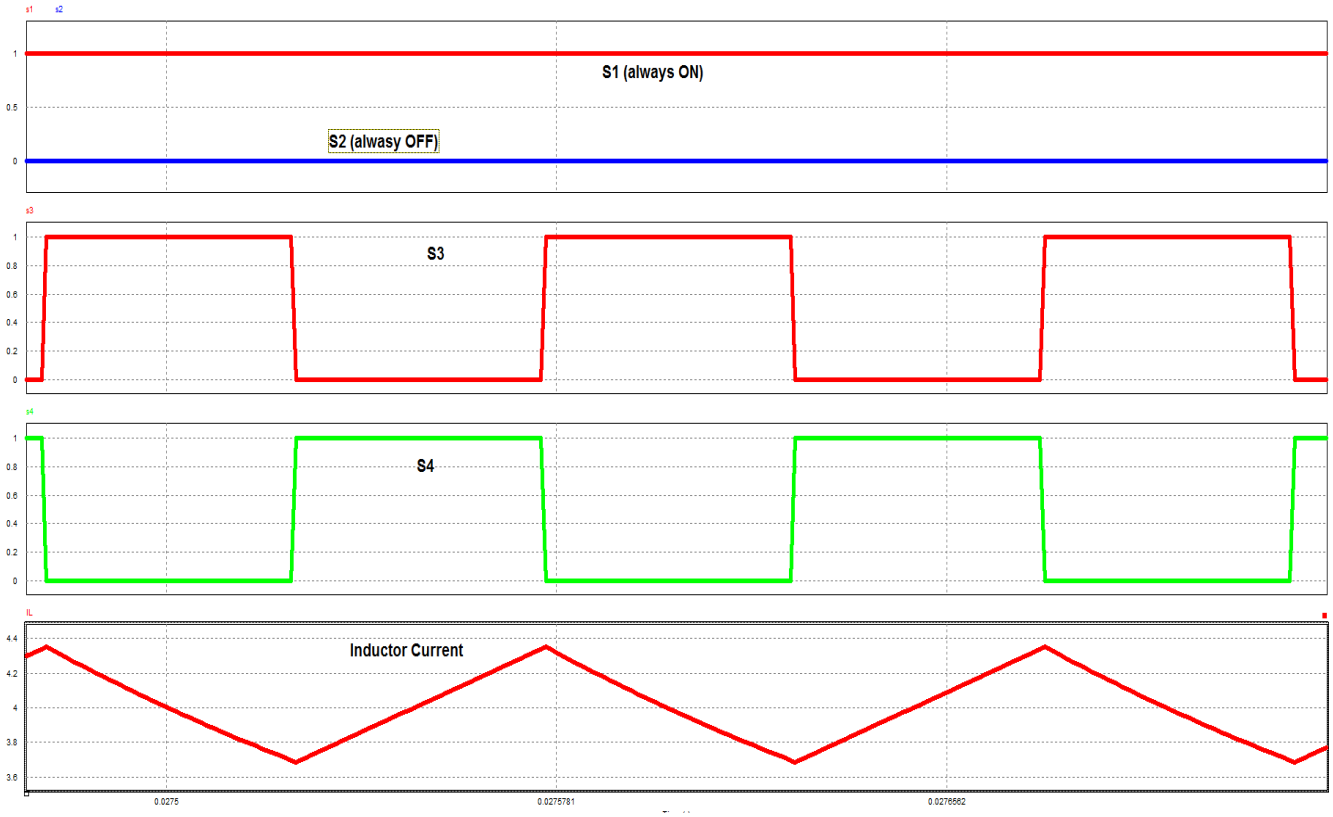

Figure 2.6 Inductor current w.r.t the Duty cycle

The truth table (Table 2.1) of all switches is given, when the converter is operating in class-C mode.

Table 2.1: Truth-Table of 4-switches for both modes of operation.

Mode	State	Switch 1	Switch 2	Switch 3	Switch 4
Class-C	D_{ON}	ON	OFF	$\overline{PWM}$	PWM
	D_{OFF}	ON	OFF	PWM	$\overline{PWM}$

2.2.2 Component calculation and selection

When designing a power converter, one has to consider a few specification parameters first. These calculations are being made considering the Texas Instrument Converter Power stage calculation manual [12]:

1) Input voltage range: $V_{IN(min)}$ and $V_{IN(max)}$
2) Nominal output voltage: V_{OUT}
3) Maximum Output current: $I_{OUT(max)}$
4) Switching Frequency: f_s

After considering these parameters, one can then use this data to select the appropriate inductor and capacitor required for the converter. The minimum input voltage of the converter is the minimum voltage of the super capacitor. The super capacitor used in this projects, is a "Maxwell Tech BMOD0165 P048 B09". The maximum voltage level that one can get is 51V. For this project, the minimum and maximum voltage range are chosen to be 24V to 44V. Later on, the voltage regulation in the super capacitor will be discussed. The nominal voltage of the super capacitor for this project is 32V. The nominal output voltage of the power converter is the same as the DC bus voltage, which is 48V. Considering the maximum current limit of the available inductor, the maximum output current of the 4 switch DC-DC converter was chose to be 10A. The value of the switching frequency is selected to be 10 kHz, considering the 4-switch Texas Instrument (TI) DC-DC converter. Once these parameters are selected, now one can move on to the selection of inductor, capacitors and other components required.

1) Duty cycle selection [12]: $D_{(min)}$

$$D = 1 - \frac{V_{IN} \times \eta}{V_{OUT}} \tag{2.1}$$

$$D_{(min)} = 1 - \frac{V_{IN(max)} \times \eta}{V_{OUT}} = 1 - \frac{44 \times 0.9}{48} = 0.175$$

$$D_{(max)} = 1 - \frac{V_{IN(min)} \times \eta}{V_{OUT}} = 1 - \frac{24 \times 0.9}{48} = 0.55$$

Here the efficiency of the converter η is considered to be 90%, which is a realistic value for a force-commutated converter. The output voltage (V_{OUT}) in the DC bus will remain constant at 48V. The minimum input voltage $V_{IN(min)}$ is 24V while the maximum input voltage $V_{IN(max)}$ of converter is 44V. After putting the input voltage values in the above equation, one can get the minimum duty cycle of 0.175 and maximum duty cycle of 0.55.

2) Current Ripple estimation [12]:

$$\Delta I_L = Ripple\% \times I_{OUT}(max) \times \frac{V_{OUT}}{V_{IN}} \tag{2.2}$$

$$\Delta I_L = Ripple\% \times I_{OUT}(max) \times \frac{V_{OUT}}{V_{IN}} = \frac{2}{100} \times 10 \times \frac{48}{24} = 0.4\text{A}$$

In order to select the inductor for the power converter one has to consider the allowed ripple in the inductor current (ΔI_L). If the inductor current presents a large ripple, the RMS current imposed on the output capacitor can be very large, which can reduce its life time. A practical value of the current ripple to be used is 2% of the output current. From Eq. 2.2, one can see that inductor current ripple would be maximum when the input voltage of converter is 24V (minimum voltage level of SC).

3) Inductor Selection [13]:

$$L \geq \frac{T_s \times V_{OUT}}{2 \times I_{LB}} \times D(1-D) \tag{2.3}$$

From Figure 2.7, one can see that in case of D_{ON}, the inductor current rises as the inductor charges and it falls in case of D_{OFF}, when the inductor discharges. In Figure 2.6 (b), one can see that inductor current never goes to zero in continuous conduction mode (CCM).

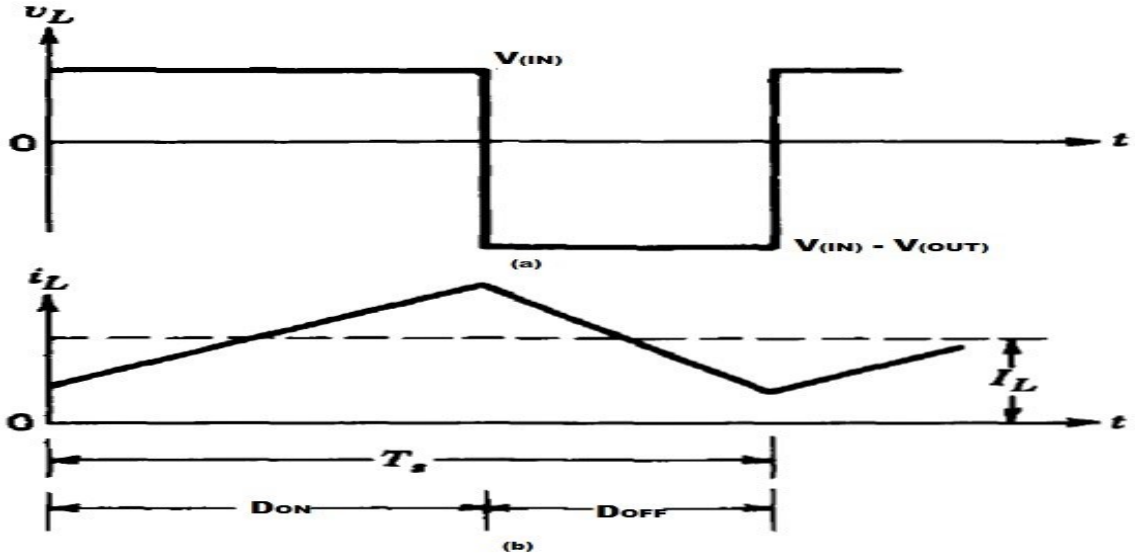

Figure 2.7 (a) Duty Cycle (b) Inductor current [13]

Figure 2.8 shows the inductor current i_L. The average value of the inductor current (I_{LB}) will be [13]:

$$I_{LB} = \frac{1}{2} i_{L.\,peak} \tag{2.4}$$

The maximum inductor current ripple has been defined previously. Using Eq. 2.4 one can calculate the average value of inductor current I_{LB} which is 0.2A.

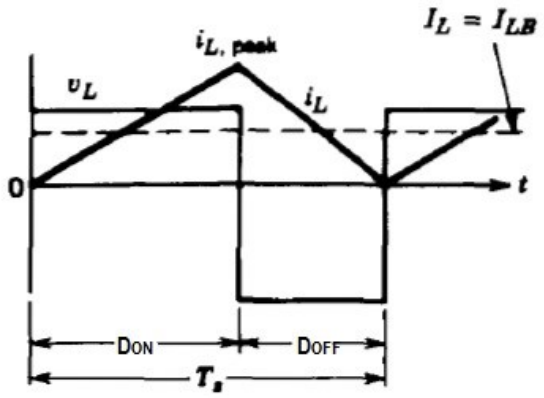

Figure 2.8 Inductor current vs T_s (switching period) [13]

From Figure 2.9, one can see that the duty cycle goes from 0.175 to 0.55. For this converter, the value of I_{LB} is maximum when D is 0.5. For the calculation D is considered 0.5.

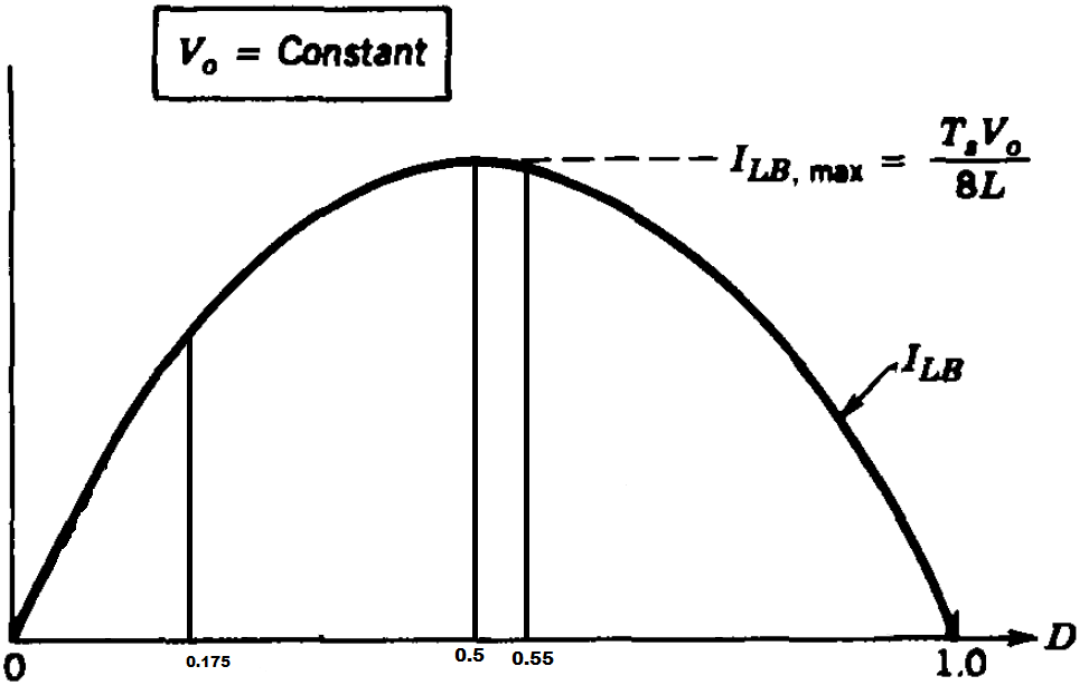

Figure 2.9 Duty Cycle vs average inductor current

One can re-write equation 2.3 as:

$$L \geq \frac{\frac{1}{f_s} \times V_{OUT}}{2 \times I_{LB}} \times D(1-D)$$

$$L \geq \frac{\frac{1}{10000} \times 48}{2 \times 0.2} \times 0.5(1-0.5) \geq 3.0\text{mH}$$

A lower inductor value will reduce the solution volume. One also has to consider that the inductor must always have higher current rating than the maximum given current because the current increases with decreasing inductance. That is why in practical implementation these values can change. In the practical implementation, one should either shield the inductor or keep it far from the printed circuit board as much as possible to avoid any interference with the control circuitry.

After careful consideration of the above calculations and the availability of inductors in the market, three high frequency "IHV-15-500" inductors were selected from Mouser Electronics [14]. Each inductor was 500 μH, so 3 inductors were connected in series to get 1.5mH inductance. The rated DC current rating of each inductor is 15A which is well within range.

4) Output Capacitor Selection [13]:

$$C_{OUT} \geq \frac{V_{OUT} \times D \times T_s}{R \times \Delta V_{OUT}} \tag{2.5}$$

One can re-write equation 2.5 as:

$$C_{OUT} \geq \frac{I_{OUT} \times D}{f_s \times \Delta V_{OUT}}$$

$$C_{OUT} \geq \frac{I_{OUT} \times D}{f_s \times \Delta V_{OUT}} \geq \frac{10 \times 0.55}{10000 \times (0.02 \times 48)} \geq 573\ \mu F$$

To calculate the maximum capacitor value for this converter, D was considered 0.55. The capacitor value directly affects the ripple in the output voltage ΔV_{OUT}, the desired ripple was considered to be less than 2%. Considering the above calculation, the capacitor required, should be at least 573 μF power capacitor for the output. Best practice is to use low ESR capacitors to minimize the ripple in the output voltage, ceramic capacitors are a good choice. As mentioned earlier, this board is a new realization of Texas Instrument (TI) 4-switch DC-DC converter board. Considering that a capacitor bank with 4.7 μF ceramic capacitors, 100 μF and 39 μF hybrid polymer aluminum electrolytic capacitors are used, in total, the output capacitance is roughly 637 μF. The output and input capacitors are the same.

After selecting the inductor and capacitors, now one has the power components of the converter. In order to make the converter work, to get boost and buck operations MOSFETs are selected for high speed switching of inductor current. For that, one need a switching (gate drive) circuitry for turning MOSFET's ON and OFF. One also needs to measure the inductor current and the load current of the system for the feedback loop, as explained in Chapter 3. In Figure 2.10 the circuit of the power converter is shown. To measure the current and voltage values, one will use appropriate measuring sensors V_s and I_s as shown in Figure 2.10. Those sensors output will be sent [15]controller. The controller will process the input signals from the voltage and current sensors, pass them into the PI controller closed loop and then it will generate gating signals for all 4 MOSFETs. The design of the PI controller is explained in Chapter 3. The gating signals from DSP cannot directly be sent directly to the MOSFETs because the DSP output signal is 3.3V to 0V which is not enough to switch the MOSFET ON/OFF.

The MOSFET's that are being used in this project are N-Channel surface mount MOSFETs from "STMicroelectronics" (STH185N10F3-2) [15], with maximum voltage rating of 100 V and maximum current rating of 180A which is well within range for this project. MOSFETs require ideally an external signal of 15V to turn ON and of -8.5V to turn OFF across its gate to source terminals. That signal cannot be provided from the DSP directly. That, and electrical isolation between power and signal, is why one needs gate driver circuits for the MOSFETs. For the gate driver circuit, opto-couplers are being used in this project. An opto-couplers uses an infrared led and a photosensitive sensor for high speed switching, four "HCNW3120" opto-couplers from Avago Technologies [16] are used in this project.

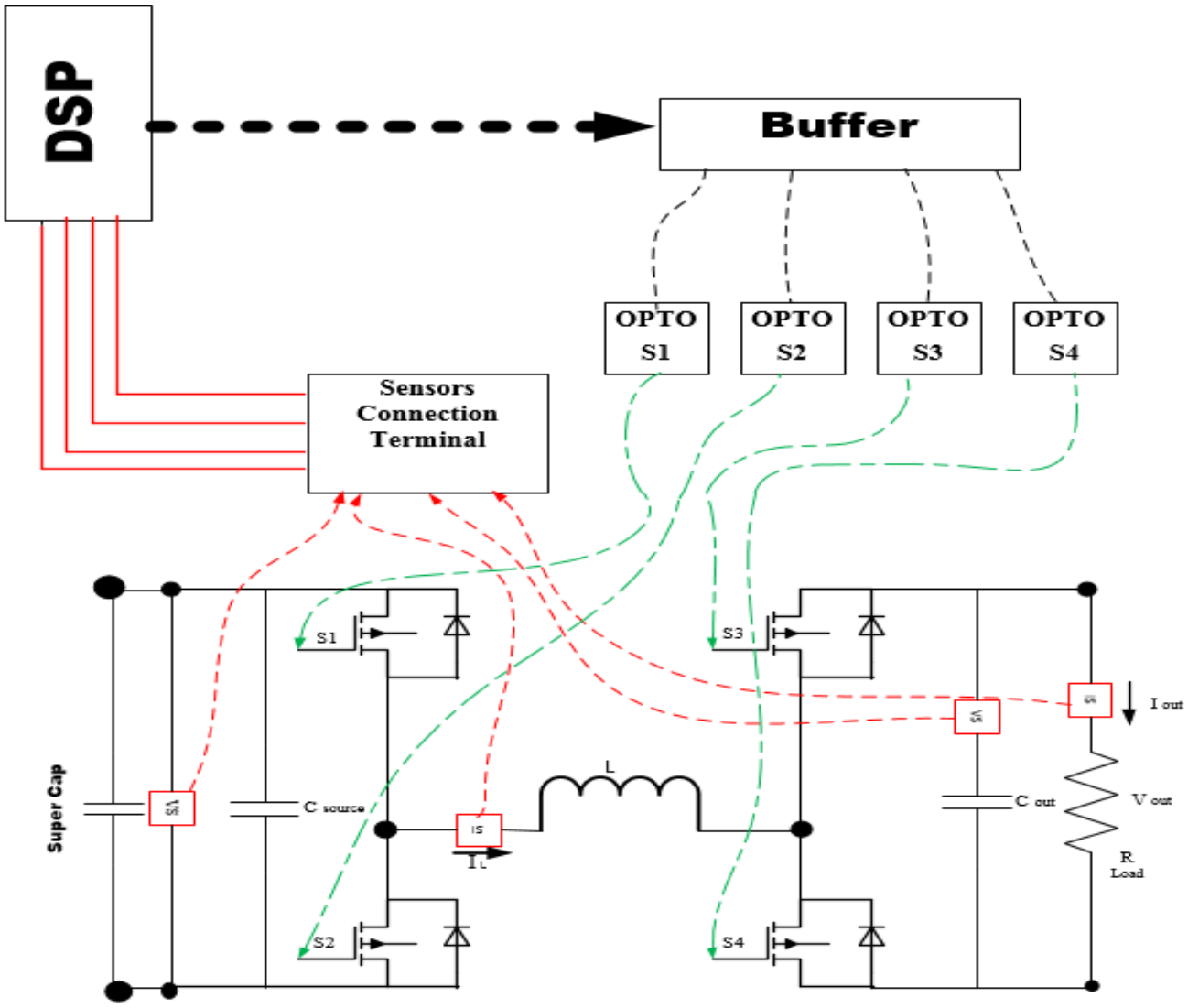

Figure 2.10 Configuration of a DC nanogrid

As mentioned above, the DSP will provide a pulsed 3.3V to 0V output signal to the gate driver circuit. From Figure 2.10, one can see that the PWM output signals from the DSP will go to the buffer first, then to the opto-coupler and then to the MOSFET. In Figure 2.11 the driver circuit for one MOSFET is shown. There, one can see that an external voltage regulator "7805" is used to get 5V and this voltage regulator gets input from an external power supply. One needs a 5V input because the buffer "SN7407" requires 5V input to work. After powering up the buffer, now the signal provided by the DSP can be processed. The buffer gets the PWM signal from the DSP, then the 3.3V to 0V signal from DSP is stepped-up to 5V to 0V at the output of the buffer. The output

signal from the buffer is provided to the anode of the opto-coupler. An external isolated power source, supplies 15V V_{CC} and -8.5V GND to the opto-coupler which is then provided to the MOSFET. The source of each MOSFET is connected to the 0V potential of the isolated power supply. For the four MOSFETs in the converter, four isolated power supplies were required and for that "M57994-1" power supply from POWEREX was used, which includes four isolated power supplies.

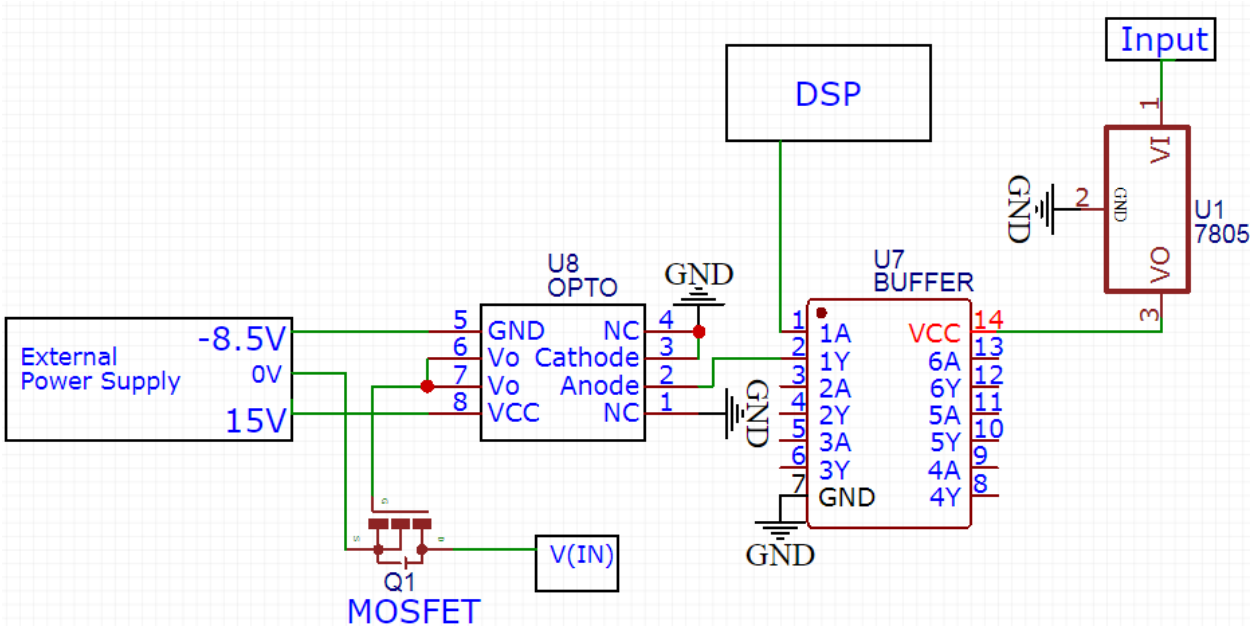

Figure 2.11 Configuration of a DC nanogrid

In Figure 2.10, it is shown that the data from the current and voltage sensors will be sent to the DSP. Inside the DSP, they will be processed by the PI control loops and then the DSP will generate the gating signals. The measurement from the current and voltage sensors are in form of voltage signals, and the DSP can only read up to 3.3V. An analog to digital converter (ADC) was used inside the DSP to convert the analog measurements into usable digital values. Using the appropriate voltage division resistors, the output voltage of the sensors was set to vary from 0V to 3V, so the ADC of the digital controller can read it. The sensor analog output voltage signal is very weak and if one uses long wires to transmit it to the digital controller then it might get contaminated with noise. In order to avoid that, the wires were shielded, to protect the signal from noise as much as possible. In Figure 2.12 one can see the current sensor "LEM 55-P" to measure

the inductor current of the DC-DC converter and the voltage sensor “LEM 20-P” at the input of the converter.

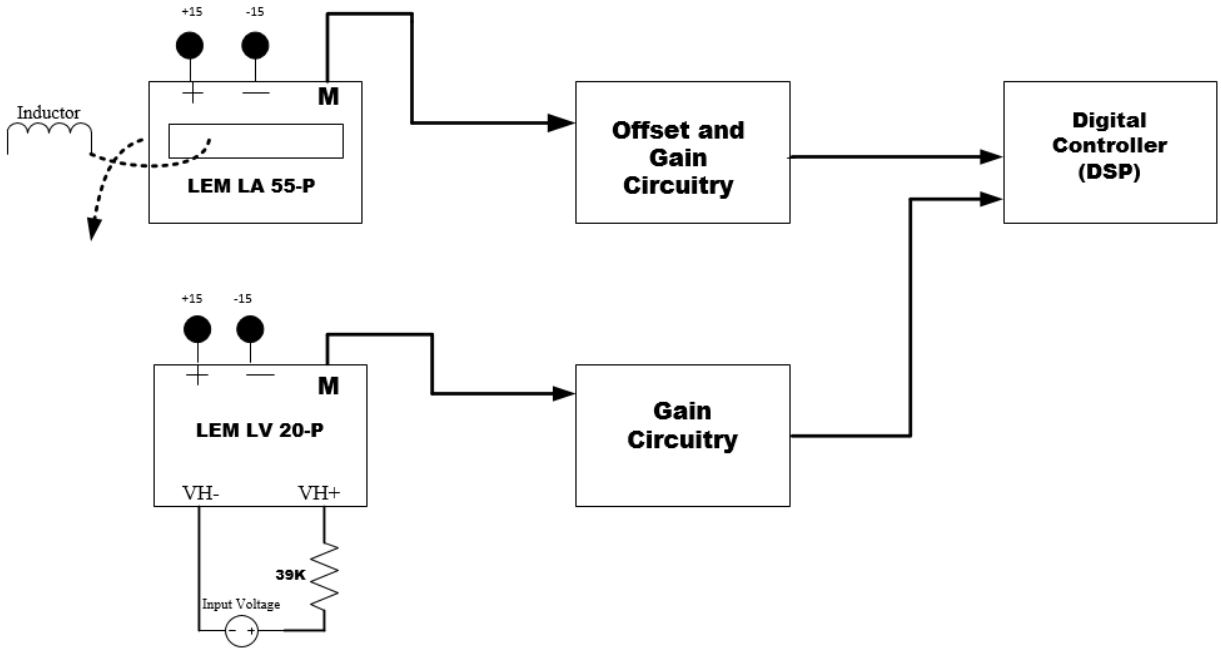

Figure 2.12 Current and Voltage Sensor Block diagram

In this project Hall Effect current sensors “LA 55-P” from LEM are used. The inductor wire will pass through the Hall Effect current sensor, because of the magnetic field of the current passing through the wire, a certain voltage will be generated in the hall sensor which is then processed and sent to the gain amplifier. For measuring the inductor current, one will need to set an offset at the sensor output because one is measuring negative current, as well, for the inductor. By selecting appropriate number of turns of wire, which in case of inductor current is two turns and by calculating the appropriate resistor voltage divider, to provide an offset of 1.5V, one sets the output of the current sensor to vary from 0V to 3V instead of -1.5V to 1.5V. So that it can accurately measure from -10A to 10A inductor currents, in the form of data which is readable for the digital controller. In Figure 2.12 one can see that the current sensor data cannot directly go to the digital controller, which is explained in the paragraph below. The sensor output goes to the op-amp circuit first as shown in Figure 2.13, before it enters the digital controller. A unity gain amplifier circuit is used in this case.

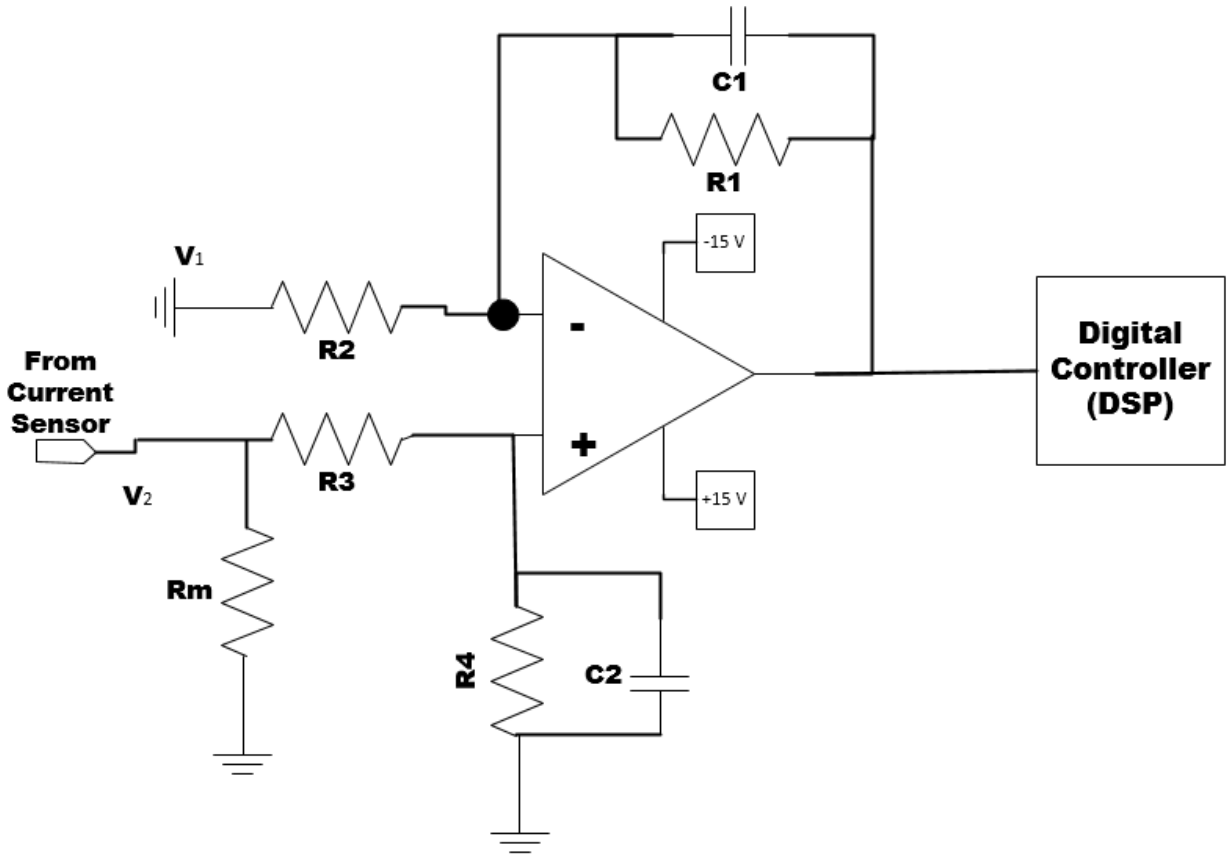

Figure 2.13 Unity gain circuit for current sensor

In order to design an op-amp circuit for unity gain, one has to consider the transfer function of the op-amp circuit:

$$V_{OUT} = \left[\left(\frac{Z_4}{R_3 + Z_4}\right) \times \left(\frac{R_2 + Z_1}{R_2}\right) \times V_2\right] - \frac{Z_1}{R_2} V_1 \qquad (2.5)$$

With ($R_1 = R_4$) and ($R_3 = R_2$) this equation simplifies to

$$V_{OUT} = \left(\frac{Z_1}{R_2}\right)(V_2 - V_1) \qquad (2.6)$$

In the above circuit, one can see that R_1 and R_2 are the same, so if one puts the values in the Eq 2.6, V_{OUT} will be the same as V_{IN}. Which means that after passing through the amplifier circuits, the gain is unity. The reason one needs this unity gain op-amp amplifier is that it does not take any current from the input source, therefore, it completely isolates the input side of the circuit from the output side.

To further explain the need of unity gain op-amp, one knows that an op-amp is a very high input impedance circuit. When a circuit has a very high input impedance, very little current is drawn from the source circuit. In that way, the power of the source is not affected when feeding a high impedance load. Because the source signals are coming from voltage and current sensors, they are very weak and one cannot draw much power from them. By using a unity gain op-amp one can send the regenerated signal of source, with the same voltage level to the controller.

In the case of the current sensor, the resistors and capacitors that are being used in the gain circuitry are given in the Table 2.2.

Table 2.2 Parameters for current sensor measurement and gain offset circuitry

C1 (pF)	C2 (pF)	R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	Rm (Ω)
820	820	39k	39k	39k	39k	100

One can see that by using the same resistors for each node, the op-amp is forced to be in unity gain mode. In Figure 2.13, one can see that capacitor C_1 is connected in parallel with resistor R_1 and capacitor C_2 is connected in parallel with resistor R_4. Capacitors are included in this circuit to cancel high frequency noise in order to get better results.

Table 2.3 Parameters for current sensor measurement and gain offset circuitry

C1 (nF)	C2 (nF)	R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	Rm (Ω)
2.2	2.2	22k	22k	22k	22k	100

For the voltage sensors, the same circuit is used with different values of resistors and capacitors as shown in Table 2.3. Sensors and op-amp require $\pm 15\ V$ supply to operate. Which is provided by an external power supply. In this converter board, two external power supplies are being used, one for powering up the gate drivers and one for the sensors and gain circuit.

In this project, a Texas Instrument DSP "TMS320F2833X" is used as a digital controller. The reason of using this controller is that, it's a modern 32-bit high performance digital controller with

processor speed up to 150MHZ and enhanced peripherals. It also contains 6 channel ADC and has real-time debugging capability which gives the circuit designer benefits of digital control and supports the implementation of high bandwidth and high frequency power converter.

2.3 Summary

This Chapter discusses the circuitry and implementation of the FC Converter for voltage regulation in the DC bus and the design of the DC-DC bi-directional converter in class-C mode. The selection of the inductors, capacitors and implementation of control circuitry was presented. This bi-directional DC-DC converter will be used to interface the super capacitor with the DC bus. It will be used for current control in the DC-bus and to set the minimum and maximum values of voltage, in the super capacitor. Chapter 3 discusses the design and simulation of the bi-directional DC-DC converter and of the FC Converter. Later in Chapter 4, these converters are practically implemented and experimental results are presented.

Chapter 3 System Design and Analysis

Once the design parameters and the components of converter are selected, one can move on to the implementation of system including fuel cell source, storage unit, power converters and load in the DC bus. Before practical implementation, the verification of design and control logic through simulation is essential. This Chapter discusses and compares different configurations to connect the SC to the FC, with a focus on the design and simulation of the control logic for current control in the DC bus and voltage control in the SC.

3.1 Configuration of DC-nanogrid

Different configurations of FC and SC connection are analyzed in [17]. The configuration shown in Figure 3.1 (a), allows a complete discharge of the SC but in this configuration, whole of the current that comes from the FC flows through the SC, vanishing the aim to adapt load and FC dynamics. The cascade connection of the SC is reported in Figure 3.1 (b). Using this configuration one can manage the energy that is stored in the SC independently from the energy that flows from the FC to the load in steady state. The critical disadvantage of this configuration is that it limits the utilization of the energy stored in the SC. Moreover, all the fuel cell energy flows through two converters, causing a reduction in the efficiency of conversion system. Figure 3.1 (c), in this configuration, there is no such issue of limited utilization of the energy stored in the SC. This configuration appears to be a good option, where the SC can be used to support the FC, by supplying and absorbing energy whenever there is a load change, to ensure that the fuel cell is working at the maximum power point.

In this project, the configuration in Figure 3.1 (c) is used. The system which is considered for this research work is shown in Figure 3.2. It consists of a fuel cell as a DC power source feeding a variable load R, through a DC-DC boost converter. The boost converter used in this case is a commercial unidirectional DC-DC converter from Zahn Electronics (FC Converter) as mentioned in the previous chapter.

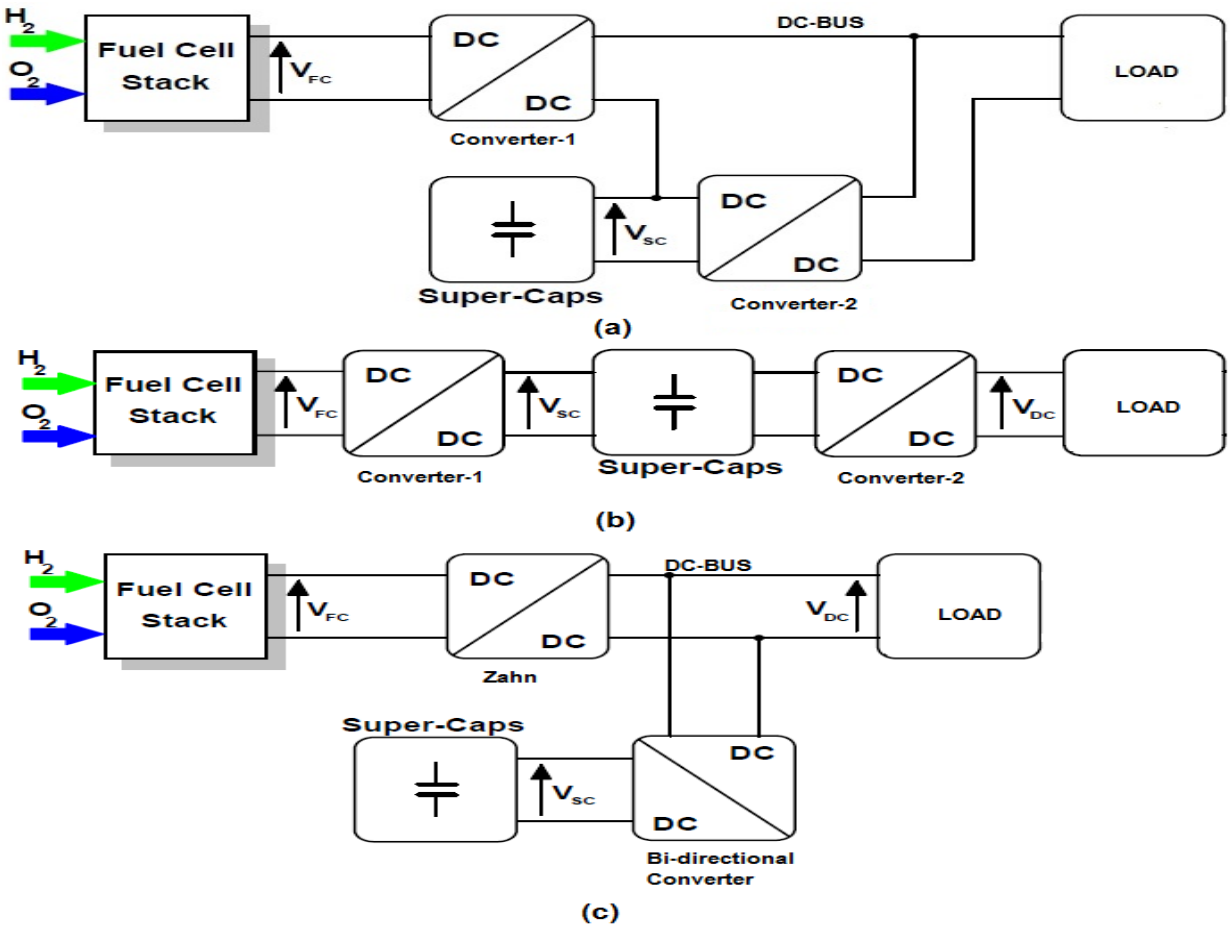

Figure 3.1 Comparison of different FC and SC system configurations

In Figure 3.2, one can see that the DC bus is connected to the super capacitor (energy storage) through a class C bi-directional DC-DC Converter. For a class C bi-directional DC-DC Converter to work, the voltage level of the storage side should be lower than the voltage level of the DC bus. Otherwise, the antiparallel diode D3 conducts and one loses control of the power flow. The class C converter works in two modes: Step-down/buck when the power flows from the DC bus to the SC and the SC charges, and Step-up/boost when the power flows from the SC to the DC bus and the SC discharges. This allows the super capacitor to force the FCS, to operate at maximum power point, provided that one controls the amount of current injected/absorbed by the SC interface from the load DC bus.

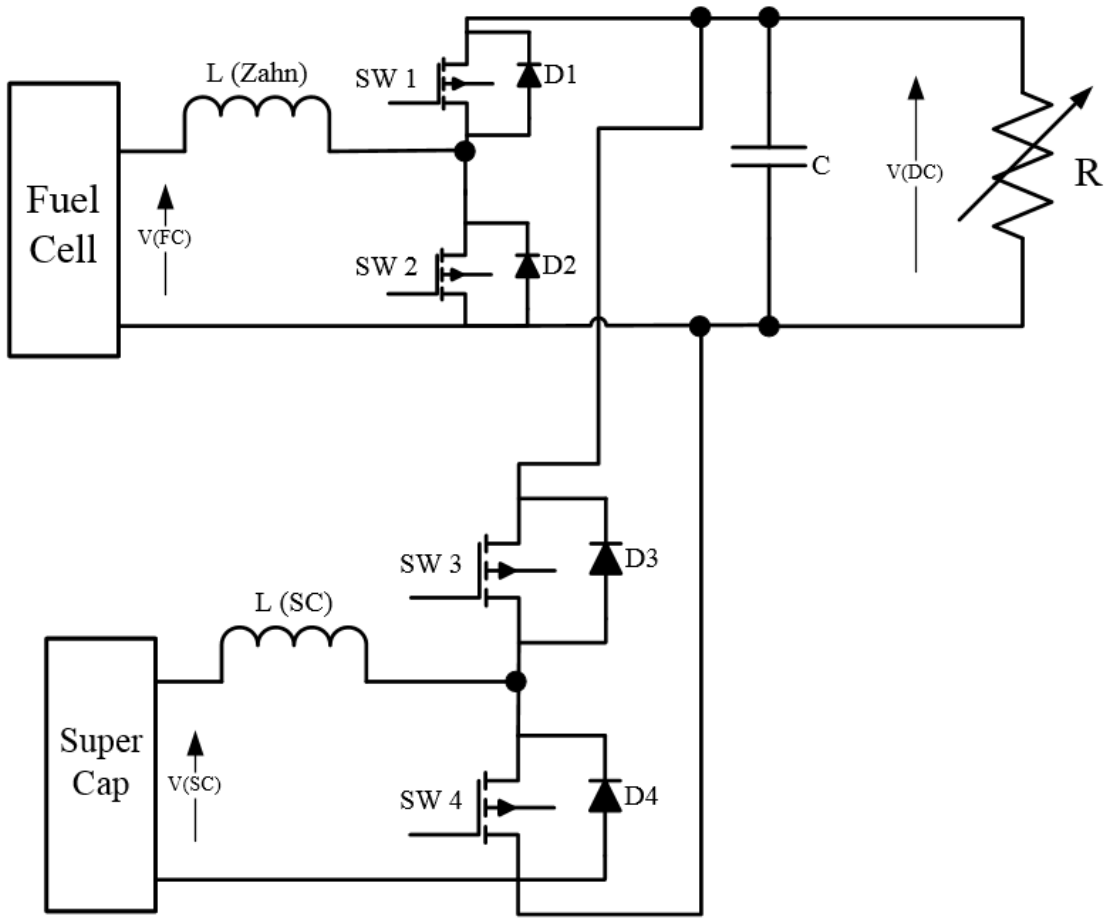

Figure 3.2 Typical Configuration of fuel cell based DC nanogrid.

The main principle behind its action is that it will absorb power, when the load demand becomes smaller than what is required from the FCS, in order to operate at maximum power point. The excess of power will be absorbed by the ESS and the FCS will keep operating at its maximum power point. Conversely, the ESS will supply power when the load demand becomes greater than what is required from the FCS, in order to operate at maximum power point. In this way, FCS will be operating at maximum power point, regardless of the load variation. The super capacitor is connected to the DC bus through a power electronic interface that is controlled using proportional integral (PI) controllers.

3.2 Voltage Regulation in the DC Bus

Voltage in the DC bus should remain constant at 48V in the nanogrid. This project uses a Zahn unidirectional converter (FC Converter) to boost the output voltage of fuel cell to 48V. The FC Converter makes sure that the change of load on the DC bus does not affect the DC bus voltage. In order to keep the DC bus voltage constant, the current supplied by the FCS changes with the changes in the load. The output current of the FCS is kept constant to ensure maximum power point operation of FCS, by connecting ESS with the DC bus (Figure 3.2). There are two power electronics converters with different control schemes in this project. Therefore, before the hardware implementation of this system, one needs to verify the power and control design scheme for the DC nanogrid. For the design verification through simulation, PSIM (Power electronics simulator) has been used in this project. PSIM is one of the most robust power electronics simulator on the market due to its speed, accuracy, intuitive user interface and controllability.

3.2.1 FC Converter schematic

To simulate the DC bus voltage regulation, the converter's power and control circuit are implemented in PSIM. For the FC Converter simulation, the data provided by Zahn Electronics and pre-existing circuit designed by a former student were used. In Figure 3.3, one can see the implementation of the power and control circuitry, of the FC Converter in PSIM. In PSIM, there is no model for a fuel cell yet, therefore in this project, a step voltage source is used to represent the variation of the output voltage of the fuel cell. In the power circuit (represented in red rectangle), the output voltage of the fuel cell (*V_FC)* is the input voltage of FC Converter, as the output of the fuel cell is connected to the input of the FC Converter. Therefore, the current that flows through the input inductor of the Zhan Converter (*I_Input*), is represented as the output current of the fuel cell. The gating signal for MOSFET S1 is a complement of the gating signal that goes to S2. One can see that in the FC Converter, the MOSFETs are connected in class C configuration. In Figure 3.3, case-1 (represented by the green dotted line), when S2 is ON and S1 is OFF. The inductor will charge and the output capacitor (C_out) will discharge across the load. While in case-2 (represented by the red dotted line), when S1 is ON and S2 is OFF. The inductor will discharge across the load.

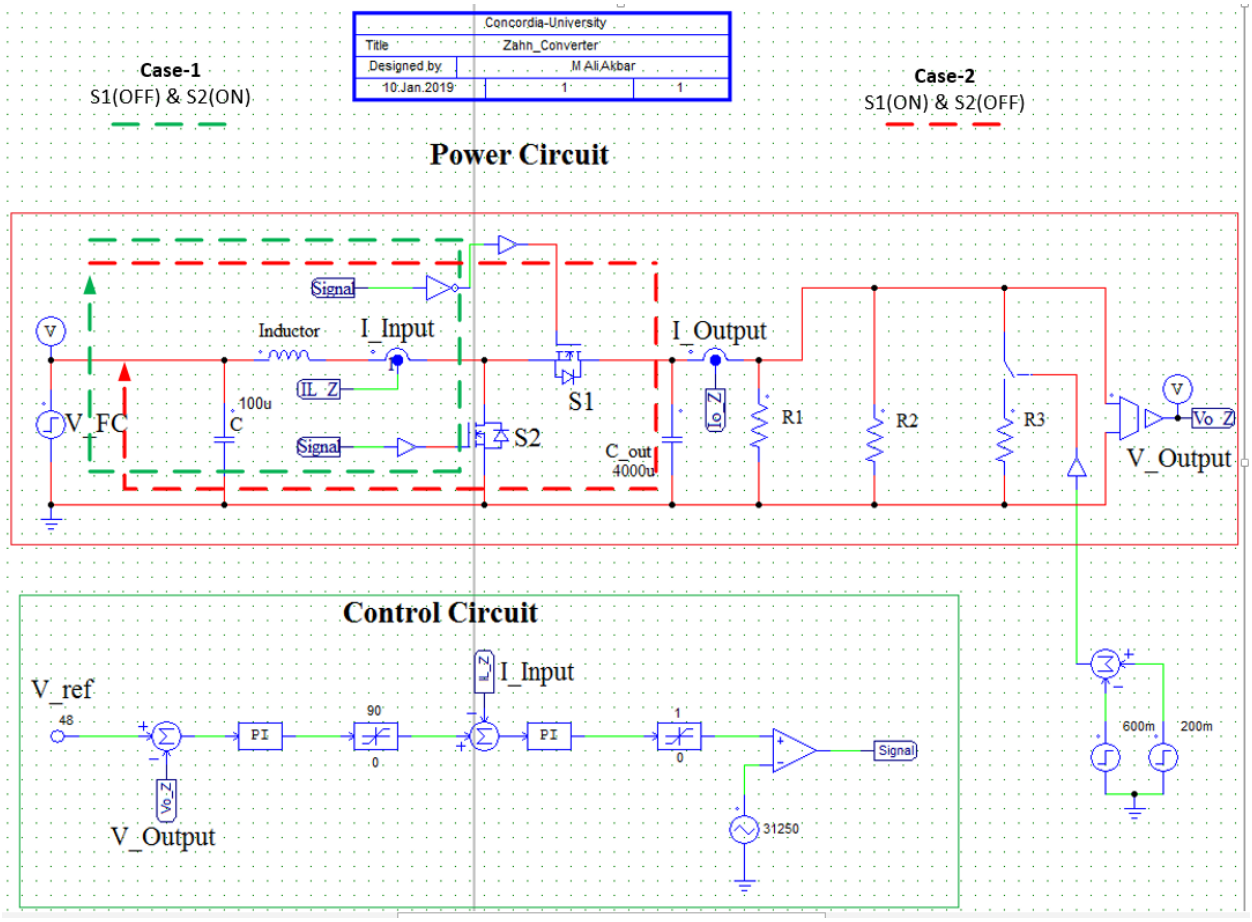

Figure 3.3 FC Converter Power & Control circuit in PSIM

In Figure 3.3, one can also see the control circuit of the FC Converter (represented in the green rectangle) as presented in Chapter 2. There, the output voltage (V_Output) and the reference voltage (V_ref) are compared to generate the error which is then fed to a PI controller. The PI controller provides an output voltage corresponding to the current reference for the inductor. This input reference is then compared with the actual inductor current (I_Input), in order to generate the error in the inductor current. This error is then fed to another PI controller that provides the modulating signal for the pulse width modulator (PWM) that defines the gating signals of the two MOSFETs, at a switching frequency of 31250 Hz. In the control loop, one can see a limiter of 0 to 90. This limiter is placed to make sure that under no circumstance, the current should flow back into the fuel cell.

3.2.2 FC Converter simulation results

Simulation results of FC Converter voltage regulation are presented in Figure 3.4.

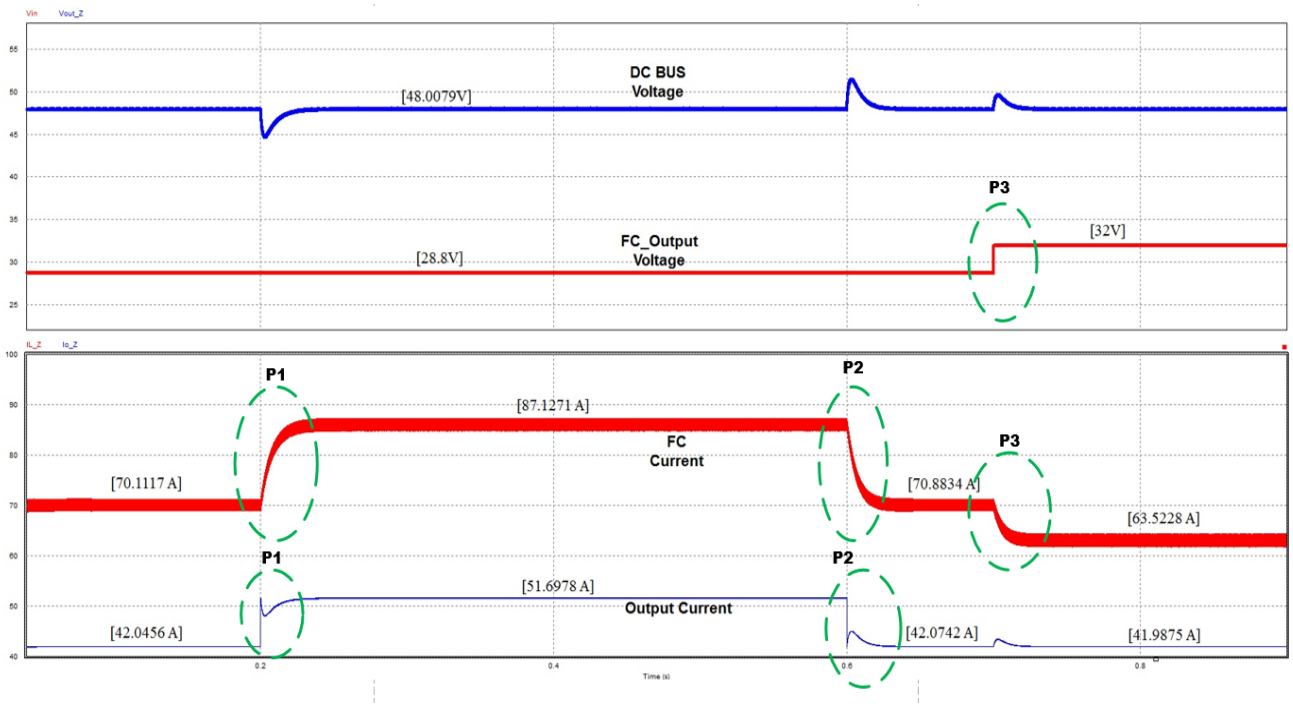

Figure 3.4 FC Converter Simulation Results

At the start of the simulation, one can see that when the output voltage of the fuel cell (input of FC Converter) is at 28.8V, the DC bus voltage (output of FC Converter) is at 48V because of the boost operation. The fuel cell output current (input current of FC Converter) is around 70A while the output current of FC Converter is around 42A. The power at the input is always equal to the power at the output, assuming that the converter is lossless.

- Case-P1: An extra load is added at the output, which results in an increase in the output current, the output current rises to 51.69A. Because of which, the fuel cell current rises to 87.12A and the fuel cell output voltage remains at 28.8V. Following a short dip, the DC bus voltage is regulated at 48V, as a result of the action of the PI controllers.

- Case-P2: The extra load is removed because of which the output current goes back to 42A and the FC current goes back to 70A. Following a short surge, the DC bus voltage returns at 48V.

- Case-P3: The output voltage of the fuel cell rises up to 32V while the output load remains the same. This results in a decrease in the output current of the fuel cell, which decreases to 63.52A. The output current remains at 42A. The DC bus voltage briefly increases but returns to the reference voltage as a result of the action of the PI controllers.

Considering the simulation results, one can say that, the DC bus voltage control loop is effective in regulating the output voltage at 48V in steady state for load and input voltage (voltage of FC) variations. It should be noted that whenever there is a change in the output load, the DC bus current changes, which in turn changes the input current of the FC Converter, driving the output current of fuel cell away from the point of maximum power. Therefore, a supporting unit is needed to keep the output current of the FC Converter constant, thus keeping the fuel cell current constant, in order to make the fuel cell operate at maximum power point.

3.3 Control strategy for the ESS

As a supporting unit, a super capacitor along with a controllable interface is used in this project to keep the FCS current constant. The SC is interfaced with the DC bus through class C bi-directional DC-DC power electronic Converter. In order to make the FCS operate at maximum power point, one needs to controls the amount of current injected/absorbed by the SC interface from the load DC bus. To achieve that, one needs to design a control logic for the class C bi-directional DC-DC Converter. The considered control circuit for the SC converter can be seen in Figure 3.5. I_{ref} is the reference value for the output current of FC Converter, to make the FC operate at its maximum power point.

In Figure 3.5, I_{ref} is compared with the output/load current I_{out}. At stage-2, the difference of I_{ref} and I_{out} is multiplied with the difference of V_{out} and V_{sc}. Due to the charging and discharging, the voltage level of the super capacitor changes. The super capacitor has upper and lower voltage limits, as mentioned in Chapter 1. One needs to make sure that the voltage in the super capacitor should stay within these limits, to ensure that, a voltage control scheme is designed. V_{sc} is compared with the reference voltage for the super capacitor V_{sc_ref} (stage-3). The error is then fed

into a PI controller which produces a reference current for the voltage regulation in the super capacitor.

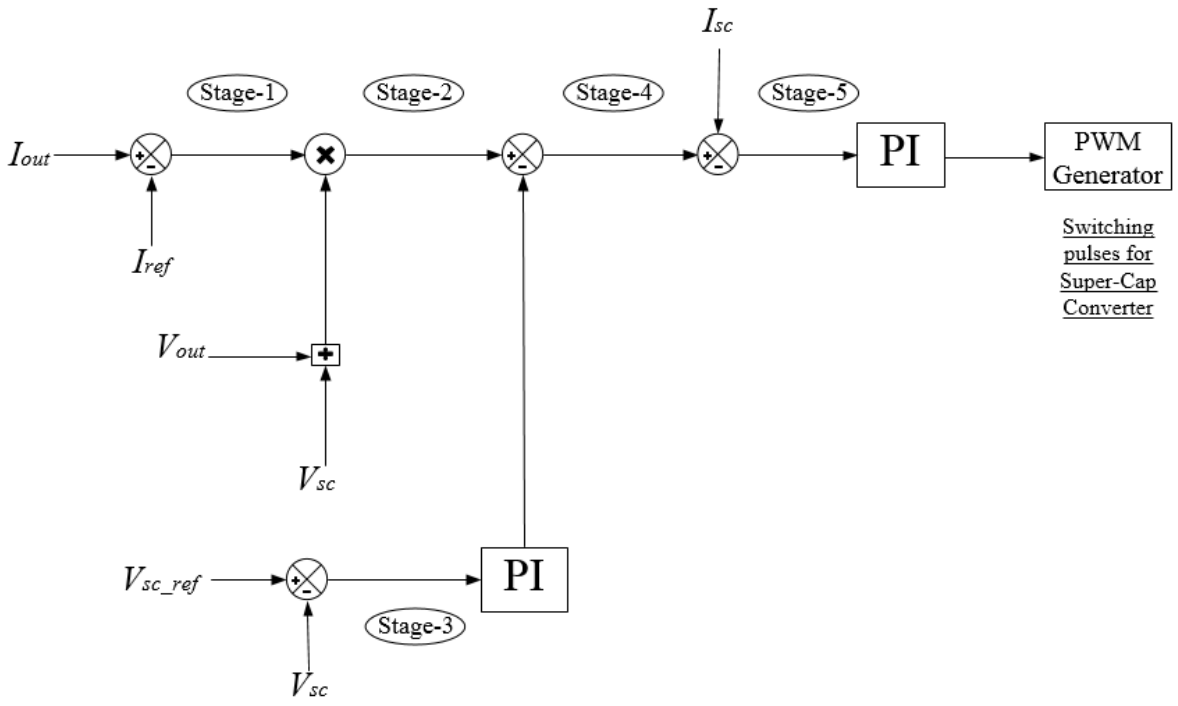

Figure 3.5 Control Scheme for Super capacitor Converter.

This reference current is compared with the result at stage-2, which will result in the final reference current value for the SC current, it is then compared with the actual super capacitor current I_{sc}. The error is then fed to another PI controller that provides the modulating signal for the pulse width modulator (PWM), which defines the gating signals of the two switches of the super capacitor converter.

Using this control scheme, one can make the FCS provide the desired value of current, in order to operate at its maximum power point.

3.4 SC integration with the DC bus

The DC bus voltage will be regulated by FC Converter. To keep the FCS current constant, the ESS is interfaced in the DC bus, as shown in Figure 3.2. ESS needs to absorb and supply current in order to support the FCS and to force the FCS to operate at the maximum power point. When the ESS absorbs current, the voltage level of SC rises as it charges. The super capacitor can store a finite amount of charge, and it cannot charge above its maximum charging limit. In the same way, when the ESS supplies current, the voltage level of SC falls as it discharges. The super capacitor should not be discharged below a minimum discharge limit. Therefore, one needs a voltage control loop, as well, to keep the voltage level of super capacitor within the limit. One needs to design a PI controller for current and voltage control of the super capacitor.

3.4.1 Converter Transfer Function

It can be shown that a class C converter operating in the charging/buck and discharging/boost modes can be represented by the $I_L(s)/D(s)$ transfer function, where I_L is the inductor current and D is the duty cycle of the bottom switch of the class C converter. Therefore, a unified controller can be employed for both modes of operations. It should be noted that the switches of a class C converter operate complementarily and the signal of the PWM comparator is sent to the bottom switch of the converter.

One can derive the transfer function of the “plant” based on the equations which describe the operation of the power electronics converter, used to interface super capacitor to the DC bus. From that, a PI controller for the current control loop will be designed. The derivation of transfer function and design of controller are as follows:

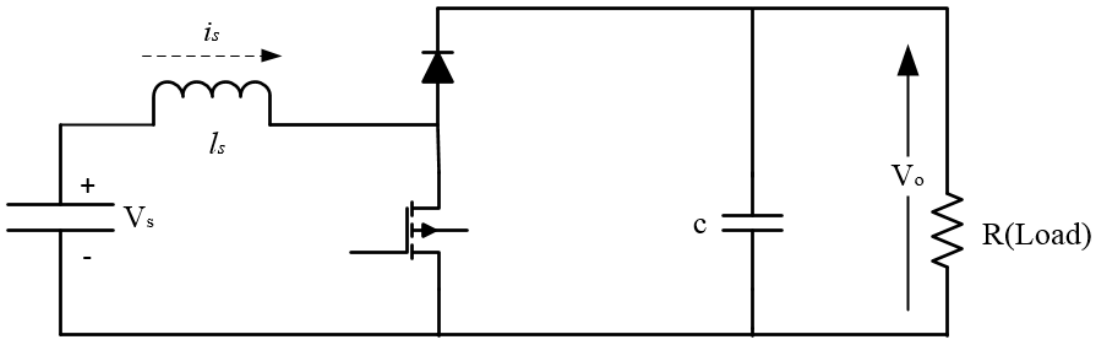

Figure 3.6 Boost Converter with load

- The converter operation can be represented by two different states:

ON state: $t_{on} = DT_s$

$$l_s \frac{di_s}{dt} = V_s \tag{3.1}$$

$$c \frac{dV_o}{dt} = -\frac{V_o}{R} \tag{3.2}$$

OFF state: $t_{off} = (1\text{-}D)Ts$

$$l_s \frac{di_s}{dt} = V_s - V_o \tag{3.3}$$

$$c \frac{dV}{dt} = i_s - \frac{V_o}{R} \tag{3.4}$$

- Averaging the converter's differential equations

$$l_s \frac{di_s}{dt} = V_s - (1 - D)V_o \tag{3.5}$$

$$c \frac{dV_o}{dt} = (1 - D)i_s - \frac{V_o}{R} \tag{3.6}$$

- Introducing small signal perturbations around a base operating point

$$l_s \frac{d(\tilde{\imath}_s + I_s)}{dt} = (V_s + \tilde{v}_s) - (1 - (D + \tilde{d}))(V_o + \tilde{v}_o) \tag{3.7}$$

$$c \frac{d(V_o + \tilde{v}_o)}{dt} = (I_s + \tilde{\imath}_s)(1 - (D + \tilde{d})) - \frac{(V_o + \tilde{v}_o)}{R} \tag{3.8}$$

- The linearized equivalent model can be represented by

$$l_s \frac{d\tilde{\imath}_s(t)}{dt} = \tilde{v}_s(t) - (1 - D)\tilde{v}_o(t) + \tilde{d}V_o \tag{3.9}$$

$$c \frac{d\widetilde{v_o(t)}}{dt} = \tilde{\imath}_s(t)(1 - D) - I_s\widetilde{d(t)} - \frac{\tilde{v}_o(t)}{R} \tag{3.10}$$

- Using Laplace transform

$$L_s i_s(s) = v_s(s) - (1-D)v_o(s) + d(s)V_o \tag{3.11}$$

$$Cv_o(s) = i_s(s)(1-D) - I_s d(s) - \frac{v_o(s)}{R} \tag{3.12}$$

- Finding the transfer function of the plant for the design of inductor current controller

$$G_{p\_is}(s) = \frac{i_s(s)}{d(s)} = \frac{V_o C s + \frac{V_o}{R} + (1-D)I_s}{CL_s s^2 + \frac{L_s}{R}s + (1-D)^2} \tag{3.13}$$

With the transfer function, one can calculate the proportional and integral constants of the PI controller.

3.4.2 Current control loop for the super capacitor (SC)

As discussed in Chapter 2, the switching frequency of converter is 10 kHz (f_s). In order to design the current control loop, the bandwidth of the control loop is chosen by $f_x = \frac{f_s}{6}$. The crossover frequency of the converter becomes:

$$\omega_x = 2\pi f_x = 10471.9 \ {}^{rad}/_{sec}$$

In order to design the controller, the phase margin (PM) can be selected as 60°. In Chapter 2, the values of inductor and capacitor were calculated.

The basic parameters of the SC converter are shown in Table 3.1

Table 3.1 Nominal SC Converter Parameters

V_o	I_s	V_s	L_s	D_s	R	C
48V	2.25A	32V	1.5mH	0.4	32Ω	637µF

At the crossover frequency ($s = j\omega_x$) Eq 3.13 becomes:

$$G_{p\_is}(j\omega_x) = \frac{i_s(j\omega_x)}{d(j\omega_x)} = \frac{2.85 + 320.06j}{-105.15 + 0.4899j} \tag{3.14}$$

To design a PI controller for the SC inductor current control, one needs to compute the values of gain and phase at the crossover frequency. From Eq 3.14, the gain and phase are computed as:

$$|G_{p\_is}(j\omega_x)| = 9.66dB$$

$$\varphi_{p\_is} = 89.93^{o}$$

In general, to minimize the steady state error, the loop gain should be high at the low frequency range. On the other hand, the loop gain should be low at high frequency range, in order to limit/attenuate the switching harmonics. In order to obtain a satisfactory phase margin, the gain slope should be -20 dB/dec around the crossover frequency. As shown in Figure 3.7, the Bode plot of the plant G_{p_is} presents a constant gain at the low frequency range. In this project PI "type I" is used.

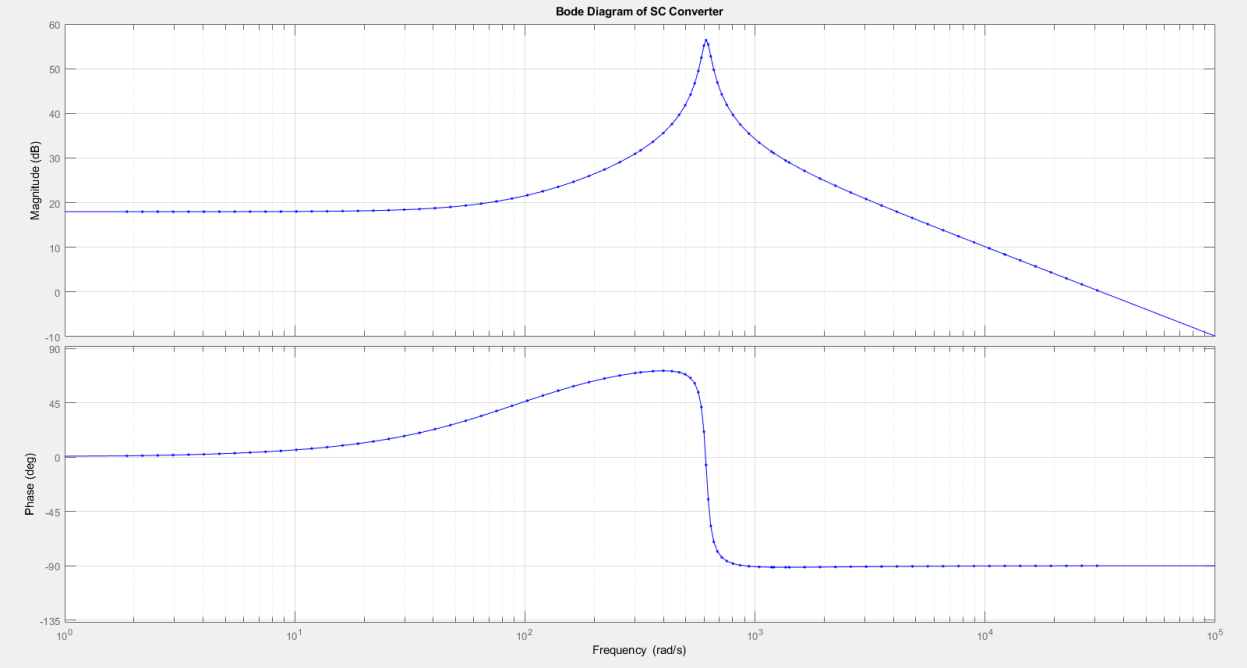

Figure 3.7 Bode plot of the plant for the design of current loop for the SC

The transfer function of the PI "type I" is given:

$$G_{pi\_is}(s) = K_p + \frac{K_i}{s} \tag{3.15}$$

The parameters are computed as follows:

$$|G_{pi\_is}(j\omega_x)| = \frac{1}{|G_{p\_is}(j\omega_x)|} = -9.66dB = 0.328 \tag{3.16}$$

From Eq 3.16:

$$|G_{pi\_is}(j\omega_x)| = \sqrt{(K_p)^2 + \left(\frac{K_i}{s}\right)^2} \tag{3.17}$$

$$(K_p)^2 + \left(\frac{K_i}{s}\right)^2 = 0.1075$$

Phase of PI controller:

$$\varphi_{pi} = -180^o + PM - \varphi_{p\_is} \tag{3.18}$$

$$\varphi_{pi} = -180^o + 60^o - 89.75^o$$

$$\varphi_{pi} = -209.75^o$$

Computing time constant:

$$\tau = \frac{\tan(\varphi_{pi} + 90)}{\omega_x} \tag{3.19}$$

$$\tau = \frac{\tan(-209.75 + 90)}{10471.9}$$

$$\tau = 167\ \mu s$$

$$K_i = \frac{K_p}{\tau} \tag{3.20}$$

After calculation:

$$\tau = 167\ \mu s \quad , \quad K_p = 0.284$$

Figure 3.8, illustrates the Bode plot of the transfer function of the plant (G_{pi_is}) and the loop transfer function (LTF), with the designed PI controller. One can see that, with the designed PI (type I) controller, the design specs ($\omega_x = 2\pi f_x = 10471.9\ {}^{rad}/_{sec}\ and\ PM = 60°$) were accomplished.

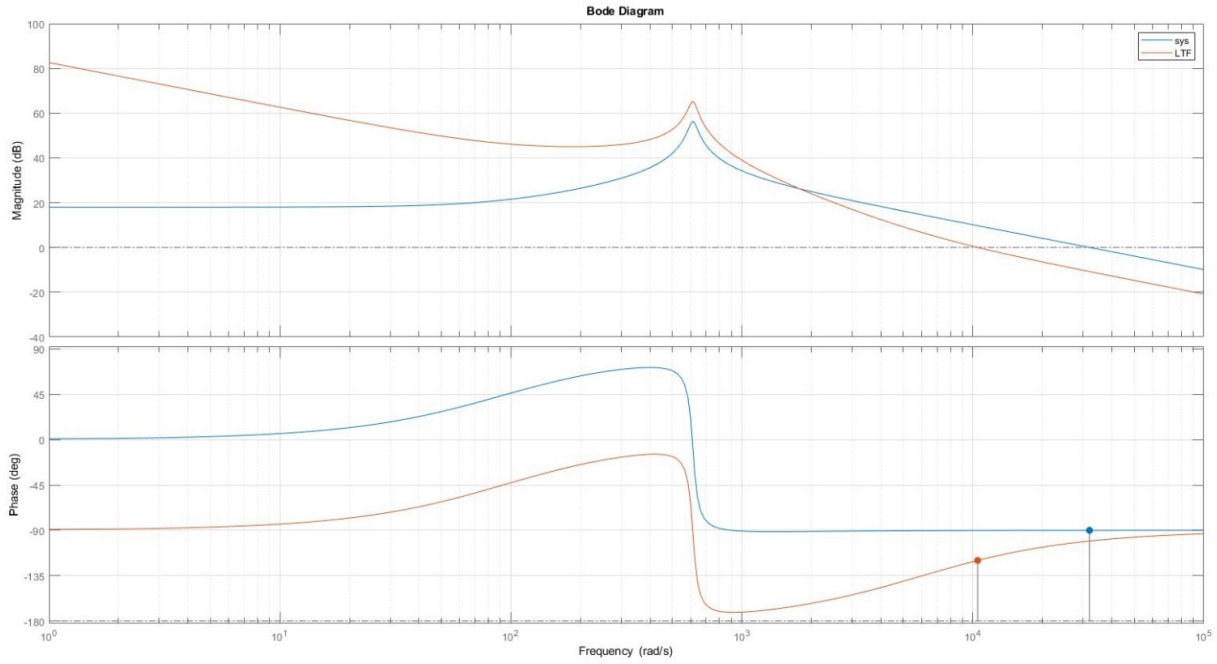

Figure 3.8 Bode plot of the plant (G_{pi_is}) and LTF of the SC

Once the proportional and integral coefficients are computed, one can now substitute them in the controller transfer function. In Figure 3.9, one can see the block diagram of current control loop for the super capacitor. Where I_{sc_ref} is the reference value of current as explained previously. G_{pi_is} is the PI controller, G_{p_is} is the plant and gain ($1/H_{p\_is}$).

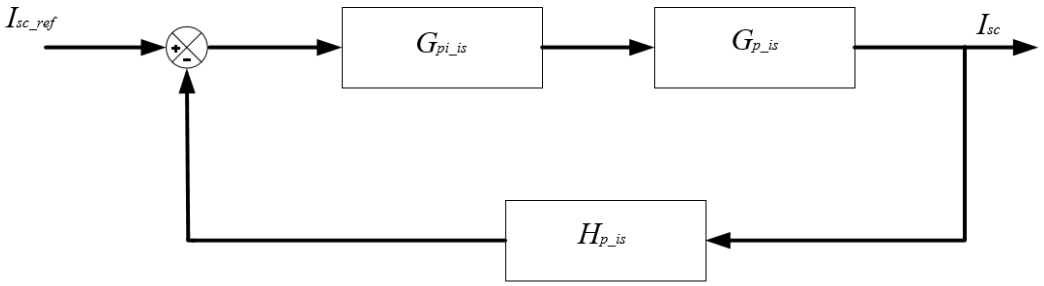

Figure 3.9 Block diagram of the SC current control loop

3.4.3 Voltage control loop of SC

In order to keep the voltage of the super capacitor within the upper and lower voltage limits as explained previously, one needs a voltage regulation loop for the ESS. For the choice of the reference value, one can select a value that allows the SC to support the FCS by supplying a given amount of energy before reaching its minimum voltage limit, and absorb the same amount of energy before reaching its maximum voltage limit. One can set the reference value for SC voltage to 36V, assuming the maximum voltage limit for the SC is 48V and the minimum voltage limit for the SC is 24V, so that the SC can absorb and supply a given amount of energy before reaching its voltage limits. In this project, for the simulations and experimentation, the reference value of the SC voltage is set to 32V. SC's main task is to supply and absorb current, in order to support the FCS. Therefore, this control loop should be slow as compared to the current control loop, attempting to charge/discharge the SC with low values of currents, which comes from the FCS.

Figure 3.10, shows the block diagram of the SC voltage control loop. It includes the inner inductor current (I_{sc}) control loop, where a PI-type-I (G_{pi_is}) controller is used, and a duty-cycle to inductor current transfer function (G_{p_is}), which was designed in the previous Section. For the SC voltage regulation, the SC voltage is measured and compared with the reference value (V_{sc_ref}). The error is then passed through a low bandwidth PI controller (G_{pi_vs}), it produces a slow varying current required to bring the voltage of SC to the reference value. This current is then added to the fast (I_{sc_ref}) reference current for the SC inductor, as discussed previously, to provide the fast varying current component for the ESS. For the design of the SC voltage loop, one needs to know

how the inductor current of the SC affects the voltage in the SC. This relation, transfer function (G_{p_vs}), can be obtained from the power converter and SC shown in Figure 3.6.

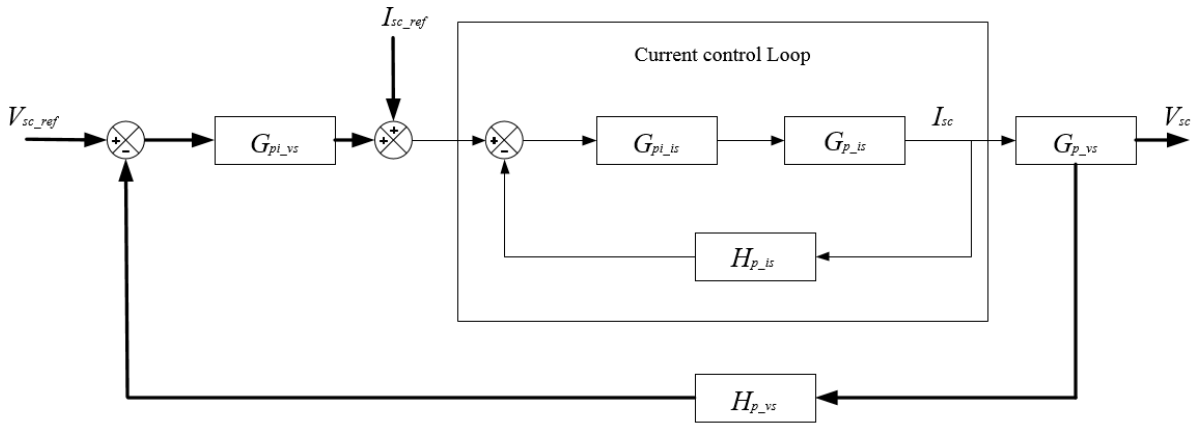

Figure 3.10 Block diagram of the SC voltage control loop.

The closed loop controller for the SC voltage regulation is based on the SC current and the SC voltage.

Calculation of the transfer function (G_{p_is}):

- State equation

$$C\frac{dv_{sc}}{dt} = i_{sc} \tag{3.21}$$

- Using Laplace transform

$$Cs\ v_{sc}(s) = i_{sc}(s) \tag{3.22}$$

- Transfer function

$$G_{p_{vs}(s)} = \frac{v_{sc}(s)}{i_{sc}(s)} = \frac{1}{Cs} \tag{3.23}$$

The voltage control loop for the ESS should be slower than the inner current loop of SC. Therefore, the bandwidth of the voltage control loop for ESS is chosen as 10% f_x, where f_x is the BW of the current control loop of SC, and the phase margin PM = 60°. For this case, a PI-type-I controller can be selected.

The parameters of the designed controller are computed using the approach described in previous Section, are shown in Table 3.2.

Table 3.2 Parameter of the PI controller for the SC voltage control loop

C	K_p	τ	K_i
0.5F	0.67	1.10s	0.61

3.5 Current control scheme for the SC

The main task in this project is to make the FCS operate at the maximum power point. Therefore, one needs to control the output current of the fuel cell. As in Chapter1 Figure 1.3, one can see that the output current of fuel cell should be 70A, for it to operate at the maximum power point. In Figure 3.11, one can see a detailed block diagram of the current control scheme of the SC converter. When the fuel cell is operating at 70A, the current in the DC bus would be different because of the boost (FC Converter) conversion. Therefore, one can come up with a reference value (I_{ref}) for the FC Converter output current in the DC bus, which would ensure the maximum power point operation of the fuel cell. In the control scheme, one can see that the output/load current (I_{out}) and the reference value (I_{ref}) for the FC Converter output current, are compared. This result is then multiplied with the result that one gets by dividing the super capacitor voltage level (V_{sc}) with the DC bus voltage level (V_{out}). This will provide the (inductor) current reference for the

super capacitor converter. By comparing this current reference with the actual current in the super capacitor, one can get the error value (e). This error value is then fed to the PI controller. The PI controller for the current control loop was designed in the previous section, where the values of proportional (K_p) and integral (K_i) components of PI controller were computed. This PI controller will provide the modulating signal for the pulse width modulation (PWM) block that generates the gating signals for the gate driver circuits, which switch the MOSFETs accordingly.

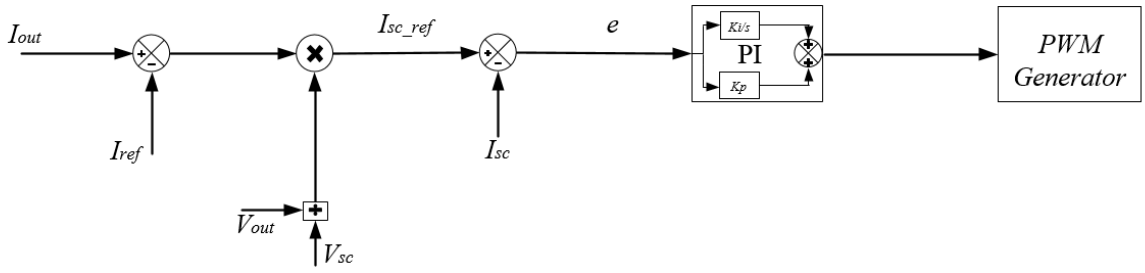

Figure 3.11 Current control scheme for SC Converter

The implementation of the power converter and control scheme for the super capacitor current (I_{sc}), in PSIM, is shown in Figure 3.12. One can see the power circuit which contains a sub circuit of FC Converter as discussed previously. The FC Converter will boost the output voltage of the fuel cell and regulate the voltage at 48V in the DC bus. One can also see the SC converter. Which will boost the super capacitor voltage and supply/absorb current in the DC bus whenever required. One can see that there are two MOSFETs, S1 and S2. Where S1 is the complement of S2. Therefore, when S2 is ON and S1 is OFF (Case-2), the inductor will charge and the current in the inductor (I_{sc}) rises. On the other hand, when S1 is ON and S2 is OFF, the power is supplied to the load and the inductor discharges (Case-1). There are four different resistive loads, which are turned on and off for testing the performance of the control loops. V_FC in the circuit represents the fuel cell output voltage, which is a kept at 28.8V for this simulation. V_out is the DC bus voltage. V_sc is the voltage level of the super capacitor. I_out is the total current required by the load.

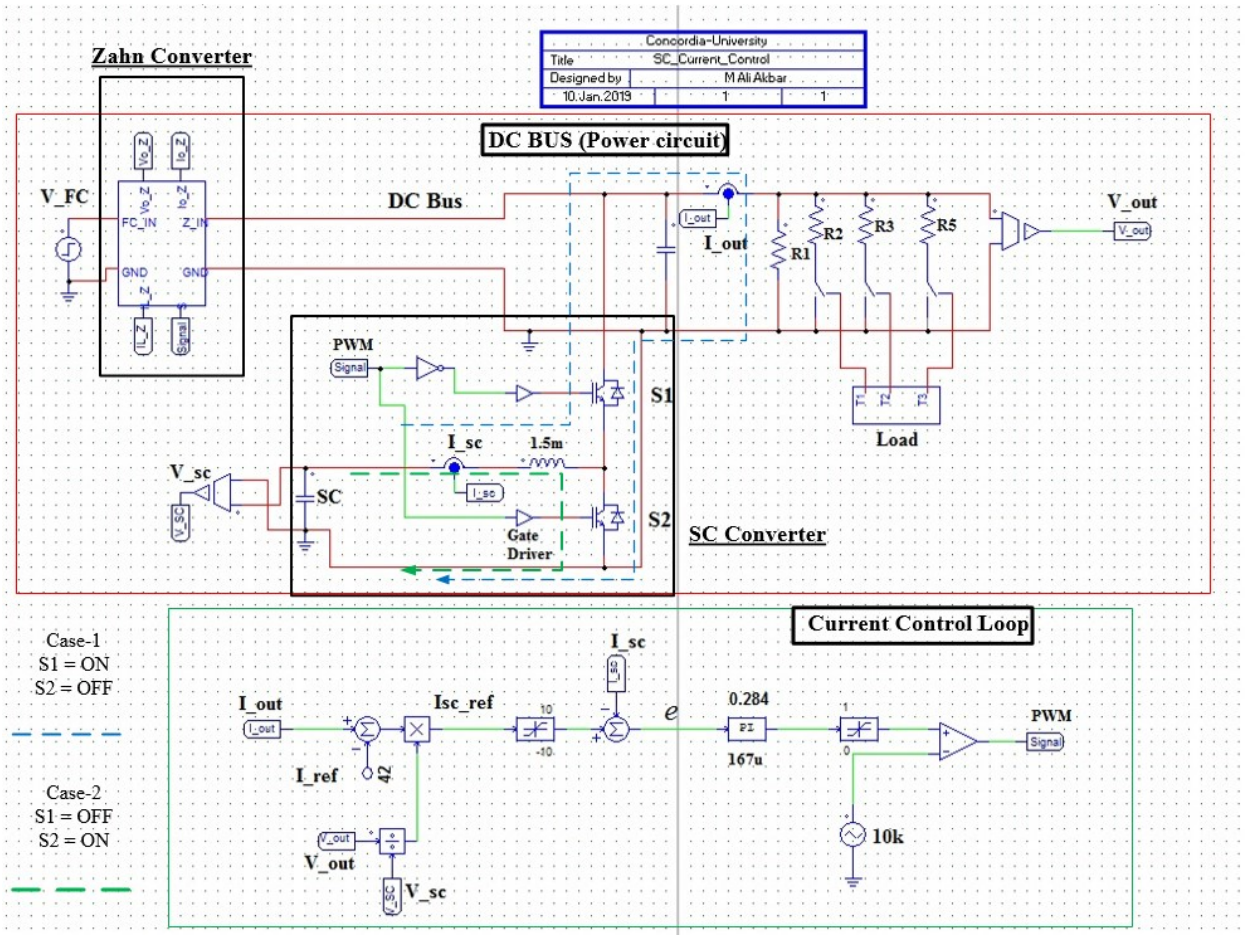

Figure 3.12 Current control scheme for SC Converter

One can also see the current control loop in Figure 3.12. For this simulation the fuel cell output voltage is kept at 28.8V and the fuel cell output current will be 70A (maximum power point), at the start of the test.

As one knows:

$$\mathrm{P(in)} = \mathrm{P(out)}$$

$$\mathrm{V\_FC.I\_FC} = \mathrm{V\_out.I\_out}$$

$$\mathrm{I\_out} = \frac{28.8 \times 70}{48} = 42\mathrm{A}$$

$$I\_ref = 42A$$

In order to keep the fuel cell output current at 70A the reference current for the output of FC Converter (I_ref) is set to 42A. As explained above, the super capacitor reference current (Isc_ref) passes through a limiter and then compared to the actual super capacitor current (I_sc). The limiter is there to limit the SC current in case of short circuit, so that the SC (I_sc) current should not go above 10A in any case.

In the control loop, after the PI controller, there is a limiter, it limits the modulating signal to keep the PWM in the linear region. The comparator compares the triangular wave signal at 10 kHz (switching frequency of the converter) with the output of PI to generate, PWM signal for the MOSFET's gate driver circuits. PWM signal for MOSFET S1, passes through a NOT gate. To make sure that whenever S1 is ON, S2 will stay OFF. The proportional and integral constants values were computed in the previous section.

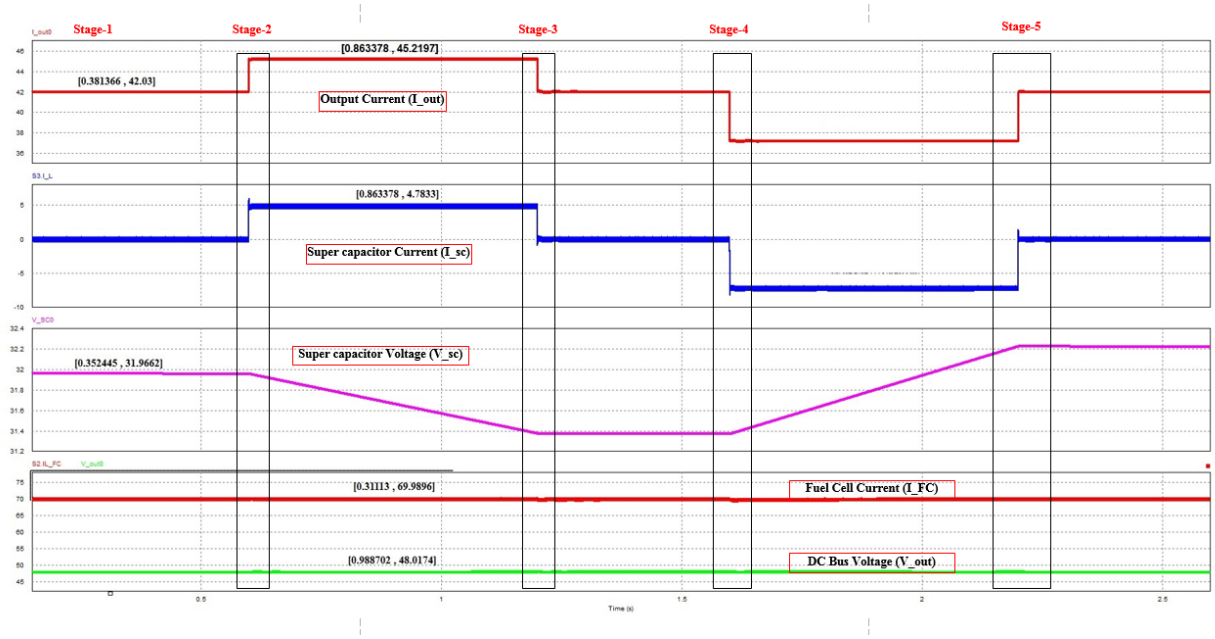

Figure 3.13 Simulation results of Current control scheme for SC Converter

Figure 3.13 shows the simulation results of the current control scheme. The explanation of different stages of the simulation results is provided:

- Initially at Stage-1, one can see that the DC bus voltage is regulated at 48V by the FC Converter. The fuel cell current is 70A (maximum power point). The output/load current (I_out) is at 42A. As one knows that the reference current for the output of FC Converter (I_ref) is also 42A. That is why at stage-1, the ESS is not supplying or absorbing any current because of which the super capacitor current (I_sc) is at 0A and the super capacitor voltage is (V_sc) is at 32V.

- At Stage-2, more load is added. The output/load current (I_out) increases to 45.2A, which is more than the reference value (I_ref) for the output of FC Converter, without a current control loop, this can result in an increase in the fuel cell output current. Due to the current control scheme, the ESS supplies the rest of the required current that is why the super capacitor current rises to 4.8A.

  Current supplied by the SC at Stage-2:

$$I\_sc = \frac{V\_out \times (I\_out - I\_ref)}{V\_sc}$$

$$I_{sc} = \frac{48 \times (45.2 - 42)}{32} = 4.8A$$

  One can see that as the ESS supplies the current to the DC bus, the voltage of the super capacitor (V_sc) decreases due to discharging. As the ESS is supplying the extra current, because of which the fuel cell current (I_FC) stays at 70A.

- At Stage-3, the extra load is removed. The output/load current (I_out) goes back to 42A. Because of which the super capacitor current (I_sc) goes to 0A again, as the output/load current is at the reference value (I_ref) for the output of FC Converter and the error (e) is "zero". One can see that the super capacitor voltage (V_sc) has settled at a lower voltage level of 31.4V now.

- At Stage-4, some of the load is removed from the DC bus. The output/load current becomes less than the reference value (I_ref) for the output of FC Converter, due to the change in load. In order to compensate, the ESS absorbs the extra current, because of which the fuel

cell will keep supplying 70A. Therefore, the fuel cell current (I_FC) still remained the same. The super capacitor current (I_sc) at this stage becomes negative. At stage-4, the ESS is absorbing power. That is why the voltage of the super capacitor is rising.

- At Stage-5, the load is added again, in order to make the output/load current (I_out) 42A. Because of the control scheme the super capacitor current (I_sc) goes to 0A again, as the output current is at reference value (I_ref) for the output of FC Converter. As from Stage-4 the super capacitor voltage was rising, therefore, at Stage-5 the super capacitor voltage settles at a higher voltage level of 32.2V.

In Figure 3.13, one can see that in all five stages of the test, the fuel cell current (I_FC) remained at 70A (maximum power point). Whenever there is a change in load, the ESS current increases or decreases, in order to force the FCS to keep operating at its maximum power point. The output voltage is regulated at 48V by FC Converter for this test.

For hardware implementation in the lab, the reference current for the output of FC Converter (I_ref) for the test is kept 2A. Before the hardware implementation, simulations are required in PSIM to verify the control scheme. In Figure 3.14, one can see the current control loop of the ESS, used for hardware implementation and testing. The control scheme is same as the previous one and the only difference is that the reference current for the output of FC Converter (I_ref) is kept at 2A instead of 42A.

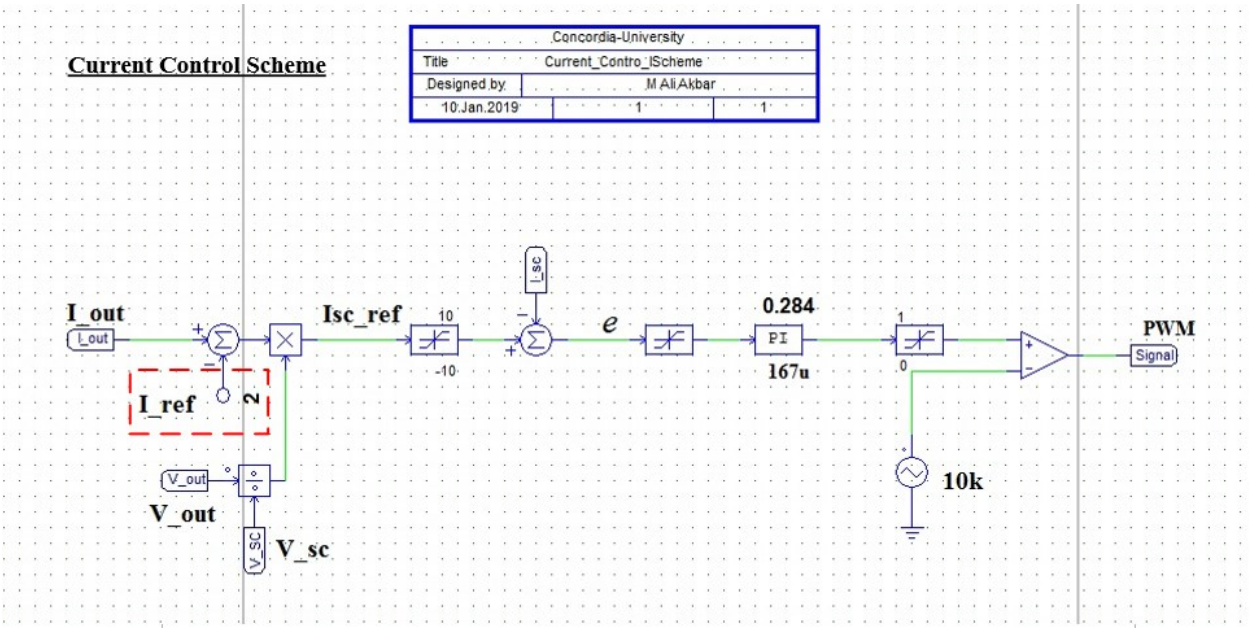

Figure 3.14 Current Control Scheme of SC Converter (For simulation and practical implementation)

3.6 Voltage regulation in the SC

The current control loop of ESS, forces the FCS to operate at maximum power point, by absorbing and supplying current from the ESS. In Figure 3.13, one can see that when the ESS absorbs energy, the voltage level of SC rises and the voltage level of SC decreases, when it supplies energy. A voltage control loops is required for the SC, to keep the voltage level of the SC within the maximum and minimum voltage limits. One should consider three cases to design a voltage control loop.

- First, if the supercapacitor keeps absorbing energy due to the current control scheme, the voltage level of the SC may exceed the maximum voltage limit of the SC. The voltage level of SC should not go above the maximum voltage limit.
- Second, when the ESS is supplying energy, the voltage level of the SC decreases, it should not go below the minimum voltage limit of the SC.
- Third, the SC should have enough energy stored in it, that it can support the FCS whenever required (Whenever extra load is added or removed).

In Figure 3.15, the voltage regulation scheme for the ESS is presented. One can see that the reference current for the SC (for current control loop as shown in Figure 3.14) is generated at Stage-1 (red rectangle). For voltage regulation in the SC, the result of the PI control loop will be added to the Stage-1 value, to provide a reference value for the SC current. In the voltage regulation loop, one can see that there is a block (SC Voltage Reference Selection), which selects the reference value for the PI controller (PI-v1). This block has two inputs, SC upper voltage limit (Vsc_UL) and SC lower voltage limit (Vsc_LL). This block provides a voltage reference (either Vsc_UL or Vsc_LL) for the SC. The result is provided to the PI controller (PI-v1). The base voltage reference of SC (Vsc_ref) or the voltage level which the super capacitor should maintain in order to support the FCS, is set to 32V as mentioned previously. In Figure 3.15, one can see that the base voltage reference (Vsc_ref) is compared with the SC voltage (Vsc) and the results is provided to the PI controller (PI-v2).

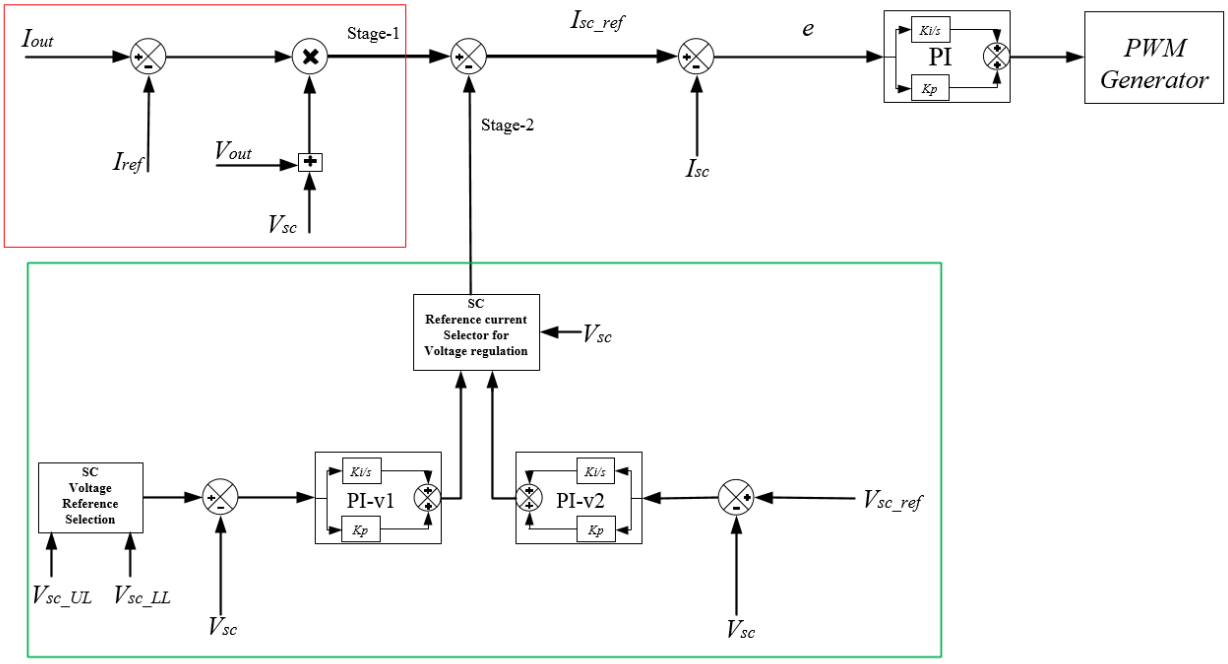

Figure 3.15 Voltage regulation scheme for SC Converter

Both the PI controllers will provide the reference current for the voltage regulation in the SC. The PI controller (PI-v2) to maintain the SC voltage at the base voltage reference, is slower as compared to the PI controller (PI-v1). The PI controller (PI-v1) is faster than the PI-controller (PI-v2) because, whenever the SC voltage reaches the upper voltage limit (Vsc_UL), the SC should

not charge anymore. Similarly, whenever the SC voltage reaches the lower voltage limit (Vsc_LL), the SC should not discharge anymore. In any other case, the slow PI controller (PI-v2) should provide the reference current to maintain the voltage level of SC at its base voltage reference (Vsc_ref). The block (SC Reference Current Selector for Voltage regulation), is where the super capacitor voltage (Vsc) is measured, depending upon which, it selects one of the two PI controllers outputs, for the voltage regulation of SC. Which is explained in detail below. The reference current value at Stage-2 is compared to the value at Stage-1, which in turns provides the reference value (Isc_ref) for SC current. This reference value is then compared with the actual value of the super capacitor current (Isc) that results in the error value (*e*) for the PI controller.

For the simulation, the upper and lower voltage limits of the super capacitor are chosen to limit the run time of the test. The voltage limits of SC are given in Table 3.3.

Table 3.3 Voltage limits of Super capacitor

Vsc_UL	Vsc_LL	Vsc_ref
33V	31V	32V

3.6.1 Lower voltage limit

As mentioned previously, the lower voltage limits for the super capacitor is 31V for simulation. When extra load is added to the DC bus, the ESS will keep the fuel cell current at the 3.3A (maximum power point), by supplying energy to the DC bus. The voltage in the super capacitor will keep on reducing as it discharges. Once the voltage reached the lower voltage limit, the super capacitor will stop discharging.

In Figure 3.16, one can see the lower voltage limit indicator of the SC. The measured output current (I_out) is compared with the Output current upper limit (I_out_UL), which is set at 2.1A (It is to indicate that, the output/load current is higher than 2A).

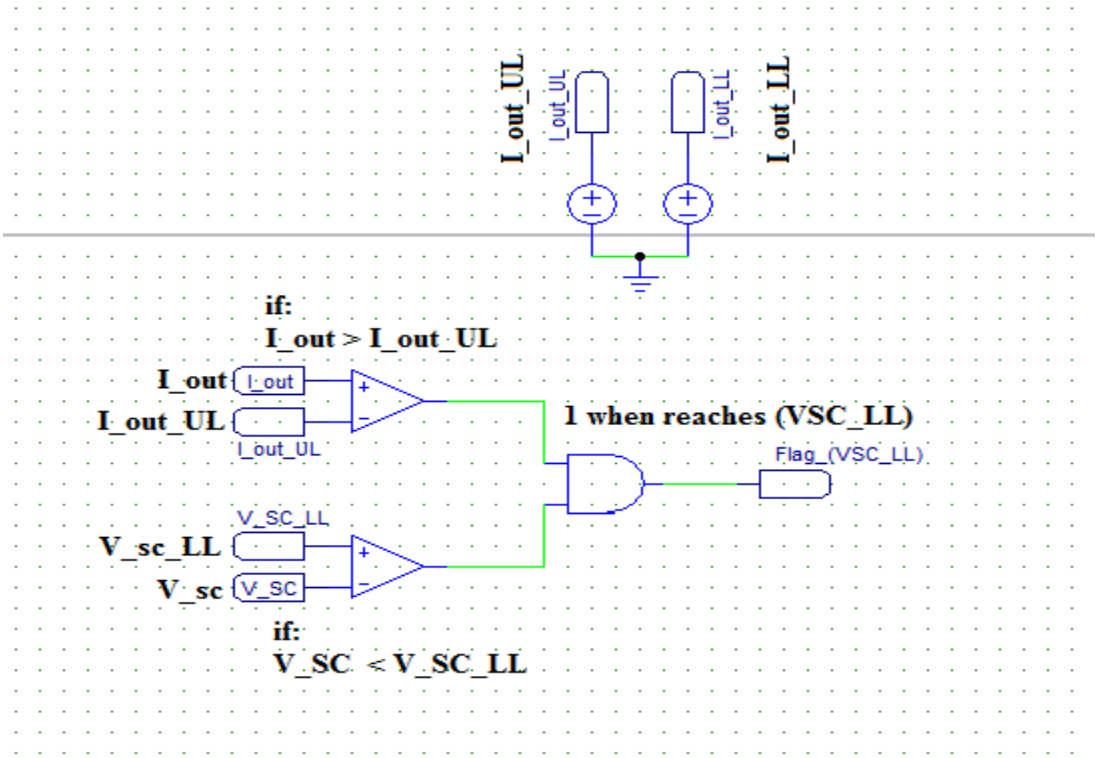

Figure 3.16 Lower voltage limit of SC (logic circuit)

The first comparator will result "1" if the super capacitor is discharging (I_out > I_out_UL). Second comparator will result "1", if the voltage in the super capacitor has reached the lower voltage limit (V_sc_LL). The resultant of this circuit will be "1", when the super capacitor voltage has reached the lower voltage limit and is still discharging. The output of this circuit is represented by (Flag_(VSC_LL)).

In Figure 3.17, one can see the control loop for current control and lower voltage limit of the Super capacitor. There is a multiplexer, which provides reference for the voltage control loop. This multiplexer has two inputs and one control signal. When extra load is added to the DC bus, the SC will discharge. As the SC voltage reaches the lower voltage limit (V_SC_LL), the Flag_(VSC_LL) becomes "1". In which case the multiplexer will provide lower voltage limit reference value (V_SC_LL), to the voltage control loop, which will be compared with the super capacitor voltage (V_sc). The result will be provided to the PI controller. For the PI controller the values of gain (kp) and time constant (t) were calculated in the previous section. This PI controller will provide a reference current, which is required to keep the voltage of the super capacitor at the reference

value (V_SC_LL). That current reference will be added in the control loop (Stage-1). Which will result in a reference value for super capacitor current (I_sc).

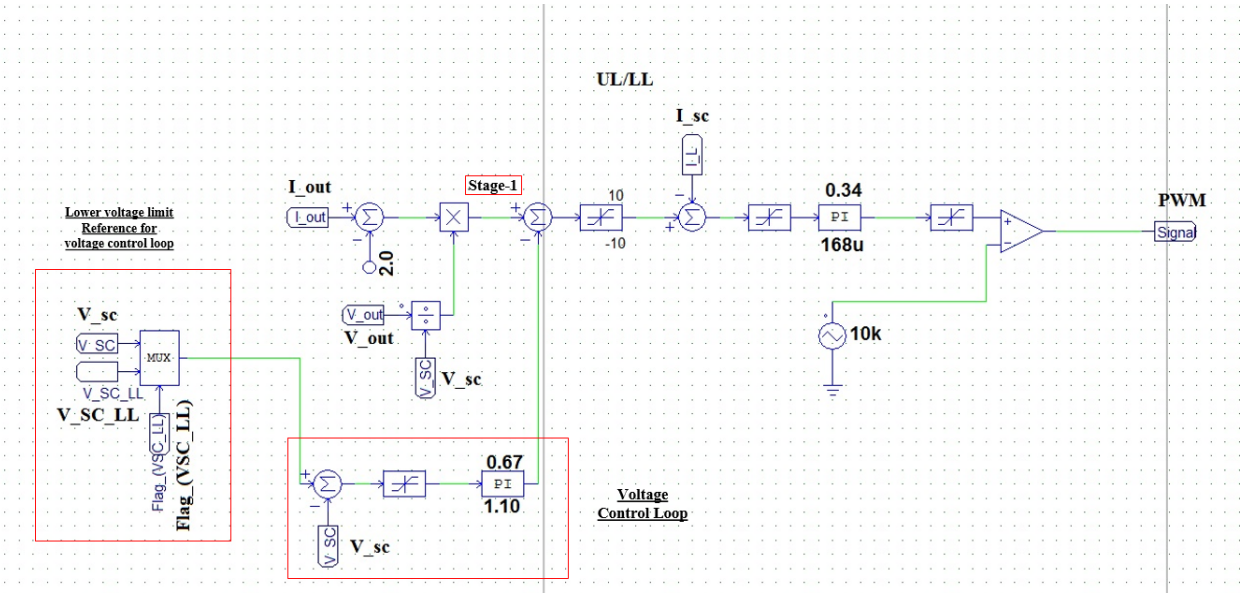

Figure 3.17 Lower voltage limit control Loop of the SC

Figure 3.18, show the simulation result of the voltage control loop, for lower voltage limit. When the output/load current (I_out) is 2A (reference value for the output of FC Converter), the super capacitor is not discharging and its voltage stays at 32V (base voltage level). When extra load is added to the DC bus, the output/load current (I_out) rises to 4.5A. The super capacitor discharges to keep the fuel cell current constant at 3.3A (maximum power point). When the SC reaches the lower voltage limit (V_SC_LL), due to the voltage control loop, the super capacitor stops discharging and the super capacitor current (I_sc) goes to 0A. Because of which the fuel cell current (I_FC) rises to 7.3A.

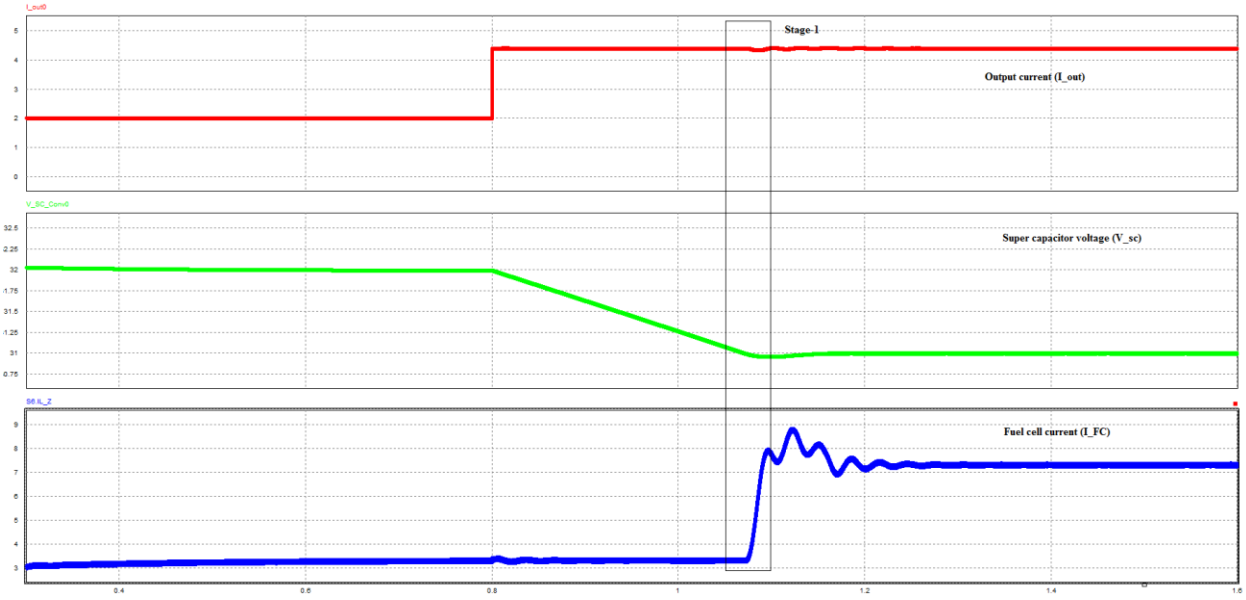

Figure 3.18 Lower voltage limit control Loop Simulation

The result shows that once the voltage in the super capacitor reached its lower voltage limit, it is no longer able to support the FCS until the voltage in the super capacitor rises later on, due to a decrease in the load demand.

3.6.2 Upper voltage limit

The upper voltage limit of the super capacitor is considered 33V for the simulation. If the load connected to the DC bus requires 2A current, in that case the fuel cell will be supplying 3.3A (maximum power point). If one reduces the load, the output current will go below 2A (reference value for the output of FC Converter). In that case the ESS will start absorbing power in order to keep the FCS operating at maximum power point. Due to which the voltage level in the super capacitor rises, the voltage in the super capacitor should not go above the upper voltage limit of the SC. In that case the super capacitor should stop charging. The logic circuit of upper voltage limit indicator of SC is similar to the one shown in Figure 3.17. When the super capacitor voltage reaches the upper voltage limit (V_sc_UL) and is still charging. The output of the indicator circuit is “1”, which is represented by (Flag_(VSC_UL)).

Figure 3.19, show the simulation result of the voltage control loop, for upper voltage limit. When the output/load current (I_out) is 2A (reference value for the output of FC Converter), the super capacitor is not charging or discharging and its voltage stays at 32V (base voltage level). When the output load is reduced, the output/load current (I_out) goes down to 0.3A (Stag-1). The super

capacitor charges to keep the fuel cell current constant at 3.3A (maximum power point). When the SC reaches the upper voltage limit (V_SC_UL), the super capacitor stops charging and the super capacitor current (I_sc) goes to zero. Because of which the fuel cell current (I_FC) goes down to 0.5A. The result shows that once the voltage in the super capacitor reached its upper voltage limit, it is no longer able to support the FCS until the voltage in the super capacitor decreases later on, due to an increase in the load demand.

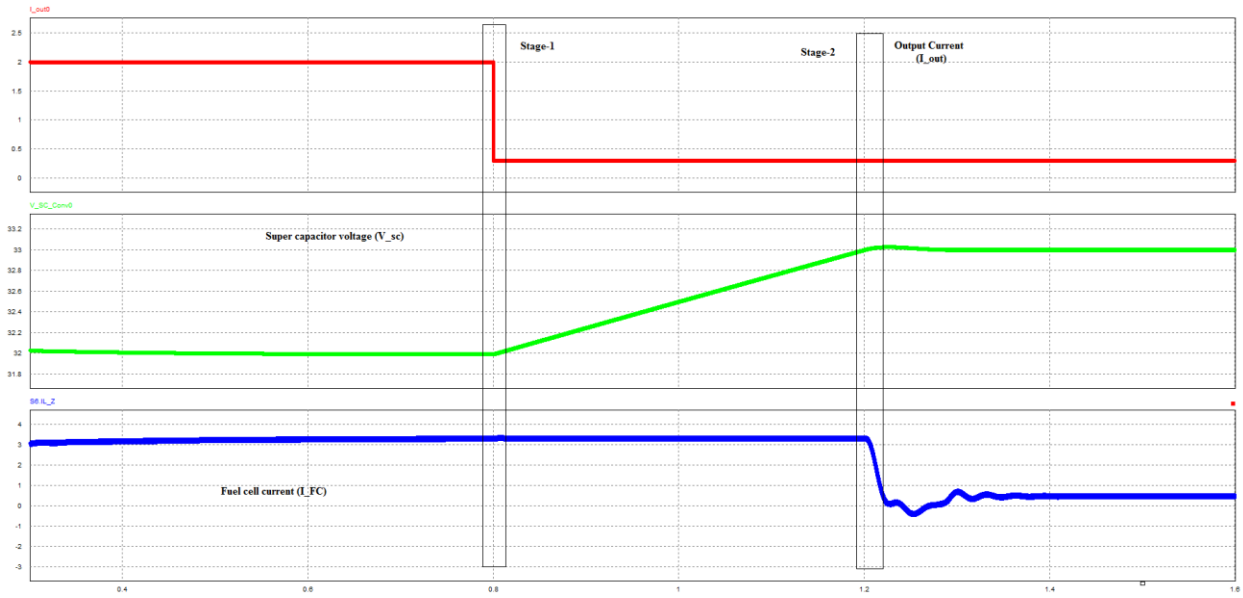

Figure 3.19 Upper voltage limit control Loop Simulation

The upper and lower voltage control loops will prevent the super capacitor to overcharge or discharge. If the voltage in the SC reaches its maximum of minimum voltage limit, it will not be able to support the FCS. At that stage, the FCS will not be operating at its maximum power point. When the voltage of the super capacitor is within its maximum and minimum voltage level. Another slow voltage control loop, having a bandwidth which is, 33% of the bandwidth of the upper and lower voltage control loop, will bring the voltage level of the supercapacitor to its base voltage level of 32V, which is explained in the next section.

3.7 Final Simulation

In order to make the FCS operate at the maximum power point, the control loops for current control and voltage control of the ESS are designed. A fast PI controller is designed for the super capacitor current control. The voltage level of the super capacitor should stay within the maximum and minimum voltage limit of super capacitor, PI control loop is designed to restrain the super capacitor voltage from crossing these limits. When the voltage level of super capacitor is within these limits, it should be able to support the FCS when required. Therefore another very slow PI control loop is designed to keep the voltage of the super capacitor at the base voltage level.

3.7.1 Control loops

In Figure 3.20, one can see the control loop for the ESS. The current control loop has been explained previously. This section explains the voltage control loops. One can see that, the reference current value for voltage regulation in the super capacitor (PI_VSC), which is explained in detail below, will be added in ref_1. The result will be the reference for the super capacitor current (I_sc), which is then compared with the actual super capacitor current to provide the error (*e*) for the PI controller.

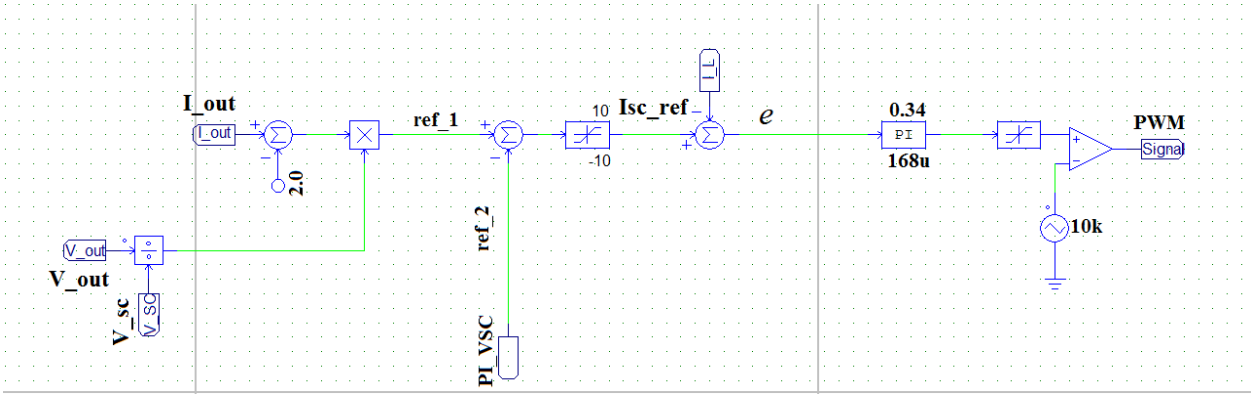

Figure 3.20 Current and voltage control loop for Super Capacitor Converter

In the complete control loop (current and voltage) of the SC converter as shown in Figure 3.20, one can see, at ref_2, the reference current to control the voltage level of the super capacitor (PI_VSC) is provided. Different PI control loops are designed to regulate the voltage in the ESS, which is shown in Figure 3.21.

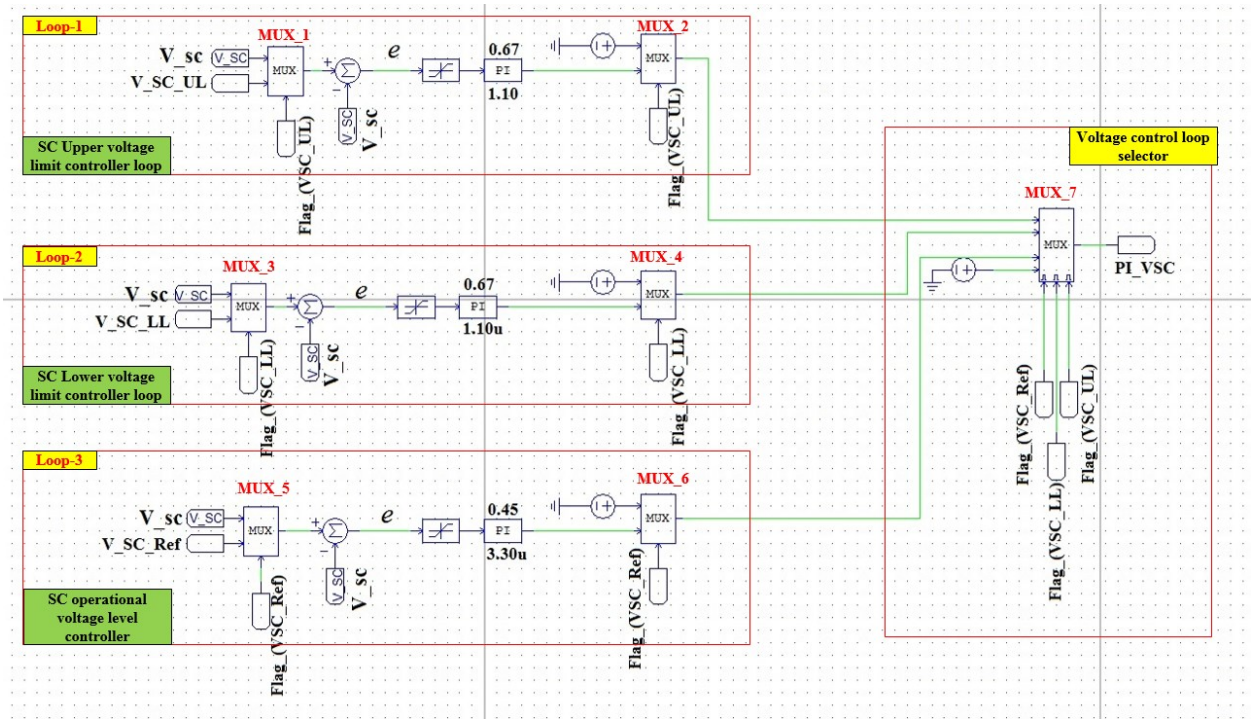

Figure 3.21 Controller loops of SC voltage level control

In Figure 3.21, one can see that, three different PI control loops are designed. Which are explained below.

- Loop-1: It is the control loop which provides the value of the reference current, needed to prevent over charging of the super capacitor. In this control loop, "V_SC_UL" is the upper voltage limit of the super capacitor. Which is kept at 33V, as mentioned previously. The output of "MUX-1" will provide the reference voltage level for the PI controller in Loop-1. The control signal of "MUX-1" is "Flag_(VSC_UL)", which was explained in the previous section.

  Case-1: When the voltage of the SC reaches the maximum voltage limit of SC, the "Flag_(VSC_UL)" will be "1", in any other case it will be "0". When the "Flag_(VSC_UL)" is "1", the multiplexer "MUX-1" will provide "V_SC_UL" as output. "V_SC_UL" will be compared with the actual voltage of the super capacitor (V_sc) and the resultant error (*e*) will be the input of the PI controller. The values of the gain and time constant of the PI controller were calculated in the previous section. The output of the PI controller will be the input of "MUX-2". "MUX-2" also has "Flag_(VSC_UL)", as a input

signal. In case when “Flag_(VSC_UL)” is “1”, “MUX-2” will simply pass the output of the PI controller to “MUX-7”.

Case-2: When the voltage of the SC is less than the maximum voltage limit of the SC, the “Flag_(VSC_UL)” will be “0”. In that case, the output of “MUX-2” will be “0”. Which will be passed to the “MUX-7”.

- Loop-2: It is the control loop which provides the value of reference current, required to prevent discharging of the super capacitor beyond the lower voltage reference of SC (V_SC_LL). The design of Loop-2 is the same as Loop-1, the only difference is that, the second input of multiplexer MUX-3 is “V_SC_LL” instead of “V_SC_UL”, which is kept at 31V for the simulation.

  Case-1: When the SC discharges and its voltage reaches the lower voltage limit (V_SC_LL), the value of “Flag_(VSC_LL)” will be “1”. Therefore, the multiplexer “MUX-3” will provide “V_SC_LL” as output. Which is then compared with the actual super capacitor voltage (V_sc) and the resultant error will be provided to the PI controller. The output of the PI controller is passed on to the “MUX-7” through “MUX-4”.

  Case-2: When the voltage of SC is higher than the minimum voltage limit of SC (V_SC_LL), the “Flag_(VSC_LL)” will be “0”. In that case the output of “MUX-4” will be “0”. Which will be passed to the “MUX-7”.

- Loop-3: This is the slow PI control loop, which is designed to keep the voltage of the super capacitor at the base voltage level, in order to support the FCS. The base voltage level is 32V for simulation. When the voltage of the super capacitor is within the maximum and minimum voltage limits, the reference “Flag_(VSC_Ref)” will “1”, in any other case it will be “0”. When the “Flag_(VSC_Ref)” is “1”, “MUX-5” provide 32V reference voltage level for the PI controller, which is then compared with the actual super capacitor voltage (V_sc). The resultant error is provided to the PI controller. “MUX-6” will pass on the output value of the slow PI controller, to “MUX-7”. In case when the voltage of SC is not within the upper and lower voltage limits, the “Flag_(VSC_Ref)” will be “0”. In which case “MUX-6” will provide “0”, as an output to “MUX-7”.

In Figure 3.21, one can see that in all the cases, one of the flags for the SC voltage, will be “1” and the other two flags will be “0”. Which means, that the reference value for the SC voltage control loop will be either “V_SC_LL”, “V_SC_UL” or “V_SC_Ref”, depending upon the flags.

The control signals of the "MUX-7" are the same flags signals, which indicates, when the voltage of SC has reached the upper or lower voltage limits. When the SC voltage reaches the upper voltage limit (V_SC_UL), the value of "Flag_(VSC_UL)", will be "1". In this case, the output of "Loop-1" will be the output of "MUX-7" (PI_VSC). When the SC voltage reaches the lower voltage limit (V_SC_LL), the value of "Flag_(VSC_LL)", will be "1" and the other two flags will be "0". In this case, the output of "Loop-2" will be the output of "MUX-7" (PI_VSC). In any other cases, the output of "Loop-3" will be the output of "MUX-7" (PI_VSC). In order to keep the voltage of the super capacitor within the upper and lower limits, the output of "MUX-7" (PI_VSC), is provided to the final control loop, shown in Figure 3.20.

3.7.2 Simulation results

For simulation and experimentation, the reference value for the output of FC Converter is 2A in this study. There are three possible cases to consider for simulation. The load current at the DC bus can be at the reference value (2A) for the output of FC Converter, higher than the reference value or lower than the reference value. In all these scenarios, the FCS should operate at the maximum power point. The ESS should support the FCS until the voltage in the super capacitor reaches the upper or the lower limit. For the final simulation, the same power circuit is used as shown in Figure 3.12. The control circuit used for the simulation is shown in Figure 3.20. In order to reduce the processing time, the operating parameters chosen for simulation are given in Table 3.4.

Table 3.4 Operating parameters for simulation

SC(capacitance)	V_out	V_SC_LL	V_SC_Ref	V_SC_UL
1F	48V	31V	32V	33V

Figure 3.22, shows the simulation results, when the DC bus load, is higher than the 2A. Results for the current control and voltage control loop of the ESS are presented.

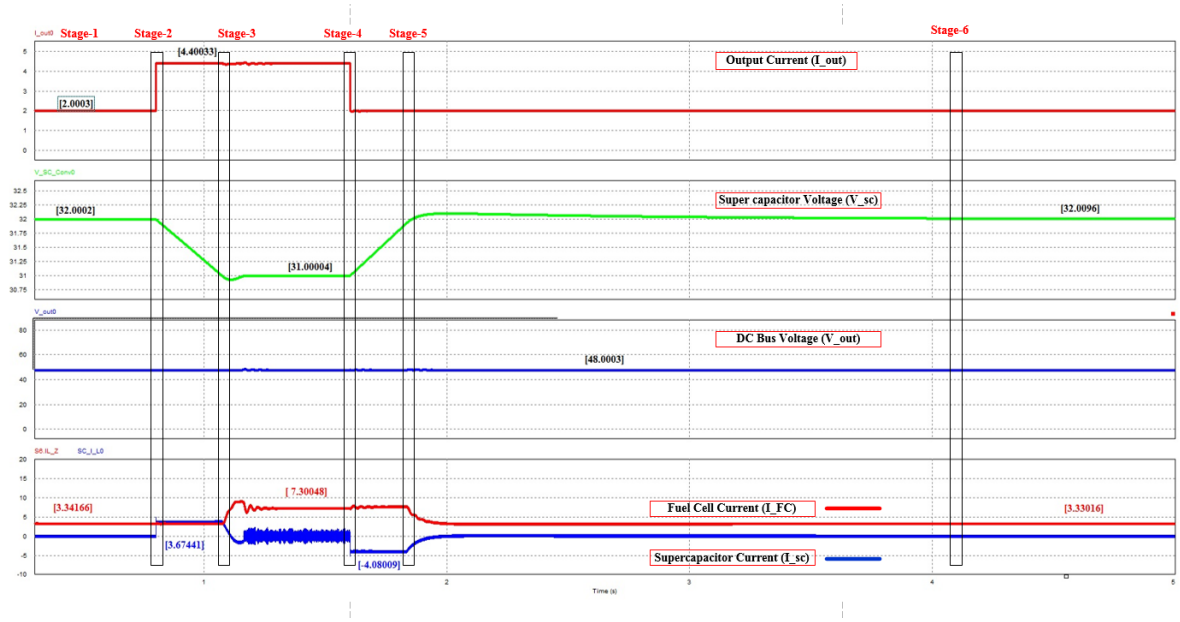

Figure 3.22 Simulation results for high DC bus load

Below is the explanation of different stages in the simulation results:

- Initially at Stage-1, one can see that the fuel cell current (I_FC) is 3.3A (maximum power point). The output/load current (I_out) is at 2A. As one knows that the reference current for the output of FC Converter (I_ref) is also 2A. That is why at stage-1, the ESS is not supplying or absorbing any current because of which the super capacitor current (I_sc) is at 0A and the super capacitor voltage is (V_sc) is at 32V (base voltage level).

- At Stage-2, more load is added. The output/load current (I_out) increases to 4.4A, which is higher than the reference value (I_ref) for the output of FC Converter. Due to the current control scheme, the ESS supplies extra current that is why the super capacitor current rises to 3.6A.

Current supplied by the SC at Stage-2:

$$I\_sc = \frac{V\_out \times (I\_out - I\_ref)}{V\_sc}$$

$$I_{sc} = \frac{48 \times (4.4 - 2)}{32} = 3.6A$$

One can see that as the ESS supplies the current to the DC bus, the voltage of the super capacitor (V_sc) decreases due to discharging. While the fuel cell (I_FC: Zain converter input current) current remains at the maximum power point (3.3A).

- At Stage-3, the voltage of the super capacitor reaches the lower voltage limit (V_SC_LL). Therefore the voltage control loop, won't allow the super capacitor to discharge any further. That is why super capacitor voltage (V_sc) stays at 31V. Because of the voltage control loop, the super capacitor current (I_sc) goes to 0A. Now, the fuel cell has to supply the total current required by the DC bus load and the FCS is no longer operating at the maximum power point.

  Current supplied by the fuel cell at Stage-3:

$$I\_FC = \frac{V\_out \times I\_out}{V\_FC}$$

$$I\_FC = \frac{48 \times (4.4)}{28.8} = 7.3A$$

  One can see that the fuel cell current (I_FC) goes up to 7.3A. The super capacitor cannot discharge any further.

- At Stage-4, the extra load is removed from the DC bus and the output/load current (I_out) goes down to 2A again (reference current for the output of FC Converter). The super capacitor voltage is still at the lower voltage limit (V_SC_LL) of 31V. Therefore, the super capacitor voltage will start to rise, because of the slow PI control loop. The super capacitor current (I_sc) will become negative, as the ESS is absorbing power. The FCS will keep supplying current for the DC bus load and to charge the super capacitor as well, therefore it won't be operating at the maximum power point.
- At Stage-5, the super capacitor voltage (V_sc) reaches the base voltage level (V_SC_Ref) of 32V. Therefore because of the voltage control loop, the super capacitor will stop charging (as the output/load current is at 2A). The voltage of the super capacitor will slowly go to the base voltage level due to the slow PI control loop. The fuel cell current will start

dropping to 3.3A (maximum power point). The super capacitor current (I_sc) will start going up to 0A smoothly.

- At Stage-6, the super capacitor voltage (V_sc) stabilizes at the base voltage level (32V) because of the slow PI control loop. At this stage, the fuel cell is operating at the maximum power point and the super capacitor current (I_sc) will be 0A, as its not supplying or absorbing energy, because the output/load current (I_out) is at 2A (reference current for the output of FC Converter).

In this simulation result, one can see that the DC bus voltage remained constant at 48V. It is also evident that the ESS can support the FCS until, the voltage in the super capacitor drops down to its lower voltage limit (V_SC_LL). The slow PI control loop also forces the super capacitor to reach its base voltage level.

Figure 3.23, shows the simulation results, when the external load is less than the reference current for the output of FC Converter. Results for the current control and voltage control of the ESS are presented.

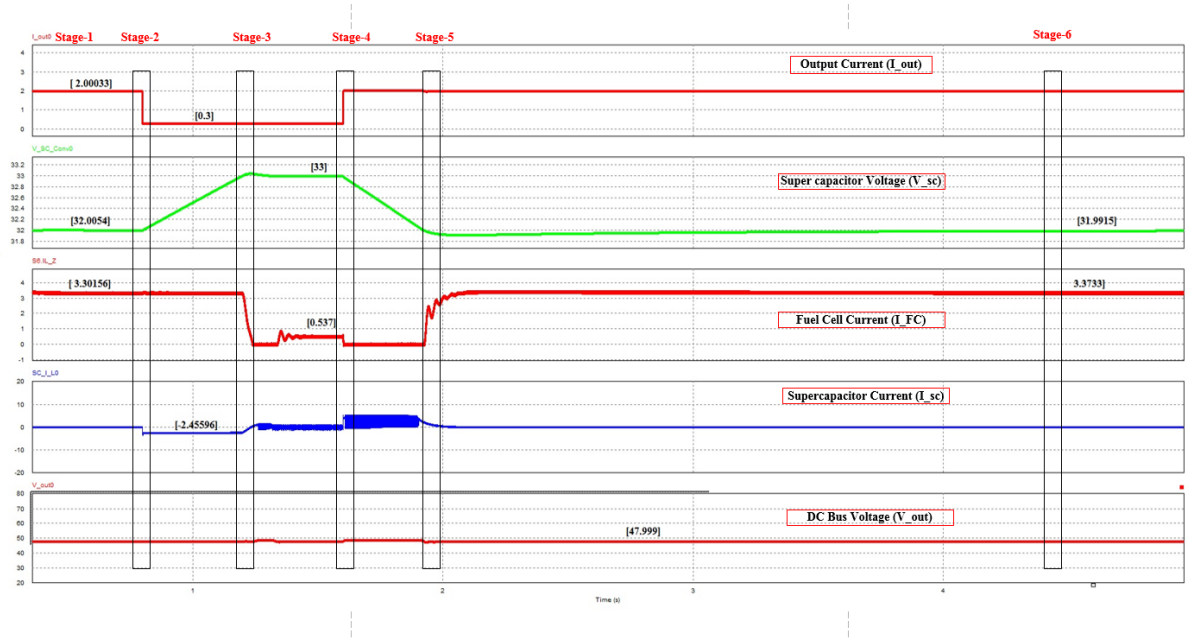

Figure 3.23 Simulation results for low DC bus load

The explanation of different stages in the simulation results is given below:

- Initially at Stage-1, one can see that the fuel cell current (I_FC) is 3.3A (maximum power point). The output/load current (I_out) is at the 2A (reference current for the output of FC Converter). That is why at stage-1, the ESS is not supplying or absorbing any current. Thus, the super capacitor current (I_sc) is at 0A and the super capacitor voltage is (V_sc) is at 32V (base voltage level).

- At Stage-2, some load is removed. The output/load current (I_out) decreases to 0.3A. Due to the current control scheme, the ESS absorbs the extra current to keep the FCS at maximum power point, that is why the super capacitor current goes to -2.4A.

  Current absorbed by the SC at Stage-2:

$$I\_sc = \frac{V\_out \times (I\_out - I\_ref)}{V\_sc}$$

$$I_{sc} = \frac{48 \times (0.3 - 2)}{33} = -2.4A$$

  One can see that as the ESS absorbs the current from the DC bus, the voltage of the super capacitor (V_sc) increases due to charging, while the fuel cell current remains at the maximum power point (3.3A).

- At Stage-3, the voltage of the super capacitor reaches the upper voltage limit (V_SC_UL). Therefore, the voltage control loop, prevents the super capacitor from charging any further. That is why the super capacitor voltage (V_sc) stays at 33V (upper voltage limit). Because of the voltage control loop, the super capacitor current (I_sc) goes to 0A. Now the fuel cell has to supply less current (as required by the output load) and the FCS is no longer operating at the maximum power point.

Current supplied by the fuel cell at Stage-3:

$$I\_FC = \frac{V\_out \times I\_out}{V\_FC}$$

$$I\_FC = \frac{48 \times (4.4)}{28.8} = 0.5A$$

One can see that the fuel cell current (I_FC) goes down to 0.5A because the super capacitor cannot charge any further.

- At Stage-4, the load removed at Stage-2, is added again to the DC bus and the output/load current (I_out) goes down to 2A (reference current for the output of FC Converter) again. The super capacitor voltage is still at the upper voltage limit (V_SC_UL) of 33V. However, the super capacitor voltage will start to drop, as the super capacitor discharges because of the slow PI control loop. The super capacitor current (I_sc) will become positive, as the ESS is supplying power to the DC bus. Fuel cell will keep supplying less current for the DC bus load because the super capacitor is discharging slowly as well, to reach its base voltage level. Therefore, FCS is still not operating at the maximum power point.

- At Stage-5, the super capacitor voltage (V_sc) reaches the base voltage level (V_SC_Ref) of 32V. Therefore, because of the voltage control loop, the super capacitor will stop discharging (as the output current is at 2A). The fuel cell current will start rising to 3.3A (maximum power point). The super capacitor current (I_sc) will start going down to 0A, steadily.

- At Stage-6, the super capacitor voltage (V_sc) stabilize the base voltage level (32V) because of the slow PI control loop. At this stage, the fuel cell is operating at the maximum power point and the super capacitor current (I_sc) will be 0A, as its not supplying or absorbing energy, because the output/load current (I_out) is at 2A (reference current for the output of FC Converter).

In this simulation results, one can see that the ESS can support the FCS until the voltage in the super capacitor rises up to its upper voltage limit (V_SC_UL).

One can see that the ESS can support the FCS by supplying or absorbing energy, in order to keep it operating at the maximum power point. But, when the voltage in the super capacitor reaches its upper or lower voltage limit, at that stage, it can no longer support the FCS, by absorbing and injecting energy, respectively. A slow PI control loop in used to bring the voltage level of super capacitor at a certain point (32V), from where it can support the FCS, in an event of load variation.

3.8 Summary

In this Chapter, the FC Converter's power and control circuits were simulated for voltage regulation in the DC bus and the simulation results were shown. The design of PI controllers, for the regulation of the inductor current of the bi-directional Class-C DC-DC converter (SC converter), and for the voltage regulation of the ESS is presented. The control scheme, is capable of controlling the inductor current (of SC converter) and voltage regulation ESS. Different tests were carried out to simulate several possible scenarios. The controller showed good performance for current control and voltage regulation, and the expected results were obtained and presented. Both power converters will be implemented and the experimental implementation and results will be presented in Chapter 4.

Chapter 4 Experimental Implementation

The primary goal in this work is to implement the proposed indirect current control scheme for the hydrogen fuel cell (source) and voltage control scheme for the super capacitor (storage element) in a DC nanogrid. The experimental setup for obtaining the results is described in this Chapter. Then, experimental tests are performed for different cases. Finally, the experimental results are presented and discussed for all the cases.

4.1 Experimental setup

The experimental prototype of the bi-directional 4-switch DC-DC converter (SC converter) is implemented in this work, which is a new realization of an existing Class-C Texas Instruments (TI) converter "LM5170EVM-BIDIR Evaluation Module*"* that was designed for a similar application. The specifications of the converter are already mentioned in Chapter 2. The 4-switch DC-DC converter is able to control the injected and absorbed current in the DC bus. It consists of four MOSFETS with the respective gate driver circuits. Also, voltage and current sensors are installed for sensing the input and output voltages as well as the inductor current. The converter is equipped with a digital controller (DSP). The layout of the printed circuit board (PCB) was designed using "EASYEDA" software. The PCB was ordered and then populated in the lab.

In Figure 4.1, one can see the implemented bi-directional 4-switch DC-DC converter (SC converter). The inductor is kept away from the board in order to minimize the electromagnetic interference with the sensors. The dual arrows indicate that the converter can supply or absorb power in either direction. The voltage sensors for the super capacitor voltage measurement and for the DC bus voltage measurement, are mounted on the PCB board, with the MOSFETs and the gate driver circuits. The microcontroller (Texas Instrument DSP "TMS320F2833X") is interfaced with the PCB through the connecting wires. One can also see, that the current sensors for the measurement of the inductor current and the output current are implemented on another circuit board, with the unity gain amplifier circuit.

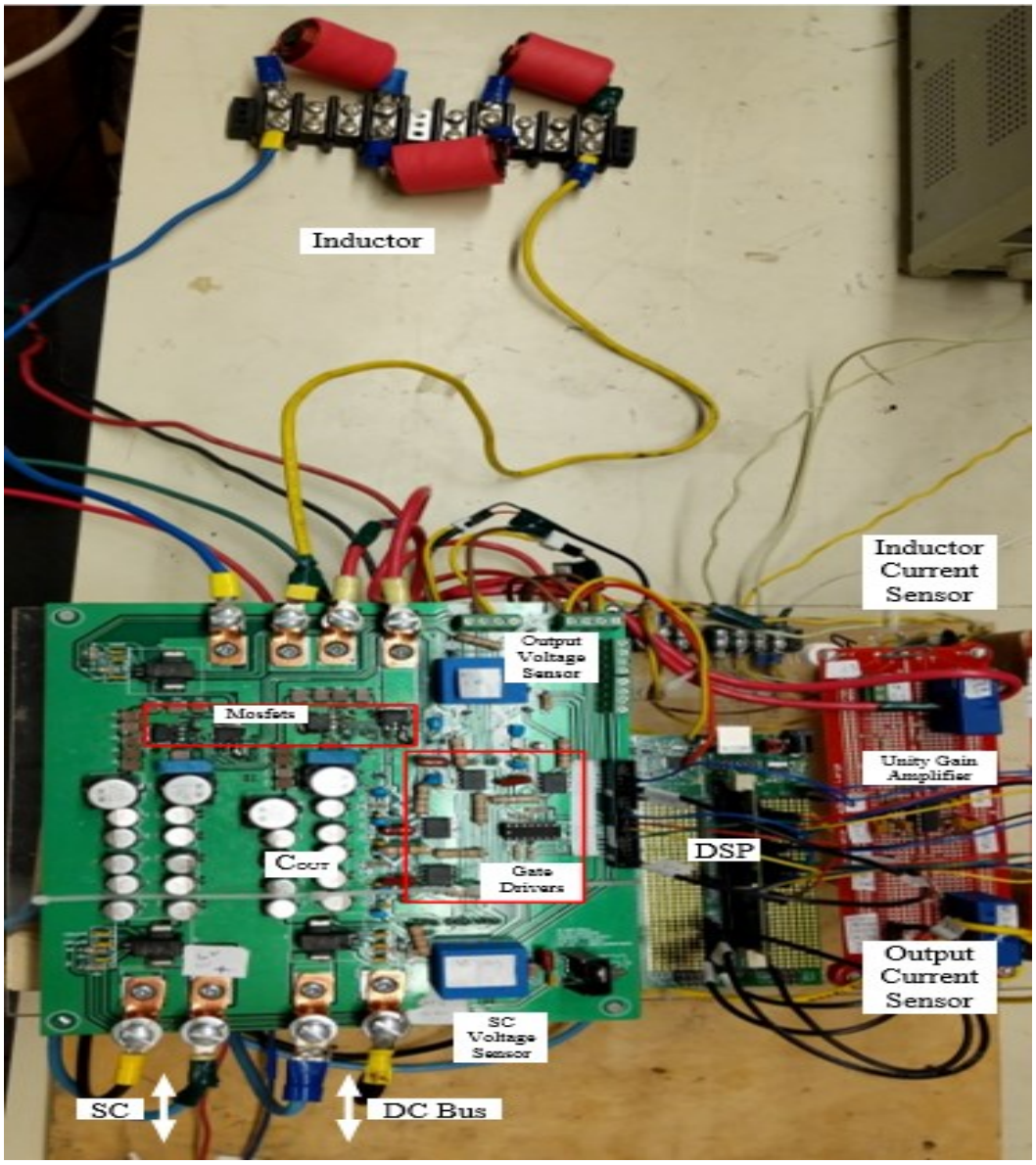

Figure 4.1 Snapshot of the 4-switch DC-DC converter (SC converter)

In Figure 4.1, one can see that SC converter is connected in shunt with the output of the FC converter. The current and voltage sensors data is sent to the unity gain amplifier circuit and then to the DSP through the connection points on the converter PCB board. Current and voltage control loops are implemented in the DSP, which provides the resultant PWM signal. The PWM signal is then provided to the gate drive circuits through connection points in the converter PCB board. The gate driver circuits then switch the MOSFETSs "ON" and "OFF" accordingly.

In Figure 4.2, one can see the layout of the complete system. For preliminary experimentation, a DC power supply is used instead of the fuel cell. The output of the power supply is connected to

the FC Converter input, and the FC Converter provides regulated voltage (48V) to the DC bus. The super capacitor is connected to the input of the SC converter, the converter output is connected to the DC bus.

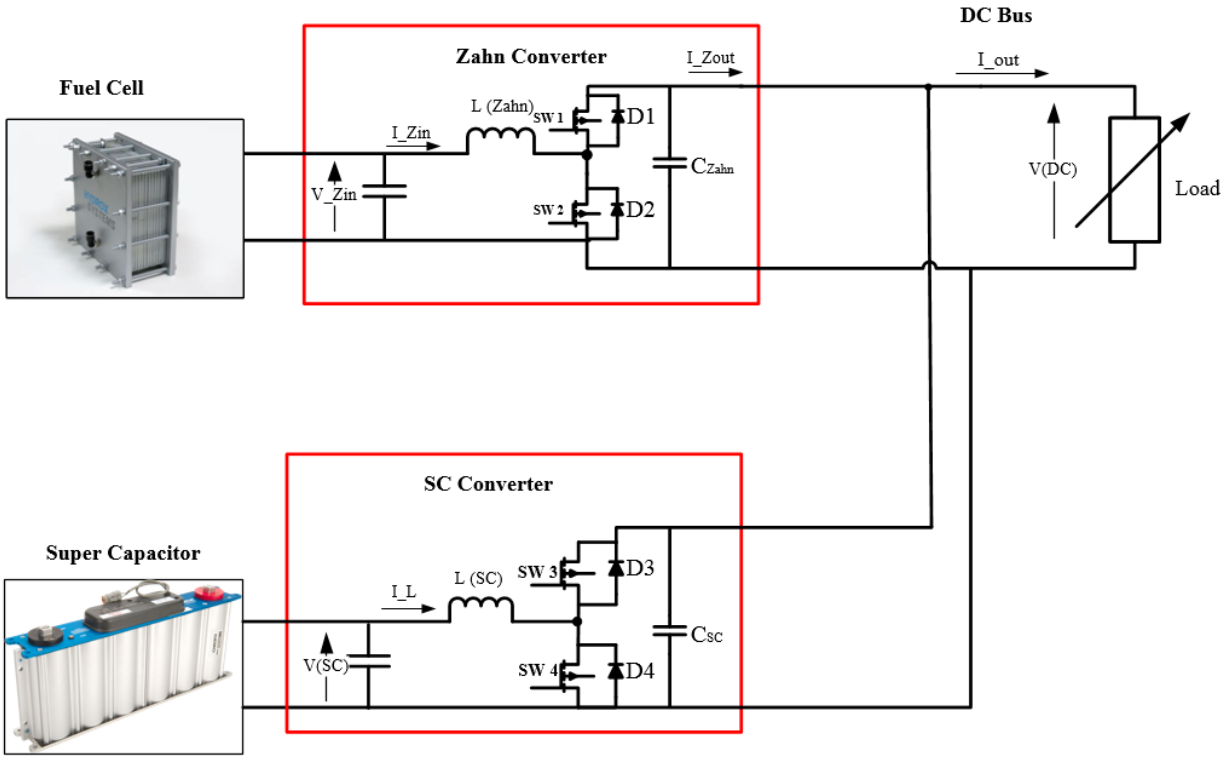

Figure 4.2 Complete System Layout.

Figure 4.3 shows the experimental setup, which is assembled in the laboratory. Where the arrows indicate the direction of current flow. The arrow at the FC Converter shows that, it is operated as unidirectional and the arrow at the SC converter indicates that it is operated as bi-directional. That is, it can inject or absorb current from the DC bus. The experimental results are presented on the oscilloscope.

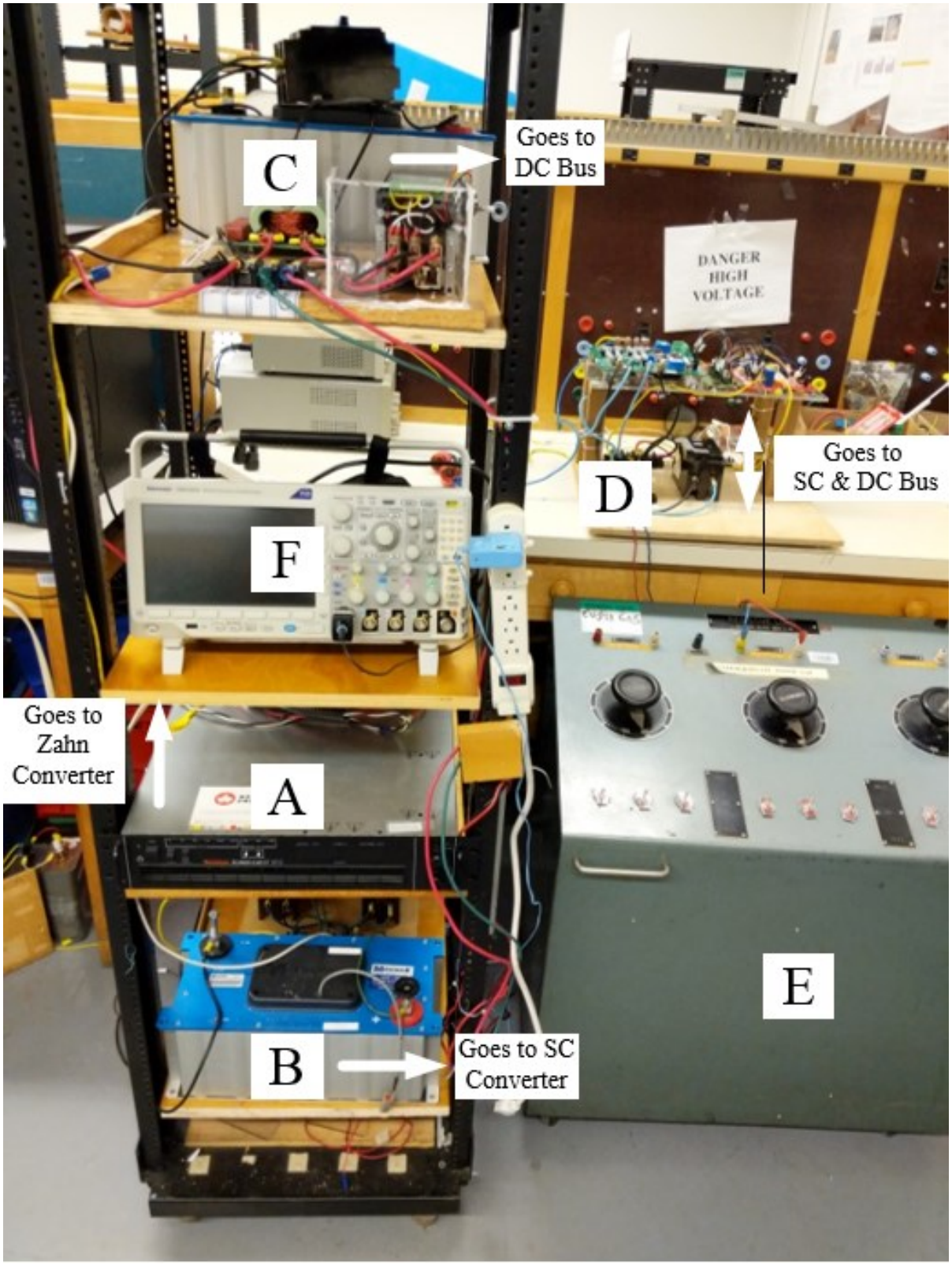

Figure 4.3 Snapshot of the actual experimental setup. (A) Power supply. (B)Super Capacitor. (C) FC Converter. (D) 4-switch DC-DC converter (SC converter). (E) DC Bus Load. (F) Oscilloscope

4.2 FC Converter Output

As one knows that FC Converter is used in this project to regulate the DC bus voltage at 48V. In Figure 4.4, one can see the voltage regulation achieved by FC Converter. From the results, it can be observed that the output voltage of the FC Converter is 48.1V (1), while the FC output voltage (2) is 28.8V (voltage of the FC at maximum power point). The output current of the FC should be 3.47A (ideally), when the output current of FC Converter is 2.08A (4). In this case, the FC output current which is measured through current sensor is 3.88A (3).

$$I\_FC = \frac{V\_out \times I\_Zout}{V\_FC}$$

$$I\_FC = \frac{48.1 \times 2.08}{28.8} = 3.47A$$

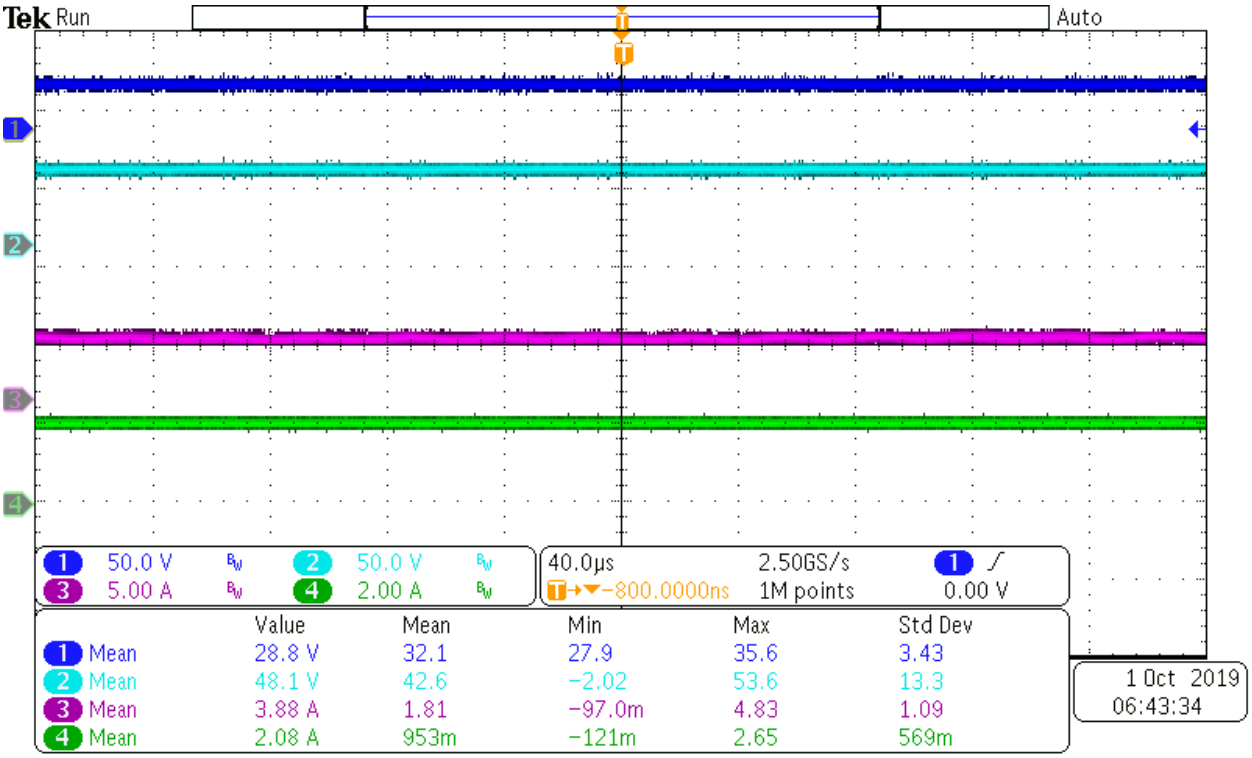

Figure 4.4 FC Converter output voltage

4.3 Open loop test

In this project, two power electronics converters are used. In the previous Chapter, all the necessary simulations were done, to get the required results. The FC Converter was configured for voltage regulation of the DC bus. After the design and assembly of the bi-directional 4-switch DC-DC converter (SC converter), to check the SC converter performance, open loop tests were conducted. Before performing buck and boost mode tests, the gate driver circuit of SC converter is tested. Recall the Figure 2.3, where one can see that the SC converter contains four MOSFETs. +15V potential is provided from an onboard power supply to turn the MOSFET "ON" and -8.5V potential is provided to turn the MOSFET "OFF".

4.3.1 Gate driver circuit test

Below are the switching signals, provided to all four MOSFETs for this test.

Switching Signals:

- S1: Always ON
- S2: Always OFF
- S3: Switching (Duty Cycle 48%)
- S4: Complement of S3

In order to make the SC converter operate in class-C mode, MOSFET S1 has to stay "ON" and MOSFET S2 has to stay "OFF", in all the tests. A 48% duty cycle signal is provided from the DSP to the gate driver circuit, of MOSFETs S3 at a frequency of 10 kHz. In Figure 4.5, one can see the gate to source signals for each MOSFET of the SC converter.

Results:

- 1. ---- S3 (switching 48% Duty Cycle)
- 2. ---- S4 (Complement of S3)
- 3. ---- S1 (always ON)
- 4. ---- S2 (always OFF)

The results are displayed on the oscilloscope screen. Where one can see that, the gate to source signal of S3 is a complement of S4. While the gate to source value of S1 is at 15.9V and that of S2 is at -8.31V.

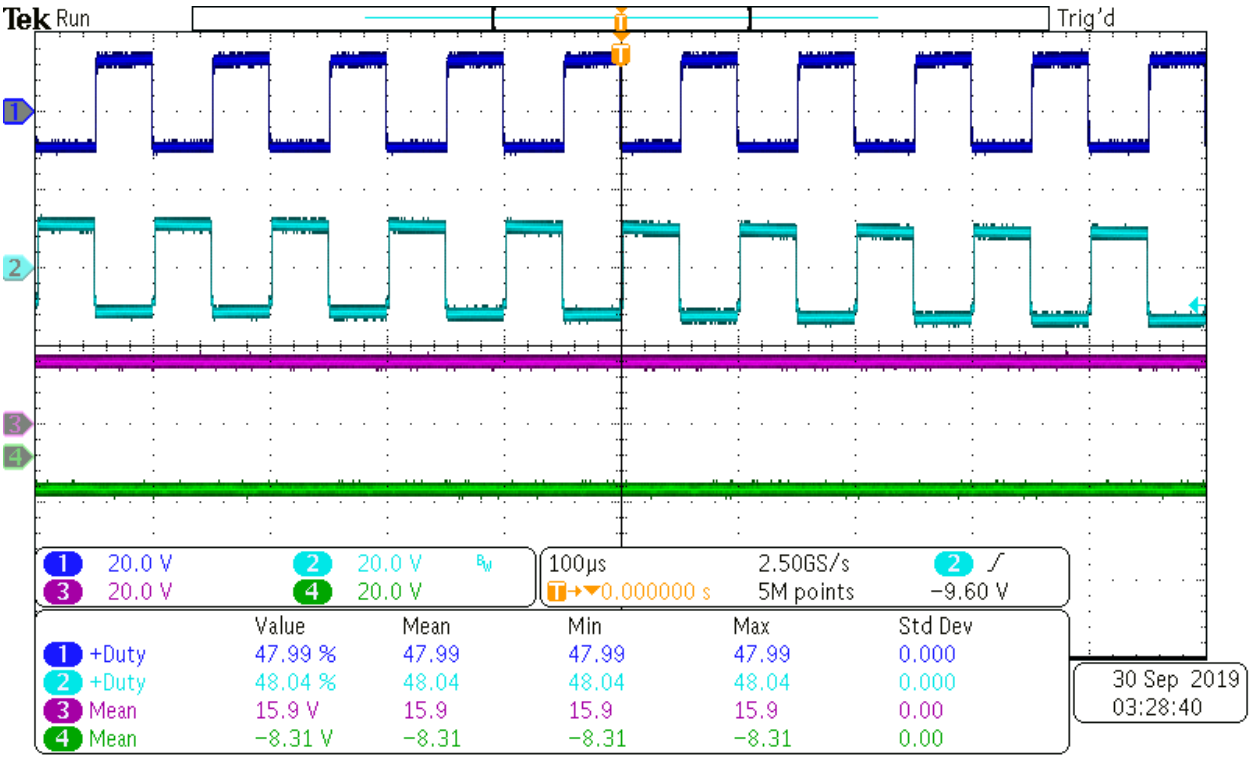

Figure 4.5 Switching Signals for the MOSFETs

4.3.2 Boost mode test

In boost mode, power flows from LV side to the HV side. Therefore, the SC Converter will be provided power (using a DC voltage source), at the low voltage side. At the high voltage side (where the load is connected), one should get a higher voltage, depending upon the duty cycle. Same gating signals are used for this test as shown in the previous test. The mathematical calculation for the boost mode test are given below, where D is the duty cycle for MOSFETs S3 and S4.

Calculations for boost mode test [13]:

$$V\_out = \frac{V\_in}{1 - D} = \frac{25.6}{1 - 0.48} = 49.23V$$

Expected results:

$$V\_in = 25.6V$$

$$V\_out = 49.2V$$

Results:

- 1. V_in: ---- Input voltage (LV side)
- 2. V_out: ---- Output voltage (HV side)
- 3. I_L: ---- Inductor current
- 4. I_out: ---- Output/load current

In Figure 4.6, one can see the results of the boost mode test. Where the 2nd oscilloscope signal is the output voltage (V_out), the 1st oscilloscope signal is the input voltage (V_in), the 3rd oscilloscope signal is the inductor current (I_L) and the 4th oscilloscope signal is the output/load current (I_out: after the output capacitor filter of the 4-switch converter).

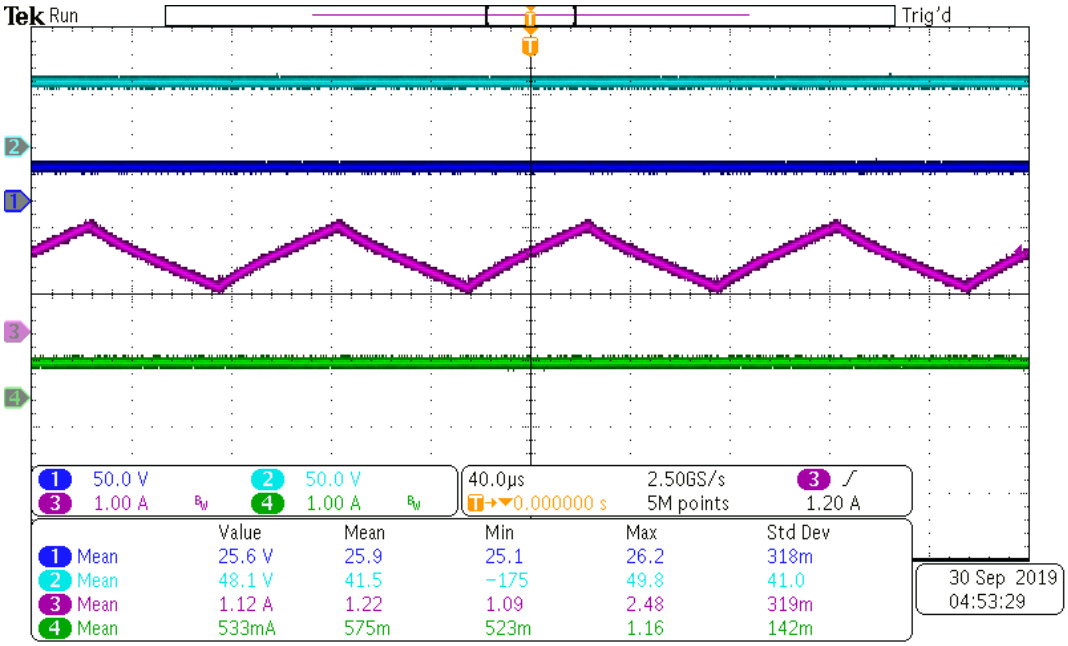

Figure 4.6 Boost mode test

The slight mismatch in the output voltage is due to the losses in the circuit. Several boost mode tests were performed to verify the performance of the SC converter, one is shown above. Table 4.1 shows, some boost mode test results, with different output loads to test the performance of SC converter.

Table 4.1 Boost mode test results

Tests	**Input Voltage**	**Output Voltage**	**Inductor Current**	**Output Current**	**Load**
Test 1	25.6V	48.1V	1.12A	533mA	90 Ω
Test 2	25.8V	48.5V	2.25A	1.15A	42 Ω
Test 3	25.4V	47.6V	3.21A	1.67A	15 Ω

One can see from the boost mode test results, the power flow from LV side to HV side. The voltage at the HV side (V_out), is close to the expected voltage value, shown in the calculation

above. When the load at HV side change, the inductor current (I_L) and output/load current (I_out) also change accordingly.

4.3.3 Buck mode test

In buck mode, power flows from HV side to the LV side. Therefore, the SC Converter will be provided power, at the high voltage side through a DC power supply. At the low voltage side (where the load is connected), one should get a lower voltage, depending upon the duty cycle. For this test the Duty cycle for (MOSFET) S3 is 46%. The calculations for this test are given below.

Calculations for buck mode test [13]:

$$V\_out = V\_in \text{ x } D == 48.4 \text{ x } 0.46 = 22.26V$$

Expected results:

$$V\_in = 48.4V$$

$$V\_out = 22.26V$$

Results:

- 1. V_out: ---- Output voltage (LV side)
- 2. V_in: ---- Input voltage (HV side)
- 3. I_L: ---- Inductor current
- 4. I_out: ---- Output/load current

In Figure 4.7 above, one can see the results of the buck mode test. Where 1st oscilloscope signal is the output voltage (V_out), the 2nd oscilloscope signal is the input voltage (V_in), the 3rd oscilloscope signal is the inductor current (I_L) and the 4th oscilloscope signal is the output/load current (I_out).

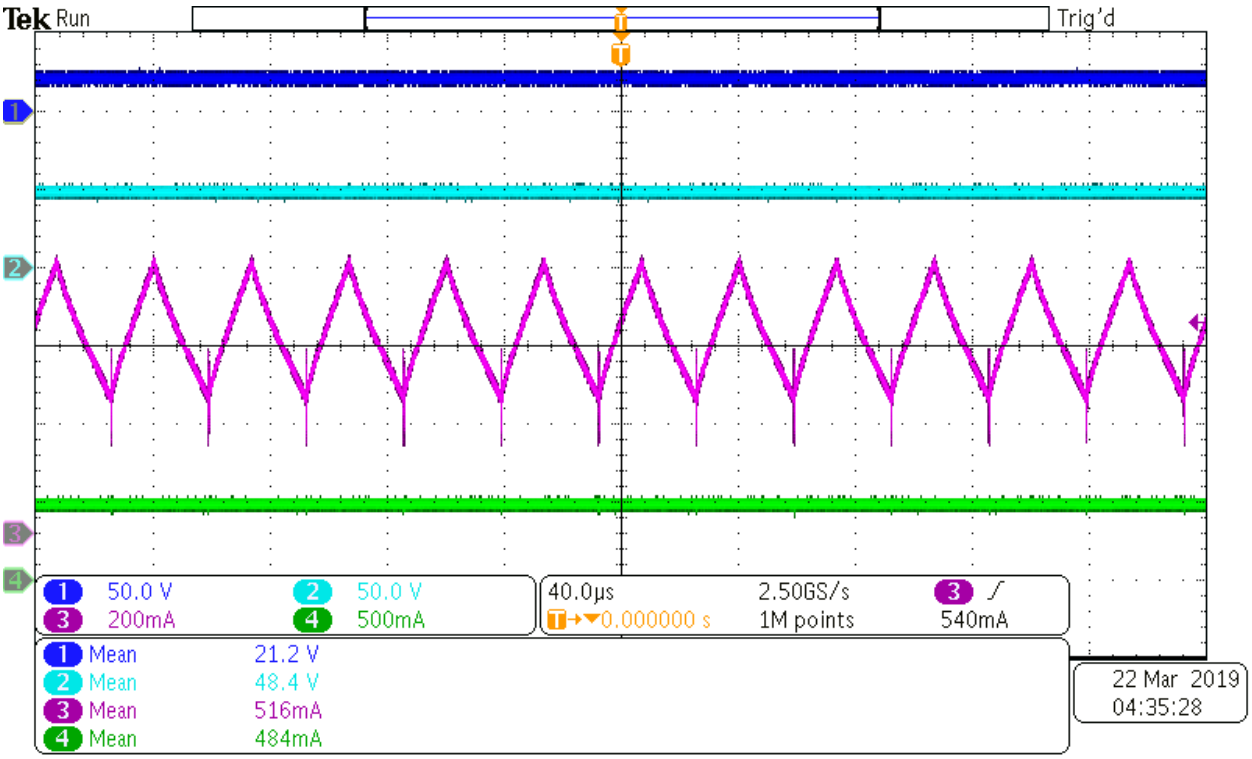

Figure 4.7 Buck mode test

Buck mode test results are shown in Table 4.2.

Table 4.2 Buck mode test results

Tests	Input Voltage	Output Voltage	Inductor Current	Output Current	Load
Test 1	48.4V	21.2V	516mA	484mA	40 Ω

In Table 4.2, one can see that the SC converter is working as expected in the buck mode. One can see from the buck mode test results, the power flow from HV side to LV side. The voltage at the LV side (V_in), is close to the expected voltage value, shown in the calculation above.

From the test results, one can see that the SC converter is working as expected in boost mode and buck mode.

4.4 Closed loop test

After getting satisfactory results in the open loop test, closed loop tests are performed. The current control scheme was designed in PSIM, the code was generated for the DSP/MCU through PSIM. For the closed loop tests, the FC Converter will regulate the DC bus voltage at 48V. In the closed loop scheme, a reference current value for the output of the FC Converter is provided to the control loop. Two different types of tests are performed to verify the control scheme.

Test 1: Whenever the load connected to the DC bus, requires more current than the reference current value for the output of the FC Converter, the ESS should support, by supplying the rest of the power and keeping the FCS output current, at the reference value. Therefore, keeping the input current of FC Converter (I_Zin) at the desired value (desired value of current at maximum power point of FC).

Test 2: Whenever the DC bus load requires less current than the reference current for the output of the FC Converter, the ESS should absorb power, in order to keep the FCS output current, at the reference value. Therefore, keeping the input current of FC Converter (I_Zin) at the desired value.

Expected results: The input current of FC Converter should remain at the desired value (maximum power point of FC), regardless of the load variation, unless the super capacitor voltage has reached its maximum or minimum voltage limit.

4.4.1 Test 1

For this test the FCS and ESS are connected in parallel, as shown in Figure 4.2. The DC bus voltage is regulated at 48V through FC Converter. The input voltage of FC Converter (Output voltage of FC) is at 28.8V, to match the FC voltage at maximum power point, as shown in Figure 4.4. The reference current value (I_ref) for the output of the FC Converter is kept at 2A in for this test.

Below are the calculations (expected results) for “Test 1”. As one knows that in “Test 1”, load is changed to make the output/load current (I_out) higher than the reference value (I_ref) of current for the output of FCS (output current of FC Converter). In this case, ESS will supply the required extra current, to keep the FCS output current (output current of FC Converter) at the reference value of 2A (maximum power point of FC). Figure 4.8, shows the results of “Test 1”. In Table 4.3, one can see that the results are close to the expected value, which one gets in the calculation below.

Calculations for Test 1:

$$I\_sc = \frac{V\_out \times (I\_out - I\_ref)}{V\_sc}$$

$$I_{sc} = \frac{49.0 \times (3.38 - 2.0)}{31.0} = 2.18A$$

Results:

- 1. V_out: ---- DC bus voltage (HV side)
- 2. V_sc: ---- SC voltage (LV side)
- 3. I_sc: ---- ESS Inductor current
- 4. I_out: ---- Output/load current

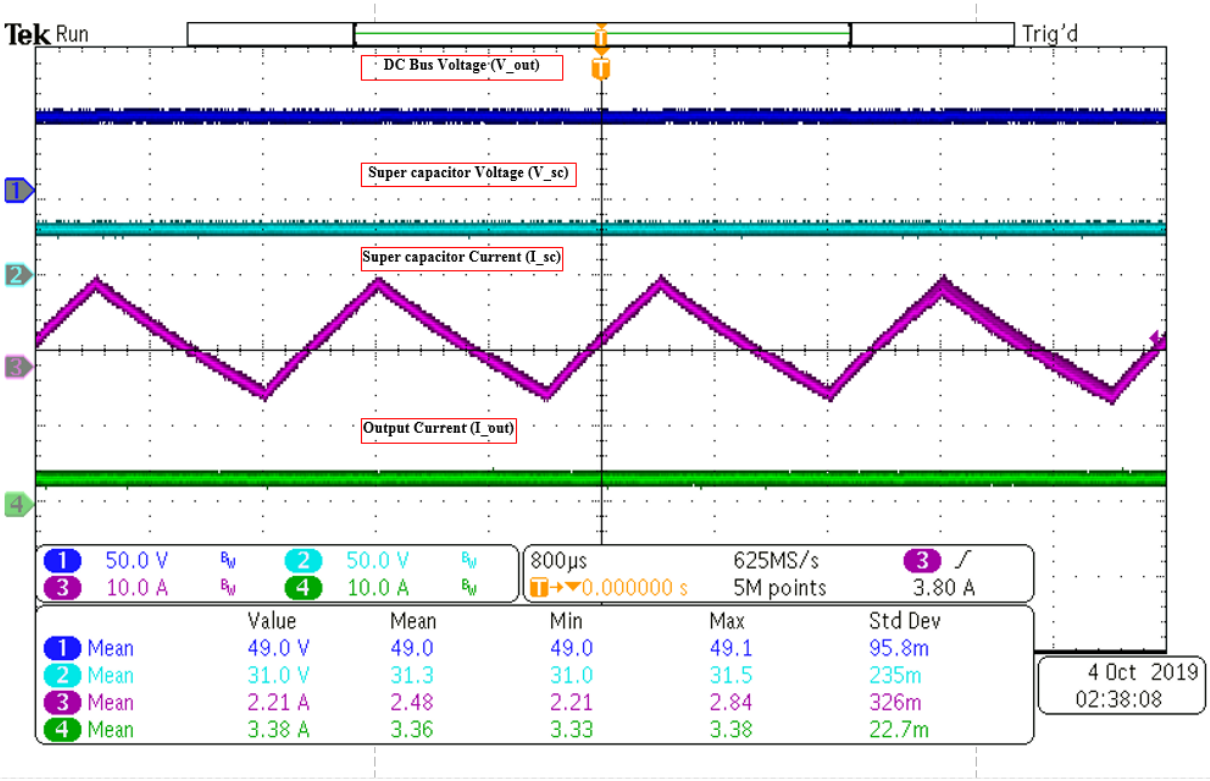

Figure 4.8 Test 1: I_out (Output/Load current) higher than I_ref (Reference for the output of FC Converter)

The results of "Test 1" are shown in Table 4.3.

Table 4.3 Test 1 results

Tests	SC Voltage	DC bus Voltage	ESS Inductor Current	Output Current	Load
Test 1	31.0V	49.0V	2.21A	3.38A	14.5 Ω

In Figure 4.9, one can see the three stages of "Test 1", which are explained below.

- Initially at Stage-1, one can see that the DC bus voltage is regulated at 48V by the FC Converter. Whereas the value of output/load current, (I_out) ≤ 2A. As one knows that the reference current for the output of FC Converter (I_ref) is also 2A. That is why at stage-1, the ESS is not supplying any current because of which the value of super SC Converter (inductor current), (I_sc) ≤ 0A.

- At Stage-2, more load is added. The output/load current (I_out) becomes greater than the reference value (I_ref) for the output current of FCS. Due to the current control scheme, the ESS supplies the rest of the required current, (I_sc > 0A).

- At Stage-3, the extra load is removed. The value of output/load current, (I_out) ≤ 2A. Because of which the value of SC Converter inductor current (I_sc) goes down again, (I_sc) ≤ 0A.

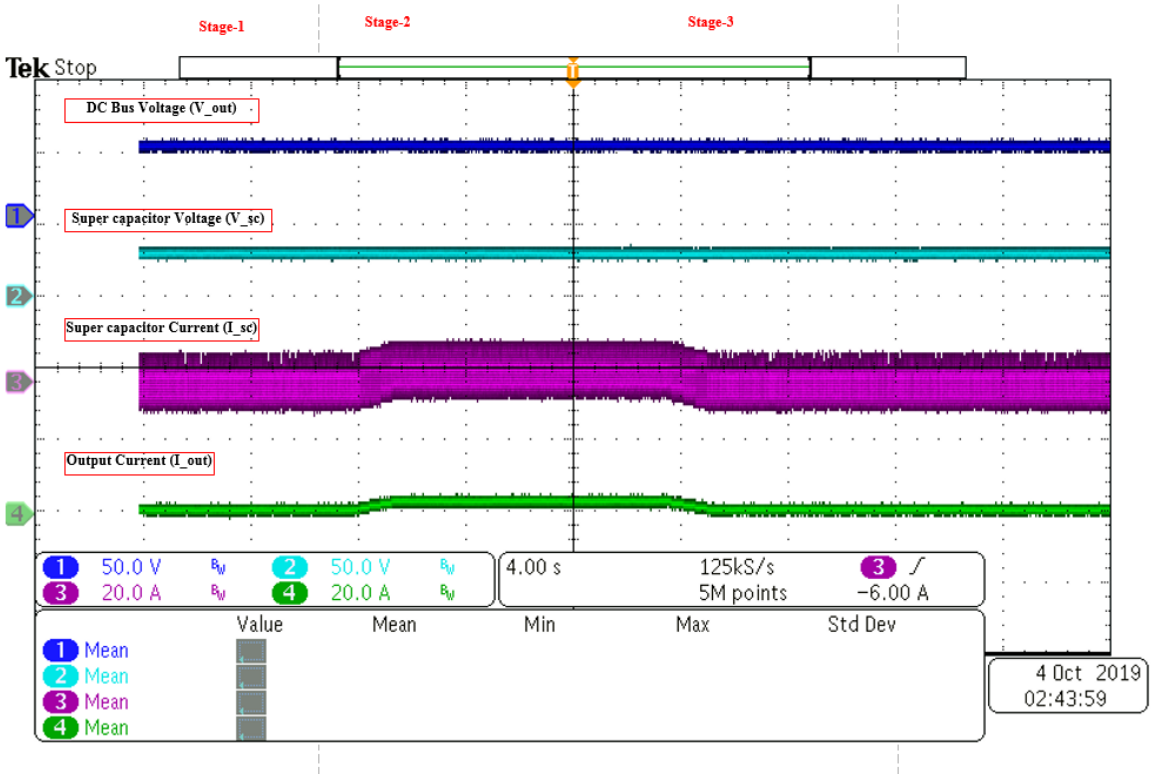

Figure 4.9 Test 1: Transition stage (I_sc (SC current) and I_ out (Output/Load current) comparison)

In Figure 4.10, one can see that during "Test 1", the output/load current (I_out) becomes greater than the reference value (I_ref) for the output current of the FCS. To support the FCS, the ESS supplies the required extra current. One can observe in Figure 4.10, that the output current of FC (I_FC) have not changed during this transition of I_out and it remained at the maximum power point. Similarly, the output voltage of the FC (V_FC) remained at 28.8V (maximum power point).

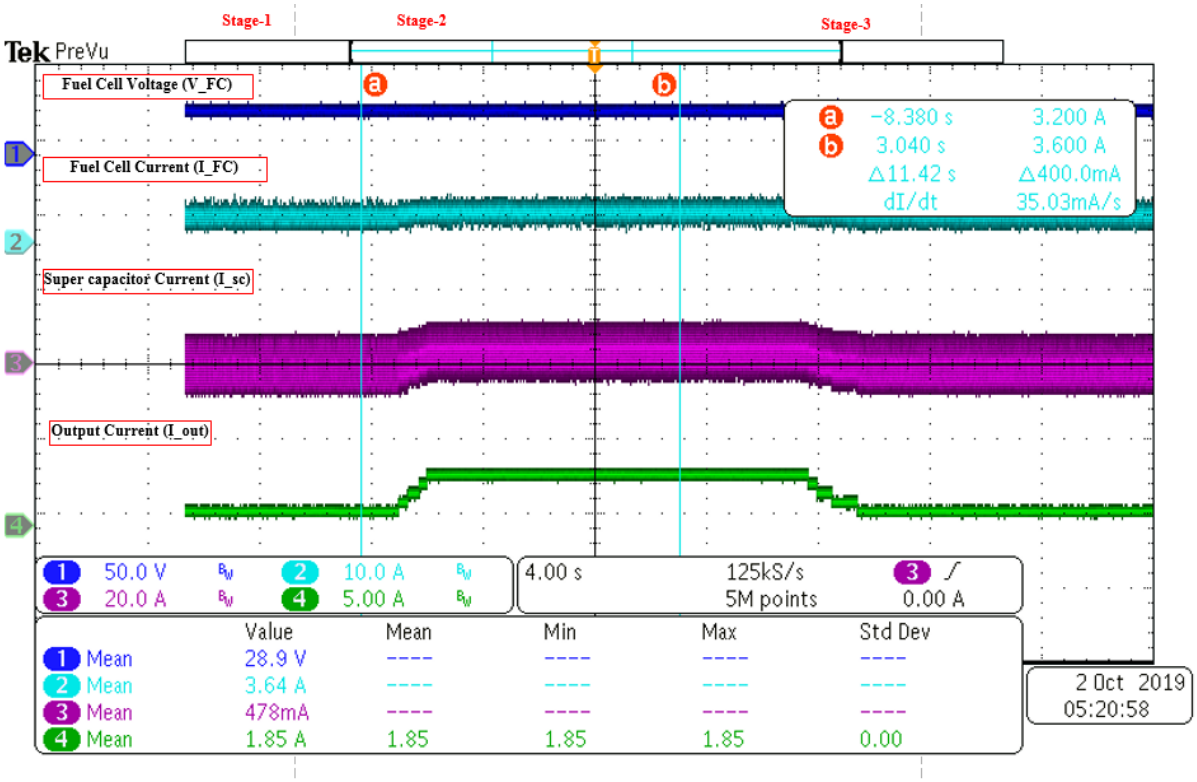

Figure 4.10 Test 1: I_FC (FC output current) and I_ out (Output/Load current) comparison

4.4.2 Test 2

For this test the setup is same as in "Test 1". The reference value of the output of FCS is 2A. Below are the calculations (expected results) for "Test 2". As one knows that in "Test 1", load is changed to make the output/load current (I_out) lower than the reference value (I_ref) of current for the output of FCS (output current of FC Converter). In this case, ESS will absorb the required extra current, to keep the FCS output current (output current of FC Converter) at the reference value of 2A (maximum power point of FC). Figure 4.11, shows the results of "Test 2". In Table 4.4, one can see that the results are close to the expected value, which one gets in the calculation below. In "Test 2", DC bus voltage is 49V.

Calculations for Test 2:

$$I\_sc = \frac{V\_out \times (I\_out - I\_ref)}{V\_sc}$$

$$I_{sc} = \frac{49.0 \times (0.925 - 2.0)}{28.9V} = -1.82A$$

Results:

- 1. V_sc: ---- SC voltage (LV side)
- 2. I_FC: ---- FC output current
- 3. I_sc: ---- ESS Inductor current
- 4. I_out: ---- Output/load current

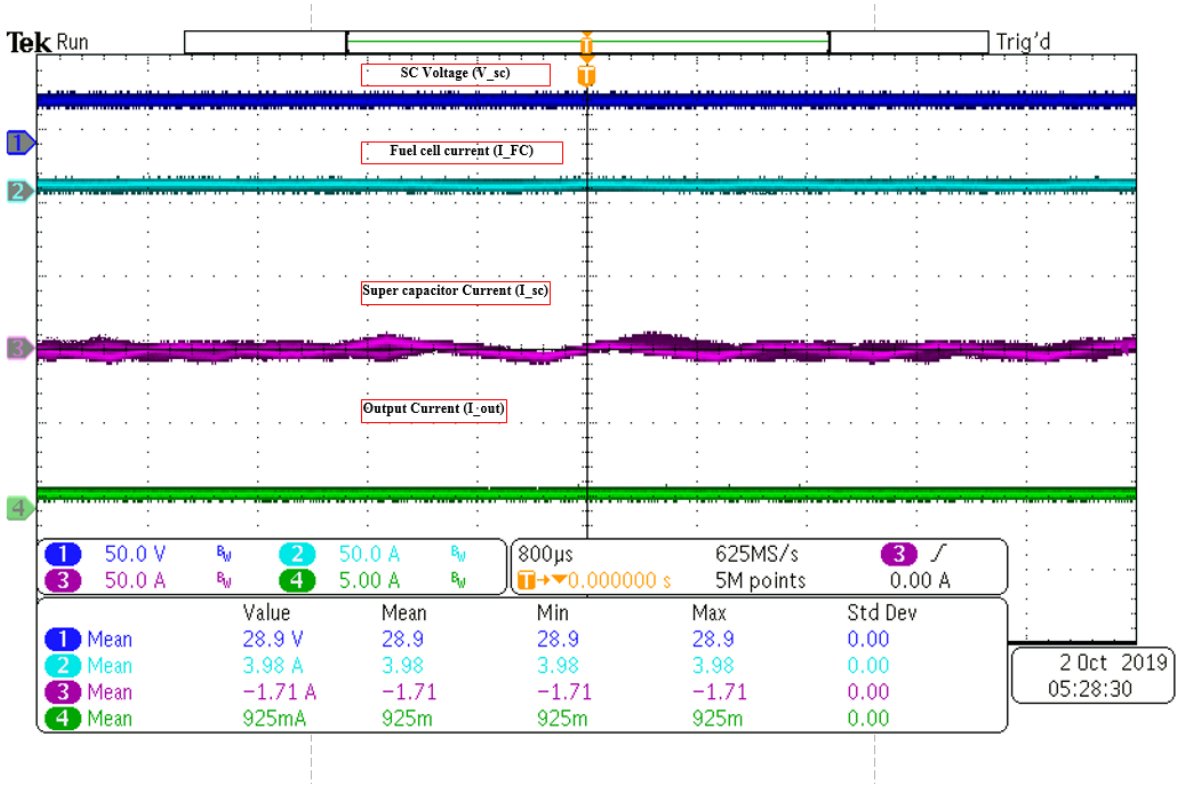

Figure 4.11 Test 2: I_out (Output/Load current) lower than I_ref (Reference for the output of FC Converter)

The results of "Test 2" are shown in Table 4.4.

Table 4.4 Test 2 results

Tests	SC Voltage	DC bus Voltage	ESS Inductor Current	Output Current	Load
Test 2	28.9V	49.0V	-1.71A	925mA	53Ω

In Figure 4.12, one can see the three stages of "Test 2", which are explained below.

- Initially at Stage-1, one can see that the DC bus voltage is regulated at 48V by the FC Converter. Whereas the value of output/load current, (I_out) ≥ 2A. As one knows that the reference current for the output of FC Converter (I_ref) is also 2A. That is why at stage-1, the ESS is not absorbing any current because of which the value of super SC Converter (inductor current), (I_sc) ≥ 0A.

- At Stage-2, output load is reduced. The output/load current (I_out) becomes less than the reference value (I_ref) for the output current of FCS. Due to the current control scheme, the ESS absorbs the rest of the required current, (I_sc < 0A).

- At Stage-3, the load is increased again. The value of the output/load current, (I_out) ≥ 2A. Because of which the value of SC Converter inductor current (I_sc) goes up again, (I_sc) ≥ 0A.

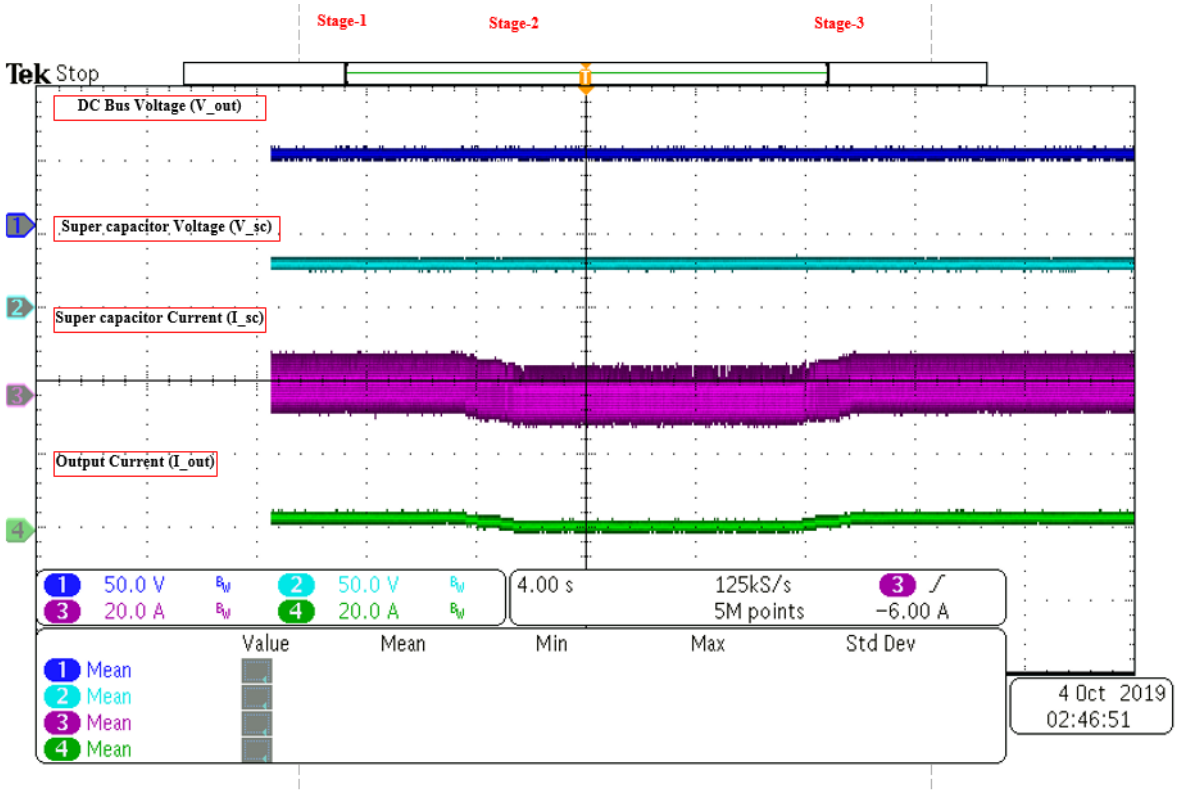

Figure 4.12 Test 2: Transition stage (I_sc (SC current) and I_ out (Output/Load current) comparison)

In Figure 4.13, one can see that during "Test 2", the output/load current (I_out) becomes less than the reference value (I_ref) for the output current of the FCS. To support the FCS, the ESS absorbs the required extra current. One can observe in Figure 4.13, that the output current of FC (I_FC) have not changed during this transition of I_out and it remained at the maximum power point. Similarly, the output voltage of the FC (V_FC) remained at 28.8V (maximum power point).

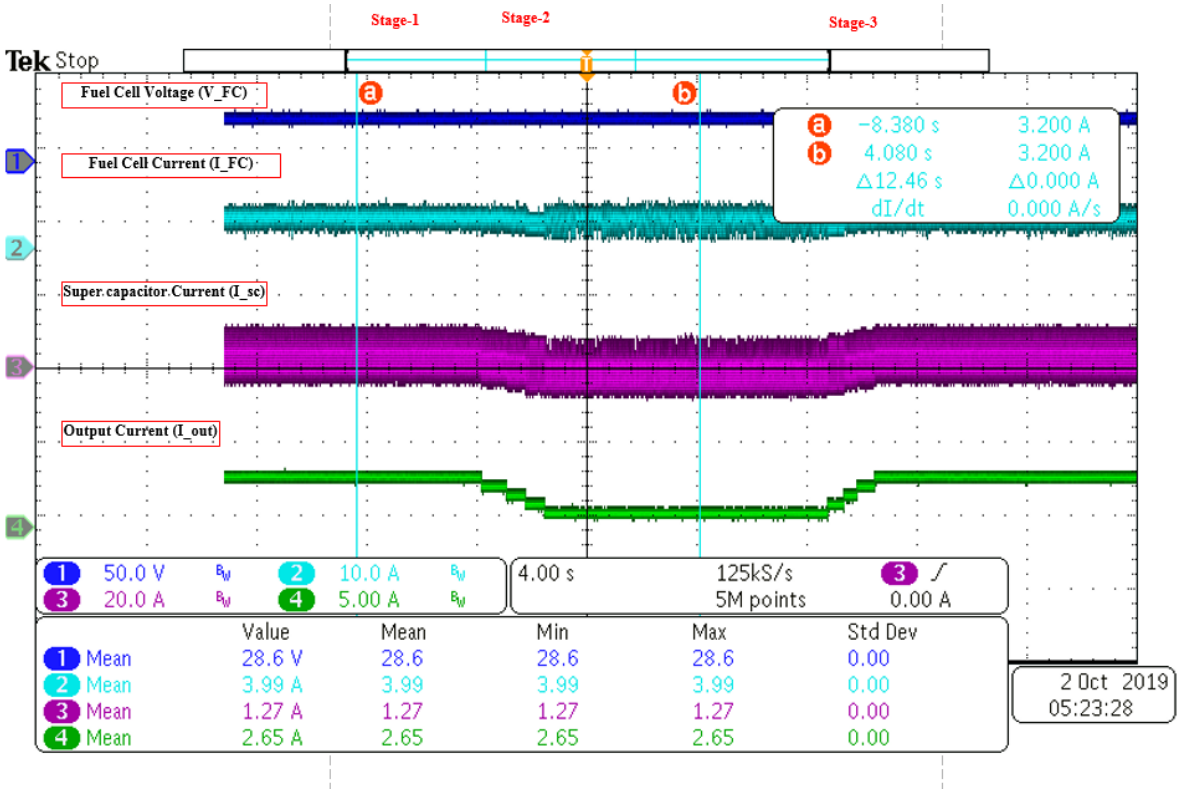

Figure 4.13 Test 2: I_FC (FC output current) and I_ out (Output/Load current) comparison

From "Test 1" and "Test 2", one can see that the ESS supports the FCS. Therefore, the value of output current of the FC (I_FC) does not change, regardless of the load variation. The current control loop is working as expected. The FC will keep operating at the maximum power point, regardless of any change in the output load, until the ESS supports the FCS.

In Figure 4.14, one can see that whenever the output/load current (I_out) is very close the reference value (I_ref) for the output of FCS, the current supplied/absorbed by the ESS (I_sc) will be very close to 0A. Which mean the ESS will neither supply not absorb any current when the output/load current value is at 2A (reference value).

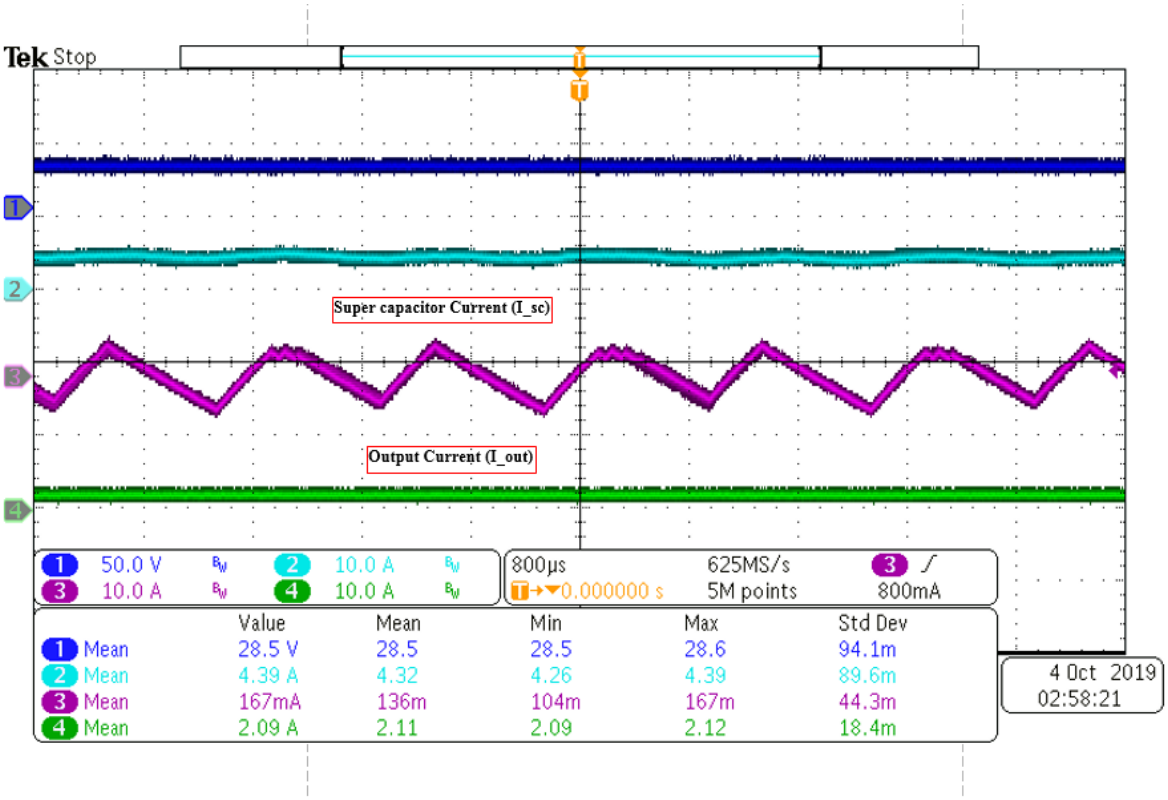

Figure 4.14 I_out (Output/Load current) at I_ref (Reference value for the output of FC Converter)

4.4.3 Super capacitor voltage level control

The current control scheme is verified in "Test 1" and "Test 2". In "Test 2", when the output/load current is less than the reference current value (I_ref) for the FCS (output current of the FC Converter). The super capacitor starts to absorb power, in order to keep the input current of FC Converter (I_Zin) at the desired value (maximum power point for FC). Because of which the voltage in the super capacitor will keep on rising. As explained in Chapter 3, when the super capacitor voltage reaches its upper voltage limit, a voltage control loop will not allow the SC to charge more. Similarly, if the output/load current is more than the reference current value (I_ref) for the FCS (output current of the FC Converter), like in "Test 1", the super capacitor will discharge due to the current control loop. When the voltage in the super capacitor, reaches its lower voltage limit, the SC will stop discharging, because of the voltage control loop. In both of the above scenarios, when the SC voltage is at its upper/lower voltage limit, ESS will not be able to support the FCS. When the SC voltage is between the upper and lower voltage limit, the SC will be supplying/absorbing power from the DC bus, to keep the output current of FCS constant. Therefore, keeping the input current of FC Converter (I_Zin) at the desired value (maximum power point for FC).

When the SC voltage reaches the upper/lower limit, the value of I_Zin will change accordingly. The input voltage of the FC Converter (V_Zin) in the tests below is 28.8V. The test results, to show the SC voltage regulation are provided.

In Figure 4.15, one can see the results of "Test 3". For this test, firstly, the DC bus voltage is regulated at 48V. The output/load current is higher than the reference current value (I_ref) for the output of the FC Converter (I_ref = 2A). ESS is supplying power, to keep the input current of FC Converter (I_Zin) at the desired value (maximum power point for FC). The lower voltage limit of SC, for this test is 30V.

In Figure 4.15, one can see the three stages of "Test 3", which are explained below.

- Initially at Stage-1, the DC bus voltage is regulated at 48V by the FC Converter. Whereas the value of output/load current, (I_out) > 2A. As one knows that the reference current for the output of FC Converter (I_ref) is 2A. That is why at stage-1, the ESS is supplying current to the DC bus, in order to keep the FC output current (I_FC) at the maximum power point. Therefore, (I_sc) > 0A and the SC voltage is decreasing (as SC discharges).

- At Stage-2, the SC voltage reached the lower voltage limit. Because of the voltage control loop of SC, the ESS will stop supplying current to the DC bus. Therefore, (I_sc) = 0A. Because of which the output current of the FC (I_FC) will increase. FC is no longer operating at its maximum power point.

- At Stage-3, the load is decreased. Now, (I_out) < 2A. At this stage, ESS will start absorbing power, in order to support the FCS, (I_sc) < 0A. The FCS output current (output current of FC Converter "I_Zout") will return back to the reference value (2A). FC will start operating at the maximum power point again.

Results:

- 1. V_sc: ---- SC voltage
- 2. I_FC: ---- FC output current
- 3. I_sc: ---- Inductor current (SC Converter)
- 4. I_out: ---- Output current

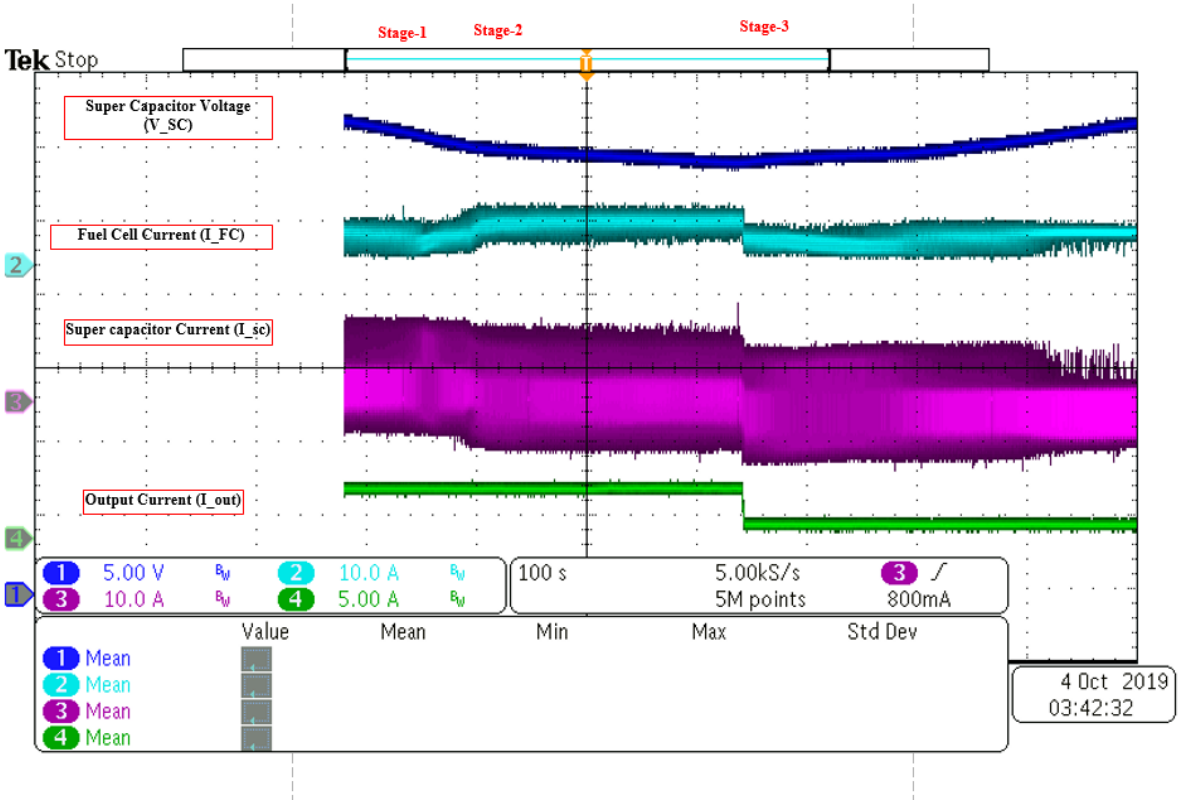

Figure 4.15 Test 3: lower voltage limit of SC

In Figure 4.16, one can see the results of “Test 4”. For this test, firstly, the DC bus voltage is regulated at 48V. The output/load current is lower than the reference current value (I_ref) for the output of the FC Converter (I_ref = 2A). ESS is absorbing current, to keep the input current of FC Converter (I_Zin) at the desired value (maximum power point for FC). The upper voltage limit of SC, for this test is 34V.

In Figure 4.16, one can see the three stages of “Test 4”, which are explained below.

- Initially at Stage-1, the DC bus voltage is regulated at 48V by the FC Converter. Whereas the value of output/load current, (I_out) < 2A. As one knows that the reference current for the output of FC Converter (I_ref) is 2A. That is why at stage-1, the ESS is absorbing current from the DC bus, in order to keep the FC output current (I_FC) at the maximum power point. Therefore, (I_sc) < 0A and the SC voltage is increasing (as SC charges).

- At Stage-2, the SC voltage reached the upper voltage limit. Because of the voltage control loop of SC, the ESS will stop absorbing current from the DC bus. Therefore, (I_sc) = 0A. Because of which the output current of the FC (I_FC) will decrease. FC is no longer operating at its maximum power point.

- At Stage-3, the load is increased. Now, (I_out) > 2A. At this stage, ESS will start supplying power, in order to support the FCS, (I_sc) > 0A. The FCS output current (output current of FC Converter "I_Zout") will return back to the reference value (2A). FC will start operating at the maximum power point again.

Results:

- 1. V_sc: ---- SC voltage
- 2. I_FC: ---- FC output current
- 3. I_sc: ---- Inductor current (SC Converter)
- 4. I_out: ---- Output current

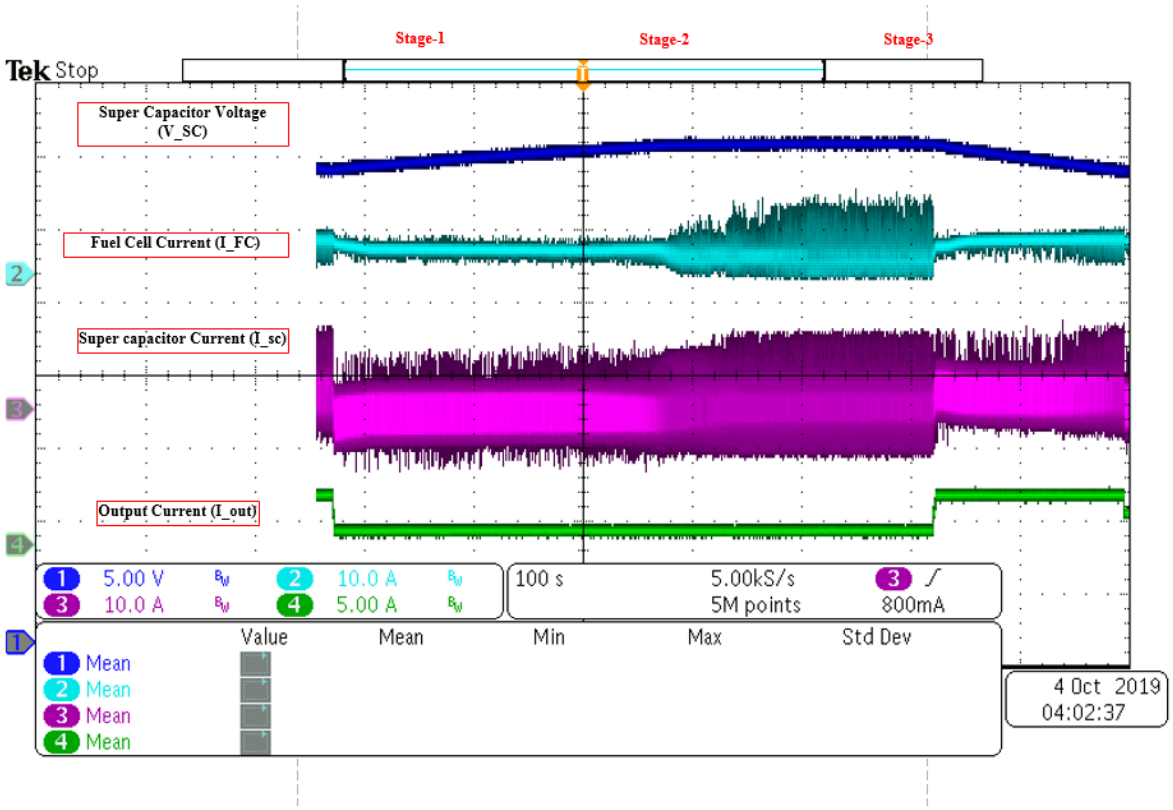

Figure 4.16 Test 4: upper voltage limit of SC

In “Test 3” and “Test 4”, the designed voltage control scheme was tested with the full setup and it worked as expected. In case-1 (Test 3), when the load/output current is higher than the reference current value (I_ref) for the output of the FC Converter (2A), the SC will support the FC by supplying the required extra power, because of the current control loop, due to which the voltage in the SC starts to decrease. When the voltage level of SC reaches its lower voltage limit, the SC will no longer support the FCS by supplying power to the DC bus. Therefore the output current of the FC (input current of FC Converter “I_FC”) will increase and FC will no longer be able to operate at its maximum power point. Similarly in case-2 (Test 4), when the load/output current is less than the reference current value (I_ref) for the output of the FC Converter (2A), the SC will support the FCS by absorbing the extra current, because of the current control loop, due to which the voltage in the SC starts to increase. When the voltage level of SC reaches its upper voltage limit, the SC will no longer support the FCS by absorbing power from the DC bus. Therefore the output current of the FC (input current of FC Converter “I_FC”) will decrease and FC will not be able to operate at its maximum power point. In both cases, whenever the output/load current goes

close to the reference value (2A), a slow voltage control loop will bring the voltage level of the SC to 32V (base voltage level), to support the FCS, whenever required.

4.5 Summary

The proposed current and voltage control scheme for the SC converter supporting the FC converter in the DC nanogrid is implemented and its performance is reported in this Chapter. The performance of the current and voltage control scheme is also verified by showing the experimental results. The voltage of the DC bus was regulated at 48V through the FC Converter. The output current of the DC power supply (in place of Fuel cell) remained at the maximum power point, in all the tests, while the voltage of the SC is within the upper and lower voltage limit. Whenever the voltage of SC, reaches the upper or lower voltage limit, the ESS can no longer support the FCS. In which case, the output current (the input current of the FC Converter "I_FC") of the power supply (in place of Fuel cell), will not remain at the desired value (maximum power point). When the SC voltage reached the upper voltage limit, the voltage regulation loop stops any further charging of the SC. Similarly, when the voltage of the SC reached the lower voltage limit, the voltage control loop, stops any further discharging of SC. In order to support the FCS when required, a slow voltage control loop will bring the voltage level of the SC to 32V (base voltage level), whenever the output/load current goes close to the reference value (2A). In the next Chapter, the conclusions of this work and the guidelines for future work are presented.

Chapter 5 Conclusions

5.1 Summary

This Thesis presented a control scheme that enables the FC system to operate at it maximum power point by using ESS based on a super capacitor, which is connected in shunt with the FCS. A current control scheme, enables the ESS to supply/absorb power from the DC bus, in order to support the FCS. By keeping the output current of FC constant (at the maximum power point). Moreover, a voltage control scheme is also implemented, in order to keep the voltage of the SC within the maximum/minimum voltage limits.

In Chapter 2, the power and control circuitry of the Fuel cell interface, i.e. the FC Converter, is presented, which is required for the voltage regulation in the DC bus. The ESS has to supply/absorb power from the DC bus, therefore a bi-directional DC-DC converter is used to interface the storage unit with the DC bus. The design of a bi-directional DC-DC converter as interface for the SC unit (storage unit), is also presented in Chapter 2. Calculations were made for the required inductors and capacitors for the power electronic converter. The gate driver circuitry for MOSFETs and the circuitry for implementation of current and voltage sensors is presented. The primary goal of this converter is to control the injected/absorbed current in the DC bus, so as to support the fuel cell converter, and to keep the voltage of the supercapacitor within safe limits.

The control scheme for the fuel cell current and voltage control of the super capacitor was developed and presented in Chapter 3. The FC Converter power and control circuit was implemented in PSIM and the simulation results of FC Converter were verified. The PI controller for the injected/absorbed current by the super capacitor, in order to make the fuel cell operate at the maximum power point, was designed. The reference current (for the output of FC Converter), at which the fuel cell is at its maximum power point, is provided to the PI current control loop. When the output/load current is greater than the reference value (for the output current of FC Converter), the super capacitor will inject current in the DC bus, because of the current control loop. Similarly, when the output/load current is less than the reference current value, the current control loop will make the super capacitor absorb power from the DC bus, in order to make the fuel cell operate at the maximum power point. Simulation results for the current control loop were

also presented, which shows that the fuel cell is operating at the maximum power point, regardless of the load variation. The design of a PI control loop, for the voltage control in the super capacitor was also presented. The voltage control loop ensures that the voltage of the super capacitor does not rise above the maximum voltage limit or fall below the minimum voltage limit of super capacitor. The voltage control strategy for super capacitor is presented. From the presented simulation results in Chapter 3, it is observed that, both current and voltage controllers show good performance, and expected results were obtained.

In Chapter 4, a laboratory-scale hardware based DC power system was developed to experimentally verify the effectiveness of the developed current and voltage control scheme for a DC nanogrid with energy storage system (ESS). Complete details of the circuits and systems used in the experimental set-up were shown and described in this Chapter. Finally, experimental results were presented for all the cases. The results have shown that the developed current and voltage control schemes were accurate, the super capacitor supplies and absorbs power, whenever the output/load current is higher or lower than the reference value (for the output current of FC Converter), in order to make the fuel cell operate at the maximum power point. The voltage in the super capacitor does not rises above the maximum voltage limit or falls below the minimum voltage limit of the super capacitor, because of the voltage control scheme. In chapter 4, one can see that the experimental results are very similar to the simulation results.

A current and voltage control scheme, in order to make the fuel cell operate at the maximum power point, was the main goal of this work. As shown in this Thesis, a control scheme with this criteria was successfully designed and accomplished.

5.2 Future work

A lot of research needs to be done in this field especially for the effective utilization of the power generated by the fuel cell. Some of the suggestions for future work related to this study are as follows:

- Most of the energy generated by the fuel cell is dissipated in the form of heat. One of the potential future works is to develop a system, where the fuel cell is working at the maximum power point and the heat generated by the fuel cell is also utilized.

- Develop a hybrid energy storage system for the fuel cell, to make it operate at the maximum power point for longer intervals, because the super capacitor cannot support the fuel cell, by continuously supplying or absorbing power, for very long intervals.
- The current and voltage control scheme has been verified experimentally at the low voltage, low power level. These results give confidence that the control scheme can also be tested for a higher voltage and power level in the further research work.

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