Analysis and Design of High Efficiency Grid-to-Vehicle (G2V) Plug-in Chargers for Local e-Transportation

Abhinandan Dixit

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By: Abhinandan Dixit

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Signed by the final examining committee:

_____ Chair
Dr. Sébastien Le Beux

_____ External Examiner
Dr. Ilamparithi T.Chelvan

_____ Examiner
Dr. Sébastien Le Beux

_____ Supervisor
Dr. Akshay Kumar Rathore

Approved by: _____
Dr. Yousef R. Shayan, Chair
Department of Electrical and Computer Engineering

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Gina Cody School of Engineering and Computer Science

ABSTRACT

Analysis and Design of High Efficiency Grid-to-Vehicle (G2V) Plug-in Chargers for Local e-Transportation

Abhinandan Dixit, MASc.

Concordia University, 2020

Electric transportation worldwide has witnessed a tremendous increase in the use of electric vehicles (EV's) due to increased awareness of environmental issues. Road EV's compromise a broad spectrum of vehicles right from two-wheelers three-wheelers (rickshaws/Auto/Trio), cars and electric buses. E-Rickshaw has gained popularity in the Asian market post-2010 because of their symbolic resemblance with traditional auto-rickshaw. The fast growth of the market is principally pushed by the low ownership cost of electric three-wheelers, falling battery prices, and favorable government policies and support. These EVs run on low-cost 48 V, 120 Ah lead acid battery packs having low depth-of-discharge (DOD). Hence, frequent battery charging becomes essential for such EVs. Conventional battery chargers available in the market utilize flyback converter based topologies in order to charge such battery packs. On one hand such battery chargers are easy to implement, these topologies fail to achieve unity power factor (UPF) operation leading to high total harmonic distortion (THD) and poor input power quality at the input. Thus active power factor correction (PFC) becomes a vital constituent in AC-DC converters. By understanding the constraints posed by continuous current mode (CCM) based battery chargers, the proposed converters are designed to operate in discontinuous current mode (DCM) because of its evident benefits such as inherent PFC, zero current turn-on and zero diode reverse recovery losses. By omitting sensors at the input and utilizing only the output sensors, regulated voltage or current can be obtained which makes the system cost-effective and improves its reliability and robustness to high frequency noise.

This thesis presents both isolated and non-isolated battery charger for local e-transportation EVs utilizing 48 V lead acid battery pack. At first, a non-isolated single-stage interleaved buck-boost float charger is proposed by considering the advantages such as reduced current stresses, minimum

number of semiconductor devices and absence of bulky high frequency transformer. DCM operation of the proposed converter ensure UPF operation for variable input voltage and utilizing just a single sensor makes this charger configuration economical and easyto implement. However, such a configuration had high current stress on the semiconductor devices leading to increased thermal requirement and reduced efficiency at light loads. Thus addressing these problems, a high efficiency two-stage battery charger is proposed. The battery charger uses an interleaved DCM buck-boost converter in order to achieve PFC at variable input voltage, whereas the second stage is an unregulated half-bridge LLC resonant converter which provides isolation as well as soft-switching for the primary switches. Synchronous rectification (SR) along with only capacitive filter is used on center tapped transformer secondary to improve converter efficiency. Due to DCM of the front-end AC-DC converter achieves zero current turn-on of the switches and DC-DC converter switches achieve zero voltage turn-on because of the LLC resonant. The proposed battery charger implements constant current (CC) and constant voltage (CV) method of charging using simple PI controllers, thus making it suitable for commercial use. Small signal models for both the battery charger configurations are developed using the current injected equivalent circuit approach and a detailed controller design is illustrated. Simulation results using PSIM11.1 software and experimental results from proof-of-concept laboratory hardware prototypes are provided in order to validate the reported analysis and design which demonstrates their performance.

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List of Abbreviations

EVs	Electric Vehicles
PHEV	Plug-in Hybrid Electric Vehicle
OBCs	On-board Battery Charger
BMS	Battery Management System
PFC	Power Factor Correction (or Corrected)
THD	Total Harmonic Distortion
EMI	Electromagnetic Interference
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
AC	Alternating Current
DC	Direct Current
LLC	Inductor-Inductor-Capacitor
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching
UPF	Unity Power Factor
kW	Kilo-Watt
CC	Constant Current
CV	Constant Voltage
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
CIECA	Current Injected Equivalent Circuit Approach
RMS	Root Mean Square
ms	Millisecond
PF	Power Factor
FFT	Fast Fourier Transform
G2V	Grid to Vehicle
V2G	Vehicle to Grid

SOC	State-of-Charge
DOD	Depth-of-Discharge
ATV	All Terrain Vehicles
IC	Internal Combustion
RCD	Resistor Capacitor Diode
LC	Inductor Capacitor
PLL	Phase-locked-loop
CSI	Common Source Inductance

List of Symbols

$v_{in} = V_{in,pk}\sin(\omega t)$	Line input voltage
$i_{in} = i_{in,pk}\sin(\omega t)$	Line input current
$L_1 = L_2 = L$	DCM buck-boost inductor
$i_{Lk,pk_{k=1,2}}$	Peak inductor current
$i_{o,avg}$	Average output current in one switching cycle
K_{crit}	Critical Conduction Parameter
R_{crit}	Critical Load Resistance
K_{cond}	Conduction Parameter
$C = C_o$	Output capacitor
f_c	Cut-off frequency
L_f, C_f	Filter inductor and capacitor
L_o	Output inductor
P_o	Output power
$I_{o,BB} = I_{o,avg}$	Buck-boost average output current
$V_{dc,link}$	DC-link voltage
D	Duty cycle
V_o	Converter output voltage
$T_{sw_{kB,k=H,B}}$	Switching time period of buck-boost or half-bridge converter
$1:n:n$	Transformer turns ratio
M	Buck-boost converter gain
$R_{D,bridge}$	Diode bridge resistance for one leg
$V_{f,d}$	Forward voltage for diode bridge
L_{para}	Parasitic inductance
$V_{g,eff}$	Effective gate voltage
$V_{g,off}$	Turn-off gate voltage
V_{miller}	Miller Plateau Voltage
$C_{j,D}$	Diode junction capacitance
DT_s	Switch On-Time
D	Duty Cycle

$I_{sw,rms}$	Switch rms current
$I_{d,rms,avg}$	Diode rms and average current
$I_{g_k,off,k=1,2,\ldots}$	Gate current during turn off
$C_{oss,kB,k=H,B}$	MOSFET Output capacitance
v_{sw}	Switch Voltage stress
$I_{SW_{BB},rms}$	Buck-boost switch RMS current
$R_{DS,on,kB,k=H,B,SR}$	Switch drain-to-source on resistance
$P_{c,limit}$	Inductor core loss limit, mW/cm^3
V_e	Effective core volume, cm^3
$I_{d,rms}$	Diode RMS current
$I_{d,rms}$	Diode average current
V_f	Buck-boost diode forward voltage
R_d	Buck-boost diode resistance
$I_{C_{dc,link},rms}$	DC-link capacitor rms current
$R_{C_{dc,link}ESR}$	DC-link capacitor ESR
R_L	Load resistance
$i_r(t)$	Resonant current
i_{L_m}	Magnetizing current
L_m	Transformer magnetizing inductance
T_{dead}	Dead-time for back-end switches
L_r	Resonant inductor
L_{lk}	Transformer leakage inductance
$C_{r_1} = C_{r_2}$	Resonant capacitor
$I_{sw_k,rms;k=BE,SR}$	Back-end switch current
R_{DCR}	DC winding resistance
$I_{L,rms}$	Buck-boost inductor RMS current

$I_{C_o,rms}$	Output capacitor ripple current
$R_{C_{o,ESR}}$	Output capacitor equivalent series resistance
R_P	Self-discharge resistance
R_{int}	Battery internal resistance
V_{batt}	Battery voltage
$R_{g,switch}$	MOSFET switch resistance
$R_{g,driver}$	Gate driver resistance

Chapter 1: Introduction

1.1 Introduction

With growing environmental concerns and increased emissions the world is moving towards electrification in every industrial sector. The automotive industry is one of them to observe a rapid growth where the internal combustion (IC) engines are being replaced by the electric motors. Electric motors are a viable option because of their higher efficiency and robustness. Fig. 1.1 shows a comparison between the classical IC engine vehicle and electric vehicles (EVs) [1]. It is observed that EVs are a realistic solution to offer reduced maintenance cost, better fuel economy, and limits CO_2 emissions as compared to the classical IC engines. Electrification of not only the private vehicles but also of the local transport vehicles has seen a major boom recently. One of the major parts of local transport is an inverter which is supplied from a battery pack to propel the electric motor and the vehicle. EVs can be classified into three major categories as two-wheelers, three-wheelers, and four-wheelers. Two-wheelers are used mostly in personal transportation and currently for delivery service, whereas three-wheelers are used for short range local mobility, along with four-wheelers that are mainly used as personal and passenger vehicles for higher range. Three wheeler vehicles have become popular in Asian market because of its cheap price and high robustness. In Thailand and India these three wheelers are commonly known as tuk-tuk or e-rickshaws [2] and have evolved from IC engine vehicles to full-electric vehicles. Small four-wheeler such as golf carts and all terrain vehicles (ATVs) have also gone full electric to reduce the size and increase efficiency. These vehicles are comparatively cheaper as they are hauled by 850 W motors which are powered by low voltage battery packs of 48 V, 120 Ah lead-acid batteries. As the depth-of-discharge for these lead-acid battery packs is only 20% battery packs require to be charged often [3]. Thus a charger becomes a fundamental component for these vehicles. Charging these battery packs without compromising with the IEEE standards of low total harmonic distortion (THD) is an essential requirement.

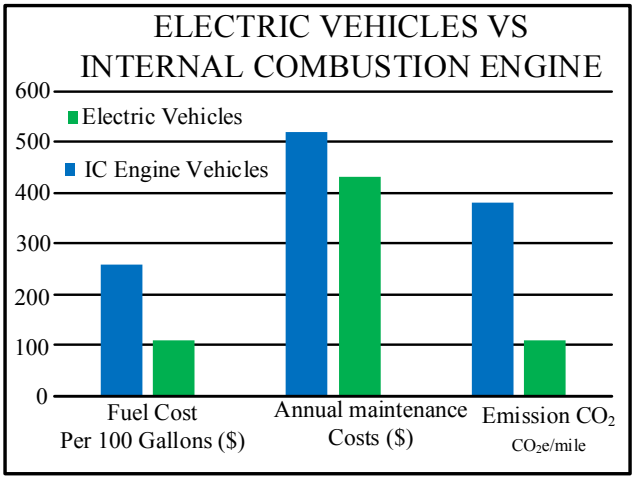


Fig. 1.1 Comparison between EV and IC engines.

1.2 Literature Review

In this Section, a detailed overview of various types of battery charging methods and conventional charging topologies is presented.

1.2.1 Types of Battery Chargers

Fig. 1.2 shows the classification of battery chargers. Battery chargers can be broadly classified into two categories i.e. plug-in chargers and wireless chargers. Wireless chargers are

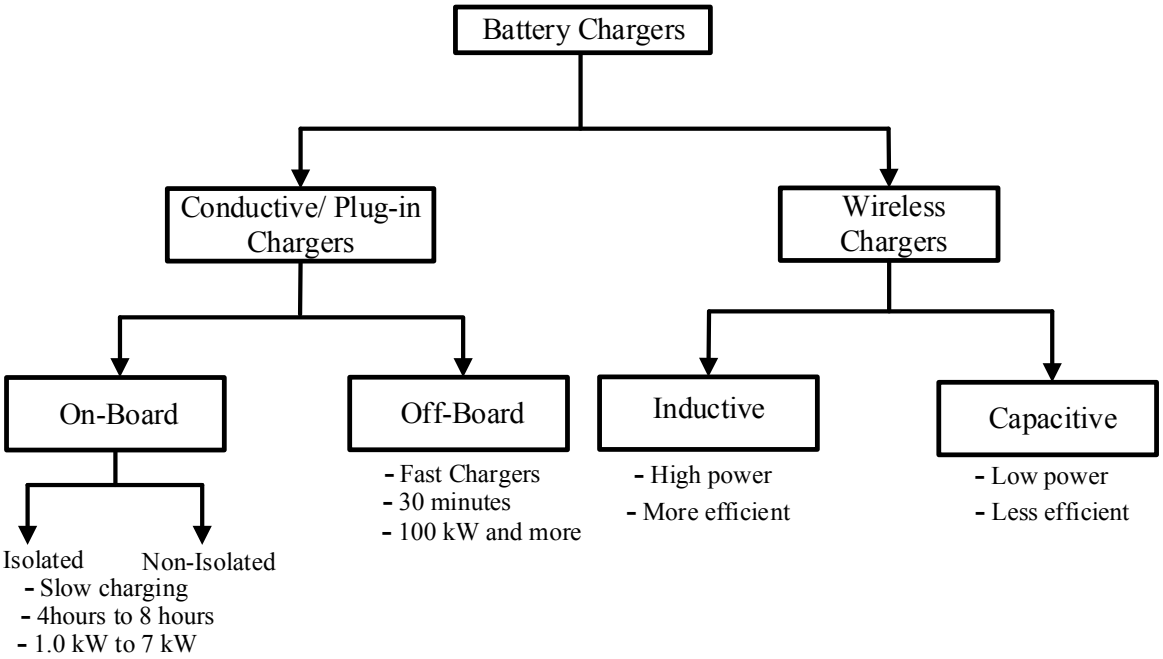


Fig. 1.2 Battery charger classification.

comparatively lesser in use due to lower efficiency and complex design. Plug-in chargers are one the most popular and are currently in practice because of their higher efficiency and simpler design. Off-board chargers are usually fast chargers and require a dedicated power system to charge batteries at high power whereas on-board chargers are relatively slow chargers and can be used when plugged in AC mains. On-board chargers are further classified into isolated and non-isolated topologies. As there is no such requirement in standards for safety of EVs as specified in SAEJ1772 (from the North American standard for electrical connectors for EVs maintained by the Society of Automotive Engineers). Furthermore, there is no electrical reason that the battery should be isolated from ac input power, because its ground is generally floating with the body ground of the vehicle [11]. Non-isolated topologies have low component count and thus achieve higher efficiencies as compared to isolated topologies [4]. Isolated topologies can be further segregated into single-stage and two-stage topologies. Several single-stage isolated topologies have been reported in the literature but deal with poor efficiency due to the transformer leakage inductance [5]. Other topologies present complex control algorithms to implement power factor correction (PFC) which increase the computational burden on the microcontroller [6]. Two-stage non-isolated configurations have also been reported [6] but such topologies increase switch count and system losses.

1.2.2 Battery Charger Architectures

Several battery charger topologies for charging high-voltage battery packs (450 V-650 V) and low voltage battery packs (48 V-72 V) have been proposed in the literature [7], [8]. High voltage

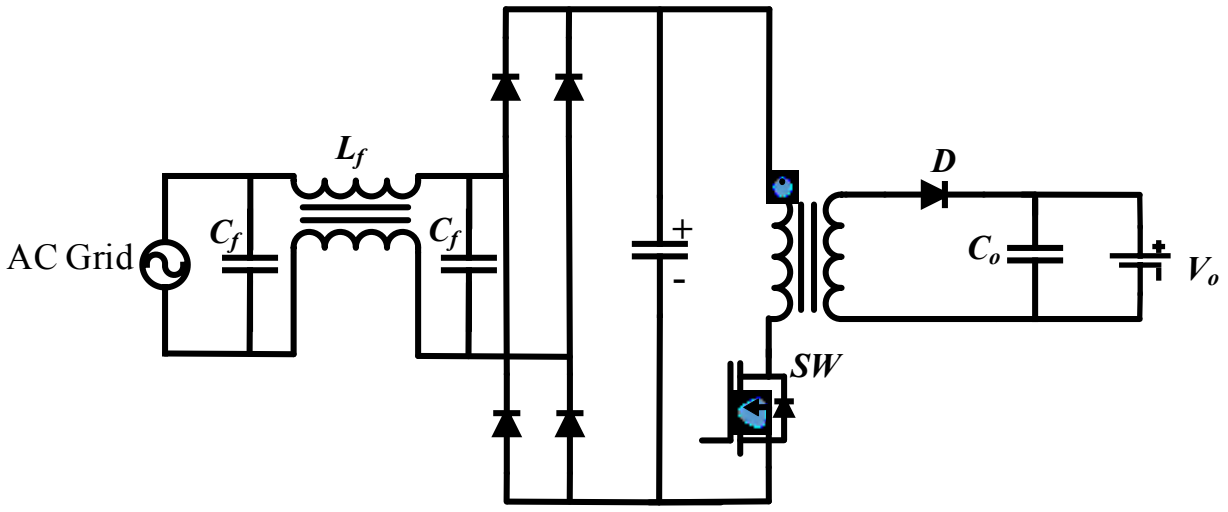


Fig. 1.3 Fly-back converter based battery charger.

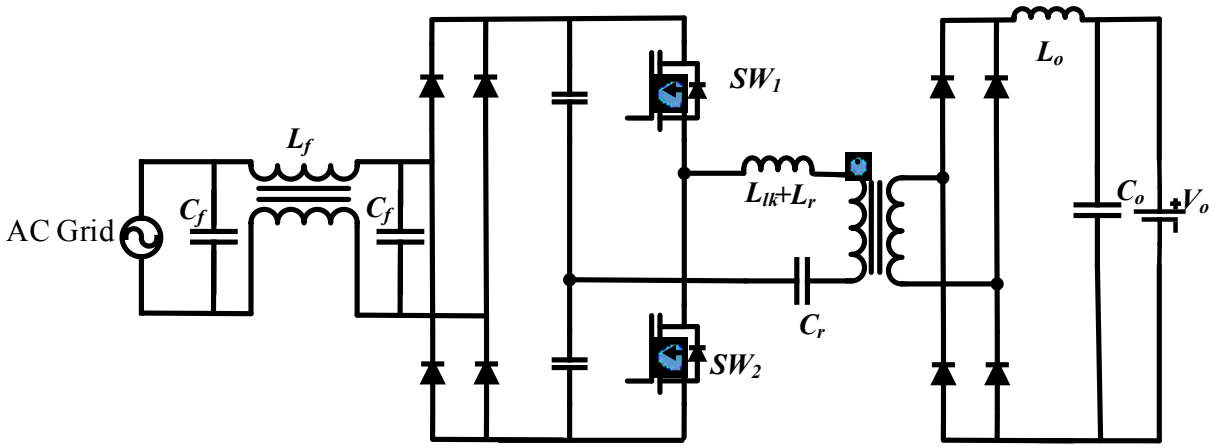


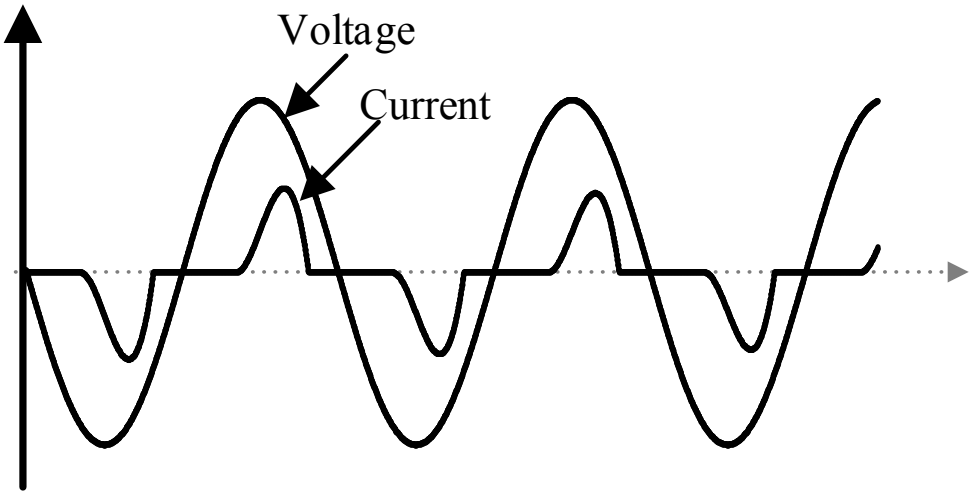
Fig. 1.4 Half-bridge series resonant converter based battery charger.

lithium-ion battery packs are used for sophisticated EVs like Tesla and Toyota and lead-acid based low voltage battery packs are used for e-rickshaws, golf carts, airport movers and fork-lifts. Battery chargers employed for such low-voltage battery packs are not refined in order to cut down the cost of such systems. One of the most common topologies used for charging such battery packs is shown in Fig .1.3 [9]. One of the main drawbacks of using such topologies is the effect of leakage inductance on the switch voltage. During turn-off of the switch *SW*, the leakage inductance of the high-frequency transformer is discharged and hence gives a voltage spike across the switch. External RCD snubber is connected to dissipate this energy and to clamp the switch voltage leading to, losses [10]. Moreover, connecting diode at the secondary for the low voltage battery charging application induces high conduction and turn-on losses for the diode leading to reduced efficiency. Though the topology is simple and easy to implement, it lacks the basic requirement of achieving unity power factor (UPF) for various line voltages. Such topology presents poor power factor and THD as no active current wave shaping unit is present [9]. An improved version for a low voltage battery charger that is available in the market and is shown in Fig. 1.4. It is seen that though losses due to leakage inductance do not occur due to soft switching achieved because series resonant tank, poor efficiency due to the output diode bridge rectifier losses is one of the main issues. Also such battery charger configuration lacks PFC unit, which induces odd harmonics in the grid leading to poor power quality. The presence of an LC filter at the transformer secondary induces duty cycle loss on transformer primary voltage. As the output of the inductor does not allow a sudden change in current, secondary diodes are shorted that leads to duty cycle loss and rectifier snubber losses

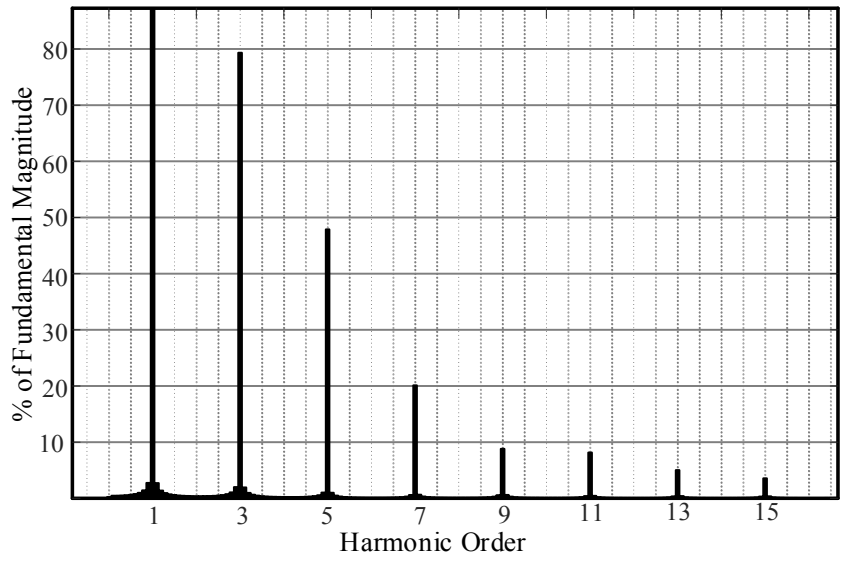
[11]. It is observed that such a PFC unit becomes essential for chargers in order to improve power quality at the input and enhance converter performance.

The above-mentioned charger configurations come in the category of float chargers [7] [8]. Such chargers are easy to implement in terms of control with one control loop to control the charging battery. Float chargers require current limiting resistors at the output and use a single sensor, making them a less complicated solution for battery charging.

1.2.2.1 AC-DC Converters



(a)



(b)

Fig. 1.5 (a) Diode bridge voltage and current waveform. (b) Input current THD.

AC-DC converters are an essential part of the battery chargers in order to convert AC voltage to stiff DC. Diode rectification is one of the most common ways which is implemented in current chargers but draws discontinuous peaky current. Input current waveform and FFT analysis with diode rectification-based chargers is shown in Fig. 1.5(a) and Fig. 1.5(b). It is seen that odd harmonics are injected in the grid leading to poor input current THD and reduced power quality. Such battery chargers require a bulky passive filter to filter out these harmonics leading to increased weight and size. As per IEC-6000-3-2 [12], the input current THD limit should be below 5% for automobile battery chargers.

The PFC control objectives can be defined as follows:

1.) Sinusoidal input current is in-phase with the input voltage over a range of frequencies.

2.) Low input current THD over entire range of power.

3.) Stiff Regulated DC output voltage.

Thus an active PFC becomes an essential need for battery charging application in order to meet the above mention control objectives. In order to reduce the cost and the weight single-stage, isolated, and non-isolated charger configurations have been developed [13]. Such chargers don't require a dedicated second stage for charging, which reduces cost and improves efficiency. Isolated single-stage topologies present poor efficiencies because of losses due to leakage inductance. Huge voltage spikes at turn-off reduce reliability and require an RCD snubber which reduces the efficiency drastically [14]-[27]. Secondary converters and control schemes are developed in order to improve the efficiencies of such topologies [28]. On the other hand, non-isolated topologies possess no such problems owing to the absence of high-frequency transformer, thus presenting higher efficiencies. But deal with the problem of an increased number of semiconductor count and sensors, which increases the cost greatly. Two-stage battery charging topologies have been popular

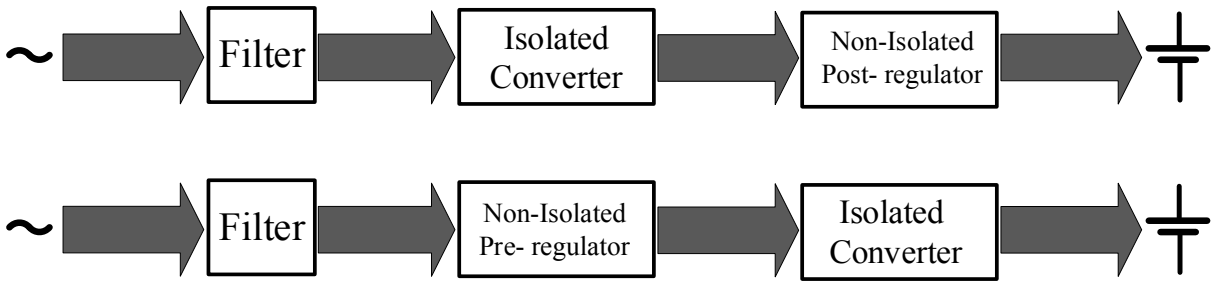


Fig. 1.6 Two types of proposed concept.

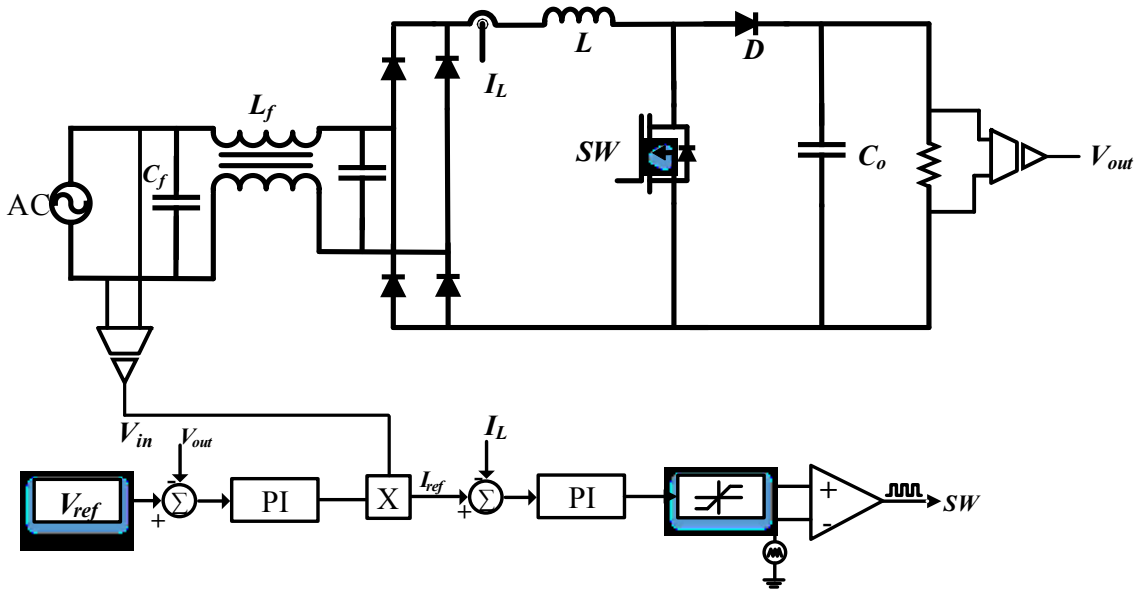


Fig. 1.7 Boost converter as pre-regulator in CCM

in industries and have one stage dedicated to PFC regulation and the second stage for battery charging control [29]. As shown in Fig. 1.6 such battery charger can have two configurations:

1. Post-regulator type
2. Pre-Regulator type

In a post-regulator configuration, an isolated converter is used to provide isolation from AC mains and a non-isolated converter to shape the input current and control the battery charging process. Such a battery charging configuration has been reported in [30] but presents comparatively less efficiency as the primary side switches have high conduction losses. Moreover such a topology is not suited for charging low voltage battery packs as the current wave-shaping unit has high conduction and switching losses. On the other hand, a pre-regulator configuration [31]-[35] has the non-isolated converter is used to shape the input current in order to achieve UPF and an isolated converter to control the battery charging process. This configuration is more reliable and is used in current battery chargers.

The most commonly used pre-regulator topology for such an implementation is the use of boost converter because of its simple structure and grounded FET as shown in Fig. 1.7 [35]. Boost inductors are operated in CCM and control is designed in order to shape this inductor current sinusoidal. Inductor current can be shaped in three ways mainly peak current control, average current control, and hysteresis control. These control techniques require sensing of input current

for wave shaping and input voltage in order to synchronize with the grid. Fig. 1.7 shows the circuit and control of a boost converter for active PFC. To implement such control it requires two control loops; the outer loop to regulate the output voltage and inner loop to shape input current by maintaining UPF. Such control strategies have been extended to various topologies like SEPIC converter but deal with issues like increased component count leading to higher losses. Interleaved boost converter has also been presented [32] [33] to reduce the size of the input filter and reduce current stress through the switches. CCM based converters can be extended to various bridgeless topologies as shown in Fig. 1.8 [36]. The input diode bridge is eliminated in order to reduce losses due to the diode forward voltage drop and achieve higher efficiency. Such converters require a bulky isolated transformer for input voltage and current sensing in order to implement phase-locked loop (PLL) for grid synchronization, which increases the cost and weight of the system significantly. It is observed that in a total of three sensors or in some cases four are used to achieve control goals. Moreover, sophisticated microcontrollers are required in order to sample high-frequency data, leading to reduced reliability and converter robustness. In the prospect of control and cost, such converters present high complexity as it requires to determine the phase angle for

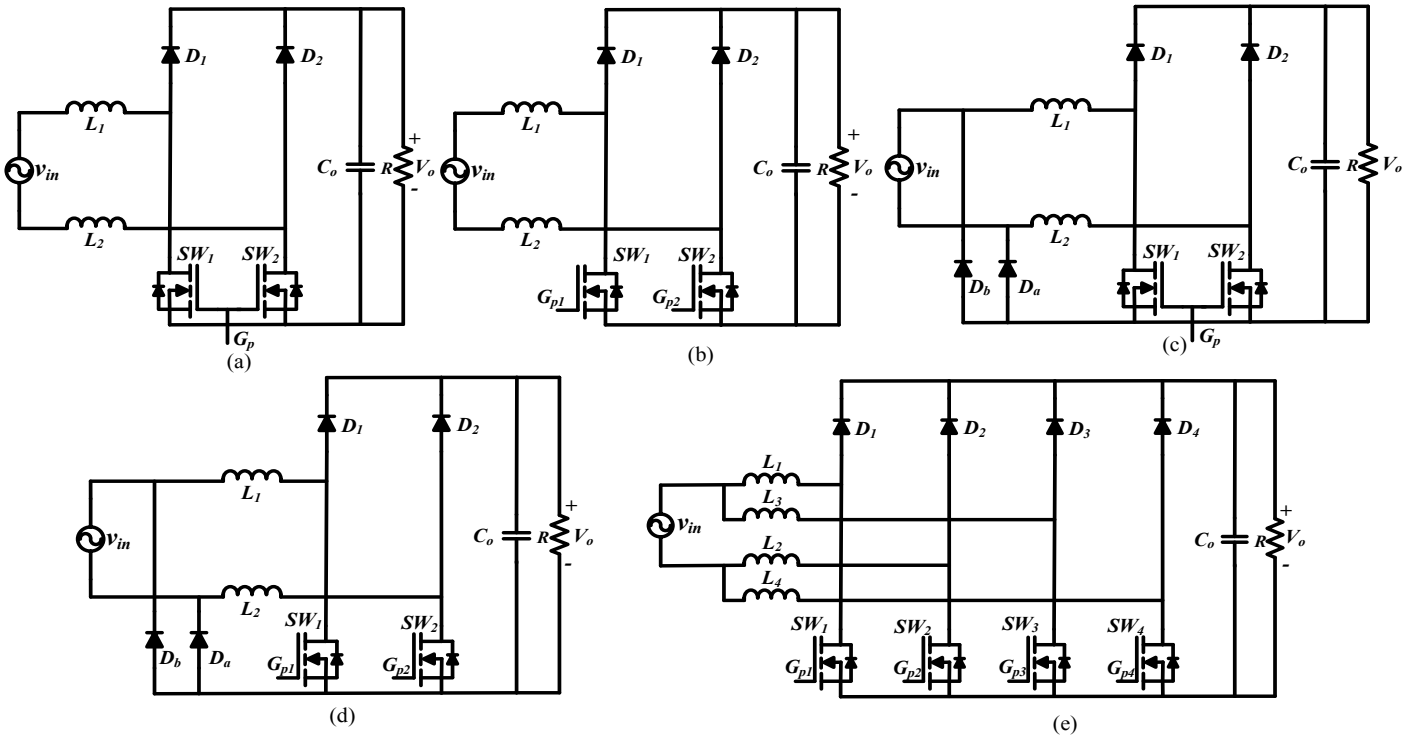


Fig. 1.8 Schematics of state-of-the-art topologies (a) bridgeless boost PFC; (b) dual boost PFC; (c) semi-bridgeless PFC; (d) phase-shifted semi-bridgeless PFC; (e) bridgeless interleaved boost PFC converter.

implementation of PLL. Failure of PLL can lead to non-sinusoidal input currents, leading to poor THD and efficiency. As the front-end converter is operated in CCM, it presents right half plane zero (RHZ) during transient operations leading to instability. Thus the controller designed for such implementation should be robust and reliable in order to meet the control objectives and maintain stability. This increases the computation burden on the microprocessor, which indirectly affects the converter performance and start-up.

Reduction in sensors and control complexity has several benefits and can be listed as follows:

1) System weight reduction.
2) Reduction in cost.
3) Improved system reliability.
4) Reduced control burden on microcontroller
5) High frequency noise robustness.

In order to reduce sensors several algorithms has been reported in literature for estimating the input current and voltages. Such approaches are complex in nature and require rigorous computation burdening the microcontroller, making it difficult for practical application.

In a converter, the number of sensors by default can be reduced by operating it in DCM. In DCM, the average value of the input current in a switching cycle is determined by the input voltage at that instant, therefore the average input current naturally follows the input voltage, which means the DCM operation inherently fulfills the PFC, the first control objective. The second objective of PFC control can be achieved by using a single voltage control loop. To conclude, the DCM operation by default eliminates requirement of the input voltage and input current sensing and therefore, only one output voltage sensor is required. Further the DCM operation inherently realizes the zero-current switching (ZCS) of the converter switches and the zero reverse recovery losses in the converter diodes [10]. Since a small inductor is required for converter DCM operation, it reduces the converter total weight and improves power density. But, the drawback of DCM operation is the high current stress of the semiconductor devices, however the higher current rating semiconductor devices are commercially available at reasonable price. Therefore, by considering all the benefits of DCM, the DCM operated converters are considered in this research work.

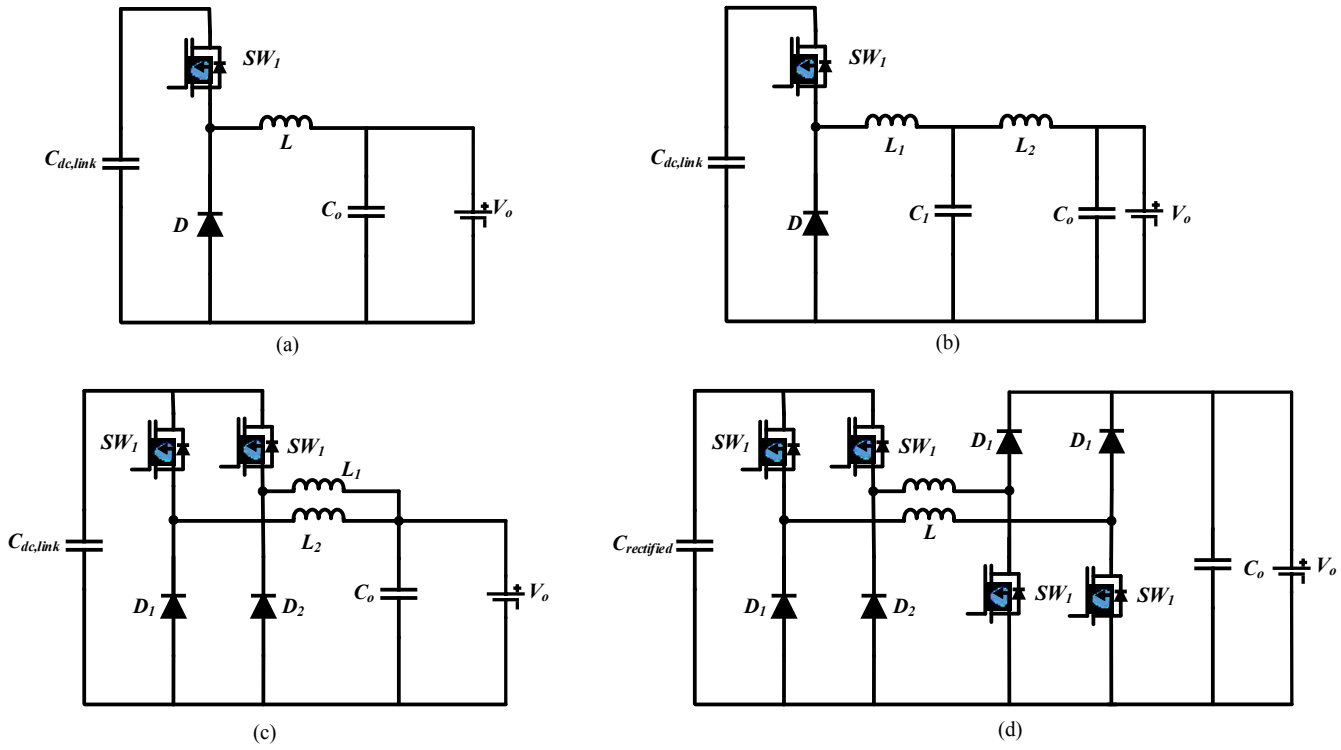


Fig. 1.9 Non-isolated DC-DC state-of-the-art topologies (a) Buck; (b) buck with output filter; (c) interleaved buck; (d) non-inverting buck-boost.

1.2.2.2 DC-DC Converter Architecture

The nominal traction battery pack for various categories of EVs ranges from 48 V to 650 V and, for that reason, the most employed DC/DC converter for the battery current regulation (BCR) stage consists of a unidirectional buck converter in order to reduce the voltage from the DC-link to the voltage level of the battery as shown in Fig 1.9. Sometimes an LC output filter is added to reduce the filtering components as in Fig. 1.9 (b). In addition, the interleaving technique can be applied to these topologies [6] [32] as depicted in Fig. 1.9 (c) and Fig. 1.9 (d). In particular, a diode rectifier followed by two interleaved noninverting buck-boost converters is proposed in [4] to design a single-stage battery charger. Other topologies include a high-frequency switched transformer to provide galvanic isolation between the grid and the battery [31]-[35].

In this sense, it is preferable to use high-frequency switched transformers in terms of size and weight than line-frequency transformers [31]. Two of the most widely used topologies are the phase-shifted full-bridge DC-DC converter [32] and the full-bridge LLC resonant converter [35] [36] as shown in Fig. 1.10. Such topologies have been well in use in current chargers but face issues regarding battery charger control. Phase-shift control presents complex switching states and

circulating currents in order to achieve zero voltage switching (ZVS) of primary switches. Such modulation technique tends to lose ZVS at light load leading to low efficiency at partial loads. LC filter connected at the output induces duty cycle loss and rectifier diode ringing due to secondary diode bridge short-circuit during polarity reversal [32]. On the other hand, LLC converters do not present such problems but require complex variable frequency modulation and microcontroller with a high clock rate to control the charging the battery voltage and current. Sophisticated small

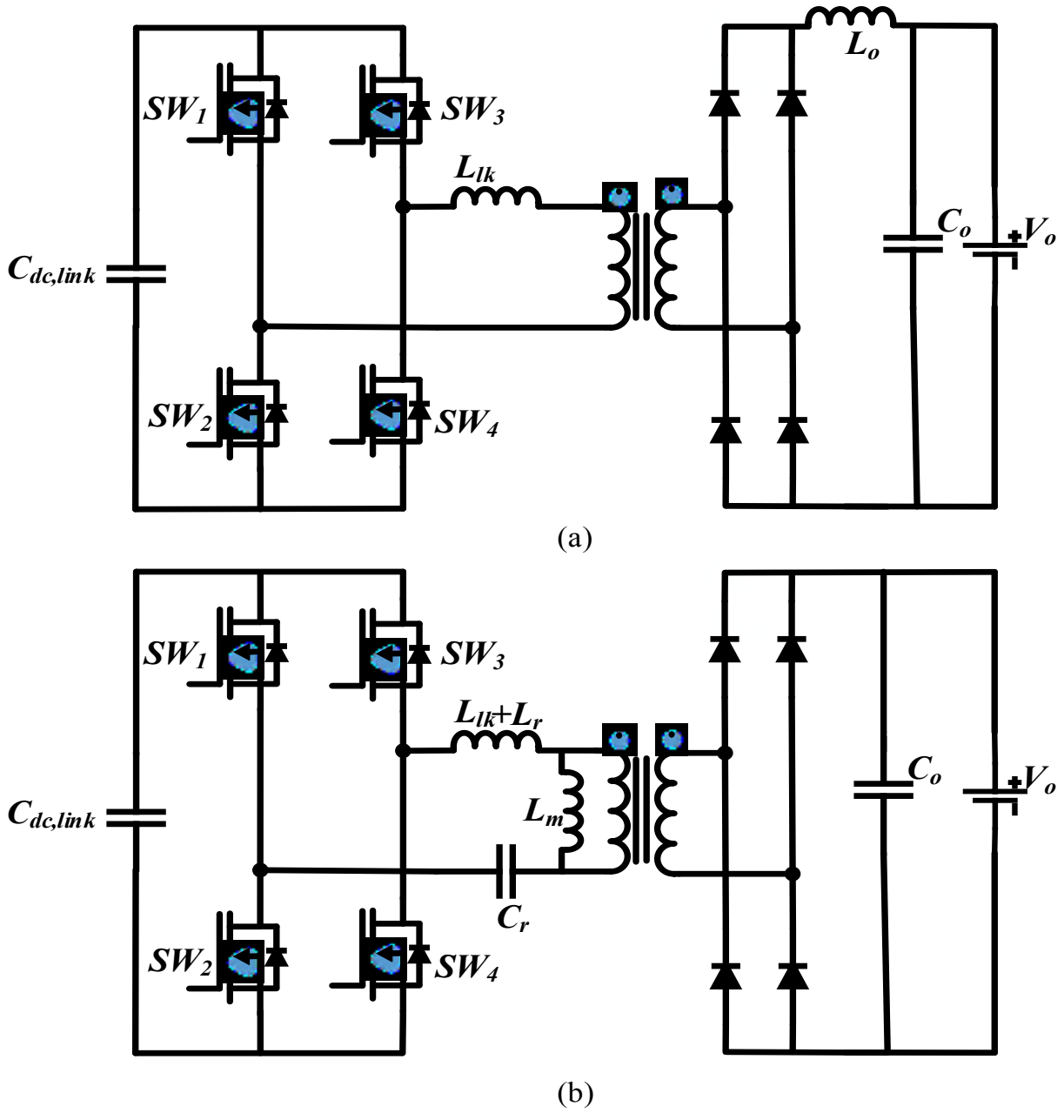


Fig. 1.10 (a) Phase shifted full-bridge. (b) full bridge LLC resonant converter.

signal modelling is required in order to design a robust control for such charging application. Moreover, the use of full-bridge topology for the LLC converter does not hold valid until unless the charger has bidirectional flow. Unidirectional battery chargers with full-bridge configuration present high conduction and switching losses due to increased semiconductor devices. LLC converter also has an issue of output voltage increase during light-load conditions [6]. Thus keeping the above points proper hardware topology needs to be selected for optimal performance for power conversion.

1.3 Research Objectives

The fundamental objective of this thesis is to propose battery charging topologies (both isolated and non-isolated) to replace currently used battery chargers with reduced sensing and control requirement by fulfilling the current THD requirements with active PFC for low voltage battery EVs. In particular AC-DC and DC-DC converters are studied and analyzed with a focus on minimizing the total number of components, improving power quality, and improving the overall operating efficiency and power density. The proposed converters are designed for the DCM operation in order to simplify the control circuit and to reduce the number of sensors which consequently increases the converter reliability, and robustness. Further, the design and performance of the converter are tested for input voltage change and load perturbations.

The objectives of this thesis are:

1) Simplified control and easy implementation

2) Reduced number of sensors

3) Higher reliability

4) Improved power quality (THD < 5%)

5) Improved efficiency

6) UPF operation for input voltage variation

To accomplish these objectives, and to replace the conventional diode rectifier active PFC rectification, this thesis proposes two battery charging topologies which have been briefly described in the thesis outline in the next section 1.4 and in detail in Chapter 2 and 3 respectively.

1.4 Thesis Outline

The objectives of the thesis are realized in Chapter 2 and 3 and the thesis outline is:

In Chapter 2, a non-isolated single-stage interleaved buck-boost converter based battery charger configuration is studied with the inductors operating in DCM. The proposed charger configuration uses the simple concept of float charging in order to reduce weight due to the bulky transformer. The steady-state DCM operation, converter design, DCM condition, small-signal model, and closed-loop controller design have been reported. The analysis and design are validated with simulation results from PSIM11.1 software and further verified with the experimental results from a 1.0 kW hardware prototype developed in the lab.

In Chapter 3, a low cost two-stage isolated battery charger has been proposed. The battery charger configuration uses an interleaved buck-boost converter operated in DCM boost mode as a first stage and a half-bridge LLC converter is used in order to provide high-frequency isolation as the see second stage. The loss analysis of each stage is done in order to obtain optimal DC-link voltage for the optimal performance of the converter. Small signal analysis for constant current (CC) and constant voltage (CV) mode is done in order to improve battery charger performance. The analysis and design are validated with simulation results from PSIM11.1 software and further verified with the experimental results from a 1.0 kW proof-of-concept hardware prototype developed in the lab. The proposed charger uses only two sensors and simple control architecture which is easy to implement. The results show high efficiency and low THD as per the requirement

1.5 Conclusion

This Chapter discusses the current trends in the automotive market intending to incorporate more EVs in the fleet of ever-growing EVs. Due to higher efficiency, better fuel economy and reliability have led to an increase in EV sales annually. The current EV industry faces challenges in the area of battery charging for the low voltage battery packs for golf-cart and e-rickshaws.

A comprehensive review of the currently used diode bridge base AC-DC converters that are available in the market and their limitations to meet the power quality requirements have been discussed. Their inability to meet the THD standards as per [12] poses challenges to current battery charging configurations. The literature study reveals the current trends in the battery charger configurations, which include both isolated and non-isolated topologies. Complications regarding

the currently available single-stage isolated and non-isolated topologies are discussed which shows that these topologies offer poor efficiency and extra footprints. Types of two-stage battery charger topologies are discussed 3 front-end and back-end architectures for such configurations. The literature study revealed that the CCM operated converter requires at least three sensors and two control loops which increase the computational burden on microcontrollers. Reduction in the number of sensors has various merits such as a reduction in cost, reduction in control complexity, increased reliability, and robustness to high frequency.

Given this DCM based battery charger configurations (isolated and non-isolated) are studied in order to reduce cost and achieve higher efficiency and contribute to novel power electronic solutions for EV battery charging application. The next chapter deals with design and development of a DCM single stage non-isolated battery charger for low voltage battery driven EVs.

Chapter 2: DCM Based Non-Isolated Battery Charger

2.1 Introduction

Typically the low power (slow) battery chargers for the low voltage battery packs (48 V) do not employ any active PFC unit for wave shaping. A two-stage battery chargers can be implemented for such low voltage battery packs where a non-isolated converter performs PFC followed by a DC-DC converter for isolation at second stage. This is one of the simplest approach with two power processing stages that leads to higher conduction losses and complex control. Moreover two-stage converters require additional semiconductor devices and bulky dc-link capacitors which increases and compromise the system reliability. Single stage converter is an appealing choice as the power is processed only once with reduced semiconductor devices. Single-stage isolated topologies have also been presented [5], [22] but offer poor efficiency because of losses associated with the leakage inductance of the transformer and require RCD snubber and overrated devices. Non-isolated battery chargers present comparatively higher efficiency, as they have reduced number of components and reduces system weight. As such converters are operated in CCM and have multiple of sensors and control requirement [37]. With the focus on reducing total number of components and sensors, a non-isolated interleaved buck-boost converter operated in DCM has been presented that addresses these concerns.

2.2 Topological Selection and Proposed Converter

CCM based PFC converters have been in implementation but the concept of DCM cannot be implemented to all the basic topologies. Boost converter and buck converter cannot be implemented in DCM for power factor correction for the following reason. The input current for a boost converter can be given as

$$i_{in}(t) = \begin{cases} \frac{v_{in}(t)}{L} t, & 0 < t \leq t_{on} \\ \frac{(v_{in}(t) - V_o)}{L} t, & t_{on} < t < T_s \end{cases} \tag{2.1}$$

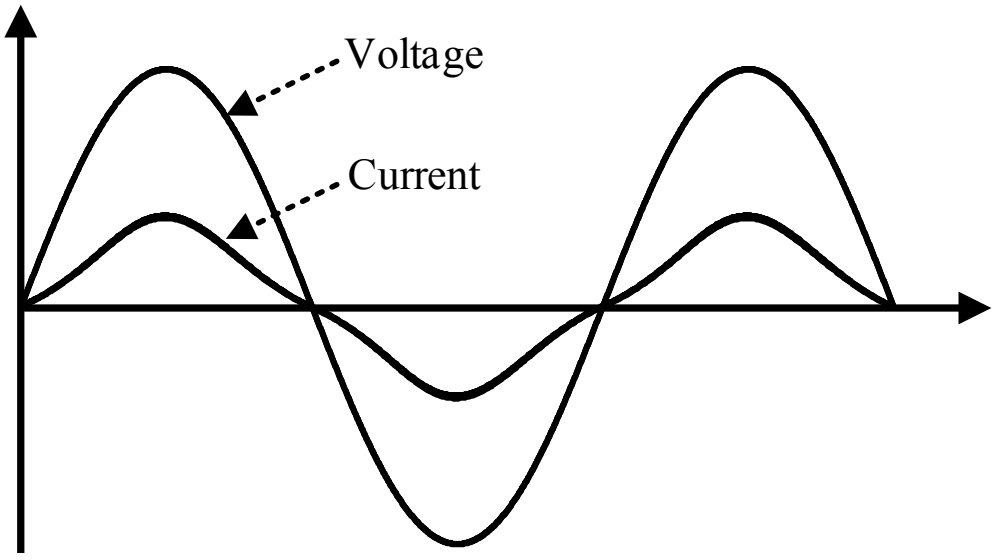
By performing FFT of the (2.1) using (2.2), one can get,

$$i_{in}(t) = \frac{a_0}{2} + \sum_{h=1}^{\infty}(a_h \cos(h\omega_{sw}t) + b_h \sin(h\omega_{sw}t)) \quad (2.2)$$

$$a_h = \frac{V_0}{h\omega_{sw}L}\left(Dsin(2\pi hD) + \frac{1}{2h\pi}\cos(2\pi hD) - \frac{1}{2h\pi}\right) \quad (2.3)$$

$$b_h = \frac{V_0}{h\omega_{sw}L}\left(1 - Dcos(2\pi hD) + \frac{\sin(2\pi hD)}{2\pi h}\right) - \frac{V_{in}}{h\omega_{sw}L} \quad (2.4)$$

From (2.3) and (2.4), it is observed that lower order odd harmonics are present, which leads to poor input current THD. Fig 2.1 shows the input current waveform and FFT analysis for a boost



(a)

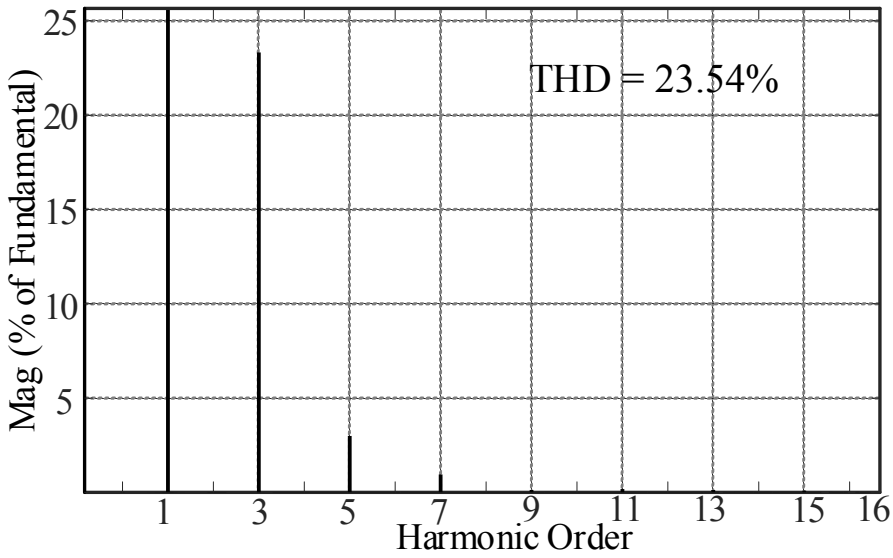


Fig. 2.1 Boost PFC input current in DCM (a) waveform (b) THD.

PFC converter operating in DCM. It is seen that higher amplitude low order harmonics are injected (2.3), (2.4) in input current leading to poor THD. Such a waveform is obtained due to its boost structure as the boost inductor is connected to the input throughout the switching cycle. Thus any non-linearity from the output is transferred to the input leading to peaky input current waveform. As a consequence, DCM boost and boost derived configurations require a large filter at the input side to filter out lower order harmonics, which in turn reduces the power density of the system. Several methodologies have been proposed for improving the current quality in DCM boost converter by reducing the lower order harmonic content. However, such approaches are complex in nature and require extra sensing without having a significant impact on the harmonic content [38]-[42]. Therefore, DCM based boost topologies are not feasible for such PFC application. On the other hand, buck or buck derived topologies cannot be implemented PFC, which can be understood by performing FFT analysis of input current expression expressed as

$$i_{in}(t) = \begin{cases} \frac{(v_{in}(t)-V_o)}{L} t\ ,\ 0 < t \le t_{on} \\ 0,\ t_{on} < t < T_s \end{cases} \tag{2.5}$$

Using (2.1),

$$a_h = \frac{(v_{in}(t)-V_o)}{h\omega_{sw}L}\left(Dsin(2\pi hD) + \frac{1}{2h\pi}\cos(2\pi hD) - \frac{1}{2h\pi}\right) \tag{2.6}$$

$$b_h = \frac{(v_{in}(t) - V_o)}{h\omega_{sw}L}\left(\frac{sin(2\pi hD)}{2h\pi} - Dcos(2\pi hD)\right) \tag{2.7}$$

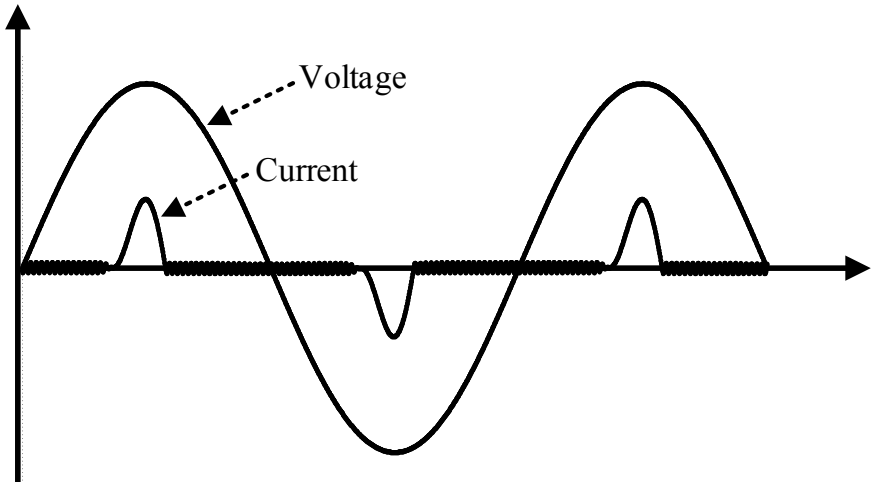


Fig. 2.2 Input current and voltage waveform for buck converter in DCM.

Even though this topology does not present odd harmonics at the input as seen from (2.6) (2.7), unlike boost converter, power transfer doesn't take place for $v_{in}(t) < V_o$, as duty cycle saturates at its maximum limit, leading to poor power factor as seen from Fig. 2.2.

A DCM buck-boost becomes advantageous as the input inductor is either connected to the input or the output, thus harmonics from the output are not reflected across the input side thus achieving a good THD and UPF operation. Moreover, it has less passive components' count as compared to the conventional Sepic or Cuk converter making it a cost effective option for charging.

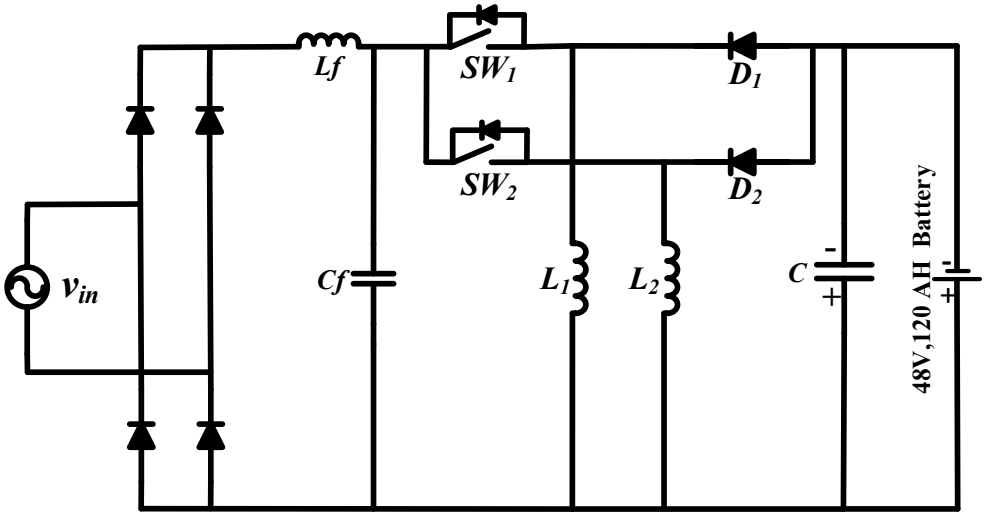


Fig. 2.3. Proposed non-isolated interleaved two-cell battery charger

Fig. 2.3, shows an interleaved PFC buck-boost converter for the low voltage battery charging. It is the fusion of a full-bridge diode rectifier and two-cells (switch, inductor and diode). Both the cells operate on a similar switching frequency and the switching signals are 180^0 phase shifted. By interleaving operation of two-cells, not only the current stress is reduced through the devices but also the input filter size is also reduced, which leads to increased power density of the converter. The proposed configuration uses the simple concept of float charging to charge the battery. It uses a simple charging method by just pushing current equal to the maximum current limit of the lead acid battery. As the battery voltage increases gradually this current falls and charging is turned off. Such battery charging method is a cost effective solution as it reduces the sensor count and complexity.

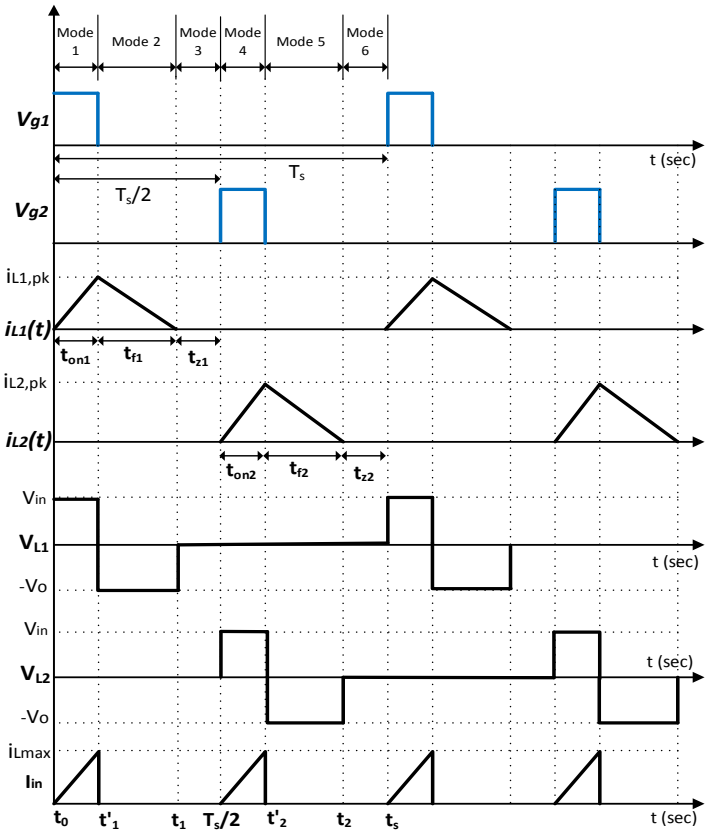


Fig.2.4. Steady-state waveforms of two-cell converter.

2.3 Steady State Analysis

Steady-state operation of the two-cell buck-boost for one high frequency switching cycle is shown in Fig. 2.4. With following assumptions [49], [50] and the same analysis can be done for single-cell converter.

a) All the components are ideal and lossless.

b) Within one switching cycle, input and output voltages are constant.

c) The output capacitor is bulky enough to maintain output voltage constant.

d) Duty cycle is fixed for one power level.

Mode I: $0 < t < t_1'$

In this mode switch SW_1 is turned on with gating pulse V_{g_1}, L_1 charges and stores energy whereas capacitor C supplies the load. No energy is stored in L_2. Inductor current i_{L1} is given by

$$i_{L1}(t) = \frac{v_{in}(t)}{L_1} \tag{2.8}$$

Mode II: $t_1' < t < t_1$

Switch SW_1 is turned off and inductor current i_{L1} freewheels through diode D_1. Capacitor C filters out the ripple current and supplies pure DC current to the battery. Inductor current $i_{L1}$for this stage is given by

$$i_{L1}(t) = i_{L1,pk} - \frac{V_o}{L_1} t_1 \tag{2.9}$$

Mode III:- $t_1 < t < {}^{T_s}/_2$

This is the DCM condition where energy stored in L_1becomes zero and the capacitor supplies the load. At the end of this interval, half of the high frequency cycle is over. This time duration is given by

$$t_{z1} = \frac{T_s}{2} - t_{on1} - t_{f1} \tag{2.10}$$

Mode IV: ${}^{T_s}/_2 < t < t_2'$

Switch SW_2 is turned ON in this mode, inductor L_2 charges, and stores energy. Capacitor C supplies the load and whereas energy stored in L_1 is zero. Inductor current $i_{L2}(t)$ is given by

$$i_{L2}(t) = \frac{v_{in}(t)}{L_2} \tag{2.11}$$

Mode V:- $t_2' < t < t_2$

Gating pulse from switch SW_2 is removed. Inductor L_2 discharges through the load and diode D_2, thus supplies power to the load $i_{L2}(t)$ is given by

$$i_{L2}(t) = i_{L2,pk} - \frac{V_o}{L_2} \tag{2.12}$$

Mode VI:-$t_2 < t < T_s$

This is the same as *Mode III*, and the DCM period is given

$$t_{z2} = T_s - t_{on2} - t_{f2} \tag{2.13}$$

2.4 Converter Design

In this section, the expressions for converter average output current and input current, and the DCM condition are derived. Further, the design equations for each passive component of converter are developed.

2.4.1 Average output current

The average load current in one switching cycle $i_{o,avg}$ is nothing but the average current of both diodes D_1 and D_2 i.e. the sum of area under the i_{L1}curve and i_{L2} curve during interval $t_{f1}$and t_{f2} respectively. Substituting $t = t_{f1}$ and $t = t_{f2}$we get,

$$i_{o,avg} = \frac{1}{2} t_{f1} i_{L1,pk} + \frac{1}{2} t_{f2} i_{L2,pk} \tag{2.14}$$

where,

$$t_{f1} = \frac{i_{L1,pk}}{V_o} L_1 \tag{2.15}$$

$$t_{f2} = \frac{i_{L2,pk}}{V_o} L_2 \tag{2.16}$$

$$i_{L1,pk} = \frac{v_{in}(t)}{L_1} D_{1,on} T_s \tag{2.17}$$

$$i_{L2,pk} = \frac{v_{in}(t)}{L_2} D_{2,on} T_s \tag{2.18}$$

Thus the average output over one switching cycle can be given as

$$i_{o,avg} = \frac{1}{2}\left(\frac{i_{L1,pk}^2}{V_o}L_1 + \frac{i_{L2,pk}^2}{V_o}L_2\right) \tag{2.19}$$

$$= \frac{v_{in}^2(t)T_s}{V_o}\left(\frac{D_{1,on}^2 L_2 + D_{2,on}^2 L_1}{L_1 L_2}\right) \tag{2.20}$$

The average output current $I_{o,avg}$ over a line period is calculated by integration of the switching cycle average output current and can be given as

$$I_{o,avg} = \frac{1}{2\pi}\int_0^{2\pi} i_{o,avg}\, d\omega t \tag{2.21}$$

$$I_{o,avg} = \frac{V_{in,pk}^2 T_s}{4V_o}\left(\frac{D_{1,on}^2 L_2 + D_{2,on}^2 L_1}{L_1 L_2}\right) \tag{2.22}$$

where $D_{1,on} = D_{2,on} = D$, D = duty cycle.

2.4.2 Input current

Assuming the lossless circuit, i.e., 100% efficiency, the input power of is equal to the output power

$$v_{in} i_{in} = v_o i_{o,avg} \tag{2.23}$$

Substituting (2.20) in (2.23)

$$v_{in} i_{in} = \frac{v_{in}^2(t)T_s}{2}\left(\frac{D_{1,on}^2 L_2 + D_{2,on}^2 L_1}{L_1 L_2}\right) \tag{2.24}$$

$$i_{in} = \frac{v_{in}(t)T_s}{2}\left(\frac{D_{1,on}^2 L_2 + D_{2,on}^2 L_1}{L_1 L_2}\right) = \frac{V_{in,pk}T_s}{2}\left(\frac{D_{1,on}^2 L_2 + D_{2,on}^2 L_1}{L_1 L_2}\right)\sin(\omega t) \tag{2.25}$$

$$i_{in} = I_{in,pk}\sin(\omega t) \tag{2.26}$$

where,

$$I_{in,pk} = \frac{V_{in,pk}T_s}{2}\left(\frac{D_{1,on}^2 L_2 + D_{2,on}^2 L_1}{L_1 L_2}\right) \tag{2.27}$$

Since the duty cycle of the converter is constant in DCM, the relation given by (2.26) indicates the UPF operation of the converter and the input current is sinusoidal with peak current $I_{in,pk}$ given by (2.27). The higher switching order harmonics present in the input currents will be filtered out by the input inductors and result in low input current THD.

2.4.3 DCM operation and critical conduction parameter

Following inequalities must hold for DCM operation Fig. 2.4

$$I_o < \Delta i_{L1} + \Delta i_{L2} \tag{2.28}$$

$$I_o < \frac{V_{in.pk} T_s}{2V_o} \left(\frac{D_{1,on} L_2 + D_{2,on} L_1}{L_1 L_2} \right) \tag{2.29}$$

where,

$$I_o = \frac{D V_{in,pk}}{(1-D) * R} \tag{2.30}$$

$$K_{crit} > \frac{4 L_1 L_2}{R T_s (L_1 + L_{2)}} \tag{2.31}$$

To maintain DCM for all cases, the critical conduction parameter is given as K_{crit}

$$K_{crit}(D) = 1 - D \tag{2.32}$$

This can also be expressed in terms of critical load resistance R_{crit}. Thus equation can be expressed as

$$R_{crit} > \frac{4 L_1 L_2}{D_{crit} T_s (L_1 + L_{2)}} \tag{2.33}$$

Critical duty cycle D_{crit} is calculated in order to maintain DCM for all cases. To maintain DCM at all times

$$t_{on1} + t_{f1} + t_{on2} + t_{f2} < T_s \tag{2.34}$$

$$D\left(1+\frac{1}{M}\sin(\omega t)\right)<1 \tag{2.35}$$

where $M = {V_o}/{V_{in,pk}}$

Average output current is given by

$$I_{o,avg} = \frac{V_o}{R} \tag{2.36}$$

$$D = M\sqrt{K_{cond}} \tag{2.37}$$

where K_{cond} is the conduction parameter for is interleaved buck-boost and is defined in equation (2.37). The critical value of K_{cond} to keep the converter in DCM is

$$K_{crit} = \frac{1}{2(M+1)^2} \tag{2.38}$$

2.4.4 Design of inductor

To ensure PFC, the inductor needs to be in DCM for worst-case input voltage as input current will be maximum for that case. The inductor can be computed as follows,

$$L < \frac{V_{in,pk}^2\, D^2 T_s}{2P_o} \tag{2.39}$$

A value below this critical inductor value should be selected in order ensure DCM operation. Due to

2.4.5 Design of output capacitor

In PFC converters, the output capacitor is designed to filter the harmonic components occurring at twice the line frequency. Thus, the variation in the power (input and output) discharges through the output filter capacitor and is expressed as

$$P_c(t) = P_{ac}(t) - P_o(t) \tag{2.40}$$

$$V_o i_c = V_{in,pk} I_{in,pk} cos2\omega t - V_o I_o \tag{2.41}$$

Considering efficiency equal to 100%,

$$i_c(t) = \frac{V_{in,pk} I_{in,pk}}{V_o} cos2\omega t = I_o cos2\omega t \tag{2.42}$$

The output voltage ripple equation is given by,

$$V_{o,ripple}(t) \approx \frac{1}{C} \int i_c(t) dt \tag{2.43}$$

By putting (2.21) into equation (2.22),

$$V_{o,ripple}(t) \approx \frac{1}{C} \int i_c(t) dt \tag{2.44}$$

$$C = \frac{I_o}{2\omega V_{o,ripple}} \tag{2.45}$$

2.4.6 Design of input filter

Input current in an interleaved DCM buck-boost converter is defined as

$$i_{in}(t) = \begin{cases} \frac{v_{in}(t)}{L}, & 0 < t \leq t_{on} \\ 0, & t_{on} < t \leq T_s \end{cases} \tag{2.46}$$

On performing FFT of input current using (2.2), we get

$$a_0 = \frac{v_{in}(t)}{L} D^2 T_s \tag{2.47}$$

$$a_h = \frac{v_{in}(t)}{2\pi h f_{sw} L} \left(Dsin(2\pi hD) + \frac{1}{2h\pi} \cos(2\pi hD) - \frac{1}{2h\pi} \right) \tag{2.48}$$

$$b_h = \frac{v_{in}(t)}{2\pi h f_{sw} L} \left(\frac{sin(2\pi hD)}{2h\pi} - Dcos(2\pi hD) \right) \tag{2.49}$$

Equation (2.47) indicates the fundamental component of the input current and (2.47), (2.49) indicates the switching order harmonics present, which needs to be filtered out. Upon comparing (2.3) and (2.4) with (2.48) and (2.49), it is noted that unlike conventional boost converter the proposed converter does not inject higher lower order amplitude harmonics in the input and thus requires a small filter. By designing a low-pass LC filter with a cutoff frequency much lower than the switching frequency, the harmonic currents can be filtered out.

The criteria to design low-pass LC Filter is as follows:

1) Selection of cut-off frequency f_c given by

$$f_c = \frac{1}{2\pi}\sqrt{\frac{1}{L_f C_f}} \tag{2.50}$$

2) Minimization of filter reactive power consumption for 60 Hz at 1.0 kW. The reactive power is minimum when filter characteristic impedance is equal to the converter impedance i.e.

$$Z_{ch} = \sqrt{\frac{L_f}{C_f}} = Z_{in} \tag{2.51}$$

where Z_{ch} is the characteristic impedance and Z_{in} is the input impedance at rated load and is given by

$$Z_{in} = \frac{2L}{D^2 T_s} \tag{2.52}$$

Using (2.51) and (2.52), the low-pass filter parameters L_f and C_f can be obtained as

$$L_f = \frac{Z_{ch}}{2\pi f_c} \tag{2.53}$$

$$C_f = \frac{1}{2\pi Z_{ch} f_c} \tag{2.54}$$

2.5 Converter small signal model

The small-signal model of the proposed converter is obtained by using current injected equivalent circuit approach (CIECA) [51], [52] [53]. In this approach, the non-linear part of the circuit is

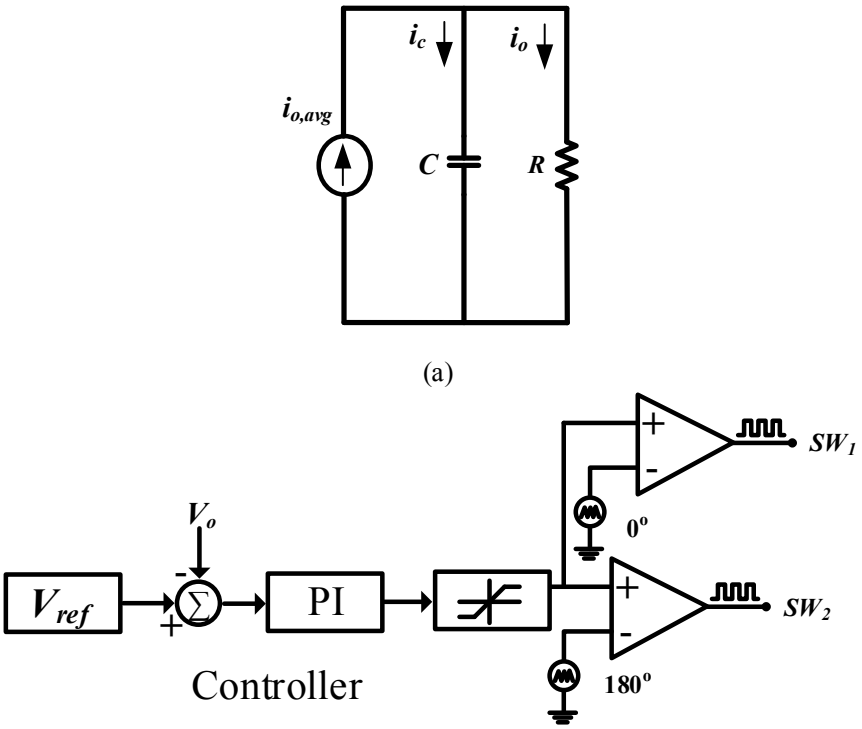


Fig. 2.5. (a) CIECA for small signal modelling. (b) Control diagram for proposed converter

linearized by injecting the average output current in a switching cycle ($i_{o,avg}$) produced by the non-linear part into the linear part. From Fig. 2.5(a), we know that

$$\hat{\imath}_{o,avg} = \left(sC + \frac{1}{R}\right)\hat{v}_o \tag{2.55}$$

Applying perturbations to (2.22) around the steady state operating point and making the small signal approximation gives

$$\hat{\imath}_{o,avg} = \frac{V_{in,pk}^2 DT_s}{LV_o}\hat{d} + \frac{V_{in,pk}D^2T_S}{LV_o}\hat{v}_{in,pk} - \frac{i_{o,avg}}{V_o}\hat{v}_o \tag{2.56}$$

On equating (2.55) and (2.56) and substituting $\hat{v}_{in,pk} = 0$,

$$G(s) = \frac{v_o(s)}{d(s)} = \frac{2V_o}{M\sqrt{K_{cond}}(sRC + 2)} \tag{2.57}$$

DSP TMS320F28335 is used as a digital control platform to implement the converter control. Hall Effect sensor LV 25-P is used to sense the output voltage across the load. The sensed voltage and

Table 2.1: Design Specifications.

Parameters	Value
Source Voltage, Vs (rms)	$110V \pm 25\%$, 60 Hz
Output Voltage, V_o	65V
Output Power, P_o	1 kW
Output voltage ripple, $V_{o,\ ripple}(t)$	5% of output voltage (V_o)
Switching frequency, f_s	50 kHz

reference voltage are compared, and the error is fed to the PI Controller which generates the control signal d_{con}. This d_{con} is fed into a comparator with sawtooth signal shifted by 180^o in order to generate pulses for interleaving operation Fig. 2.5(b).

2.6 Results and Discussion

This section presents the simulation and experimental results of the proposed converter along with a comparison with other state-of-art topologies.

2.6.1 Simulation Results

This sub-section presents the simulation results of the proposed battery charger on PSIM 11.1 software. The converter is designed with the specifications mentioned in Table 2.1, and the designed parameters are given in Table 2.3. The input LC low-pass filter is designed for a cut-off frequency of 5 kHz. The control-to-output transfer function is obtained by using (2.53) and is given by (2.58)

$$G(s) = \frac{498.82}{0.0124s + 1} \tag{2.58}$$

As the transfer function is a single pole system, a simple PI controller $\left(K_p + \frac{K_i}{s}\right)$ given by (2.59) is used to control the output voltage as shown in Fig. 2.5(b). As the output capacitor sees a voltage ripple of twice the line frequency, a PI controller with bandwidth lower than the 120Hz is selected with a phase margin of 60^0. The controller is tuned using sisotool in Matlab and the controller is designed at a gain crossover frequency of 314.4 rad/sec.

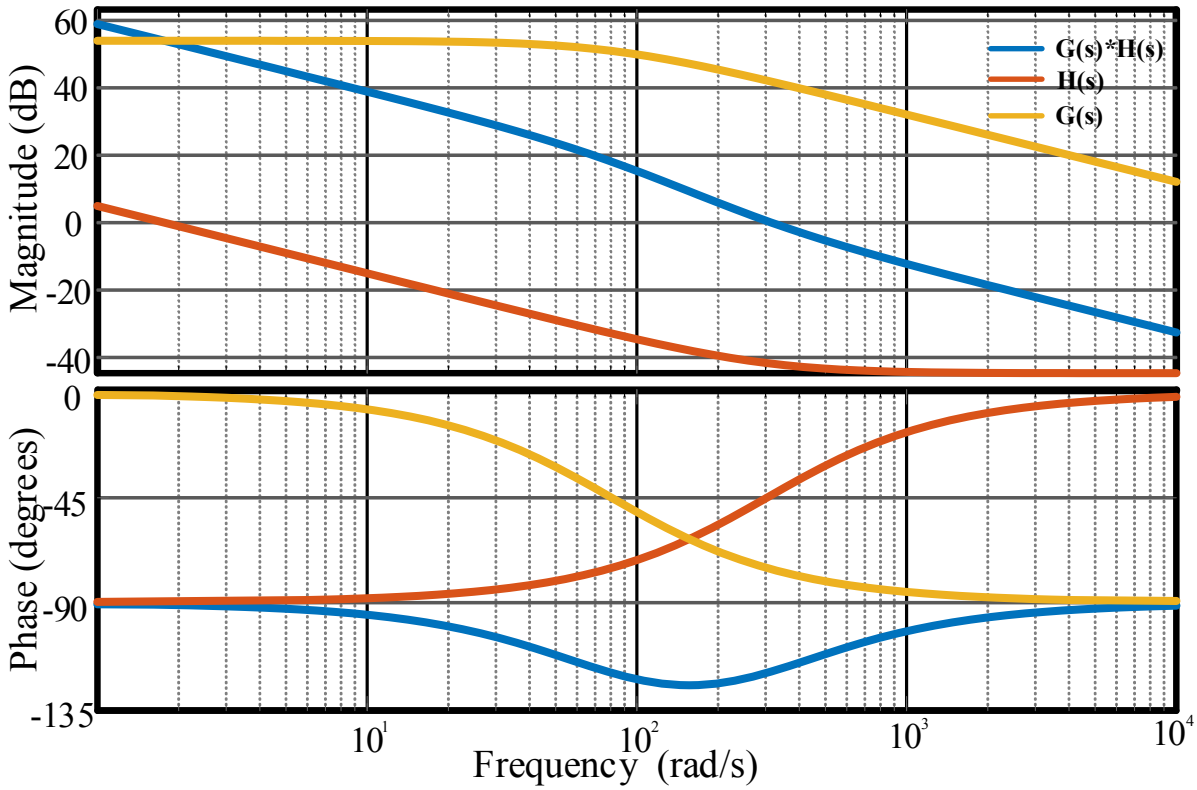


Fig. 2.6. Bode plot with plant G(s), controller H(s) and open loop transfer function G(s)*H(s)

Fig. 2.6 shows the frequency response of plant transfer function G(s), controller transfer function H(s) and open loop transfer function G(s)*H(s). The open loop transfer function has an infinite dc gain which indicates the system reference tracking with zero steady state error, and the system robustness for input and load disturbances. The open loop phase margin of 60^0 indicates enough damping of the system and the -20 dB slope at zero gain crossover frequency indicates system robustness towards the high frequency noise rejection. The sensed voltage is compared with the reference voltage and error is fed into the PI controller. The PI controller generates the duty cycle to control switch SW_1 and SW_2. A limiter is connected in order to limit the duty cycle during start-up and overload conditions.

With the designed controller, a closed-loop simulation for the proposed converter is performed in PSIM11 software, and the results are depicted in Fig. 2.7. Fig. 2.7 (a) shows the input voltage and current waveform of the proposed battery charger. Input current is perfectly sinusoidal and in phase with the input voltage thus confirming UPF operation of proposed configuration. Fig. 2.7 (b) shows the output voltage and current of the single stage charger at rated power of 1.0 kW. The output

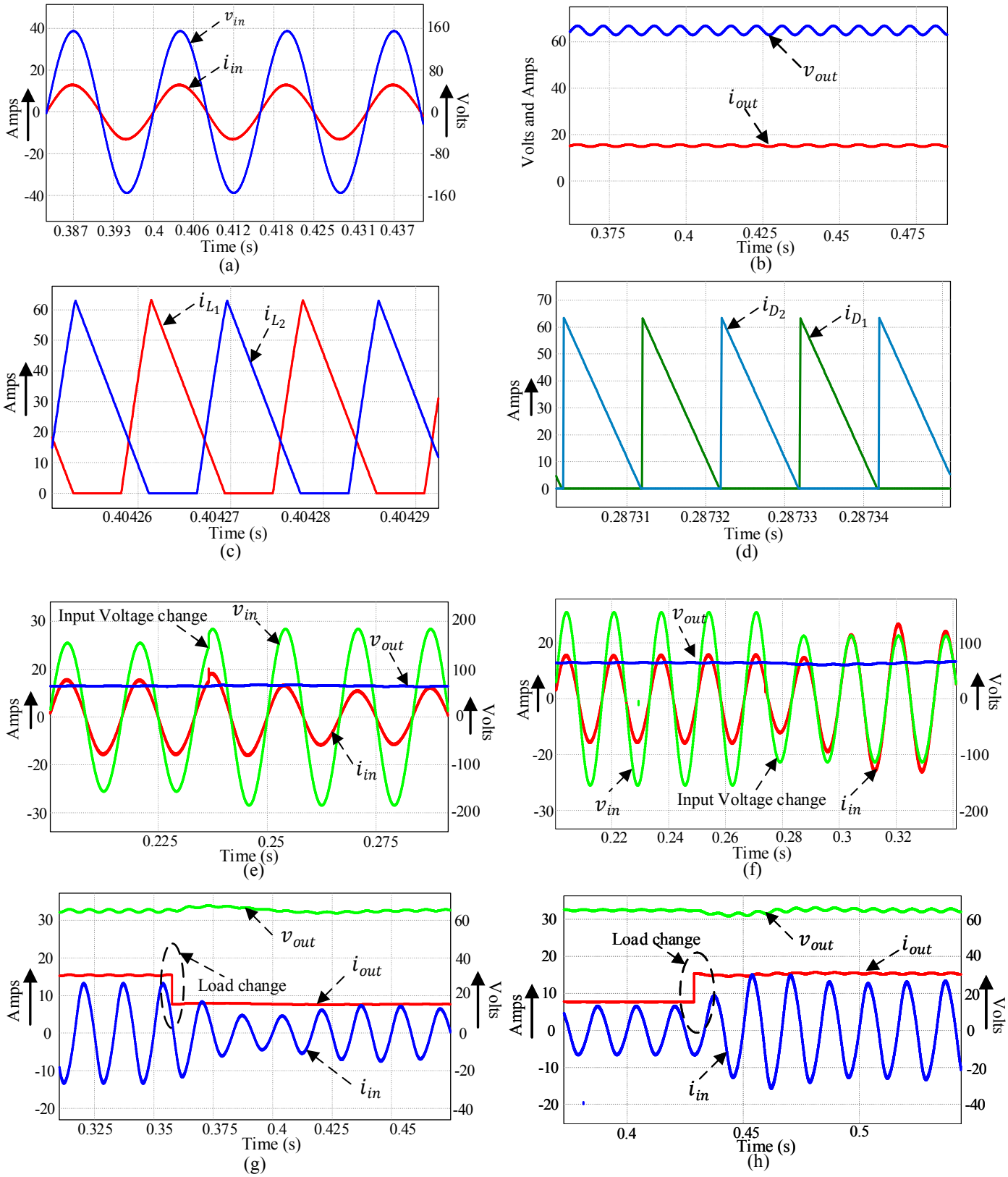


Fig. 2.7. (a) Input voltage and current (b) output voltage and current (c) Interleaving operation of DCM inductor (d) (e) input voltage swell (f) input voltage dip (g) load change from 500 W to 1.0 kW (h) load change from 500 W to 1.0 kW.

voltage is constant and settled at a reference value of 65 V. Interleaving and DCM operation of the buck-boost converter is shown in Fig. 2.7 (c). Inductor currents are discontinuous thus validating the design. Fig. 2.7(d) shows the diode current waveform of the interleaved converter. It is observed as the diode current is zero in every switching cycle, zero reverse recovery losses occur in such converters which boosts up the efficiency. Fig. 2.7 (e) and Fig. 2.7 (f) show the converter response to input voltage variation from 110V to 80 V and 110V to 130 V respectively. Output voltage is maintained nearly constant with a small fall and rise during voltage dip and voltage swell conditions. The output voltage remains stable and closely tracks the reference voltage which confirms the controller design. Input current is maintained sinusoidal and in-phase with input voltage throughout its operation. The output voltage and input current of the converter when subjected to a load step change from 50% to 100% and 100% to 50% of the rated power are shown in Fig. 2.7(g) and Fig. 2.7(h).It is observed that the output voltage is closely tracking the reference voltage and settled within the settling time of 30ms, which confirms the robustness of the

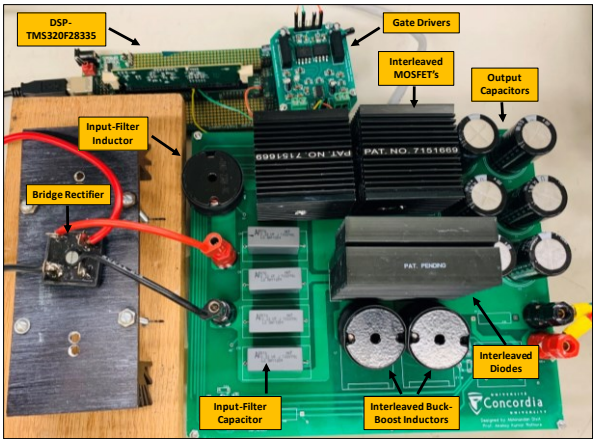
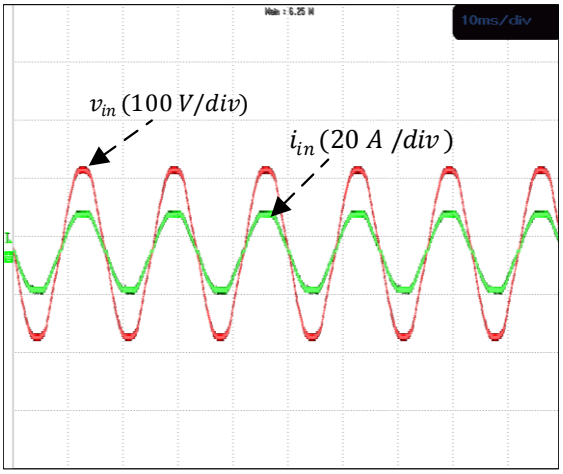


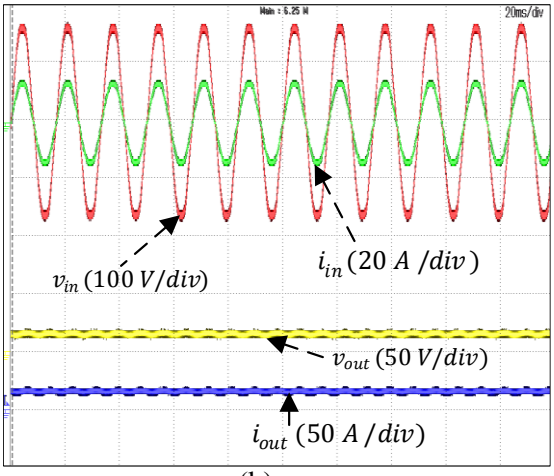
Fig. 2.8 Hardware Prototype.

Table 2.2: Component Specification

Components	Two Cell Specifications
MOSFET	UJ3C065030K3S, SIC
Diode	RURG80100
Input filter inductor	$110\mu H$,1140-221K-RC/2
Input filter Cap	$0.22\mu F * 4$, 480 VAC, R76QR32204030J
Output Filter Capacitor	$1800\mu F$ *6, 100 VDC, LGU2A182MELA
Buck-Boost Inductor	$10\mu H$, 1140-100K-RC
DSP	DSP-TMS320F28335
Gate Driver	HCNW3120



(a)



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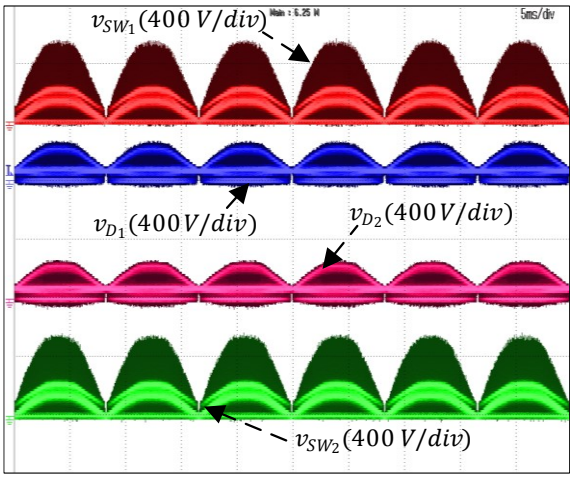

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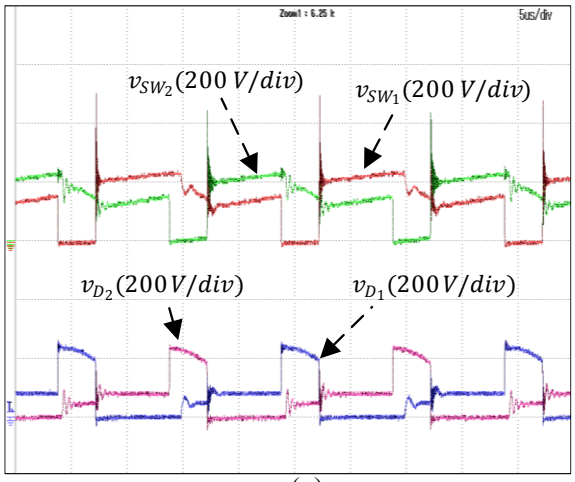
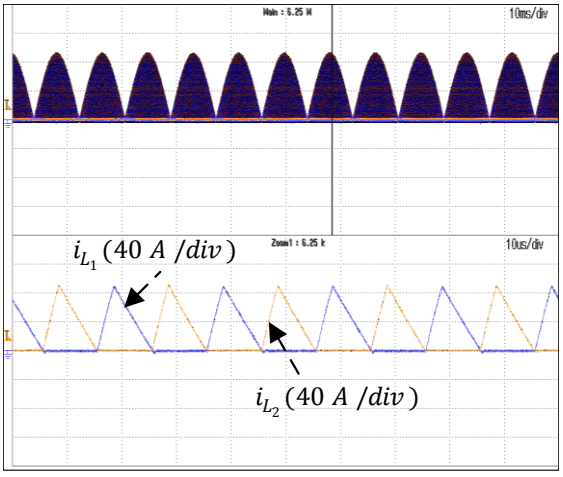
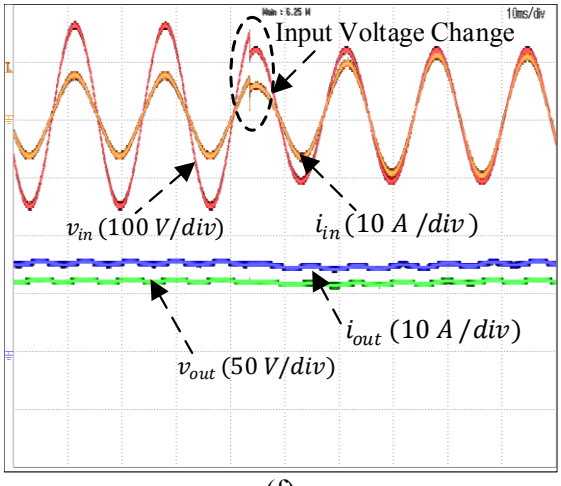


(e)



(e)



(f)

Fig. 2.9. (a) Input voltage and current (b) input voltage, input current ,output voltage and output current (c) switch voltage and diode voltage profile (d) Switch voltage and diode voltage stresses (e) Interleaving operation of DCM inductors (f) input voltage dip

controller.

2.6.2 Experimental Results

To validate the converter design and to further verify the simulation results, a proof-of-concept 1.0 kW hardware prototype is developed with the components specified in Table 2.2. Fig. 2.8 shows the hardware prototype developed in lab with TMS320F28335 is used to program the designed controller and hall-effect based LEM voltage sensor LV-25P is used to sense the control output voltage.

Steady state results for an interleaved buck-boost converter is shown in Fig. 2.9. Fig. 2.9(a) show the input voltage and current for the converter. Both voltage and current are in phase with each other which confirm UPF operation of the converter. Fig. 2.9 (b) the converter output voltage and currents along with PFC operation. Diode and switch voltage profiles are shown in Fig. 2.9(c) and Fig. 2.9(d) respectively. When switch SW_1 is turned on corresponding inductor L_1 charges (Fig. 2.9(e)) and diode D_1 blocks the voltage equal to $V_o + V_{in,pk}$. The corresponding switch SW_2 blocks with a voltage equal to $V_{in,pk}$. As SW_1 is turned off, SW_2 blocks a voltage equal to $V_{in,pk}$ and the inductor L_1 discharges through diode D_1 where D_2 blocks V_o voltage. Switch SW_2 is turned on and inductor L_2 starts charging as shown in Fig. 2.9(d), Fig. 2.9(e), which confirms the interleaving operation and ZCS turn-on of proposed two-cell converter. Voltage spike of up to 450V at device

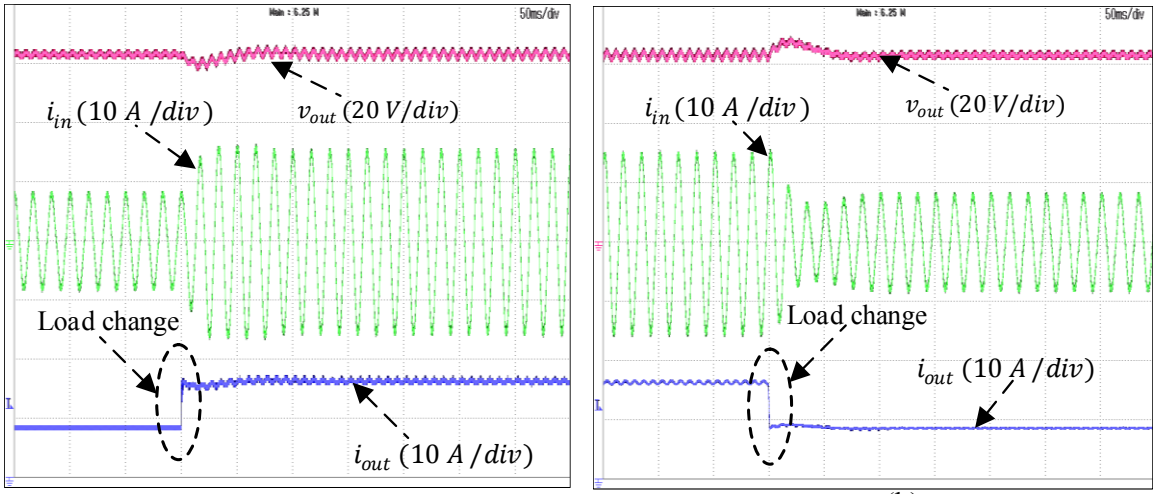
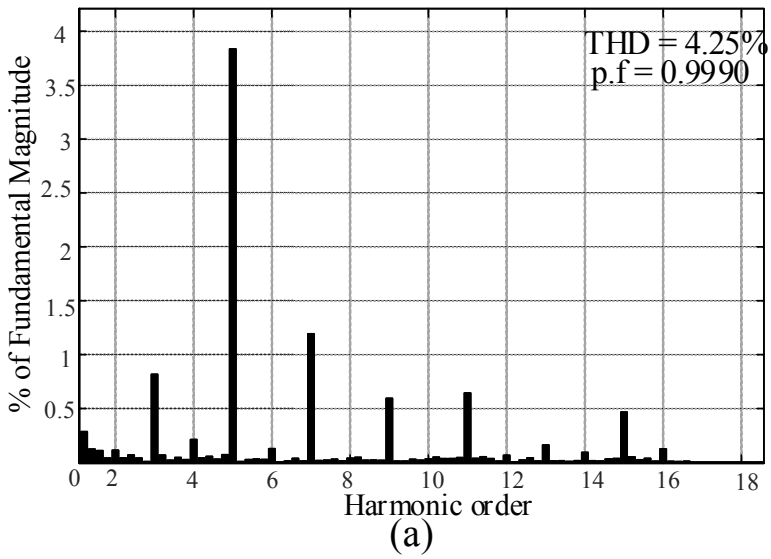


Fig. 2.10. (a) Load change from 500W to 1.0 kW. (b) Load change from 1.0 kW to 500W.



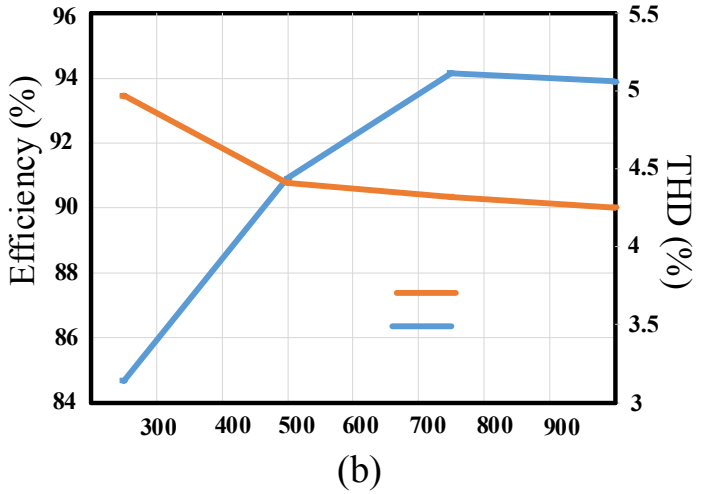


Fig. 2.11. (a) Input current THD at 1.0 kW. (b) Variation of THD and efficiency with power.

turn off is observed in Fig. 2.9(d) which is due to the interaction of parasitic inductance with switch capacitance C_{oss}. Transient results for proposed interleaved converter for input voltage change from 110 V to 80 V is shown in Fig. 2.9(f). It is observed that input current increases during voltage change to maintain the same power level and remains sinusoidal throughout the operation. Transient results for proposed two-cell converter for a load change from 500W to 1 kW and 1 kW to 500W are shown in Fig. 2.10(a) and Fig. 210(b). Input current remains sinusoidal in both cases and output voltage settles in less than 30ms for first case and less than 80ms for second case. Efficiency of the interleaved converter is about 93.89% at 1.0 kW. Input current FFT analysis is shown in Fig. 2.11(a) and is around 4.25% which is below IEC-61000-3-2. Fig 2.11 (b) shows the variation of efficiency and THD with load. It is observed that the THD always remain below 5% and follows IEC standards, thus achieving comparatively higher efficiency. As the converter is

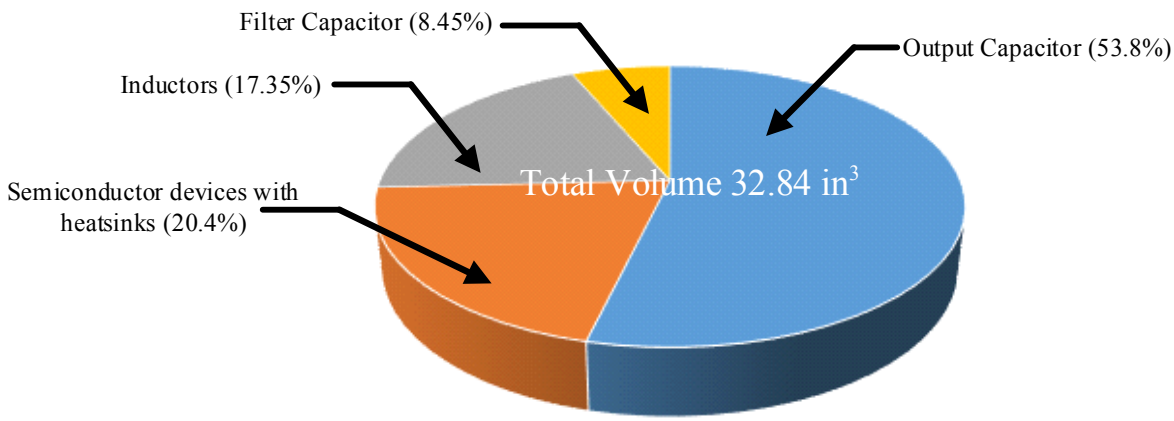


Fig. 2.12. Volumetric distribution of interleaved converter

operated in DCM, semiconductor devices experience high current stress leading to higher thermal management and reduced power density. As the operation of the converter is for low voltage high current application the losses increase drastically. Fig. 2.12 shows the volumetric distribution on the proposed converter. It is observed that output capacitors occupy more than half of the total volume. This is because the output capacitor needs to handle twice the input frequency current ripple and maintaining a low ripple voltage for battery charging, six 1800µF capacitors are connected in order to meet the above requirements. The next major component occupying the total volume are the semiconductor along with their heatsinks. As the semiconductor devices have higher conduction and switching losses due to DCM operation, larger heatsinks are required. The overall power density of the hardware prototype is 30.45 W/in^3 and weighing 1.4 kg. Table 2.3 shows a comparative analysis between single stage isolated and non-isolated battery charging topologies along with the proposed converter. Single stage isolated topologies present poor peak efficiency because of losses due to leakage inductance of the transformer. On the other hand non-

Table 2.3: Comparison between proposed and other topologies

Attributes	**[5]**	**[22]**	**[4]**	**Proposed**
Switch	1	2	4	2
Diode	1	3	4	2
Sensors	2	3	6	1
Inductor	2	2	2	2
HFT	Present	Present	Not Present	Not Present
Control	Moderate	Moderate	Complex	Simple
Peak Efficiency	83%	82%	97.6%	93.89%

isolated topology given in [4] present higher efficiencies as the application is for high voltage low current battery charging application leading to reduced current stresses. As the converter is CCM based, significant amount of sensors are required in order shape the input current and control the battery charging operation. Proposed topology mitigates such problem and achieve higher efficiency of 93.89% by using a single sensor for battery charge control in the absence of PLL results in cost effective and compact EV charging solution and can achieve even higher efficiency if implemented for high voltage low current battery charging application. Minimum number of switching components are used in high efficiency.

2.7 Conclusion

In this Chapter, a two-cell interleaved buck-boost PFC battery charging converter is proposed considering the merits of reduced input size filter and reduced peak currents. It is operated in DCM to obtain the PFC at AC mains for wide range of voltage. The steady-state operation, and design have been presented in detail. A simple voltage control loop with single output voltage sensor is used to regulate the output voltage, which makes the control simple, reliable and robust for battery charge control. The converter realized zero current turn-on of the switches, and zero diode reverse recovery losses. The converter detailed small-signal model using CIECA approach is presented to aid the controller design.

The converter analysis and design are confirmed with the simulation results using PSIM 11.1 software. It is shown that the input current is sinusoidal and in-phase with input voltage under all conditions. An experimental laboratory prototype of 1.0 kW is designed and built to further validate the simulation results. The experimental results are in good agreement with the simulation results and validating the converter analysis and design. A high efficiency of 93.89 % and an input current THD of 4.85 % are recorded at rated output power with the developed laboratory hardware prototype. A volumetric analysis is done, which shows the effect of various active and passive components on overall power density of the converter. A brief comparison between other single-stage isolated and non-isolated converters shows that the proposed configuration presents an efficiency of nearly 94% with simple control and utilizing a single sensor. Such a float charger can be extended to higher power rating of up to 2kW by integrating more cells which reduces the current stresses on semiconductor devices drastically, thus reducing the thermal management requirements. The next Chapter deals with a high efficiency two-stage battery charger with CC-CV control for low voltage battery driven EVs.

Chapter 3: A Dual-Sensor based High Efficiency Two-stage Battery Charger for Local e-Transportation

3.1 Introduction

The charger studied in Chapter 2 are easy to develop and can be a viable option for charging low voltage battery pack in countries like Germany and Japan. In countries like India, isolation becomes necessary due to the presence of the weak grid and lack of proper earthing system. Single-stage isolated chargers have been reported in literature but they suffer with poor efficiency and their inability to charge battery pack in CC-CV mode [13]-[24]. Two-stage chargers have been reported in the literature but they suffer from higher number of sensors and complex control for the back-end DC-DC converter, leading to higher control burden and reduced reliability [32][33]. DCM based battery chargers for low voltage battery packs cause issues such as low efficiency and high current stress. Thus, the problems to be addressed as follows:

1. Reduced control burden in terms of PLL and sensing.
2. Reduced switching blocks in order to minimize losses.
3. Minimum number of sensors to implement a simple control.
4. High Efficiency and low input current THD should be maintained at different current levels.

Therefore, with a focus on addressing the above issues, a two-stage high efficiency battery charger is proposed in this Chapter.

3.2 Proposed Converter

Fig. 3.1 shows the proposed two-stage isolated charger configuration. First stage is an interleaved buck-boost DCM PFC converter which ensures UPF operation at all operating conditions. LC filter is connected to filter out high frequency switching harmonics and allow pure sine wave current at the input. The interleaved PFC consists of two DCM buck-boost converters in parallel which operate at 180° out of phase. This reduces the input current ripple, resulting in reduction of size and input filter. Since the input current is the sum of DCM inductor currents L_1 and L_2, inductor peak current is lowered thus reducing the turn-off losses. Interleaving inherently reduces the

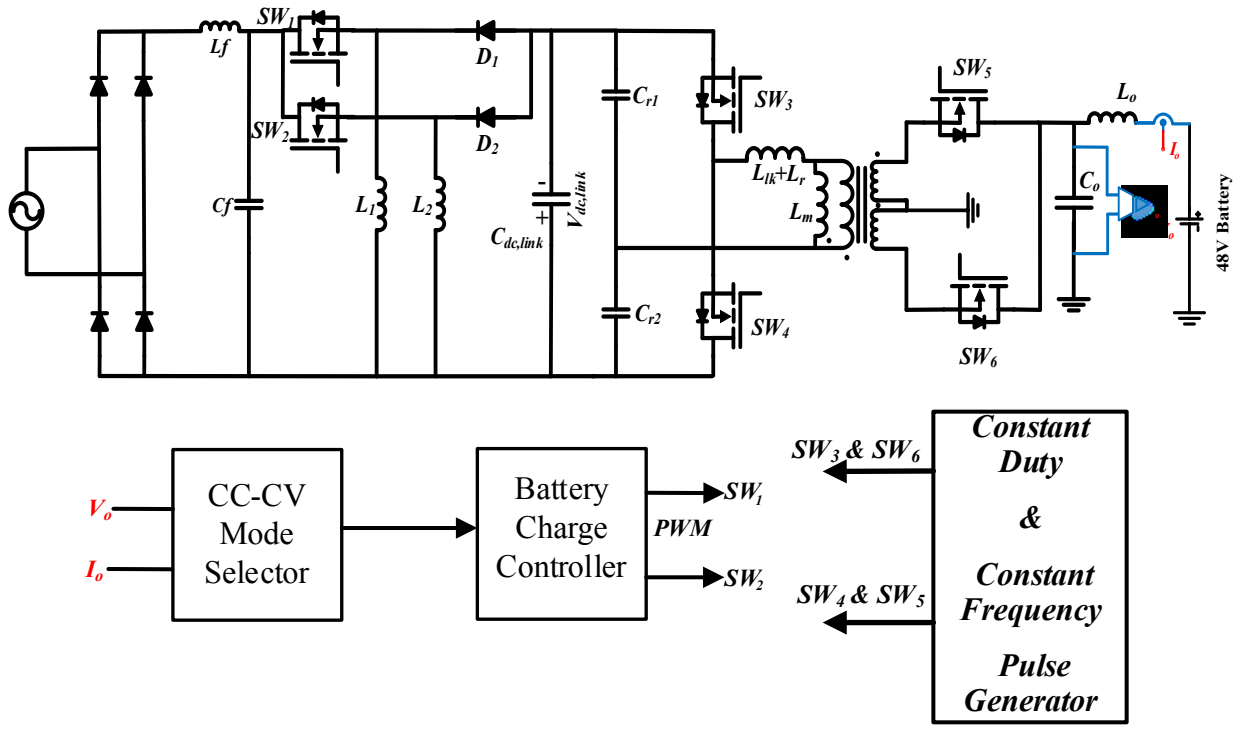


Fig. 3.1. The proposed three-phase interleaved buck-boost derived PFC converter.

conduction losses, and by operating the buck-boost converter in boost mode it cuts down the current stresses on the switch and diodes. Even though voltage stress is high across semiconductor devices, low current stress on devices lead to smaller heatsink requirement, lower conduction losses, thus leading to overall reduction of weight. Second stage is an isolated half-bridge LLC resonant converter with centre-tap transformer along with synchronous rectification on secondary. This particular topology is selected because of the following reasons:

1) Less number of semiconductor device count.
2) By splitting the resonant capacitor into two capacitors half-bridge is formed in order to reduce resonant capacitor size thus reducing number of primary turns.
3) LLC resonant tank when reflected to secondary appear as a current source [55], thus making it suitable for charging applications, along with the capability to achieve ZVS at light load.

Centre-tap transformer and synchronous rectification on secondary improves the overall efficiency and reduces cost of the converter. Generally regulated LLC resonant converters with wide operation range possess the problem of increased output voltage during hold-up time [6]. At the

output rather than connecting an LC filter which induces duty cycle loss [32], a capacitive filter is used along with an output inductor to reduce the effect of a sudden change in output current during transient operation. The proposed configuration of the battery charger has easier control than conventional chargers that require the first stage for active PFC with three sensors and the second stage purely to control the charging voltage and current [9]-[27].

The second stage is an unregulated LLC resonant DC-DC converter to provide electrical isolation and voltage step down. By operating this stage at constant duty and frequency, it not only reduces the control burden on the microcontroller in terms of voltage and current control, but also the presence of magnetizing inductance large enough allows soft switching of half-bridge FET's [6]. Thus conduction losses due to circulating currents are minimized. As the charger configuration is based on the pre-regulator concept and the second stage is a constant frequency, constant duty operated, the output of the buck-boost converter controls the total power transfer. In the absence of feedback control for DC-DC converter, it acts just as a voltage amplifier with a fixed gain, thus operating with minimum switching losses. As the stress on all semiconductor devices tend to increase or decrease based on dc-link voltage $V_{dc,link}$, it needs to be optimized to achieve a high overall efficiency of the converter. The method for dc-link voltage selection is explained in the next section. The output-to-input relationship of the proposed configuration is a product of individual gains of two stages and can be defined as

$$\frac{V_{dc,link}}{V_{in,pk}} \times \frac{V_{out}}{V_{dc,link}} = \frac{D}{1-D} \times n \times \left(\sqrt{\left(1+\lambda\left(1-\left(\frac{\omega_o}{\omega}\right)^2\right)\right)^2 + \left(\frac{\pi^2}{8} Q \left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)\right)^2} \right)^{-1} \quad (3.1)$$

where $Q = \frac{\omega_o L}{R_L}$, $\lambda = \frac{L_r}{L_m}$, $\omega_o = \frac{1}{\sqrt{L_r C_r}}$, $\omega = 2\pi f_{sw,HB}$. As the LLC converter switching frequency $f_{sw,HB}$ is selected same as the resonant frequency, i.e. $\omega = \omega_o$ to obtain resonant tank gain as unity and to minimize circulating current losses, (3.1) can be simplified by

$$\frac{V_{out}}{V_{in,pk}} = \frac{V_{dc,link}}{V_{in,pk}} \times \frac{V_{out}}{V_{dc,link}} = \frac{D}{1-D} \times n \quad (3.2)$$

Where D is the duty cycle of front-end converter and is same as Chapter 2 and is defined by

$$D < \left(\frac{M}{M+1}\right) \tag{3.3}$$

3.3 Optimal DC-Link Voltage Selection

In order to select an optimal dc-link voltage, it is important to derive a relation between all semiconductor devices and dc-link voltage $V_{dc,link}$ in order to minimize losses. A guideline for selecting dc-link voltage has been presented in order to operate converter efficiently.

3.3.1 Front-End Loss Analysis

The front-end converter comprises of diode bridge along with DCM buck-boost inductors. Fig. 3.2 shows inductor current $i_L(t)$, voltage stress across the switches and diode current for one leg

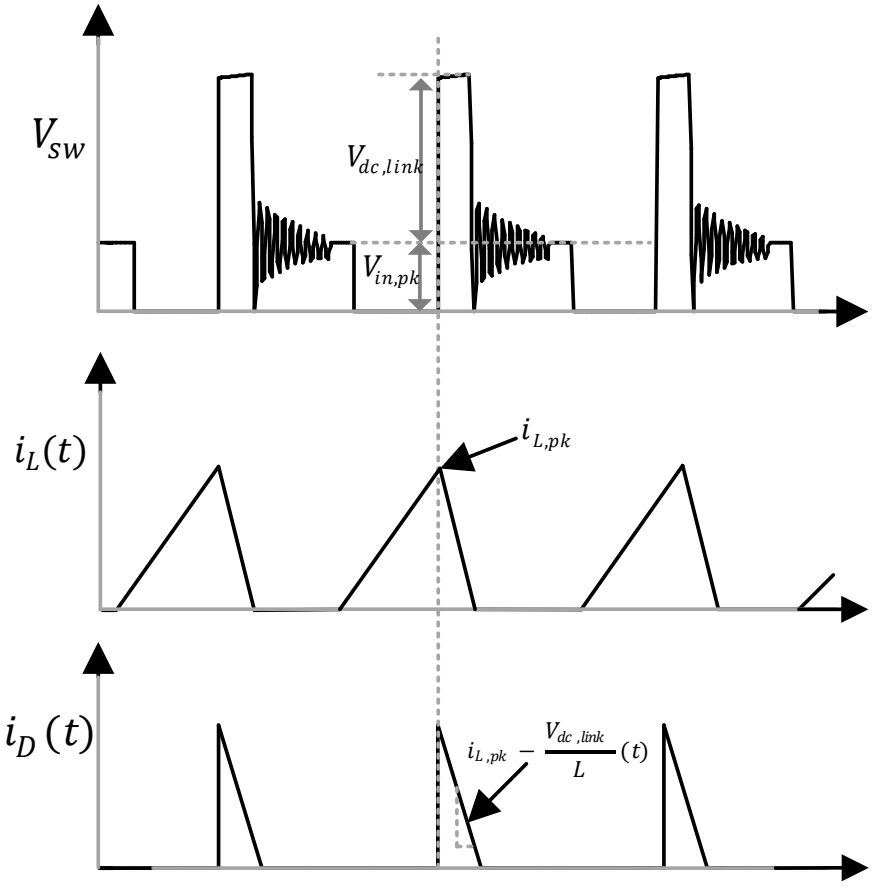


Fig. 3.2. Key waveforms for front-end converter for one-cell.

of the converter. To maintain the converter symmetricity and simplify analysis, it is considered that both cells are identical and inductor values of both the cells are same defined by (3.4)

$$L_1 = L_2 = L \tag{3.4}$$

Design of this inductor does not depend on the ripple as the inductor needs to be charged and discharged during one switching cycle in order to maintain DCM condition. Assuming input voltage to be constant for one switching period, the peak inductor current $i_{L_{pk}}(t)$ as

$$i_{L_{pk}}(t) = \frac{V_{in} D T_{sw,BB}}{L}(t) \tag{3.5}$$

The average output current of the first stage interleaved buck-boost is the average diode current of both diodes which is given by

$$I_{o,BB} = \frac{V_{in,pk}^2 \, D^2 T_{sw,BB}}{2 L V_{dc,link}} \tag{3.6}$$

To ensure DCM operation of both inductors, value of L can be given as

$$L < \frac{V_{in,pk}^2 \, D^2 T_{sw,BB}}{2 P_o} \tag{3.7}$$

By using (3.6) and applying power balance, the input current expression can be given as

$$I_{in}(\omega t) = \frac{V_{in,pk} \sin(\omega t) D^2 T_{sw,BB}}{L} \tag{3.8}$$

Equation (3.8) shows that input current is sinusoidal in nature which confirms UPF operation of the front-end converter. Thus losses due to diode-bridge can be given as

$$P_{bridge} = 4\left[I_{in}^2 \times R_{D,bridge} + V_{f,d} \times I_{in}\right] \tag{3.9}$$

From Fig. 3.2 it is observed that the operation of interleaved buck-boost converter in DCM inherits the advantage of ZCS turn-on of switches, as inductor current goes to zero in every switching

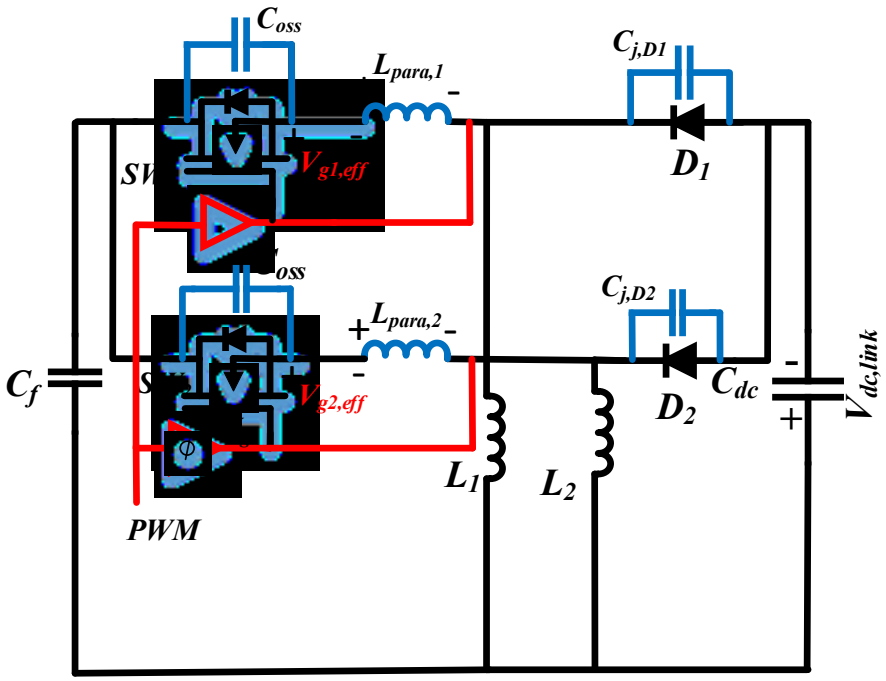


Fig. 3.3. Schematic of front-end converter using CSI consideration.

cycle. Turn-off switching losses are more due to higher peak currents due to DCM operation and are computed by considering the effect of lead inductances present on the PCB and MOSFET terminals. Common source inductances (CSI) [55] slow down the turn-off of switches, thus leading to higher switching losses. As shown in Fig. 3.3 if a common source inductance (CSI) L_{para} is present, then changes in current will affect the gate voltage in a way that is proportional to the inductance L_{para}, and the rate of change of the current. When the gate is driven off, the voltage developed across the inductance L_{para} acts to hold the gate on longer, slowing the current fall. As the switch begins to turn-off, $I_{sw,BB}$ starts decreasing and a voltage drop which is proportional to $\frac{dI_{L_{pk}}}{dt}$ is built across L_{para}. Thus the effective gate-source voltage decreases and is presented by

$$V_{g,eff} = V_{miller} - V_{g,off} - L_{para}\frac{dI_{DS}}{dt} \tag{3.10}$$

In order to account for losses due to CSI, let us consider the area Q_{GD} during the time interval t_1 from Fig. 3.4. The buck-boost diode output capacitance C_{j,D_1} is charged, and the current flows through L_{para}. This current decreases the effective gate-source voltage of the MOSFET, hence

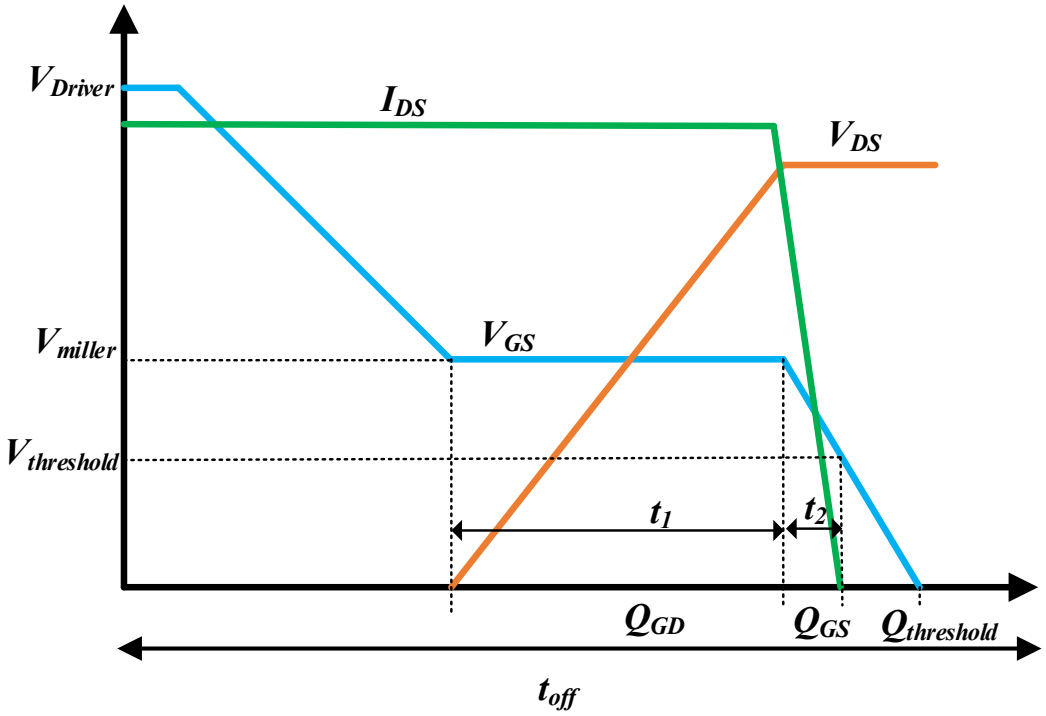


Fig. 3.4. Waveformat device turn-off.

the gate current $I_{g_2,off}$ can be computed, by considering $V_{L_{para(t1)}}$ across CSI. The diode capacitance current, CSI voltage and gate current can be obtained as follows

$$I_{j,D_1} = C_{j,D} \times \frac{V_{in} + V_{out}}{dt_1} = \frac{Q_{j,D}}{dt_1} \tag{3.11}$$

$$dt_1 = T_{off,BB} = \frac{Q_{GD,BB}}{I_{g_{1,off}}} \tag{3.12}$$

$$V_{L_{para(t1)}} = L_{para}\frac{dI_{j,D_1}}{dt_1} = \frac{L_{para}Q_{j,D_1}I_{g_{1,off}}{}^2}{Q_{GD,BB}{}^2} \tag{3.13}$$

$$I_{g_1,off} = \frac{V_{miller} - V_{L_{para(t1)}}}{R_{g,driver} + R_{g,switch}} \tag{3.14}$$

Solving (3.15), and taking most positive real roots, $I_{g_1,off}$ is computed

$$aI_{g_1,off}^2 + bI_{g_1,off} + c = 0 \tag{3.15}$$

where

$a = \frac{L_{para} Q_{j,D_1}}{Q_{GD,BB}^2}$; $b = R_{g,driver} + R_{g,switch}$; $c = -\left(V_{miller} - V_{g,off}\right)$;

During interval t_2, Q_{GS} area is analyzed. When the gate-source voltage reaches miller plateau voltage V_{miller} , device current I_{DS} starts decreasing and reaches 0 at the end of t_2. This change of current induces $V_{L_{para(t2)}}$ due to CSI L_{para} . $V_{L_{para(t2)}}$ and $I_{g_2,off}$ during t_2 can be computed by

$$V_{L_{para(t2)}} = L_{para} \frac{dI_{DS}}{dt_2} = L_{para} \times \frac{I_{L_{1,pk}}}{dt_2} \tag{3.16}$$

$$I_{g2(off)} = \frac{V_{miller} - V_{L_{para(t2)}}}{R_{g,driver} + R_{g,switch}} \tag{3.17}$$

$$dt_2 = \frac{Q_{GS.BB}}{I_{g_2,off}} \tag{3.18}$$

$$I_{g_2,off} = \frac{V_{miller}}{R_{g,driver} + R_{g,switch} + L_{para} \frac{I_{L_{1,pk}}}{Q_{GS,BB}}} \tag{3.19}$$

It is observed that turn-off losses also depend on the gate driver resistance $R_{g,driver}$ and switch gate resistance $R_{g,switch}$. The time period t_2 is critical as switch current starts decreasing during that instant. By referring the datasheet for the particular switch, output capacitance is calculated, and hence gate resistance $R_{g,driver}$ is computed to minimize the time constant for the faster turn-off. Hence, turn-off losses for both buck-boost MOSFETs are given by

$$P_{SW_{BB},off} = V_{sw,avg} I_{SW_{BB},rms} f_{SW,BB} \left(\frac{Q_{GD,BB}}{I_{g_1,off}} + \frac{Q_{GS,BB}}{I_{g_2,off}} \right) \tag{3.20}$$

where a method to estimate various MOSFET parameters are given in [56].

Besides the turn-off losses, the switching losses due to both MOSFET output capacitance $C_{oss,BB}$ can be given as

$$P_{coss,BB} = \frac{1}{2} \times C_{oss,BB} f_{SW,BB} \int_0^{2\pi} C_{oss,BB} v_{sw}^2 (\omega t) \tag{3.21}$$

FET conduction losses can be calculated by the RMS current expression that can be derived by examining the waveform in Fig (3.2), and can be expressed are given as

$$I_{SW_{BB},rms} = \frac{V_{in,pk} D}{L f_{SW,BB}} \sqrt{\frac{D}{6}} \tag{3.22}$$

$$P_{SW_{BB},cond} = 2\left(I_{SW_{BB},rms}\right)^2 \times R_{DS,on,BB} \tag{3.23}$$

As the front-end converter is operating DCM, both the inductor core loss and winding losses are significant due to large flux swing and high RMS current through inductor windings. Inductor core loss estimation for any DCM converter can be given by [57], thus losses are computed as

$$P_{L,losses} = 2\left[P_{c,limit} \times V_e + I_{L,rms}^2 \times R_{DCR}\right] \tag{3.24}$$

where

$$I_{L,rms} = \frac{V_{in,pk} D}{L f_{SW,BB}} \sqrt{\frac{D}{18\pi V_{dc,link}} \left(3\pi\left(V_{dc,link} - 1\right) + 8V_{in,pk}\right)} \tag{3.25}$$

Diode buck-boost losses comprise of turn-on losses, conduction losses, and reverse recovery losses. As the operation of the PFC converter is in DCM, reverse recovery losses are zero as the current is zero in every switching cycle as shown in Fig. 3.2. Turn-on losses can be calculated as the product of average current $I_{d,avg}$ and forward voltage V_f whereas the conduction losses can be calculated by estimating the resistance of the diode [58] and is given as

$$P_{diode_{loss},BB} = 2\left[\left(I_{d,rms}\right)^2 \times R_d + \left(I_{d,avg} \times V_f\right)\right] \tag{3.26}$$

where

$$I_{d,rms} = \frac{V_{in,pk} D T_{sw,BB}}{L} \sqrt{\frac{D}{3\pi V_{dc,link}} \left(\frac{4V_{in,pk}}{3} - \frac{\pi}{2}\right)} \tag{3.27}$$

$$I_{d,avg} = \frac{V_{in,pk}^2 D^2 T_{sw,BB}}{4 L V_o} \tag{3.28}$$

The RMS current flowing through the dc-link capacitive filter is the difference between the diode RMS currents and the average output current which can be calculated as

$$I_{C_{dc,link},rms} = \frac{V_{in,pk} D T_{sw,BB}}{L} \sqrt{\frac{V_{in,pk} D}{V_{dc,link}} \left(\frac{8}{9\pi} - \frac{V_{in,pk} D}{4 V_{dc,link}} \right) - \frac{D}{3 V_{dc,link}}} \tag{3.29}$$

Thus loss due to capacitor ESR is given as

$$P_{C_{dc,link}} = I_{c,rms}^2 \times R_{C_{dc,link} ESR} \tag{3.30}$$

3.3.2 Back-end Loss Analysis

Fig. 3.5 shows the resonant current and the magnetizing current of the LLC resonant converter. The resonant current $i_r(t)$ can be expressed as

$$i_r(t) = \sqrt{2} I_{pri,rms} sin(\omega t - \varphi) \tag{3.31}$$

where $\omega = \frac{2\pi}{T_{sw,HB}}$

Since the output voltage clamps the magnetizing inductor in the first half of a PWM cycle and negative output voltage in the second half, it can be reduced to

$$i_{L_m}(t) = \begin{cases} -I_{L_m,pk} + \frac{V_o}{n L_m} t, & 0 < t < \frac{T_{sw,HB}}{2} \\ I_{L_m,pk} - \frac{V_o}{n L_m} \left(t - \frac{T_{sw,HB}}{2} \right), & \frac{T_{sw,HB}}{2} < t < T_{sw,HB} \end{cases} \tag{3.32}$$

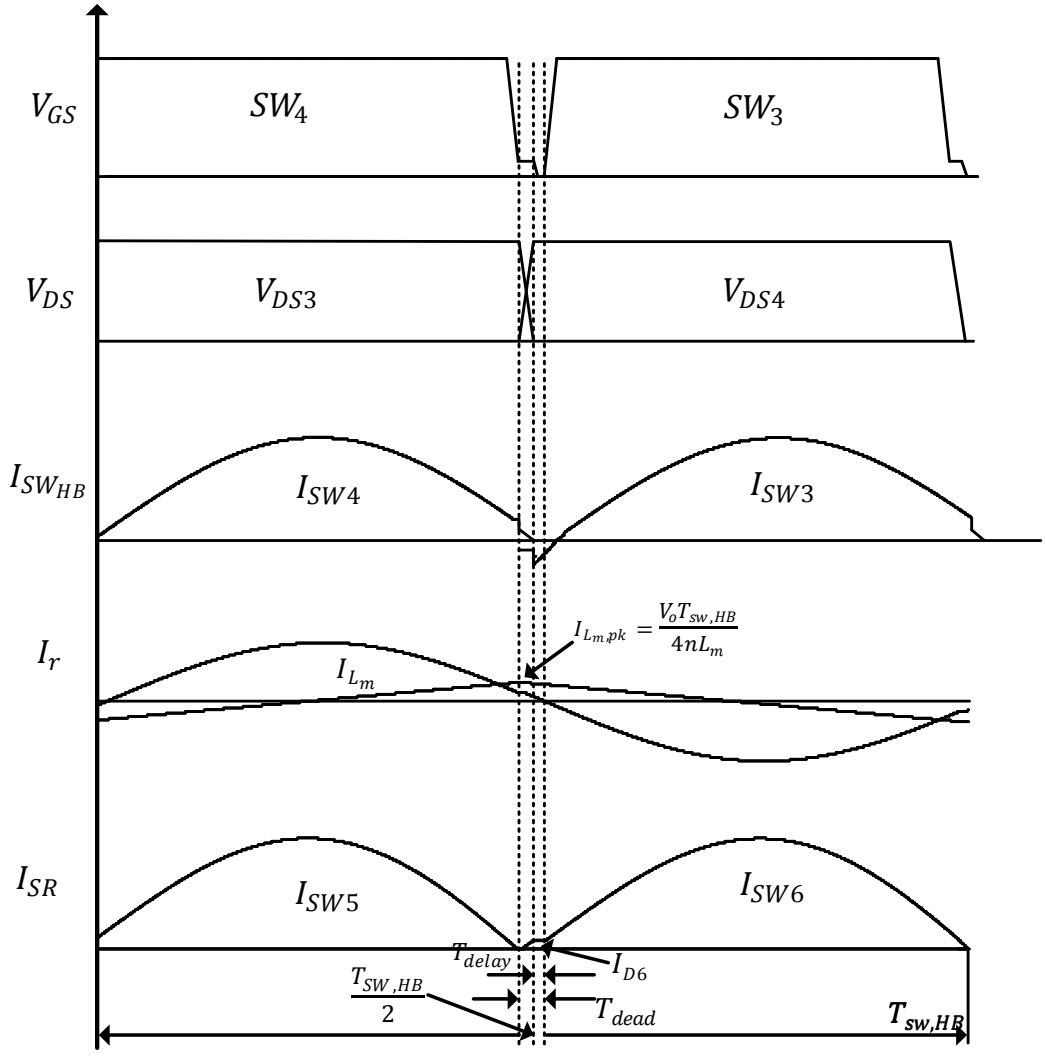


Fig. 3.5 Switching waveforms for Unregulated LLC converter

At time t, $i_{L_m}(t)$ is equal to the peak magnetizing current $I_{L_m,pk}$, which is given by

$$I_{L_m,pk} = \frac{V_o T_{sw,HB}}{4nL_m} \tag{3.33}$$

At time t= $T_{sw,HB}$, the resonant current equal to the magnetizing current which is given by

$$\sqrt{2} I_{pri,rms} sin(-\varphi) = -\frac{V_o T_{sw,HB}}{4nL_m} \tag{3.34}$$

The difference between i_r and i_{L_m} is the current flowing through the switch and is supplied to the load which is given by

$$\frac{2}{T_{sw,HB}}\int_0^{2/T_{sw,HB}}\left(\sqrt{2}I_{pri,rms}sin(\omega t-\varphi)+\frac{V_oT_{sw,HB}}{4nL_m}-\frac{V_o}{nL_m}t\right)dt=\frac{nV_o}{R_L} \tag{3.35}$$

$$I_{sw_{HB},rms}=\frac{nV_o}{8R_L}\sqrt{\frac{2{R_L}^2}{n^4L_m^2f_{sw,HB}^2}+8\pi^2} \tag{3.36}$$

Thus, both primary switch conduction losses can be given by

$$P_{HB,cond}=\left(I_{sw_{HB},rms}\right)^2\times R_{DS,HB} \tag{3.37}$$

As the LLC converter achieves ZVS turn-on, the switching losses only comprises of losses due to turn-off. From Fig. 3.5, it is observed that when switch SW_4 turns off, it experiences linear operation. As the slope of V_{DS4} determines the slope of V_{DS3} , the discharge current through drain-source capacitance can be given as

$$I_{SW,3}=-C_{oss,HB}\frac{V_{dc,link}}{T_{off,HB}} \tag{3.34}$$

$T_{off,HB}$ can be calculated by the same analysis as per section 3.3.1 using Fig. 3.6

The current during turn-off of switch SW_4 can be given as

$$I_{SW_4,off}=I_{L_m,pk}+I_{SW,3} \tag{3.38}$$

$$=\frac{V_oT_{sw,HB}}{4nL_m}-C_{oss,HB}\frac{V_{dc,link}}{T_{off,HB}} \tag{3.39}$$

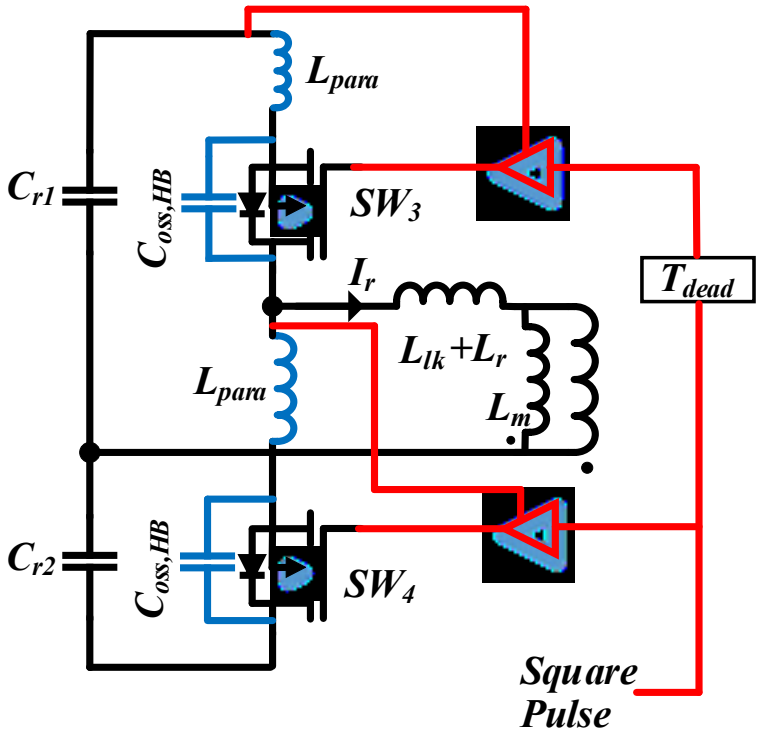


Fig. 3.6. Schematic of back-end converter using CSI consideration.

From (3.39) switching losses can be calculated. Considering both switches identical and same, the switching losses for primary side switches is given by

$$P_{SW_{HB},off} = 0.1667 \times f_{sw,HB} \times V_{dc,link} \left(\frac{V_o}{4nL_m f_{sw}} - \frac{C_{oss.HB} V_{dc,link}}{\left(\frac{Q_{GS,HB}}{I_{g_3,off}} + \frac{Q_{GD,HB}}{I_{g_4,off}} \right)} \right) \times \times \left(\frac{Q_{GS,HB}}{I_{g_3,off,HB}} + \frac{Q_{GD,HB}}{I_{g_4,off,HB}} \right) \quad (3.40)$$

It is observed that both the conduction and switching losses are directly dependent on the magnetizing current I_m. Higher magnetizing current leads to higher conduction losses as circulating current is high. On the other hand low magnetizing current leads to loss of soft-switching. Thus, the proper value of magnetizing inductance L_m need to be selected. L_m energy should be high enough to discharge the output capacitance of primary switches. Too high inductance can cause low currents during dead-time which leads to bigger core size and loss of

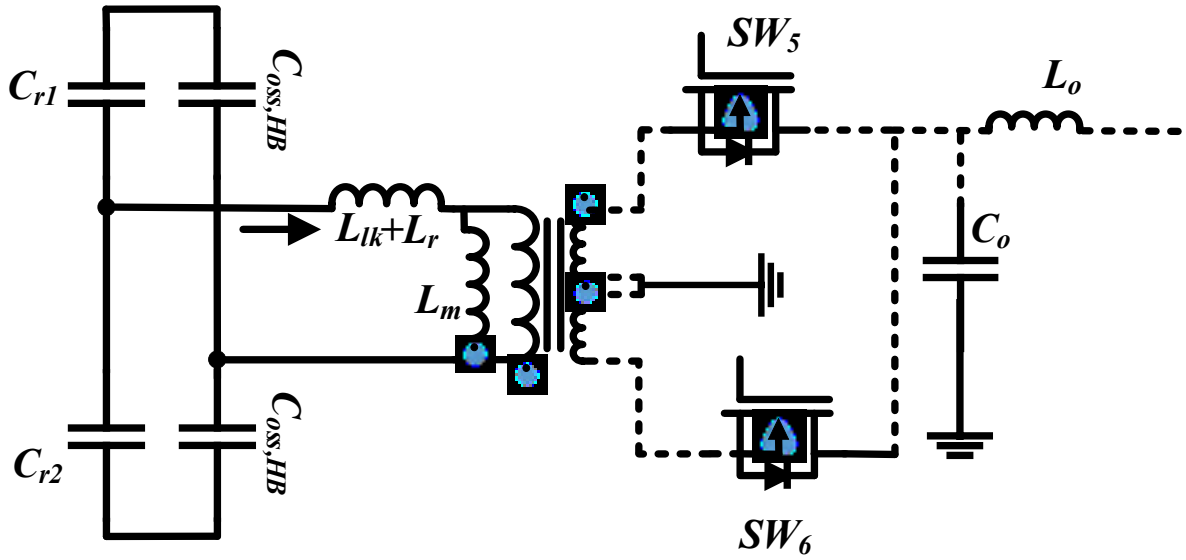


Fig. 3.7 The Equivalent circuit of back-end during dead-time.

soft switching [6]. The equivalent circuit during dead-time is shown in Fig. 3.8. Thus L_m can be calculated as

$$L_m < \frac{V_O T_{dead} T_{sw,HB}}{8nC_{oss,HB}V_{dc,link}} \tag{3.41}$$

Equation (3.41) guarantees ZVS and loss analysis is performed by considering the above assumption.

As the proposed charger is for low-voltage high-current applications, secondary losses become significant and are accounted for in the loss analysis. Because of synchronous rectification switching losses are zero and losses are mainly dominated by the conduction losses in the switch secondary side RMS current can be given by

$$I_{SR,rms} = \frac{\sqrt{3}V_o}{24\pi R_L}\sqrt{12\pi^4 + \frac{(5\pi^2 - 48)R_L^2 T_{SW,HB}^2}{n^4 L_m^2}} \tag{3.42}$$

Thus, secondary switches conduction losses can be given by

$$P_{cond,SR} = \left[I_{SR,rms}^2 \times R_{DS,SR} + (2 \times T_{delay} \times I_{SR,rms} \times f_{SW,HB} \times V_{f,SR}\right] \tag{3.43}$$

where T_{delay} is the time in which the body diode of SR switch conducts. This time is the duration required to charge the gate-source capacitance of the switch and is given by

$$T_{delay} = \frac{Q_{GS,SR}}{I_{g,on}} \tag{3.44}$$

The RMS ripple current through output capacitor can be given as the difference between the secondary resonant current and average output current which can be given as

$$I_{C_o,rms} = \frac{V_o}{R_L}\sqrt{\frac{1}{96\pi}\left(12\pi^4 + \frac{(5\pi^2 - 48)R_L^2 T_{SW,HB}^2}{n^4 L_m^2}\right) - 1} \tag{3.45}$$

$$P_{C_o} = I_{C_o,rms}^2 \times R_{C_o,ESR} \tag{3.45}$$

3.3.3 Battery Charging profile

To design the converter with the proper voltage and current limits, it is important to understand the battery dynamics. As a practical battery was not available for experimentation, it is important to understand the feasibility of the proposed charger for battery charging applications. The proposed battery charger is for a low voltage battery charging application that uses 850 W motor

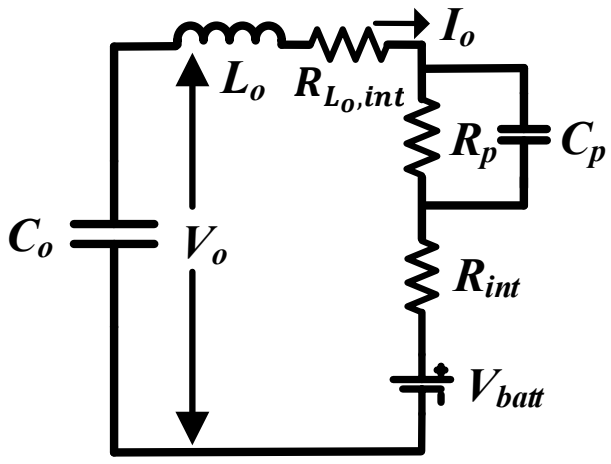


Fig. 3.8 Battery Equivalent circuit when connected to battery charger.

that is powered by four 12V series-connected, 120 Ah VRLA lead-acid battery packs [59]. By observing the C/7 discharge rate for 120Ah battery [59], the allowable depth-of-discharge (DOD) is 20% for VRLA battery, as below this point the battery voltage drops sharply i.e. below 11 V point. Moreover, lead-acid battery packs when discharged, have higher internal resistance as lead sulphate is accumulated over the electrodes. With a rise in battery voltage, the concentration of sulphuric acid increases thus decreasing the effective internal resistance. So in general it can be said that for any battery, internal resistance is a function of state-of-charge (SOC) of the battery [60]. Battery resistance of a lead-acid battery pack decreases exponentially to SOC [60]. With only 20% DOD allowed, internal resistance remains relatively constant for higher SOC and temperatures [61]. The battery equivalent model when connected to a battery charger is shown in Fig. 3.8.

The battery equivalent circuit is represented by a parallel combination of self-discharge resistance R_p and storage capacitor C_p which describes the total energy stored in the battery. Equivalent internal resistance R_{int} is connected in series with a dc voltage source representing the battery voltage. Value of C_p can be calculated by

$$C_p = \frac{kWh * 3600 * 1000}{0.5(V_{batt,max}^2 - V_{batt,min}^2)} \tag{3.46}$$

In the above expression by substituting $V_{batt,max}$ and $V_{batt,min}$ equal to 56 V and 44 V respectively which are the charged/discharged voltages of a 48 V, 120 Ah VRLA battery pack [4], C_p can be obtained as $3.456 \times 10^4 F$. Self-discharge resistance is taken to be 10kΩ [4], thus the effective impedance of the parallel network is very low, hence the voltage drop is neglected across that network. By applying kirchoff's voltage law (KVL) and neglecting the voltage drop across the series resistance $R_{L_o,int}$ of the inductor L_o , we get

$$I_o R_{int} + V_{batt} = V_o \tag{3.47}$$

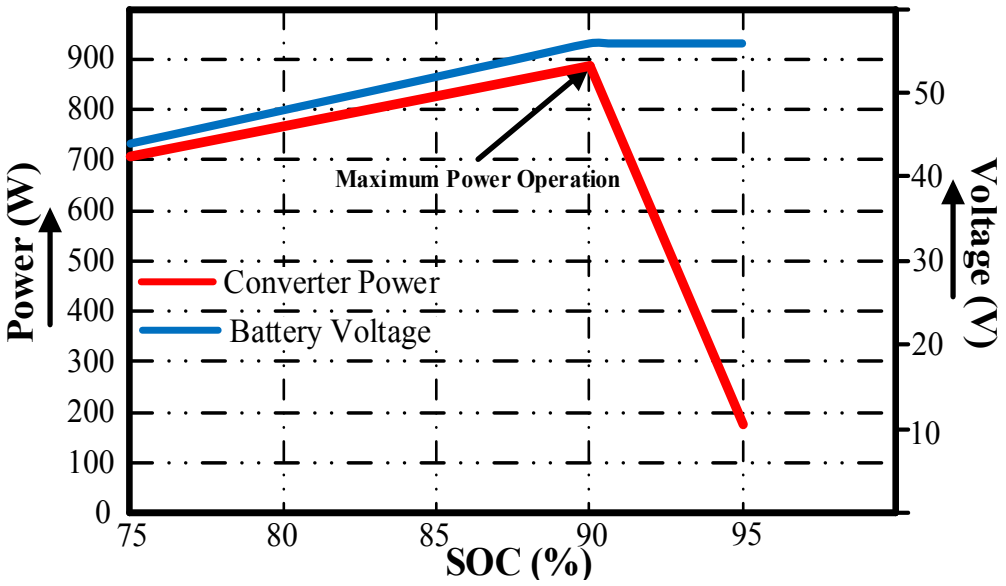


Fig. 3.9 Variation of converter power and battery voltage with respect to SOC.

Output voltage for converter needs to be designed with the worst case which occurs when the converter operates with maximum power where the battery is fully charged and charging current is high as shown in Fig. 3.9. Considering a total internal resistance R_{int} of 0.16Ω for a battery voltage of 56V [61], with a charging current of 15 A [59], the required output voltage can be computed to be 58.4V. The entire process of battery charging is controlled by a battery management system (BMS) in sophisticated battery chargers in order to maintain battery health.

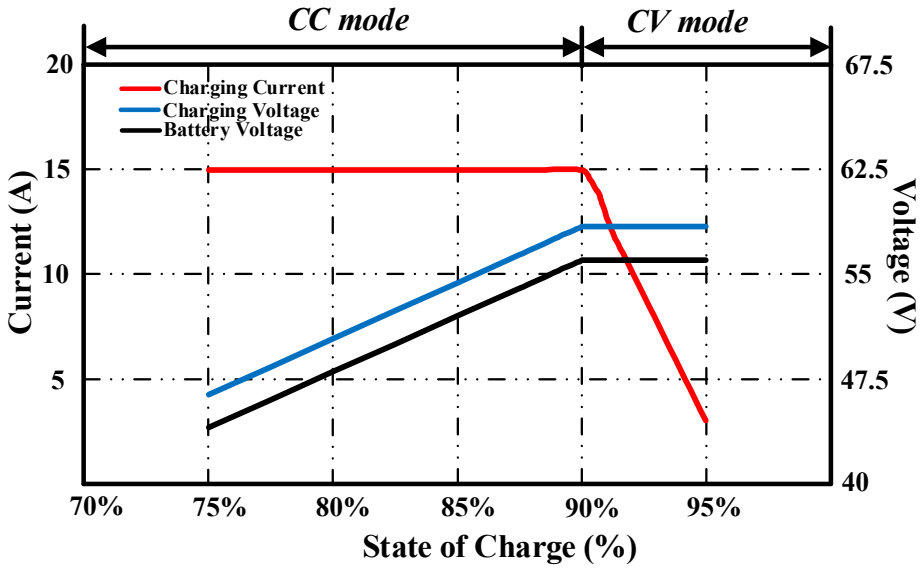


Fig. 3.10 Charging profile of lead acid battery pack.

Such BMS system controls the CC-CV mode of charging by ensuring battery cell voltage balancing, thus providing protection against overheating and overvoltage. Even though such systems are present, battery aging is one such issue which is more prominent in lead-acid battery. Due to low DOD and repetitive charging of VRLA batteries, battery gets heated up often, leading to increased internal resistance R_{int} with time. Due to increase in R_{int} voltage drop across the resistance, thus higher charging voltage is required in order to charge the battery pack. An output voltage of 65 V is selected assuming these voltage margins and physical constraints such as temperature and wire resistance. It should be noted that any battery charger should be efficient over a range of power and should exhibit high efficiency from 80 % of the rated power to 10%. High efficiency at light load becomes a crucial aspect of designing a battery charger.

Fig. 3.10 shows the battery charging profile for a 48 V, 120 Ah battery. Charging starts when the output capacitor senses a voltage of 44 V or below. Current control is initiated by sensing the battery voltage (CC mode) which ensures a constant current flow of 15 A into the battery. CC mode is enabled until the battery voltage reaches up to 56.4 V with 14.1 V for each battery [62]. The converter operates with maximum power at this point as indicated in Fig 3.10. From [62] it is noted that the temperature rise is not significant for a battery voltage of 14.1 V as compared to other charging voltage levels where temperature increases significantly for every 10% rise in SOC. This voltage is known as the boost voltage of the battery and the charge mode is shifted to constant voltage (CV) mode where it holds the same battery voltage of 56.4V. As the battery gets charged, its opposition to charge current is high in the absence of the current controller. Thus the charging current starts tailing off when a constant voltage is applied across the battery terminals. As the current reaches a value equal to 20% of the initial charging current, the charging process is terminated. At this point, the battery is considered to be 95% charged.

The proposed converter is designed as per the specifications listed in Table 3.1. Based on the loss analysis equations derived from the above sections, and using the components and parameters

Table 3.1: Design Specifications.

Parameters	Value
P_o	1.0 kW
$V_{in,rms}$	110 V
$f_{SW,BB}$	50 kHz
V_o	65 V
$f_{SW,HB}$	50 kHz

Table 3.2: Actual parameters and for loss analysis.

Parameter	Value	Parameter	Value	Parameter	Value
$R_{g,switch}$	9 Ω	V_f	0.8 V	$V_{f,SR}$	1.6 V
$Q_{GD,BB}$	18 nC	$R_{DS,HB}$	80 mΩ	L_m	150 µH
$Q_{GS,BB}$	17 nC	$Q_{GD,HB}$	11 nC	$R_{C_o,ESR}$	31.8/18mΩ
$R_{DS,on,BB}$	75 mΩ	$Q_{GS,HB}$	19 nC	R_L	4.225 Ω
R_{DCR}	15 mΩ	$C_{oss,HB}$	77pF	V_{miller}	8 V
$R_{C_{dc,link}ESR}$	34.7/12mΩ	$C_{oss,SR}$	640 pF	$R_{g,driver}$	7.5 Ω
R_D	98 mΩ	$R_{DS,SR}$	28 mΩ	$P_{e,limit}$	500mW/cm^3
L_{para}	4nH	V_e	0.559cm^3		

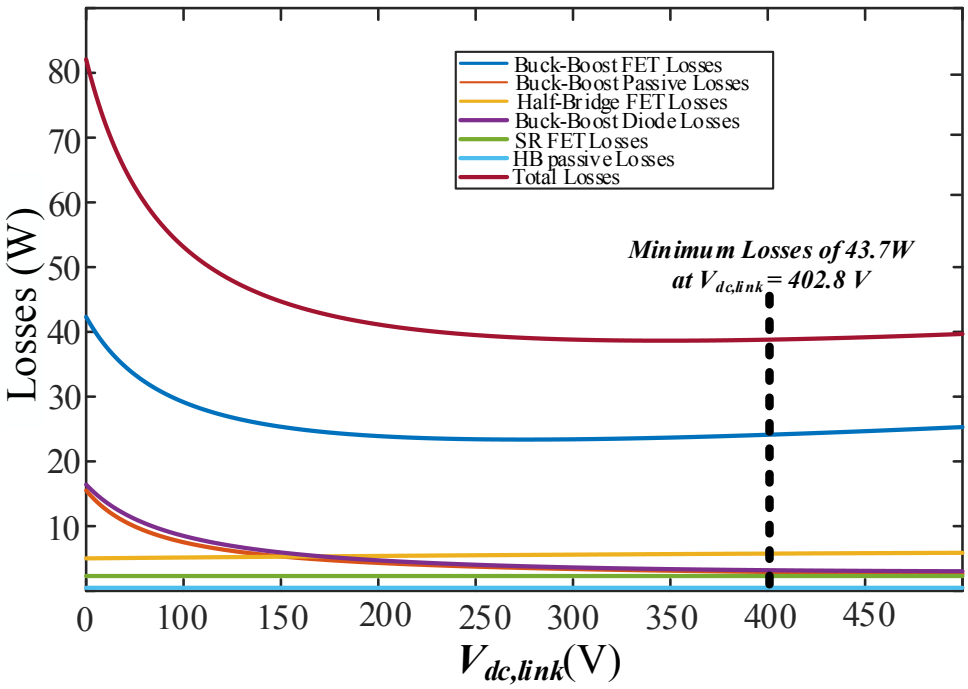


Fig. 3.11 Calculated Losses according to various DC-Link Voltages.

listed in Table 3.2, optimal DC-Link is selected as shown in Fig 3.11. At a dc-link voltage of 402.7 V the total losses are 43.7 W. It is observed that the interleaved buck-boost losses tend to increase significantly from the obtained optimal point due to high voltage stresses on semiconductor devices even though other losses reduce drastically. A dc-link voltage of 400 V is selected to design the proposed charger and the passive components are designed accordingly. On the selection of optimum dc-link voltage, the transformer turns ratio n can be calculated from (3.2).

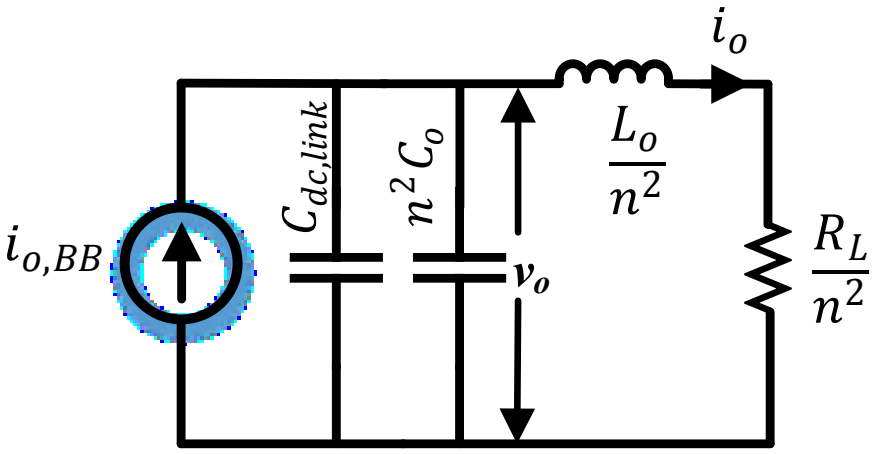


Fig. 3.12 CIECA Equivalent Model.

3.4 Small-Signal Model of Proposed Charger

As stated earlier, the small-signal model of the proposed converter is less complex as the second stage acts as a voltage amplifier with a gain proportional to the turns ration n, neglecting the dynamics offered by L_r and C_r. Thus, the secondary side state variables can be referred to as the primary as shown in Fig 3.12. The current injected equivalent circuit approach (CIECA) [51],[52],[53] is used to model the charger dynamic model. This modeling approach is simpler with respect to the state-space average model as it only accounts for the transfer characteristics of the converter. By considering the battery equal to R_L , and applying perturbations to (3.6) and neglecting the second order terms,

$$\hat{\imath}_{o,BB} = \frac{V_{in,pk}^2 DT_{sw,BB}}{LV_{dc,link}}\hat{d} + \frac{V_{in,pk}D^2T_{sw,BB}}{LV_{dc,,ink}}\hat{v}_{in,pk} \tag{3.48}$$

From Fig. 3.12 we know that

$$\hat{\imath}_{o,BB} = \left(s(C_{dc,link} + n^2C_o) + \frac{n^2}{sL_o + R_L}\right)\hat{v}_o \tag{3.49}$$

On equating (3.48) and (3.49) and substituting $\hat{v}_{in,pk}$= 0, CV mode transfer function to control the output voltage of the converter is given by

$$\frac{\hat{v}_o}{\hat{d}} = \frac{V_{in,pk}^2 DT_{sw,BB}(sL_o + R_L)}{LV_{dc,link}(s^2L_o(C_{dc,link} + n^2C_o) + sR_L(C_{dc,link} + n^2C_o) + n^2)} \tag{3.50}$$

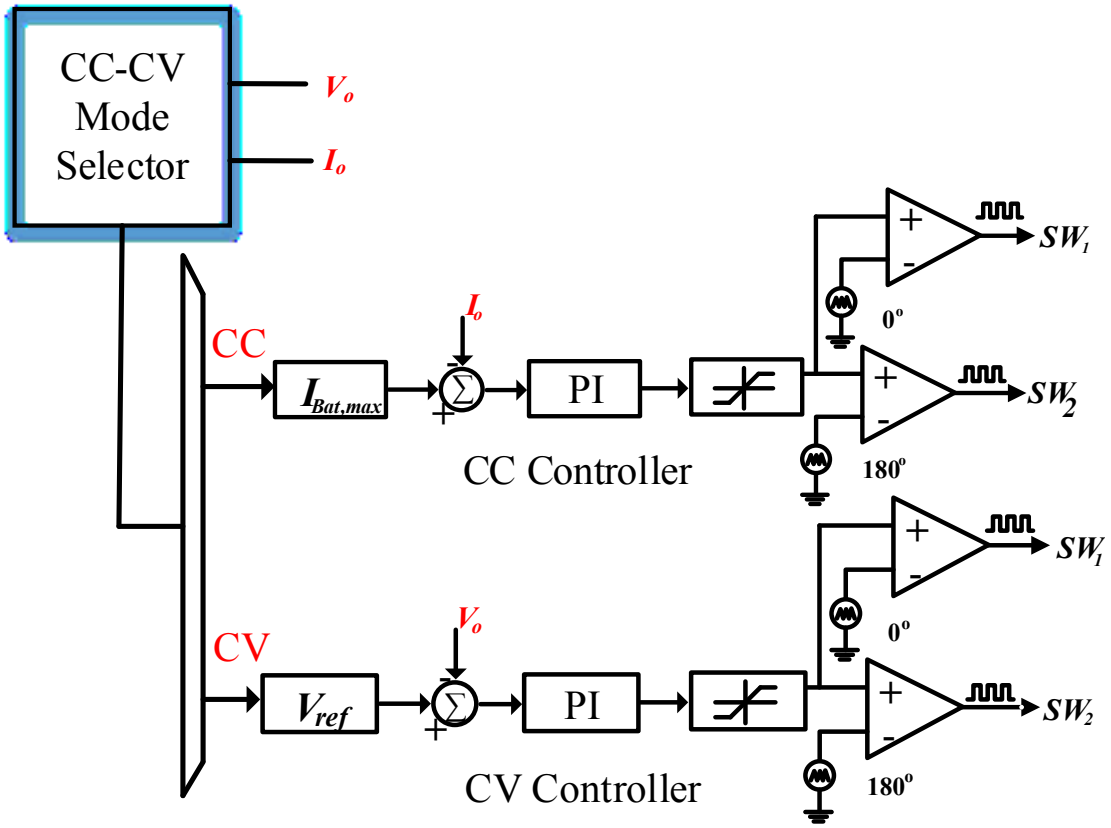


Fig. 3.13 CC-CV Charge Controller

In order to control the charging current of the converter, L_o current is controlled. From Fig. 3.12 the charging current expression can be given as

$$\hat{\imath}_o = \frac{n^2 \hat{v}_o}{sL_o + R_L} \tag{3.51}$$

On substituting $\hat{v}_o$ from (3.50), CC mode transfer function to control the charging current is given as

$$\frac{\hat{\imath}_o}{\hat{d}} = \frac{n^2 V_{in,pk}^2 D T_{sw,BB}}{L V_{dc,link}(s^2 L_o(C_{dc,link} + n^2 C_o) + sR_L(C_{dc,link} + n^2 C_o) + n^2)} \tag{3.52}$$

Fig. 3.14 shows the control scheme for the proposed battery charger. Charging is initiated and follows the charge control algorithm as per Fig. 3.13. As primary switches are directly controlling the charging voltage and current along with drawing sinusoidal input current, the bandwidth of the

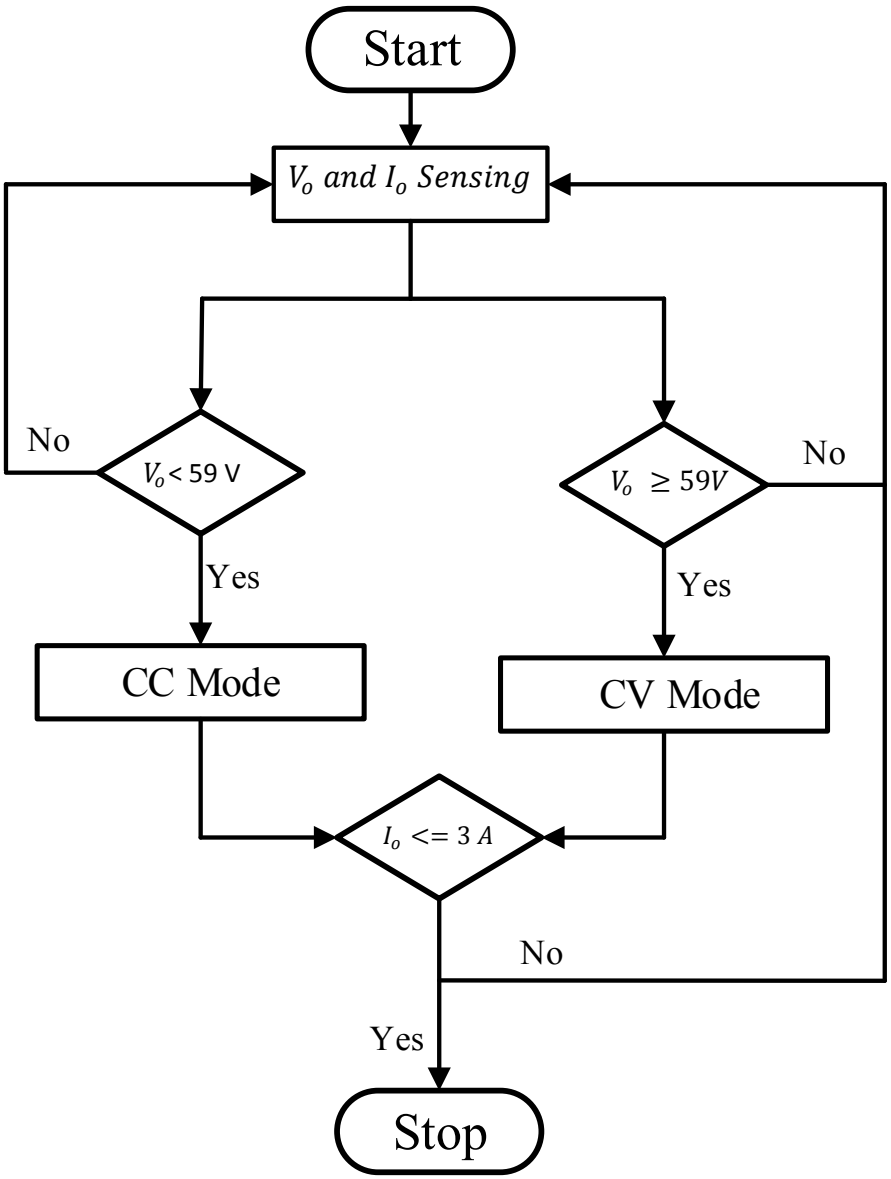


Fig. 3.14 CC-CV mode selector algorithm

controller is selected to be less than 120 Hz. PI controllers are used to controlling the charging current and voltage with a phase margin of 60° and 70° respectively.

3.5 Results and Discussion

This section presents the simulation and experimental results of the proposed converter along with a comparison with other state-of-art topologies.

3.5.1 Simulation Results

This sub-section presents the simulation results of the proposed battery charger using PSIM 11.1 software. The converter is designed with the specifications mentioned in Table 3.1, and the designed parameters are given in Table 3.4. The input LC low-pass filter is designed for a cut-off frequency of 10 kHz. The control-to-output current and control-to-output voltage to control transfer function is obtained by and is given by (3.53) and (3.54)

$$I(s) = \frac{\hat{\imath}_o}{\hat{d}} = \frac{8.96}{9.64e^{-7}s^2 + 0.0109s + 1} \tag{3.53}$$

$$V(s) = \frac{\hat{v}_o}{\hat{d}} = \frac{0.0305s + 343.74}{9.64e^{-7}s^2 + 0.0109s + 1} \tag{3.54}$$

For a double pole system, a simple PI controller is sufficient to get the desired response. The controller transfer function is designed at a phase margin 60^0, and gain crossover frequency 80 Hz. Fig. 3.15 and Fig. 3.16 shows the frequency response of plant transfer function I(s) and G(s), controller transfer function H(s), and the open-loop transfer function I(s)*H(s). Both open-loop

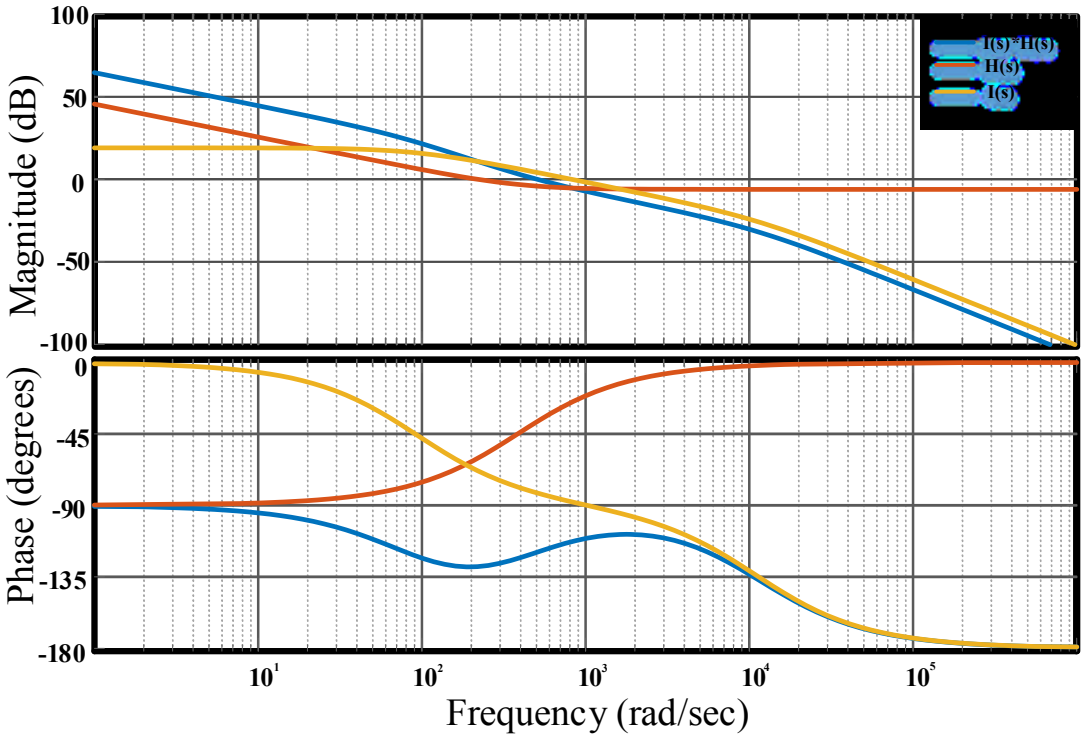


Fig. 3.15 Frequency response of plant I(s), controller H(s) and open loop I(s)*H(s).

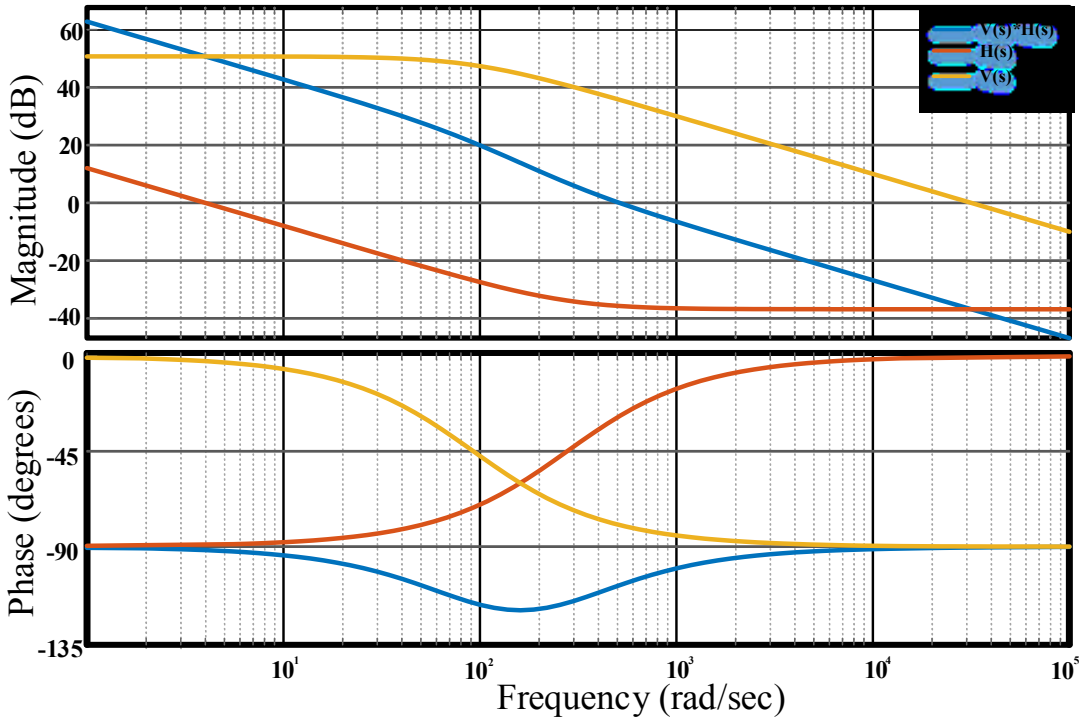


Fig. 3.16 Frequency response of plant V(s), controller H(s) and open loop V(s)*H(s).

transfer function has an infinity dc gain which indicates the system reference tracking with zero steady-state error, and the system robustness for the input and load disturbances.

With the designed controller, a closed-loop simulation for the proposed converter is done using PSIM11 software, and the results are depicted in Fig. 3.17. Fig. 3.17 (a) shows the input current and input voltage waveform during the CC mode of operation. It is observed that input current and the voltage are sinusoidal and in-phase with each other confirming the UPF operation of the charger. Fig. 3.17(b) shows the converter output voltage, and charging current waveforms at rated output power. The output current is constant and settled at reference current of 15 A. Fig. 3.17(c) and Fig. 3.17 (d) shows the current controller response during input voltage variation from 110 V to 80 V and 110 V to 130 V. Output current is maintained at constant 15 A and the input current is closely tracking the input voltage both being in-phase and shape. The output current is stable and tracking the reference current with a settling time of 15ms, which confirms the robustness of the designed current controller. Fig. 3.17(e) shows the input inductor current waveforms at rated output power, the inductor currents are discontinuous thus validating the design. Fig. 3.16 (f) shows the converter response for 10% load perturbation from 1 kW to 100 W which is the turning

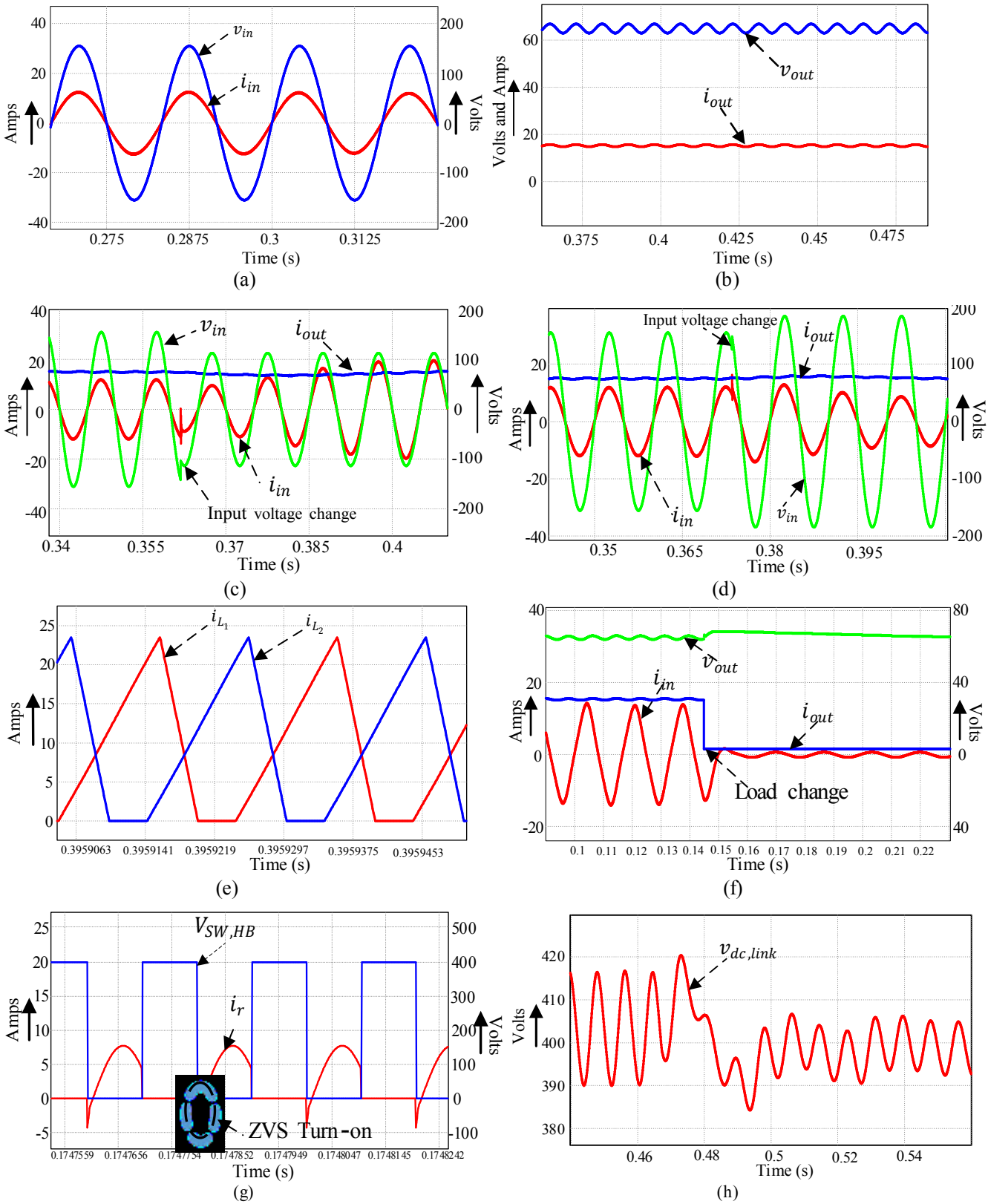


Fig. 3.17 Simulation results (a) input voltage and current. (b) output voltage and current. (c) input voltage change from 110 V to 80 V. (d) input voltage change from 110 V to 130 V. (e) inductor current. (f) load change from 100% to 10% . (g) ZVS turn-on of half-bridge switch. (h) DC-link voltage variation during load change.

Table 3.3: Comparison of analytically calculated and simulated average and rms current values of active and passive devices at rated condition of 1 kW. $V_{in} = 110\ V$, D=0.56, L=75µH

Parameters	Calculated	Simulated
I_{in}	9.16 A	9.11 A
$I_{SW_{BB},rms}$	7.07 A	7.01 A
$I_{L,rms}$	8.14 A	8.12 A
$I_{d,rms}$	4.04 A	4.06 A
$I_{d,avg}$	1.255 A	1.251 A
$I_{C_{dc,link}rms}$	5.13 A	5.19 A
$I_{sw_{HB}rms}$	5.70 A	5.88 A
$I_{SR,rms}$	12.08 A	12.2 A
$I_{C_o,rms}$	8.20 A	8.28 A

point for the battery charger controller (CC mode to CV mode). The output voltage is stable and tracking the reference voltage with a settling time of 10 ms, which confirms the robustness of the voltage controller. Fig. 3.17(g) shows the ZVS turn-on operation of the back-end DC-DC converter. The switch turns on with zero voltage, thus confirming the soft switching of the primary side half-bridge switches. Fig. 3.17 (h) shows dc-link voltage variation during the transient condition. It is observed that dc-link voltage remains relatively the same during load change which verifies the assumption and the gain expression. DC-link tries to reduce for huge load changes as the duty cycle reduces drastically and dc-link capacitor supplies power to the load. To verify the above-derived formulas in the section 3.3 for dc-link selection, the average and RMS currents for an output power of 1.0 kW and input voltage of 110 Vrms are calculated and compared with the simulated values as listed in Table 3.3. The calculated values are very close to the simulated values, thus validating the dc-link voltage selection criteria.

3.5.2 Experimental Results

To validate the loss analysis, and to further verify simulation results, a 1.0 kW proof-of-concept hardware prototype is developed and the details are mentioned in Table 3.3. Fig. 3.18 depicts the hardware prototype developed in the lab where DSP TMS320F28335 is used to program the designed controller, and LEM voltage sensor LV-25P and current sensor LV-55P is used to measure the charging voltage and current. Fig. 3.19 (a) and Fig. 3.19 (b) show the PFC operation at 500 W and 1.0 kW, respectively. The input currents are sinusoidal and are tracking the input voltage both in-phase and shape endorsing the simulation results. Fig. 3.19 (c) shows the voltage

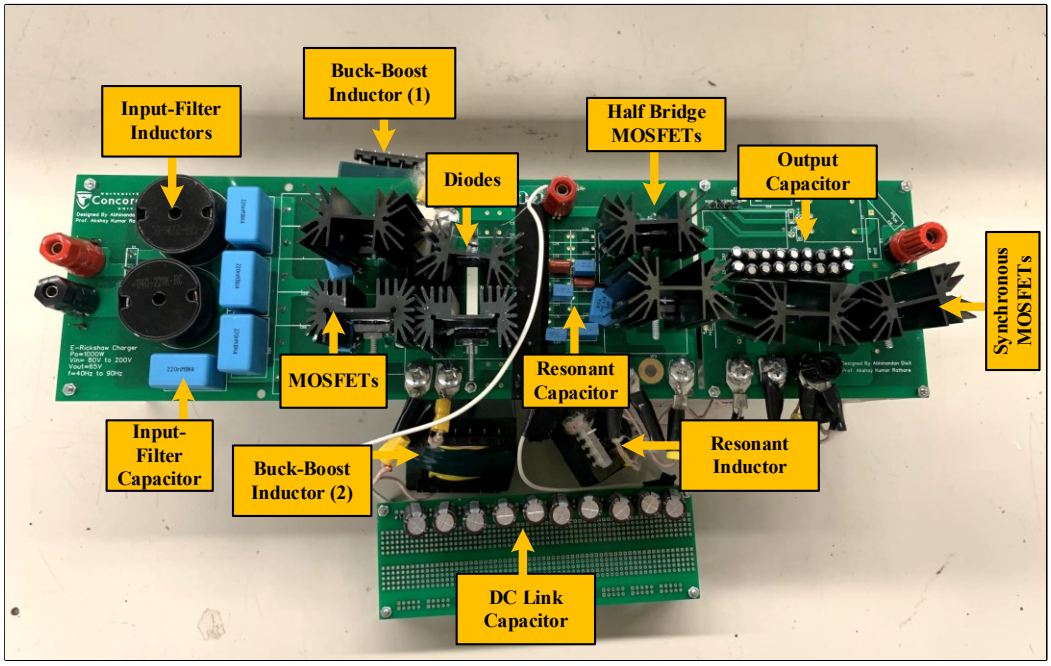


Fig 3.18 Hardware prototype

Table 3.4: Hardware Component specifications

Components	Specification
DCM inductor L_1, L_2	75 µH
Resonant inductor L_r	78 µH
Resonant Capacitor C_{r_1}, C_{r_2}	PHE450XD5100JD15R06L2,10 nF*8
Transformer turns ratio, n	1:0.33:0.33
DC-link Capacitor, $C_{dc,link}$	UCY2W220MHD, 22 µF*12
Output Capacitor, C_o	UVP2A100MPD1TD, 10 µF*18
Input capacitor, C_f	PHE845VY6220MR06L2, 0.22*10 µF
Input inductor, L_f	1140-221K-RC, 220/2µH
Buck-boost MOSFETs, SW_1, SW_2	C3M0075120K, 1200V 30A
Half-bridge MOSFETs, SW_3, SW_4	SCT3080AR, 650 V 30A
SR MOSFETs, SW_5, SW_6	STW75NF20, 200 V 75A
Schottky Diodes, D_1, D_2	RURG80100
Output Inductor L_o	371µH

stress and inductor current profile of the front-end PFC converter. The switch sees maximum voltage stress equal to the dc-link voltage plus the peak input voltage. Fig. 3.19 (d) shows the interleaving and DCM operation of the front end converter. It is observed that the switch turn-on with zero current, thus reducing switching losses. Fig. 3.19(e) shows ZVS turn-on operation of

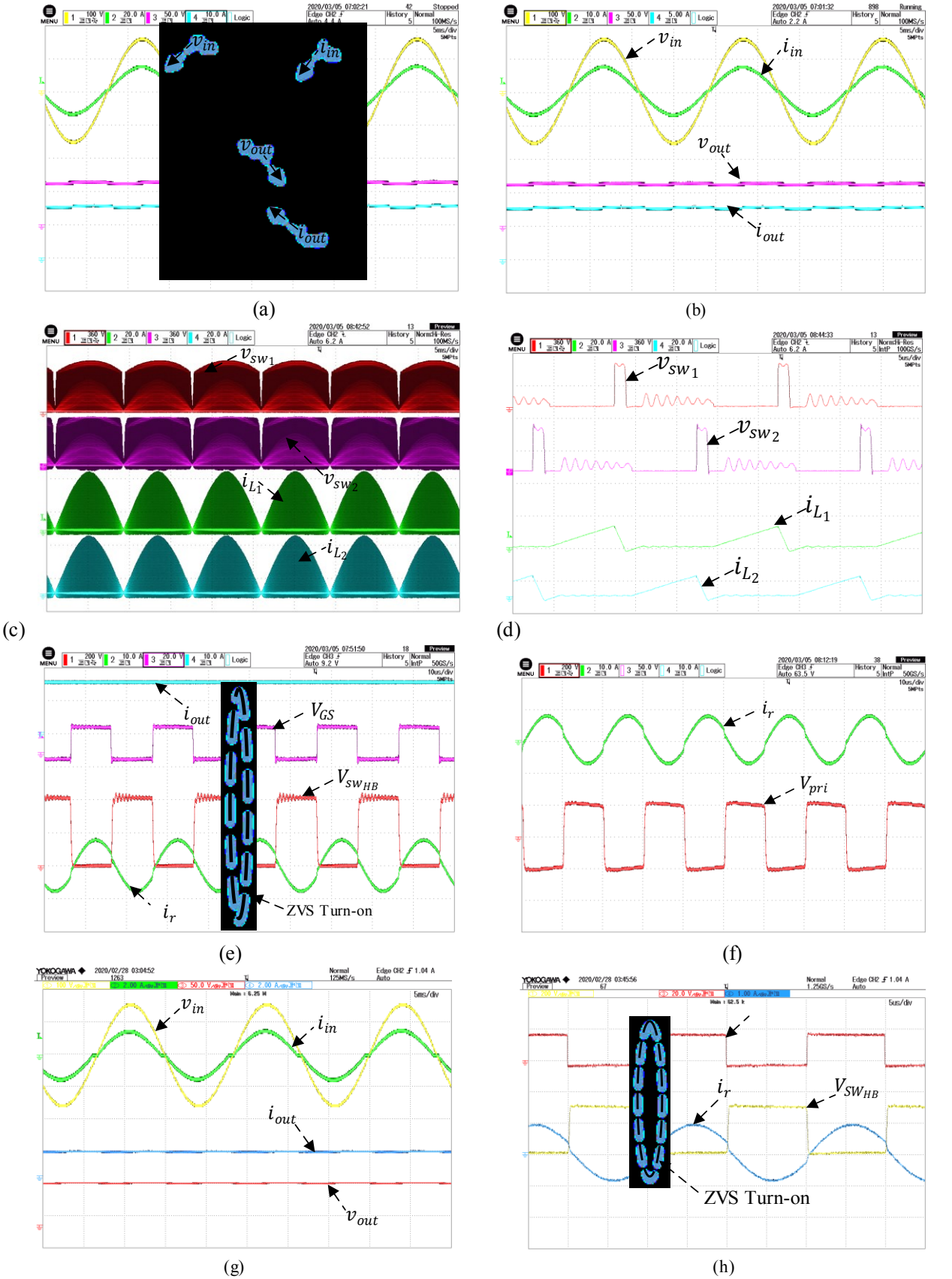


Fig. 3.19 Experimental results (a) input voltage 100 V/div , input current 20 A/div, output voltage 50 V/div and output current 10 A/div. (b) input voltage 100 V/div , input current 10 A/div, output voltage 50 V/div and output current 5 A/div. (c) & (d) switch voltage 360 V/div, inductor current 20 A/div (e) & (f) switch voltage 200 V/div, gate 20 V/div, resonant current 10 A/div (g) input voltage 100 V/div , input current 2 A/div, output voltage 50 V/div and output current 2 A/div. () ZVS turn-on of half-bridge switch. (h) switch voltage 200 V/div, gate 20 V/div, resonant current 1 A/div

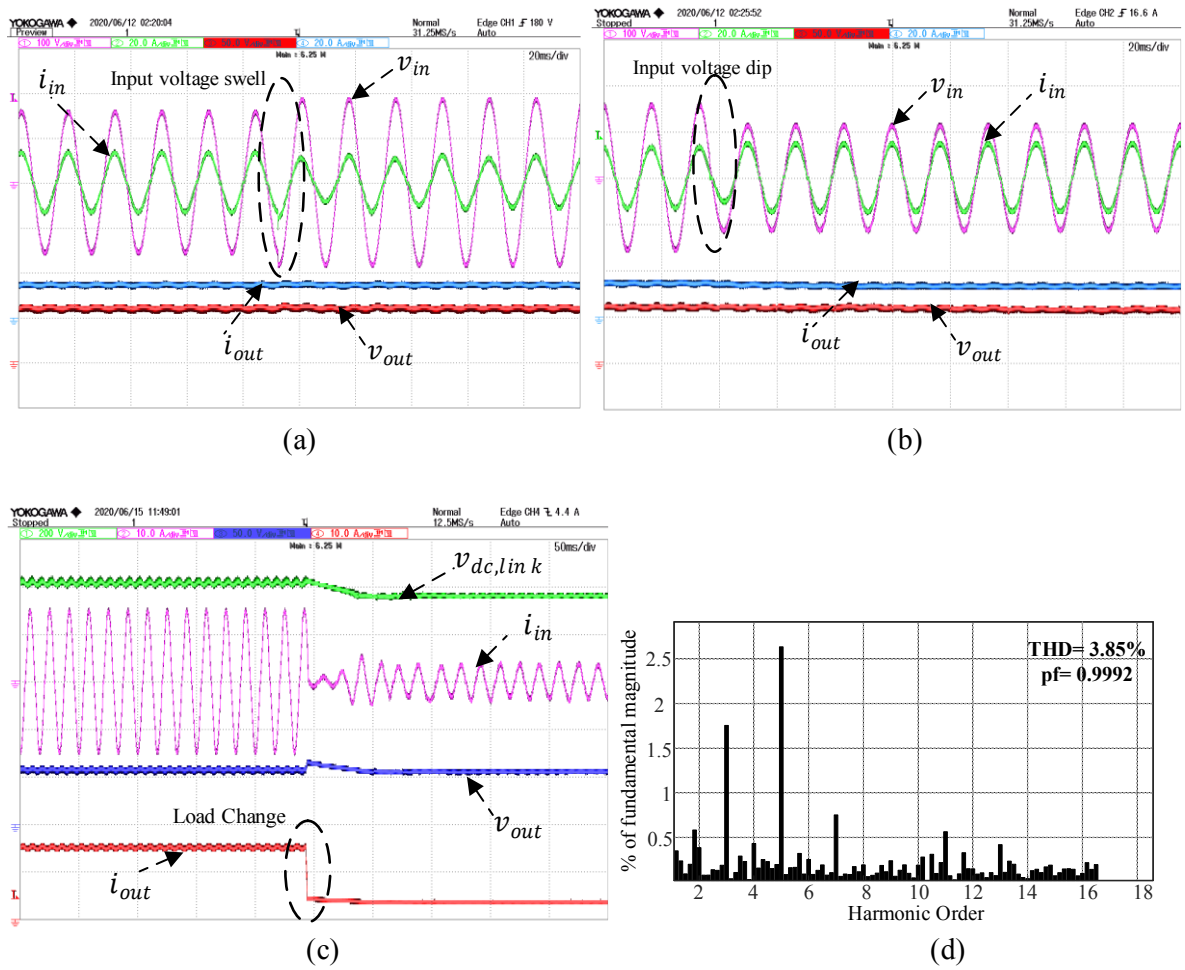


Fig. 3.20 (a) input voltage 100 V/div , input current 20 A/div, output voltage 50 V/div and output current 10 A/div. (b) input voltage 100 V/div , input current 20 A/div, output voltage 50 V/div and output current 10 A/div. input voltage dip (c) dc-link voltage 100 V/div , input current 10 A/div, output voltage 50 V/div and output current 10 A/div. (d) input current FFT at 1.0 kW

half-bridge MOSFETs which confirms the soft-switching of the switches. It is observed that the switch current is negative (body diode conduction) at the moment when the gate pulse is given, which confirms the ZVS operation. Fig. 3.19 (f) shows transformer primary voltage and current which is square and sinusoidal current and voltages are sinusoidal even for light loads thus confirming the CV mode operation respectively. Fig.3.19 (g) shows the CV mode of operation which is at a low load of 100W. Fig. 3.19 (h) show the ZVS operation at low load thus achieving higher efficiency at low loads as well. In order to validate the robustness of the current controller input voltage perturbations are applied. Input voltage swell is applied form 110 V to 130 V as shown in Fig. 3.20 (a). It is seen that input current remains sinusoidal with stiff output current thus validating the robustness of the controller. Similarly effect of input voltage dip is shown in Fig

Table 3.5: Comparison between the proposed topology and other topology for battery charging

Attributes		[27]	[20]	[9]	[5]	[6]	[33]	**Proposed**
No. of Components	DBR	-	-	-	Yes	Yes	Yes	Yes
	HFT	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	S_w	3	3	3	1	6	6	6
	D	5	3	5	1	8	6	2
	L	4	2	4	1	4	2	3
	Int C	2	1	2	1	-	-	-
Mode of Operation		DCM	DCM	DCM	DCM	DCM	CCM	DCM
Switches with SS		3	3	3	1	6	4	6
Diode with Reverse Losses		0	0	0	0	4	6	0
Current Stress		High	Moderately high	Moderately high	High	Moderate	Low	Moderately Low
Voltage Stress		High	High	High	High	Moderate	Moderate	High
Control and Modelling approach		Complex	Complex	Complex	Complex	Very Complex	Very Complex	Very Simple
Efficiency at 100 % load		91%	90.8%	85%	82%	93.7%	95%	96.06%
Efficiency at 10 % load		60%	60%	60%	70%	90%	80%	90.2%
Sensors		3	3	3	2	4	5	2

3.20 (b). Input current increases in order to maintain the same power and remains in-phase with the input voltage. In order to emulate the effect change from CC to CV a load change from 100% load to 20% is applied in order to test the controller robustness as shown in Fig. 3.20 (c). It is observed that output voltage remains stiff at 65 V with and settles in 40ms, thus validating the controller design. Fig. 3.20 (d) shows the input current FFT at 1 kW. It is observed that input current THD is 3.85% with a power factor of 0.9992.

A comparative analysis of the proposed charger is illustrated for better performance over traditional topologies mentioned in Table 3.5 based upon the efficiency, current stress, voltage stress, control complexity, and sensor requirement. It is observed that the converter [5]-[27] which are for low voltage high current charging applications present low efficiency at full load and 10% load by achieving PFC through DCM operation. Even though the modified and the bridgeless topologies of the classical converters are presented, they pose problems such as increase active and passive components' count, high current stress, complex control, and rigorous design

approach. Even single-stage isolated topologies present poor efficiency due to the presence of leakage inductance [5]. Interleaved configuration of the Landsman converter fails to achieve higher efficiency. The second stage in this application involve a flyback converter to control the charging voltage and current. Such a topology is highly inefficient because of losses due to leakage inductance and output diode conduction and turn-on losses. On the other hand, CCM based converters deal with problems such as increase sensor count, complex control and modeling approach, and lower efficiency at low loads. Conventional CCM based converters need a complex modulation scheme and require frequency variation to control the charging voltage and current. DCM based high power boost derived chargers have been proposed in [6] but they deal with complex control owing to rigorous mathematical computation to implement such control. Moreover, CCM converters propose in [33] implement full-bridge as the second stage which effectively doubles the switching and conduction losses. The proposed configuration mitigates the above problems by incorporating interleaved structure at the front end and a half-bridge LLC based converter for the back end. Moreover, the proposed converter has zero sensors for the front-end converter and uses only two sensors to control the charging voltage and current. All these factors

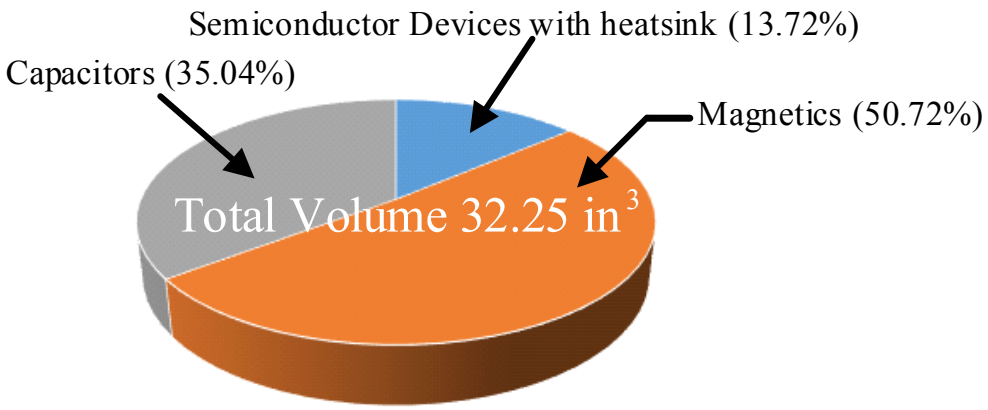


Fig. 3.21 Volumetric distribution

make the converter achieve higher efficiency by a factor of 10% as compared to [9] [20] and nearly 4-5% as compared to [6]. The proposed configuration also achieves higher efficiency by 2-3% than the charging topologies presented by [33] and [6]. It should be noted that the proposed converter configuration can be extended to high voltage charging applications with minor changes in design parameters. As compared to the charger discussed in Chapter 2, the proposed battery charger presents high power density of 32.30 W/in^3 as the thermal requirement are reduced as shown in Fig 3.21.

3.6 Conclusion

In this Chapter a low-cost battery charger topology for battery charging application has been proposed, analyzed, designed, and tested. Interleaved buck-boost converter operating in DCM is used as the first stage in order to achieve PFC and controlling charging voltage and current. In the second stage a half-bridge LLC converter is utilized in order to provide isolation and high-efficiency over wide power variation. The proposed configuration uses only two sensors to control the output voltage and current by directly controlling the front-end switches. The control burden is reduced on the microcontroller by operating the second stage with constant duty and constant frequency. Design equations for the design of DCM inductor and LLC parameters are presented. Loss analysis of the proposed topology has been done using the CSI approach in order to select an optimal value of DC-Link voltage so that minimum losses occur at every stage. The proposed configuration was simulated using PSIM11 and results were presented. A 1.0 kW hardware prototype was developed to validate the analysis and design. The converter achieved UPF along with a THD of less than 5% which is within the limits of IEC61000-3-2 [12] and an efficiency of 96.02%. It presents low input current THD at various power levels and provides relatively high low load efficiency as compared to other topologies. With reduced sensors and high efficiency, the proposed charging topology is another candidate for the battery charging application. Such battery charger can be extended to higher power rating of up to 7kW by integrating more cells and selecting a higher dc-link voltage. The next chapter deals with the conclusion and contribution of the research work and proposes future work that can be done for EV charging applications.

Chapter 4: Conclusion and Future Research

This Chapter presents the contributions of this research and thesis in the Section 4.1 and also highlights the scope of research for the possible extension of this work.

4.1 Contributions of Thesis

In battery charging applications, AC-DC converters play a major role for PFC. This thesis focusses on the development of two simple cost effective battery charger topologies both isolated and non-isolated to replace the traditional battery charging technology which employs diode based rectifiers for charging low voltage battery packs.

This thesis contributes to the analysis and design of single-stage non-isolated and two-stage isolated converters for battery charging application with focus to meet the industry standards of low THD (<5%) and high efficiency. The proposed battery charging technologies are analyzed and designed for DCM operation of AC-DC for simple control and reduced sensor count, which consequently boosts up the converter reliability and robustness, high input power quality, simple charging mechanism and high efficiency are the key highlights of this research.

1. In a first attempt to develop a simple charger, an interleaved buck-boost DCM float charger is analyzed and designed in Chapter 2. Such battery charger is simple to implement and uses a single voltage sensor to control the charging process. A high efficiency of about 94% is achieve. Iinterleaving technique reduces the current stresses on the converter drastically. An input current THD of 4.85 % is recorded which meets the standards as per [12]. A volumetric analysis shows the distribution of the various components and presents a power density of 32 W/in^3. Though such a converter is easy to implement, it utilizes more space due to presence of high value electrolytic capacitors.
2. In order to incorporate isolation and increase converter efficency over a range of power level, a high efficency two-stage battery charger is proposed in Chapter 3. It incorporates an interleaved buck-boost AC-DC converter operated in boost mode(presented in Chapter 2) and followed by a half-bridge soft-switching LLC DC-DC converter with syncronous rectification. Such a configuration improves the efficency of the charger. CC-CV charging is implented in order to control the charging voltage and current by studying the battery

charging profile. Detailed loss analysis is conducted in order to select optimim dc-link voltage to operate the converter with high efficiency. The proposed charging scheme presents a high efficency of 96.06 % at full-load and a peak efficiency of 96.4%. The converter presents a high efficiency of 90.2 % at 100 W an input currenmt THD of 3.85% at full load.

In addition to the above contributions, the following conclusions which are common to all the proposed topologies are summarized as follow:

- The proposed battery charging converter achieves soft-switching of every switch with zero reverse recoverly losses of the diode.
- The charger utilizes a maximim of two sensor offering higher reliability and robustness.
- The steady state operation, analysis and design of the charger configurations are reported in detail along with optimum dc-link voltage selection.
- The small-signal models for both the topologies using CIECA approach are derived, along with closed-loop controller design.
- Output voltage control in Chapter 2 and CC-CV control in Chapter 3 is verified for changes in input voltage and load. Output voltage and current remains stiff and regulated thus validating the design and robustness.
- Detailed simulation results as well as experimental results are provided to validate the analysis, design, and their performance.
- An input current THD less than 5 %, and efficiency greater than 90 % are recorded at rated output power from the proof-of-concept hardware prototypes.
- DCM operation of both charger configurations reduces the control burden as grid synchronization is not required. Moreover, DCM operation is more stable as it does not present any RHZ during transient operation making it robust to high frequency noise.
- As the proposed charger configurations are in DCM, inductor sensitivity analysis is crucial. Due to inductor core heating over time, inductance decreases leading to higher peak currents across the switch. A tolerance of 10% in inductor value the typical allowable limit, provided the MOSFET has higher current rating than critical designed value.

4.2 Comparison Between Proposed Battery Charger Configurations

Table 4.1: Comparison between Proposed Battery Charger Configurations

Attributes		Chapter 2 charger	Chapter 3 Charger	
			Front End	Back End
MOSFET	Voltage stress	Moderate	High	Moderate
	Current stress	Very high	Moderate	Low
	Cost	Very high	Moderate	Low
	Heatsink size	Big	Small	Small
Diodes	Voltage stress	Moderate	High	N.A
	Current Stress	Very High	Moderate	
	Cost	Very High	Moderate	
	Heatsink size	Big	Small	
Inductor size		Small	Moderate	Small
Capacitor	Size	Big	Moderate	Small
	Reliability	Low	Moderately High	Moderately High
Count	Active	4	4	4
	Passive	3	3	4
Isolation		No	Yes	
Gate Driver Requirement		Low	High	
Control		Very Simple	Simple	
Sensor Count		1	2	
Design Flexibility		Less	More	
Charger Type		Float Charger	Two-Stage charger (CC-CV Mode)	
Estimated Charging Time		12hrs approx.	8hrs approx.	
Power Density		30.45 W/in^3	32.30 W/in^3	

Table 4.1 shows a comparison between the charger topologies proposed in Chapter 2 and Chapter 3 in terms of semiconductor stresses, component count and size. The interleaved buck-boost float charger is operated in buck mode in Chapter 2, current stress on semiconductor devices are high leading to increase heat sink requirement and poor low load efficiency. On the other hand, as the front-end buck-boost converter in Chapter 3 is operated in boost mode it has reduced current stresses and reduced thermal requirement leading to improved overall efficiency. Moreover, output capacitor size for the charger proposed in Chapter 2 handles high current ripple due to buck operation at twice line frequency leading increased size and reduced power density. Whereas, the dc-link capacitor and output capacitors in two-stage chargers has reduced size due to reduced current ripple because of boost operation at the front-end and output capacitors observe switching frequency ripple leading reduced size and increased power density. Even though gate driver

requirements are high in the two-stage battery charger due to increased MOSFET count, MOSFET driver integrated chips (IC) such as TI TL145A and TI UCC24624 for back-end converter can be used in order reduce gate driver burden and improve overall efficiency of the converter. Two-stage charger has increased component count as compared to the float charger which reduces overall system reliability of such battery charger configurations. Moreover, magnetic elements in two stage charger utilize a significant amount of area and add to increase weight which can be further optimized by optimal selecting switching frequency for both front-end and back-end converter. Back-end converter can utilize higher switching frequency in order to reduce tank kVA rating whereas front-end converter switching frequency should be selected optimally for reduced switching losses. Higher switching frequency for front-end converter leads to high switching losses due to increased current peaks because of DCM operation. Single stage non-isolated float charger has reduced number components but has less design flexibility. Such float charger also have increased charging time as they lack sophisticated BMS system and utilize single voltage sensor. Two stage charger presents CC-CV mode control which reduces the charging time to approximately 8 hours.

Fig. 4.1 shows cost analysis of a both battery charger configurations presented in Chapter 2 and Chapter 3 scaled to 3.3 kW power rating. It is observed that charger presented in Chapter 2 has higher cost as compared to two-stage charger mainly due to increased semiconductor stresses. Medium voltage high current rating semiconductor devices are costly as compared to high voltage moderate current rating devices as cost of semiconductor devices are a function of its current rating. Thus it can be concluded that for higher power rating such as 3.3kW a two-stage converter becomes a viable option as compared to single-stage non-isolated charger. The charger presented in Chapter 3 can also be extended to even higher power rating of up to 7kW by adding interleaving cells and selecting a higher dc-link voltage. Such an implementation reduced current stress on

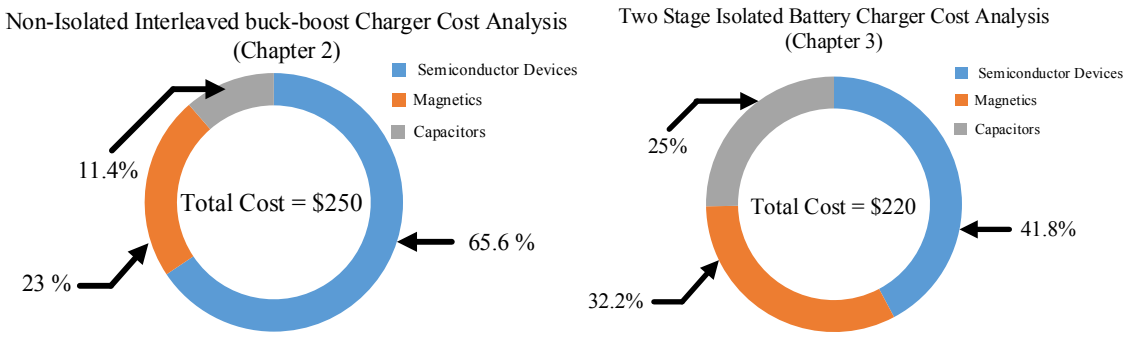


Fig. 4.1 Cost Analysis of proposed charger configurations scaled to 3.3kW

front-end converter significantly and can be a good option. On the other hand, integrating interleaving cells to the float charger in chapter can reduce semiconductor device stresses, but output capacitor size increases significantly leading reduced power density, poor efficiency and increased overall weight. Such float chargers are a good option where engineers require simple design and robust control in order to meet power quality standards where isolation is not a mandatory requirement.

4.3 Future Scope Of Research

Proposed battery charger configurations can be further improved in terms of dynamic performance and it's suceptibility to high frequency noise. The recommendations for future research based on findings from this work are as follows

4.3.1 Design and Development of EMI/EMC Filter

The design and development EMI/EMC filters for the proposed battery charging configuration and imvestigating their high frequency emissions as per CISPR standards [63].

4.3.2 Non-Linear control for better dynamic response

In order to improve and have faster response of the charger, fuzzy-logic based controllers (FLC) can be used which improves converter dynamic response [64] [65]. Such controllers are AI based controllers and work on the model predictive control and presents faster response during transient conditions. A fuzzy control system is a control system based on fuzzy logic—a mathematical system that analyzes analog input values in terms of logical variables that take on continuous values between 0 and 1, in contrast to classical or digital logic, which operates on discrete values of either 1 or 0. It relies on the degrees of state of the input and the output depends on the state of the input and rate of change of this state. Such system is robust for imperfect inputs and presents faster response. Thus replacing conventional PI controllers with non-linear controllers can be one of the future scope of research.

4.3.3 Bridgeless AC-DC converter as active front-end

Proposed battery charger incorporates diode-bridge rectifier based AC-DC converter. Diode bridge incorporates significant amount of losses in the front-end converter, thus reducing charger efficiency and reliability [67]. Diode bridge at the input presents high input current THD as at low line voltages input diode does not turn-on leading to no power transfer during that period. Development of bridgeless topologies is one solution to such problems. Absence of the diode bridge at input substantially reduces the loss and improves input current THD. Moreover, bridgeless topologies allow the flexibility to implement the charger configuration in bi-directional mode. Thus replacement of the front-end conventional diode-bridge based AC-DC converter with bridgeless topologies can be considered as future scope of research.

4.3.4 Current-fed converters as back-end

Commercial battery chargers utilizes voltage-fed dc-dc converter as their second stage for the charge control. Full-bridge LLC converters are popular in battery chargers because of low circulating currents and tendency to achieve better efficiency. Voltage -fed converters incorporate capacitors that have low reliability and thus decreases over system performance in the long run [67] [68]. Moreover for charging battery rated at for higher voltage 420 V to 450 V Li-polymer packs incorporates more number of turns on transformer primary, thus increasing the transformer volume and weight. Incorporating current-fed converters as second stage can mitigate such problems and increase overall converter reliability. Current-fed converters which are boost derived topologies provide high voltage gain thus reducing transformer size and weight. Moreover the inductors have high reliability as compared to the capacitors, which effects the converter performance. Thus study of current-fed converters as a possible second stage for battery charging can be considered as one of the possible scope of research.

Bibliography

[1] Electric vehicle sales in 2020 para 1, line 2 Available [Online]- https://about.bnef.com/blog/electric-vehicle-sales-to-fall-18-in-2020-but-long-term-prospects-remain-undimmed/

[2] "India's Rickshaw Revolution Leaves China in the Dust" [online]. Available: https://www.bloomberg.com/news/features/2018-10-25/india-s-rickshaws-outnumber-china-s-electric-vehicles

[3] "India EV Story Emerging Opportunities by Innovation Norway" [online].Available: https://www.innovasjonnorge.no/contentassets/815ebd0568d4490aa91d0b2d5505abe4/india-ev-story.pdf

[4] C. Oh, D. Kim, D. Woo, W. Sung, Y. Kim and B. Lee, "A High-Efficient Nonisolated Single-Stage On-Board Battery Charger for Electric Vehicles," in IEEE Transactions on Power Electronics, vol. 28, no. 12, pp. 5746-5757, Dec. 2013, doi: 10.1109/TPEL.2013.2252200.

[5] R. Kushwaha and B. Singh, "UPF-isolated zeta converter-based battery charger for electric vehicle," in IET Electrical Systems in Transportation, vol. 9, no. 3, pp. 103-112, 9 2019, doi: 10.1049/iet-est.2018.5010.

[6] J. Lee and H. Chae, "6.6-kW Onboard Charger Design Using DCM PFC Converter With Harmonic Modulation Technique and Two-Stage DC/DC Converter," in IEEE Transactions on Industrial Electronics, vol. 61, no. 3, pp. 1243-1252, March 2014, doi: 10.1109/TIE.2013.2262749.

[7] Axiom Powering Ideas" [online]. Available: http://axiomevproducts.com/pdf/PDF2.pdf

[8] Rapidtron Electronika Private Limited " [online]: Available: "http://rapidtron.co.in/3-wheeler-chargers/

[9] R. Kushwaha and B. Singh, "A Modified Luo Converter-Based Electric Vehicle Battery Charger With Power Quality Improvement," in IEEE Transactions on Transportation Electrification, vol. 5, no. 4, pp. 1087-1096, Dec. 2019, doi: 10.1109/TTE.2019.2952089.

[10] S. Gangavarapu, A. K. Rathore and D. M. Fulwani, "Three-Phase Single-Stage-Isolated Cuk-Based PFC Converter," in IEEE Transactions on Power Electronics, vol. 34, no. 2, pp. 1798-1808, Feb. 2019, doi: 10.1109/TPEL.2018.2829080.

[11] J. Afsharian, D. Xu, T. Zhao, B. Gong and Z. Yang, "Reduced duty-cycle loss and output inductor current ripple in a ZVS switched three-phase isolated PWM rectifier," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 33-37, doi: 10.1109/APEC.2016.7467848.

[12] Limits for Harmonic Current Emissions (Equipment Input Current < 16 A per phase), IEC/EN61000-3-2,1995

[13] R. Kushwaha and B. Singh, "A Bridgeless Isolated Half Bridge Converter Based EV Charger with Power Factor Pre-regulation," 2019 IEEE Transportation Electrification Conference (ITEC-India), Bengaluru, India, 2019, pp. 1-6, doi: 10.1109/ITEC-India48457.2019.ITECINDIA2019-190.

[14] R. Kushwaha and B. Singh, "Bridgeless Isolated Zeta-Luo Converter Based EV Charger with PF Pre-regulation," 2019 International Conference on Computing, Power and Communication Technologies (GUCON), NCR New Delhi, India, 2019, pp. 959-964.

[55] R. Kushwaha and B. Singh, "A Power Quality Improved EV Charger with Bridgeless Cuk Converter," 2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Chennai, India, 2018, pp. 1-6, doi: 10.1109/PEDES.2018.8707701.

[16] R. Kushwaha and B. Singh, "An EV battery charger based on PFC Sheppard Taylor Converter," 2016 National Power Systems Conference (NPSC), Bhubaneswar, 2016, pp. 1-6, doi: 10.1109/NPSC.2016.7858944.

[17] R. Kushwaha and B. Singh, "An Improved Battery Charger for Electric Vehicle with High Power Factor," 2018 IEEE Industry Applications Society Annual Meeting (IAS), Portland, OR, 2018, pp. 1-8, doi: 10.1109/IAS.2018.8544585.

[18] R. Kushwah and B. Singh, "A Modified Bridgeless Cuk Converter based EV Charger with Improved PowerQuality," 2019 IEEE Transportation Electrification Conference and Expo (ITEC), Detroit, MI, USA, 2019, pp. 1-6, doi: 10.1109/ITEC.2019.8790509.

[19] R. Kushwaha and B. Sigh, "A unity power factor converter with isolation for electric vehicle battery charger," 2018 IEEMA Engineer Infinite Conference (eTechNxT), New Delhi, 2018, pp. 1-6, doi: 10.1109/ETECHNXT.2018.8385321.

[20] B. Singh and R. Kushwaha, "A PFC Based EV Battery Charger Using a Bridgeless Isolated SEPIC Converter," in IEEE Transactions on Industry Applications, vol. 56, no. 1, pp. 477-487, Jan.-Feb. 2020, doi: 10.1109/TIA.2019.2951510.

[21] R. Kushwaha and B. Singh, "An Improved PFC Bridgeless SEPIC Converter for Electric Vehicle Charger," 2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020), Cochin, India, 2020, pp. 1-6, doi: 10.1109/PESGRE45664.2020.9070375.

[22] B. Singh and R. Kushwaha, "An EV battery charger with power factor corrected bridgeless zeta converter topology," 2016 7th India International Conference on Power Electronics (IICPE), Patiala, 2016, pp. 1-6, doi: 10.1109/IICPE.2016.8079359.

[23] R. Kushwaha and B. Singh, "An Improved Battery Charger for Electric Vehicle with High Power Factor," 2018 IEEE Industry Applications Society Annual Meeting (IAS), Portland, OR, 2018, pp. 1-8, doi: 10.1109/IAS.2018.8544585.

[24] R. Kushwaha and B. Singh, "An Electric Vehicle Battery Charger with Interleaved PFC Cuk Converter," 2018 8th IEEE India International Conference on Power Electronics (IICPE), JAIPUR, India, 2018, pp. 1-6, doi: 10.1109/IICPE.2018.8709494.

[25] J. Gupta, R. Kushwaha and B. Singh, "Improved Power Quality Charger Based on Bridgeless Canonical Switching Cell Converter for a Light Electric Vehicle," 2020 IEEE 9th Power India International Conference (PIICON), SONEPAT, India, 2020, pp. 1-6, doi: 10.1109/PIICON49524.2020.9112905.

[26] J. Gupta, R. Kushwaha and B. Singh, "Improved Power Quality Charger Based on Bridgeless Canonical Switching Cell Converter for a Light Electric Vehicle," 2020 IEEE 9th Power India International Conference (PIICON), SONEPAT, India, 2020, pp. 1-6, doi: 10.1109/PIICON49524.2020.9112905.

[27] R. Kushwaha and B. Singh, "Power Factor Improvement in Modified Bridgeless Landsman Converter Fed EV Battery Charger," in IEEE Transactions on Vehicular Technology, vol. 68, no. 4, pp. 3325-3336, April 2019, doi: 10.1109/TVT.2019.2897118.

[28] D. Patil and V. Agarwal, "Compact Onboard Single-Phase EV Battery Charger With Novel Low-Frequency Ripple Compensator and Optimum Filter Design," in IEEE Transactions on Vehicular Technology, vol. 65, no. 4, pp. 1948-1956, April 2016, doi: 10.1109/TVT.2015.2424927.

[29] J. Lee, Y. Jeong and B. Han, "An Isolated DC/DC Converter Using High-Frequency Unregulated LLC Resonant Converter for Fuel Cell Applications," in IEEE Transactions on Industrial Electronics, vol. 58, no. 7, pp. 2926-2934, July 2011, doi: 10.1109/TIE.2010.2076311.

[30] K. Yoo, K. Kim and J. Lee, "Single- and Three-Phase PHEV Onboard Battery Charger Using Small Link Capacitor," in IEEE Transactions on Industrial Electronics, vol. 60, no. 8, pp. 3136-3144, Aug. 2013, doi: 10.1109/TIE.2012.2202361.

[31] H. J. Chae, W. Y. Kim, S. Y. Yun, Y. S. Jeong, J. Y. Lee and H. T. Moon, "3.3kW on board charger for electric vehicle," 8th International Conference on Power Electronics - ECCE Asia, Jeju, 2011, pp. 2717-2719, doi: 10.1109/ICPE.2011.5944762.

[32] D. S. Gautam, F. Musavi, M. Edington, W. Eberle and W. G. Dunford, "An Automotive Onboard 3.3-kW Battery Charger for PHEV Application," in IEEE Transactions on Vehicular Technology, vol. 61, no. 8, pp. 3466-3474, Oct. 2012, doi: 10.1109/TVT.2012.2210259.

[33] H. Wang, S. Dusmez and A. Khaligh, "Design and Analysis of a Full-Bridge LLC-Based PEV Charger Optimized for Wide Battery Voltage Range," in IEEE Transactions on Vehicular Technology, vol. 63, no. 4, pp. 1603-1613, May 2014, doi: 10.1109/TVT.2013.2288772.

[34] H. V. Nguyen and D. Lee, "Advanced Single-Phase Onboard Chargers with Small DC-Link Capacitors," 2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC), Shenzhen, 2018, pp. 1-6, doi: 10.1109/PEAC.2018.8590400.

[35] F. Musavi, M. Craciun, D. S. Gautam, W. Eberle and W. G. Dunford, "An LLC Resonant DC–DC Converter for Wide Output Voltage Range Battery Charging Applications," in IEEE Transactions on Power Electronics, vol. 28, no. 12, pp. 5437-5445, Dec. 2013, doi: 10.1109/TPEL.2013.2241792.

[36] F. Musavi, W. Eberle and W. G. Dunford, "A High-Performance Single-Phase Bridgeless Interleaved PFC Converter for Plug-in Hybrid Electric Vehicle Battery Chargers," in IEEE Transactions on Industry Applications, vol. 47, no. 4, pp. 1833-1843, July-Aug. 2011, doi: 10.1109/TIA.2011.2156753.

[37] S. Jeong, Y. Jeong, J. Kwon and B. Kwon, "A Soft-Switching Single-Stage Converter With High Efficiency for a 3.3-kW On-Board Charger," in IEEE Transactions on Industrial Electronics, vol. 66, no. 9, pp. 6959-6967, Sept. 2019, doi: 10.1109/TIE.2018.2877093.

[38] A. Gupta, A. Panwar, S. K. Sahoo and I. Jacob Raglend, "A CCM/DCM Hybrid Control Scheme for Single Channel Boost PFC Converter to Improve Power Quality," 2019 Innovations in Power and Advanced Computing Technologies (i-PACT), Vellore, India, 2019, pp. 1-5, doi: 10.1109/i-PACT44901.2019.8960037.

[39] S. F. Lim and A. M. Khambadkone, "A Simple Digital DCM Control Scheme for Boost PFC Operating in Both CCM and DCM," in IEEE Transactions on Industry Applications, vol. 47, no. 4, pp. 1802-1812, July-Aug. 2011, doi: 10.1109/TIA.2011.2153815.

[40] H. Luo, J. Xu, Y. Luo and J. Sha, "A Digital Pulse Train Controlled High Power Factor DCM Boost PFC Converter Over a Universal Input Voltage Range," in IEEE Transactions on Industrial Electronics, vol. 66, no. 4, pp. 2814-2824, April 2019, doi: 10.1109/TIE.2018.2842776.

[41] C. W. Clark, F. Musavi and W. Eberle, "Digital DCM Detection and Mixed Conduction Mode Control for Boost PFC Converters," in IEEE Transactions on Power Electronics, vol. 29, no. 1, pp. 347-355, Jan. 2014, doi: 10.1109/TPEL.2013.2252471.

[42] K. Yao, W. Hu, Q. Li and J. Lyu, "A Novel Control Scheme of DCM Boost PFC Converter," in IEEE Transactions on Power Electronics, vol. 30, no. 10, pp. 5605-5615, Oct. 2015, doi: 10.1109/TPEL.2014.2372152

[43] Y. Chen and Y. Chen, "Line Current Distortion Compensation for DCM/CRM Boost PFC Converters," in IEEE Transactions on Power Electronics, vol. 31, no. 3, pp. 2026-2038, March 2016, doi: 10.1109/TPEL.2015.2434885.

[44] Gandhi B and M. Ezhilmaran, "Achieving high input power factor for DCM boost PFC converters by controlling variable duty cycle," 2013 International Conference on Computation of Power, Energy, Information and Communication (ICCPEIC), Chennai, 2013, pp. 18-20, doi: 10.1109/ICCPEIC.2013.6778514.

[45]] K. Yao, L. Li, H. Tang, C. Mao and K. Chen, "Optimum Boundary Inductance Control Concerning Limited PF for a DCM Boost PFC Converter," in IEEE Transactions on Power Electronics, vol. 35, no. 1, pp. 443-454, Jan. 2020, doi: 10.1109/TPEL.2019.2912324.

[46] L. Huber, B. T. Irving and M. M. Jovanovic, "Open-Loop Control Methods for Interleaved DCM/CCM Boundary Boost PFC Converters," in IEEE Transactions on Power Electronics, vol. 23, no. 4, pp. 1649-1657, July 2008, doi: 10.1109/TPEL.2008.924611.

[47] K. De Gusseme, D. M. Van de Sype, A. P. M. Van den Bossche and J. A. Melkebeek, "Input-Current Distortion of CCM Boost PFC Converters Operated in DCM," in IEEE Transactions on Industrial Electronics, vol. 54, no. 2, pp. 858-865, April 2007, doi: 10.1109/TIE.2007.892252.

[48] L. Huber, B. T. Irving and M. M. Jovanovic, "Effect of Valley Switching and Switching-Frequency Limitation on Line-Current Distortions of DCM/CCM Boundary Boost PFC Converters," in IEEE Transactions on Power Electronics, vol. 24, no. 2, pp. 339-347, Feb. 2009, doi: 10.1109/TPEL.2008.2006053.

[49] R.W Erickson and D. Maksimovic, " Fundamentals of Power Electronics (2nd ed)," Springer Science+Buisness Media, LLC,2001

[50] D. S. L. Simonetti, J. Sebastian, F. S. dos Reis and J. Uceda, "Design criteria for SEPIC and Cuk converters as power factor preregulators in discontinuous conduction mode," Proceedings of the 1992 International Conference on Industrial Electronics, Control, Instrumentation, and Automation, San Diego, CA, USA, 1992, pp. 283-288 vol.1, doi: 10.1109/IECON.1992.254619.

[51] P. R. K. Chetty, "Current Injected Equivalent Circuit Approach to Modeling and Analysis of Current Programmed Switching DC-DC Converters (Discontinuous Inductor Conduction Mode)," in IEEE Transactions on Industry Applications, vol. IA-18, no. 3, pp. 295-299, May 1982, doi: 10.1109/TIA.1982.4504077.

[52] P. R. K. Chetty, "Current Injected Equivalent Circuit Approach to Modeling of Switching DC-DC Converters in Discontinuous Inductor Conduction Mode," in IEEE Transactions on Industrial Electronics, vol. IE-29, no. 3, pp. 230-234, Aug. 1982, doi: 10.1109/TIE.1982.356670.

[53] P. R. K. Chetty, "Current Injected Equivalent Circuit Approach to Modeling Switching DC-DC Converters," in IEEE Transactions on Aerospace and Electronic Systems, vol. AES-17, no. 6, pp. 802-808, Nov. 1981, doi: 10.1109/TAES.1981.309131.

[54] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," in IEEE Transactions on Power Electronics, vol. 3, no. 2, pp. 174-182, April 1988, doi: 10.1109/63.4347.

[55] B. Wang, R. Chen and D. Jauregui, "Common source inductance (CSI) of power devices and the impacts on synchronous buck converters," 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, Fort Worth, TX, 2014, pp. 157-162, doi: 10.1109/APEC.2014.6803303.

[56] Estimating MOSFET Parameters From the Datasheet, Texas Instrument Seminar Topics Slup170, 2002. [Online]. Available: http://focus.ti.com/ lit/ml/slup170/slup170.pdf

[57] “Inductor and Flyback Transformer Design” [Online] Available: https://www.ti.com/lit/ml/slup127/slup127.pdf.

[58] “Diode conduction losses” [Online] Available: https://www.st.com/resource/en/application_note/cd00003894-calculation-of-conduction losses-in-a-power-rectifier-stmicroelectronics.pdf

[59] “E-Rickshaw Tubular Battery”, [Online] Available: https://5.imimg.com/data5/IM/UU/MY-2905462/eastman-em100er-110-ah-e-rickshaw-tubular-battery.pdf

[60] Q. Chen, J. Jiang, H. Ruan and C. Zhang, "Simply designed and universal sliding mode observer for the SOC estimation of lithium-ion batteries," in IET Power Electronics, vol. 10, no. 6, pp. 697-705, 19 5 2017, doi: 10.1049/iet-pel.2016.0095.

[61] "Temperature, Overcharge and Short-Circuit Studies of Batteries used in Electric Vehicles" . doi:10.15199/48.2017.05.13 http://pe.org.pl/articles/2017/5/13.pdf

[62] "Charging Valve Regulated Lead Acid Batteries". [Onilne] Available: https://www.cdtechno.com/pdf/ref/41_2128_0212.pdf

[63] CISPR 14-1, Electromagnetic compatibility - Requirements for household appliances, electric tools and similar apparatus - Part 1: Emission.

[64] R. S. Rebeiro and M. N. Uddin, "Performance Analysis of an FLC-Based Online Adaptation of Both Hysteresis and PI Controllers for IPMSM Drive," in IEEE Transactions on Industry Applications, vol. 48, no. 1, pp. 12-19, Jan.-Feb. 2012, doi: 10.1109/TIA.2011.2175876.

[65] P. K. Khanke and S. D. Jain, "Comparative analysis of speed control of BLDC motor using PI, simple FLC and Fuzzy - PI controller," 2015 International Conference on Energy Systems and Applications, Pune, 2015, pp. 296-301, doi: 10.1109/ICESA.2015.7503359

[66] A. Dixit, K. Pande, S. Gangavarapu and A. K. Rathore, "DCM Based Bridgeless PFC Converter for EV Charging Application," in IEEE Journal of Emerging and Selected Topics in Industrial Electronics, doi: 10.1109/JESTIE.2020.2999595.

[67] Pan Xuewei and A. K. Rathore, "Comparison of bi-directional voltage-fed and current-fed dual active bridge isolated dc/dc converters low voltage high current applications," 2014 IEEE 23rd International Symposium on Industrial Electronics (ISIE), Istanbul, 2014, pp. 2566-2571, doi: 10.1109/ISIE.2014.6865024.

[68] P. Xuewei and A. K. Rathore, "Small-Signal Analysis of Naturally Commutated Current-Fed Dual Active Bridge Converter and Control Implementation Using Cypress PSoC," in IEEE Transactions on Vehicular Technology, vol. 64, no. 11, pp. 4996-5005, Nov. 2015, doi: 10.1109/TVT.2014.2375828.

List of Publications

Journal Paper

1) **A. Dixit**, K. Pande, S. Gangavarapu and A. K. Rathore, "DCM Based Bridgeless PFC Converter for EV Charging Application," in IEEE Journal of Emerging and Selected Topics in Industrial Electronics, doi: 10.1109/JESTIE.2020.2999595.

Conference Paper

1) **A. Dixit**, K. Pande, A. K. Rathore, R. K. Singh and S. K. Mishra, "Design & Development of On-Board DC Fast Chargers for E-Rickshaw," 2019 IEEE Transportation Electrification Conference (ITEC-India), Bengaluru, India, 2019, pp. 1-6, doi: 10.1109/ITEC-India48457.2019.ITECINDIA2019-40.
2) **A.Dixit**, A K Rathore "High-Efficient G2V Battery Charger Charger for 48 V Local e-transportation" 2020 IEEE Industry Applications Society Annual Meeting, Detroit, Michigan, USA **[Accepted]**.
3) K. Pande, **A. Dixit,** A. K. Rathore, R. K. Singh, S. K. Mishra and J. Rodriguez , "Design & Development of Bridgeless Buck-Boost Derived PFC Converter for On-Board EV Charging Application" 2020 IEEE Energy Conversion Congress and Exposition (ECCE- Detroit, Michigan, USA) **[Accepted]**.
4) K. Pande, **A. Dixit**, S. Gangavarapu and A. K. Rathore, "Two-Stage On-Board Charger using Bridgeless PFC and Half-Bridge LLC Resonant Converter with Synchronous Rectification for 48V e-Mobility" 2020 IEEE Industry Applications Society Annual Meeting, Detroit, Michigan, USA **[Accepted]**.