An Investigation of Series and Parallel Configurations for Hybrid Power Amplifiers

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ABSTRACT

An Investigation of Series and Parallel Configurations for Hybrid Power Amplifiers

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Power Hardware-in-the-Loop (PHIL) is becoming increasingly popular for compartmentalized testing of electric power equipment in several areas such as in electric drive systems and distributed power generation systems. The fundamental idea of PHIL is to create flexible conditions for Devices under Test (DUT) to be properly assessed in real time and dynamic conditions with their rated power levels. Connected to the DUT is the Power Amplifier (PA), which is responsible for increasing the voltage and current levels, given from the Real-Time Simulator (RTS). The DUT is a physical equipment and high-complexity models are used to control the PAs to emulate necessary conditions for the DUT to be evaluated. One of the main benefits of PHIL is that it can provide a platform for conducting a number of severe tests without risking damaging the equipment that is being emulated, while testing the actual response of the DUT. It can also help with the preliminary design and performance assessment of new types of machines, drivers and controllers, thus significantly reducing the time to market of new equipment. The flexibility of PHIL is also one of its main assets, since the combination of the RTS and the PA can be used for various applications only by changing the model and/or parameters of the emulated element.

This thesis will evaluate the main architectures, control strategies and PHIL applications of PAs. Linear Power Amplifiers (LPA) provide an overall great performance due to its high bandwidth but are expensive, mostly at increased power ratings. For high PAs with fast dynamic response and reduced waveform distortion, the Hybrid Power Amplifier (HPA) configuration provides a good cost-performance compromise. HPAs are built essentially with the association of a low-cost Switch Mode Power Amplifier (SMPA) and an LPA.

The first configuration to be investigated is the series connected HPA intended for high voltage systems. The SMPA consists of a Cascaded H-Bridge Multilevel (CHBM) converter for increased modularity. A single-pulse per H-bridge modulation technique called Nearest Level of

Control (NLC) is used for minimizing the switching losses. However, this leads to unbalanced power consumption by the H-bridges when the SMPA provides relatively low output voltages, thus compromising the reliability and power quality of the SMPA. A new modulation technique called Split-Voltage Fist-In First-Out (SV-FIFO) that mitigates this issue is proposed. Its implementation requires the use of a supplemental, but simple, control loop based on the magnitude and frequency of the reference output voltage. Experimental results are presented to validate the design approach and demonstrate the high performance achieved with SV-FIFO.

The parallel connected HPA is also evaluated in this thesis. In a similar way to the series connected HPA, the LPA provides high bandwidth (BW) and active power filtering while the bulk of the power is provided by the SMPA. The SMPA is realized with a three-phase Voltage Source Converter (VSC) and three single-phase LPAs. The contribution relies on proposing a new topology and current control strategy that aims to reduce the size of the required LPA, which is costly. This is achieved by using the reference current of the HPA for the current control loop of the LPA, and the actual HPA current as the reference for the SMPA current loop. By making the bandwidth of the current loop of the LPA higher than that the SMPA one, the first provides the fast transient components and harmonic filtering while the second, the bulk of the HPA current.

Additionally, this thesis also covers the evaluation of techniques for Amplitude, Phase Angle and Frequency (APAF) detection for single-phase systems. Amplitude, phase and frequency detection is a key feature for the control of the series HPA, but it is also useful for other important applications, such as the synchronization of renewable sources to Alternate Current (AC) grids, which is a largely growing practice. APAF for single-phase systems are more challenging since they require additional and more complex techniques to determine the phase angle. Usually, both single and three-phase systems are designed for a single and known frequency, usually the grid's frequency. However, a wider range of frequencies is necessary for other applications such as HPAs. This thesis will examine two proposed techniques for APAF. The first is based on the combination of the integral and derivative actions and the second is based on the modification of a zero-crossing detection system. Both systems are discussed in detail and validated experimentally.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

NOMENCLATURE

4Q	Four Quadrant
AANF	Amplitude Adaptive Notch Filter
AC	Alternating Current
ACPS	Alternating Current Power Supplies
AFEC	Active Front End Converter
ANF	Adaptive Notch Filter
AOI	Area of Interest
APAF	Amplitude, Phase Angle and Frequency
APF	Active Power Filter
AP-MCA	Amplitude-Modulated and PWM Multicell Amplifier
BJT	Bipolar Junction Transistor
BW	Bandwidth
CBPWM	Carrier-Based PWM
CHBM	Cascade H-Bridge Multilevel
CP	Coupling Point
CPU	Central Processing Unit
DB	Derivative Base
DOL	Direct On-Line
DSP	Digital Signal Processor
DUT	Device Under Test
EMI	Electromagnetic Interference
EPLL	Enhanced-PLL
FACTS	Flexible AC Transmission System
FEA	Finite Element Analysis
FIFO	First-In First-Out
FILO	First-In Last-Out
FPGA	Field-Programmable Gate Array
GUI	Graphic User Interface
HD	Harmonic Distortion

HF	High Frequency
HPA	Hybrid Power Amplifier
IB	Integral Based
ILB	Independent Load Balancing
IM	Induction Machine
IUT	Inverter Under Test
KFB	Kalman Filter Based
LIM	Limiters
LPA	Linear Power Amplifier
LPF	Low Pass Filter
LS-PWM	Level-Shifted PWM
MCCPA	Multicell Cascade Power Amplifier
ME	Machine Emulation
MMC	Modular Multilevel Converter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NLC	Nearest Level of Control
NLM	Nearest Level Modulation
NPDC	Neutral-Point Diode-Clamped
OSG	Orthogonal Signal Generator
PA	Power Amplifier
PCB	Printed Circuit Board
PD	Passive Damping
PHIL	Power Hardware-in-the-Loop
PLL	Phase-Locked Loop
P-MCA	PWM MCA
PMSM	Permanent Magnet Synchronous Machine
PR	Proportional-Resonant
PS-PWM	Phase-Shifted PWM
PV	Photovoltaic
PWM	Pulse-Width Modulation
RF	Radio Frequency

RTS	Real-Time Simulator
SDEV	Standard Deviation
SHE	Selective Harmonic Elimination
SM	Safety Margin
SMPA	Switch Mode Power Amplifier
SOGI	Second Order Generalized Integrated
SPWM	Sinusoidal Pulse-Width Modulation
SRF-PLL	Synchronous Reference Frame
SV-FIFO	Split-voltage First-in First-out
TD-PLL	Transfer Delay-Based PLL
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supplies
VFD	Variable Flux Drive
VFM	Variable Flux Machine
VSC	Voltage Source Converter

1. INTRODUCTION

A power amplifier is a device that provides gain to a voltage or current signal, increasing significantly its power level. It is largely used in interfaces between a signal component (i.e. a digital controller) and an electrical load that is to be supplied with a large power signal. Early days topologies of power amplifiers used vacuum tubes and triodes until the invention of the transistors and all the power electronics based amplifiers [1], [2]. These power electronics amplifiers can work with semiconductor devices operating in the linear or dissipative region. As an example for this application, one can mention the Bipolar Junction Transistors (BJTs) and Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs). The system implementing them are called Linear Power Amplifiers (LPA) and they have the best performance tracking references (high fidelity) because of their very high bandwidth (BW) [3], [4]. In addition, since the semiconductors operate as variable resistors not producing any switching harmonic components, they have higher quality on the output signal. As disadvantages of the LPA, it is possible to highlight their low efficiency, which require large heatsinks and cooling leading to larger volumes and weights [5]. This fact, together with the high price of high bandwidth (quality or accuracy) power components (MOSFETs and BJTs) significantly increase the price of this solution. Also power components when used in the linear region will be more expensive when compared to discrete or switched components for the same rated current, because they need to support a higher dissipated power, which is proportional to the varying voltage drop across its terminals when there is current flowing [1].

An alternative option is to use semiconductors as switches in Switched-Mode Power Amplifiers (SMPA) [6]. Their principle of operation relies on the fast switch of semiconductors, once again, the MOSFET can be used as an example, but only the switched, or on-state and off-state regions are used. The losses related to the linear region are minimal, only happening at short periods during the rise and fall times of the voltage across the switches terminals. This significantly increases the efficiency of the overall system, since the losses at the switches are now limited to the switching and small conductive losses. In addition, the fast switching enables the harmonic filters to be smaller, which leads to higher power densities. The choice of the switching frequency needs to balance the size of the filter (related to the order of the switching harmonics), the limitations of the components and the switching losses, which are proportional to the frequency. Since todays' switches are very efficient with very small on-state resistance and small input and

output capacitances, the losses with SMPAs in general are significantly lesser than with the LPA. As a disadvantage, the required output filter, usually a second or third order one, decreases the dynamic response and limits the bandwidth of the system.

In order to benefit from the advantages of both SMPA and LPA, their series, parallel or combinations of both connections are used to build a Hybrid Power Amplifier (HPA). In the HPA, the SMPA will provide the larger portion of power (either voltage or current) and the LPA will contribute with the increased bandwidth, thus assisting with fast, precise and high quality outputs. Each system must be designed to make up for each other's main limitations. This chapter will evaluate existing topologies, switching schemes and control logics related to HPAs.

1.1. Power Hardware-in-the-Loop and Power Amplifiers

Power amplifiers are an essential equipment for Power-Hardware-In-the-Loop (PHIL) simulations. They are required in the emulation of rotating machines, loads and even power grids to create all sorts of testing conditions. It is a common equipment used in the automotive, aerospace and drive/relay industries [7], [8]. PHIL is increasingly becoming popular for compartmentalized testing of electric power equipment in several areas such as in electric drive systems, distributed power generation systems, etc. [8]–[10]. Machine Emulation (ME), is one such application area of PHIL simulations, and is becoming an essential tool for the fast development of high performance motor drives in industry, robotics and electric mobility [9], [11], [12]. It can provide a platform for conducting a number of severe tests without risking damage to the machine or even to test machine performance before it is actually built [13]–[15].

PHIL can help with the preliminary design and performance assessment of new types of machines such as synchronous reluctance [16]–[18] and variable flux synchronous machines [19], [20]. While ME systems are not expected to replace the conventional dynamometer-based tests, their programmable nature offers a high degree of flexibility for testing various types/parameters of machine designs and drives [21]–[23].

1.2. Configurations of Hybrid Power Amplifiers

A Hybrid Power Amplifier (HPA) aims to combine the best of both LPA and SMPA [24]. In series and parallel configuration, the SMPA is responsible for processing the largest portion of power, and it can do it with an elevated power density and efficiency. The LPA is responsible only

for the difference between the reference and the output of the SMPA, operating as a correction amplifier. This operation is very similar to the operation of an active filter. The main drawback of LPAs in any of the configurations is the cost. A four quadrant (4Q) LPA capable of outputting positive and negative voltages with an 1.2 kVA sinking power costs around $8,333/kW (AE Techron 7548) [25], while switched 4Q solutions can cost as low as $350/kW (440 V/ 30 A Semikron SemiTEACH) [26].

1.2.1. Envelope Tracking HPA

One example of an HPA with envelope configuration is presented in Figure 1.1. In the envelope configuration, the SMPA regulates the input/supply voltages of the LPA, to reduce the voltage drops on the LPA, thus minimizing its power losses. In this example, two half-bridges are used as SMPA to create the positive and negative voltages for the LPA, but any other converter can be used, as long as it is able to regulate its output voltage fast enough as required on the input side of the LPA. Since the LPA has to process all the load power, this configuration is common in low power applications, such as Radio Frequency (RF) and telecommunications, with PAs operating in the MHz and GHz ranges [3], [27], [28].

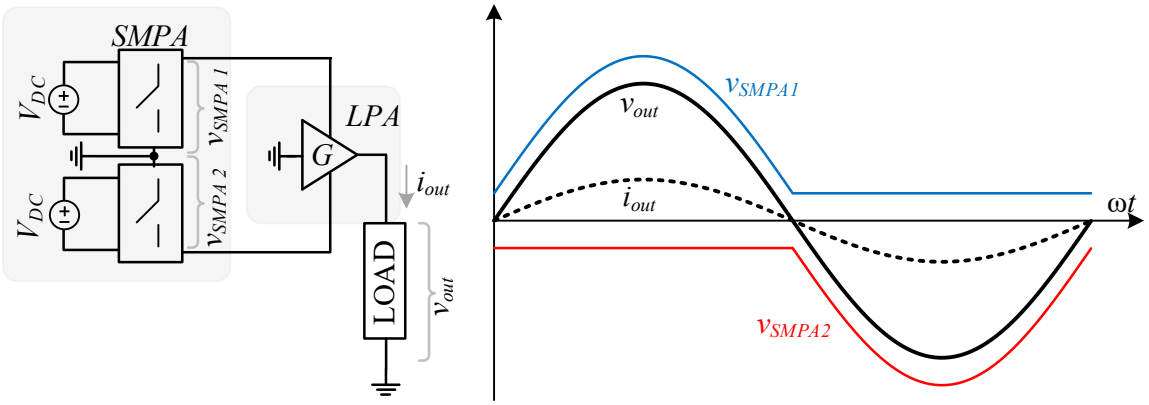


Figure 1.1 – HPA envelope configuration [3], [27], [28]

1.2.2. Series Connected HPA

The series configuration, as shown in Figure 1.2, is indicated for high voltage applications with a low voltage LPA. The SMPA, through v_{SMPA}, provides the bulk of the output voltage (v_{OUT}) and the LPA, via v_{LPA}, the corrections to realize the target voltage waveform. In the example shown in Figure 1.2, v_{SMPA} is of the staircase type, a typical output voltage waveform of multilevel converters when used for sinusoidal outputs or applications (such as v_{OUT}). Each time the reference

voltage is higher than a certain level, another cell is turned on or off. Considering that the SMPA is fast enough, the v_{LPA} will be mostly the mathematical difference between the reference voltage and the v_{SMPA}. The disadvantage is that the LPA has to withstand the full output/load current. Recall that the cost of LPAs tend to increase with the increase in the rated current and the sinking capability is typically lower than the sourcing [25]. The series configuration has been employed for high power voltage amplifiers [6], [24], [29] and for AC Power Supplies (ACPS) [30], [31].

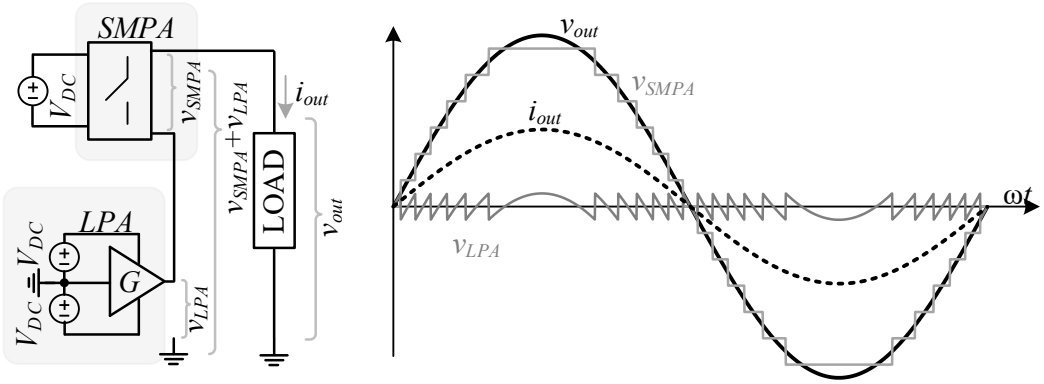


Figure 1.2 – HPA series connected [6], [24], [29]–[31]

In [4] a series configuration is proposed by using a single half-bridge converter as SMPA, which is operated at 180 kHz. Operating a SMPA in high switching frequency demands the utilization of low-pass filters to mitigate the switching harmonics, such as the LCL filter with a 30 kHz cutoff frequency used in [4], causing limitation of the maximum achievable bandwidth.

In order to reduce the switching losses, remove the output filter and the limitation on the bandwidth caused by low pass filters, several topologies implement cascaded or multilevel converters with low frequency modulation. One benefit across all configurations is the modularity and flexibility, at the cost of a higher number of components and consequently a more complex control strategy. The low frequency modulation in combination with the multilevel construction will generate a staircase voltage waveform in which the steps (transitions between cells turning on and off) will be compensated by the LPA [29]–[32].

The minimum frequency of commutations, and consequently the smaller switching losses, can be achieved by using a staircase modulation with the Nearest Level of Control (NLC) modulation [33]. With this modulation, the output filter volume, weight, and cost are reduced because low-order harmonics are eliminated [34]. One of the constraints of the staircase modulation under dynamic modulation indexes and output frequencies is the need for numerical

algorithms, equations solvers, so real time processors are required for the implementation of it [34]. The NLC is an open-loop control strategy used in the SMPA. For the LPA, some studies rely on open or closed loop strategies, such as feed-forward compensation [4] and phase lead and lag compensation [31], [35].

1.2.3. Parallel Connected HPA

In the parallel configuration, the load current (i_{out}) is shared by the LPA (i_{LPA}) and SMPA (i_{SMPA}). In Figure 1.3, a parallel HPA is represented, connecting the LPA and the SMPA to the load at a coupling or common point, CP. Although the load voltage, v_{out}, is controlled, in this configuration both systems must have current outputs, which means that the SMPA, when built using voltage converters, must include a coupling inductor. To synthesize the load or output current i_{out} (dashed line in Figure 1.3), the SMPA (light grey) once again will contribute with most of the power and in this case, current. The LPA will once again be controlled to compensate for the error, or difference, but this time, between the currents. As the dual of the series configuration, in parallel HPAs, the LPA and SMPA are subject to the same output/load voltage [6]. The parallel configuration has been used to drive high-end audio amplifiers [36], ACPS [6] and low-power RF applications [37].

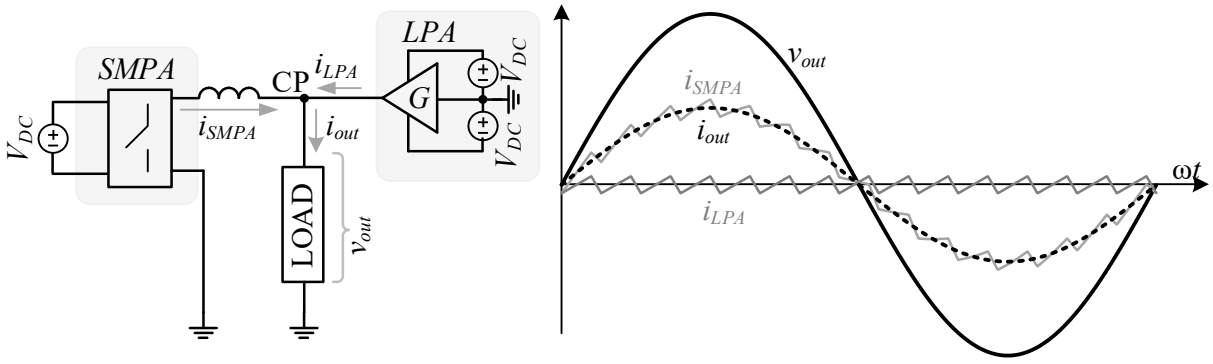


Figure 1.3 – HPA parallel configuration [6], [36], [37].

Several topologies can be used on the SMPA side, including single or interleaved half-bridges [6], single or interleaved full or H-bridges [38], [39] and even multilevel converters [6]. Interleaved and multilevel topologies decrease the ripple of the SMPA current and they are modular and flexible, which enables the increase of output power, bandwidth and reliability at the cost of a higher number of components and complex control strategy.

The control strategies for parallel connected HPAs rely on the closed loop control of both systems. While the SMPA is controlled to provide the load current, the LPA is controlled to ensure the load voltage. One of the most common control strategies for the SMPA, due their robustness and simplicity are the hysteresis [38], [39] and the dead-band hysteresis current control [36]. The challenges with the hysteresis are well known, such as variable frequency output and the difficulty to design filters for it. Another constraint for hysteresis-type controllers is the impossibility to work with interleaved converters, since the share of the current will not be symmetrical or the requirement of sophisticated and complex controllers. Pulse-Width Modulation on the other hand, offers a fixed switching frequency, which alleviates the challenge of the filter design and enables phased-shifted carriers to be used for modular topologies [6].

1.3. Series Connected Hybrid Power Amplifier

As mentioned before, series connected HPAs can be used for several applications, such as high power voltage amplifiers [6], [24], [29], [32], as ACPS [30], [31] and for high-end and power audio systems [4]. This study will focus on the two first applications, in addition to PHIL applications for machine emulation in motor and/or generator mode. More specifically, the study focus on applications in which the SMPA portion of the system is built with Cascaded H-Bridge Multilevel (CHBM) converters, given their modularity and flexibility [40], [41], as shown in Figure 1.4. In addition to that, a multilevel SMPA controlled with lower switching frequencies provides the benefit of lower switching losses, higher bandwidths with smaller or even no output filters and higher power density.

1.3.1. Conventional Modulation Techniques for Multilevel Inverters

There are several modulation techniques for multilevel converters, employing either half-bridge or H-Bridge cells. They can be classified as Carrier-Based PWM (CBPWM), Selective Harmonic Elimination (SHE) and Nearest Level Modulation (NLM) methods [42], [43].

CBPWM usually employs as many carriers as H-bridges, with high ratios between the frequency of the carrier (f_c) and of the modulating signal (f_m), to avoid sub-harmonics [44]. CBPWM can be classified into Level-Shifted PWM (LS-PWM) and Phase-Shifted PWM (PS-PWM) [43]. In LS-PWM, the carriers present different Direct Current (DC) offset levels while in PS-PWM, they are symmetrically phase-shifted. Power amplifiers with LS-PWM and high f_c have

been reported in the literature, but they are not suitable for high output power and high frequency applications [45]. LS-PWM is not ideal for CHBM converters since it creates unequal power distribution among the H-bridges [45].

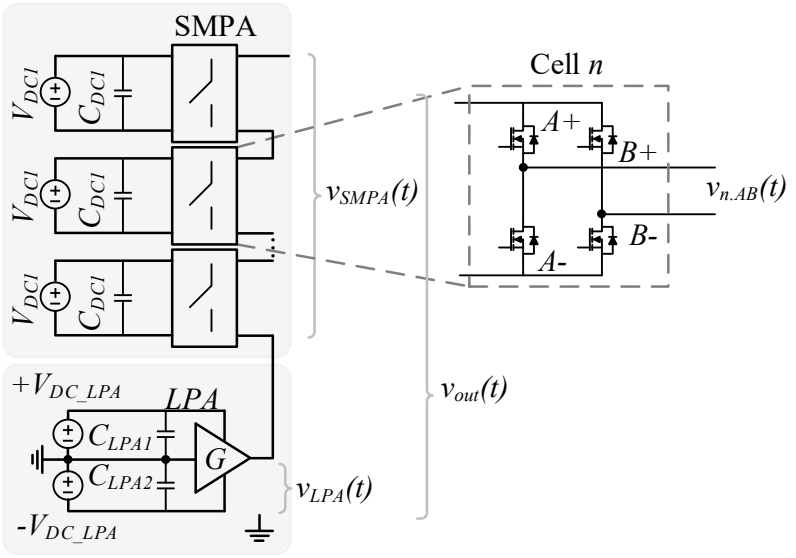


Figure 1.4 – HPA composed of a SMPA (CHBM converter) and an LPA

The SHE method employs optimization algorithms to eliminate certain low-order harmonics and improve the harmonic spectrum of the output voltage while operating with low switching frequencies. SHE can be used with one pulse per H-bridge and minimal switching frequency, which leads to a staircase-like waveform. NLM or Nearest Level Control (NLC) is a non-carrier method that also produces a staircase waveform. The modulating signal is compared to DC levels, one per H-bridge, to generate the transition angles, from one step to the next [43]. It was shown in [46] that the implementation of NLC is much simpler than SHE with one voltage pulse per H-bridge, for a similar performance in terms of harmonic spectrum.

1.3.2. Nearest Level Control Modulation Technique for Multilevel Inverters

The NLC technique is a popular technique for CHBM and Modular Multilevel Converters (MMC) [47]–[49]. The NLC technique can be described as follows [40], [48], [50]. Initially, it is assumed that the reference output voltage is sinusoidal and the CHBM is a symmetrical multilevel inverter (DC bus voltages of the *Nt*-cell CHBM converter are identical and constant to V_{DC}). In such a case, one can obtain all transition angles of the staircase waveform from those in the first 90°, known as the primary angles, due to a quarter-wave symmetry. The transition angles (γ_n) are

obtained by comparing the reference output voltage (v_{ref}) with a number of DC voltage levels (ψ_n) given by

$$\Psi_n = \left(n - \frac{1}{2}\right) V_{DC} \tag{1.1}$$

where ψ_n are the comparison voltage levels

$n = 1 \ldots Nt$

When the reference (v_{ref}) signal becomes higher than one of the comparison voltage levels, the next cell in order is turned on. The NLC method is also referred to as "roundup modulation", because it will force the output value of the SMPA to be in the closest possible multiple of V_{DC}, when compared to the instantaneous value of the reference signal. For example, if in a certain moment in time the v_{ref} is between 1.51 and 2.49 times the V_{DC} level, the control strategy will turn on two cells and output $2V_{DC}$.

Considering the system presented in Figure 1.4, Figure 1.5 shows the theoretical output voltage waveforms of the SMPA (v_{SMPA}), LPA (v_{LPA}) and the resulting output voltage of the HPA, v_{OUT} assuming that the output follows the same pattern as the voltage reference. For this example, an Nt of three was used and two different conditions were evaluated, showing the behavior of the NLC for both. All voltage comparison limits, Ψ_n, are shown in the solid lines of the top graph.

The first condition (index 1) represents the SMPA (in blue v_{SMPA1}), LPA (in gold v_{LPA1}) and HPA (in blue v_{out1}) output voltages for a reference voltage with a peak value of $3.2V_{DC}$. It can be seen that, as soon as the output voltage requires a value higher than Ψ_1, the first cell is turned on, creating the first positive transition from 0 to $1V_{DC}$. This exact moment happens when the output voltage reaches $0.5V_{DC}$. Until this moment, only the LPA was contributing to the output voltage. On the exact moment of the transition, the LPA output voltage changes from $0.5V_{DC}$ to $-0.5V_{DC}$ to preserve the required output value of $0.5V_{DC}$. This is one of the constraints of this topology, in which the LPA must be able to output at least $0.5V_{DC}$ in positive and negative quadrants. Considering a three cell CHBM, a reference signal of $3.5V_{DC}$ is the maximum value for a linear operation, meaning that any value higher than that would oblige higher LPA output voltages, higher losses and compromise of the signal bandwidth since saturation is prone to happen. To take advantage of the maximum range of voltage outputs and ensure optimal optimization of all components of the system, this limit can also be defined as the system's rated voltage. Still

considering the first condition, is it possible to see that every crossing in the voltage limits, Ψ_n, creates transitions on the SMPA and LPA output voltages, creating the staircase pattern for the first and the compensation waveform for the second.

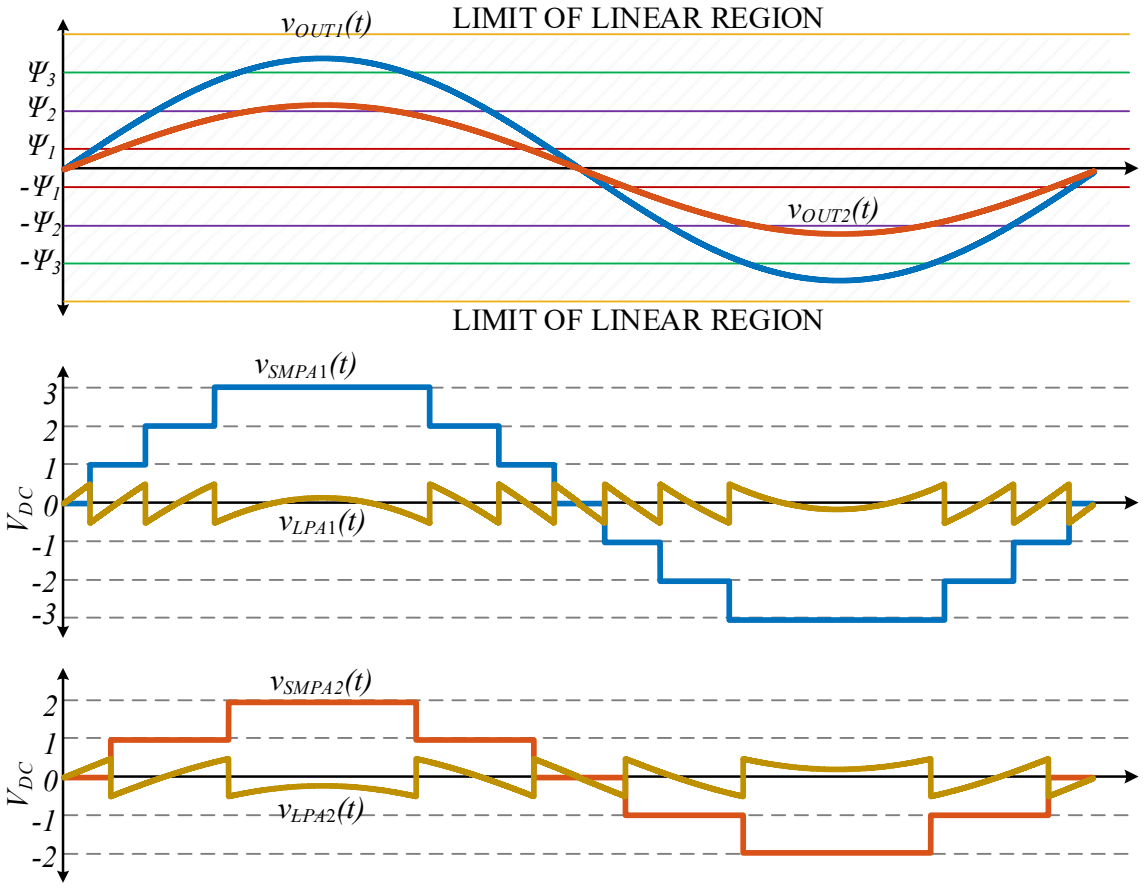


Figure 1.5 – Theoretical reference/output voltage waveforms of the SMPA (in blue), LPA (in gold) and HPA (in blue/red - top) for two different conditions.

The second example (index 2) represents the SMPA (in red v_{SMPA2}), LPA (in gold v_{LPA2}) and HPA (in red v_{OUT2}) output voltages for a reference voltage with a peak value of $1.8V_{DC}$. Since the output peak voltage is smaller, it takes more time for the output voltage value to reach the first voltage limit, Ψ_1. The LPA is, in this case, responsible to take over the load for a longer time, although with lower voltage. One important aspect for this condition is that the output voltage is never higher than Ψ_3 ($2.5V_{DC}$), which means that the third cell is never on. This can be seen when the two SMPA waveforms are compared, considering that, the first one has three positive levels and the second only two (not considering the zero level).

Assuming that the peak value of v_{ref} ($\hat{v}_{ref}$) is smaller or equal to $(Nt+½)V_{DC}$, the limit of the linear operation of the CHBM converter, as shown in Figure 1.5, the primary angles (n = 1 ... Nt) are given by

$$\gamma_n = \sin^{-1}\left(\frac{\Psi_n}{\hat{v}_{ref}}\right) = \sin^{-1}\left[\frac{\left(n-\frac{1}{2}\right)V_{DC}}{\hat{v}_{ref}}\right] \tag{1.2}$$

where γ_n are the primary transition angles

If $\hat{v}_{ref}$ is higher than the cited limit, the LPA will have to contribute not only with the harmonic compensation, but also with some portion of the fundamental frequency component. This is only possible if the LPA still has not reached its maximum output voltage, otherwise it will lead the system to saturation or clipping of the output voltage, compromising the overall quality of the output. The number of primary angles, and consequently the number of voltage levels in a half-cycle of the staircase waveform (only considering non-zero levels), will be lower than Nt (maximum) if

$$\hat{v}_{ref} < \left(Nt+\frac{1}{2}\right)V_{DC} \tag{1.3}$$

Figure 1.6 shows some waveforms to illustrate the generation of the staircase voltage waveforms using the NLC technique, once again for a three-cell CHBM converter but with additional focus on the power consumption for each cell. Two sinusoidal outputs, as presented in Figure 1.5, with peak values of 3.2 and $1.8V_{DC}$ will be again used as reference.

Each one of the possible outputs will demand from the SMPA to output voltage waveforms as shown in Figure 1.6 (on the top screen) with peak values of $3V_{DC}$, in blue at the left, and $2V_{DC}$, in red at the right. The first intersects three comparison voltage levels (1.1), producing a staircase of three non-zero positive levels, while the second only intersects two voltage levels.

The transition angles obtained with the NLC technique can be used in different ways to produce a staircase voltage waveform, depending on the type of multilevel converter. For CHBM converters, there are two main modulation techniques. The first one is called First-In Last-Out (FILO), where the first cell, or H-bridge, to be turned on is the last one to be turned off [50]. On the top of Figure 1.6, one can see waveforms for a CHBM converter with three H-bridges operating with FILO and voltage references that require from the SMPA $3V_{DC}$ (left) and 2 V_{DC} (right). They

show the positive semi-cycle of v_{SMPA} and the output voltage of each H-bridge, which present different pulse widths. Besides, it shows the power supplied by each H-bridge (P_1, P_2 and P_3) considering a resistive load. It is evident that those values are quite different, showing the power unbalance among the three H-bridges. The issue is more critical when the reference voltage requires only $2V_{DC}$ from the SMPA, top right, where $P_3 = 0$. One can mitigate this issue somewhat by swapping the transition angles (pulses) sent to each H-Bridge every fundamental cycle. However, this creates a sub-harmonic power ripple [51], [52].

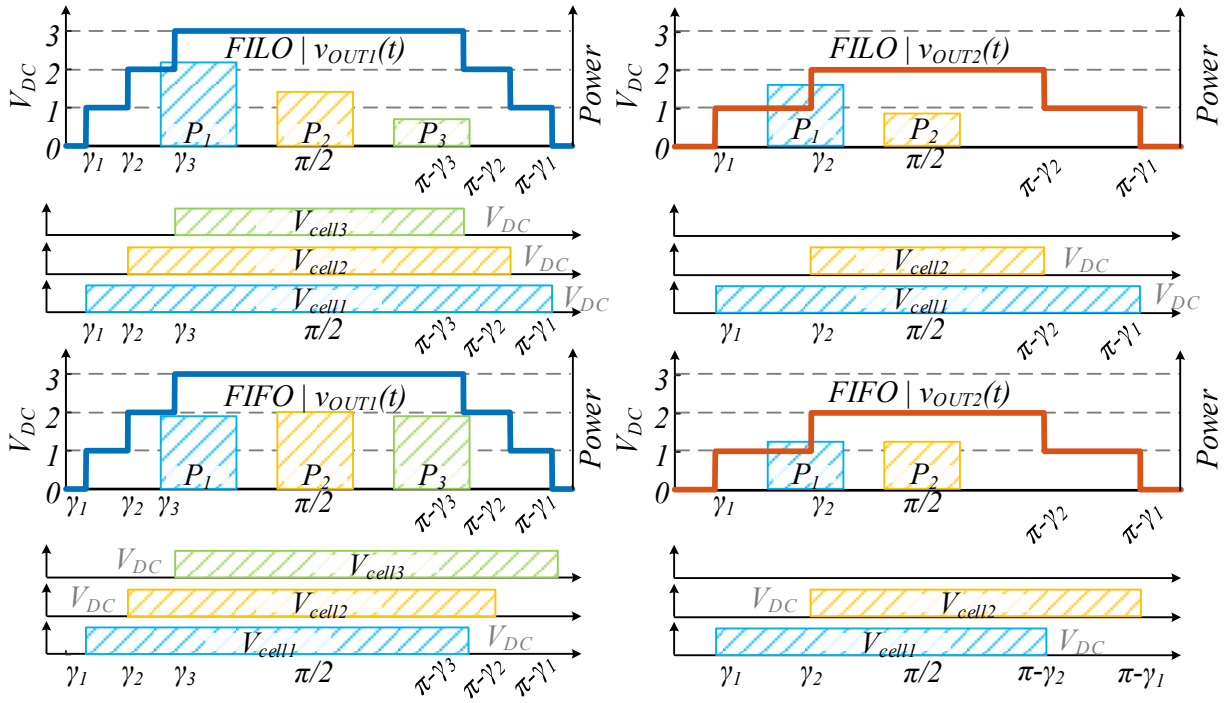


Figure 1.6 – Output voltages of the SMPA, H-bridge cells and their power contributions considering a high ($3.2V_{DC}$ with v_{out1}) and medium ($1.8V_{DC}$ with v_{out2}) reference voltages with FILO (top) FIFO (bottom)

The second conventional technique is called First-In First-Out (FIFO), where the first H-bridge to be turned on is also the first to be turned off [53], [54]. The benefits of FIFO can be observed by comparing the waveforms of the second row of Figure 1.6 (FIFO) with the first row (FILO). For the $3.2V_{DC}$ peak output voltage, on the left, the pulse widths of the output voltages of the three H-bridges are similar leading to a better power balance among H-bridges. However, as shown in the bottom-right of Figure 1.6, FIFO cannot avoid having one H-bridge always off ($P_3 = 0$), when the peak reference voltage is $1.8V_{DC}$. It should be noted that for both FILO and FIFO,

only one H-bridge would be activated for peak reference voltages between $0.5V_{DC}$ and $1.5V_{DC}$. This issue has been reported in the literature [51]–[56], and is of concern in series HPA applications, where operation with lower modulation signals for lower output voltages is more likely to occur.

It is well known that load demand variation plays a key role in the voltage regulation efforts of DC power supplies. A poor regulation of the DC power supplies will cause the SMPA voltage steps to be smaller than the desired multiplier of V_{DC}. This corresponds to a change and reduction on the linear region limits. This will cause the LPA to provide higher voltage levels to compensate it. This does not translate automatically to higher losses, but it may limit drastically the HPA bandwidth if the LPA starts to saturate or clip the signal. There should always be a safety margin between the rated and maximum LPA voltage, but if a large margin is used, it corresponds to a larger and more costly LPA.

Therefore, if one wishes to employ a lower cost multi-output DC source, as in [57], with a single controlled output, the (active) power demanded by the H-bridges should be well balanced. However, available techniques such as FILO and FIFO do not promote or focus on this matter. What is more, unbalanced power implies different voltage and current stresses on the switches, which can reduce the reliability of some H-bridges and of the overall system over time. As mentioned before, some techniques achieve better power balance by swapping the control signals for each input reference cycle but generate low order harmonics on the system [51], [52]. This technique is not considered under this study, because it focuses on strategies that can provide improvement on the balance within a reference cycle. With a better balance between the cells, the filters at the input side of the H-Bridges can be smaller and more uniform, since the variation and ripple on the power will be similar for all cells, independent of the input reference conditions.

1.3.3. Conventional Series Connected HPA Topologies

A symmetrical CHBM converter as a SMPA with a high slew-rate LPA to provide high power density and bandwidth, as shown in Figure 1.7, is presented in [5] and referred to as Multicell Cascaded Power Amplifier (MCCPA). The topology is completely bidirectional, able to source or sink power. The same topology [5] is also evaluated in [32] for symmetrical and asymmetrical multilevel SMPAs, however it acts as a controlled output current source, while [5] operates as an isolated voltage source. In [5] the design, modeling and simulation of the proposed

HPA is presented, while in [31], [58] the experimental validation of the system is demonstrated. The NLC technique is used to find the primary commutation angles and the unbalanced power consumption, caused by the FILO strategy, by the CHBM cells is evaluated [5].

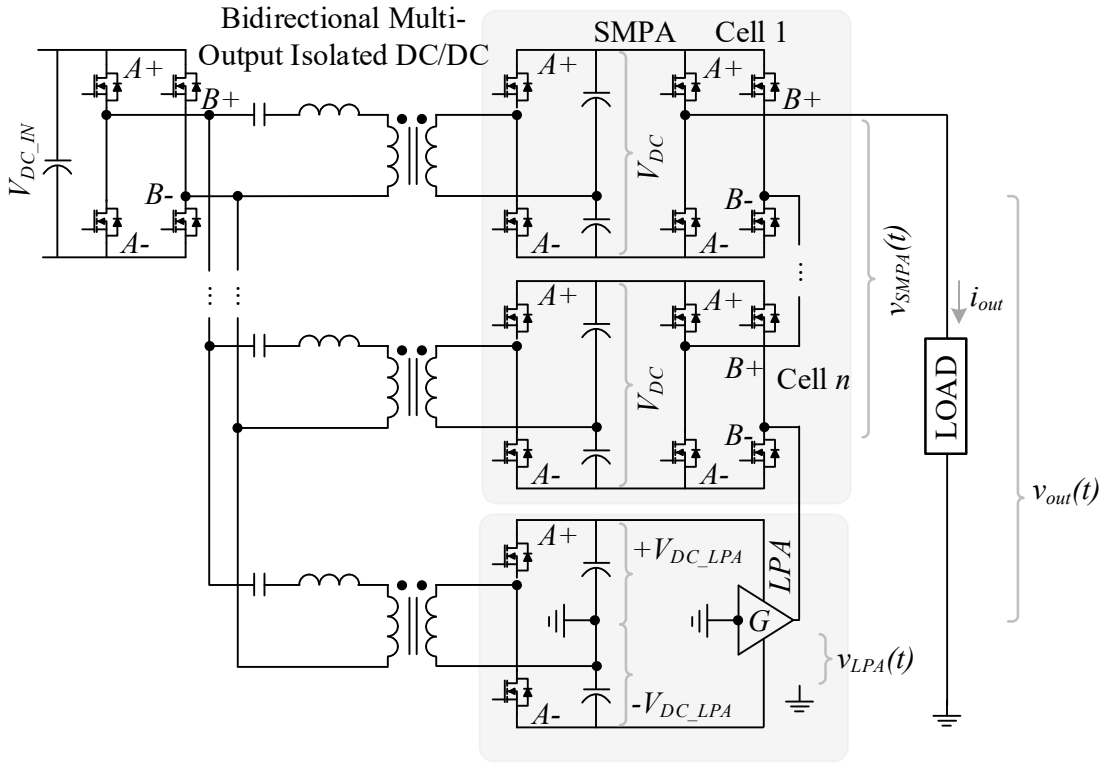


Figure 1.7 – Series connected HPA [5]

The MCCPA topology is designed to be an ACPS and achieves a high output voltage and control bandwidth of 20 kHz (meaning the MCCPA can output voltages or voltage harmonic components until that frequency), 1.1 kW output power and sinusoidal output voltage of 80 to 240 Vac. The SMPA is controlled with an analog implementation of the NLC technique, as shown in Figure 1.8.

The effects of the staircase and NLC modulation, using FILO as the method to generate the individual pulses are visible in Figure 1.9. For a 10-cell CHBM, under rated conditions it is possible to see the difference on the cell's output power of more than three times when considering the higher and the lower. Although the output range of the converter is from 80 to 240 Vac, the study does not evaluate different modulation indexes than the rated (highest), where clearly a few or even close to half of the cells would be off.

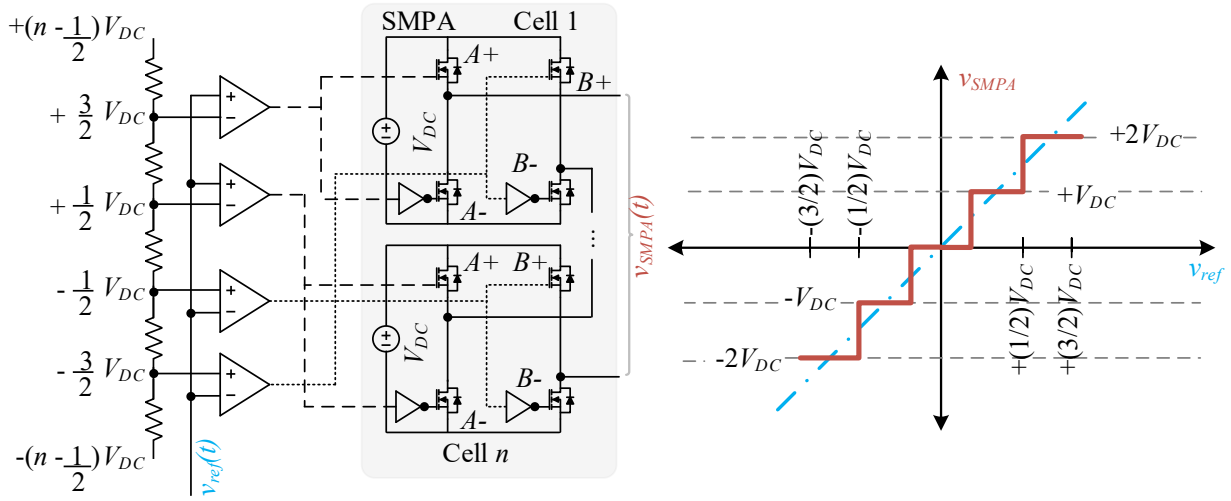


Figure 1.8 – Nearest Level of Control modulation technique

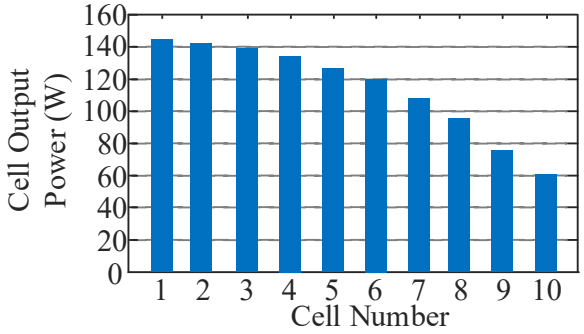


Figure 1.9 – Unbalanced consumption of multilevel cells [5].

Based on the MCCPA, two alternative systems are proposed [31], [58]. In the first, an Amplitude-Modulated and PWM Multicell Amplifier (AP-MCA) is proposed, with a replacement of the LPA by another H-Bridge, controlled in higher switching frequencies (500 kHz PWM signals generated and controlled by a Field-Programmable Gate Array, FPGA). The unbalance on the SMPA cells, which are controlled again with the NLC method is not solved or investigated for rated or below rated condition. Similar study is presented in [49]. The second alternative is to control all the H-Bridges with a 50 kHz/cell interleaved method, as in the PWM MCA (P-MCA), reaching at the end once again the effective switching frequency of 500 kHz. Although a valid approach, the second alternative increases the system (switching) losses and neither of the AP-MCA or P-MCA discuss the power unbalance of the H-Bridge cells for any conditions. Even though AP-MCA and P-MCA are not hybrid topologies, meaning they apply only SMPAs in

series, they are worth mentioning, since they both use the same CHBM SMPA as this study for the bulk processing of power. On top of that, AP-MCA models and controls the last H-Bridge cell to behave as an LPA.

Also in [31], the experimental validation of [5] is presented. Some constraints are changed, such as the output voltage and control bandwidth, which is reduced to 5 kHz and the output voltage range, which is increased to 0 to 270 Vac. Although [31], [58] present an in-depth study on the control strategies, it does not evaluate the dynamic conditions and the impact of the modulation techniques on the power consumption of the H-Bridge cells.

Another study considers the use of a multilevel inverter as SMPA in series connection with an LPA, such as the Hybrid AC Power Source (H-ACPS) [35], [57]. The SMPA part is built in a similar configuration as in [5], [31] but instead of H-Bridges, half-bridges are used in series, as it can be seen in Figure 1.10.

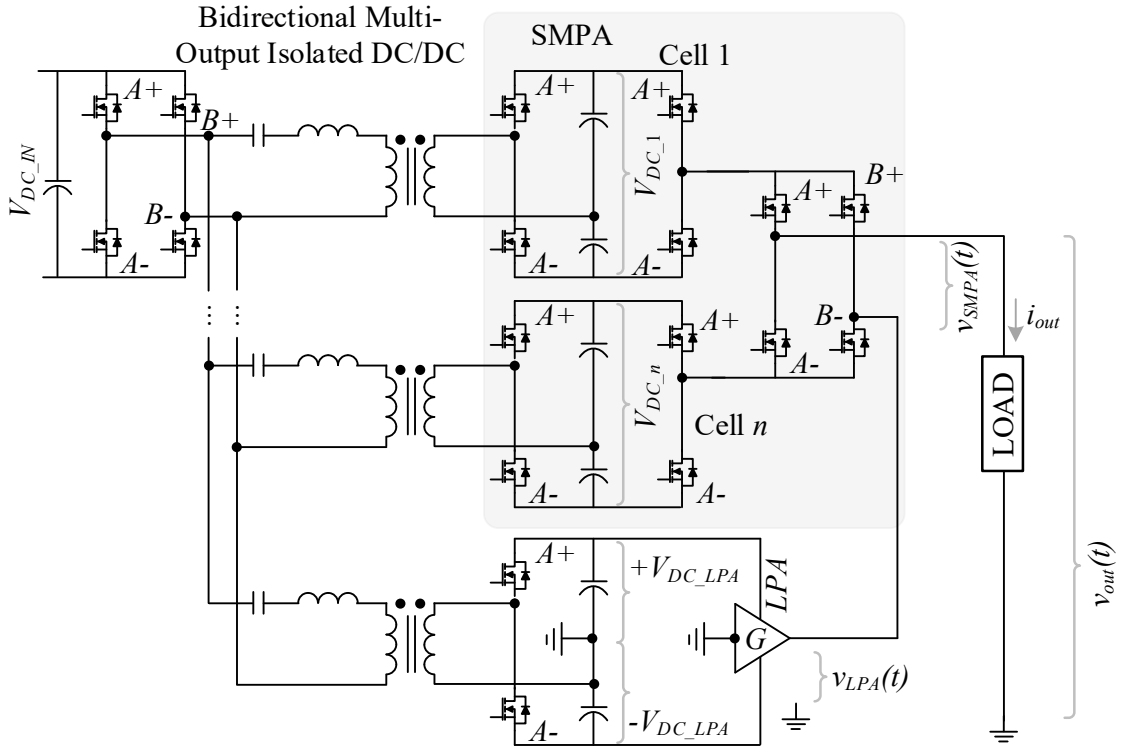
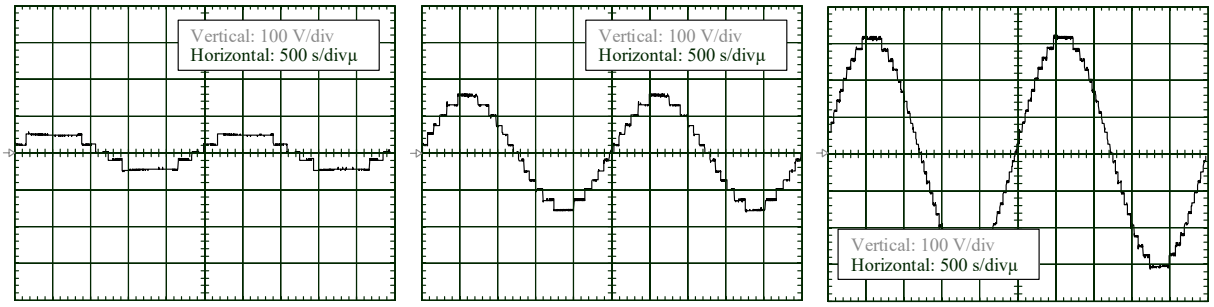


Figure 1.10 – Series connected HPA with *n* half-bridge cells and one inverter H-Bridge

All the *n* cells are only able to output signals with one polarity, same as V_{DC_1} and V_{DC_n}, so an additional high voltage H-Bridge is required to output positive and negative values, one of the most common requirements for an ACPS or generic HPA. The H-ACPS has a smaller component

count, which is even more evident considering a higher number of cells, but the unbalanced power consumption by the cells (now half-bridges) is still present.

The experimental results of [35], are presented in Figure 1.11, showing the output waveform of the SMPA, considering HPA outputs of 50 Vrms, 115 Vrms and 220 Vrms. The topology is evaluated for symmetrical and asymmetrical DC sources. The latest has the advantage of the SMPA being able to synthetize more voltage levels with the same number of cells but the complexity is higher, since several DC sources have to be used or designed. In addition, the design of a single front-end DC-DC converter with multiple outputs of different voltages is more challenging. In [35], lower modulations indexes are used on the evaluation of the experimental results, but there is no detailing of the power consumption of each cell for any of the configuration (symmetrical/asymmetrical). The asymmetrical configuration can promote even worse conditions for unbalance based on the choices for the DC supply levels. This can significantly affect the load regulation on the secondary side of the front-end converter, increasing the LPA output voltage closer or above saturation regions, compromising the quality of the output or requiring an excessive larger and more expensive LPA.



(a) (b) (c)

Figure 1.11 – SMPA output waveforms for an HPA output of (a) 50 Vrms, (b) 115 Vrms, (c) 220 Vrms [35]

Since the previous topologies did not present any studies or considerations regarding the unbalance in CHBM cells, there is a clear research opportunity to tackle this problematic. Consider that all cells of a CHBM are built with forced-commutated switches and all cells require independent DC sources, gate drivers and protection circuits. Every component, circuit and printed circuit board (PCB) has a limited amount of times it can be used. Ideally, all these components, if used at the same rate, same number of times, statistically will have similar life expectancy. Using

cells of a multilevel converter equally (or as close to that) means improved load sharing and power balance. Expanding this concept to an industrial point of view, means that an equipment built with better power balance has a better possibility of lasting longer and being more economically viable. As presented in this section, there are techniques available that promote improvements on the power balance contribution of multilevel converter cells operating with one pulse per line cycle and for rated conditions but not for low modulation indexes.

1.4. Parallel Connected Hybrid Power Amplifier and Switched Mode Power Amplifiers

This section includes a literature review of parallel hybrid power amplifiers (built with a SMPA and LPA) and parallel SMPAs, as shown in Figure 1.12 and Figure 1.13, respectively. Although the latest is a pure switched solution, both parallel topologies under review can be used either as a general ACPS or as a Machine Emulator (ME). The pure switched parallel SMPA has the objective of increasing the available power, reducing current ripple using interleaved techniques, which relates to a higher output waveform quality. Due to the similarities between the two parallel topology types and their common utilization, they will be evaluated together.

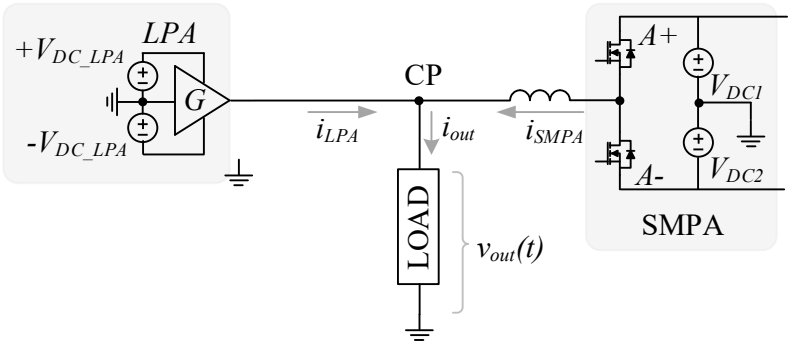


Figure 1.12 – Parallel connected HPA with H-Bridge [6], [24], [36].

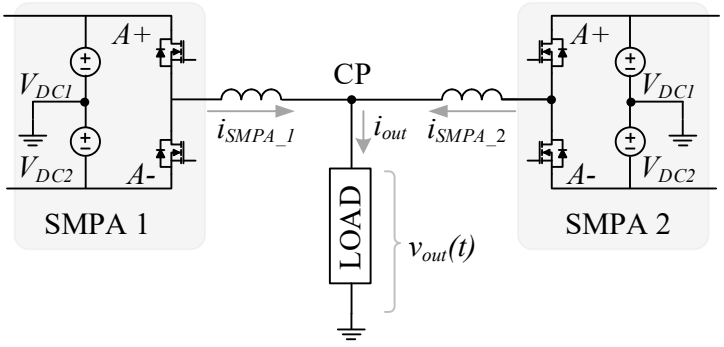


Figure 1.13 – Switched parallel connected HPA

Parallel topologies are also very diffuse and well known in the literature and industry. The SMPA and LPA outputs are connected in parallel, as shown in Figure 1.12 for the hybrid configuration, and in Figure 1.13 for the pure switched parallel configuration. The later can also be understood as an interleaved converter. Traditional DC-DC converters, such as buck, boost, VSC or multilevel converters, such as CHBM converter, flying capacitor converter, Neutral-Point Diode-Clamped (NPDC) converter, MMC are used as SMPA. The later, and other topologies of multilevel converters, are good candidates to be used as SMPA since they allow further voltage stress reduction of the power devices, switching losses reduction and high-quality output waveform with low Electromagnetic Interference (EMI) [31].

In the hybrid configuration, the LPA limits the overall system voltage, since the LPA must withstand the full output voltage while being sized for a share of the load current. While both parallel and series systems are usually controlled to regulate output voltages (especially for ACPS applications), the parallel configuration will require inner current control loops. The LPA in the parallel configuration has an analog operation to a shunt active power filter, injecting harmonic content to smooth the load current. This configuration is mostly used for high-end audio applications [6], [36], but also used for RF applications [59] and low voltage power supplies [60].

1.4.1. Parallel Connected Hybrid Power Amplifiers

This section will focus on the HPA built with the parallel connection of SMPA and LPAs, presenting the base topologies and their main applications, advantages, disadvantages and limitations. The same topology is used in [6], [24], [36] for ACPS and audio applications. It is a half-bridge converter as SMPA, connected to positive and negative DC sources. The SMPA contributes to the bulk portion of the load current and it is connected to the load using a single coupling inductor, which partially determines the output current switching frequency ripple. The LPA is controlled to compensate this ripple. Control strategies are designed to make the LPA output impedance as small as possible, to compensate for the effects of the switching frequency ripple with enough bandwidth. As required by the parallel configuration, the LPA still has to withstand the same SMPA and load voltage.

An alternative to a class D power amplifier (SMPA), to reduce the complexity and limitation of the high-order filters, is presented in [24], as shown in Figure 1.12. The LPA operates as an active filter to compensate the switching frequency ripple from the SMPA. The topology uses a

half-bridge converter as SMPA with a hysteresis current control connected in parallel with a (Class AB) LPA. Between the Coupling Point (CP) and the LPA there is the filter coupling network, or L_{COUP}, which is a single inductor that yields a first-order coupling transfer function. The SMPA is switched at 100 kHz and the HPA bandwidth corresponds to the higher bandwidth between the LPA and SMPA (usually LPA due to its high slew rates), which is experimentally validated. For the control strategy, the chosen way to control the SMPA switches was the bang-bang, a classical hysteresis controller, as shown in Figure 1.14. While monitoring the LPA current between positive and negative thresholds, the controller decides which one of the switches, connected to positive or negative buses, must be turned on, creating the repetitive process to form a self-oscillating regulating system. Theoretically, this strategy can be used for ME, but only for current-in voltage-out machine models, since the reference for the controller is based on the load voltage. Machine models based entirely on current-in and voltage-out strategy are mathematical models in which the machine excitation voltage is found using the line current drawn by the machine model. The main disadvantage is the reduced machine emulation accuracy [62]. Further in the study, additional models will be evaluated and detailed. The main drawback of the topology presented in [24] and its control strategy is the high current requirement of the LPA, which must be capable of outputting current in steady state based on the chosen hysteresis current control band. In addition, controllers based in hysteresis actions produce outputs with variable frequencies, which demand more complex filter designs.

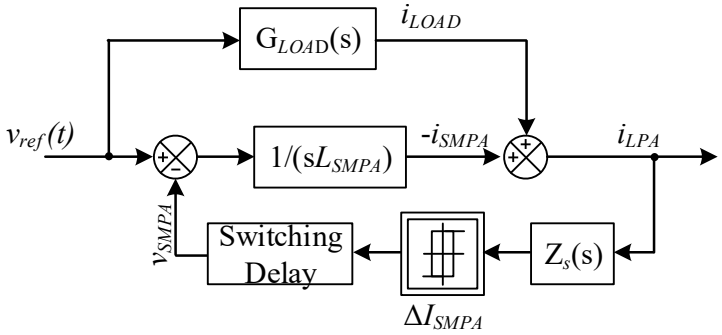


Figure 1.14 – Bang-bang controller for parallel topology [24]

Similarly as [24], a half-bridge as SMPA in parallel connection with an LPA is modelled and simulated in order to evaluate the tradeoffs between switching frequency, coupling network

impedance value, ripple current, bandwidth and power dissipation [6]. Figure 1.15 shows the proposed topology. Once again, the SMPA is switched with variable frequency because of the hysteresis control, as in Figure 1.14, reaching a maximum frequency of 200 kHz. There are improvements on the LPA feedback loop, which lowers its output impedance. In addition, several novel topologies of HPAs are presented, as shown in Figure 1.16, including unidirectional half-bridges, interleaved half-bridges (for increased output current with low ripple) and neutral point diode clamped multilevel converter as SMPA. Since the same control is used, still based on the voltage reference as an input signal, this topology can be used for ME, but is limited to current-in voltage-out models.

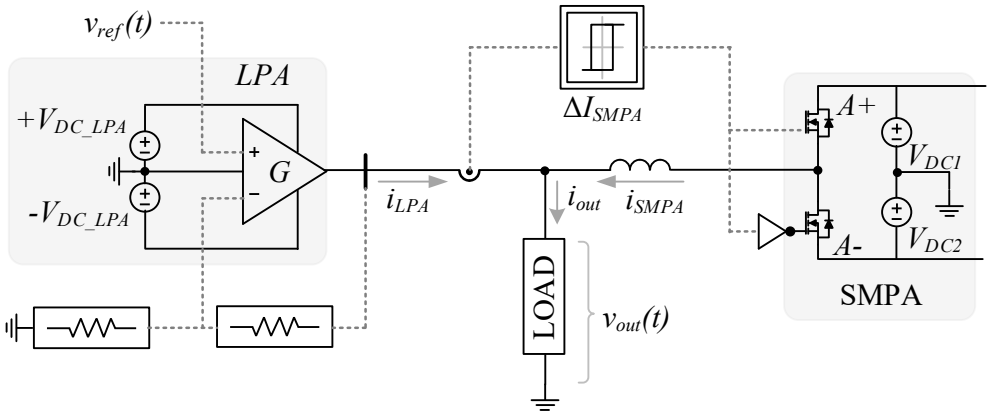


Figure 1.15 – Parallel connected HPA with hysteresis controller [6]

Based on [6], a topology with two unidirectional buck converters as SMPA with a new control is proposed by [36], using two independent hysteresis controllers, also known as dead-band control, as shown in Figure 1.17. This control strategy is designed to ensure that the LPA will contribute alone in cases of low current and power, increasing the output quality for this range as well. The LPA is controlled in voltage mode and the reference current for the SMPA comes from the actual current of the LPA. Since the LPA is voltage controlled, and the SMPA is current controlled, no further analysis is needed for stability analysis because the control has two independent variables. It is very important in terms of making sure that the output current of the LPA is kept under a maximum value. It suffices to keep the output voltage smaller than a certain value. On the other hand, if the load impedance changes, some sort of outer current loop, limiting the reference voltage of the LPA, would be necessary to keep the LPA's current lower than rated at all times. With the dead-band controller, only for output power higher than 2 W, the SMPA will

take over the main part of the load. The SMPA is switched at a variable frequency, with a maximum value of 130 kHz. The power bandwidth of the system is around 10 kHz but it presents significant noise after 6 kHz.

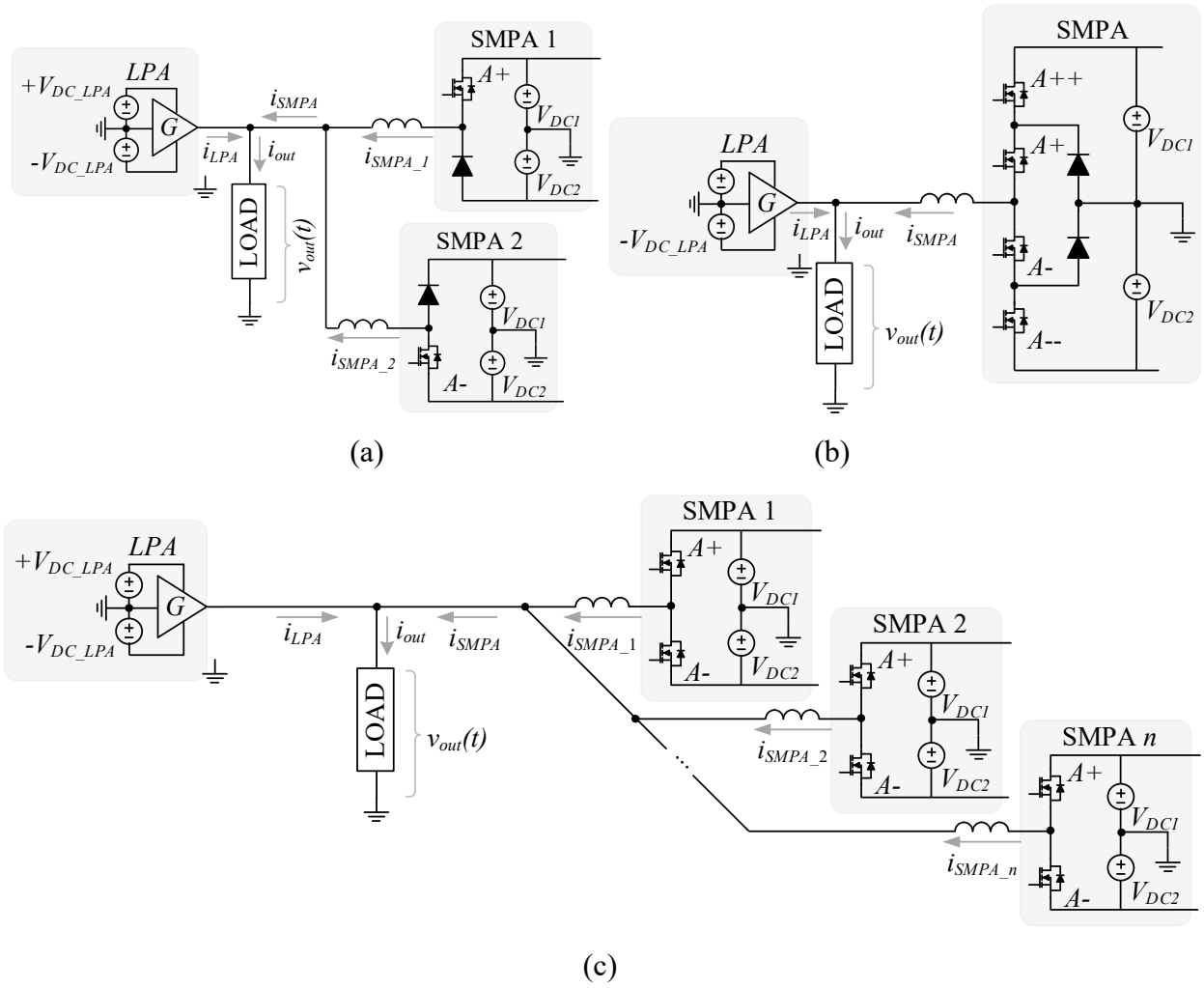


Figure 1.16 – Alternative HPAs proposed by [6] (a) unidirectional half-bridges (b) neutral-point diode-clamped multilevel converter and (c) interleaved half-bridges as SMPA

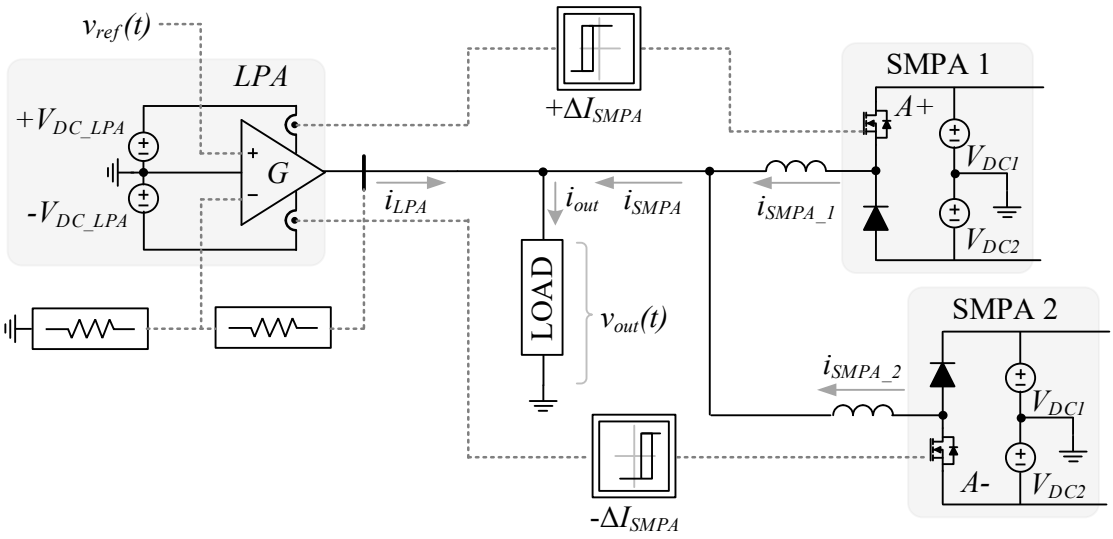


Figure 1.17 – Parallel connected HPA with dead-band controller [36]

1.4.2. Power Amplifiers for Machine Emulation

This subsection will focus on the different configurations of SMPAs and LPAs (not necessary using both at the same time) and their relevance to Machine Emulation (ME) for PHIL applications. ME system consists essentially of a Real-Time Simulator (RTS), where the machine model is emulated, and a Power Amplifier (PA) that is connected to a physical motor drive, Inverter Under Test (IUT) or the utility system. Sensors placed between the motor drive, or utility system, and the PA, provide the feedback signals required for the RTS to compute the reference current, or voltage, signals corresponding to the emulated machine. These signals are sent to the PA that replicates the machine terminals behavior according to the action of the motor drive and the virtual mechanical torque in the shaft of the emulated machine [15], [22], [63]. The accuracy of the ME system depends on the machine model [64]–[66], on the time step of the RTS [66], [67] and on the closed loop bandwidth of the PA and its controller [62], [68], [69]. Conversely, its cost is determined mostly by the PA, which is one of the problems that this study investigates. ME is also a specific application of power electronics based load emulation. In this broader field, not only the effects of machines can be emulated, but also any previously modelled linear, non-linear and transient loads can be implemented [22], [68], [70], [71].

RTS is a specific category of simulation in which a model is executed in a digital domain on a processing unit at the same time rate (or time step) as the real physical system under evaluation [72]. In power electronics and power systems, the models are extracted mathematically and should

have an acceptable degree of fidelity with the actual voltages and currents of the physical system. Low time steps are desired to execute complex models with high accuracy but they would also require a high computational burden [72]–[74]. Typically, a RTS can be implemented in a variety of processing units such as Digital Signal Processors (DSP), Field-Programmable Gate Array (FPGA), Personal Computers (PC) microprocessors [73] or combinations of them. For instance, RTSs such as the OPAL-RT OP4510 [73], [74] combines the FPGA and the Central Processing Unit (CPU) for enhanced performance. An RTS can execute models on its CPU cores with time steps on the tens of microseconds, while on the FPGA, it can go as low as tens of nanoseconds [73], The challenge that comes with the low FPGA's time step is the difficulty of programming it (lower level coding), the bitstream generation and the flashing of the code. The bitstream generation procedure, which is time consuming, needs to be repeated for minor changes in the model as machine model modifications [74]. This is avoided when using the CPU of the RTS solution [74], which is integrated with Matlab/Simulink (higher level coding) providing significantly lower compiling times. This study will use the latter approach due to its high simplicity when compared to low-level FPGA programming.

As previously introduced, machine models are used to replicate the behavior of actual machines in a computational model that can be reproduced by simulation or emulation using a PA. The complexity of the models are proportional to type of machine and the additional effects that are included on it, such as variations on armature and stator parameters, saturations, flux leakages and others [75]. The models under the scope of this study can be classified in current-in voltage-out or voltage-in current-out. The first reads the current on the coupling element and uses it as an input to find the actual motor voltages to be synthesized by the PA [69], [76]. The technique is less precise since it can lead to undesired voltage drops on the coupling element. The voltage-in current-out models can include models that are more precise because they provide the current reference considering all desired effects and saturations. They read the input voltage at the IUT side and provide the reference for the machine currents to be drawn by the emulating PA [64], [65], [77]–[79].

In several cases, the IUT operates in current control mode [65], [69], [76], [80]. As stated before, the ME and PA deliver more precise outputs when also operating in current control mode [12]. This leads to both systems being controlled at the same time in current control mode, which characterizes a control conflict, causing control oscillations and compromising the stability of the

emulation system, since two systems are controlling the same variable (the current at the common or coupling point).

To solve this conflict, [65] uses a transformer-based LCL filter with additional coupling elements in each side of the PA and IUT, as shown in Figure 1.18. The inclusion of the LCL filters enables the use of a voltage-in current-out model and the voltage control mode of the PA by removing the conflict of both elements trying to control the current. Two problems arise from that action. The first is the challenge associated with generating the voltage reference for the PA, since the controller must implement the necessary voltage difference (because of the added phase) between the IUT and PA in order to achieve the desired ME current. The second is related to the LCL coupling network with second order filters at each terminal, which reduces the maximum bandwidth and consequently the accuracy of the emulation. High-fidelity models cannot be emulated with limited bandwidth. Filter elements are prone to causing oscillations and the external resistive damping element causes excessive losses on the system. The LCL as a coupling network between a grid (or an IUT) and power electronics based loads, including ME cases is also evaluated in [22], [68], [70], [71]. In [65] the inclusion of the delta-wye transformer enables a lower voltage amplifier to be connected with higher voltage IUT, with the challenge of the inclusion of a 30° phase-shift on the voltages between PA and IUT, that must be compensated on the control loops.

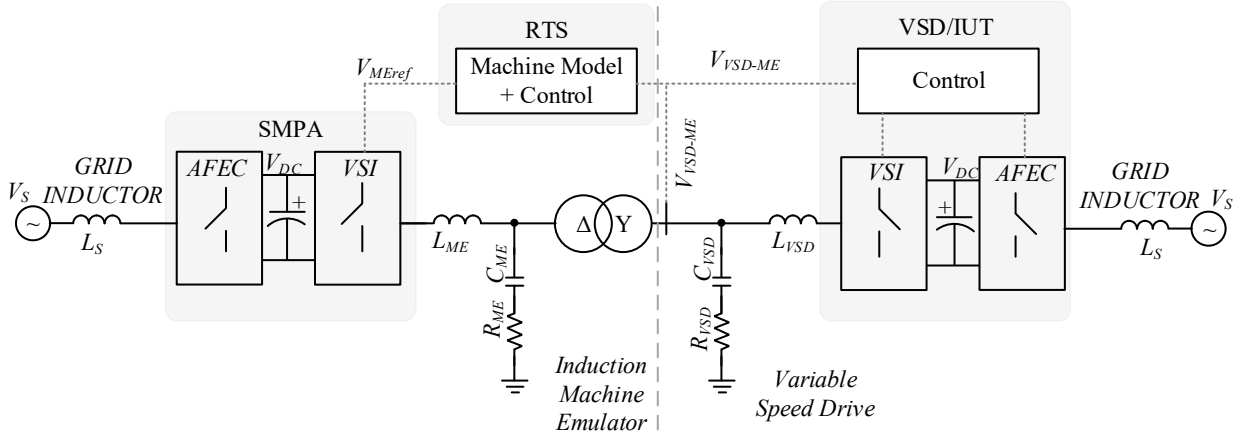


Figure 1.18 – Induction machine emulator with transformer-based LCL coupling [65]

Another alternative to solve the conflict between control strategies is explored by [67], [69], [76], [80] with an inverted machine model based on current-in voltage-out. The model reads the line current drawn by the machine model and generates a respective voltage of the machine terminals, which is used as voltage reference to the PA responsible for the ME.

In [69], a parallel configuration is used, with five three-phase Voltage Source Inverters (VSIs) operating in parallel, as shown in Figure 1.19. The sequential switching is used, by shifting the PWM carriers by 70° (360°/5), generating a combined switching frequency of 40 kHz. Placing VSIs in parallel the SMPA will increase its current capacities, reduce the current ripple and consequently increase its output bandwidth, making it possible to emulate models that are more complex. The disadvantage is the higher complexity and the number of components (switches and gate drivers). As the induction machine model used is based on current-in voltage-out, referred to as an "inverted machine model" (it calculates the machine voltage as a response on the machine current controlled by IUT), a closed loop current control on the PA can be avoided. These current-in voltage-out models are based on approximated models and they do not contain all details related to the machine geometry and magnetics, non-modeled saturation effects, delays, switches voltage drops, dead time on the inverter legs and filter losses, reducing the accuracy of the emulation. The emulated motor drawn currents from the model present an adequate tracking performance, but the switching harmonics are not properly attenuated. In addition, the zero-crossing regions of the emulated motor drawn currents present a significant distortion, caused by non-attenuated low order harmonics.

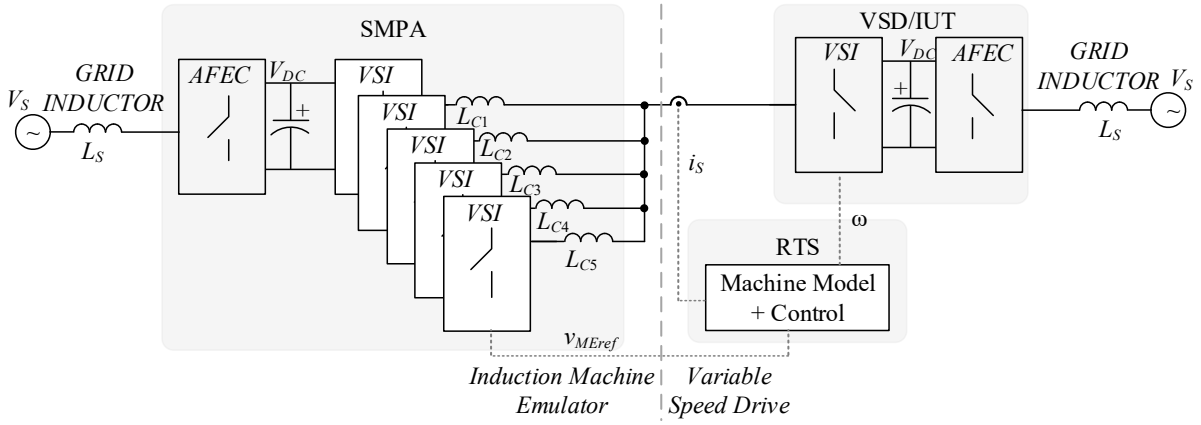


Figure 1.19 – Five sequentially switched SMPA in parallel for ME [69].

Another strategy considers maintaining both components (PA and IUT) in current control mode but with different closed loop control bandwidths, similar to an inner and outer loop control. In [62] an ME system implemented with a SMPA (back-to-back 6-switch three-phase Voltage Source Converters, VSCs) is evaluated, while running voltage-in and current-out complex permanent magnet synchronous machine (PMSM) model built using finite element analysis

(FEA), as shown in Figure 1.20. It includes a simple inductance as coupling impedance between the actual drive inverter and the SMPA. The grid-side VSC is controlled as an Active Front End Converter (AFEC) to provide 4-quadrant capabilities to the SMPA and regulate the intermediate DC bus voltage [81]. The SMPA at the coupling point, acting as the main ME, is switched at 20 kHz and controlled with an RTS (20 µs sampling time) using a coupling inductance of 3 mH, presenting a current bandwidth of 1.8 kHz. The IUT current bandwidth is set at 350 Hz and the experimental results proved that a SMPA bandwidth of five times higher than that of the IUT is enough to keep the system stable and with high accuracy, considering even magnetic (saturation) and geometric (cogging-torque) characteristics of the model, since the results achieved with the ME system were very similar to the actual physical machine. The PMSM FEA model is implemented on the digital processor of the RTS, in which the sampling time had to be higher than when it was implemented in the FPGA. This negatively affects the bandwidth of the current control loop but significantly simplifies the complexity of the setup. Considering the limitations on the maximum current control bandwidth (BW), this setup might not be sufficient for testing motor drives with high BW, such as those used in power steering applications [82].

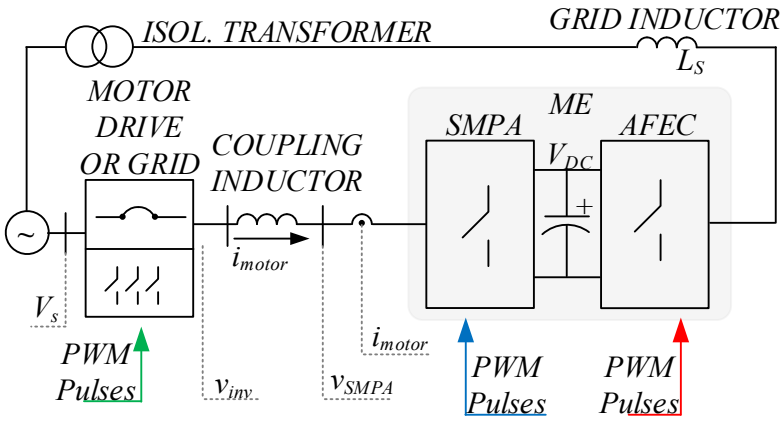


Figure 1.20 – SMPA with back-to-back AFEC as bidirectional ME [62]

Still with the same strategy of using closed loop current control on both IUT and PA, with bandwidths as far as possible, [19], [61] evaluates an LPA for machine emulation, as shown in Figure 1.21. In [19], the study is similar to [62] with two main different aspects. The first is that another voltage-in current out machine model is being validated, a Variable Flux Machine (VFM), obtained once again using FEA tools. The model is based on look-up tables containing the variation of machine inductances, flux and lastly torque, considering variations of rotor positions, winding

current and different magnetization levels. The second is the replacement of the SMPA with a 4-quadrant (4Q) LPA and the elimination of the grid (side) inductor. The LPA used [25] has a 100 kHz open loop voltage BW controlled with an RTS (5 µs sampling time). Connected to the LPA there is a coupling inductance of 5 mH, which results in a closed loop current BW of 7.5 kHz for the emulation of a Variable Flux Machine (VFM), fifteen times higher than the close loop current control BW of the IUT inverter. It is worth mentioning that the RTS used in [19] implements the control actions on a FPGA, which demands a high complexity, low level programming, which is a drawback of the proposed system implementation. It requires lower level coding, time-consuming bitstream generation and the flashing of the code, which can take up to 4 to 5 hours and needs to be repeated for minor changes in the model as machine model modification, gain adjustments or parameters tune ups [74].

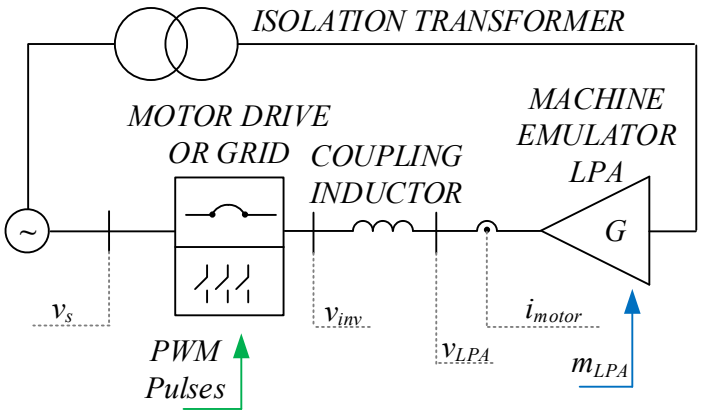


Figure 1.21 – Machine emulation system with LPA [19], [61]

When compared to the SMPA [62], the increase of the closed loop LPA bandwidth [19], as ME, is possible because of the FPGA lower sampling time, the LPA higher open loop BW and there is no limitation of the switching frequency of the SMPA. In addition, the rule of thumb for designing closed loops based on switched converters is to set the bandwidths at one tenth (or a decade below) of the switching frequency [83]. It should be noted that most LPAs can operate as voltage and as current sources [25]. One issue in the current source mode is that the gain varies with the load impedance. Thus, for the emulation of machines using a voltage-in current-out model, one can operate the LPA in the voltage source mode but needs to create a current control loop for the LPA, which leads to a lower closed loop BW. Also, the SMPA [62] and LPA [19] as ME studies are used to validate proposed models but they do not present a systematic approach for

calculating the parameters used in the system, which makes it difficult comparing their implications. The LPA ME [19] has the advantage of working with more precise machine models and presents a way to overcome the current conflict. The main disadvantage of the study is the high cost associated with the LPA [25] and the complexity of the practical implementation because of the FPGA.

A voltage-in current-out machine model, based in a three-phase, 5-hp, squirrel cage induction motor is evaluated in [64], as shown in Figure 1.22. The model considers magnetic saturation effects and the experimentally determined machine's leakage and main flux saturation characteristics and will give current references based on the voltage at the machine terminals. As SMPA, the same two-level converter-based power amplifier as in [62]. One of the main focus of the study [64], [75] is to validate the proposed model based on the leakage reactance parameters and saturation effects as the stator and rotor leakage flux paths, so the system is simplified by a direct connection with the grid, without a Variable Frequency Drive (VFD) or IUT, as in [19]. The direct connection with the grid enables an accurate dynamic performance evaluation of the model and motor during Direct On-Line (DOL) start-up and loading conditions.

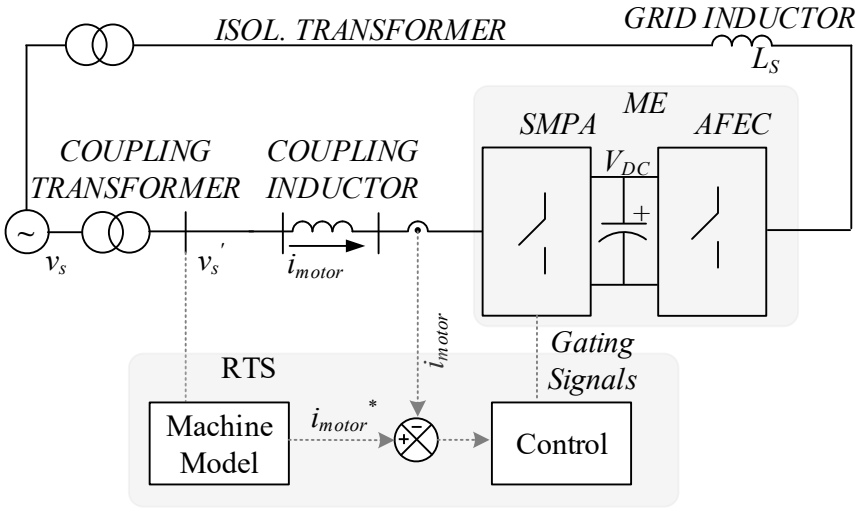


Figure 1.22 – Induction machine emulation with direct connection to the grid [64]

The SMPA in [64], acting as ME is operated with a switching frequency of approximately 15 kHz with a RTS sampling time of 40 μs. The current controller of the SMPA achieves a bandwidth of around 2 kHz, which is based on the Proportional-Resonant (PR) controller used to regulate the current in grid-tied systems (showing the benefit of eliminating the steady state error

when regulating sinusoidal waveforms). The experimental results show a relatively good tracking performance of the model when given a reference and compared with the actual motor, but the presence of the switching harmonics reduces the accuracy of the overall system, especially at lower modulation indexes. In addition, the presence of 5^{th} and 7^{th} harmonics of the fundamental modulation signal are present due to the VSCs dead-time.

Considering the constraints found in previous studies regarding the inefficient switching harmonics attenuation, high implementation complexity or cost associated with LPAs, a new application of an HPA for ME and a novel current control strategy is proposed further on this study, favoring the enrichment of the body of knowledge related to machine emulation. One of the objectives is to present an induction motor ME setup, which combines the low cost and power capacities of a two-level converter-based voltage source inverter, as SMPA solution, with the high bandwidth of an LPA (small as possible). The SMPA will provide the bulk portion of the current while the LPA will provide only the compensation for switching harmonics and assist partially on transient conditions. Including the LPA in parallel, and consequently improving the overall system bandwidth and the quality of the signal output, this flexibility is even higher because it can emulate high-fidelity voltage-in current-out models with precision. In addition, the study also proposes and validates a novel control strategy, based on using the measured coupling inductor current as a reference for the SMPA. Lastly, it evaluates different conditions or ratios between the bandwidths of the LPA and SMPA while seeking an LPA current rating reduction. The proposed system will be connected directly to the grid for a DOL start-up, using just an autotransformer, but it can be connected to prototype IUTs or commercial VFDs for further validation. Commercials VFDs (below 20 kVA) present maximum output frequencies (which corresponds to the effective power bandwidth at their outputs) of 300 [84], 400 [85] and 500 Hz [86]. The overall HPA current control bandwidth, which corresponds to the control ability of the system, must have a minimum crossover frequency five times higher than the fastest VFD drive, so above or equal to 2.5kHz.

1.5. Frequency, Amplitude and Phase Angle Detection for Single Phase Systems

Amplitude, Phase Angle and Frequency detection (APAF) are imperative for Power Hardware-in-the-Loop (PHIL), where an external signal from a controller is given to a Power Amplifier (PA) [29], [87]–[91] to test systems as a whole or just any parts or combinations of it, such as controllers, actuators, motors, drives or loads. The challenge in this case is identifying the

characteristics of the given external reference signal, especially when the PA is built using Switched Mode Power Amplifiers (SMPAs) or hybrid solutions with Linear Power Amplifiers (LPAs). The reference signals given to these PAs must be in accordance with their capabilities and the APAF detection must match those limits, which can go up to tens of kHz [87], [90]–[92].

A second and important application of APAF is for power electronics converters connected to the utility grid. The synchronization of their gating signals and corresponding output voltage with the grid is critical for an effective control of the power flow [93]–[95]. Recently this topic has received a lot of attention due to the ongoing increase in deployment of renewable energy sources, such as photovoltaic (PV) and wind energy connected to all the levels of the grid. The power converters' APAF must be able to identify voltage and frequency levels in steady state and dynamic conditions, like voltage sags, phase inversion and frequency steps/variation [96]–[99]. Another use for the APAF detection is for synchronizing power converters used for: active filtering next to non-linear loads, dynamic voltage restorers, Flexible AC Transmission System (FACTS) controllers and Uninterruptible Power Supplies (UPSs) [95].

The challenge with HPA and PHIL systems is that they can be requested to output signals in a wide range of amplitudes and frequencies, not only in steady state but also in dynamic scenarios. An example is the acceleration of a car, in which the signal from the inverter to the motor will increase the frequency overtime. Another case is the emulation of electrical machines during start-up, such as the DOL [64], load steps [19], in which both frequency and amplitude can be changed quite abruptly, such as for direct on-line start-ups of an induction machine.

On HPAs with the multilevel SMPA controlled to produce staircase waveforms, the APAF must be fast enough to update the reference levels, otherwise more power is requested from the LPA. The LPA is a sensitive element on the HPA in terms of losses and can contribute to up to 75% of the HPA losses, but the most critical in this situation is the possibility of saturating the LPA and the loss of significant quality on the output signal of the HPA. The APAF also must be quick enough for other applications, such as digitally controlled staircase converters (inverters) that operate with variable output.

In the literature, most systems are designed for a single and known frequency, usually the grid's frequency. However, a wider range of frequencies is necessary for the applications mentioned above. For grid-connected applications, the converter must be able to identify frequencies around 50 or 60 Hz. According to IEEE Standard 1547-2018 [100] "*Interconnection*

and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces", the power converter must be able to inject power into a 60 Hz grid, but the converter must operate differently according to the grid frequency within the limits of 56.5 and 62.0 Hz. If the grid frequency is out of those limits, proper measures must be taken to disconnect the power converter and the renewable sources from the grid. This means that the APAF detection must work outside those limits to ensure the coverage throughout all the necessary range. In terms of voltage, several conditions in [100] are set between ranges from 1.2 and 0.45 pu of the grid voltage and the detection techniques should be able to identify precise amplitudes beyond those limits. As an example, for 120 Vac, the limits are 144 and 54 Vac. The homogeneous attributes of these three growing power electronics applications is that they all require precise techniques to identify the signal amplitude, the phase angle and frequency. This assures the synchronization of the renewable energy, power converter interfaces and high-bandwidth with precise outputs for PHIL.

As a part of the APAF, the phase angle determination is referred to as Phase-Locked Loop (PLL) and several techniques are available for detecting voltage amplitude, RMS values, phase angle and frequency. They can be categorized into Synchronous Reference Frame (SRF-PLL) systems [95], [101]–[103] and adaptive or hybrid systems [96], [104]–[106], [106], [107]. This study focuses on the single-phase PLL, which is more complex because an additional Orthogonal Signal Generator (OSG) is required to identify the phase angle, prior to the amplitude detection. The phase angle and amplitude are the most important parameters and they alone can be used for the diverse applications listed above. Frequency identification, differently from the phase angle identification, is not mandatory for the synchronization of power converters with the grid, but they can offer parameters for supervision and demonstration, i.e. a Graphic User Interface (GUI).

1.5.1.1. Conventional APAF Detection Topologies

For three-phase systems, the OSG is based on Clark's Transformation (*abc*-αβ), which will naturally output the orthogonal (α and β) signals. With these signals and the inverse tangent trigonometric function, it is possible to determine the estimated phase angle, θ, as in (1.4). Detailed evaluations of three-phase and single-phase APAF (for a single and known frequency) detection are presented in references [106], [108] and [94], [95], respectively.

$$\theta = arctan\frac{v_\alpha}{v_\beta} \tag{1.4}$$

As mentioned before, single-phase APAF detection requires unconventional implementations for the OSG. As single-phase systems do not have the additional two phases to apply Clark's transformation, alternative solutions for the OSG must be used [102], [105], [107]. The main problem and disadvantage is that most of them require a fixed and previously known frequency. Figure 1.23 shows a conventional Single-Phase SRF-PLL with the OSG at the input of the system. The symbol || or |•| represents the operation with the absolute value. For the purpose of this study, it is defined that the term central frequency, ω_{cf}, refers to the main or fundamental frequency for those topologies based on fixed or synchronous reference. The central frequency also allows positive and negative variance around it. For example, most topologies are designed for a ω_{cf} of 314.16 rad/s (f_{cf} of 50 Hz), but will allow the parameter identification for the range of 295.31 to 326.72 rad/s (47 to 52 Hz), with an acceptable range of error [103], [109].

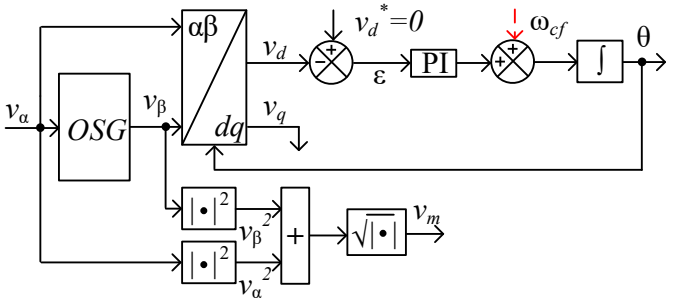


Figure 1.23 – Conventional single-phase Phase-Locked Loop (PLL) with Orthogonal Signal Generation (OSG).

The most common, and simple, OSG is the Second Order Generalized Integrator (SOGI), as presented in Figure 1.24 [102], [110]. The system generates an orthogonal signal, v_β, from an input signal, v_α, with the same amplitude and frequency. It works due to the dual integral blocks, denoted by the $\int$ symbol. The central frequency, ω_{cf}, is used to multiply the intermediate signals, which is the main constraint of the system. The gain K_1 has to be determined and it will affect the response of the system in terms of gain, phase, settling time and ringing. Details on determining K_1 are presented in reference [88] and experimental results evaluating different gains are presented in Chapter 4.

A variation from traditional SOGI-PLL is a system that uses a time delay to generate the orthogonal signal, v_β. Figure 1.25 shows the topology of the single-phase transfer delay-based PLL (TD-PLL) [103]. As illustrated, the orthogonal signal is generated by delaying the original single-

phase signal by T/4, where T is the inverse of the central frequency, ω_{cf}. As disadvantage, the topology presents high sensitivity to the grid frequency variations, because the phase shift caused by the transfer delay will not be exactly 90° in the presence of frequency changes, steps or variations.

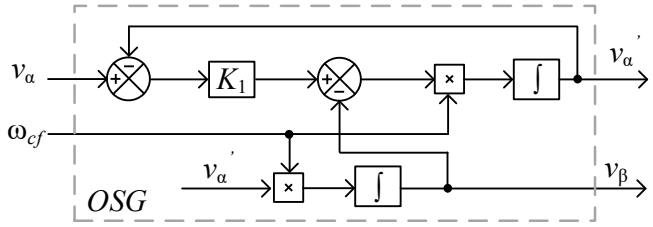


Figure 1.24 – Second Order Generalized Integrator (SOGI) as OSG.

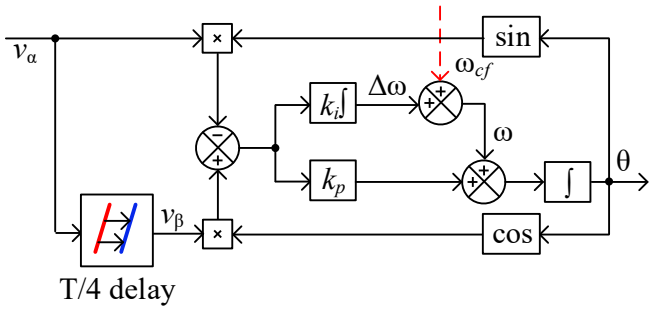


Figure 1.25 – Schematic of the TD-PLL [103]

Presented in [105], [111] and experimentally validated in [96], [105], [111] the Adaptive Notch Filter (ANF) and Amplitude Adaptive Notch filter (AANF), shown in Figure 1.26, offer a sound strategy for single-phase parameter identification for signals with considerable amplitude variation. In reference [111], the system is tested for steps on amplitude from 0.5 to 1 pu and 1 to 1.5 pu, and the frequency step is minimal, from 50 to 51 Hz, since the focus of the study is on the adaptive amplitude identification. Both topologies require the input of ω_{cf} as the initial condition for one of the central integrators, placing this topology within the SRF-PLL category. In [105], the ANF is experimentally validated for a very small amplitude (1 to 1.1 pu) and frequency (60 to 61 Hz) variation, but it is a solid study describing how the choice of the gains K_2 and K_3 can impact the speed of the detection.

In [106], [108] a valuable study on frequency identification that updates the necessary blocks of the system in order to improve the quality of the signal identification is presented, as an adaptive approach. The systems under study are three-phase, where it is easier to get the orthogonal signals,

but the efficiency of the method is validated with highly distorted and unbalanced input with a wide variation on the amplitude. The only weakness of the study is that the frequency variation is evaluated only within the range of 50–59 Hz [106].

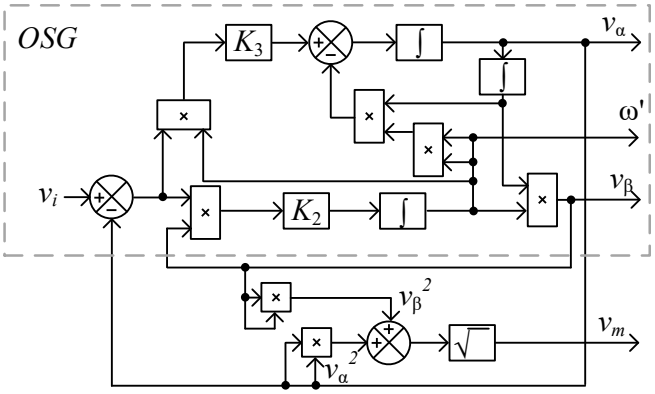


Figure 1.26 - Single phase PLL with Adaptive Notch Filter (ANF) [105]

As one of the most recent areas of development, the implementation of Kalman Filters on PLL has received significant attention [112], [113]. Kalman Filters are used after the orthogonal signal is generated, no matter if the system is single or three-phase. In [112], the study compares the performance of two and three-state prediction models with conventional SRF-PLLs. The study does not cover significant frequency steps, only a step from 50 to 55 Hz and a frequency ramp (+40 Hz/s) from 50 to 53 Hz. The utilization of Kalman filters, after the OSG, is a viable alternative and they will be further implemented on the proposed systems.

Two topologies under the SRF-PLL category are shown in Figure 1.27(a) and both are recognized for their simplicity and accurate results. The first one is the inverse Park's PLL [114], [115], in which the orthogonal signal v_β is generated by the inverse Park's transformation of the filtered signals from v_d and v_q. The filters are set to the same cut frequency and they determine the APAF dynamic speed and accuracy. In Figure 1.27(b), the Enhanced-PLL (EPLL) is presented [116], [117]. Similarly to Park's PLL, EPLL also outputs the phase angle, which is reintroduced on algorithm, on the first to synchronize the *dq*-αß transformation and on the second to generate internal error signals. For both systems the integral and proportional compensator gains, k_i and k_p are designed to achieve the expected dynamic behavior and disturbance rejection. The main disadvantage of both systems is the constraint of the central frequency, ω_{cf}, and they present accurate results only in a small range (approximately ±10%) around to ω_{cf}.

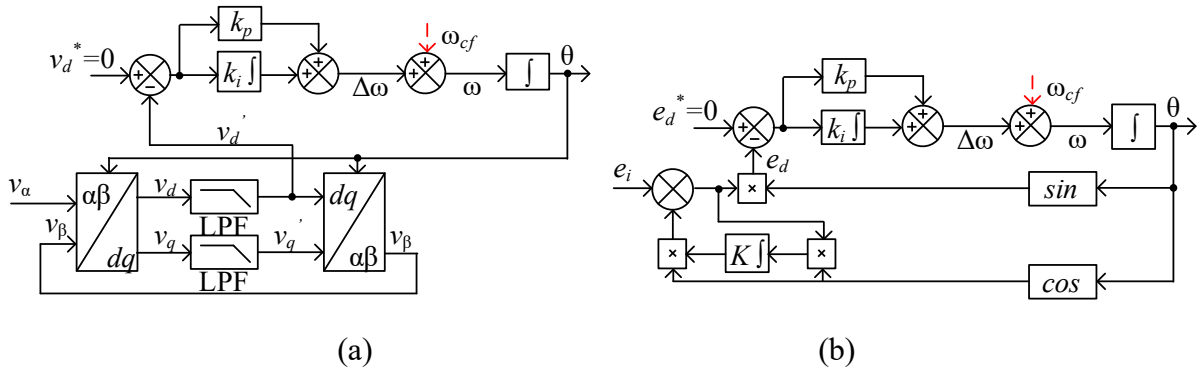


Figure 1.27 - (a) Inverse Park's PLL; (b) enhanced-PLL.

An alternative for the SP-PLL and traditional SOGI as OSG is presented in Figure 1.28. The study presented in [107] can be defined as a frequency-independent topology, considering there is no input of ω_{cf}, but another constraint is introduced on the system, which is related to a compensation, C_1 (1.5), of the gains of the derivative based (DB or $DB_{TF}(d/dt)$), k_d, and integral based (IB or $IB_{TF}(\int)$), k_i, applied to the input signal. The orthogonal signal v_β is given by Equation (1.6). The function *sign* or *signal* is used to extract only the signal (positive or negative) of its input. Even though the system presents the above-mentioned limitation there are key advantages proposed in the topology. The main disadvantage is the lack of equations showing what are the frequency detection limitations or operating frequency range (maximum and minimum values that can be detected with sufficient accuracy). In terms of frequency variation, the results for the amplitude detection are evaluated for a steady ω_{cf} of 314.16 rad/s (f_{cf} of 50 Hz), and the phase-angle detection for steps between 295.31 to 326.72 rad/s (47 to 52 Hz).

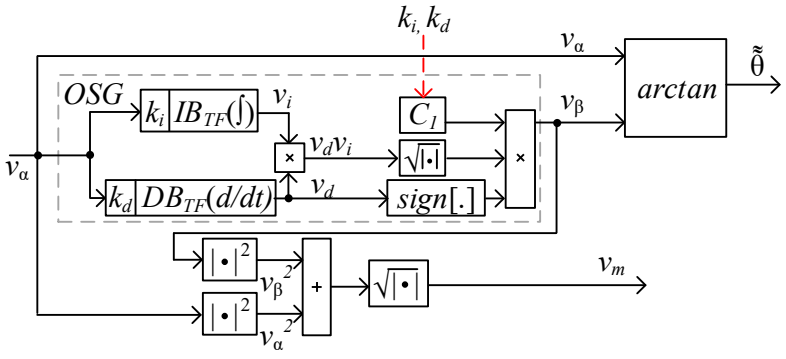


Figure 1.28 – Derivative-integral frequency independent OSG [107]

If one can ensure that the multiplication of k_d and k_i is unitary, the dependency of the variable responsible for the k_d and k_i compensation, C_1, is removed. This is the main idea for the proposed APAF circuit described further in this study. What is more, the detailed and instructive design procedure is presented in Chapter 4.

$$C_1 = \frac{1}{\sqrt{|k_d k_i|}} \tag{1.5}$$

$$v_\beta = C_1\sqrt{|v_d v_i|}\text{sign}[v_d] = \frac{C_1\sqrt{|v_d v_i|}\text{sign}[v_d]}{\sqrt{|k_d k_i|}} \tag{1.6}$$

The literature focuses heavily on the central frequency identification [118], for grid-connected systems under distorted conditions (mostly with the impact of noise, low and high order harmonics) [119]–[122], but there is a lack of studies in which APAF detection could be performed in significant wide ranges, especially for single-phase systems. For grid-connected converters, the phase-angle and amplitude identification must work with small variations in frequency (0.95 and 1.03 pu) and moderate variations in amplitude (0.45 to 1.2 pu). Now, for PHIL and HPA applications, the APAF must be able to identify phase angles varying within frequencies from dc to 1000 Hz and amplitudes from 0 to rated voltages (230 Vac i.e.) [29], [89]. Not only that, the dynamics related to these applications are more substantial. Therefore, this research work proposes a new APAF circuit capable of performing with wide ranges of frequencies and voltage magnitudes while the input signals vary with fast dynamics.

1.6. The Scope of the Research Work

Given the unbalanced power contribution by each cell of a staircase-controlled CHBM in a series connected HPA, this study proposes a novel modulation technique called Split-Voltage First-In-First-Out (SV-FIFO). The objective is to improve the power balance (while switching the cells at the same frequency as the reference) without changing the SMPA's output voltage (*staircase)* by controlling the cascaded individual outputs, for rated and non-rated conditions. All analytical equations for the power demanded by the H-bridges and a basic design procedure for a series type HPA are presented. A suitable control scheme for the series HPA operating with SV-FIFO is devised. It employs a digital open loop controller for the CHBM converter (SMPA) and an analog closed loop controller for the LPA, with power isolation between the power and control

signals. A 1 kVA single-phase HPA with a six-cell CHBM converter and a commercial LPA was built in the laboratory and used for extensive testing and performance verification under steady state and transient conditions. SV-FIFO focuses on improving the power balance for resistive load, while an additional modulation technique called Independent Load Balancing (ILB) modulation is proposed for improving the balance of the cells for other linear loads, such inductive or capacitive loads.

Considering HPAs with parallel connected LPA and SMPA, this study proposes a new parallel type HPA for ME systems using voltage-in current-out machine models. It is a compromise solution where the LPA and its high BW allows fast dynamic responses, while the SMPA provides the bulk of the power of the ME system. In order to minimize the cost of the HPA, it is essential to minimize the current rating of the LPA. This is ensured by using the control technique proposed in this study, where both the LPA and the SMPA operate in parallel with current control loops. The reference current of the LPA is that of the ME system, computed by the RTS, while the one for the SMPA is the LPA current. The SMPA is controlled with a lower BW current loop in order to take over the current from the LPA, following a short transient. In steady state, the LPA inherently provides active power filtering for the SMPA, reducing the switching Harmonic Distortion (HD) of the ME system. A complete design procedure for the control scheme of the HPA is presented and illustrated for the emulation of a direct on-line start-up of an Induction Machine (IM). Experimental results are shown to validate the proposed control scheme for the parallel HPA in ME systems. Besides, the impact of the bandwidths of the control loops of the LPA and SMPA and the switching frequency of the SMPA, on the accuracy of the ME system and on the current requirement of the LPA are highlighted.

The implementation of the proposed SV-FIFO for the staircase controlled CHBM converters in series type HPAs for ME systems requires single-phase APAFs with wide ranges of frequency and amplitude as well as fast dynamic response. A simple version of an APAF with the above-mentioned requirements was not available in the literature, which led to the development of two techniques. The first presents an improvement on the OSG topology presented in [107], for a single-phase amplitude, phase angle detection, which is frequency independent (for a known range) and self-reliant in terms of gains and initial state settings. It will be benchmarked against well-known topologies and evaluate the frequency detection block from the phase angle with traditional derivative action and a modern Kalman filter solution. The second is based on a hybrid

construction of an algorithm part (developed in C) followed by a traditional SOGI SP-PLL, composed of adders, multipliers, gains and square root blocks.

1.7. Outline of the Thesis

Chapter 2 presents the issue of unbalanced output power among cells in Cascaded H-Bridge Multilevel (CHBM) converters with conventional staircase modulation techniques under low modulation signals. The application of CHBM is in series with Linear Power Amplifier (LPA) to build high voltage/frequency Hybrid Power Amplifiers (HPAs). A modulation technique and its on-line implementation called Split-Voltage First-in First-out (SV-FIFO) are presented. Experimental results for a series type HPA with a six-cell CHBM converter and a commercial LPA are provided to validate the design procedure of the HPA, demonstrate the enhanced (active) power balance of SV-FIFO and the effectiveness of the proposed control scheme for the HPA under transient and steady state conditions. An additional technique called Independent Load Balancing (ILB) modulation is proposed, which improves the power balance of the cells for non-resistive loads.

Chapter 3 proposes a Machine Emulation (ME) based on a Hybrid Power Amplifier (HPA), with parallel LPA and SMPA. A new current control scheme for the HPA, suitable for voltage-in current-out machine models, is proposed to reduce the required current rating, and thus the cost, of the LPA. A design procedure for the control scheme of the HPA is presented and illustrated for the emulation of a direct on-line start-up of an Induction Machine (IM). Simulation results evaluate and compare systems built exclusively with SMPA or LPA for ME. Experimental results are shown to validate the proposed control scheme for the parallel HPA in ME systems. Besides, the impact of the bandwidths of the control loops of the LPA and SMPA and the switching frequency of the SMPA, on the accuracy of the ME system and on the current requirement of the LPA are highlighted.

Chapter 4 presents the design of two APAF techniques and circuits. This first one presents an Orthogonal Signal Generator (OSG) based on integral and derivative actions, while the second one based on the input's zero-crossing detection. The performance of the APAF techniques for single-phase signals with wide range amplitude and frequency are experimentally validated under steady state and dynamic conditions.

Chapter 5 presents the main conclusions from this research work and suggests prospective research work in continuation of the main topics.

1.8. List of Publications

Several papers could be published during and as a result of the research of the doctoral studies. They are summarized here and classified as journal or conference publications,

1.8.1. Journal Publications (most recent first)

1. L. M. Kunzler, L. A. C. Lopes, K. S. Amitkumar, P. Pillay, J. Belanger, "Parallel Hybrid Linear-Switched Power Amplifier and Control Strategy for Machine Emulation". International Journal of Electrical Power & Energy Systems. Volume 131, 2021,107063, doi: 10.1016/j.ijepes.2021.107063.
2. L. M. Kunzler and Luiz A. C. Lopes, “Wide Frequency Band Single-Phase Amplitude and Phase Angle Detection Based on Integral and Derivative Actions”. Electronics, 9, 1578, 2020. doi: 10.3390/electronics9101578
3. L. M. Kunzler and Luiz A. C. Lopes, “A novel algorithm for increased power balance in cascaded H-bridge multilevel cells in a hybrid power amplifier”. Electrical Engineering, 2020. doi: 10.1007/s00202-020-01102-7

1.8.2. Conference Publications (most recent first)

4. L. M. Kunzler and L. A. C. Lopes, "Algorithm for Improving Power Balance for Cascaded H-Bridge Multilevel under Staircase Modulation for Linear Loads," IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal, 2019, pp. 6066-6071, doi: 10.1109/IECON.2019.8927489.
5. L. M. Kunzler and L. A. C. Lopes, "Hybrid Single Phase Wide Range Amplitude and Frequency Detection with Fast Reference Tracking," 2019 IEEE 28th International Symposium on Industrial Electronics (ISIE), Vancouver, BC, Canada, 2019, pp. 878-883, doi: 10.1109/ISIE.2019.8781515.
6. L. M. Kunzler and L. A. C. Lopes, "Power balance technique for cascaded H-bridge multilevel cells in a hybrid power amplifier with wide output voltage range," 2018 IEEE

International Conference on Industrial Technology (ICIT), Lyon, 2018, pp. 800-805, doi: 10.1109/ICIT.2018.8352280.

1.9. Conclusion

This chapter provides a detailed literature review on several topics related to making Power Hardware-In-the-Loop (PHIL), for Machine Emulation (ME) more affordable and better performing. It was noticed that there are a number of improvements that can be made on the Power Amplifier (PA) part of the ME system. The main idea is to associate high performance, but costly, Linear Power Amplifiers (LPAs) with high power density, but harmonic generating, Switch-Mode Power Amplifiers (SMPA), in Hybrid Power Amplifiers (HPAs) that offer a compromise solution with desirable features of LPAs and SMPAs.

For high voltage applications, a series-type HPA where the SMPA consists of a Cascaded H-Bridge Multilevel (CHBM) converter controlled with staircase modulation to minimize the switching losses and enable operation with high frequency output voltages is considered. The issue of unbalance, in power flow, stress and potentially lifetime, among H-Bridges, was identified when the CHBM converter operates with low modulation indices.

For lower voltage ranges, the cost of the LPAs is highly influenced by their current ratings. To mitigate this issue, parallel-type HPAs are a good option. Considering that many machine models are of the voltage-in current-out model, a suitable current control scheme for the parallel-type HPA is required for ME.

The magnitude and frequency of the reference signals used for ME tend to vary significantly. This requires the use of wide range Amplitude Phase Angle and Frequency (APAF) detection. This is not common in the literature, mostly for single-phase systems. The majority of the APAF systems concern highly distorted signals with frequencies and amplitudes varying within relatively narrow ranges.

2. STUDY OF A SERIES HPA

2.1. Introduction

This chapter concerns the issue of unbalanced output power among cells in Cascaded H-Bridge Multilevel (CHBM) converters with conventional staircase modulation techniques under low modulation signals. This is a common condition in high voltage/frequency Hybrid Power Amplifiers (HPAs) consisting of a CHBM converter in series with a Linear Power Amplifier (LPA). This chapter discusses and extends the principle of traditional switching techniques, called First-In First-Out (FIFO) and First-In Last-Out (FILO) and proposes a novel switching technique called Split Voltage First-In First-Out (SV-FIFO) for a wide output voltage variation, especially for lower output voltages. Mathematical equations are derived for a quantitative comparison of the conventional and proposed methods, with the statistical analyses for various operating conditions.

Differently from conventional techniques, SV-FIFO, takes into consideration the magnitude and frequency of the reference voltage to generate the gating signals of the CHBM converter. A design procedure for a series type HPA and a method for generating on-line the gating signals of the CHBM converter, with SV-FIFO are evaluated. Experimental results for a series type HPA with a six-cell CHBM converter and a commercial LPA are provided to validate the design procedure of the HPA, demonstrate the enhanced (active) power balance of SV-FIFO and the effectiveness of the proposed control scheme for the HPA under transient and steady state conditions.

Lastly, a new technique for improving the power balance, not only for resistive loads, but also for inductive and capacitive loads, among all the cells is proposed. It is based on the selection of all possible combinations of the switching angles, generated by the Nearest Level of Control (NLC) technique. By improving the power balance, the cells can be designed in a uniform way, requiring smaller DC supplies and making it possible to use multi-output DC power supplies. This new modulation technique will be detailed and simulations results will be presented to validate the technique.

2.2. Split Voltage First-In First-Out Switching Technique and Proposed Algorithm

As the main contribution of this study, a splitting technique, SV-FIFO, will be used for lower reference voltages to ensure a better power distribution between the cells. This technique is constructed on a series of binary decisions based on the number of cells in the system, amplitude

of the reference and DC voltage levels. The best way to represent it is graphically, using a process flowchart, presented in Figure 2.1. This technique can be implemented with digital processors with the flexibility to make changes, corrections and adaptations since the base of it would be coded. The technique is conceived for a CHBM system that can be built from three to ten cells. However, once the algorithm is understood, it is possible to expand it for any number of cells.

The basis of the proposed technique relies on comparing the total number of cells of the system, N_T, which is a constructive constraint of the system, and how many levels, given by (1.1), the reference signal reaches, N_L. In addition, as input to the system, all angles found in (1.2) are supplied to the algorithm. New variables are created representing the turn on, $\alpha_{n.on}$, turn off, $\alpha_{n.off}$, of each cell (n). In addition, the variable Δ will be used to quantify the total required conducting interval for each level on the output signal.

The algorithm consists of a main routine, shown in Figure 2.1. Some routines repeat themselves during the main routine, and they are shown in Figure 2.2.

The system relies on four main aspects:

(i) the numeric difference between N_T and N_L;

(ii) if N_T is even or odd;

(iii) if N_T is divisible by 2, 3, 4 or 5;

(iv) if the surrounding integral numbers (-4 to +4) around N_T are divisible by 2, 3, 4 or 5.

Figure 2.3 shows some waveforms to illustrate the generation of the staircase voltage waveforms using the NLC technique for a three-cell CHBM converter. Two reference/output voltage waveforms are shown on the top screen with peak values of $3.2V_{DC}$, in blue, and $1.8V_{DC}$, in red. The first intersects three "comparison" voltage levels (1.1), producing a staircase of three non-zero positive levels, while the second only intersects two voltage levels. The impact of the number of voltage levels of a staircase waveform on the power unbalance among cells of a CHBM converter is discussed in the following subsection.

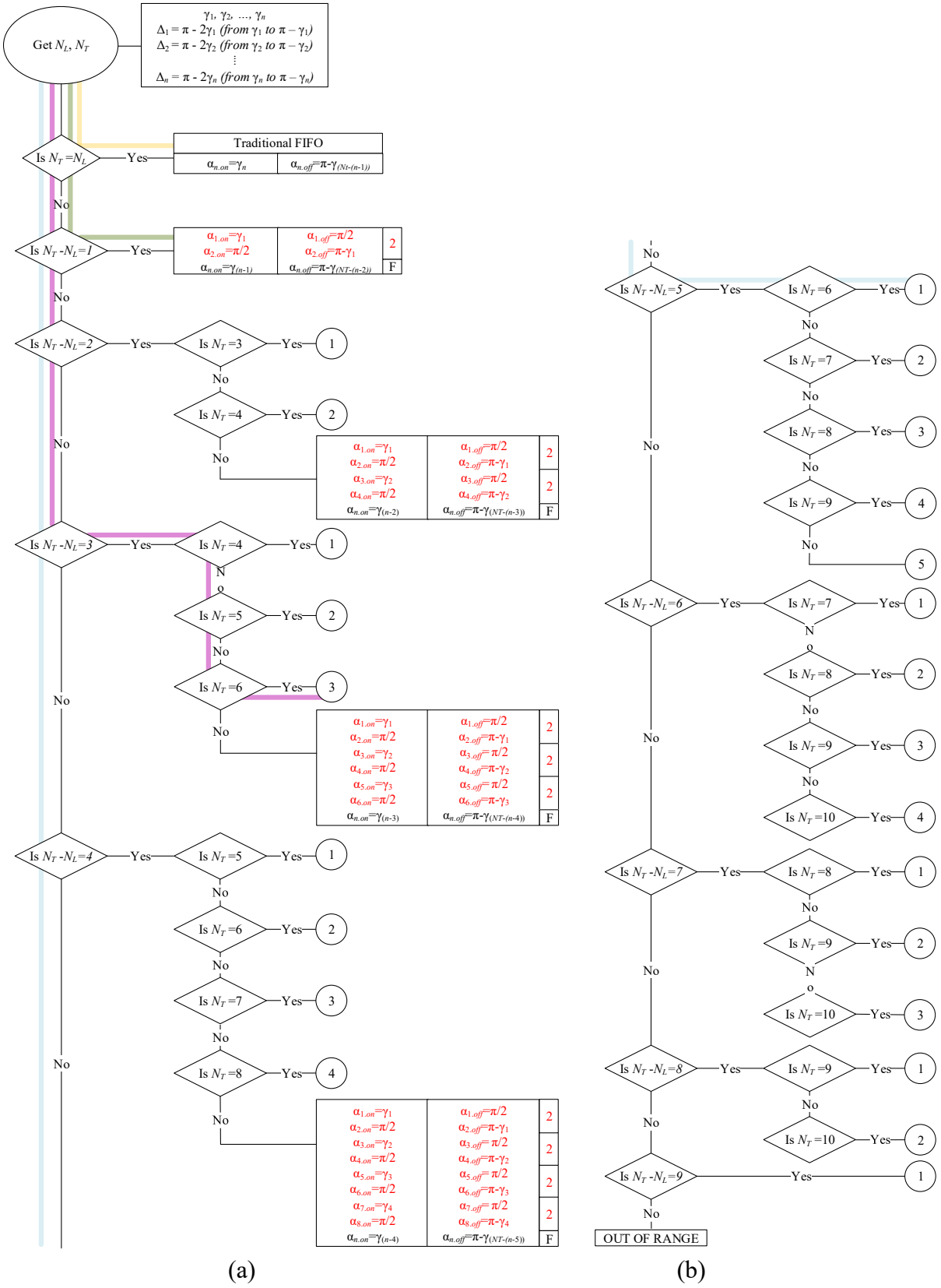


Figure 2.1 – Main routine of the SV-FIFO algorithm (a) first part (b) second part

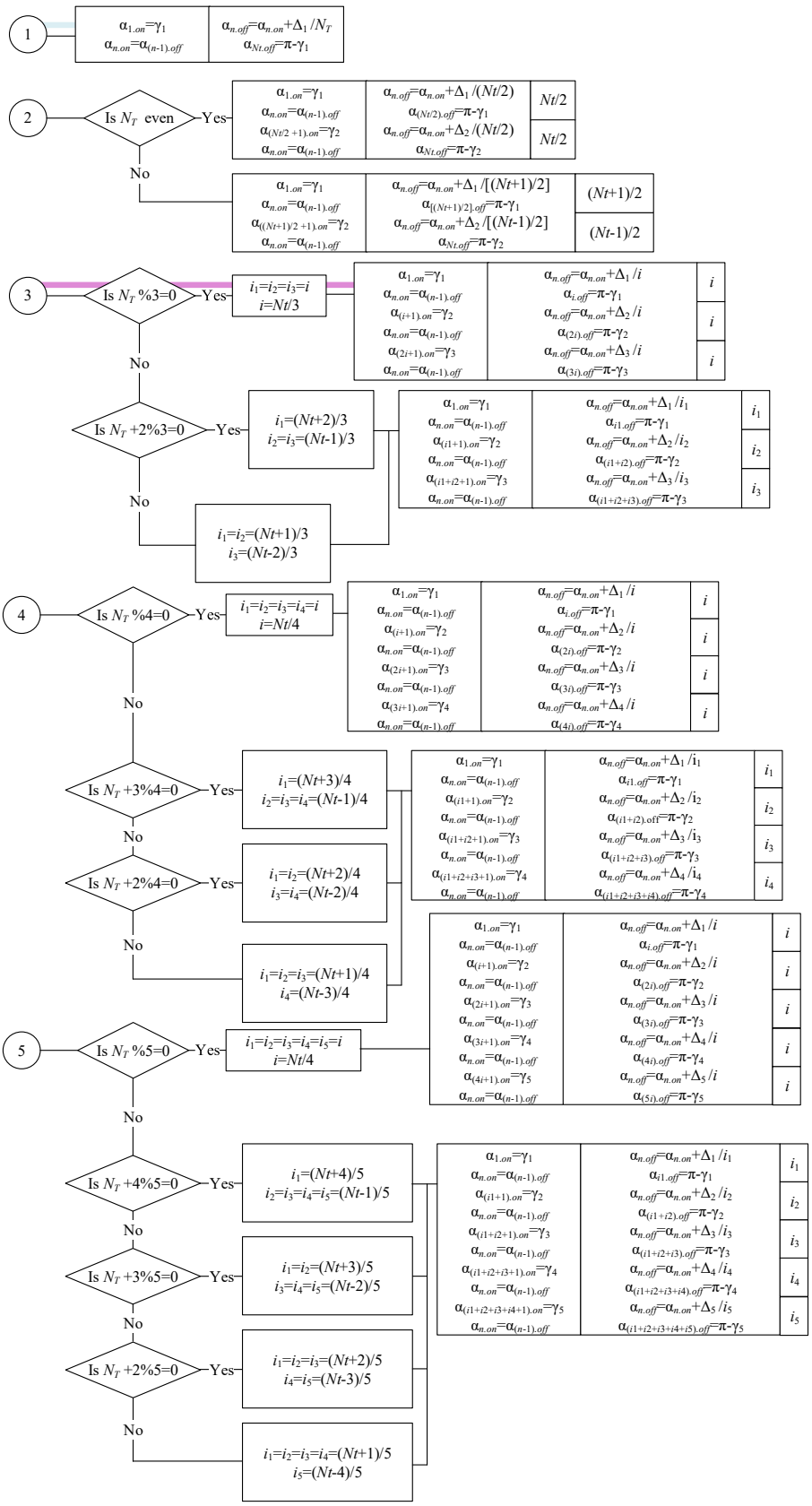


Figure 2.2 – Multi-occurrence patterns to be used on the main routine

2.1. Basic Design Approach for a Series Type HPA

The waveforms presented in the third row of Figure 2.3 concern the new modulation technique called Split-Voltage First-In First-Out (SV-FIFO). There, one sees that it manages to yield output voltage waveforms for the H-bridges with comparable pulse widths, leading to an improvement on the balance in the power supplied by them within one line cycle, considering a unity power factor load.

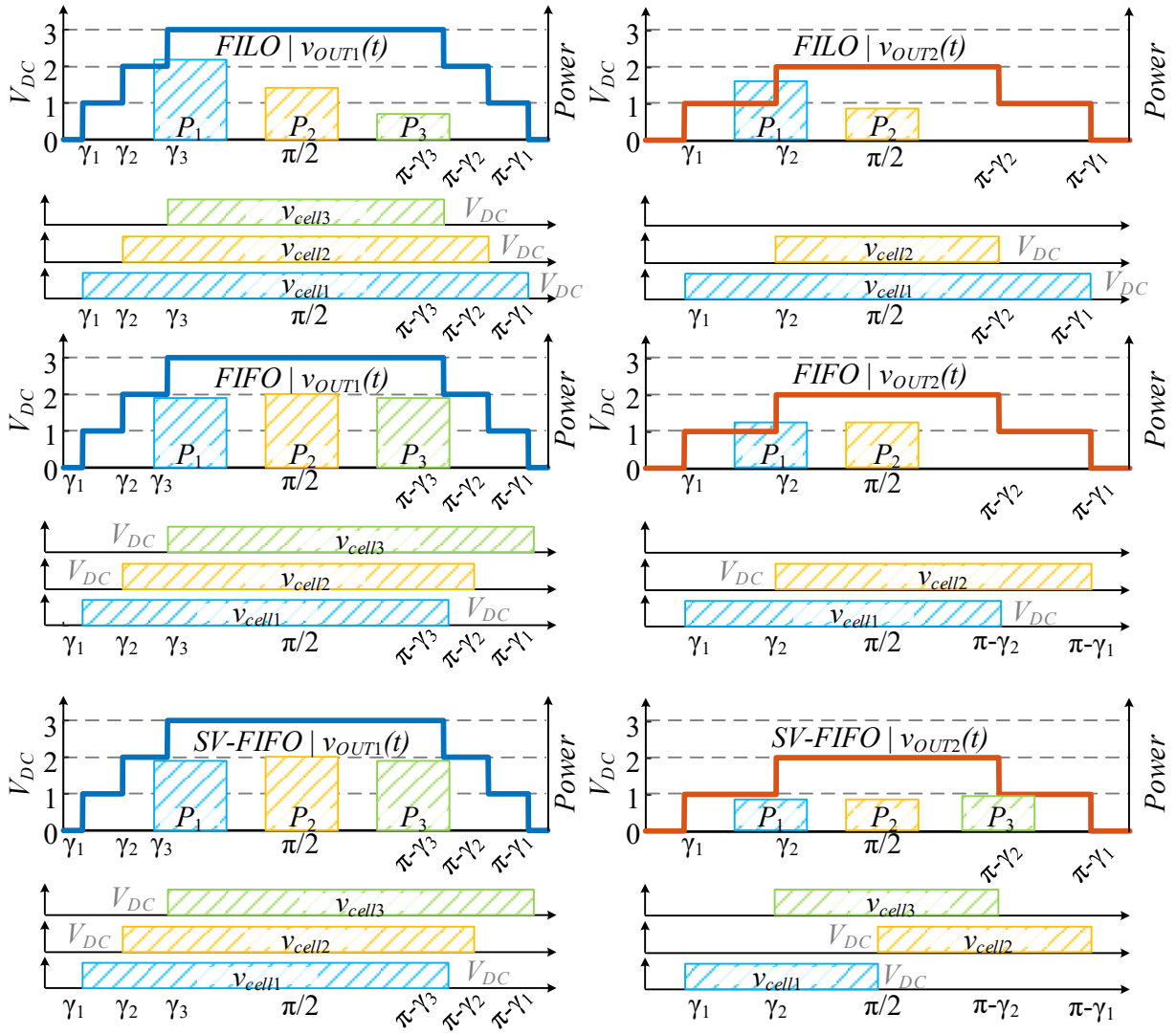


Figure 2.3 – Output voltages of the SMPA, H-bridge cells and their power contributions considering a high ($3.2V_{DC}$ with v_{out1}) and medium ($1.8V_{DC}$ with v_{out2}) reference voltages with FILO (top) FIFO (middle) and SV-FIFO (bottom).

2.1.1. Equations for Power per H-Bridge and its Standard Deviation

The power demanded by each cell (n = 1 to Nt) of a CHBM converter operating with a staircase voltage and a sinusoidal current can be computed as presented in (2.1). The equation is valid for FILO, FIFO and SV-FIFO and for any number of voltage levels.

$$P_{out\_cell,n} = \frac{\sqrt{2}}{\pi} V_{DC}\, I_{out}\left[cos(\alpha_{n.on} + \theta) - cos\left(\pi - \alpha_{n.off} + \theta\right)\right] \tag{2.1}$$

where V_{DC} is the DC bus voltage,

I_{out} is the RMS value of the load current,

θ is the phase angle between $v_{ref}(t)$ and $i_{out}(t)$,

$\alpha_{n.on} = \gamma_n$ for FILO and FIFO

$\alpha_{n.off} = \pi - \gamma_n$ for FILO

$\alpha_{n.off} = \pi - \gamma_{(Nt-(n-1))}$ for FILO

$\alpha_{n.on}$ and $\alpha_{n.off}$ for SV-FIFO

γ_n is calculated from (1.2) for a given v_{ref}.

Figure 2.4 shows the variation of the standard deviation (*SDEV*) in the average power demanded by the cells of a CHBM converter with the magnitude of the reference output voltage, for FILO, FIFO and SV-FIFO for a resistive load. The plot was obtained for Nt = 6, V_{DC} = 48 V and 25 V $\leq \hat{v}_{ref} \leq$ 311 V (which are some of the parameters used for experimental validation in Section 2.3). For generating the plot, a 5 V step in $\hat{v}_{ref}$ was used, in that voltage range.

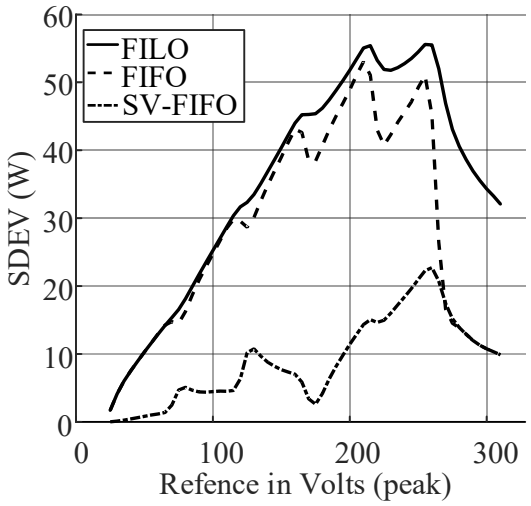


Figure 2.4 – Trend lines for the standard variation with FILO, FIFO and SV-FIFO

Figure 2.4 shows that the SDEV in the power demanded by each H-bridge cell with SV-FIFO is less than half that for FILO and FIFO, except for $\hat{v}_{ref} \geq 264$ V, where according to (1.1) and (1.3), all 6 H-bridge cells are active. There, FIFO and SV-FIFO are equivalent.

2.1.2. On-Line Operation and Proposed HPA Control Scheme

A few studies concerning HPAs with the CHBM converter supplying a staircase waveform and in series with an LPA have been reported in the literature [35], [58]. Both employed the same LPA, a low-cost chip based Apex MPU 111A [123], which has a very high open-loop gain. The control scheme of the LPA was of the feed-forward type as shown in Figure 2.5, the same traditionally used for the control of signal (low power and voltage) amplifiers. The closed loop voltage gain of the LPA is set to a fixed value defined by the ratio of resistors R_2 and R_1. The reference signal of the HPA (v_{ref}^*) is inverted by OP1 (AD8033), a voltage feedback amplifier with Field Effect Transistors (FET) input, low noise and high speed (80 MHz bandwidth and 80 V/μs slew rate). The reference signal for the LPA, $v_{LPA}^*(t)$, is generated by the difference between the inverted HPA reference voltage, $v_{ref}^*(t)$, and the SMPA output, $v_{SMPA}(t)$. Although this system is very fast, reaching bandwidths of around 500 kHz, there is no isolation or separation between power and signal levels.

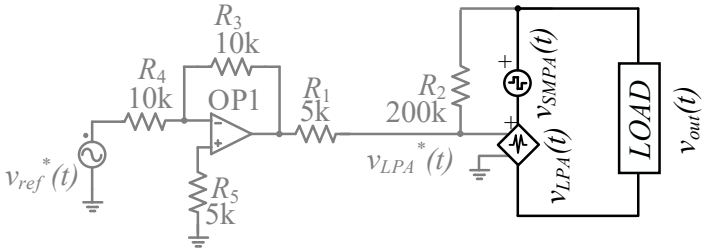


Figure 2.5 – Feed-forward LPA control [58]

In this study, the selected LPA is a complete commercial solution, the AE Techron LVC5050 [124]. It presents a low but constant input-to-output gain, which can be set from 0 to 20, controlled by a knob and a bandwidth of about 20 kHz. In such a case, the scheme shown in Figure 2.5 cannot be used. An alternative solution is shown in Figure 2.6, which also includes isolation between power and signal levels. OP1 (ISO124p) is a precision isolation amplifier with high bandwidth (50 kHz), while OP2/3 are LT1226, a low noise, very high speed operational amplifier, with extremely high bandwidth and slew rate, 1 GHz and 400 V/μs, respectively.

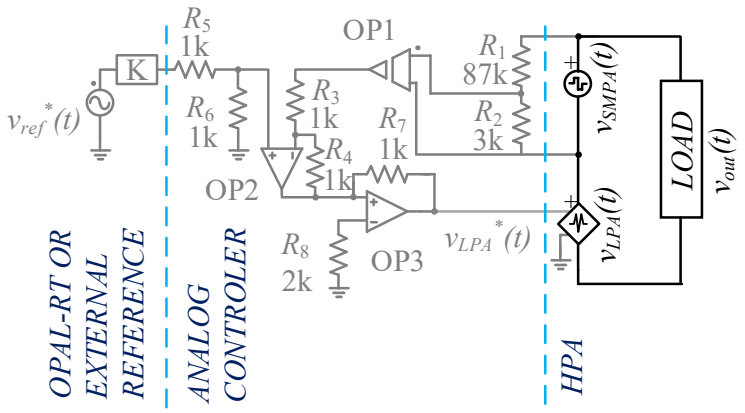


Figure 2.6 – Proposed isolated analog control for the LPA

The proposed solution senses the output voltage of the SMPA throughout a resistive voltage divider set with a gain of 1/30. OP1 is responsible for isolating the power and signal levels, one of the main benefits of the proposed solution. It has enough bandwidth to replicate the fundamental and harmonic components of the output voltage of the CHBM converter, a staircase waveform. OP2 is responsible for generating a reference signal for the LPA based on the difference between the SMPA isolated signal and the HPA reference signal, processed by the *K* block with the same gain of the voltage divider. The gain *K* is implemented on the reference signal independently from the source (internally from the OPAL-RT or from an external reference). OP3 applies a gain of 1.5 to the resulting signal, producing an LPA control signal, which corresponds to 1/20, of the voltage of the SMPA and reference for the HPA. Since the gain of the LPA (LVC5050) was set to 20, one should obtain the expected output voltage for the HPA. The performance of the proposed controller is evaluated experimentally in Section 2.3 under steady state and transient conditions.

2.1.3. Design Approach

This section discusses some considerations for a basic design of a series type HPA with a CHBM converter operating with staircase modulation. The main specifications are the desired output RMS voltage (V_{out}), and RMS current (I_{out}) and the HPA's rated output voltage (V_{LPA}). Since the LPA operates as an active power filter, to compensate the harmonics of the staircase voltage waveform of the CHBM converter (v_{SMPA}), its rated voltage has an impact on the number of cells (Nt) and DC bus voltage (V_{DC}) of the CHBM converter. Besides, since all LPAs have a finite slew rate (SR or dv/dt) while the output voltage of the CHBM converter can change very fast, it is

important to slow the latter down, with a slew rate limiter, to minimize glitches and notches in the output voltage of the HPA. Details of these designs are discussed in the following subsections.

2.1.3.1. Number of CHBM Converter Cells

The minimum number of cells (n_{min}) for the CHBM converter can be found as given by (2.2), using the ceiling function. The division by two is justified because the LPA should provide, or output, both positive and negative voltages during any polarity of the reference voltage. A safety margin (SM) must be used for the LPA to ensure that it can provide enough voltage (v_{LPA}) to synthesize the desired output voltage during dynamic conditions such as reference voltage variations.

In (2.3), one can observe the relation between the required value of V_{DC} and the number of cells of the CHBM converter ($n_{min} \leq Nt$). There, a trade-off must be taken into account according to the designer's constraints and preferences. More H-bridge cells require more switches, gate drives and additional connections but they are of lower power and require lower power DC supplies. Conversely, fewer H-bridges cells reduce the system complexity but require higher power and voltage cells and DC power supplies. The switches of the H-Bridge are selected according to the cells' voltage, current and maximum frequency of the output voltage. Recall that with staircase modulations, the cells are switched at the frequency of the reference output voltage. Using (2.2) and (2.3) in (2.1), one determines the power requirement of the DC power supplies of the CHBM converter.

$$n_{min} = \text{ceiling}\left[\frac{\sqrt{2}V_{out\_R} - (1 - SM)V_{LPA}}{2(1 - SM)V_{LPA}}\right] \tag{2.2}$$

$$V_{DC} = \frac{\sqrt{2}V_{out\_R} - (1 - SM)V_{LPA}}{n_{min}} \tag{2.3}$$

where V_{out_R} is the rated RMS value of the HPA reference voltage.

2.1.3.2. LPA Selection Criteria

In series type HPAs, the LPA has to withstand the entire load current (I_{out}). Its differential output voltage should be such that it can at least cover one level/step of the SMPA voltage waveform, between -0.5V_{DC} and +0.5V_{DC}, in addition to the applied safety margin. The LPA's output voltage during normal operating conditions (for HPA sinosoidal outputs), presents the shape

shown in Figure 1.5, where the points of discontinuity are defined by the transition angles of the staircase voltage waveform of the SMPA. Therefore, one can compute the average output power of the LPA (P_{outLPA}) according to (2.4) [35], where angles γ_n are obtained using (1.2) for a given output voltage (V_{out}).

$$\begin{aligned} P_{out_{LPA}} = \frac{\sqrt{2}}{\pi}\, I_{out} \Bigg\{ & \frac{V_{out\_R}}{2}(\pi \cos\theta) \\ + \; & V_{DC}\big[-\cos(\gamma_n + \theta) \\ & - \cos\big(\gamma_{(n+1)} + \theta\big) - \cdots \\ & + \cos\big(\pi - \gamma_{(n+1).off} + \theta\big) + \cos(\pi - \gamma_n + \theta)\;\big]\Bigg\} \end{aligned} \tag{2.4}$$

where γ_n are the primary angles (1.2) for $n = 1 \ldots Nt$ for a given v_{ref}.

V_{out_R} is the rated RMS value of the HPA reference voltage.

I_{out} is the RMS value of the load current

θ is the phase angle between V_{out_R} and I_{out}

Another parameter for the selection of LPAs is the minimum required slew rate, as in (2.5) [125].

$$SR_{LPA} > 2\pi f_{max} \hat{v}_{ref} \tag{2.5}$$

where f_{max} is the maximum output frequency

$\hat{v}_{ref}$ is the maximum peak reference/output voltage.

2.1.3.3. Voltage Slew Rate Limiter Filter Design

As mentioned before, a voltage slew rate limiter should be added to the output of the CHBM converter to allow an LPA with a finite SR to fully compensate for the harmonic distortions of v_{SMPA}. The voltage slew rate limiter is usually composed of a Passive Damping (PD) filter and an LC low-pass filter, as shown in Figure 2.7(a). It is usually set to limit the *SR* of the SMPA (SR_{SMPA}) between 1/10th and 1/8th, of the *SR* of the LPA (SR_{LPA}) [58].

With the chosen value for SR_{SMPA}, it is possible to determine the natural frequency, f_n, of the LC low-pass filter, as presented in (2.6) [35], [58], [83].

$$f_n = \frac{SR_{SMPA}\, 10^6}{3.072\, V_{DC}} \text{ Hz} \tag{2.6}$$

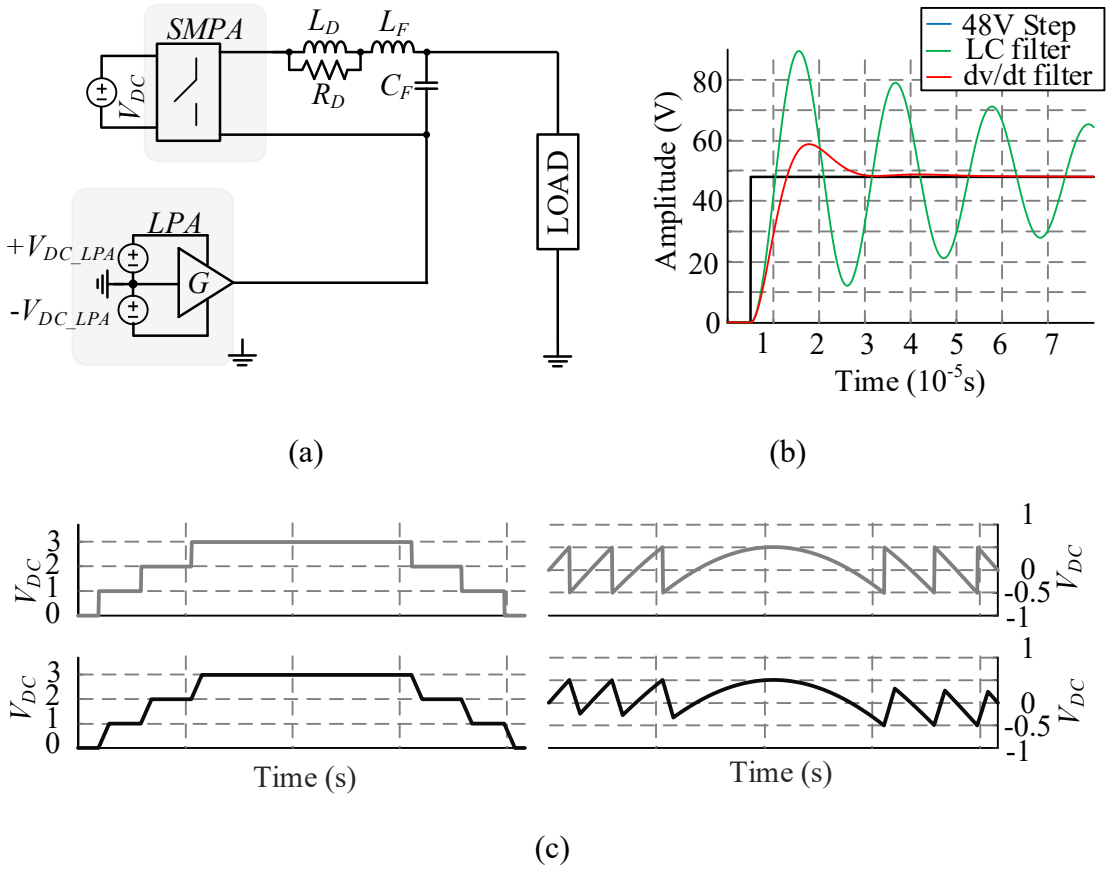


Figure 2.7 – (a) Series HPA with voltage slew-rate (*dv*/*dt*) limiter [35], (b) simulation results for LC and PD+LC filter, (c) theoretical representation of the effect of the PD+LC in the SMPA and LPA output voltages

According to [35], [83], the filter capacitor (C_F) must be designed to conduct 50% of the load current, in the worst-case scenario (nominal/full load, R_{rated}, and maximum output frequency, f_{max}). The minimum requirements for C_F and L_F are shown in (2.7) and (2.8).

$$C_F \leq \frac{0.5}{2\pi f_{max} R_{rated}} \tag{2.7}$$

$$L_F = \frac{1}{(2\pi f_n)^2 C_F} \tag{2.8}$$

The PD circuit is designed to reduce the overshoot and the oscillations (usually referred to as ringing) in the output of the second order LC filter, and it can be designed in accordance with [83]. For frequencies below rated, inductor L_D provides a low impedance path for the load current with minimum losses. For resistor R_D to operate as a PD element, L_D's impedance must be higher

than R_D's at the LC filter natural resonance frequency (f_n). It is calculated using (2.9)-(2.11). Typical values for b are 5 to 10 [58], [83].

Figure 2.7(b) shows some theoretical waveforms concerning the voltage slew rate limiter and a step change (48 V) in the output voltage of the SMPA. The latter, with high dv/dt, is shown in blue. The second order LC filter reduces the dv/dt, but results in an oscillatory transient, green waveform. The addition of the PD circuit damps the oscillation but a small overshoot remains, as shown in the red waveform. With the designed filter, the output voltage settles within ±2.5% of the steady state value in 46 μs for the PD+LC filter and in 5.75 ms for the LC only filter. Another aspect to be considered is the impact of the slew rate limiter on the operation of the LPA in the series type HPA. Figure 2.7(c) shows the theoretical voltage waveforms of the SMPA and LPA, without the voltage slew rate limiter, in grey, and with it, in black. There one can see that one of the consequences of the delay introduced by the voltage slew rate limiter is the loss of quarter-wave symmetry in the output voltage of the LPA. The higher the frequency of the reference output voltage, the higher should be the degradation of the symmetry.

$$R_D = \frac{\sqrt{L_F/C_F}}{Q} \tag{2.9}$$

$$Q = \left(\frac{1+b}{b}\right)\sqrt{\frac{2(1+b)(4+b)}{(2+b)(4+3b)}} \tag{2.10}$$

$$b = \frac{L_D}{L_F} \tag{2.11}$$

2.2. System Specification and Design Example

The design specifications for the single-phase 220 Vrms, 1 kW series type HPA considered in this section are shown in Table 2.1. The maximum output frequency (f_{max}) is 1 kHz, enough to emulate a broad spectrum of frequencies as an HPA for applications such as Alternating Current Power Supplies (ACPS), motor/generator emulation and other IUT.

The LPA will be operated considering a maximum output voltage ($\hat{v}_{LPA}$) of ±50 V and a safety margin (SM) of 0.5. The resulting slew rate for a SMPA associated with an AE Techon LVC5050 is lower than that of the APEX MP111 solution, thus requiring the use of a larger/slower voltage slew rate limiter. As a result, considering that the "active" compensating capabilities of

the LPA are reduced during this time interval, the output voltage waveform of the HPA will depend mostly on the behavior of the "passive" voltage slew rate limiter. Therefore, the transient distortion in the output voltage waveform of the HPA, due to a step variation in the output voltage of the SMPA, should be shorter with the APEX solution. The drawback relies on its design, since it is more complicated, all the internal connections have to be made, boost gains have to be calculated for the internal controller, and Printed Circuit Boards (PCB) breakouts or shield boards have to be designed for it. As a comparison, the AE Techron LVC5050 is a great bench product that provides a plug and play solution with extreme easiness of use. All the internal gains are set, and the user can even control the output gain by a simple knob.

Table 2.1 – Design specifications and calculated parameters of the series type HPA

	System Specifications	Calculated Parameters
Rated Power	1 kW	-
Rated Voltage (RMS)	220 V	-
Output Frequency Range	0 – 1 kHz	-
Rated Current (RMS)	4.55 A	-
Rated Load Impedance	48.4 Ω / 96.8 Ω	-
Safety Margin for the LPA	0.5	-
Number of SMPA cells (2.2)	-	6
DC bus voltage (V_{DC}) (2.3)	-	48 V
Cell's max P_{out} (2.1)	-	195 W
LPA's average power (2.4)	-	113 W
Voltage Limits Ψ_n (1.1)	-	24, 72 ... 264 V

The number of CHBM converter cells (Nt) and their DC bus voltage (V_{DC}) are computed using (2.2) and (2.3), resulting in six-cells and 48 V, respectively. The maximum average power for the CHBM cells, considering the worst modulation scheme (FILO) was computed as 195 W, using (2.1) with $n = 1$. The average output power of the LPA was computed as 113 W, about 11% of the rated power of the HPA, using (2.4). Table 2.2 summarizes all the variables discussed so far and presents the values found using the equations shown in this study. Likewise, Table 2.2 presents the design specifications and computed parameters, along with their equations, for the voltage slew rate limiter to be used in the output of the CHBM converter.

Table 2.2 – Design specifications and parameters of the voltage slew rate limiter

Parameters	Value	Commercial Value
SR_{LPAmin} (2.5)	1.95 V/µs	-
SR_{LPA} (AE Techron 5050LVC) [124]	30 V/µs	-
SR_{SMPA}	3.5 V/µs	-
f_n (2.6)	23.73 kHz	-
C_F (2.7)	< 1.64 µF	1.5 µF
L_F (2.8)	29.97 µH	30 µH
L_D (2.11)	0.149 mH	0.15 mH
b (2.11)	5	-
Q (2.10)	1.08	-
R_D (2.9)	4.13 Ω	4.2 Ω

2.3. Experimental Validation and Results

An experimental setup, shown in Figure 2.8, was built to validate the proposed modulation technique (SV-FIFO), design procedure of the series type HPA and control strategy for closed loop operation. It presents the specs and parameters described in Table 2.1 and Table 2.2.

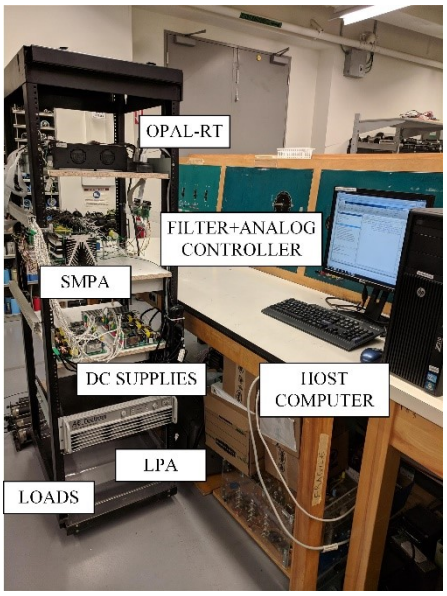


Figure 2.8 – Photo of the complete experimental setup.

The SMPA was built with six H-bridges using MOSFETs SUA70060E (Vishay) and gate driver circuits SKHI 61R (Semikron). They were powered by six 250 W AC powered DC sources SWF240P-48 (Sanken). Voltage sensors (LV-20P) are connected at the output of each H-bridge and one current sensor (LA-55P) measures the current supplied by the HPA. This allows the computation of the output power of each H-bridge. The LPA is an LVC5050, from AE-Techron.

Regarding the control system of the HPA, an OP4510 real-time simulator (OPAL-RT) is employed for generating the gating signals of the CHBM converter. The latter is controlled with a time step of 10 μs. The frequency of the reference signal, when chosen by the user and not by an external reference, ideally must be multiple of that time step to avoid any errors on the signal, which is irrelevant for lower frequencies (0.01% error in frequency for 60 Hz) but more significant closer to the upper limit frequency (up to 0.5%). This avoids problems with sub-harmonics of low order.

As mentioned in Section 2.2, the computation of the turn on and off angles of each H-bridge with SV-FIFO, which might be different from those of the staircase, requires the knowledge of the frequency and magnitude of the reference output voltage. In this study, the second topology presented and validated in Chapter 4 and [88] was used, with same gains and control strategy. It employs digital and analog blocks, easily realized in the RTS, and was devised for this application.

The reference signal for the LPA (v_{LPA}^{*}) is obtained with the analog circuit shown in Figure 2.6. It subtracts the sensed output voltage of the SMPA (v_{SMPA}), including the PD filter, from the reference signal of the HPA (v_{ref}^{*}), provided by the OPAL OP4510. It also provides isolation between power and signal stages while matching the magnitude of the input signals to the fixed gain of the LPA. The analog control circuit is implemented on an external board, which also contains the *dv*/*dt* filter and auxiliary circuits for protection and for powering gate drivers and sensors.

A host computer interfaces with the OP4510 and is used to run a Graphical User Interface (GUI) for monitoring and control. There, one can set the magnitude and frequency of the reference HPA output voltage, the modulation scheme and visualize the amount of power supplied by each H-bridge and system waveforms (due to the presence of the individual voltage sensors). The system is assembled on a 44U rack for increased mobility.

The following subsections present experimental results for the system operating in steady state, to validate the power balancing features of the new SV-FIFO modulating scheme and show the high quality of the resulting output voltage waveform. Then, results for the system operating under transient conditions are depicted to assess the accuracy of the proposed control system of the HPA.

2.3.1. Steady State Analysis and Comparison between Staircase Modulation Techniques

The first test concerns operation with rated voltage (220 Vrms) and rated power (1 kW). The waveforms of the SMPA voltage, LPA voltage and HPA voltage and current are shown in Figure 2.9, for 60 Hz, and Figure 2.10, for 1 kHz. Both results are taken when the HPA is controlled using the SV-FIFO algorithm. For all experimental results, the on-line digital controller for the SMPA is implemented in the OPAL-RT and the isolated analog controller for the LPA is implemented as an external board. The results were acquired using a Tektronix MDO Series Scope.

Figure 2.9 shows, on the top, the output voltage of the SMPA, measured at the output of the voltage slew rate limiter. It is a staircase, with small overshoots and virtually no ringing, during the transitions from one step to the other, achieved with passive damping (PD). The output waveform of the LPA is slightly different from the theoretical shown in Figure 1.5, due to the phase lag on the staircase waveform introduced by the voltage slew rate limiter. Nonetheless, the output voltage of the HPA, on the bottom, presents a sinusoidal shape, which shows the ability of the LPA (and the proposed isolated analog controller) to compensate those overshoots. Although not a design specification, the Total Harmonic Distortion (THD) can be used as a waveform quality indicator. The THD of the HPA output voltage for this condition is 1.17%, which is below the limits imposed by the IEEE 519-2014 [126].

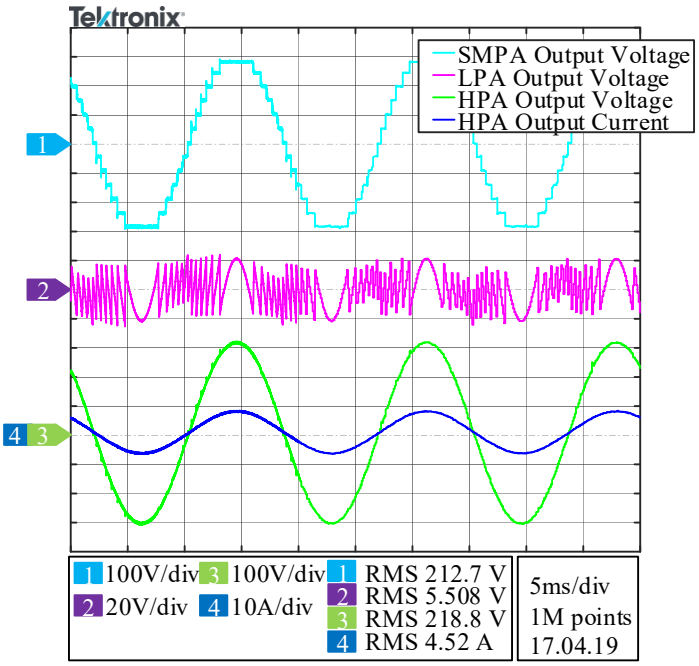


Figure 2.9 – Experimental results showing the SMPA, LPA and HPA output voltages along with the HPA output current for a 220 Vrms 60 Hz reference voltage and rated load.

The same waveforms are presented in Figure 2.10 for a reference voltage of 220 Vrms and 1 kHz. Due to the higher fundamental frequency, the overshoots in the staircase waveform are more noticeable. Besides, the delay introduced by the voltage slew rate limiter is higher, which makes the output voltage of the LPA change more with respect to that in Figure 1.5, for the ideal and unfiltered case. Nonetheless, the output voltage of the HPA still presents a high quality, with a 4.9% THD.

The effect of SV-FIFO on the output voltage of the H-bridges can be seen in Figure 2.11, along with the output voltage of the SMPA for a 200 Vpeak, 60 Hz reference voltage. In this case, only four H-bridges would be activated in a line cycle with FILO and FIFO. With SV-FIFO, all H-bridges operate in all line cycles. CHBM converter cells one and two share the first voltage level, cells three and four share the second level, while cells five and six are controlled as with the traditional FIFO.

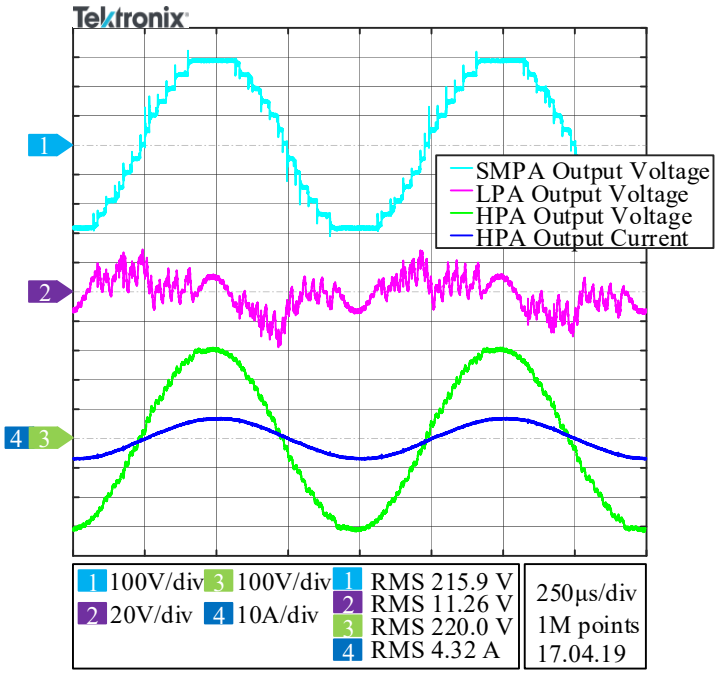


Figure 2.10 – Experimental results showing the SMPA, LPA and HPA output voltages along with the HPA output current for a 220 Vrms 1 kHz reference voltage and rated load.

Next, it is important to verify how SV-FIFO enhances the power balance among the CHBM converter cells. Figure 2.12 shows the average power supplied by each cell for FILO, FIFO and SV-FIFO for various reference output voltages (50 Vpeak, 100 Vpeak, 200 Vpeak and 300 Vpeak) and rated load.

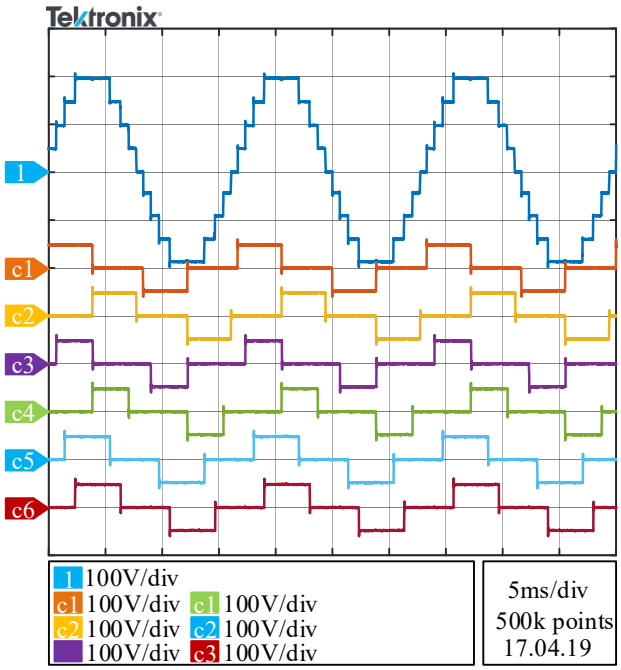


Figure 2.11 – Experimental results for rated load showing the SMPA and the individual cells output voltages for an HPA output 200 Vpeak at 60 Hz.

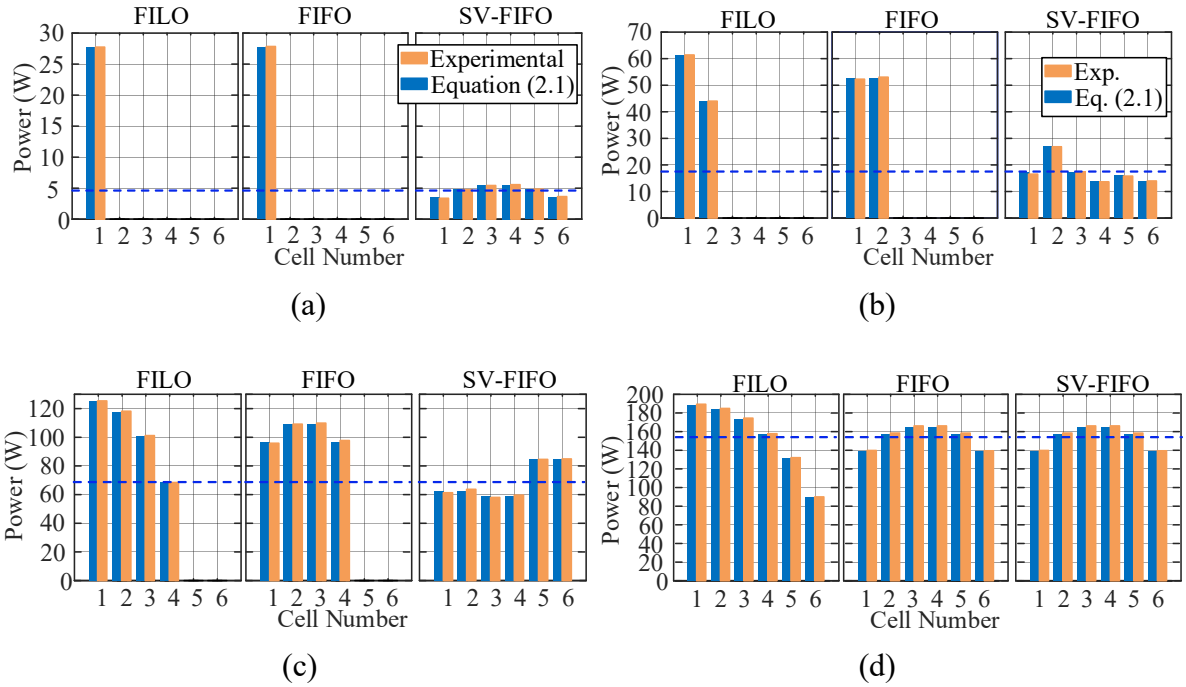


Figure 2.12 – Power contribution by each CHBM converter cell for HPA output peak voltages of (a) 50 Vpeak, (b) 100 Vpeak, (c) 200 Vpeak and (d) 300 Vpeak output, at 60 Hz.

These values were selected because they lead to staircase waveforms of lower number of steps which leads to some cells not being used in a given line cycle. The blue bars present the results of the analytical equations, as given in (2.1), and the orange bars, of the experimental results. The voltages for each cell are read using individual sensors in a real-time monitoring system in Simulink, which is also responsible for processing the voltages and current to show the individual power consumption. The results for all the strategies show a very good agreement, with a maximum error of 3.95%, which contains the error added by the sensors, acquisition systems and the general uncertainty of the data processing. The orange bars represent the average power in all cells of the CHBM converter. It is evident that SV-FIFO results in a better power balance than the others, except for high output voltage values, where FIFO and SV-FIFO result in the same number of active CHBM converter cells.

2.3.2. Dynamic Performance Analysis

The regulation of the output voltage of the HPA during transient conditions requires that the isolated analog control circuit generates the appropriate reference signal for the LPA, while the OPAL-RT, as a digital controller, provides the gating signals for all H-Bridge cells. To evaluate the dynamic performance of the system under the SV-FIFO algorithm, first, an amplitude step is given to the reference output voltage. It is changed from 220 to 127 Vrms, while keeping a constant output frequency at 60 Hz. The resulting waveforms can be observed in Figure 2.13.

The step is given shortly before the 30 ms mark. One can see, on the top, the SMPA's output voltage waveform changing from six to four positive levels almost instantaneously. The LPA's output voltage also changes, to compensate for a different staircase and achieve a sinusoidal voltage at the output of the HPA, shown in the bottom of Figure 2.13. Before the step, there are 12 transitions in the positive semi-cycle of the output voltage of the LPA, while after the step, there are only eight transitions.

Next, a step change in frequency is given to the reference output voltage, from 60 to 500 Hz, with constant amplitude of 220 Vrms and half-rated load. The same waveforms are shown in Figure 2.14. A higher frequency step could be used, but the visualization of the data for the higher frequency would not be beneficial. It can be seen that there is no change on the number of levels and shape of the SMPA's output because there is no change on the amplitude of the reference signal. Likewise, the HPA's output voltage and current do not change in amplitude. The step is

given during the fourth time division and both SMPA and LPA controllers act fast enough to avoid any saturation on the LPA and degradation of the output voltage signal of the HPA.

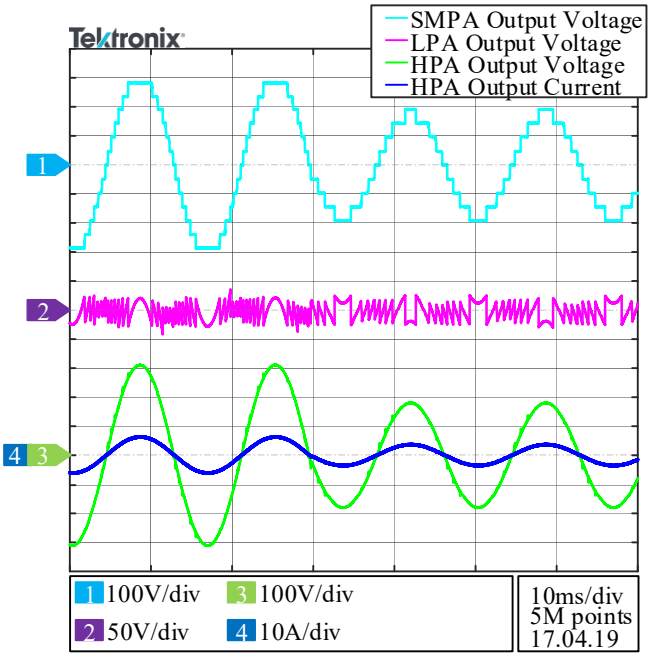


Figure 2.13 – Experimental results for rated load showing the SMPA, LPA, HPA output voltage and HPA output current for an output varying from 220 Vrms to 127 Vrms at 60 Hz

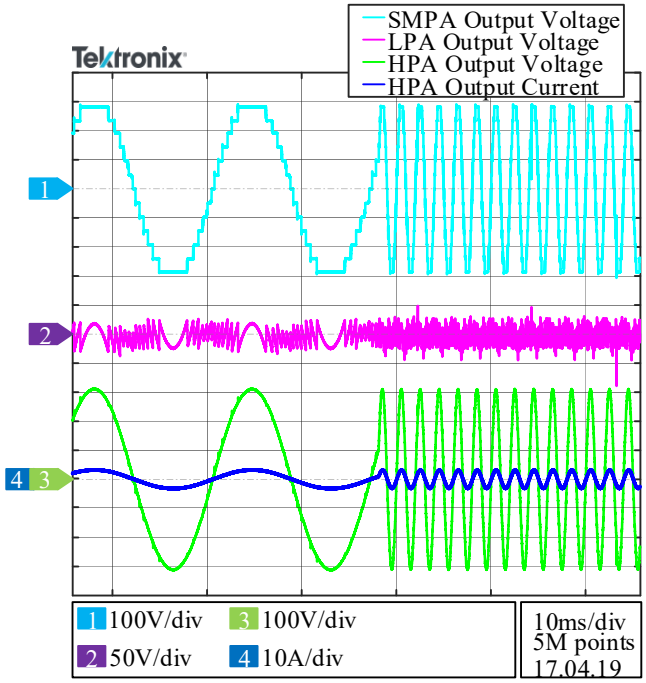


Figure 2.14 – Experimental results for half load showing the SMPA, LPA, HPA output voltage and HPA output current for an output varying from 60 Hz to 500 Hz at 220 Vrms

The SM of the LPA was marginally used just for a few corrections on the phase of the output voltage, especially for operations in higher frequencies, such as 500 Hz. This validates the proposed mixed signal control scheme, with both digital and isolated analog processing blocks.

2.4. Independent Load Balancing Modulation

The angles generated by the NLC for the SMPA must be respected because in the context of the HPA, they result in requiring a lower voltage output and voltage ratings from the LPA. Using other angles would require higher voltages from the LPA risking saturations on the output signal, compromising the output quality. The LPA is the main contributor of losses on the system [5], so using it at a lower power and voltage is desired. Although the losses on the LPA are extremely important and relevant, this study will focus on the SMPA only, since the proposed technique can be useful not only to HPA applications but to any multilevel converter under staircase modulation. As already discussed, FILO, FIFO and SV-FIFO are NLC based techniques that produce the same output, by modulating the cells in different ways.

The technique proposed in this study, the SV-FIFO focuses on improving the power balance for non-rated output voltages, but for a resistive load. The literature has a shortage of studies for improving the balance of the cells for other linear loads, such inductive or capacitive loads. Alternatives to improve the power balance are given in [127] by increasing the switching frequency of the CHBM but this is not considered in this study, since the objective is to improve the power balance while switching the cells at the same frequency as the reference voltage waveform.

2.4.1. Introduction

To improve the power balance for all linear loads (resistive, inductive and capacitive), a new technique, called Independent Load Balancing (ILB) modulation is proposed and detailed in this section. Now the half-wave and quarter-wave symmetry, in (2.1), cannot be used anymore because the switching angles from the positive and negative portions of the output signal can be different. The technique computes all the possible non-repetitive combinations for turn on and turn off angles, looking for those that generate an output power as close as possible to the average power per cell. This is another reason to consider positive and negative portions of the output to expand the possible combinations.

Differently from previous techniques, as shown in Figure 2.15, for ILB modulation there is no sequence pattern to determine the angles from 1 to *Nt*, since any possible combination can happen. In Table 2.3 there is a representation of the cells sequential order for the existing and proposed technique, based on the example of Figure 2.15. For ILB modulation, the output voltage and current must be identified, to generate the Φ angle (phase between them). Another input to the algorithm is the number of cells, and the primary angles given by (1.2).

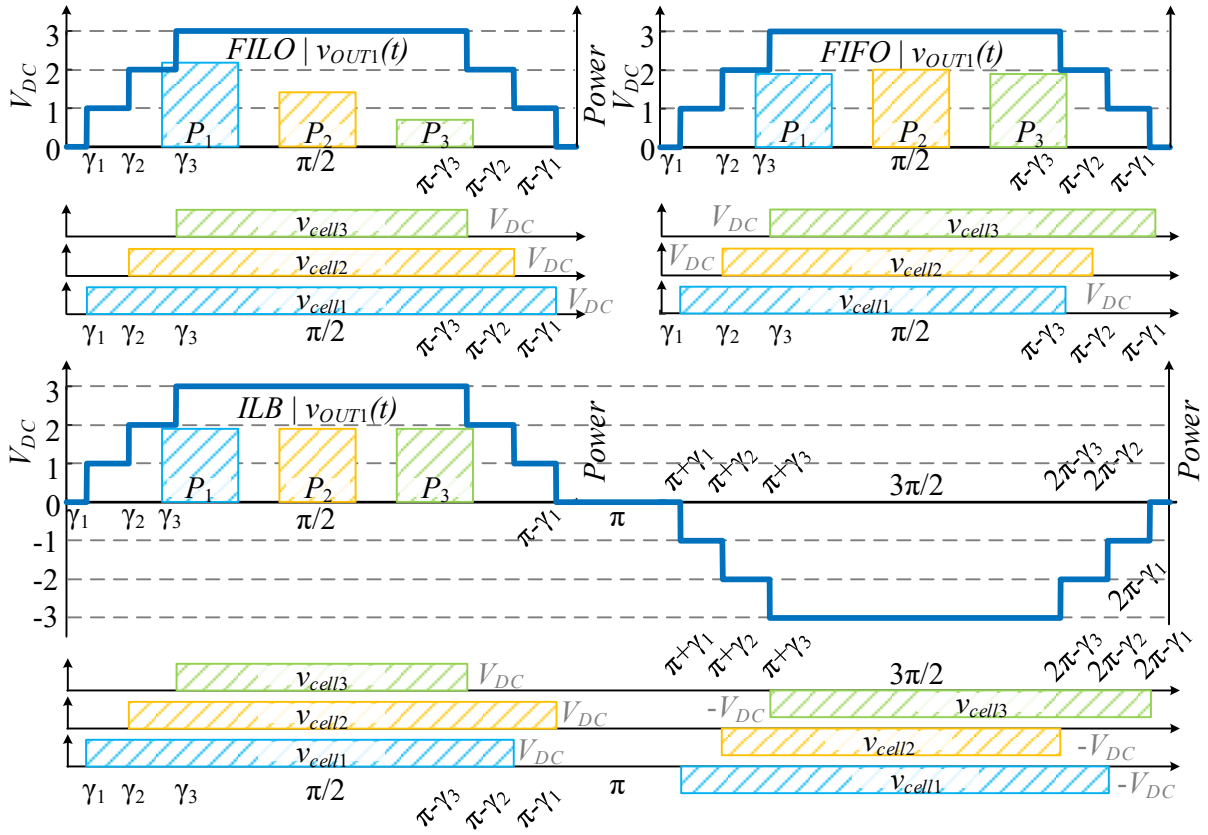


Figure 2.15 – Envelope of the SMPA output voltages and the each SMPA cell contribution with FILO on top left, FIFO on top right, and ILB on bottom and their respective theoretical power consumption behind

For ILB modulation, all reference cycles (positive and negative) must be evaluated to find combinations that will yield an individual consumption closer to the average. The individual power consumption for the cells, considering the complete reference cycle can be found using (2.12). It will be of extreme importance for ILB modulation, as described in the next section.

Table 2.3 – Sequential order of cells turn on and turn off for FILO, FIFO and ILB, based on the example of Figure 2.15

	Positive						Negative					
	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th
FILO	#1on	#2on	#3on	#3off	#2off	#1off	Same as positive					
FIFO	#1on	#2on	#3on	#1off	#2off	#3off	Same as positive					
ILB	#1on	#2on	#3on	#3off	#1off	#2off	#3on	#2on	#1on	#2off	#1off	#3on

$$P_{out_{cell},n} = \frac{\sqrt{2}}{2\pi} V_{DC}\, i_{out}\left[cos(\alpha_{n1.on} + \Phi) - cos\left(\alpha_{n1.off} + \Phi\right)\right] + \frac{\sqrt{2}}{2\pi} V_{DC}\, i_{out}\left[cos(\alpha_{n2.on} + \Phi) - cos\left(\alpha_{n2.off} + \Phi\right)\right] \quad (2.12)$$

where $\alpha_{n1.on}$ will be the positive turn on angle

$\alpha_{n1.off}$ will be the positive turn off angle

$\alpha_{n2.on}$ will be the negative turn on angle

$\alpha_{n2.off}$ will be the negative turn off angle

2.4.2. Proposed Algorithm

The proposed ILB modulation algorithm, receives as input the reference voltage, v_{ref}, the NLC primary angles (with quarter-wave symmetry) from which all full-wave angles will be found, the output current, i_{LOAD} and its phase angle when compared to the output voltage, Φ, the V_{DC} bus voltage level. With v_{ref}, i_{LOAD} and the (fixed) number of cells of the system, n, the average power, $P_{avg.cell}$, can be found using the individual power consumption as given by (2.12). The primary angles for a six-cell CHBM, based on the NLC technique, can be also arranged as a vector (2.13).

$$\gamma_n = [\gamma_1 \quad \gamma_2 \quad \gamma_3 \quad \gamma_4 \quad \gamma_5 \quad \gamma_6] \quad (2.13)$$

where $n = 1 \ldots Nt$

Initially, for the first cell, the algorithm creates all possible turn on and off combinations for both positive and negative cycles, as shown in Table 2.4. Observe that the first turn on angle is fixed for the first cell, the second turn on angle for the second cell, until the last, Nt^{th}, cell. The algorithm will use (2.12) with all the three remaining angles and generate a three dimension matrix of output power $P_1(Nt,Nt,Nt)$, each one related to a possible combination. The system will then

find the specific combination $[a,b,c]$, with the smallest difference between the average and all individual contributions.

$$[a \quad b \quad c] = \min\left|P1(Nt, Nt, Nt) - P_{avg.cell}\right| \tag{2.14}$$

Shown as an example in Table 2.4, the combination is (*1,6,6,5*). It is a computed result, which indicates that the first cell will turn on at the positive cycle with its original turn on angle and turn off with the original turn off angle from the 6th cell. On the negative cycle, it will turn on with the original angle from the 6th cell and off with the 5th. This combination is not available anymore for any other cells (the diagonal lines represent the removal). This fact can be observed in the second line of the matrix of possible combinations, presented in Table 2.5.

In Table 2.5, the (*6,6,5*) combination is not shown anymore. Now for second cell, the same equation will be used, but now the mathematical processing of the individual power will output a matrix with the same order but with reduced number of elements, $P_2(Nt\text{-}1,Nt\text{-}1,Nt\text{-}1)$. Once again, the closer value of power with the average is found and that combination is removed from the possibilities to the third and so on, until reaching the $Nt\text{-}1^{th}$ cell. In this example, the computed combination (*2,1,1,2*) will be removed.

This approach does not give any space for choice for the last cell, because the order, at that condition, will be only one possible combination for the Nt^{th} cell, on this case $P_6(1,1,1)$ with the remaining angles, but if the system could find well balanced results for all the other cells, this will also be balanced. Increasing the number of cells improves the power balance because the number of possibilities for turn on and off but it will require more computational power to process those combinations.

Table 2.4 – Possible turn on and off angles for the first cell

Positive		Negative	
$\alpha_{n1.on}$	$\alpha_{n1.off}$	$\alpha_{n2.on}$	$\alpha_{n2.off}$
$\gamma_n(1)$	π-$\gamma_n(1)$	π+$\gamma_n(1)$	2π-$\gamma_n(1)$
$\gamma_n(1)$	π-$\gamma_n(1)$	π+$\gamma_n(1)$	2π-$\gamma_n(2)$
⋮	⋮	⋮	⋮
$\gamma_n(1)$	π-$\gamma_n(6)$	π+$\gamma_n(6)$	2π-$\gamma_n(4)$
$\gamma_n(1)$	π-$\gamma_n(6)$	π+$\gamma_n(6)$	2π-$\gamma_n(5)$
$\gamma_n(1)$	π-$\gamma_n(6)$	π+$\gamma_n(6)$	2π-$\gamma_n(6)$

Table 2.5 – Possible turn on and off angles for the second cell

Positive		Negative	
$\alpha_{n1.on}$	$\alpha_{n1.off}$	$\alpha_{n2.on}$	$\alpha_{n2.off}$
$\gamma_n(2)$	$\pi-\gamma_n(1)$	$\pi+\gamma_n(1)$	$2\pi-\gamma_n(1)$
~~$\gamma_n(2)$~~	~~$\pi-\gamma_n(1)$~~	~~$\pi+\gamma_n(1)$~~	~~$2\pi-\gamma_n(2)$~~
⋮	⋮	⋮	⋮
$\gamma_n(2)$	$\pi-\gamma_n(6)$	$\pi+\gamma_n(6)$	$2\pi-\gamma_n(4)$
$\gamma_n(2)$	$\pi-\gamma_n(6)$	$\pi+\gamma_n(6)$	$2\pi-\gamma_n(6)$

The maximum computational time to converge to the optimal solution is given in (2.15) as a function of the total number of cells the time step, T_{step}, of the simulator or controller in where the algorithm will run. As an example, a six-cell system would require 441 cycles and considering a T_{step} as of 1 µs (clock 1 MHz), the solution would require 0.44 ms to achieve the optimal result. Compared to the 60 Hz grid frequency, which is approximately 40 times faster.

$$\hat{t}_{conv} = \left[\sum_{n=1}^{Nt} n^3\right] T_{step} \tag{2.15}$$

2.4.3. Complete CHBM Control System with ILB

The overall control system for a CHBM based HPA (the LPA control is not presented since it is not the focus and not impacted by the ILB) is shown in Figure 2.16. The system can be divided into a few parts. The suitable frequency and amplitude detection block (detailed in grey) is proposed in Chapter 4 and [88] to identify the angular speed, phase angle and amplitude of an external reference voltage, an important feature for HPA that are fed from external controllers as the signal is unknown. K_1 will be kept by default as 1. The area in orange represents the identification of the angle between the output voltage and the output current. It creates an orthogonal signal to the current, i_{LOAD}, by a double integration of the signal. K_2 is set to compensate for the gain introduced by both integrations and is set by default as 0.5.

The original and orthogonal signals are inputted to a Park's transformation (αβ-*dq*) block, which will synchronize those input signals with the angle reference given by the output/reference voltage. The signal on the *d*-axis is inverted and the one on the *q*-axis is directly fed to an inverse tangent block, which will provide the angle of the current, Φ, when compared to the output voltage. This is an extremely important input to the individual power calculations, as shown in (2.12).

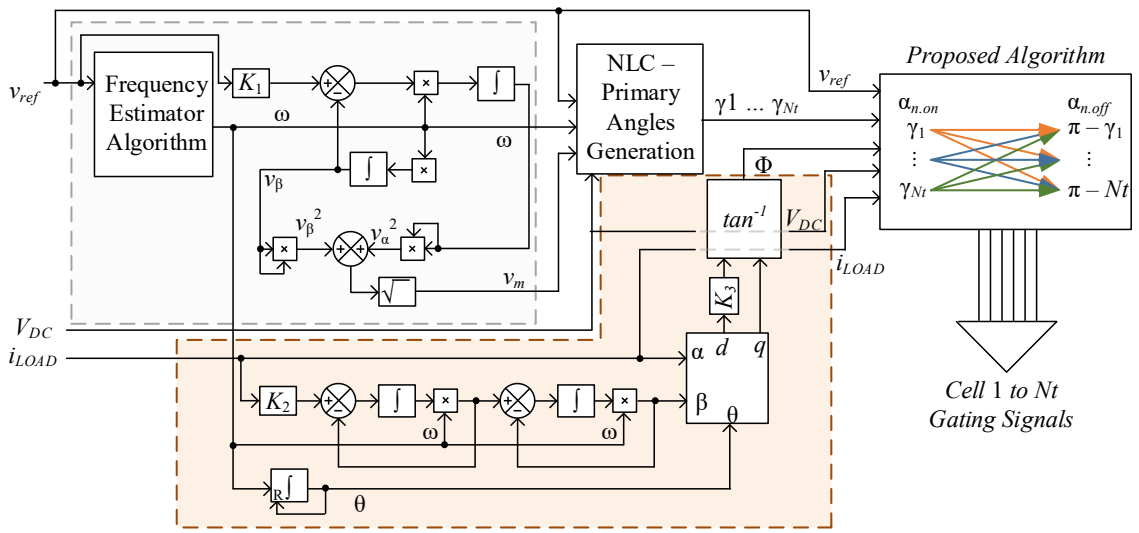


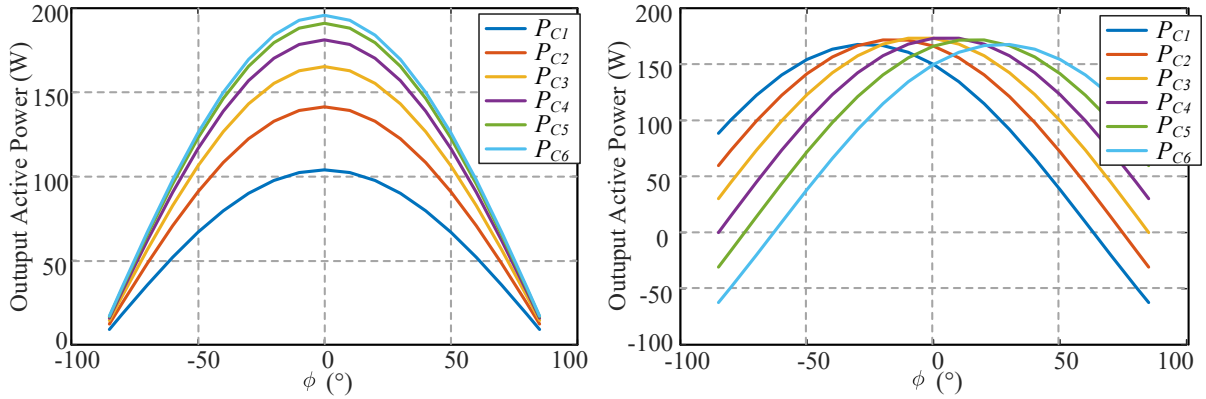
Figure 2.16 – Complete SMPA control system with proposed ILB algorithm

2.4.4. System Definition and Power Curves

To evaluate the difference on the power levels of the cells, a system must be defined. A six-cell system will be used with a DC bus of 48 V to be connected in series with an LPA that can output ±50 V (same as for the experimental validation in Section 2.3). The rated output voltage will be 220 Vrms and the module of load impedance will be kept constant at 48.4 Ω while its angle will be swept from -85° to 85° (using discrete 10° intervals between -80° and 80°), to include from RC to R and RL load impedances.

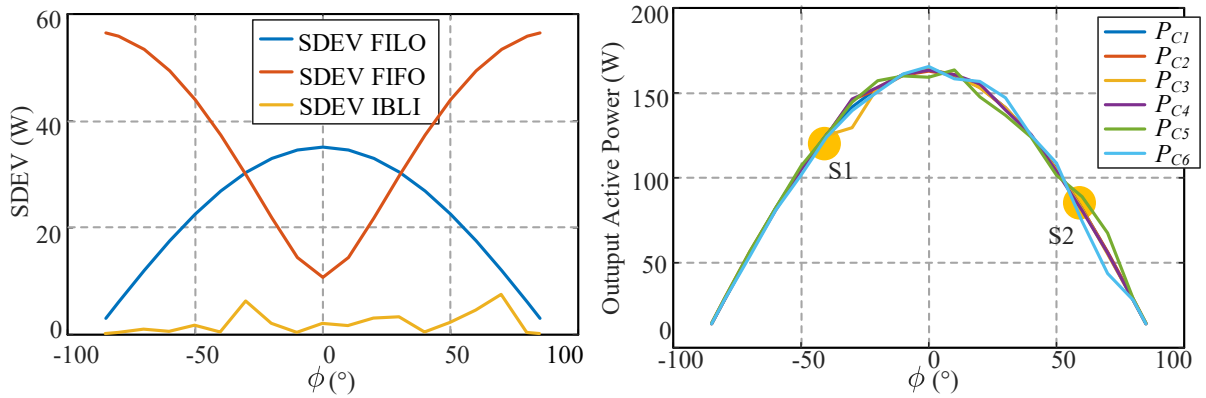
Figure 2.17(a) and (b) show the individual contributions of the cells for FILO and FIFO modulation, respectively, for different load angles and rated output voltage, according to (2.1). For FILO, the balance is improved on the extremes, at higher absolute values of Φ. However, once the load is more resistive the unbalance is higher, visible on the distance between the curves. This is expressed by the standard deviation (SDEV) in the average power demanded by the cells of a CHBM converter, in the blue curve in Figure 2.18(a). For FIFO, one can see a significant decrease on the unbalance for resistive loads, but the balance deteriorates at higher absolute values of Φ. The relative distance between the curves is smaller closer to $\Phi=0°$. The red curve in Figure 2.18(a) shows the SDEV for FIFO for different loads. The yellow curve represents the SDEV with ILB. For all the range, the SDEV with ILB modulation is lower than with any other technique. Differently from the traditional techniques, ILB modulation does not yield a mirrored SDEV for positive and negative load angles of Φ.

Figure 2.18(b) presents the same individual power consumptions but with ILB modulation, using (2.12). It is visible when compared to traditional techniques, that ILB modulation reduces significantly the power unbalance between cells, since all curves are very close together. The area marked with the S1 label represents the resistive and capacitive load simulated in Section 2.4.4.1 and S2 the simulation results shown in Section 2.6.4.2 considering a resistive and inductive load.



(a) (b)

Figure 2.17 – Individual cells consumption accordingly with the current phase for (a) FILO and (b) FIFO modulation



(a) (b)

Figure 2.18 – (a) SDEV to different load profiles and modulation techniques, (b) Individual cells consumption accordingly with the current phase for ILB modulation

2.4.1. Simulation Results

Figure 2.19 shows the HPA's output voltage in blue (100 V/div) and two different current waveforms. The desired output is a sinusoidal waveform, with 220 Vrms and 60 Hz that will be used for simulations, although the system can output up to 1 kHz. The red curve (5 A/div) represents the 45° leading current due to a resistive capacitive load (Φ = -45°). The green curve (5

A/div) shows a 60° lagging current due to a resistive inductive load (Φ = 60°). The load profiles are summarized in Table 2.6. For both load scenarios, as the given reference for voltage will be the same and rated, the HPA's output voltage is built with the series association of the SMPA's output voltage (100 V/div), in cyan, and the LPA's output voltage (50 V/div), in pink.

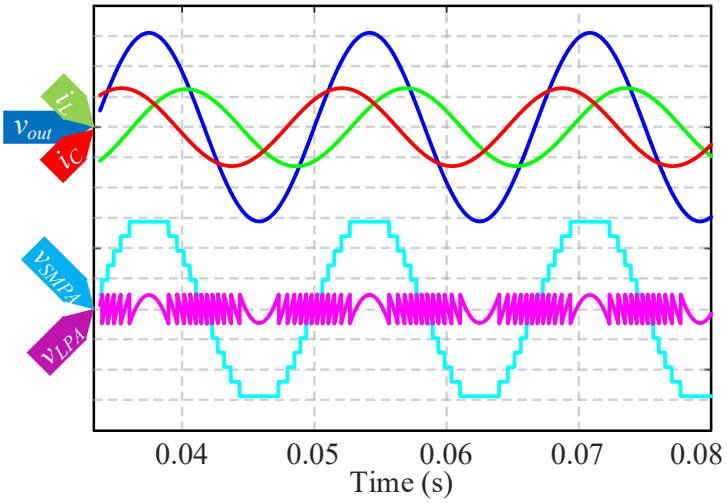


Figure 2.19 – HPA's output voltage, RC load current, RL load current, SMPA's and LPA's output voltages

Table 2.6 – Load profiles for simulation

Load	|Z|	R	X_C / X_L	C / L	Φ
RC	48.4 Ω	34.224 Ω	34.224 Ω	77.50 µF	-45°
RL	48.4 Ω	24.2 Ω	41.915 Ω	111 mH	60°

2.4.1.1. Capacitive (RC) Load (Φ = -45°)

For the first simulation, the RC load will be connected to the HPA's output and the switching angles for cells 1 to 6 will be given by the proposed solution. Due to the elimination of the combination angles for each cell, it is possible to observe on the black curve of Figure 2.20, the SMPA's output voltage, that there are no cells being turned on and/or off at the same time, reproducing the expected staircase at the output. Another thing to observe, is that differently from traditional techniques, there is no clear correlation between the angle a cell turns on and off for positive and negative semi-cycles. The algorithm converges to the solution shown in Table 2.7, within the computational time as given in (2.15). Figure 2.21 presents the power consumption by cell, for the traditional modulation techniques, FILO in blue and FIFO in green. FIFO is known to improve the power balance for rated output voltage, but only for pure resistive loads, which is visible here, since the unbalance is higher with this technique. By applying ILB modulation, the

system reaches an almost perfect balance. In addition, with this technique, the DC power supplies or the isolated DC outputs for the CHBM cells can be designed for lower power consumption.

Table 2.7 – Turn on and off angles for RC Load

Cell #	Positive		Negative	
	$\alpha_{n1.on}$	$\alpha_{n1.off}$	$\alpha_{n2.on}$	$\alpha_{n2.off}$
1	$\gamma_n(1)$	$\pi-\gamma_n(5)$	$\pi+\gamma_n(6)$	$2\pi-\gamma_n(3)$
2	$\gamma_n(2)$	$\pi-\gamma_n(1)$	$\pi+\gamma_n(4)$	$2\pi-\gamma_n(2)$
3	$\gamma_n(3)$	$\pi-\gamma_n(6)$	$\pi+\gamma_n(5)$	$2\pi-\gamma_n(4)$
4	$\gamma_n(4)$	$\pi-\gamma_n(2)$	$\pi+\gamma_n(2)$	$2\pi-\gamma_n(1)$
5	$\gamma_n(5)$	$\pi-\gamma_n(4)$	$\pi+\gamma_n(3)$	$2\pi-\gamma_n(6)$
6	$\gamma_n(6)$	$\pi-\gamma_n(3)$	$\pi+\gamma_n(1)$	$2\pi-\gamma_n(5)$

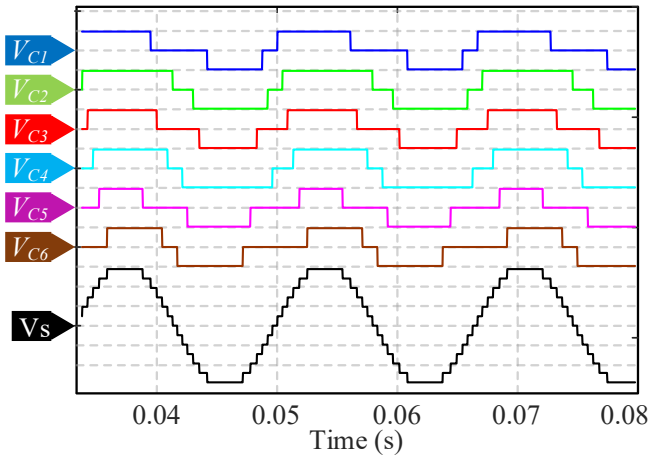


Figure 2.20 – Cells 1 to 6 output voltage and SMPA's output voltage for a RC load

2.4.1.1. Inductive (RL) Load (Φ=60°)

The second simulation will consist of a RL load connected to the HPA's output and the switching angles for cells 1 to 6 will also be given by the proposed solution. Figure 2.22 shows the individual's cell voltage output and the SMPA's output voltage, in black. Once again there are no cells being turned on and/or off at the same time, reproducing the expected staircase at the output due to the non-repetitive approach on the elimination of the angles for each cell. The algorithm converges to the solution shown in Table 2.8. Figure 2.23 presents the power consumption by cell, for the traditional modulation techniques, FILO in blue and FIFO in green. For this condition, the ILB modulation could not find a solution as good as the previous one for capacitive load, but it is still a considerable improvement on the power balance and a reduction on the power ratings required for the DC supplies or the isolated DC outputs for the CHBM.

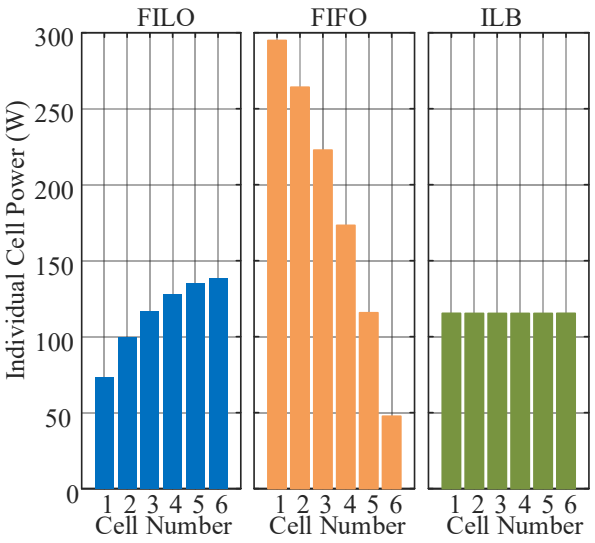


Figure 2.21 – Power consumption by cell with traditional (FILO and FIFO) and proposed modulation technique (ILB) for a RC load

Table 2.8 – Turn on and off angles for RL Load

Cell #	Positive		Negative	
	$\alpha_{n1.on}$	$\alpha_{n1.off}$	$\alpha_{n2.on}$	$\alpha_{n2.off}$
1	$\gamma_n(1)$	$\pi-\gamma_n(4)$	$\pi+\gamma_n(6)$	$2\pi-\gamma_n(3)$
2	$\gamma_n(2)$	$\pi-\gamma_n(3)$	$\pi+\gamma_n(4)$	$2\pi-\gamma_n(4)$
3	$\gamma_n(3)$	$\pi-\gamma_n(2)$	$\pi+\gamma_n(3)$	$2\pi-\gamma_n(5)$
4	$\gamma_n(4)$	$\pi-\gamma_n(5)$	$\pi+\gamma_n(1)$	$2\pi-\gamma_n(1)$
5	$\gamma_n(5)$	$\pi-\gamma_n(1)$	$\pi+\gamma_n(2)$	$2\pi-\gamma_n(6)$
6	$\gamma_n(6)$	$\pi-\gamma_n(6)$	$\pi+\gamma_n(5)$	$2\pi-\gamma_n(2)$

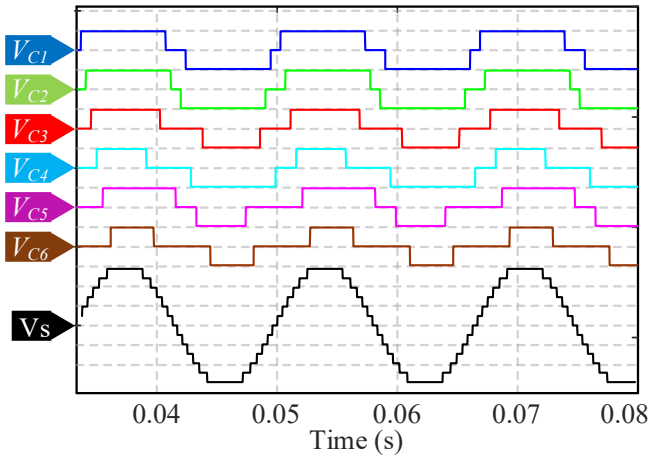


Figure 2.22 – Cells 1 to 6 output voltage and SMPA's output voltage for a RL load

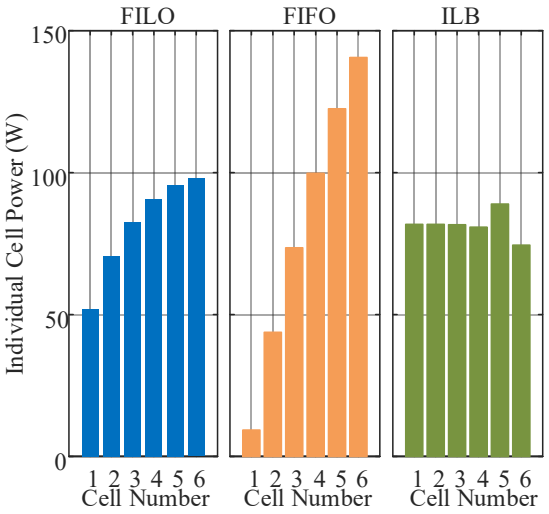


Figure 2.23 – Power consumption by cell with traditional (FILO and FIFO) and proposed modulation technique (ILB) for a RL load

2.5. Conclusion

Series type Hybrid Power Amplifiers (HPAs) offer a good trade-off between cost and performance. While the Switch-Mode Power Amplifier (SMPA) processes the bulk of the output power, the Linear Power Amplifier (LPA) mitigates harmonic distortions and provides fast tracking of the reference output voltage waveform. SMPAs consisting of Cascaded H-Bridge Multilevel (CHBM) converters operating with staircase modulation are a great choice for high voltage and/or frequency applications due to reduced switching losses. However, conventional staircase techniques lead to highly unbalanced power demands and stress on the CHBM cells, mostly for low modulation signals.

A technique that mitigates this issue, called Split-Voltage First-In First-Out (SV-FIFO), has been proposed and experimentally validated in steady state and dynamic conditions. For on-line dynamic operation, it requires suitable estimation of the magnitude and frequency of the reference output voltage, which was performed using a technique detailed in Chapter 4. In addition, a design approach and experimental verification of a series type HPA based on a CHBM multilevel converter operating with FILO, FIFO and SV-FIFO was presented. The design approach includes the sizing of the SMPA and of a voltage slew rate limiter in accordance with the voltage ratings and slew rate of the LPA. An isolated analog controller, with feedforward of the SMPA voltage, was devised for a commercial LPA (AE Techron 5050LVC). The gating signals of the SMPA with SV-FIFO are generated by means of a digital controller (OPAL-RT OP4510). Experimental results

for the HPA operating under a wide range of output voltages (35 Vrms - 220 Vrms) and frequencies (60 Hz – 1 kHz) were presented. They show the expected voltage waveforms for the SMPA and LPA, leading to a high quality sinusoidal output voltage. The enhanced power-balancing feature of SV-FIFO was verified experimentally. Dynamic tests with step variations in the magnitude and frequency of the reference output voltage demonstrate that the modulation scheme of the SMPA, implemented in a digital controller, and the isolated analog controller of the LPA allow fast tracking of the reference output voltage with no saturation of the LPA.

After a comprehensive study of traditional modulation techniques for Cascaded H-Bridge Multilevel (CHBM) converter based on the Nearest Level of Control (NLC), the issue of unbalanced power between cells was observed, and it varies for different load characteristics (RC, R, RL). The proposed solution, which still respects the constraints and switching angles given by the NLC, improves the power balance between the cells for all linear load characteristics. The novelty is based on the analysis for all load profiles, in terms of load angle, varying from -85° to 85°. The algorithm and overall system was detailed and its main aspect relies on generating turn on and off angle combinations that will consume power closer to the average power consumption. Simulation results of the proposed method were carried out to evaluate the effectiveness and impact of the proposed technique for a RC and a RL load. The results found with ILB, improve the power balance, presenting a much lower standard deviation than the other techniques for all the range of load angles, with the additional cost of a higher computational burden and the need to read or sense the output current.

3. STUDY OF A PARALLEL HPA

3.1. Introduction

Machine emulation (ME) is one of the main applications of Power-Hardware-In-the-Loop (PHIL). The performance of an emulator depends heavily on the type of Power Amplifier (PA) it employs. Linear Power Amplifiers (LPAs) produce ripple free outputs and offer high bandwidths but are costly. Switch-Mode Power Amplifiers (SMPAs) are more affordable, with higher power density, but produce switching harmonics and present lower bandwidths. Hybrid Power Amplifiers (HPAs) can provide a trade-off solution bridging the two technologies. A series connected HPA was discussed in Chapter 2 for high voltage applications. This chapter is concerned with a parallel HPA, suitable for high current applications. In this case, the current sharing between the SMPA and LPA can be an issue. In principle, the LPA should provide the fast changing and high frequency components with the SMPA providing the bulk of the slow changing and low frequency components of the HPA current. A design procedure for the current control scheme of the parallel HPA is presented and illustrated for the emulation of an induction machine (IM) with typical laboratory equipment. One of the main targets of the proposed control scheme is to minimize the cost of the HPA, and for that, it is essential to minimize the current rating of the LPA. This is ensured by using the proposed control technique, where both the LPA and the SMPA operate with current control loops. The reference current of the HPA is that of the ME system, computed by the Real-Time Simulator (RTS). The SMPA is controlled with a lower bandwidth (BW) current loop, using the actual (measured) HPA current as the reference value, in order to take over the current from the LPA, following a short transient. The LPA reference signal comes from the machine model itself. In steady state, the LPA inherently provides active power filtering for the SMPA, reducing the switching harmonic distortion of the ME system.

A design procedure for the control scheme of the HPA is presented and illustrated for the emulation of a direct on-line start-up of an Induction Machine (IM). Simulation results evaluate and compare systems built exclusively with SMPA or LPA for ME with the proposed HPA configuration. Experimental results are shown to validate the proposed control scheme for the parallel HPA in ME systems. Besides, the impact of the bandwidths of the control loops of the LPA and SMPA and the switching frequency of the SMPA, on the accuracy of the ME system and on the current requirement of the LPA are highlighted.

3.2. Machine Emulation and Real Time Simulators

An ME system consists essentially of a RTS, where the machine model is simulated, and a Power Amplifier (PA) that is connected to a physical motor drive or the utility system to emulate or replicate the machine terminals behavior according to either the instantaneous voltages applied to its terminals or to the drawn current lines. As discussed in Chapter 1, the most detailed machine models are of the voltage-in current-out type. They take voltage as input (v_{inv} in Figure 1.20) and output the machine reference current (i_{motor} in Figure 1.20) [65], [77]–[79]. A critical aspect of these models is that they need to present low computational burden for the RTS. The induction machine model used in this study accounts for machine induction variation due to saturation, which has been presented and validated against the physical machine in [64].

3.3. Detailing of Proposed System

This chapter discusses a Hybrid Power Amplifier (HPA), with parallel LPA and SMPA, for ME that offers a compromise solution with the benefits of both technologies. The LPA is to provide high bandwidth and active power filtering of the switching harmonics of the SMPA, which supplies the bulk of the current of the ME system. In order to minimize the costs, it is essential that the current ratings of the LPA be reduced. This can be achieved with a new control scheme where the reference value of the current control scheme of the LPA comes from the "machine model" while that of the SMPA, comes from the actual current flowing in the coupling impedance of the ME system. By making the bandwidth of the LPA (BW_{LPA}) higher than that of the SMPA (BW_{SMPA}), the first provides the fast changing current components while the second, the current of the ME system in steady state. The impact of the ratio BW_{LPA}/BW_{SMPA} and the switching frequency of the SMPA (f_{sw}) on the current to be supplied by the LPA (i_{LPA}) as well as the distortion/ripple of the emulated machine current (i_{motor}) are also investigated.

3.3.1. Proposed System: HPA Topology and Control

A Hybrid Power Amplifier (HPA) as shown in Figure 3.1, will be used in an ME system concerning an induction machine directly connected to an AC grid. The LPA is connected directly to the coupling impedance, L_{coup}, while the SMPA is connected to the same node through another impedance L_{SMPA}. There are isolation transformers in both grid sides of the LPA and SMPA to

prevent circulating currents. At the left side of L_{coup}, there is an autotransformer used to control and adjust the grid voltage, v_{TEST}, applied to the emulated induction machine.

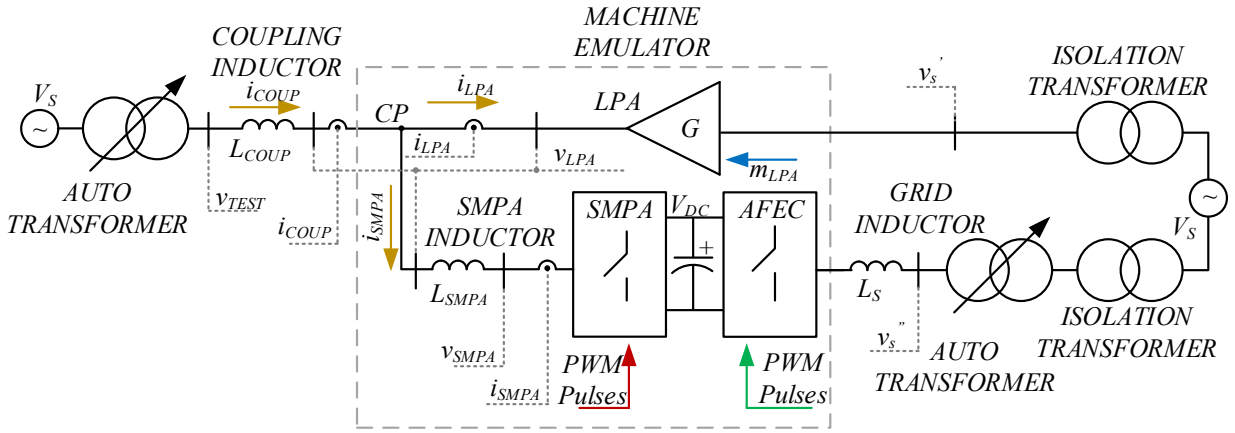


Figure 3.1 – Proposed machine emulator built with the parallel association of a SMPA and an LPA

The HPA is current controlled as shown in a simplified way in Figure 3.2, and in detail in Figure 3.3. Based on the sensed grid, or motor drive, voltage (v_{TEST}), the RTS computes the machine current, i_{COUP}*, to be synthesized by the HPA. The current i_{COUP}* is used as the reference for the LPA as in [19], determining the control signal of the LPA (m_{LPA}). The actual/sensed, i_{COUP} becomes the reference current for the SMPA, i_{SMPA}*. A current controller processes the current error and produces the modulating signal for PWM. The key requirement in the proposed scheme concerns the bandwidths of the current control loops of the LPA (BW_{LPA}) and SMPA (BW_{SMPA}). By making $BW_{LPA} > BW_{SMPA}$, the LPA reacts rapidly to synthesize i_{COUP}*, and the SMPA will eventually take over this task, providing the bulk of i_{COUP}*. As a result, in steady state, i_{LPA} will tend to be equal to only the error of the SMPA current control loop plus the switching current harmonics of the SMPA.

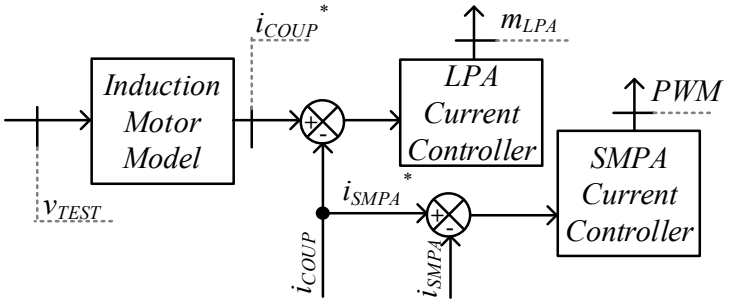


Figure 3.2 - Simplified control strategy for the proposed control system

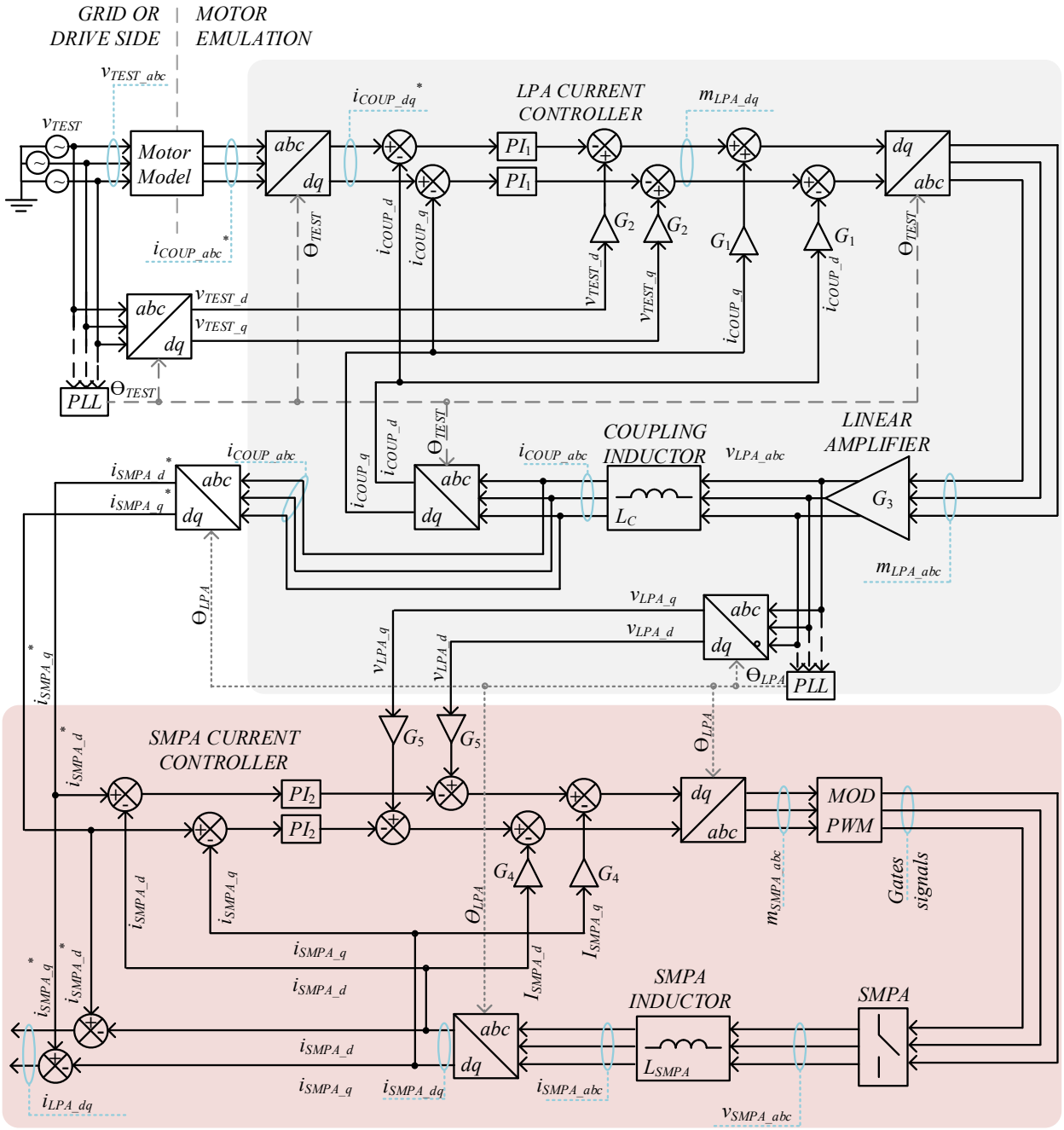


Figure 3.3 – Proposed current control scheme of the parallel HPA for machine emulation.

A realization of the proposed current control scheme of the HPA with three LPAs and a three-phase 6-switch VSC in the synchronous (*dq*0) reference frame is shown in Figure 3.3. At the top left, one can see the sensed three-phase voltage, v_{TEST_abc}, that is used by the RTS for computing the machine current, i_{COUP_abc}*, according to the machine model. The current control scheme of the LPA, on the grey region of Figure 3.3, is the same one used in [19], with a simple PI controller

(PI_1). The rotating frame angle, θ_{TEST}, is obtained from v_{TEST_abc} using a conventional PLL. The three-phase machine reference current, i_{COUP_abc}*, at the top left of Figure 3.3, is converted into $dq0$, i_{COUP_dq}*. These two signals are compared with the actual/sensed coupling inductance currents converted into $dq0$, i_{COUP_d} and i_{COUP_q}, and the error is fed to a PI controller. The current error in $dq0$ should be zero in steady state. Feedforward signals are added to the output of the PI controller to cancel the cross-coupling terms of the d and q equivalent circuits. Considering that the LPA operates as a voltage source with a constant voltage gain (G_3) [25], the gains of the feedforward paths are $G_1 = \omega L_{COUP}/G_3$ for i_{COUP_d} and i_{COUP_q} and $G_2 = 1/G_3$ for v_{TEST_d} and v_{TEST_q}. The resulting signals in $dq0$ are transformed back into abc and then used as the control signals for the three LPAs, one for each phase.

The current control scheme of the SMPA is shown at the bottom of Figure 3.3, in the light red region. The goal is to control the current flowing through L_{SMPA}, i_{SMPA_abc}, between the three-phase SMPA and the output of the three LPAs, node CP. It is also based on a rotating reference frame, but it employs angle θ_{LPA}, synchronized to the output voltage of the LPA. The reference current for the SMPA in $dq0$, i_{SMPA_d}* and i_{SMPA_q}*, are obtained from sensed i_{COUP_abc} using angle θ_{LPA}, as shown at the top right of Figure 3.3. The error between i_{SMPA_dq}* and i_{SMPA_dq} is fed to a PI controller (PI_2). As for the LPA current control loop, feedforward signals are added to the output of PI_2. For a three-phase VSC with a voltage gain $G_6 = V_{DC}/2$, where V_{DC} is the DC bus voltage of the VSC, the feedforward gains are $G_4 = \omega L_{SMPA}/G_6$ for i_{SMPA_d} and i_{SMPA_q} and $G_5 = 1/G_6$ for v_{LPA_d} and v_{LPA_q}. The resulting signals of the current control loop in $dq0$ are converted back to abc using angle θ_{LPA} to obtain the modulating signals for generating the gating signals of the SMPA with Sinusoidal Pulse-Width Modulation (SPWM).

3.4. Control & System Design

The schematic shown in Figure 3.4 will be used to find the minimum requirements for v_{LPA}, v_{SMPA} and V_{DC}. To start with, one needs the maximum input voltage of the machine to be emulated, v_{TEST}. The line current drawn by the emulated machine is the same that will flow through L_{COUP}, hence it will be called i_{COUP}. The current will have a phase when compared to V_{TEST}, which can have any value from 0 to 2π, hence the 4Q capacities of the system. It is very important to consider that the ME must be designed for start-up and transient conditions, not only for steady state. This

is reflected mainly on i_{COUP}, since this current must consider the maximum value for peak condition during start-up of an induction machine (between 7 and 10 times the rated current).

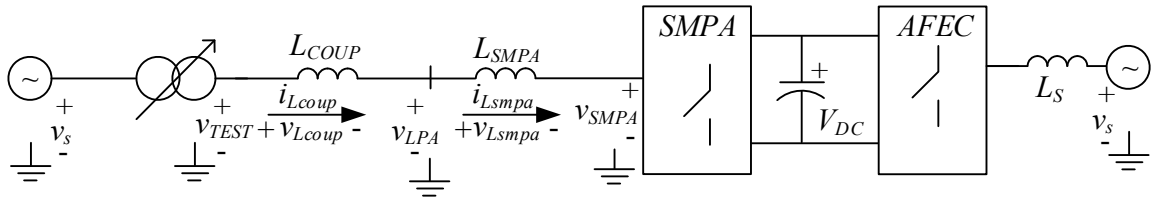


Figure 3.4 – Schematic of the HPA-ME used for v_{LPA}, v_{SMPA} and V_{DC} design.

3.4.1. LPA and SMPA Voltage Definition

Equations (3.1) to (3.6) represent the step-by-step approach to determine the LPA output voltage requirement, based on the schematic shown in Figure 3.4, using the second voltage loop (the first is irrelevant to the study). The current i_{COUP} for this case must be the maximum rms current during start-up. A Safety Margin, *SM*, must be used in (3.6) to ensure that the LPA will not saturate if a higher voltage is required during transient conditions. The parasitic resistance of the inductor is not considered. The polarities of the voltages and direction of the current are shown in Figure 3.4, where $\hat{v}_{LPA}$ is the maximum voltage requirement from the LPA.

$$-v_{TEST} + v_{Lcoup} + v_{LPA} = 0 \tag{3.1}$$

$$v_{LPA} = v_{TEST} - v_{Lcoup} \tag{3.2}$$

$$v_{LPA} = v_{TEST} - L_{COUP}\frac{di_{coup}}{dt} \tag{3.3}$$

where v_{TEST} is the time-variant phase voltage of the machine model

v_{Lcoup} is the time-variant voltage drop across L_{COUP}

v_{LPA} is the time-variant phase voltage requirement from the LPA

L_{COUP} is the coupling inductance between grid and machine emulator

i_{COUP} is the time-variant current of the machine model

The plus/minus signal is considered in (3.5) due to the possibility of the i_{COUP} to be in any phase when compared to v_{TEST}, since the 4Q capacities of the system.

$$\hat{v}_{LPA} = \hat{v}_{TEST} - L_{COUP}\frac{d\hat{\imath}_{coup}}{dt} \tag{3.4}$$

$$\hat{v}_{LPA} = \hat{v}_{TEST} \pm L_{COUP}\hat{\imath}_{coup}\omega \tag{3.5}$$

$$\hat{v}_{LPA} \geq SM\left[\hat{v}_{TEST} \pm L_{coup}\hat{\imath}_{coup}\omega\right] \tag{3.6}$$

where $\hat{v}_{LPA}$ is the peak phase voltage requirement from the LPA

$\hat{v}_{TEST}$ is the peak phase voltage of the machine model

$\hat{\imath}_{coup}$ is the peak current of the machine model

SM is the chosen safety margin for the LPA

ω is the highest angular speed required by the model ($2\pi f_{max}$)

By using the third voltage loop shown in Figure 3.4, it is possible to determine the minimum requirements for the SMPA peak output voltage, $\hat{v}_{SMPA}$. Equation (3.7) to (3.10) represent the systematic approach for determining it.

$$-v_{LPA} + v_{Lsmpa} + v_{SMPA} = 0 \tag{3.7}$$

$$-v_{TEST} + v_{Lcoup} + v_{Lsmpa} + v_{SMPA} = 0 \tag{3.8}$$

$$v_{SMPA} = v_{TEST} - v_{Lcoup} - v_{Lsmpa} \tag{3.9}$$

$$\hat{v}_{SMPA} = \hat{v}_{TEST} - L_{coup}\frac{d\hat{\imath}_{coup}}{dt} - L_{smpa}\frac{d\hat{\imath}_{smpa}}{dt} \tag{3.10}$$

where v_{SMPA} is the time-variant phase voltage requirement from the SMPA

$\hat{v}_{SMPA}$ is the maximum phase voltage requirement from the SMPA

v_{Lsmpa} is the time-variant voltage drop across L_{SMPA}

L_{SMPA} is the inductance between SMPA and coupling network

$\hat{\imath}_{smpa}$ is the peak current of the SMPA

Considering that the SMPA will end up sinking the fundamental component of the coupling current $i_{COUP} = i_{SMPA}$. Equations (3.11) and (3.12) represent the system using the same current, showing the required fundamental peak voltage requirement for the SMPA. The plus/minus signal is considered due to the possibility of the i_{COUP} to be in any phase when compared to v_{TEST}.

$$\hat{v}_{SMPA} = \hat{v}_{TEST} - \left(L_{COUP} + L_{smpa}\right)\frac{d\hat{\imath}_{coup}}{dt} \tag{3.11}$$

$$\hat{v}_{SMPA} = \hat{v}_{TEST} \pm \left(L_{COUP} + L_{smpa}\right)\hat{\imath}_{coup}\omega \tag{3.12}$$

Considering a two level, three-phase inverter, the DC bus requirement for SPWM can be found using (3.13). For other switching techniques, such as space vector modulation, the DC bus requirement can be approximately 15% smaller.

$$V_{DC} \geq 2\hat{v}_{SMPA} \tag{3.13}$$

3.4.2. Coupling Inductor Design Considerations

An inductor is usually employed to couple two AC voltage sources, such as in grid connected Voltage Source Converters (VSCs). Considering that the VSC switches at a finite frequency, there are switching voltage harmonics in their AC side, what will lead to current harmonics injected into the grid. These can be attenuated by a "large enough" coupling inductor. One common approach is to select the coupling inductor so that it limits the magnitude of the dominant current harmonic (I_h) to a percentage (k) of the rated fundamental current of the VSC according to

$$L_{coup} \geq \frac{V_{SVC\_h}}{h\ \omega\ k\ I_{SVC\_rated}} \tag{3.14}$$

where V_{SVC_h} is the rms value of the dominant voltage harmonic of the VSC

ω is $2\pi f_1$, the frequency of the AC grid in rad/s

h is the order of the harmonic (f_h / f_1)

I_{SVC_rated} is the rated current of the VSC

It is evident that one can reduce the size of the coupling inductor by increasing the switching frequency. However, this will lead to an increase in the switching losses. Conversely, a low switching frequency will require a large coupling inductor, which in turns will lead to a higher DC bus voltage for the VSC as discussed in Section 3.4.1. Therefore, a trade-off needs to be considered when selecting a coupling inductor.

In the particular case of the parallel HPA, as shown in Figure 3.4, two coupling inductors are required. L_{coup}, between the AC grid and the LPA and L_{SMPA} between the LPA and the SMPA. In principle, since the LPA does not produce any switching harmonics, L_{coup} could be made "small"

while L_{SMPA} would be sized to take the bulk of the attenuation of the harmonic currents injected by the SMPA into the AC grid. On the other hand, the LPA that is controlled to synthesize I_{Lcoup} as discussed in Section 3.3.1, should also be able to assist as an active power filter. For that, its output impedance at the frequency range of the switching harmonics of the SMPA should be lower than that of L_{coup}. Thus, using a larger than minimal value for L_{coup} can be beneficial for reducing the overall coupling inductances, $L_{coup} + L_{SMPA}$, required for the series type HPA.

Considering the phasor diagram in Figure 3.5, it is possible to visualize the maximum range of V_{LPA}, the RMS value of v_{LPA}. The LPA output voltage must withstand or be able to output any voltages inside the upper circle. The worst condition is generated by an I_{COUP} lagging V_{TEST} from 90°, which will cause V_{Lcoup} to be in phase with V_{TEST}, requiring the highest V_{LPA}, based in (3.6). The same analysis can be extended to V_{SMPA}, as presented in (3.12). Both equations are represented in the phasor diagram of Figure 3.5, with the slight change from peak to RMS values.

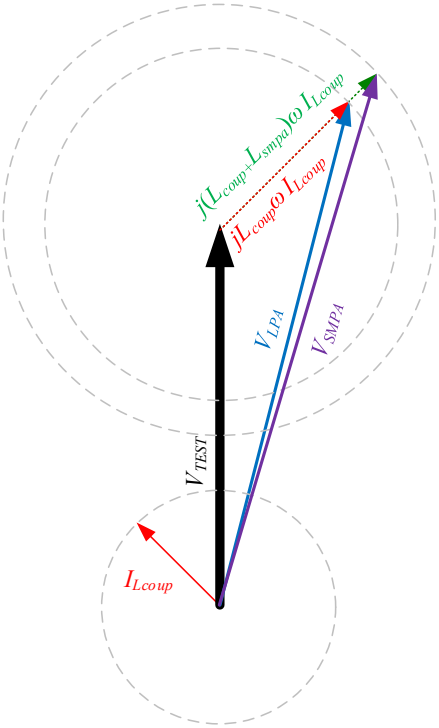


Figure 3.5 – Voltage and current phasors to assist on the V_{LPA}, V_{LPA}, L_{COUP} and L_{SMPA} determination with one example

3.4.3. Minimum Required HPA Bandwidth

The chosen model [64], [75] to validate the proposed system and control strategy is an "*5 HP machine with a stator resistance of 0.9649 Ω and a stator leakage inductance of around 5 mH,*

which results in a time constant of around 5 ms". In other terms, following a step change in the input/grid voltage, the input machine currents would present a transient response corresponding to a first order plant with a time constant of 5 ms. Therefore, the HPA should be able to synthesize a current with this characteristic with enough accuracy. The time constant for an induction machine is given by (3.15), as a function of the stator leakage inductance, L_{ls} and the stator resistance, R_s.

$$\tau_{ind} = {}^{L_{ls}}/_{R_s} \tag{3.15}$$

Figure 3.6 represents an ideal step, in blue, and a transfer function with a time constant of 5 ms, in red, as described in (3.16) in S-domain and (3.17) in time-domain. The 5 ms time constant corresponds to a signal bandwidth of 200 rad/s or 31.83 Hz. Now the signal with the time constant of 5 ms will be used as the input for another block that will try to recreate that signal. These blocks will simulate the closed loop bandwidth of the HPA, as in (3.18), by utilizing corresponding input-output transfer functions, modeled in S-domain. Equation (3.19)-(3.21) represents the ME transfer functions, considering the dynamics from the model and the limitations from the HPA controller.

$$S_\tau(S) = \frac{1}{s\tau + 1} \tag{3.16}$$

$$S_\tau(t) = 1 - e^{-t/\tau} \tag{3.17}$$

$$S_{HPA}(S) = \left(\frac{1}{s\,{}^{\tau}/_{k} + 1}\right) \tag{3.18}$$

$$S_{ME}(S) = S_\tau(S)\, S_{HPA}(S) = \left(\frac{1}{s\tau + 1}\right)\left(\frac{1}{s\,{}^{\tau}/_{k} + 1}\right) \tag{3.19}$$

$$S_{ME}(S) = \left(\frac{k}{s(s\tau + 1)(s\tau + k)}\right) \tag{3.20}$$

$$S_{ME}(t) = e^{-kt/\tau(k-1)} - ke^{-t/\tau(k-1)} - 1 \tag{3.21}$$

In Figure 3.7, several control bandwidths were tested in simulation, from 1.5x to 80x, which corresponds from 47 to 2,546 Hz. The higher the control bandwidth (and ratio with the input signal bandwidth), the closer the output signal is to the given reference. In Figure 3.8 a zoomed area is presented, from Figure 3.7.

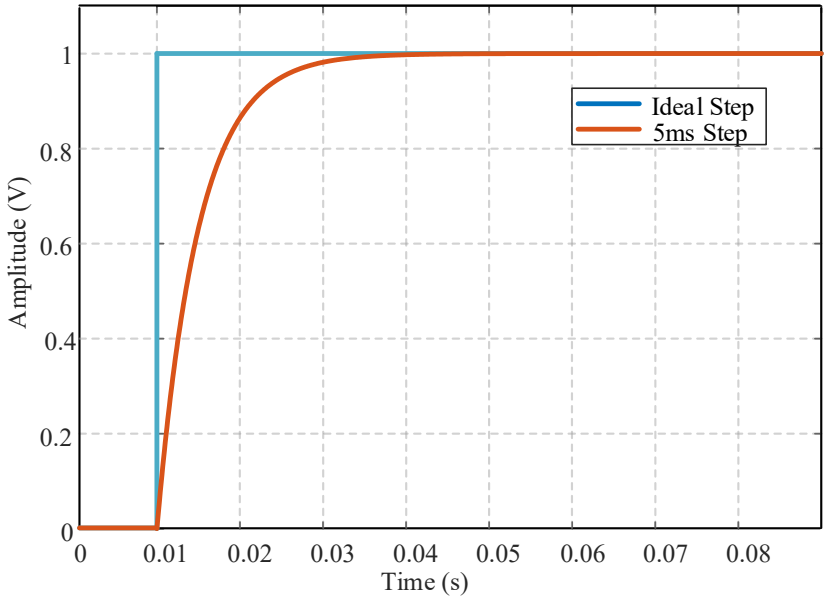


Figure 3.6 – Ideal step response (blue), the machine emulator equivalent response for a τ_{ind} = 5 ms (red)

One possible way to evaluate the speed of response and accuracy of the multiple control bandwidths is to compare each output to the reference (τ_{ind} = 5 ms) signal, by evaluating the error between them, as in (3.22), manipulated from (3.16) and (3.21).

$$Err_{ME}(t) = S_{\tau}(t) - S_{ME}(t) = ke^{-t/\tau(k-1)} - e^{-kt/\tau(k-1)} - e^{-t/\tau} \tag{3.32}$$

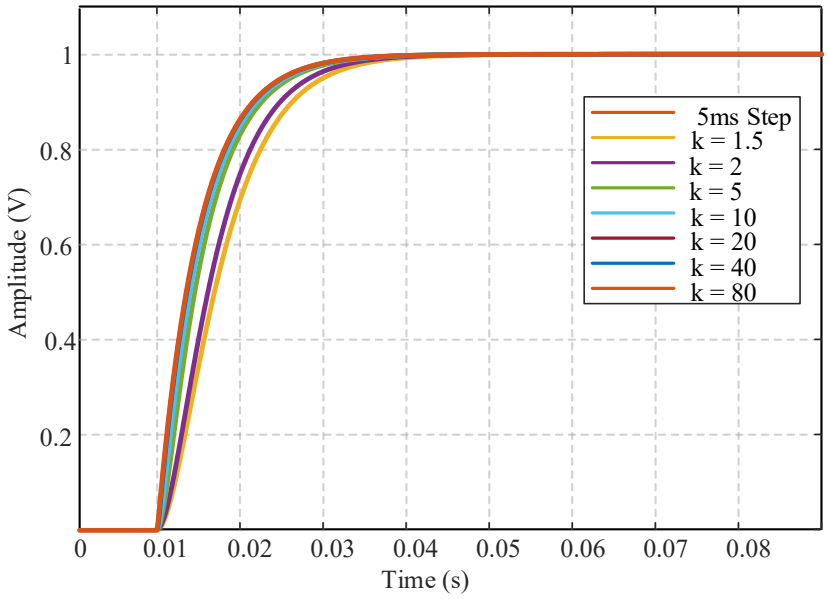


Figure 3.7 – The machine emulator equivalent response for a τ_{ind} = 5 ms and multiple outputs controller blocks with diverse bandwidth

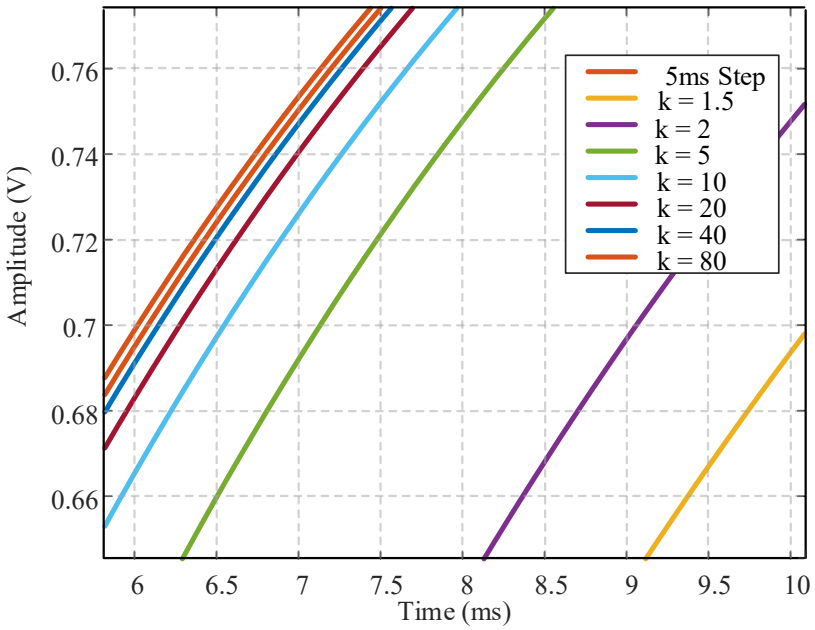


Figure 3.8 – Zoomed region of Figure 3.7

In order to find the appropriate minimum bandwidth, a key target must be determined, which is the maximum error. For this application, by design choice, the control bandwidth must allow a maximum error of 2%, which is represented in (3.23). By solving the equation for k, it is possible to find the result as shown in (3.24). This represents a minimal bandwidth of 1.4 kHz that ensures error below the range of 2%. The error signals for a low k of 5 up to 80 are presented, including the recently defined target with $k = 45.8$. Bandwidth higher than 1.47 kHz will ensure a small error on the reference tracking not only for the machine model but also for any other use of the HPA system as power amplifier. Figure 3.9 presents the error plot for three different scenarios, a small k of 5, the minimum k that will result in the 2% error (3.34) and a k that will result in a bandwidth close to the limit of the proposed control and HPA, which will be discussed in the next section.

$$\max[Err_{ME}(t)]|_{\tau=0.005} \leq 0.02 \tag{3.23}$$

$$k \geq 45.8 \tag{3.24}$$

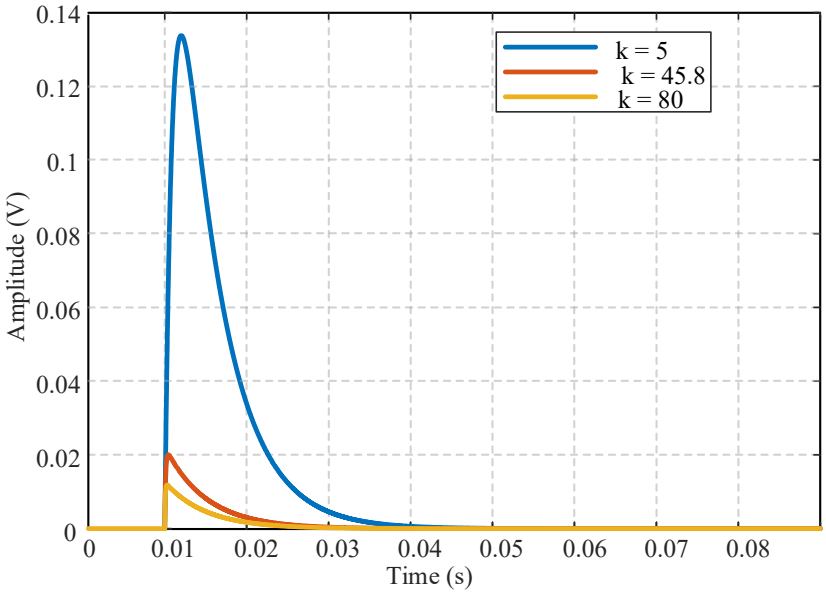


Figure 3.9 – Error between the machine emulator equivalent response for a τ_{ind} = 5 ms and multiple outputs controller blocks with diverse bandwidth

3.4.4. Control Design

The PI controllers for the current control loops of the LPA, SMPA are designed assuming that one loop will not interfere with the other. This is suggested by the fact that $BW_{LPA} > BW_{SMPA}$, by a factor of 2.5 or more. In general, the higher BW_{LPA}, the better one can track i_{COUP}^*. Likewise, the higher BW_{SMPA}, the faster the SMPA can relieve the LPA from providing the emulated machine current, thus reducing the peak current and the power the LPA has to supply.

This study, besides proposing the HPA with parallel LPA and SMPA and its associated control scheme for voltage-in and current-out machine models, intends to assess how the ratio BW_{LPA}/BW_{SMPA} and the switching frequency of the SMPA (f_{sw}) affect the current to be supplied by the LPA (i_{LPA}) as well as the distortion/ripple of the emulated machine current (i_{COUP}). For that, BW_{LPA} will be set at 2.7 kHz, which is the upper limit to keep the system stable (considering the further discussed phase and gain margins) for the given computation time of the RTS (T_c = 20 μs). Conversely, BW_{SMPA} will be varied, set at 150, 250 and 350 Hz, for switching frequencies of 1980, 3060 and 9960 Hz. Then, a specific case with BW_{SMPA} = 1000 Hz and f_{sw} = 9960 Hz will also be considered.

Next, a design approach for the current control loops is presented and exemplified for the emulation of the direct on-line start-up of an induction motor. The induction machine model is of

the voltage-in current-out type and includes main and leakage flux saturation as described in [64], [75] The chosen machine model has a time constant (3.25) of 5 ms.

The RTS used in this study is an OP4510 [74], from OPAL-RT, that has a computation time, $T_c = 20\ \mu$s, when the control action is performed on the CPU. The voltage and current sensors are the OP5511 [128], from OPAL-RT, with a time constant $T_f = 20$ µs. The LPA is an AE Techron 7548 [25], with a time delay $T_d = 500$ ns. Its gain in the voltage mode is fixed and set to $G_3 = 20$. As in [19] a coupling inductance $L_{COUP} = 4.15$ mH and an estimated resistance $R_{COUP} = 0.2\ \Omega$ was used. Concerning the SMPA, it presents a DC bus voltage $V_{DC} = 150$ V and a coupling inductance $L_{SMPA} = 2.482$ mH and estimated resistance $R_{SMPA} = 0.2\ \Omega$.

3.4.4.1. LPA Control Design

The simplified block diagram of the current control loop of the LPA, excluding the feedforward branches, is shown in Figure 3.10. There one sees that the RTS is modelled by a time-constant, T_c, with unity gain. The LPA is also modelled by a time-constant, T_d, and a gain, G_3. The model also includes the impedance of the coupling inductance: L_{COUP} in series with R_{COUP}. In the feedback path, the unity gain current sensor is also modelled by a time constant, T_f.

The parameters of the PI controller are calculated as $K_{p1} = 4$ and $K_{i1} = 80$ for a bandwidth of 2.7 kHz and a phase margin (PM) of 52°. The Bode plot of the compensated loop transfer function for the LPA is shown in Figure 3.11, where one can see that the design specifications are met. Table 3.1 summarizes the main parameters concerning the control loop of the LPA.

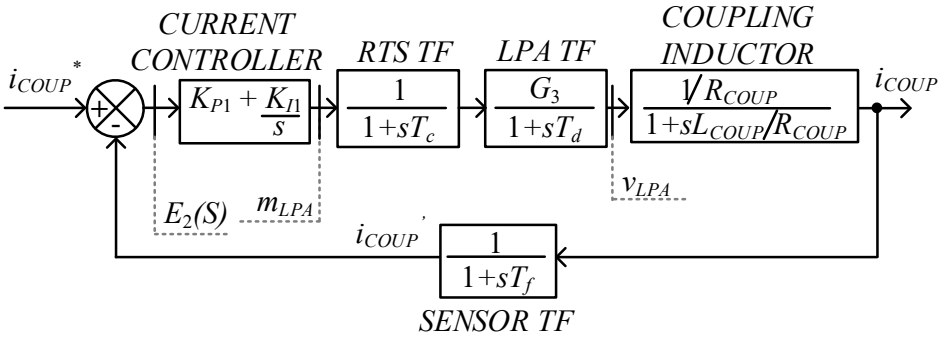


Figure 3.10 – Current control loop of the LPA

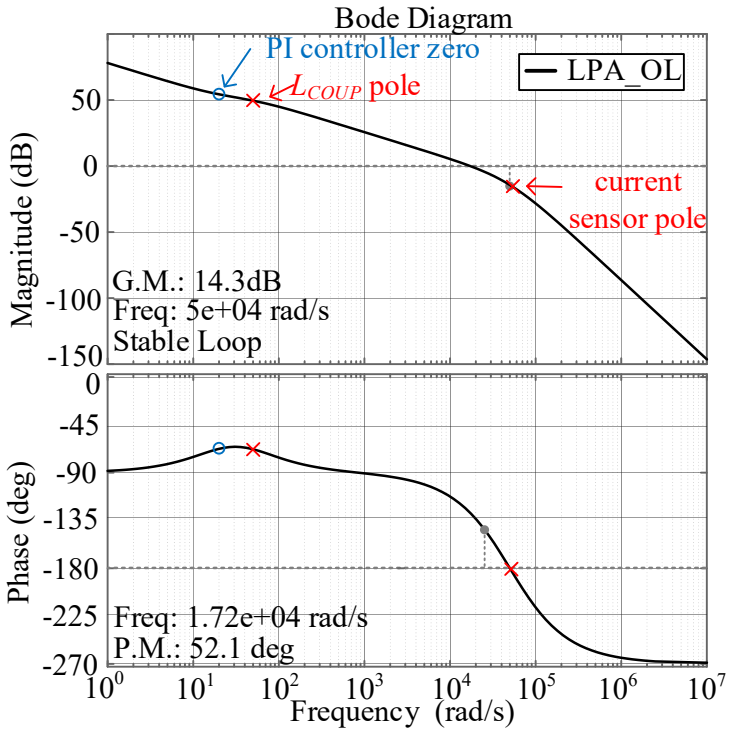


Figure 3.11 – Compensated loop transfer function of the LPA. BW_{LPA} = 2.7 kHz

Table 3.1 – Parameters for the design of the current control loop of the LPA

T_d	500 ns
T_c	20 µs
T_f	20 µs
L_{COUP}	4.15 mH
R_{COUP}	0.2 Ω
G_3	20
K_{p1}	4
K_{i1}	80

3.4.4.2. SMPA Control Design

The simplified block diagram of the SMPA is similar to that of the LPA, as shown in Figure 3.12. The main difference is on the model of the power amplifier. With a SMPA, the gain of the amplifier depends on the DC bus voltage $G_6 = V_{DC}/2$ and peak value of the carrier signal, V_m. The time constant varies with the switching frequency, $T_s = 0.5/f_{sw}$. The parameters of the PI controller are computed for the various intended operation conditions, BW_{SMPA} and f_{sw}, as previously mentioned and for a PM between 60 and 65°.

Table 3.2 summarizes the parameters concerning the control loop of the SMPA. Figure 3.13 shows the Bode plots of the compensated open-loop transfer function of the SMPA, which correspond to the cases of minimum and maximun BW_{SMPA} and f_{sw}. The Bode plots for the other operating conditions are between those two curves, with the expected *BWs* and *PM*.

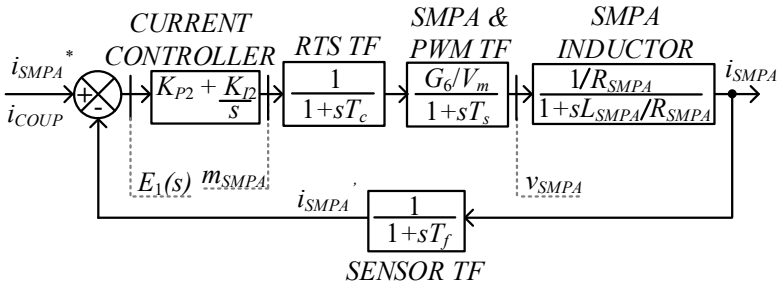


Figure 3.12 – Current control loop of the SMPA

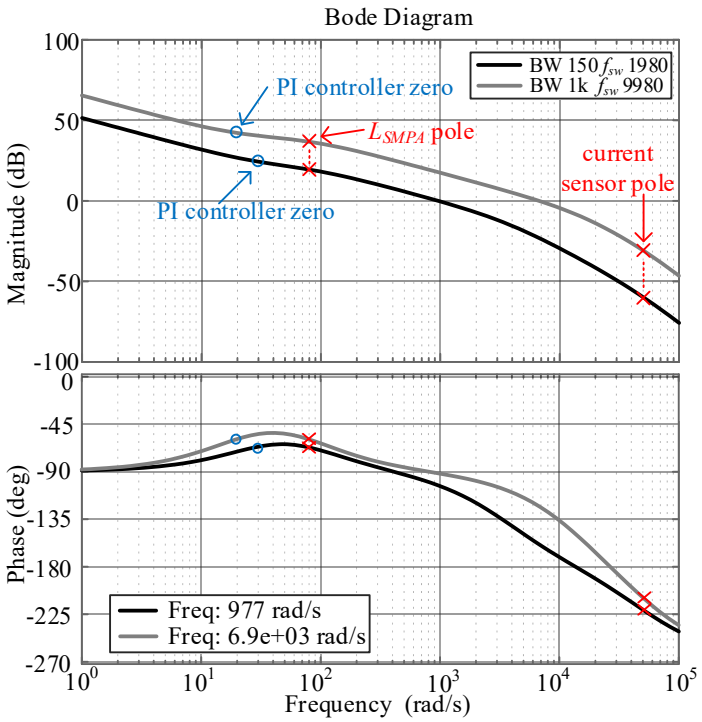


Figure 3.13 – Compensated loop transfer function of the SMPA. Black (BW_{SMPA} = 150 Hz, f_{sw} = 1980 Hz); Grey (BW_{SMPA} = 1 kHz, f_{sw} = 9960 Hz)

Table 3.2 – Parameters for the design of the current control loop of the SMPA

V_m	1 V			
T_c	20 µs			
T_f	20 µs			
L_{SMPA}	2.482 mH			
R_{SMPA}	0.2 Ω			
V_{DC}	150 V			
G_6	75 V (V_{DC}/2)			
V_{TEST}	80 V (line-rms)			
f_1	60 Hz			
f_{sw}	1980 Hz			
T_s	252.525 µs			
	1st Case	2nd Case	3rd Case	-
BW_{SMPA}	150 Hz	250 Hz	350 Hz	-
K_{P2}	0.033	0.056	0.0875	-
K_{I2}	1	1	1.75	-
f_{sw}	3060 Hz			
T_s	163.398 µs			
	4th Case	5th Case	6th Case	-
BW_{SMPA}	150 Hz	250 Hz	350 Hz	-
K_{P2}	0.033	0.05	0.075	-
K_{I2}	1	1	1.5	-
f_{sw}	9960 Hz			
T_s	50.2 µs			
	7th Case	8th Case	9th Case	10th Case
BW_{SMPA}	150 Hz	250 Hz	350 Hz	1000 Hz
K_{P2}	0.03030	0.0524	0.075	0.25
K_{I2}	1	1.75	1.5	5

3.5. Simulation and Comparison between SMPA, LPA and HPA as ME

This section will compare by simulation the implementation of the SMPA and LPA alone and its combination to build the HPA. Figure 3.14(a) and (b) show, in a very high level, the systems under evaluation with the SMPA and LPA. For the first, three bandwidths will be considered to evaluate how fast and accurately the SMPA can draw the emulated currents using L_{SMPA} as described in Table 3.2, as coupling element. For the last, only the highest bandwidth is considered, while using L_{COUP} as given in Table 3.1 as coupling element. The grid, test and bus voltages, control parameters and additional constrains are also the same described in Table 3.1 and Table 3.2. As a way to compare the systems, the maximum error between the reference and output signal will be evaluated.

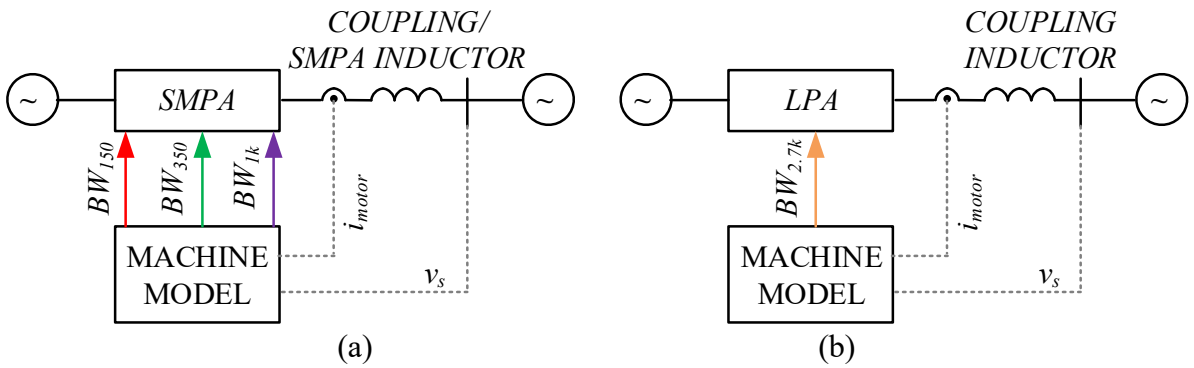


Figure 3.14 – High level systems under evaluation (a) SMPA as ME, (b) LPA as ME

For all following simulations the currents drawn from the machine emulator (either SMPA, LPA or HPA) will be evaluated based on an induction machine Direct On-Line (DOL) start-up considering a random turn on time of the grid signal (between 0 and 360°). The simulation uses the same machine model that will be further used on the experimental validation, available in [64]. Simulations are carried in the Matlab Simulink platform.

Figure 3.15, shows the reference current (in blue) for a DOL start-up and the currents drawn by the SMPA as ME, as shown in Figure 3.14(a). The red line represents the current drawn with the lower current closed loop control bandwidth of 150 Hz, the green represents the 350 Hz and the purple the 1 kHz. To achieve higher bandwidths, higher switching frequencies must be used and consequently higher will be the switching losses of the system, so a trade-off must be taken into account. For the simulations, the respective switching frequencies were used: 1980 Hz, 3060 Hz and 9960 Hz, respectively. It is clear that for lower bandwidths, the error at the start-up condition is significant, as shown in Figure 3.16, following the same color patterns.

The RMS value of the drawn currents, which will further be used as a comparison variable, is constant around 31 A, for any of the bandwidths. Even though the transient portion of the DOL for the given model takes roughly 0.25 s, the RMS value is calculated for the window of interest of 0.05s, because it is the most significant interval of interest for this application. The peak error between the drawn and reference current reached approximately 22 A for the lower bandwidth, 11 A for the middle bandwidth and 4 A for the higher.

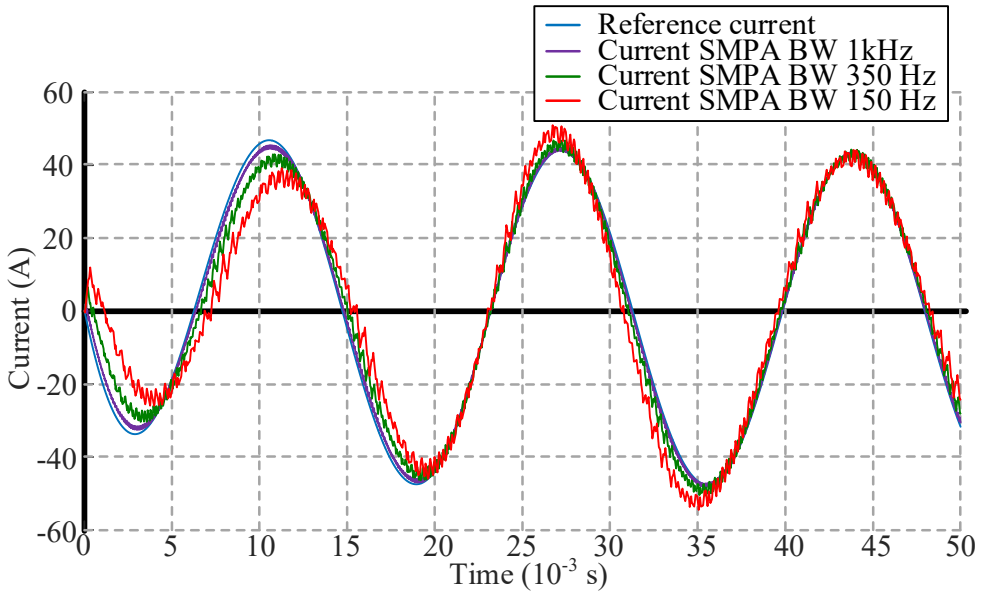


Figure 3.15 – Currents draw by the SMPA as ME with different bandwidths for an IM DOL start-up

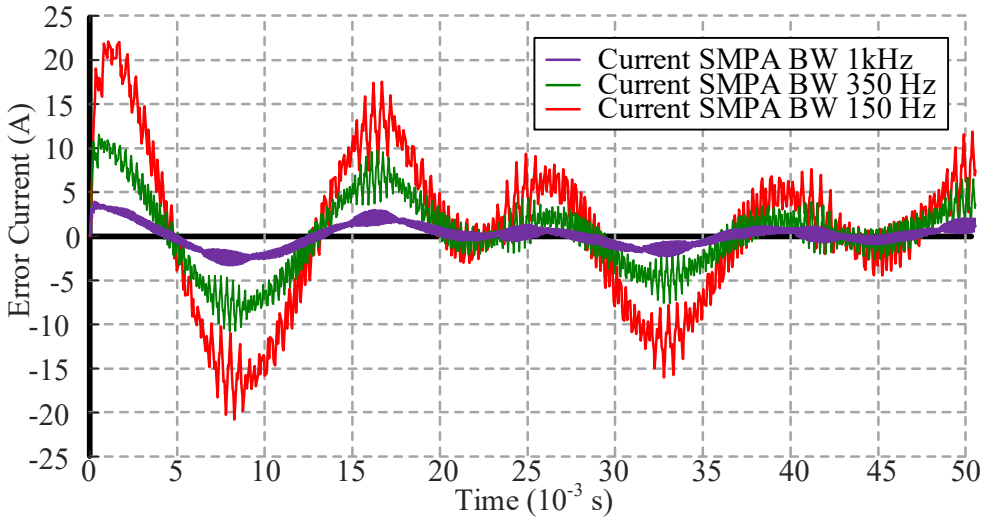


Figure 3.16 – Error in the currents draw by the SMPA as ME with different bandwidths for an IM DOL start-up

Considering the sole use of an LPA as ME, as indicated in Figure 3.14(b), Figure 3.17 shows the simulation of an IM DOL start-up. The current control bandwidth was set at 2.7 kHz, which is the limit for steady operation (phase margin of 52°, as previously described on the control design section). The drawn current of the LPA can be seen in the red waveform, while the reference is given by the blue waveform. It is effortless to see the higher speed and smaller error (shown in

Figure 3.18) of the LPA as ME. The RMS value of the drawn current for the LPA is approximately 31 A while the error between the drawn and reference current reached 1.2 A.

Including the previously mentioned in Chapter 1, price/kW for both systems, Figure 3.19 shows a comparison between the average cost for a SMPA, operating with 350 Hz bandwidth and 3060 Hz as switching frequency (in dark blue), LPA (dark red) and HPA (dark blue/red and orange) as ME.

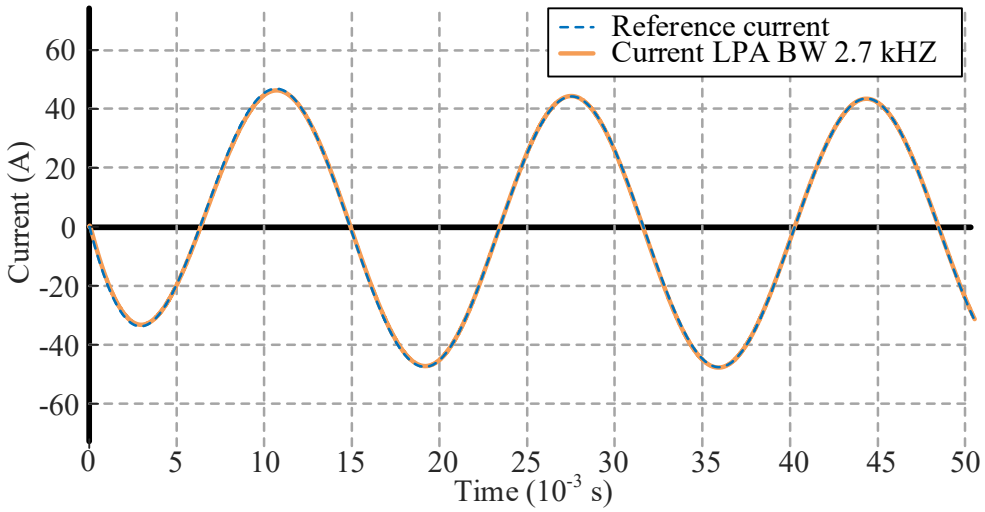


Figure 3.17 – Currents draw by the LPA as ME for a current control bandwidth of 2.7 kHz for an IM DOL start-up

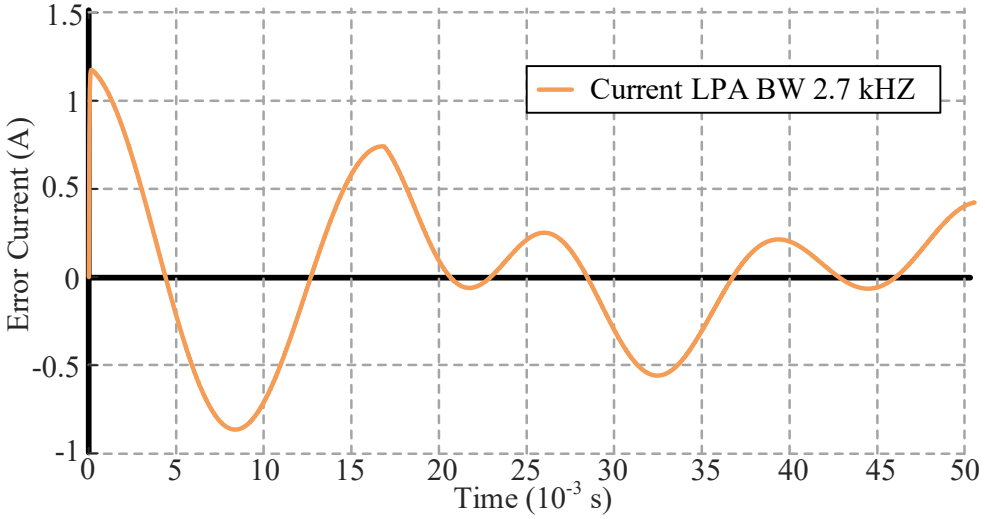


Figure 3.18 – Error in the currents draw by the LPA as ME for an IM DOL start-up

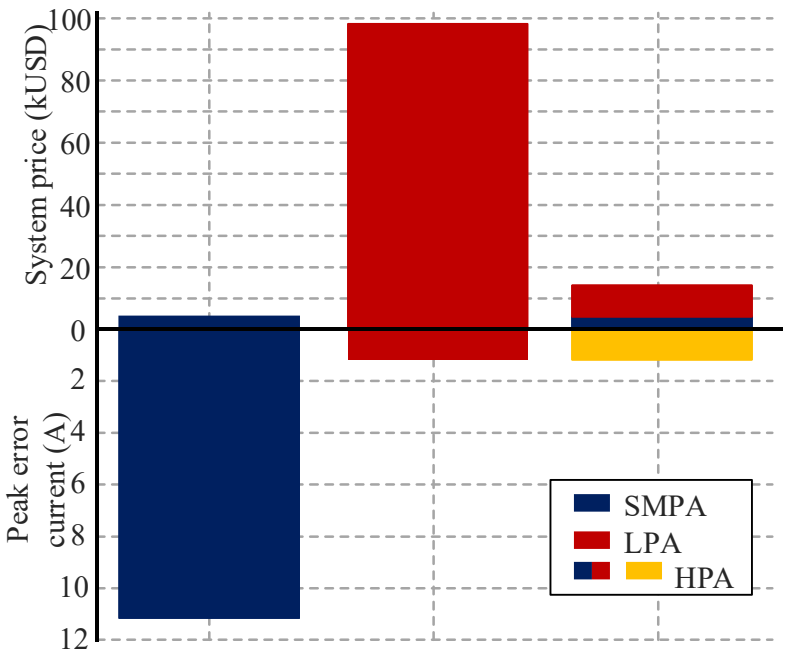


Figure 3.19 – Comparison of the cost and peak error current for ME built with SMPA (dark blue), LPA (dark red) and as the proposed HPA (dark blue/red and orange)

In the upper part of Figure 3.19, the power is calculated using the RMS currents and considers a three-phase system with 220 Vrms as line-to-line voltage and the price/kWh is then applied, using USD as currency. On the bottom part of Figure 3.19, the maximum or peak error in the drawn currents is displayed, directly linked to each system above.

It is clear that the SMPA as ME (dark blue) presents the lower cost with the highest error. On the other hand, the LPA as ME (dark red) presents the lower error at the higher cost, 25 times higher than the SMPA. The HPA solution on the other hand presents the same lowest error with a remarkable cost reduction when compared to the LPA. The simulations show that even with an average bandwidth on the SMPA, with balanced switching losses, the inclusion of a reduced current LPA can significantly increase the bandwidth of the system, decreasing the transient errors and crucially enhancing the quality of the output. This solution will be experimentally validated in the next section.

3.6. Experimental Results

3.6.1. Overall System

This section describes the experiments carried out with the proposed topology and control strategy of the HPA for ME. As a case study, the Direct On-Line (DOL) start-up of an induction motor was selected. The system is built using the same topology shown in Figure 3.1 and control strategy in Figure 3.3. The main objective is to demonstrate that with the proposed scheme, one can achieve a high bandwidth for the HPA with the LPA providing the emulated machine current during a short transient. Since LPAs typically have a maximum time during which they can supply a peak current, it is important to demonstrate that by selecting a "high enough" BW_{SMPA}, one can keep the peak current time of the LPA within allowed values. Another secondary aspect to be considered is the potential action of the LPA as Active Power Filter (APF) to the switching harmonics created by the SMPA. This helps keeping the current distortion of the HPA at low values. Figure 3.20 shows the experimental setup of the proposed HPA, consisting of parallel current controlled LPA and SMPA, for ME systems.

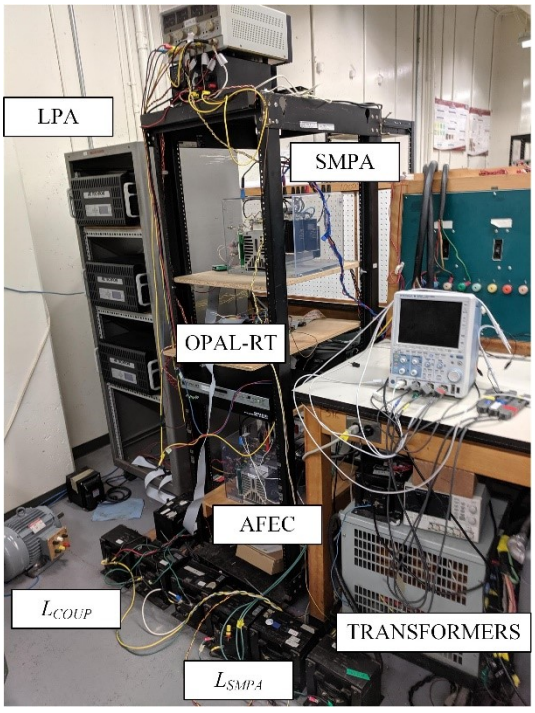


Figure 3.20 – Experimental setup for the proposed motor emulation system

In the exerimental setup, the LPAs are 4Q 7548 from AE Techron. The SMPA and its AFEC are built with two three-phase 6-switch IGBT VSCs (Semikron SemiTEACH). The results were

collected using a Yokogawa DLM3000 Mixed Signal Oscilloscope. All parameters for the experimental validation are presented in Table 3.1 and Table 3.2. A graphical user interface (GUI) and a protection interface was built using Matlab Simulink (running on the CPU of the OPAL-RT OP4510) to control and start-up all the subsystems. The ME system also contains an external analog protection circuit, which, if activated, will block all gating pulses for the switches. It monitors the DC bus voltage, between the AFEC and SMPA, and the currents of the SMPA, LPA and AFEC.

3.6.2. Lower SMPA Switching Frequency 1980 Hz – Cases 1 – 3

Figure 3.21 shows the reference current given by the machine model (i_{COUP}^*), in blue, during direct on-line start-up of an induction machine. The actual HPA current (i_{COUP}) is shown, in red, with its reference level shifted up to facilitate the comparison with i_{COUP}^*. The SMPA current (i_{SMPA}) is shown in green and the LPA current (i_{LPA}) in pink. The start-up time is not synchronized to the grid voltage and it varies accordingly with the phase angle of v_{TEST}. As a result, i_{COUP}^*, will not present necessarily the same waveform for the various tests. For all the experimental results CH1 is i_{COUP}, CH4 is i_{COUP}^*, CH2 is i_{SMPA} and CH3 is i_{LPA}. All vertical scales are 10 A/div, while the horizontal scale has the main window at 500 ms/div, Zoom1 at 10 ms/div and Zoom2 at 5 ms/div.

For the first case, Figure 3.21, f_{sw} = 1980 Hz and BW_{SMPA} = 150 Hz (a), 250 Hz (b) and 350 Hz (c). The ratio between i_{LPA} and i_{HPA} changes from 44.43% to 30.93% and finally to 23.62% with the increase of the BW_{SMPA}, showing that with a higher BW_{SMPA} the SMPA takes over the current from the LPA, faster. One can observe that, in the end, i_{LPA} decreases to about 0A, contributing only with the switching harmonic compensation due to the action of the SMPA. As expected, the SMPA takes over the task of providing the emulated machine current computed by the RTS. The current ripple in the waveform of i_{SMPA} can be easily observed on the second zoom window, in the steady state condition. It is mostly due to the switching harmonics, but there are also 5^{th} and 7^{th} harmonics created by the 5 µs dead-time used in the SMPA VSC. These harmonics however do not appear at the emulated machine current (i_{COUP}), due to the filtering action of the LPA.

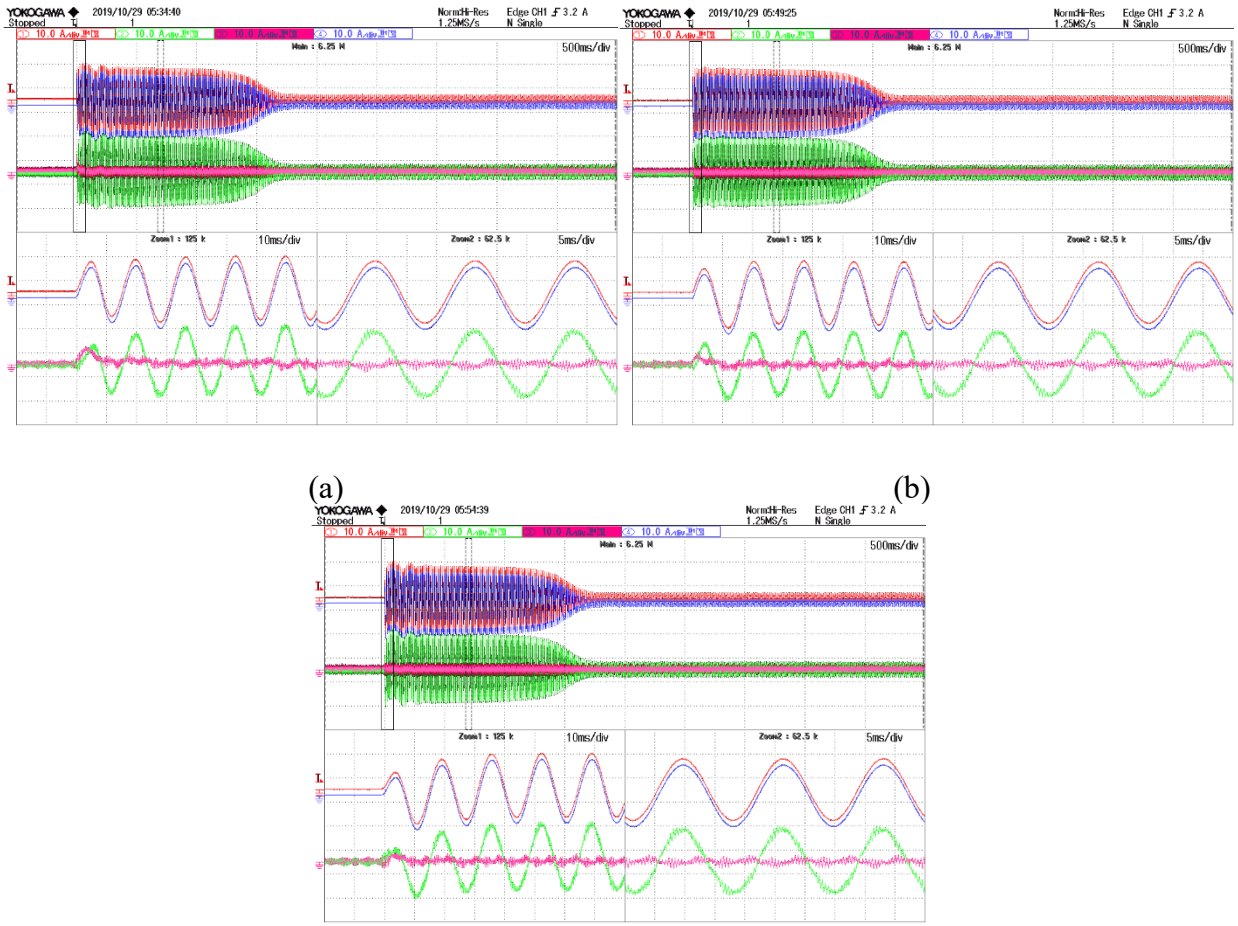


Figure 3.21 – Experimental results of the emulator response for an induction machine start up with f_{sw} 1980 Hz and BW_{SMPA} (a) 150 Hz (b) 250 Hz (c) 350 Hz

3.6.3. Intermediate SMPA Switching Frequency 3060 Hz – Cases 4 – 6

Presented in Figure 3.22, the second switching frequency is evaluated, with f_{sw} = 3060 Hz and BW_{SMPA} = 150 Hz (a), 250 Hz (b) and 350 Hz (c). The ratio between i_{LPA} and i_{HPA} changes from 43.19% to 27.27% and finally to 23.70% with the increase of the BW_{SMPA}. This improvement shows the benefits of a higher BW_{SMPA} to take over the LPA current faster and shows the positive impact, but still small, of increasing the switching frequency in reducing the ratio. As the BW_{SMPA} were the same as the first condition, the speed of the SMPA in taking over the current is similar.

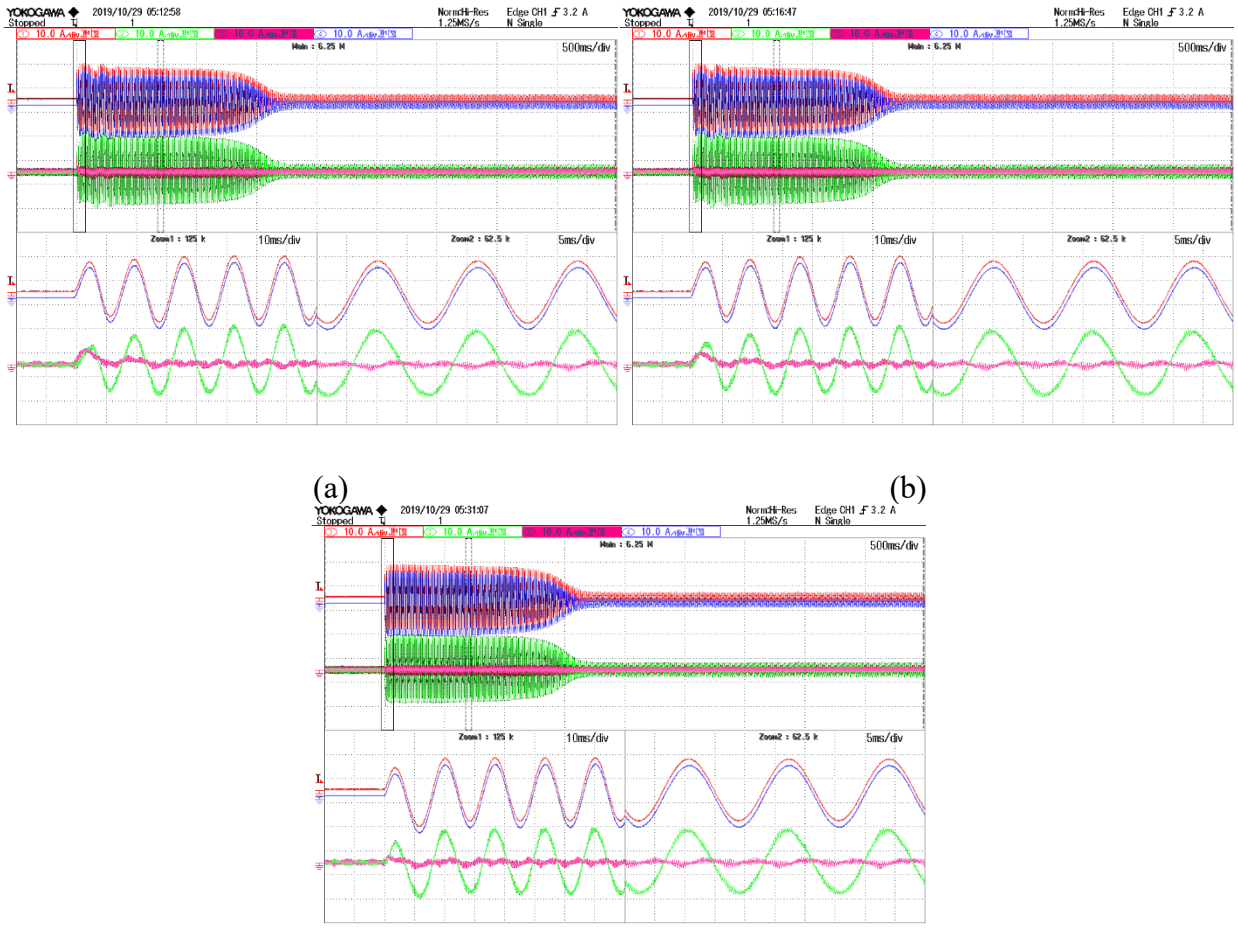


Figure 3.22 – Experimental results of the emulator response for an induction machine start up with f_{sw} 3060 Hz and BW_{SMPA} (a) 150 Hz (b) 250 Hz (c) 350 Hz

3.6.4. Higher SMPA Switching Frequency 9960 Hz – Cases 7 – 10

In Figure 3.23 the results are presented for the highest switching frequency under evaluation, f_{sw} = 9960 Hz. The bandwidths under analysis are BW_{SMPA} = 150 Hz (a), 250 Hz (b), 350 Hz (c) and 1000 Hz (d). The ratio between i_{LPA} and i_{HPA} changes from 41.76% to 12.10% at the last condition with the increase of the BW_{SMPA}. After the transient, i_{LPA} is consisted essentially of a small current ripple. These reductions are achieved due to the faster (2.7 times) response of the SMPA current control loop, in comparison with BW_{LPA}. In order to increase BW_{SMPA}, it is usually required to increase f_{sw}**.** In addition, due to the high f_{sw}, the ripple in i_{SMPA} is very small, but the LPA still prevents it from flowing to the input of the emulated machine. In general, one can

conclude that the actual contribution of the LPA in the proposed HPA for such a low (~ 2.7) ratio $BW_{LPA}/\ BW_{SMPA}$, is very small.

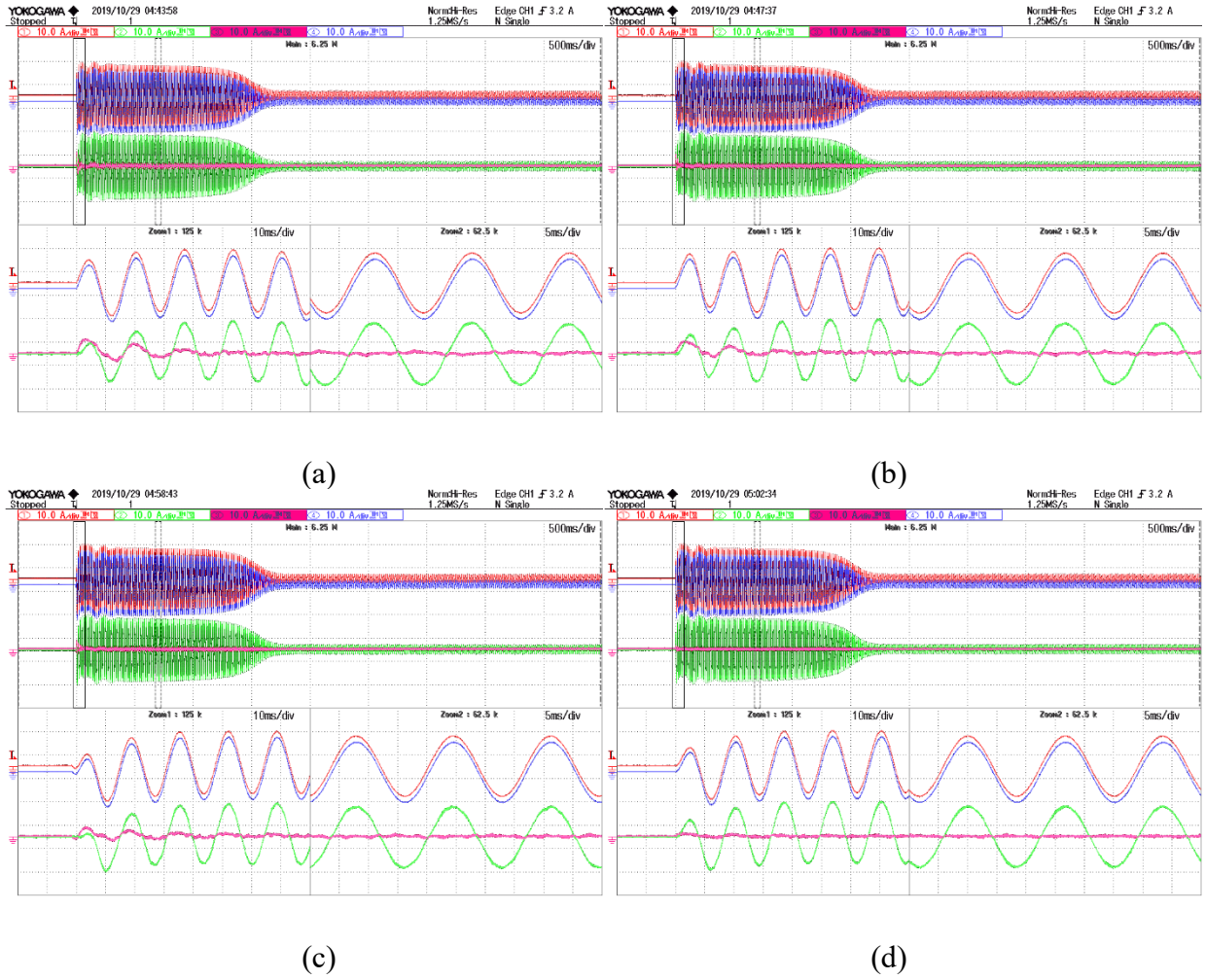


Figure 3.23 – Experimental results of the emulator response for an induction machine start up with f_{sw} 9960 Hz and BW_{SMPA} (a) 150 Hz (b) 250 Hz (c) 350 Hz (d) 1 kHz

3.7. Comprehensive Analysis of the Results

The feasibility of the proposed HPA for machine emulation, with parallel current controlled LPA and SMPA, has been demonstrated experimentally. It was also shown that, for a given BW_{LPA}, as one increases BW_{SMPA}, the peak value of i_{LPA}, during transients, decreases, what should allow the use of lower current and lower cost LPAs. However, to increases BW_{SMPA}, one needs to improve the harmonic spectrum of i_{SMPA}, so that the switching harmonics are sufficiently attenuated and the output signal of the PI controllers are virtually DC. This is usually achieved by increasing the switching frequency of the VSC. Actually, the rule-of-thumb of limiting the bandwidth of the

control loop to 10-20% of the switching frequency, or dominant harmonic, is frequently used in practice.

PI controllers for 10 different cases of BW_{SMPA} and f_{sw} were designed. Figure 3.24 shows how the ratio i_{LPA}/i_{HPA} varies with BW_{SMPA} and f_{sw}, for BW_{LPA} = 2.7 kHz and for the emulation of the DOL start-up of an induction motor with an electric time constant of 5 ms. There it is possible to observe that the BW_{SMPA} has a significant impact on the ratio i_{LPA}/i_{HPA}. In fact, for a high enough BW_{SMPA}, the ratio i_{LPA}/i_{HPA} becomes so low that an LPA becomes unnecessary. On the other hand, f_{sw} has a minimum impact. However, one should make sure that $BW_{SMPA} < 0.2\, f_{sw}$, as considered in this study.

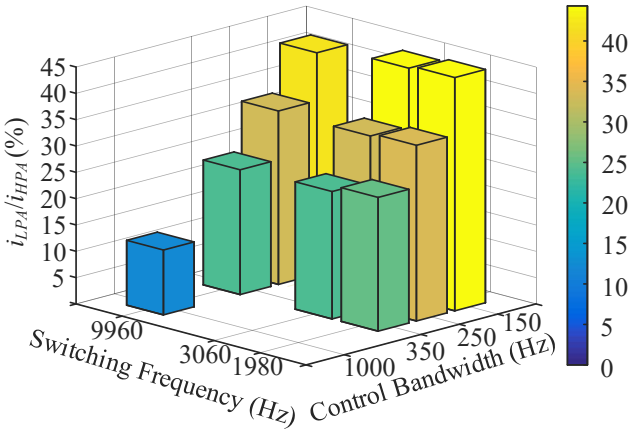
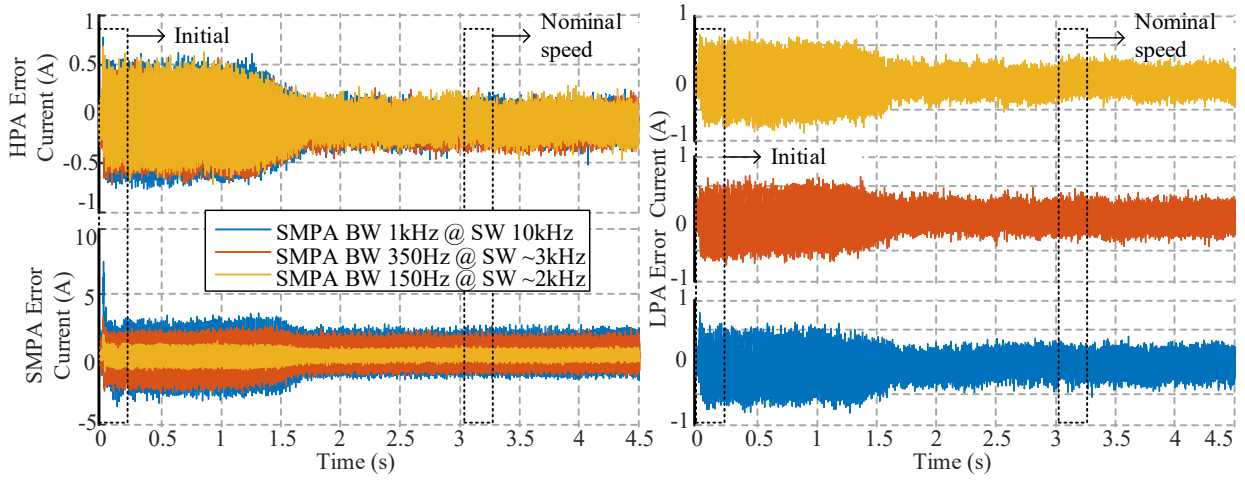


Figure 3.24 – Variation of i_{LPA}/i_{HPA} for all 10 considered cases of BW_{SMPA} and f_{sw}.

Figure 3.25 presents the analysis of the accuracy (or error) for the whole DOL start-up emulation, based on the experimental results presented in Figures 3.21-23, for the three bandwidths considered for the SMPA. Figure 3.25 presents the overall and complete DOL start-up accuracy, while Figure 3.26 will show the error at the beginning of the DOL and Figure 3.27 will show the error for steady state, after the IM has reached nominal speed. The qualitative analysis will be done over Figure 3.26 and Figure 3.27. In Figure 3.25(a) the HPA accuracy is evaluated (i_{COUP}* - i_{COUP}) in the top graph and the SMPA (i_{COUP}* - i_{SMPA}) in the bottom graph while Figure 3.25(b) presents the LPA (i_{COUP}* - i_{SMPA} - i_{LPA}) current accuracy.



(a) (b)

Figure 3.25 – Accuracy plot of experimental results (error between the drawn and reference currents) of the a) HPA, top, and SMPA, bottom; b) LPA

Considering the beginning of the DOL start-up, in the top graph of Figure 3.26(a), the HPA current error is measured by comparing the reference current i_{COUP}* with the HPA current (i_{COUP}). For all the SMPA's bandwidths, the error in the HPA current was always below 0.6 A and tends to zero after the transient (as it can be seen in Figure 3.27(a)), showing the high accuracy of the system. The results for the first comparison are similar and seem independent of the SMPA bandwidth. That can be explained because even though the SMPA is slower with slower bandwidths, the LPA bandwidth is high enough to compensate even for the worst case, with the lower SMPA bandwidth. These results are shown as the error of the LPA, which can also be understood as a residual error of the system. It is based on the difference between the i_{SMPA} error (i_{COUP}* - i_{SMPA}) and the LPA current LPA (i_{LPA}). It can be seen in Figure 3.26(b) the results for the LPA current error according to the three SMPA bandwidths reaching peak values around 0.5A, corresponding to approximately 2.5% of the HPA peak current of 20 A. The lower graph of Figure 3.26(a) shows the performance and accuracy of the SMPA (not alone, as a part of the HPA) based on the difference of the reference current i_{COUP}* with the SMPA current (i_{SMPA}). In this graph, it is possible to see the decreasing accuracy and higher error with the lower control bandwidths. Differently from the HPA current, the error in the SMPA never goes to zero because of the switching harmonics, as it can be seen in Figure 3.27(a). Lastly, it can be seen in Figure 3.27(b) the results for the LPA current error when the LPA is compensating only the switching harmonics generated by the SMPA.

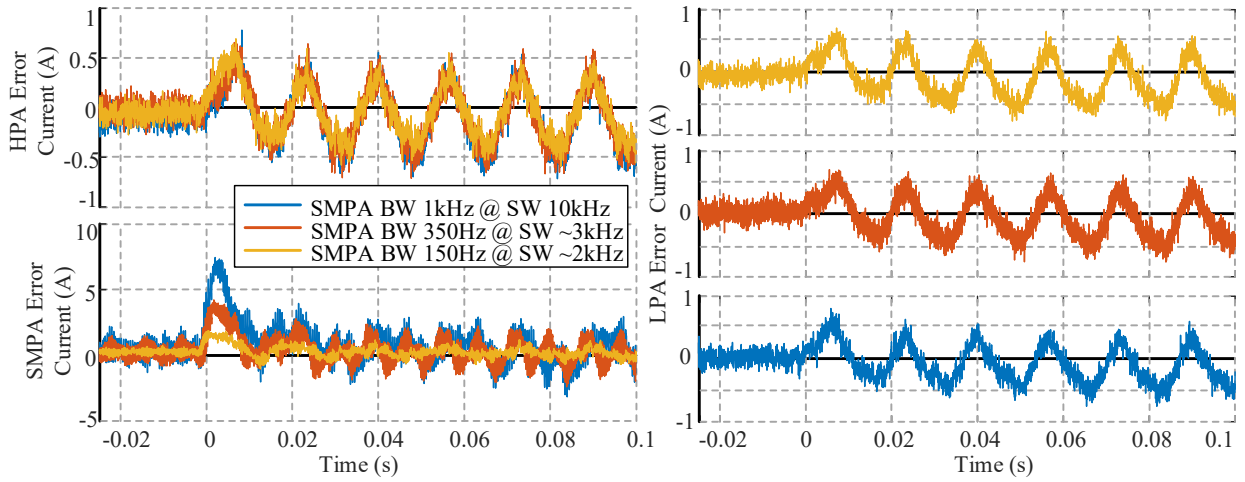
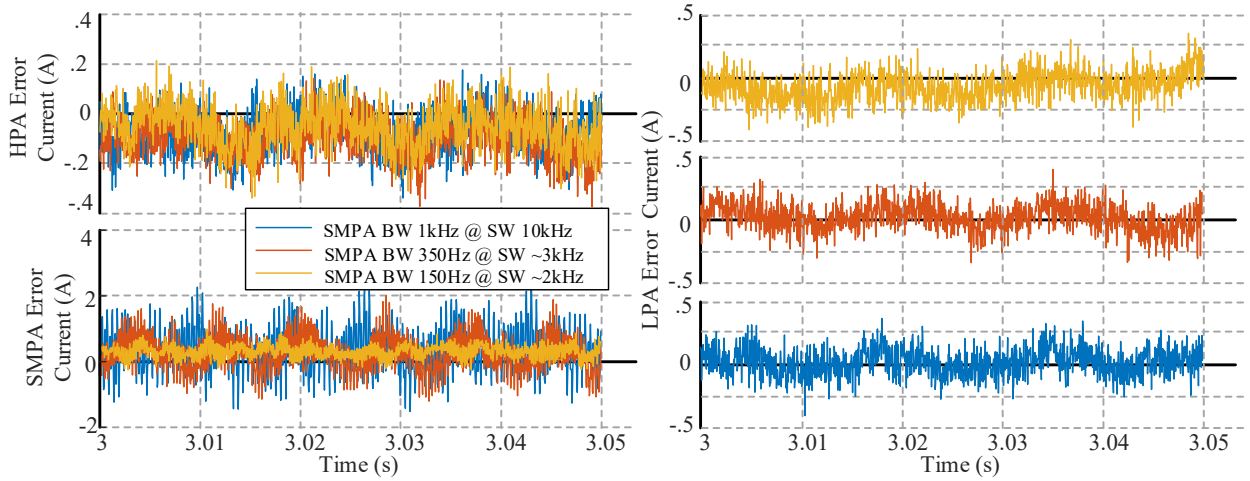


Figure 3.26 – Accuracy plot of experimental results for the initial part of the DOL, presenting currents of the a) HPA, top, and SMPA, bottom; b) LPA



(a) (b)

Figure 3.27 – Accuracy plot of experimental results for steady state, presenting currents of the a) HPA, top, and SMPA, bottom; b) LPA

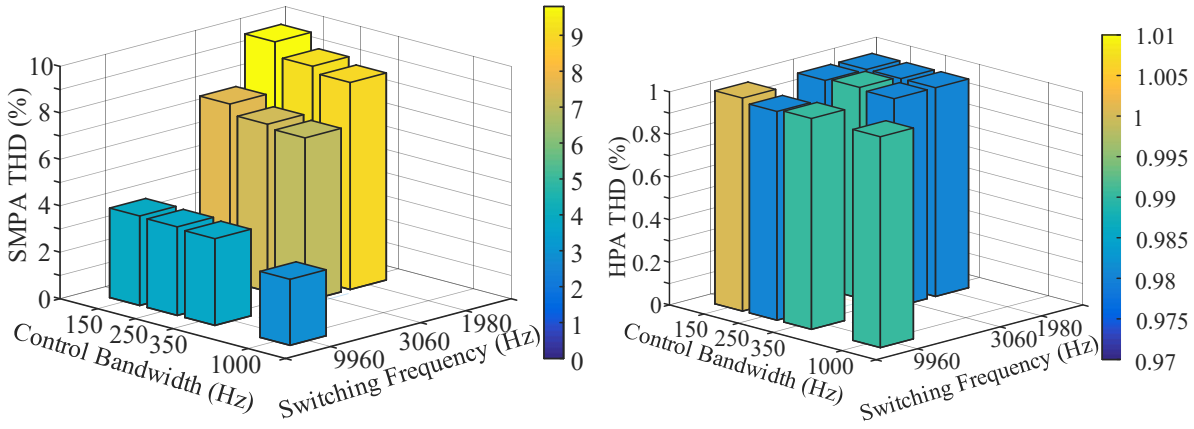
The higher the SMPA switching frequency (and BW_{SMPA}), the smaller is the size of the LPA. This also reduces the requirement for the LPA itself because the current ripple will be naturally reduced and filtered by the coupling inductor. Further increases on these parameters would further enhance the performance of the machine emulator with only the SMPA, although the LPA could still be used for compensating low order harmonics and transient responses.

Another important aspect shown by the experimental data is that the LPA must be designed mostly for the peak current but for a small interval. This peak current will be set by the output

transistor's limits. The rated current would be on a second priority, since it could be reduced even with a small BW_{SMPA} bandwidth.

In summary, the HPA system should be designed as a trade-off between the SMPA switching frequency and bandwidth, HPA output current limits, transient peak current (and time), and considering the limits of the computational time of the RTS.

The last analysis under this set of conditions is related to the THD of the SMPA and HPA, represented on Figure 3.28. In (a) it is possible to visualize the relation between increasing BW_{SMPA} and f_{sw} on the reduction on the THD and consequent improvement on the waveform quality. The THD reduces, in the worst case, from 9.80% to 2.84%. The THD of the HPA, Figure 3.28(b), does not show the same evolution, since the maximum compensation that the LPA can provide lowers the HPA's THD to 1% for all the range.



(a) (b)

Figure 3.28 – SMPA (a) and HPA (b) current THD (%) for all 10 cases

3.8. Conclusion

Power Amplifiers (PAs) are indispensable for Machine Emulation (ME). In this chapter, the issue of the cost of Linear Power Amplifiers (LPA) as PAs for ME was addressed with the proposal of a Hybrid Power Amplifier (HPA) consisting of a Switch Mode Power Amplifier (SMPA) in parallel with the LPA. A suitable control scheme for a "voltage-in current-out" machine model was conceived for the HPA. Since LPAs usually do not present a constant gain when operating in the current source mode, it is operated as a voltage source with a current control loop, like the SMPA. The reference current from the machine model is sent to the LPA, and the current in the

coupling impedance between the HPA and the grid or drive inverter is used as reference for the current loop of the SMPA. In this case, by selecting the bandwidth of the SMPA (BW_{SMPA}), as a fraction of that of the LPA, BW_{LPA}, it is possible to have an ME system with a fast dynamic response due to the high BW_{LPA}, which will provide the machine current only for a short time. The SMPA will take over the current synthesis, reducing the current ratings and cost of the LPA without performance degradation. The current control loops employ simple PI type controllers in the rotating ($dq0$) reference frame producing no errors in steady state. Simulations showed the superior performance of the HPA when compared to SMPA or LPA alone as ME, considering a trade-off between accuracy and cost. The performance of the proposed parallel HPA was verified experimentally with an ME system emulating the direct on-line start-up of an Induction Machine (IM). It was shown that for a SMPA operating with a switching frequency (f_{sw}) of 10 kHz and a BW of 1 kHz, the ratio of the LPA current (i_{LPA}) to the HPA current (i_{HPA}) for the short transient segment can be as low as 15%. As f_{sw} is reduced, so is the BW of the SMPA, which increases the stress on the LPA with higher ratios i_{LPA}/i_{HPA} and switching current harmonics. Nonetheless, the performance of the HPA, in terms of accuracy for tracking the reference current of the emulated machine, remains the same, determined by the closed loop BW of the LPA.

4. ORTHOGONAL SIGNAL GENERATORS AND PHASE LOCK LOOP FOR SINGLE-PHASE SYSTEMS

4.1. Introduction

Numerous applications, such as the synchronization of distributed energy resources to an existing AC grid, the operation of active power filters or the amplification of signals for Power-Hardware-In-The-Loop (PHIL) systems require a few tasks in common. Amplitude, Phase Angle and Frequency (APAF) detection are crucial for all these applications and many more. Various techniques are presented for three-phase and single-phase applications but only a few of them are able to identify the signals' attributes for a wide range of frequencies and amplitudes. Single-phase systems are typically burdensome, considering the challenge to create an internal signal, orthogonal with the input, in order to perform the phase angle detection. This matter is even more critical when the amplitude and frequency of the input signal varies in a wide range. This section presents two Orthogonal Signal Generators (OSG). The first is based on integral and derivative actions and it includes a detailed design procedure and a design example. The second is based on a zero-crossing detection system. The performance of both, single-phase wide range amplitude and frequency detectors are experimentally validated under steady state and dynamic conditions.

4.2. Wide Band Frequency Detection Based on Integral and Derivative Actions

The first system has the objective of providing a solution for APAF detection that can be used for the connection of converters to grid, act as a signal parameter identification for HPA and active filters, or used as feed-forward system where frequency reads are necessary. Also, it is presented as an improvement on the OSG topology presented in [107], for a single-phase amplitude, phase angle detection, making it frequency independent (for a known range) as well as self-reliant in terms of gain (C_1) or initial state settings. The topology will be benchmarked against well-known topologies. The goal is also to create a formal, instructive and effortless design procedure for a selected wide range frequency single-phase input signal. The inclusion of the frequency detection block from the phase angle with traditional derivative action and alternatively will be evaluated while employing a modern Kalman filter solution. To validate the proposed system, experimental results will verify the ability to identify the amplitude and phase angle of the system's signal in a wide range of frequency and amplitude.

4.2.1. Proposed System and Mathematical Modelling

The way to cancel the necessity of the fixed gain C_1, [107], is to guarantee that the multiplication of the integral (IB) [129], and derivative (DB) based [130], blocks have unity gain (0 dB) for all the range of frequencies of interest. This range will be called Area of Interest (AOI) when analyzing the frequency response of the system using Bode plots, presented further in this section.

Initially, it is important to understand how these IB and DB functions are built from "pure" (no gains, no additional poles/zeros) integral and derivative functions. In Figure 4.1, the pure integral ($1/s$) is shown on the blue curve. The first action is to multiply it by a gain k_i, which will increase its gain, but keep the pole in the same place, represented in the red curve. The next step is to displace that pole to p_i location. The resulting curve, in pink, will provide a gain of k_i/ω for frequencies higher than the pole, and a gain of k_{LF} for lower frequencies. It is relevant to mention the similarity of the IB transfer function, IB_{TF}, with a first-order Low-Pass Filter (LPF), which is convenient for this application, since it will attenuate high-order components outside the selected range of frequencies. In the example, k_i and p_i are respectively -5945.4 and -3.535 rad/s.

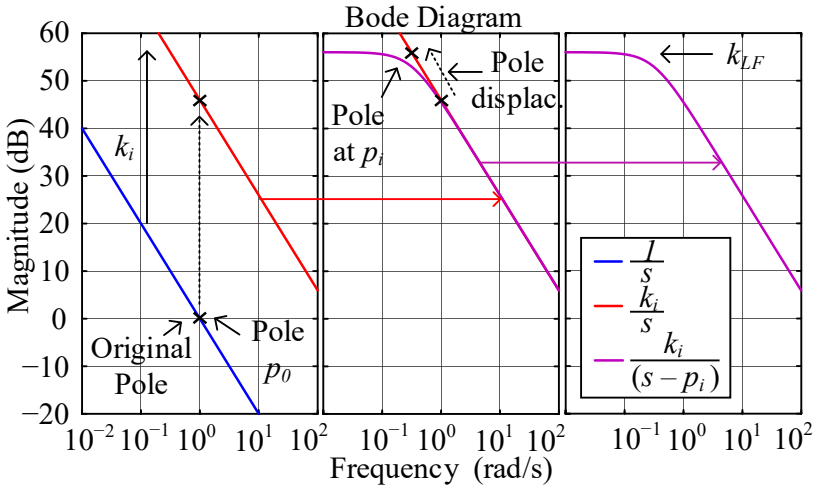


Figure 4.1 – Steps to build the IB_{TF} from a pure integral function

Similarly, the modification from pure derivative to DB function is shown in Figure 4.2. The pure derivative (s) is shown in the blue curve, with its zero located at the origin. Initially, the function will be multiplied by k_d, which will lower the transfer function gain but keep the zero in the same position ($k_d\, s$), shown in the red curve. Lastly a pole is added, p_d ($k_d\, s/(s\text{-}p_d)$), shown in the pink curve. This will guarantee a ωk_d gain for frequencies lower than the pole and k_{HF} for the

higher frequencies. In a similar fashion, the DB transfer function, DB_{TF}, resembles the behavior of a high-pass filter. In the example, k_d and p_d are respectively -1682 and -10^6 rad/s, in addition to the zero at origin.

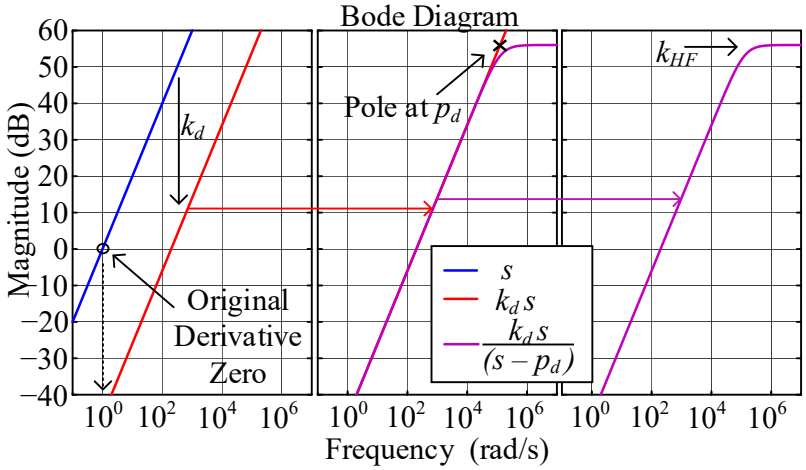


Figure 4.2 – Steps to build the DB transfer function (DB_{TF}) from a pure derivative function (blue—no gain | red—with gain | pink—with gain and added pole).

Looking at the multiplication of both functions, it becomes evident why the modification is necessary, relevant and useful. As shown in Figure 4.3, on the blue curve, if the pure integral and derivative functions are multiplied, the resulting gain would be unity with no phase added (which is an ideal feature, since any phase added by this stage will impact the variables of the APAF). This ideal scenario, however, does not offer attenuations to undesired (out of the selected range of) frequencies. On the red curve, considering the inclusion of k_d and k_i gains, if a $k_d k_i$ results in unity gain, the transfer function will have the same behavior as the previous one. Now, if a product $k_d k_i$ different from one ($\neq$1) is applied, the system would have to compensate for this introduced gain [107]. By placing p_d and moving p_i from the origin, and keeping product $k_d k_i$ as unity, the multiplication of the functions will now result in unity gain over the desired range of frequencies. This will also be able to attenuate frequencies outside it, which is a benefit when distortion or low/high order harmonics are present in the signal. The disadvantage is that a small phase error is added to the resulting signal close to the limits of the frequency range, which will be discussed further.

Regarding the requirement for the system to compensate the introduced gain, because of non-unity $k_d k_i$, as shown in [107] and considering the analog implementation of this circuit, operational

amplifiers and passive components can be used. They are prone to variances (related to precision) in their values and gains so a fixed gain at the end of the process, without any flexibility, adds undesired gains to the signals which will affect negatively the amplitude detection. In digital implementation, the removal of the gain means a reduced complexity on the system implementation. Also, working with the unity multiplication gain means flexibility to change and tune the parameters of k_i, p_i, k_d, p_d, without the need of reviewing any gain.

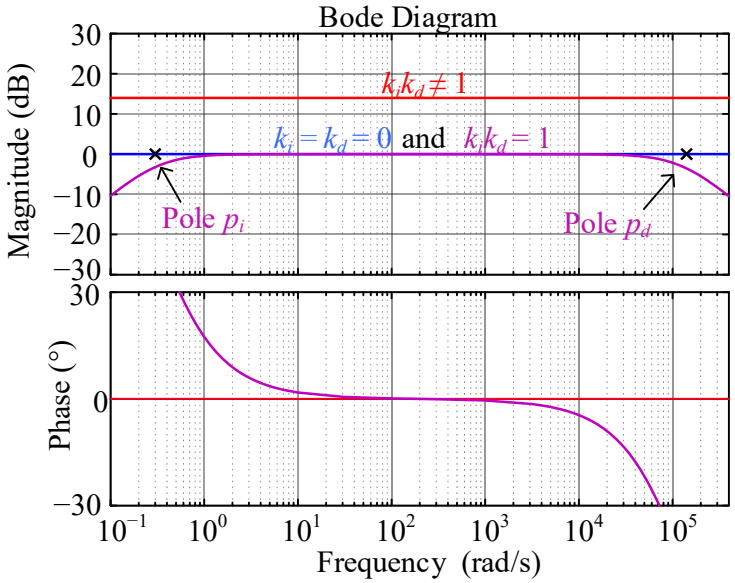


Figure 4.3 – Results from the multiplication of pure and modified integral and derivative functions

Figure 4.4 shows the proposed system, based on a simplified version of [107], with the addition of a conventional derivative block to extract the frequency from the phase angle, corresponding to Case 1. Another frequency detection block using a Kalman Filter Based (KFB) on a two-state prediction model will be evaluated as Case 2. They will be experimentally compared in Section 4.2.6.

The modeling of the main variables is presented in Equations (4.1)–(4.5). Considering an input voltage, v_α, given by a peak voltage, V_m, and a sinusoidal function of the phase angle θ, as shown in (4.1). The same can be written in terms of the angular frequency, ω, and time, t, as in (4.2). The IB and DB blocks outputs, v_i and v_d, are presented in (4.3) and (4.4), respectively. For (4.3) it is considered that signals with higher frequency than the frequency of the pole of the IB are applied, in which the gain k_i is constant. Similarly, for (4.4), the input signals with smaller

frequency than p_d will have a constant gain, k_d. Equation (4.5) represents the multiplication of v_i and v_d.

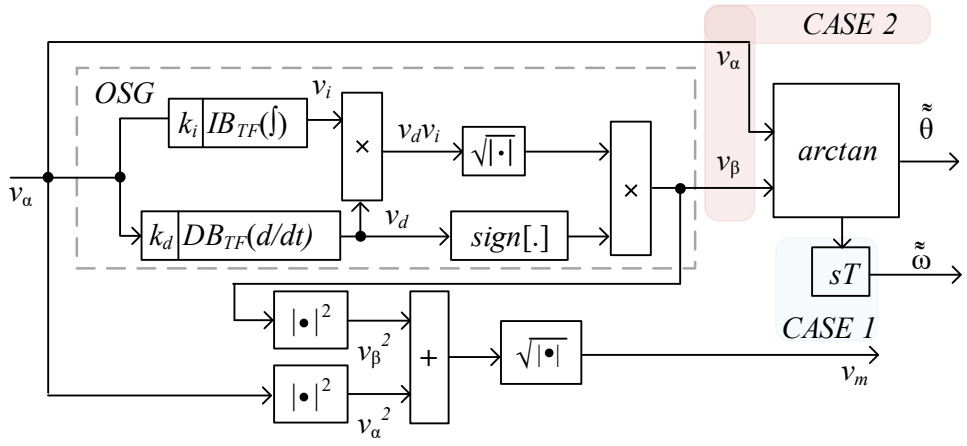


Figure 4.4 – Proposed wide band frequency detection system

$$v_\alpha(\theta) = V_m sin(\theta) \tag{4.1}$$

$$v_\alpha(\omega t) = V_m sin(2\pi f\, t) = V_m sin(\omega t) \tag{4.2}$$

$$v_i(\omega t) = IB_{TF}(v_\alpha) = -{}^{k_i}/_{\omega}\, V_m cos(\omega t) \tag{4.3}$$

$$v_d(\omega t) = DB_{TF}(v_\alpha) = k_d\, \omega V_m cos(\omega t) \tag{4.4}$$

$$v_i(\omega t) v_d(\omega t) = -k_i k_d V_m^2\, cos^2(\omega t) \tag{4.5}$$

Ensuring that the product $k_d k_i$ equals 1, which is one of the most relevant contributions of this study, will reduce (4.5) to (4.6). The goal now is to find an orthogonal signal, v_β, from v_α, which will be leading the signal by 90°. Then the next step is to apply a function to adapt the signal to positive values, before they can be processed by the square root block, as shown in (4.7). One should note that the square root of the squared cosine is not equal to the cosine ($\sqrt{(\cos^2 x)} \neq \cos x$) because the square root will only output positive portions of the signal. To achieve this the cosine has to be multiplied by the previous *signal* function of the input (–1 or 1), after applying its square root ($signal[x]\sqrt{(\cos^2 x)} = \cos x$). Considering all these operations, v_β, is found as (4.8) and the phase angle as (4.9). The output angular frequency, ω, will be found later using the two detailed Cases 1 and 2.

$$v_i(\omega t)v_d(\omega t) = -cos^2(\omega t) \tag{4.6}$$

$$v_\beta(\omega t) = \sqrt{|-V_m^2\, cos^2(\omega t)|}sign[v_d] = V_m\sqrt{cos^2(\omega t)}\, sign[v_d] \tag{4.7}$$

$$v_\beta(\omega t) = V_m cos(\omega t) \tag{4.8}$$

$$\theta = arctan\frac{v_\alpha}{v_\beta} = \frac{sin(\omega t)}{cos(\omega t)} \tag{4.9}$$

4.2.2. Kalman Filter Based Two-State Prediction Model

The implementation of the KFB two-state prediction model is proposed and evaluated in [112]. As shown in Figure 4.5, this block will operate on the comparison between prediction and correction states. The only difference from a genuine Kalman Filter is that the solution under study would have to adapt its gains for every processing time step, T_s. Its closed loop transfer function, KFB_{TF}, is given by (4.10) where $k'_{K1} = k_1/Ts = 2\zeta\omega_n$ and $k'_{K2} = k_2/Ts = \omega_n 2$. As in [112], $\zeta = 1/\sqrt{2}$ and $\omega_n = 125$ rad/s are selected. The notations ^ and ~ represent estimated values as an output or intermediate signals of the system.

$$KFB_{TF}(s) = \frac{k'_{K2}}{s^2 + sk'_{K1} + k'_{K2}} \tag{4.10}$$

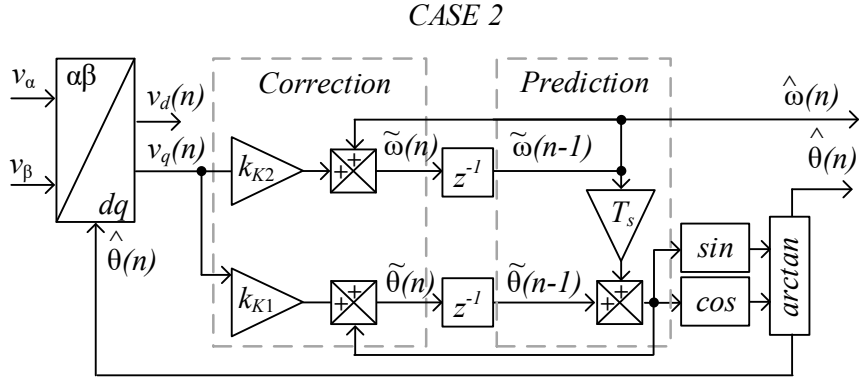


Figure 4.5 – Second case for the frequency detection based on the orthogonal signals input and a Kalman Filter Based solution.

4.2.3. Modeling, Design Constraints and Procedure

This subsection will present the design procedure and modeling as a methodological approach. The next section will include a design example, followed by the experimental validation

results. The first step is to define the limit frequencies for the desired operation range. These frequencies are the limit band frequencies, start and end (f_{ls}, f_{le}). This is strictly a design choice. For example, for grid frequencies, the start and end can be set as 50 and 60 Hz, for AC motor applications they can be set as 10 and 100 Hz, and for HPA applications they can be set as 1 and 1000 Hz [19], [29], [64], [87]–[91].

The second step is to determine the multiplier for achieving the correct bandwidth. The suggested gain (ς) is a decade further than the chosen bandwidth, but smaller or higher gains can be used to adjust the maximum phase added next to the start and end frequency limits. The resulting frequencies by the division (4.11), and multiplication (4.12), with ς are called the corner frequencies, initial and final (f_{ci}, f_{cf}), respectively. Note that the corner frequencies match the IB pole moved from the origin, p_i, and the DB placed pole, p_d.

$$f_{ci} = {f_{ls}}/{\varsigma} \tag{4.11}$$

$$f_{cf} = \varsigma f_{le} \tag{4.12}$$

Ideally, the same gain can be applied to both limits, but in the context where one wants to design an application in which there is a higher probability of using a specific frequency, a higher gain (ς_1 and/or ς_2) can be applied to that limit, as shown in (4.13) and (4.41). This will guarantee a gain close to the unity and smaller phase for that specific frequency. The average gain can be found using (4.15), denoted by the $\bar{}$ symbol.

$$f_{ci} = {f_{ls}}/{\varsigma_1} \tag{4.13}$$

$$f_{cf} = \varsigma_2 f_{le} \tag{4.14}$$

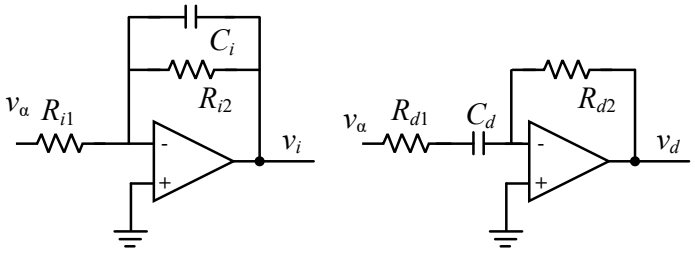
$$\bar{\varsigma} = {(\varsigma_1 + \varsigma_2)}/{2} \tag{4.15}$$

For both scenarios (same and different gains), a central cutoff frequency, f_{cc}, must be found. This frequency will be equally distant by another gain, N, from f_{ci} and f_{cf} on the logarithm distribution. The central frequency can be found as (4.16)-(4.17). Compared to Figure 4.3, for pure integral and derivative functions, N would be equal to 1 rad/s because both functions have their unity gain at 1 rad/s.

$$N = \sqrt{f_{cf} / f_{ci}} \tag{4.16}$$

$$f_{cc} = N f_{ci} \tag{4.17}$$

The first part of the proposed topology can be built with analog amplifiers for analog implementations [129], [130] or their corresponding transfer functions (4.18) and (4.19) can be used as well in any digital-based application. The analog equivalent of the IB_{TF} (4.18) is the integrator with constant DC gain, shown in Figure 4.6(a). The DB_{TF} (4.19) equivalent is the differentiator circuit with constant High Frequency (HF) gain, shown in Figure 4.6(b). The DC gain of the IB_{TF}, when multiplied by the +20 dB/decade provided from the DB_{TF} for those low frequencies, will cause the attenuation of frequencies outside the desired range of operation. Likewise, the HF gains of DB_{TF} when multiplied for the −20 dB/decade from the IB_{TF} will provide attenuation for frequencies higher than the desired range of frequencies.



(a) (b)

Figure 4.6 – Integrator and differentiator with constant LF and HF gains for analog implementation.

$$IB_{TF}(s) = \frac{v_i(s)}{v_\alpha(s)} = -\frac{1}{R_{i1}C_i}\frac{1}{s + \frac{1}{R_{i2}C_i}} = -N\frac{1}{1 + sR_{i2}C_i}. \tag{4.18}$$

$$DB_{TF}(s) = \frac{v_d(s)}{v_\alpha(s)} = -R_{d2}C_d\frac{s}{sR_{d1}C_d + 1} = -N\frac{s}{s + 1/(R_{d1}C_d)} \tag{4.19}$$

If implemented with the first part in analog mode, the gains of the integrators and differentiators for the whole operation range have to be carefully calculated to avoid saturation of the system, while considering the amplitude limits of the input. If implemented digitally using the

related transfer functions, there is no risk of saturation. Even though using the transfer functions in digital applications is straightforward and easier with the constant improvements and developments on Rapid Control Prototyping, designing the system for analog implementation can bring other benefits because it is pedagogical or approachable for some designers. Designing it in analog mode offers the designer the choice between the digital or analog implementation at the end, which is not the case when designed from the beginning in digital mode. In this study, the system is designed for analog but implemented in digital controllers (using their corresponding transfer functions) in order to evaluate the design and implementation procedures in both domains. In addition, as mentioned before, operational amplifiers and passive components are prone to variances (related to precision) in their values and gains so a fixed gain at the end of the process, without any flexibility, adds undesired gains to the signals which will negatively impact the amplitude detection. In digital implementation the removal of the gain means a reduced complexity on the system implementation and the flexibility of tuning k_i, p_i, k_d, p_d.

The integrator with DC gain is a well-known element in electronics and its generic transfer function is shown in Figure 4.7(a), with the gain on the top and the phase below. It provides constant DC gain, (4.20), for frequencies much smaller (denoted by the <<) than the corner frequency, given by (4.21), at the same location as the pole p_i in Figure 4.1. A variable gain, k_i/ω, for higher frequencies, is given by (4.22). The cutoff frequency, where the absolute gain is unity (0 dB), is defined as (4.23) for the IB output.

$$IB_{TF}(f \ll f_{ci}) = N = \frac{R_{i2}}{R_{i1}} \tag{4.20}$$

$$f_{ci} = \frac{1}{2\pi C_i R_{i2}} \tag{4.21}$$

$$IB_{TF}(f \gg f_{ci}) = -\frac{1}{R_{i1}C_i}\frac{1}{2\pi f} \tag{4.22}$$

$$f_{cci} = \frac{1}{2\pi C_i R_{i1}} \tag{4.23}$$

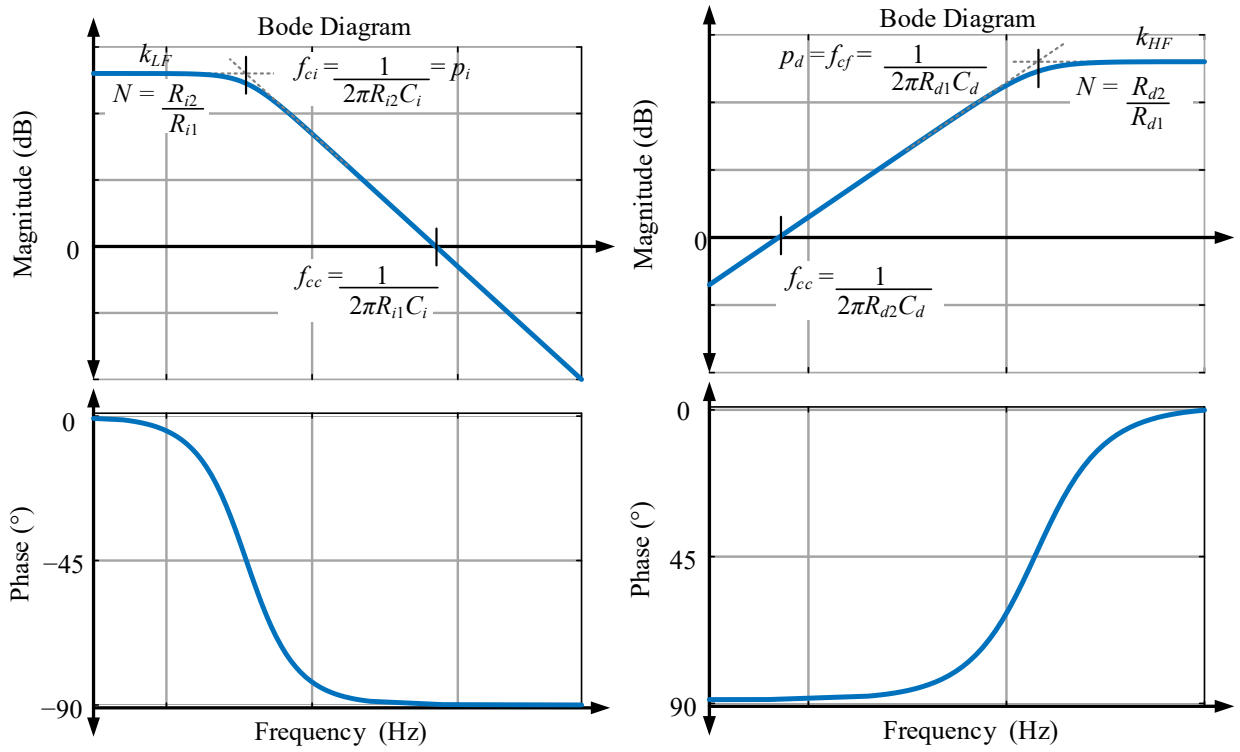


Figure 4.7 – Frequency response with gain (top) and phase (below) (a) integral block, (b) derivative block

The transfer function of the differentiator with constant HF gain is shown in Figure 4.7(b). It provides variable gain (k_d/ω), as in (4.24), with a slope of +20 dB/decade for frequencies much smaller (<<) than the corner frequency, (4.25), at the same location as the pole p_d in Figure 4.2. It also provides constant gain, (4.26), for those frequencies higher than the corner, which is the same gain as k_{HF}. The corner frequency should be higher than the end band frequency to ensure that the frequencies of the application are within the intended range. The cutoff frequency, where the gain is unity (0 dB) is defined as (4.27). The differential output has two important roles. The first one is to contribute with its differential part to the system, and to the multiplication that will follow. The second one is that the differential output has a phase of −90° with the input, and the function *signal* [v_d] complements the square root of the squared cosine, as explained before.

$$DB_{TF}(f \ll f_{cf}) = -R_{d2} C_d 2\pi f \tag{4.24}$$

$$f_{cf} = \frac{1}{2\pi C_d R_{d1}} \tag{4.25}$$

$$DB_{TF}(f \gg f_{cf}) = \mathrm{N} = \frac{R_{d2}}{R_{d1}} \tag{4.26}$$

$$f_{ccd} = \frac{1}{2\pi C_d R_{d2}} \tag{4.27}$$

By multiplying the integrator and differentiator gains, (4.28)–(4.29), a unity gain (0 dB) can be found for the desired frequency range (f_{ls} to f_{le}), if the condition stated in (4.30) is respected. In addition, there will be no phase (ideally) added to this signal, although a small phase error may be found close to the frequency limits. The corner frequencies are given by (4.21) and (4.25) and they must be equal, according to (4.30). The unity gain, as shown in any of the curves of Figure 4.8, in the entire range makes it possible to eliminate any further multiplication by gains, reducing the complexity of the proposed system.

$$IB_{TF}DB_{TF}(s) = \frac{v_i(s)v_d(s)}{v_\alpha^2(s)} = -\frac{R_{i2}R_{d2}C_d}{R_{i1}} \frac{1}{1 + s(R_{i2}C_i + R_{d1}C_d) + s^2(R_{i2}C_iR_{d1}C_d)} \tag{4.28}$$

$$\begin{aligned} |IB_{TF}DB_{TF}(f_{ls} < f < f_{le})| \\ = -\frac{R_{i2}R_{d2}C_d}{R_{i1}} \frac{1}{1 + (2\pi f)(R_{i2}C_i + R_{d1}C_d) + (2\pi f)^2(R_{i2}C_iR_{d1}C_d)} \approx 1 \end{aligned} \tag{4.29}$$

$$f_{cc} = f_{ccd} = \frac{1}{2\pi C_d R_{d2}} = f_{cci} = \frac{1}{2\pi C_i R_{i1}} \tag{4.30}$$

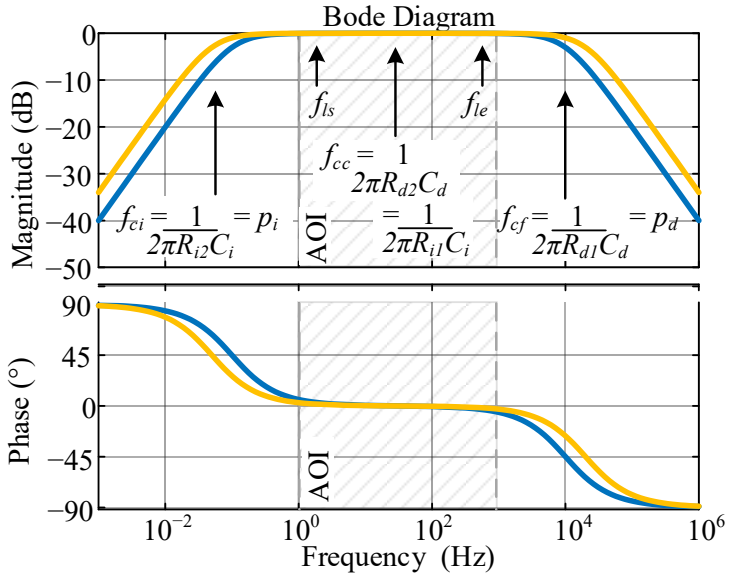


Figure 4.8 – Result of the multiplication of v_d and v_i for design example - amplitude (top) and phase (below)—first case ($\varsigma = 10$) in blue, second in orange ($\varsigma = 20$).

4.2.4. Design Example

For the PA and PHIL application, the OSG must be able to recognize input frequencies from 1 to 1000 Hz. The initial gain (ς) used for the system is 10 and, as given by (4.11)–(4.12), the corner frequencies will be 0.1 and 10,000 Hz. Using (4.16)–(4.17), the gain (4.31) and the central cutoff frequency (4.32) will be expressed as

$$N = \sqrt{10000/0.1} = 316.227766 \tag{4.31}$$

$$f_{cc} = f_{ccd} = f_{cci} = N f_{ci} = 31.6277\,Hz \tag{4.32}$$

Fixing the resistors R_{d1} and R_{i1} at 1 kΩ allows the remaining resistors, (4.33) to be found using (4.20) and (4.26). Using (4.23) and (4.27), it is possible to determine the capacitors for the integral and differential part, (4.34)–(4.35). After having defined all the parameters, it is possible to determine the transfer functions for each block, (4.18)–(4.19), and plot the amplitude and phase frequency response of the multiplication of both blocks, as shown in Figure 4.8, in the blue curve. The shadowed area represents the start and end frequency limits (1–1000 Hz). It is possible to observe the gain very close to unity for all the operation range or AOI. There is a small phase error in the system next to limits (5.7° at 1 Hz and −5.7° at 1 kHz).

$$R_{i2} = R_{d2} = N R_{i1} = 316.2277\,k\Omega \tag{4.33}$$

$$C_i = \frac{1}{2\pi f_{cci} R_{i1}} = 5.0329\,\mu F \tag{4.34}$$

$$C_d = \frac{1}{2\pi f_{ccd} R_{d2}} = 15.915\,nF \tag{4.35}$$

One solution to improve (and reduce the phase error next to the limit band frequencies) is to increase the gain (ς) to 20. The second case in Figure 4.8 is represented by the orange line. Consequently, new values for *N*, resistors and capacitors are found in (4.36)–(4.40). With a higher gain, there was an improvement on ensuring 0 dB (or unitary gain) in a more extended way. Most significantly, a phase error reduction on frequencies closer to the band limits was achieved through this process (2.86° at 1 Hz and −2.86° at 1 kHz).

$$N = 632.4455 \tag{4.36}$$

$$f_{cc} = 31.6277\,Hz \tag{4.37}$$

$$R_{i2} = R_{d2} = N\,R_{i1} = 632.4555\,k\Omega \quad (4.38)$$

$$C_i = 5.0329\,\mu F \quad (4.39)$$

$$C_d = 7.9577\,nF \quad (4.40)$$

4.2.5. Comparative Analysis and Benchmark of the Proposed System

In order to compare the proposed system APAF detection abilities, it will be compared with other three topologies. The first one is the one from which the proposed topology is based, Picardi's PLL [107], as shown in Figure 1.28. The gain C_1 is set at 1/202, and the derivative pole is at 1.6 MHz, while the integral pole is at 0.5 Hz (although the study does not mention the frequencies of these poles, they can be extracted from the passive elements used). The second system is the inverse Park's PLL [114], [115], as shown in Figure 1.27(a). The filters are set with a cut-off of 120 Hz and k_p = 200 and k_i = 20,000. The third system is the Enhanced-PLL [116], [117], with k_p = 400 and k_i = 40,000. The last two systems are set for a central frequency of 50 Hz.

All the results are simulated under the same time step of 10 μs (same as for experimental results in the next Section 4.2.6). The main aspect of the simulation is to evaluate the amplitude and frequency of the input signals. Secondarily, the error on the phase angle detection for all the systems will be evaluated. One important aspect of the simulations is that it is better to have smaller errors with higher settling times than the opposite, since high variations on APAF systems can create instability for converters or equipment dependent on them.

The first analysis is to evaluate the amplitude detection, V_m, for a wide range of frequencies, assessing the systems at 50 Hz, Figure 4.9(a) and 500 Hz, Figure 4.9(c) and zoom in Figure 4.9(c). For 50 Hz, all the systems are able to detect the amplitude. At this condition, the best systems are the EPLL and Park's PLL, since they are specifically designed for this frequency (both systems can be considered to have 0% error). The proposed system performs better than Picardi's (0.2%), with 0.1% error. The error is related to the maximum overshoot or undershoot of the signal and all the averages perfectly match the 50 Hz input signal. For 500 Hz, the inability of Park's PLL to track the amplitude is clear. EPLL was still able to track the amplitude correctly, with 0.1% error. Once again, the proposed system shows the superior performance when compared to Park's PLL and Picardi's, visible in Figure 4.9(c). The proposed system outputted an error of 0.3%, smaller than the 0.8% from Picardi's PLL. Except for EPLL's, the proposed system showed remarkable results under this evaluation.

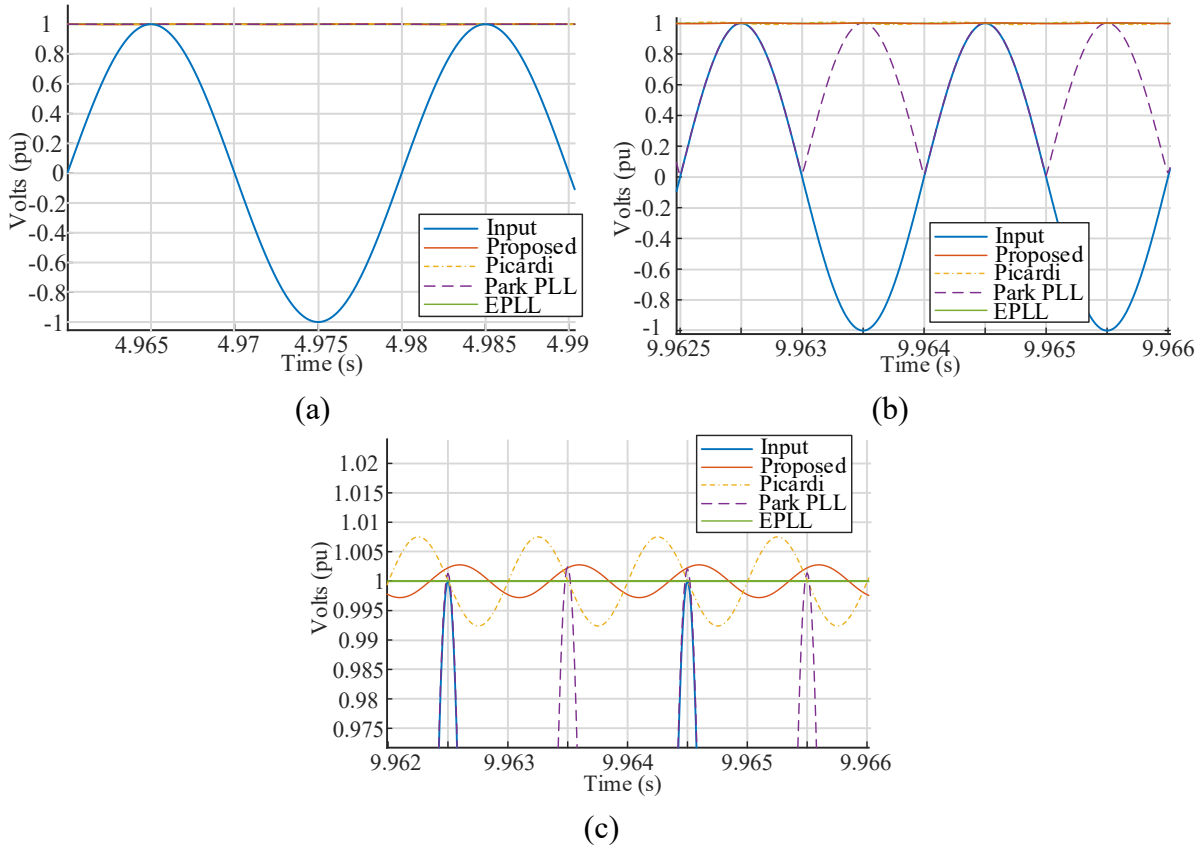
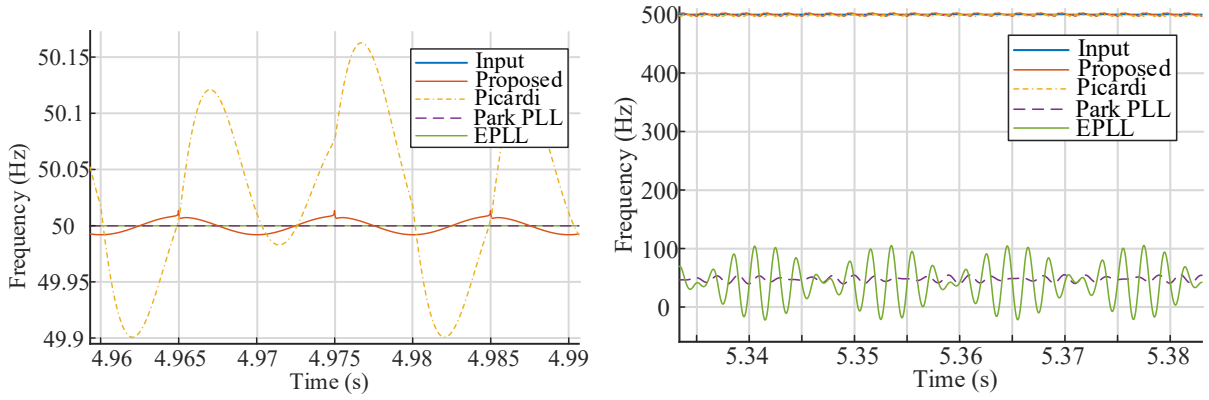


Figure 4.9 – Comparison of amplitude detection techniques for a 1 pu input of (a) 50 Hz, (b) 500 Hz, (c) zoomed at 500 Hz.

The second analysis takes into account the ability of the systems to identify the input signal's frequency, for the same 50 and 500 Hz input and constant amplitude of 1 pu. As shown in Figure 4.10(a), all systems are able to identify closely the input frequency of 50 Hz. Once again, for the fundamental frequency equal to the central frequency, Park's PLL and EPLL performed at the best level, but once a different frequency was inputted, both systems lost their capability of identifying the frequency, as can be seen in Figure 4.10(b), for an input of 500 Hz. The proposed system provided the best frequency detection for 500 Hz, with errors smaller than 0.44% (Picardi's error is 0.7%). This shows the ability of the proposed system to deliver the frequency identification for a wide range of frequencies, without compromising the quality and precision of the output. As EPLL and Park's PLL are designed for 50 Hz, they oscillate with high errors around that frequency.



(a) (b)

Figure 4.10 – Comparison of frequency detection techniques for a 1 pu input of (a) 50 Hz, (b) 500 Hz.

The third analysis is very well known in the literature [112], for evaluating the quality of APAF systems. This consists of applying a phase jump of 40° on the input signal, keeping the frequency and amplitude constant at 50 Hz and 1 pu. Several analyses can be done based on this, but the most important is the error of the phase angle (θ) when compared to the phase angle of the input signal, as shown in Figure 4.11. Picardi's PLL and the proposed PLL are in phase, outputting the same result, since 50 Hz is inside both of their ranges of frequencies. The proposed system is the one with smaller overshoot/undershoot levels, reaching only 4.4° (measured at the highest oscillation after the 40° jump). Picardi's PLL has a similar error of 4.57°. Parks' PLL is the highest error overshoot (22.2°), followed by EPLL (11.19°).

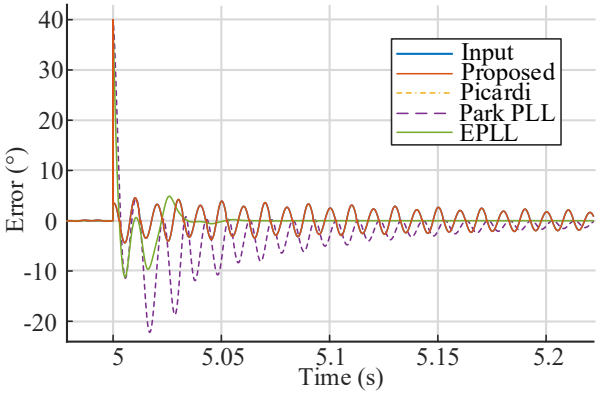
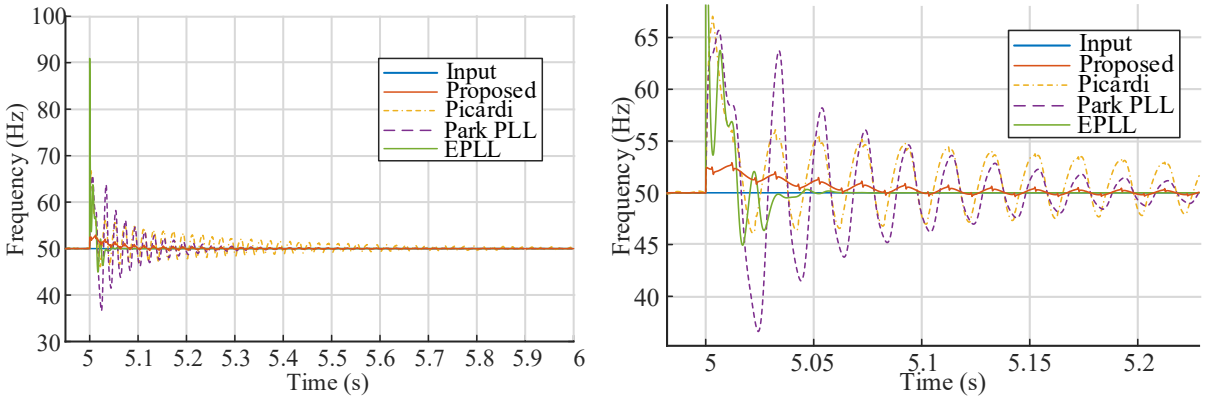


Figure 4.11 – Comparison of phase angle detection errors for a 40° phase jump for a 1 pu and 50 Hz input.

Still under the 40° phase jump condition, the next analysis is on the ability of the systems to identify the input frequency during the phase jump. Figure 4.12(a) shows the results for an extended period, while Figure 4.12(b) focuses on the transient. EPPL presents a sudden large variation, increasing the output frequency to 90.92 Hz (error of 81.84%). Park's PLL outputs a frequency of 36.61 Hz (error of 26.78%). Picardi's PLL outputs a frequency of 67.05 Hz (error of 34.1%). The proposed system on the other hand performs as the best frequency detection method, with a small overshoot of 2.91 Hz (error of 5.82%), showing the remarkable stability of the system.



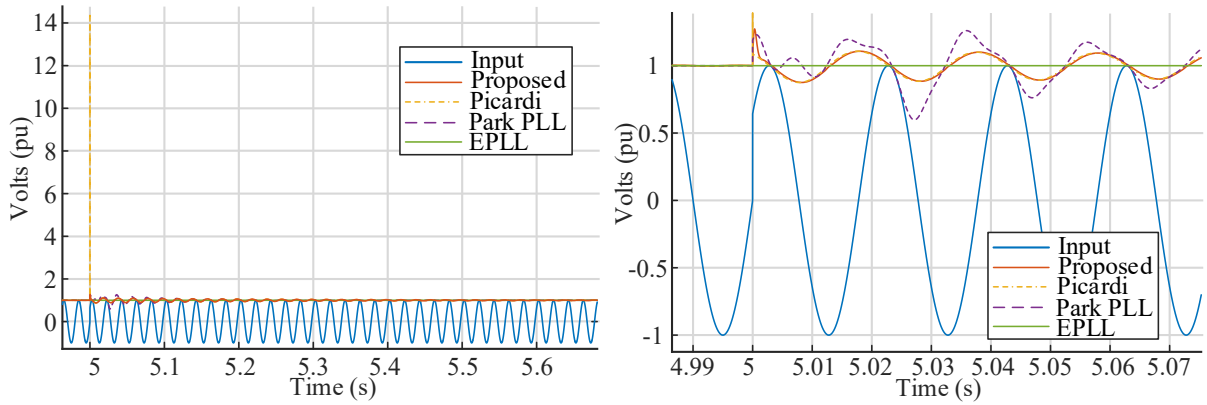
(a) (b)

Figure 4.12 – Comparison of frequency detection techniques for a 40° phase jump for a 1 pu (a) 50 Hz, (b) zoomed for 50 Hz.

The next analysis for the same test conditions, concerns the amplitude detection, V_m, during the phase jump. Figure 4.13(a) shows the extended period, while Figure 4.13(b) focuses on the initial part of the transient. The proposed PLL has a small overshoot (variation of 0.27 pu). Picardi's PLL saturates its output (14.35 pu) even though that happens for a brief time. Park's PLL gives the second highest ripple (variation of 0.4 pu), and EPLL, for this condition, does not present any overshoot, but mostly because the input matches its central frequency. The settling times for all systems are similar.

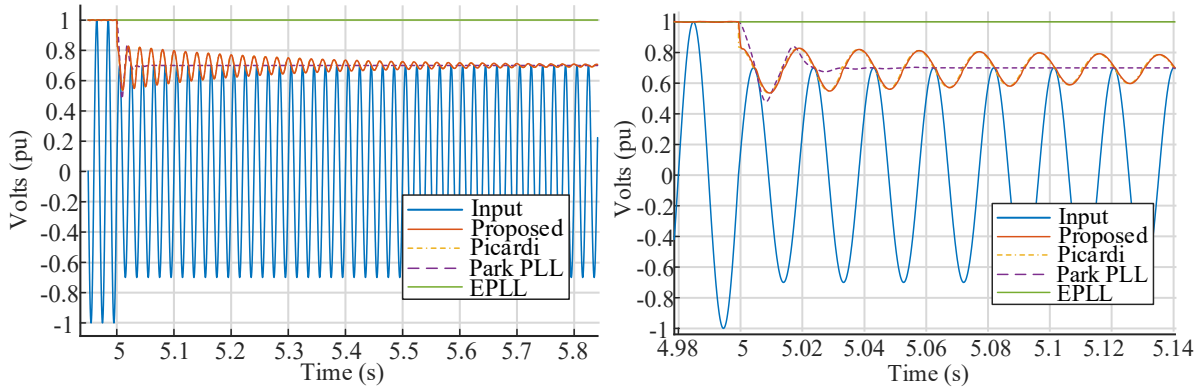
Now the systems can be evaluated at the last condition, which is a known phenomenon in AC grids, the voltage sag. At a constant 50 Hz input, the amplitude changes from 1 pu to 0.7 pu. Shown in Figure 4.14, the performance of the amplitude detection of all systems were evaluated. EPLL could not identify the signal variation, while Park's PLL provides an output with the highest error, with an amplitude of 0.47 pu. The proposed system and Picardi's present similar results, with the lowest value reaching 0.53 pu. Lastly, the frequency detection is evaluated in Figure 4.15.

Picardi's PLL takes more than a second to settle and outputs a signal that reaches 63.4 Hz (error of 26.8%). EPLL presents the worst and lowest value, with 41.88 Hz (error 16.24%), but it has a short settling time. Park's PLL is close to the latter, with the lowest value reaching 42.55 Hz (error 14.9%). Once again, the proposed system shows the superior performance with a small error of 3.12%, with a small overshoot of 1.56 Hz.



(a) (b)

Figure 4.13 – Comparison of amplitude detection techniques for a 40° phase jump for a 1 pu (50 Hz) input for (a) extended frame, (b) zoomed frame



(a) (b)

Figure 4.14 – Comparison of amplitude detection techniques for a voltage sag from 1 to 0.7 pu (50 Hz) for (a) extended frame, (b) zoomed frame.

All simulations show the ability of the proposed system to perform with high quality in all ranges of frequencies and amplitudes, differently from the other systems that can only perform well at one specific frequency. The proposed system even performs better for some conditions when comparing the other systems on their central frequency (50 Hz).

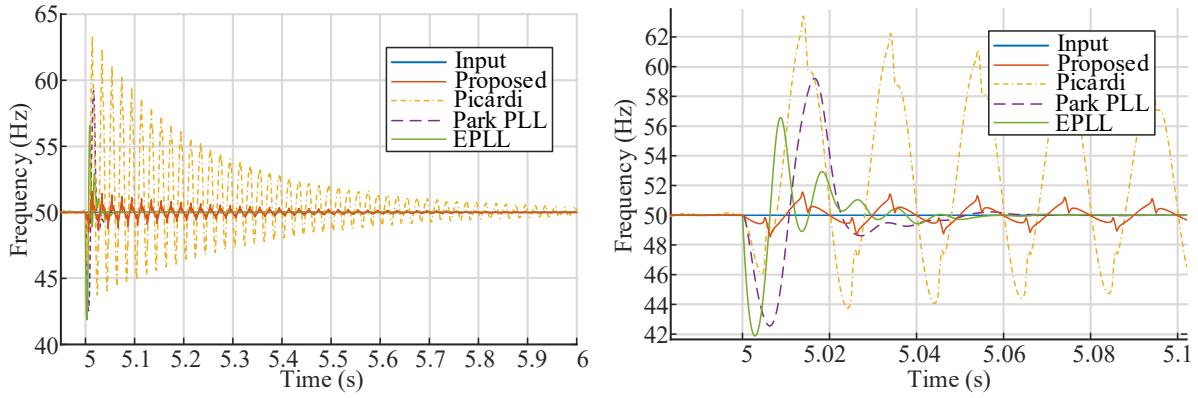


Figure 4.15 – Comparison of frequency detection techniques for a voltage sag from 1 to 0.7 pu (50 Hz) for (a) extended frame, (b) zoomed frame

4.2.6. Experimental Validation of the System

Considering the good results achieved in the simulation, an experimental setup was built to validate the proposed system. The central element is the controller, an OPAL-RT OP4510 real-time simulator that will be used to process the input voltage and output its APAF and orthogonal signals. For its input and as a reference signal provider, a Hewlett Packard 3325B Synthesizer/Function Generator was used. A Yokogawa DLM2024 Mixed Signal Oscilloscope was used to read the input signal and the output signals of the controller. The controller was implemented in the Simulink environment, which is also a GUI for OPAL-RT, following the digital implementation of the system. The minimum time step of 10 μs was used in this case. Table 4.1 presents the main parameters used for defining the variables of the system for the experimental tests. The experimental setup is presented in Figure 4.16.

Figure 4.17 shows the system that was built for validation, with the variables defined as (4.36)–(4.40) and Table 4.1. The system includes the proposed OSG with unity gain, a conventional amplitude detection and evaluates two cases for phase angle and frequency detection. In the first case, the limiters (LIM) were used to allow only positive values to be processed. The second order Low Pass Filters (LPFs) were set to remove any high frequency noise or interferences from the amplitude and from the first case of frequency detection, with a cut-off of 100 Hz and 0.707 as a damping factor.

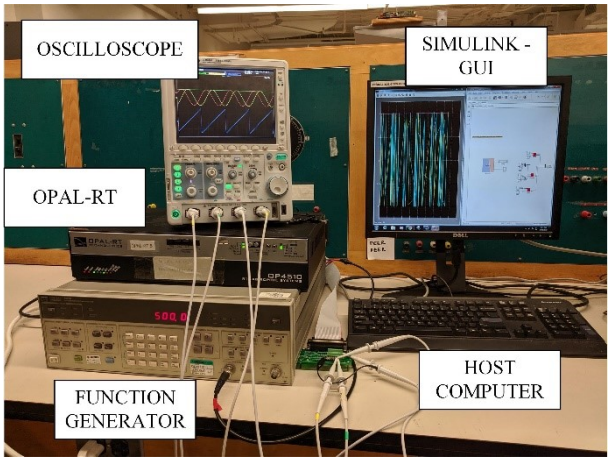


Figure 4.16 – Experimental setup built for the system validation.

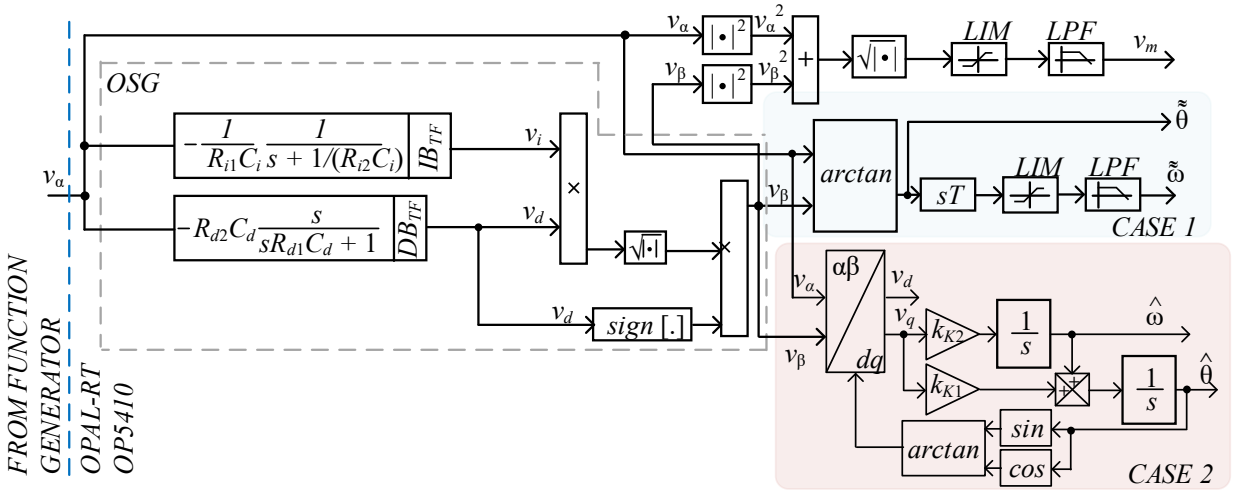


Figure 4.17 – Complete system used for the validation of the proposed OSG and frequency/amplitude detection system.

Table 4.1 – Parameters for experimental setup.

Parameter	Value OR Range
Input signal amplitude (v_α)	0.5–2 pu
Input signal frequency (v_α)	1–1000 Hz
R_{d1} & R_{i1}	1 kΩ
R_{d2} & R_{i2}	632.4555 kΩ
C_d	7.9577 nF
C_i	5.0329 µF
k_i	−0.005032
k_d	−198.692602
k_{K1}	0.01768
k_{K2}	1.5625
Processor time step (Ts)	10 µs

In the first test, the verification of the system was performed initially with a frequency ramp to evaluate which one of the cases would perform a better frequency tracking. A ramp from 60 to 1000 Hz with a duration of 5 s (±188 Hz/s) was applied as the input signal, which also had amplitude steps around halfway of the ramp from 1 to 2, and later from 2 to 1 pu, as shown in Figure 4.18. The first graph shows in blue (CH1) the input voltage, the frequency reference in cyan (CH2), the frequency detection based on the derivative action (Case 1) in pink (CH3), and the frequency detection with Kalman Filters (Case 2) in green (CH4), which is overlapped with the reference. The middle graph shows the error between Case 1 and the reference (cyan—CH5), and between Case 2 and the reference (pink—CH6). The lower graph presents the zoomed areas detailing the amplitude steps. The results for Case 2 presented better quality, since the maximum error was a little higher than 5 Hz, while Case 1 was around 20 Hz. In addition, Case 1 presented a high oscillatory behaviour, both in amplitude and time, when amplitude steps were applied. This case also showed an offset error that became more relevant in higher frequencies. As the quality of Case 2 is superior, it is clear that the system with Kalman Filter will be selected as a standard for frequency identification for the next tests.

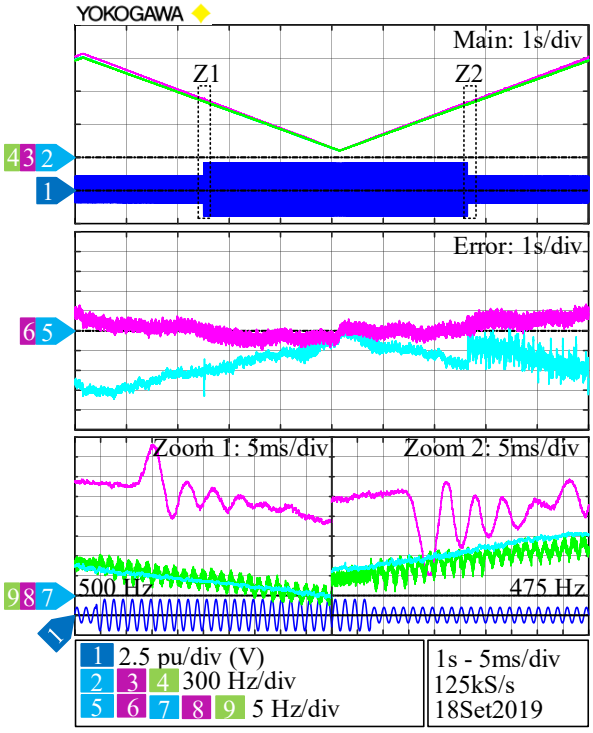


Figure 4.18 – Experimental results for a frequency ramp (±188 Hz/s) and voltages steps 1-2-1 pu.

The second test comprehends an amplitude step given to the reference (blue - CH1) from 1 to 2 pu and later removed, as shown in Figure 4.19. The amplitude detection' signal output, V_m, appears in the cyan line (CH2). The reference frequency and the Case 2 detection output are also shown (pink-CH3 and green-CH4). The lower graph shows the zoomed areas 1 and 2. The amplitude detection system could track the new signal parameters within two and a half cycles of the new signal, showing the quality of the proposed system in tracking wide variations in amplitude.

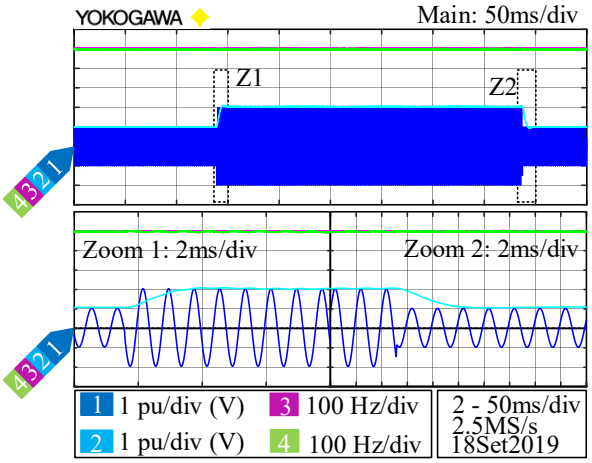


Figure 4.19 – Experimental results for amplitude steps 1-2-1 pu.

In the third test, a frequency step was given to the reference (blue - CH1) from 500 to 750 Hz, and later removed, Figure 4.20. The amplitude detection's signal output, V_m, is shown in the cyan line (CH2), similarly to the previous test. The reference frequency (pink - CH3) and the frequency detection output of Case 2 are shown in the pink and green lines (CH3 and CH4, respectively). Different from the amplitude, the frequency detection takes a few more cycles to achieve steady state, around 25 cycles (35 ms) for the increasing step and 15 (20 ms) for the decreasing. Even though it is a considerable high step (±50%), the detection was fast when only analyzing the point of view of time. The processor time step plays a major role in increasing this speed of response. There is no significant or observable impact of the frequency step on the amplitude detection, which exhibits the superior quality of the combination of the proposed system with the Kalman's Filter Based frequency detection.

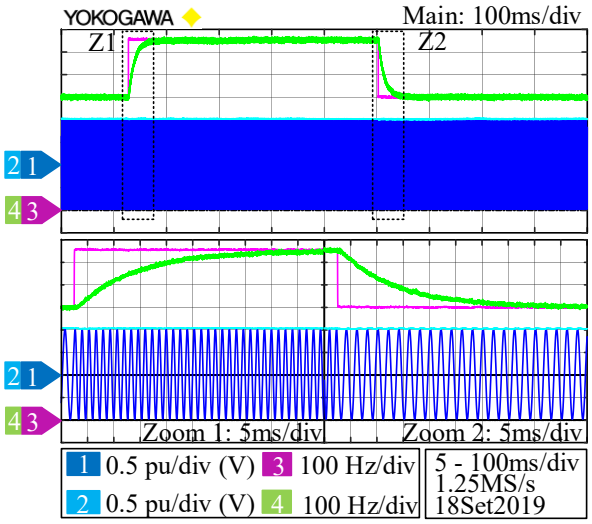


Figure 4.20 – Experimental results for frequency steps 500-750-500 Hz.

Lastly, for the fourth test, the phase angle detection, along with the amplitude detection are the most important signal parameters for the applications under study. Therefore, lastly and most importantly, this test will evaluate the ability of the system to generate appropriate orthogonal signals (pink - CH3) and the phase angle (green - CH4) of the input signal (blue - CH1), as shown in Figure 4.21. In addition, the amplitude detection is presented (cyan - CH2). A phase inversion is applied and detailed on the zoomed area below. For this set of results, the speed of response of the system adapts remarkably to the variation on the input signal, without creating any overshoot in V_m and instantaneously detecting and correcting the phase angle output.

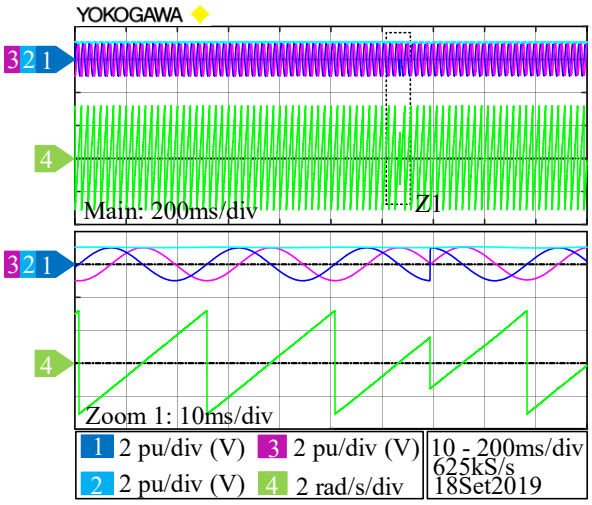


Figure 4.21 – Experimental results for orthogonal signal generation and phase angle for a phase inversion.

When looking back at the challenges proposed at the beginning of this section, a new OSG based on integral and derivative blocks was presented and validated. It presented an intuitive design process, with its supporting simulation and modelling. The removal of the C_1 (Picardi's PPL) gain makes it simpler and less prone to errors. Considering the simulations, the proposed system was considered to be the best performing APAF in several cases and the only one able to perform with small errors at all ranges of the input signal. This performance was validated experimentally in this section, proving this topology's ability to identify single-phase inputs for static and dynamic conditions.

4.3. Hybrid Single Phase Wide Range Amplitude and Frequency Detection

4.3.1. Proposed System and Mathematical Modelling

An additional technique for an OSG for APAF is presented in this section. The technique is a hybrid construction of an algorithm part (developed in C programming language) followed by a traditional SOGI SP-PLL, composed of adders, multipliers, gains and square root, as shown in Figure 4.22. The advantages of this technique are the simplicity and the accuracy of the APAF outputs.

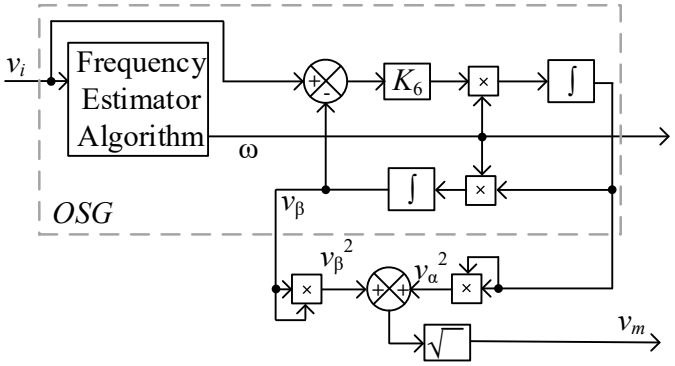


Figure 4.22 – Proposed complete Hybrid SP-PLL for wide frequency range

The only objective of the algorithm block, presented in Figure 4.23, is to determine the frequency of the signal. The logical construction is based on existing zero-crossing detection techniques, to determine the time interval between them. Although using zero-crossing detection techniques may not be a valid choice for signals with low frequency harmonics, and consequently various crossings on the voltage axis [106], [108], this technique will be used here because under

the scope of this study, only pure (one fundamental component) sinusoidal signals will be evaluated.

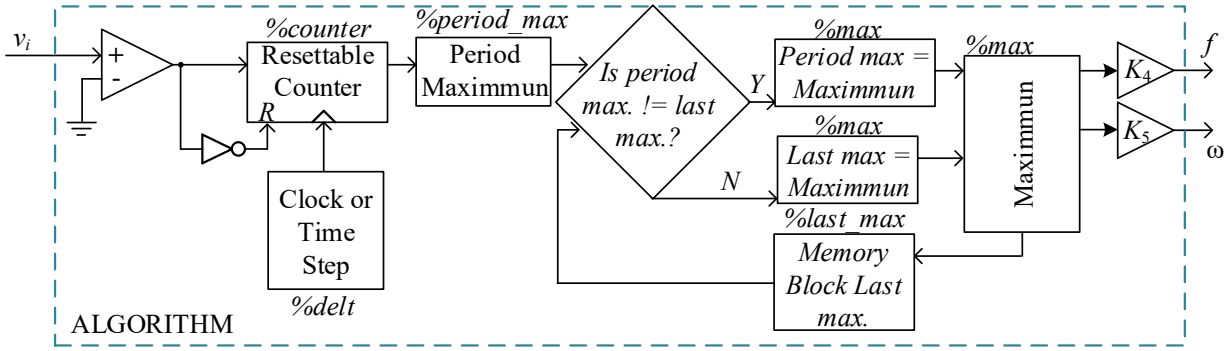


Figure 4.23 – Proposed Algorithm for wide range frequency determination

In more details, the algorithm relies on the summation of an integer counter (*%counter*) for every time step (*Tc*, *%delt* or *clock*) in which the reference signal is larger than zero. The important concern here is that the time step has to be fixed and known, which is easily found for any digital processor or RTS. The final value of this counter is stored as the maximum value for the first or current period (*%period_max*). If this value is different from the previously stored maximum (*%last_max*), the output value (*%max*) changes. Otherwise, the output value remains as the last stored maximum. Up to this point, all variables are integers, which can cause inaccuracies in outputting the relative value of the frequency if the time step is high. By ensuring a small time step, the imprecision will be reduced significantly. The system resets itself for the next period and repeats the same process. With the maximum value, a multiplication with a gain K_4 (4.41) and K_5 (4.42) is made to obtain the signal frequency in Hz, in radians per second and the period, respectively.

$$K_4 = \frac{1}{2\ \%max\ \%delt} \tag{4.41}$$

$$K_5 = \frac{\pi}{2\ \%max\ \%delt} \tag{4.42}$$

The second part is built the same way as presented in [102], using the integrators and multipliers to create the same orthogonal signals used in the SP-PLL system. The orthogonal signals are then squared, added and square rooted, as in (4.43). The result corresponds to the peak value of the reference, v_m. The complete system can be seen in Figure 4.22.

$$v_m = \sqrt{v_\alpha^2 + v_\beta^2} \tag{4.43}$$

The final part is the design of K_6, similarly to [101], [102]. The main limitation of the system is that, for practical or experimental implementation, it is impossible to have an infinite bandwidth for the system. The limits will be set mainly by the clock of the chosen digital controller. The higher the clock, the higher the frequencies that the controller will be able to process. Furthermore, the system relies on digital controllers, which may be not cost-effective for some products or solutions.

4.3.2. Experimental Results

An experimental setup was built to validate the proposed system. The central element is an OPAL-RT OP4510 real-time simulator that will be used to process the input voltage and output its peak, frequency, angle and orthogonal signals. For its input, and reference signal provider, a Hewlett Packard 3325B Synthesizer/Function Generator was used. A Tektronix MDO3024 Mixed Domain Oscilloscope was used to read the input signal and the output signals of the controller. The whole system was implemented in the Simulink environment, which is also a GUI for OPAL-RT, following the digital implementation of the system. The C code was placed inside a Simulink Matlab Function Block. A time step (*%delt*) of 10 μs was used in this case. The experimental step response (at the vertical dashed line) for different values of K_6 is shown in Figure 4.24. From the vertical dashed line, a step from 110 to 160 V is applied at a constant frequency of 60 Hz. The cyan, magenta and green lines represent gains of 0.5, 1 and 3, respectively.

The second value is chosen for K_6 (K_6=1) due to the limited overshoot. Figure 4.25 represents a step in the amplitude of the signal, from 150 to 200 V with a fixed frequency of 60 Hz. It is possible to see that within two full cycles of the peak signal, V_m, reaches steady state while the frequency, f, is steady and ripple-free.

Figure 4.26 shows the response of the system to a step in frequency from 60 to 1000 Hz and from 1000 to 60 Hz, as given by the reference, f^*. The output frequency, f, tracks the reference within one and a half cycles of the new frequency. Analyzing the time frame, the system behaves faster for steps increasing the frequency, but both responses are the same under the number of cycle's perspective. That happens due to the change of the slope that takes place on *%counter*. The

output peak voltage, V_m, is constant, although a small transient can be observed, which happens due to the dependency of the frequency to create the orthogonal signals, v_α and v_β, needed for the peak determination. The selected values, especially in terms of frequency, are within the usual output bandwidth for commercial LPA and HPA.

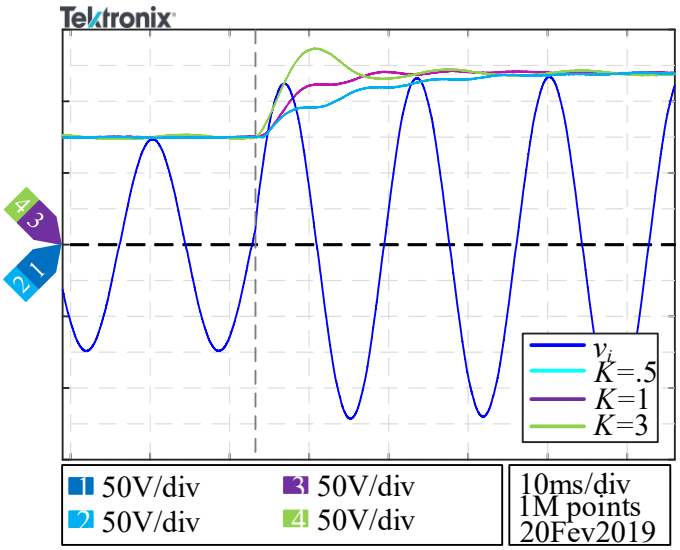


Figure 4.24 – Amplitude determination with different K_6 settings

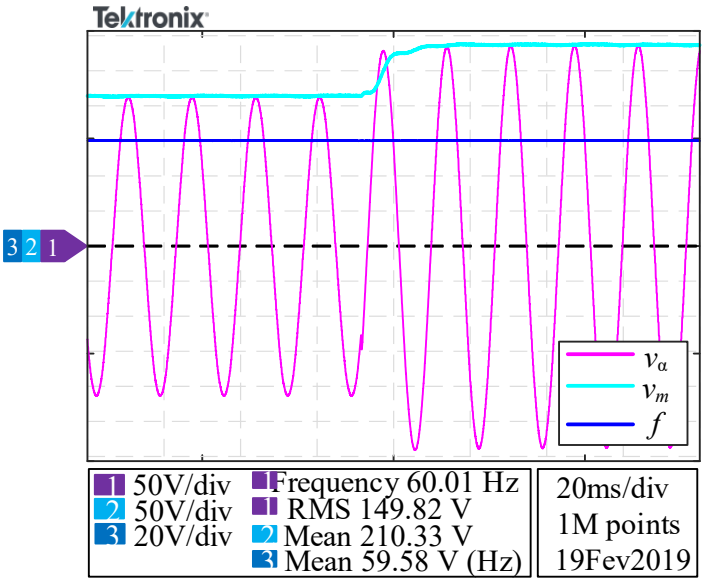


Figure 4.25 – Dynamic response due to step on the amplitude 150 to 200 Vrms at 60 Hz

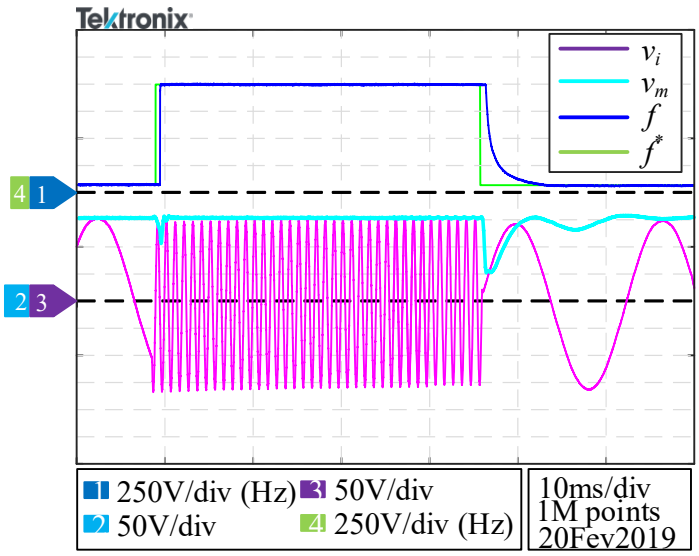


Figure 4.26 – Dynamic response due to step on the frequency – 60-1000-60 Hz at 110 V

Another feature of the system is its ability to output the orthogonal signals, v_α and v_β. They are as shown in Figure 4.27, and are required to determine the peak amplitude and the phase, θ, of the signal. All of these variables are presented in Figure 4.27 for a frequency step from 100 to 300 Hz at constant voltage of 110 V. Once again, the system was able to reach the steady state within one and a half cycles of the new frequency.

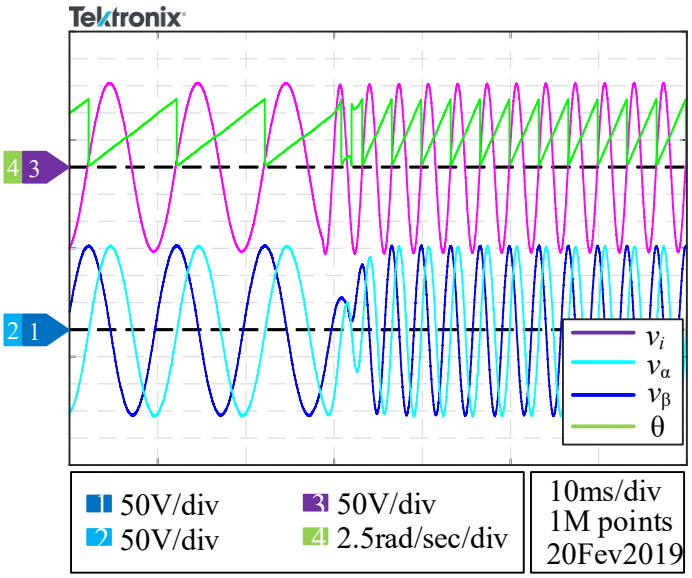


Figure 4.27 – Orthogonal signals and phase angle with a step on the frequency – 100 to 300 Hz at 110 V

4.3.3. Developed Code (C)

The code implemented on the frequency identification block in Figure 4.22 and Figure 4.23 is shown below.

```
if (x1>0) { //x1 = reference input
pos = 1; neg = 0;} else {
pos = 0; neg = 1; }
if (pos>0){
    counter++;
    if(counter > maxi){
        maxi = counter;}
    if(counter > maxi_period){
        maxi_period = counter;}
} else {
    if(maxi_period != last_maxi && maxi_period > 0){
        last_maxi = maxi_period;
        maxi = last_maxi;}
    counter=0;
    maxi_period = 0;}
if (maxi>450)
{ y1 = 1/(maxi*0.000001*2);
y2=y1*2*3.14159265359;}
//y1 – angular frequency output (Hz)
//angular frequency output (r/s)
```

4.4. Conclusion

This chapter proposed, detailed and validated two strategies for wide range Amplitude, Phase Angle and Frequency (APAF) detection. Although the techniques were initially thought to be implemented only for HPA and PHIL applications, they can also be used for grid-connected inverters or even as a part of controllers that will use this information in a feedback loop. Experimental results of both techniques demonstrated their performance for a wide range of frequency and amplitude and for dynamic scenarios.

For the first, the main benefit of the topology built is the ability to identify a single-phase signal with a wide range of frequency and amplitude, while the majority of studies operates only at a given and known frequency. The dynamic of the proposed system achieved a very fast dynamic response for APAF detection. For frequency detection, two techniques were evaluated and the second case, a Kalman Filter Based, solution provided better results for steady state and transient conditions. In addition, the proposed design procedure, which was built in a more straightforward way, enables the system to be either implemented with analog or digital devices. A set of experimental tests were performed to validate the study, under a wide range of frequency and amplitudes.

In addition, a second method was presented and detailed. The novelty is based on the fact that the range of frequencies can be wider than in studies previously presented, while keeping the system with simple implementation. The hybrid construction of the method enables one to introduce an algorithm part, designed specifically for frequency determination, which feeds into a conventional Orthogonal Signal Generation block and its following blocks consisting of a Single-Phase PLL. Experimental results demonstrated the satisfactory performance of the proposed method to track any references within the established bandwidth.

5. CONCLUSION AND PROSPECTIVE FUTURE WORK

5.1. Conclusion

A literature review was performed in Chapter 1 to identify existing limitations in well-known and established topologies of Hybrid Power Amplifier (HPA). The concept of the series and parallel associations of Linear Power Amplifiers (LPAs) and Switch-Mode Power Amplifiers (SMPA) was evaluated and the advantages, disadvantages and limitations of each were detailed. Regarding the series connected HPA, the literature is scarce on the evaluation of the power unbalance on SMPAs built with Cascaded H-Bridge Multilevel (CHBM) converter controlled with staircase modulation. The unbalance on CHBM power consumption is improved partially for rated conditions, with techniques such as the First-In First-Out (FIFO) but it is not effective for lower modulation indexes. Parallel connected HPAs allow the use of an LPA connected to a SMPA in a common coupling point with the load, increasing the capacity of providing higher currents with higher bandwidths (BW). For the specific case of machine emulation (ME), the most accurate models are the ones of the voltage-in current-out type and a proper current control scheme for the parallel-type HPA is required for ME. In addition, there is the possibility to propose a control scheme aiming at the minimum current rating necessary for the LPA, reducing the cost of the overall system. Lastly, one of the key inputs for the digital implementation of series-type HPA is the identification of magnitude and frequency from external reference signals. This requires the use of wide range Amplitude Phase Angle and Frequency (APAF) detection, which is short in the literature, mostly for single-phase systems due to the challenges required to recreate the orthogonal signals with the input. While the majority of the APAF systems concern frequencies and amplitudes varying within relatively narrow ranges, new techniques are needed for wide ranges.

Chapter 2 proposed a technique that mitigates the unbalance issue in CHBM converters operating with staircase modulation, based on the Nearest Level of Control (NLC). The technique is called Split-Voltage First-In First-Out (SV-FIFO). Together with the technique, an isolated analog controller, with feedforward of the SMPA voltage, was devised for implementation with a commercial LPA (AE Techron 5050LVC). The SMPA was a custom built, six-cell CHBM converter implemented in a Real-Time Simulator (RTS) from OPAL-RT, the OP4510. The algorithm requires suitable estimation of the magnitude and frequency of the reference output voltage, which was performed using a technique detailed in Chapter 4. Existing techniques such as First-In Last-Out (FILO) and First-In First-Out (FIFO) were modeled and compared with the

proposed technique in simulation and experimental analysis. The experimental analysis validated the improvements on the power balance and the ability of the digital and analog controllers to properly regulate the output voltage for steady state and dynamic conditions, such as steps on amplitude and frequency. Ranges and steps from amplitude of 35 Vrms to 220 Vrms and frequencies from 60 Hz to 1 kHz were implemented. The benefits of SV-FIFO are more relevant with lower modulation indexes, in which with the existing techniques, some cells would not be used, causing even higher unbalances. The technique is able to ensure better balanced power consumption, for all ranges of output voltages, while keeping the Total Harmonic Distortion (THD) below 5%. While SV-FIFO improved the unbalance issue for a CHBM based HPA for resistive loads, the Independent Load Balancing method tackled the issue for different linear load characteristics (combinations of resistive, capacitive and inductive loads). The proposed solution, which still relies on the primary angles given by the NLC, improves the power balance between the cells for all load characteristics as shown in the modelling and simulation results. The technique presents a lower standard deviation than the other techniques for all the range of angles of the load, with the additional cost of a higher computational burden and the need to read or sense the output current.

In Chapter 3 an ME application was proposed based on a high bandwidth LPA in parallel association with a high current capacity SMPA. Using high precision voltage-in current-out machine models in the HPA, a new control was proposed to ensure the minimal contribution of current from the LPA, which is directly related with the cost of the system. Selecting the bandwidth of the SMPA (BW_{SMPA}), as a fraction of the one from the LPA, BW_{LPA}, enables the first to contribute with the bulk part of the transient currents and with the whole steady state current and the second to compensate on the missing part of the transient currents and the switching harmonics introduced by the SMPA in steady state. The combination of both creates an ME system with a fast dynamic response due to the high BW_{LPA}, and with high current output because of the SMPA. The control logic is implemented with PI controllers in the rotating ($dq0$) reference frame producing no errors in steady state. Considering the trade-off between accuracy and cost the HPA system showed superior performance in the simulations when compared to an ME system implemented with a SMPA or an LPA. For simulations and for experimental performance evaluation of the proposed parallel HPA, the ME system has been set to emulate a Direct On-Line (DOL) start-up of an Induction Machine (IM). By the analysis of different control bandwidths and switching frequencies

of the SMPA, the LPA peak current contribution to the HPA could be reduced from 44.31% to 12.32%. In addition, the SMPA output THD achieved values from 9.80% to 2.84%, but the proposed control ensured that the LPA compensated it, with different efforts for each scenario, outputting an HPA THD of 1% across all ranges of bandwidth and switching frequencies. This means that the performance of the HPA, in terms of accuracy, remains the same, determined by the closed loop BW of the LPA. The controller also shows the ability of the LPA in compensating for the SMPA's fifth and seventh harmonics introduced by its dead-time.

Wide range APAF detection required for the implementation of the improved series HPA was investigated in Chapter 4. Considering the simulation results, the first proposed system was the best performing in several cases and the only one able to perform with small errors at all ranges of the input signal. Its performance was benchmarked against several other APAF techniques. The proposed APAF was validated experimentally with a frequency ramp from 60 to 1000 Hz with a duration of 5 s (±188 Hz/s), with voltage steps from 1-2-1 pu and frequency steps 500-750-500 Hz. An important experimental test was performed based on the phase inversion, where the technique could quickly readjust and identify the input orthogonal signal and most importantly, the phase angle. These tests are not quite common because the majority of studies operate only at a given and known frequency and with small freedom on the amplitude identification. The use of Kalman Filters in the block of frequency identification showed better performance when compared to the implementation with low pass filters. The second proposed system is beneficial in terms of simplicity, since it is based on zero-crossing detection. One limitation of both techniques is that they were designed and tested for ME and ACPS applications, in which the references are usually noise-free sinusoidal waveforms. For grid-tied systems, there are more components, like noise and low order harmonics, which were not evaluated in this study. The second proposed system was also validated experimentally for frequency and amplitude steps and phase angle inversion, showing excellent performance in all tests. This technique is based on the sample time of the RTS and its accuracy is directly connected to it.

5.2. Future Work

The series configuration of the HPA was investigated in Chapter 2. An experimental set-up was built with six H-bridges fed from unidirectional DC power supplies. It allowed the demonstration of the benefits of the SV-FIFO technique for power balance among H-bridges in an

Alternating Current Power Supply. It could also be used for the emulation of an AC machine as a generator. However, for operation of the AC machine in the motor mode, the DC power supplies of the H-Bridges should be replaced with bidirectional ones. Besides, the experimental set-up could be expanded to emulate three-phase machines. Lastly, one could conduct the practical validation of the ILB technique, for low modulation indices and non-linear loads.

The parallel configuration of the HPA for an ME system was discussed in Chapter 3 and tested for the direct online (DOL) start-up of an Induction Machine (IM) connected to the power grid. The connection of the HPA-ME with an inverter or variable frequency drive can also benefit in testing the machine models or the inverter itself, for normal and faulty conditions. Although the inclusion of another system with the existing SMPA and LPA can be of high complexity, there are clear advantages, as the possibility to control the ME with variable speed and dynamic input voltage.

Regarding the APAF detection, the two proposed techniques were evaluated for sinusoidal inputs, and a few dynamics on the input side were evaluated. As their implementation was designed mostly for HPA applications, it was assumed that the external reference signals are noise-free, coming from RTS or microcontrollers close by. Considering the proposed APAF techniques for grid-tied systems, there are more effects that were out of the scope, such as noise, effect of low order harmonics and DC gains on the signals that must be taken into account. There are chances to introduce filters on the input signal, which will mitigate the negative impact of the mentioned effects.

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