Design of a Triple-Mode Low Power Single-Ended Source-Series-Terminated Driver

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Abstract

Design of a Triple-Mode Low Power Single-Ended Source-Series-Terminated Driver

Sara Mahran

In data centers, the multi-mode fiber (MMF) links and vertical cavity surface emitting laser (VCSEL) diode are widely used for short-reach optical communications (< 100 m) because of their low cost and their ability to handle the ever-increasing data rates. In conventional VCSEL drivers, the laser diode driver (LDD) can be bonded to a chip carrier, while the host chip is bonded to another chip carrier. This host chip contains an electrical link driver and is connected to the VCSEL driver via a short electrical link. To reduce the overall power consumption of the conventional VCSEL driver system, the electrical link driver in the host chip can be modified so that it can drive the VCSEL diode directly, eliminating the laser diode driver. Thus, the modified driver can drive either an electrical link or a VCSEL diode. By modifying the packaging, the VCSEL diode can be wire bonded to the host chip and directly driven.

Driving a VCSEL diode requires features such as asymmetric equalization, relatively low modulation current, and DC current source to bias the VCSEL. On the other hand, driving an electrical link requires symmetric equalization, relatively high output voltage swing from the driver, and matched output impedance. Accordingly, a typical electrical link driver cannot drive a VCSEL diode and the VCSEL driver is not suitable for driving an electrical link. The proposed design is a single-ended source-series-terminated (SST) voltage-mode driver in a CMOS 65 nm technology with three driving modes: driving electrical links with losses up to 16 dB (mode I), driving VCSEL diodes through a short electrical link (mode II), and driving VCSEL diodes directly wire bonded to the driver (mode III). The proposed design provides a tunable output swing without changing the driver output impedance and achieves a smooth transition between symmetric and asymmetric equalization as needed. In simulation, the proposed triple-mode driver operates up to a bit rate of 20 Gb/s, and dissipates at most 27.6 mW of power when operating at mode II when using a supply voltage of 1.2 V.

Acknowledgments

I would like to thank my supervisor, Dr. Glenn Cowan, for his guidance and support throughout my master's program. I would also like to thank my co-supervisor, Dr. Odile Liboiron-Ladouceur (McGill University, Montreal, QC, Canada) for her continuous technical support. In addition, I would like to acknowledge the financial support from the Gina Cody Faculty of Engineering at Concordia University and the Natural Sciences and Engineering Research Council (NSERC) of Canada. Furthermore, I am sincerely grateful for the financial support I received from the Microsystems Strategic Alliance of Québec (ReSMiQ). I also acknowledge the technical support of the Canadian Microelectronics Corporation (CMC) for the use of their Computer Aid Design (CAD) tools. I am grateful to Ted Obuchowicz for his guidance in using Cadence. I would like to thank my colleagues Diaa Abdelrahman, Di Zhang, and Sami Sattar for their advice and motivation.

I am deeply thankful to my husband for his support and motivation during my study and research period. I owe a large portion of this success to my mom, dad, and siblings for their endless encouragement and support.

Dedicated

To

My husband

His love, advice, help, and patience make me able to get such success

My parents

Their love, support, and prayers encourage me to work harder

My siblings

Their encouragement helps in not giving up

My daughter

Her smile and hug help in getting over the hard times

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List of Acronyms

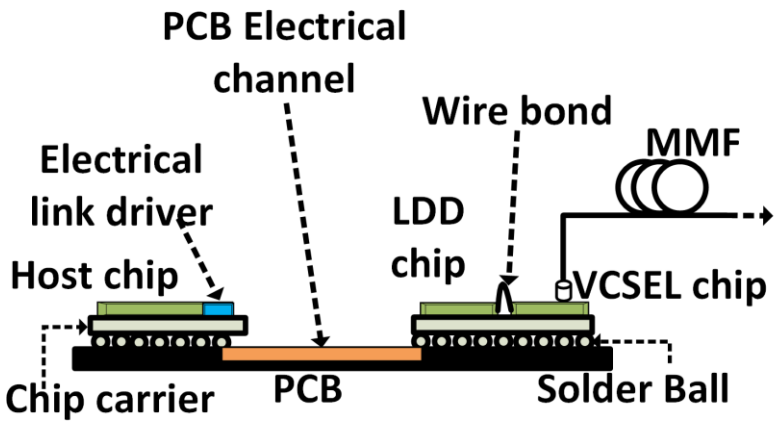
CDR	Clock and data recovery
CML	Current mode logic
CMOS	Complementary metal-oxide-semiconductor
ESD	Electro-static discharge
FFE	Feed forward equalization
HEO	Horizontal eye opening
I/O	Input-output
ISI	Inter-symbol interference
KVL	Kirchhoff's voltage law
LDD	Laser diode driver
MMF	Multimode fiber
NRZ	Non-return to zero
OMA	Optical modulation amplitude
PAM-4	Pulse amplitude modulation four levels
PCB	Printed circuit board
PD	Photodetector
PRBS	Pseudo random bit stream

SST	Source-series-terminated
TIA	Transimpedance amplifier
UI	Unit interval
VEO	Vertical eye opening
VCSEL	Vertical cavity surface emitting laser
VML	Voltage mode logic

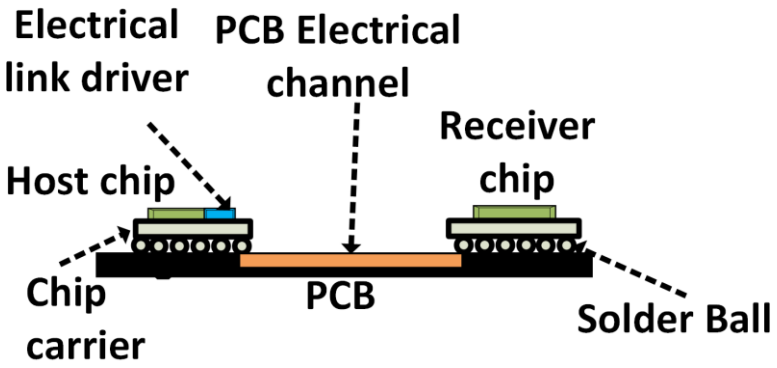
Chapter 1 Introduction

1.1 Research motivation

Multi-mode fiber (MMF) links and vertical cavity surface emitting laser (VCSEL) diodes are widely used for short-reach optical communications (< 100 m) in data centers due to their relatively low cost. The use of fiber links and VCSEL diodes helps handling the ever-increasing data rates which cannot be handled via copper channels. MMF links provide better performance than copper channels as they do not introduce frequency dependent losses. VCSEL drivers are used to directly modulate the optical carrier with the data to be transmitted. In typical VCSEL-based systems, the laser diode driver (LDD) is on one chip carrier, while the host chips (i.e., the data producer) associated with the laser driver are located on another chip carrier (see Fig. 1.1(a)). The host chip contains an electrical link driver and is connected to the VCSEL driver via a short electrical link on a printed circuit board (PCB). To reduce the power consumption in this type of system, the electrical link driver in the host chip can be modified so that it can drive the VCSEL diode, eliminating the stand-alone LDD. This modified driver can drive either an electrical link (Fig. 1.1(b), mode I) or a VCSEL diode through the same electrical link (mode II). By modifying the packaging of the host chip, the VCSEL diode can be wire bonded onto the host chip and can directly be driven (mode III). Designing a modified low-power driver (see Fig. 1.1(c)) that can work in all the previously mentioned modes (based on the given application) is an interesting and significant proposal to reduce the overall cost of the transmitter. With such driver, the proposed design can work in short-reach optical communications or die-to-die communications (i.e., transceiver systems between processor and memory or between the multiple cores of the CPU).



(a)



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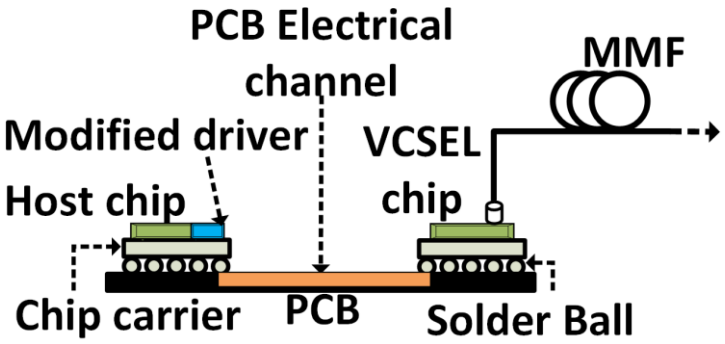


(c)

Fig. 1.1 Different chip-to-chip interconnection architecture on PCB for: (a) typical VCSEL driver, (b) typical electrical link driver, and (c) proposed driver.

To compensate for the VCSEL nonlinear behavior and channel loss, features like feedforward equalization (FFE) need to be added to the proposed design. Equalization can be either symmetrical in the case of driving an electrical link or asymmetrical when driving a VCSEL diode biased at low current.

VCSEL drivers are designed using current mode logic (CML) or voltage mode logic (VML). A CML driver is more straightforward to be designed as the output impedance depends on the drain resistor. However, it consumes more power. Although a VML driver consumes less power, it is more complex to be designed especially when impedance matching is required. This is mainly attributed to the on-state resistance of the transistors. In VCSEL drivers, impedance matching of 50 Ω is not required such that the output impedance of the drivers can be larger than 50 Ω. Based on the literature [1-4], the driver output impedance is recommended to be lower than 100 Ω to reduce the ringing in the optical output power. In typical electrical link drivers, VML inverter scheme-based drivers necessitate additional circuits to match the link impedance [5,6]. In the work reported in [6,7], the output impedance is 50 Ω to match the link impedance, but the used equalization techniques are unable to compensate for the VCSEL's nonlinear behavior. Indeed, these drivers do not contain the logic to differentiate between the rising and falling edges such that the equalization of both edges is performed in the same manner. Furthermore, these electrical link drivers naturally do not contain the bias current circuits as it is not needed in such drivers. A bias current circuit is needed in VCSEL drivers to bias the VCSEL above the threshold current (i.e., forward biasing) to reduce the ringing in the optical output power due to the relaxation and turn-on delay.

Adding an electrical link between the VCSEL diode and a typical VCSEL driver is currently not feasible as the driver output impedance does not match the required impedance for the electrical link. Furthermore, connecting a VCSEL diode to the electrical link driver is not recommended since compensating the VCSEL nonlinear behavior is necessary. The compensation of the nonlinear behavior requires asymmetric equalization. Typical electrical drivers also lack the bias current circuit to forward bias the VCSEL diode.

The modulation current required for a VCSEL diode can be relatively small as long as the optical output power is suitable to meet the optical receiver sensitivity considering the link margin. Driving

a VCSEL diode in such case does not require large output current amplitude (i.e., modulation current), leading to reduce the power consumption for the transmitter.

In our proposal, the output signal amplitude from the driver must change without altering the impedance matching condition to ensure good signal integrity and exhibit good energy efficiency. Accordingly, there is a need to develop a driver that can:

- provide tunable output impedance (from 50 Ω to 200 Ω) to match the VCSEL or the electrical link impedances,
- provide both symmetric and asymmetric equalizations with smooth toggling between them,
- offer tunable output signal amplitude without affecting the output impedance of the driver,
- provide a biasing current to the VCSEL diode when driving the VCSEL directly or through an electrical link and disable such feature when driving an electrical link.

1.2 Objectives

The design and implementation of a low-power high-speed VML source-series-terminated (SST) electrical link driver which can also drive a VCSEL diode are presented and discussed in this dissertation. This proposed electrical driver design has the following features:

- Drives a microstrip electrical link with a length up to 5 cm introducing a total loss of 16 dB at the Nyquist frequency including the wire bonding and the capacitor associated with the electrostatic discharge (ESD) protective circuit.
- Drives a VCSEL diode through an electrical link with 16 dB loss.
- Drives a VCSEL diode directly without an electrical link.
- Exhibits lower power dissipation in the transmitter compared to those reported in the literature.
- Operates at data rates up to 20 Gb/s.

- Offers output impedance to match the 50 Ω electrical link impedance to reduce reflections.
- Offers a tunable output impedance from 50 Ω to 200 Ω to match the VCSEL impedance through changing the number of the source-series-terminated (SST) slices.
- Toggles between symmetric and asymmetric equalization based on the selected operating mode by using edge detectors and changing the number of the SST slices.
- Achieves a suitable modulation current range when operating in the VCSEL driver mode (1.5 mA to 4.5 mA) through using a voltage regulator.
- Implements a VCSEL bias current circuit that can be disabled when the proposed design operates in the electrical link driver mode.
- Enables a low modulation current when the proposed design operates as a VCSEL driver to save power.

Table 1.1 summarizes achievable specifications of conventional chip-to-chip interconnection systems (columns VCSEL drivers and electrical link drivers) and what is achieved in the proposed design (last column).

Table 1.1 Modes of operation requirements comparison.

	VCSEL drivers	**Electrical link drivers**	**Triple mode proposed system**
Output current swing	Between 1.5 mA [4] and 8.5 mA [1]	High to mitigate inter-symbol interference (ISI) (e.g., 2.2 mA [7], 7 mA [8])	Tunable (1.5 mA to 4.5 mA)
DC biasing current	Above threshold current (i.e., 0.6 mA [11])	Not Applicable	Enable (2.5 mA) /Disabled
Equalization	Asymmetric	Symmetric	Symmetric/ Asymmetric
Output impedance	Lower than 100 Ω	50 Ω	Tunable (50 Ω to 200 Ω)

1.3 Contribution

This work presents the design and implementation of a high-speed low-power electrical link circuit with flexible driving capabilities. The proposed design can:

- Eliminate the required stand-alone laser diode driver which saves about 58.6% of power consumed in the conventional VCSEL driver systems.
- Drive an electrical link, a VCSEL diode through an electrical link, or a VCSEL diode directly (i.e., a low-power multi-purpose driver circuit).
- Provide adjustable output impedance to match the electrical link impedance with low signal reflection and low ringing in the VCSEL optical output power.
- Achieve tunability of the output current modulation without affecting the output impedance of the proposed design.
- Achieves lower energy efficiency (~ 27% in mode I and ~ 19% in mode II) through changing the output current signal amplitude without affecting the output resistance.

1.4 Contribution to research

Two significant contributions were made which were disseminated to the research community.

1. A preliminary design including the first two mode of operations (mode I and II) has been presented and published in the proceedings of the IEEE Midwest Symposium on Circuits and Systems (MWSCAS) 2021 conference:

   S. Mahran, O. Liboiron-Ladouceur, and G. Cowan, "20 Gb/s Dual-Mode SST VCSEL Driver," *2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2021, pp. 428-431, (virtual).

S. Mahran: contributed to the idea, performed all analysis and simulations, drafted the manuscript, and presented the work at the conference.

O. Liboiron-Ladouceur: co-supervised the work, edited, and reviewed the manuscript.

G. Cowan: proposed the idea, supervised the work, edited, and reviewed the manuscript. He also reviewed the slides and provided feedback in the presentation delivery.

2. The complete driver design which includes the three modes of operation had been accepted by The International Symposium on Circuits and Systems (ISCAS) 2022 conference.

S. Mahran, O. Liboiron-Ladouceur, and G. Cowan, "Triple-Mode Low-Power 20 Gb/s SST Driver for Short Reach Interconnects," *2022 IEEE International Symposium on Circuits and Systems (ISCAS),* 2022.

S. Mahran: proposed the idea, performed all analysis and simulations, and drafted the manuscript.

O. Liboiron-Ladouceur: co-supervised the work, edited, and reviewed the manuscript.

G. Cowan: supervised the work, edited, and reviewed the manuscript.

1.5 Thesis organization

The thesis contains five chapters. In Chapter 2, the fundamentals and background related to the proposed circuit and applications are presented. Chapter 3 introduces the electrical channel model used as well as the VCSEL modeling. The equalization strategy and the proposed driver design with simulation results are presented in Chapter 4. Finally, the conclusion is presented in Chapter 5 and the possible future work directions have been discussed.

Chapter 2 Fundamentals and background

2.1 Introduction

In electrical chip-to-chip interconnection systems as illustrated in Fig. 2.1, data is transmitted from the transmitter side to the receiver side via an electrical channel. The output impedance of the driver and the input impedance of the receiver are key parameters when designing a transceiver. To reduce the reflections of the signal propagating through the electrical link, both impedances (i.e., output impedance of the driver and input impedance of the receiver) should be equal to the characteristic impedance of the electrical channel (i.e., matched impedances).

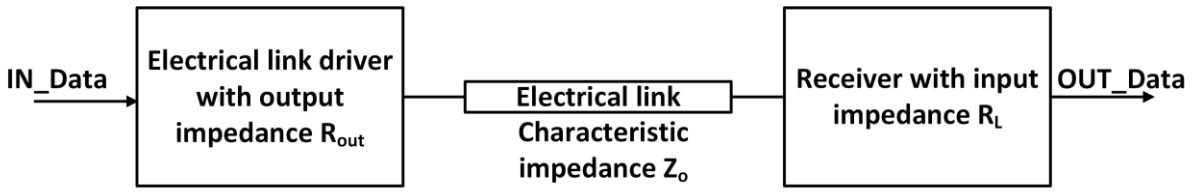


Fig. 2.1 Conventional chip-to-chip interconnection system.

In an optical communication system, (Fig. 2.2), the transmitter consists of a laser diode driver (LDD) which modulates the current to the laser diode. The modulated optical signal from the laser diode propagates through an optical multimode fiber (MMF) of length less than 100 m (i.e., short reach optical communications) to the receiver side (RX). MMF links have better signal integrity performance compared to copper links, as they have no frequency dependent losses and are immune to electromagnetic interference. The receiver consists of a photodetector (PD) that converts the modulated light with data to current. The photocurrent from the PD is the input signal to the transimpedance amplifier (TIA). The TIA converts the current to voltage with some amplification. Then, this voltage is amplified further through the receiver main amplifier leading

to large enough signal to drive the clock and data recovery unit (CDR). The CDR unit is used to synchronize the received data with the internal clock to regenerate the data (OUT_Data) for the electrical processing element.

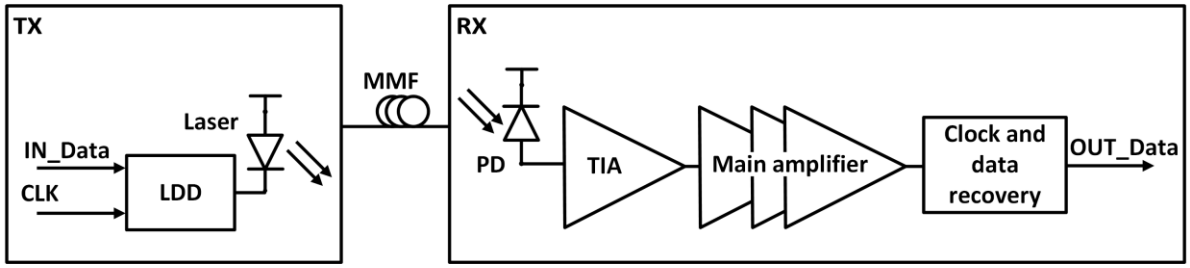


Fig. 2.2 Typical VCSEL-based multimode optical link. TX: transmitter; RX: receiver; MUX: multiplexer, LDD: laser diode driver, MMF: multimode fiber, PD: photodetector, TIA: transimpedance amplifier.

Electrical channels in a transceiver system introduce a non-negligible frequency dependent loss which affects the transmitted data due to inter-symbol interference (ISI). ISI is a distortion in time of the transmitted pulses, in which one pulse interferes with subsequent pulses due to pulse spreading in time. The maximum ISI can be calculated from the system pulse response. The pulse response shown in Fig 2.3 is used to quantify the ISI of a link when the transmitted data consists of an isolated binary "1" or an isolated binary "0". The maximum ISI (ISI_{max}) is the sum of the pre/post pulse cursors (h_k) illustrated in Fig. 2.3:

$$ISI_{max} = \sum_{k \neq 0} |h_k| \qquad \text{Eq. 2.1}$$

Fig. 2.4 illustrates the impact of ISI on the transmitted data. ISI increases the number of errors in the data at the receiver side.

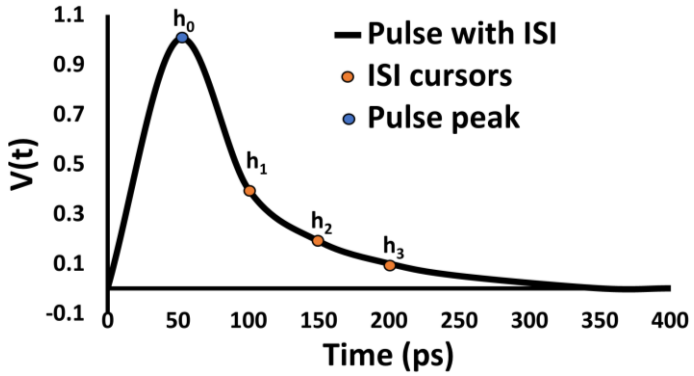
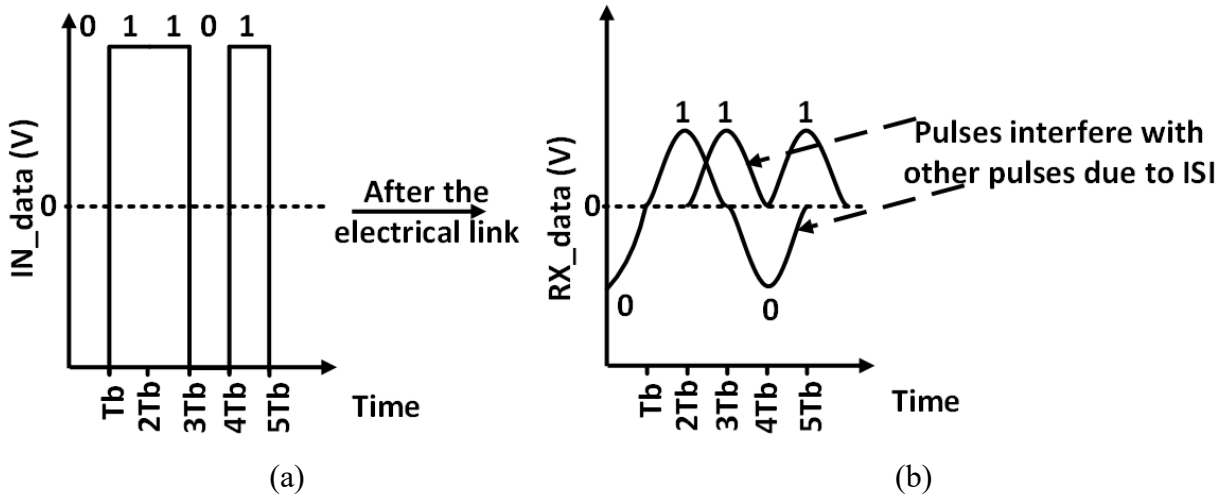


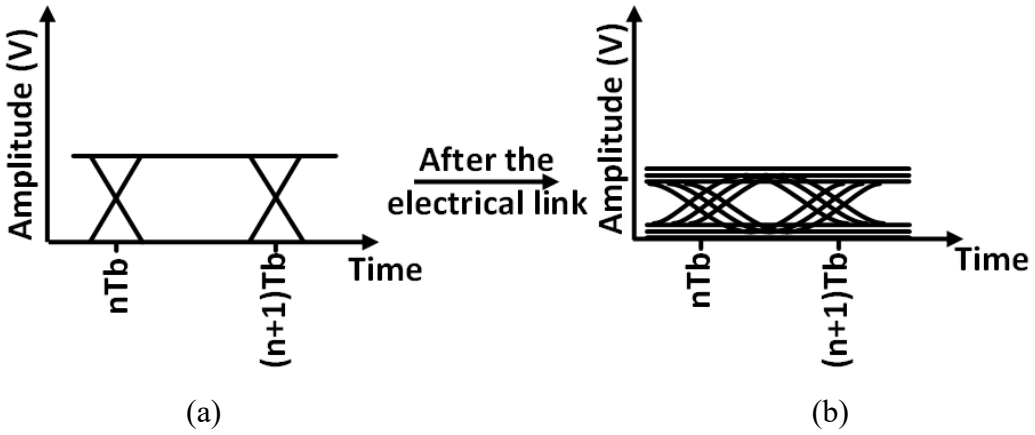
Fig. 2.3 An example of a system pulse response.



(a) (b)

Fig. 2.4 Illustration of ISI effect on the transmitted data: a) original pulses, and b) spreaded pulses in time due to ISI. Tb: bit period; n: an integer greater than 0.

Such interference leads to worsen signal integrity of the transmitted data, causing smaller height and width of the eye diagram. An eye diagram is a time domain representation of overlaying sections for a digital signal. Fig. 2.5 shows the impact of ISI on the eye diagram where the width and height are reduced.



(a) (b)

Fig. 2.5 A comparison between the transmitted and received eye diagrams: (a) without ISI effect, and (b) with ISI effect. Tb: bit period; n: an integer greater than 0.

The vertical eye opening (*VEO*) of the eye diagram is determined based on the amount of the ISI in the spreaded pulses. The value of VEO is the difference between the main cursor (h_0 in Fig. 2.3) and the maximum ISI calculated in Eq. 2.1:

$$VEO = 2(h_o - ISI_{max}) \qquad \text{Eq. 2.2}$$

Equalization strategies in drivers compensate for the VCSEL nonlinear behavior, or for the loss introduced by the electrical links. In general, feedforward equalization (FFE) is an equalization strategy in which the delayed version of the signal is subtracted from the original signal [1]. This delayed signal is scaled by a ratio (a quantity referred as the equalization ratio or the tap coefficient) less than one. This ratio is also based on the ISI in the system's pulse response. The equalization ratio α (Eq. 2.3) is the amount of the ISI cursor (e.g., h_1 in Fig. 2.3) divided by the main cursor (h_0).

$$\alpha = \frac{h_1}{h_o} \qquad \text{Eq. 2.3}$$

As shown in Fig. 2.6, the original (i.e., received) pulse (V_{RX}) occupies more than one bit duration (T_b). This is due to the frequency dependence of the electrical link, leading to ISI. When a delayed scaled pulse version ($V_{Rx}\,(t - T_b)$) is multiplied by the equalization ratio (α) and subtracted from

the original signal (Eq. 2.4), a pulse (V_{Eq}) occupying only one T_b is generated. This leads to an ISI-free signal. This is the basis of equalization techniques.

$$V_{Eq}(t) = V_{RX}(t) - \alpha * V_{Rx}(t - T_b) \qquad \text{Eq. 2.4}$$

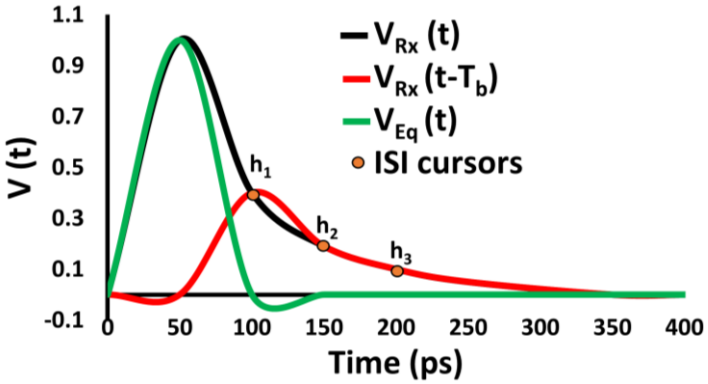


Fig. 2.6 The transmitted and received signal (black), ratioed and delayed signal (red), and equalized (green) signal.

FFE is used in the transmitter side of the electrical link drivers and VCSEL drivers to compensate for the channel loss and VCSEL nonlinear behavior, respectively. Transmitter side pre-emphasis FFE enlarges the amplitude of the first transmitted bit compared to the second bit (see Fig. 2.7).

There are two types of equalization: a) symmetric equalization, and b) asymmetric equalization. Fig. 2.8(a) shows the block diagram of the symmetric equalization in which the rising and falling edges of the signal are equalized by the same equalization ratio. It consists of main tap with an input (IN_Data (n)) and equalizer tap with a delayed version (one T_b delay) of the input (IN_Data (n-1)). To achieve equalized output, the outputs of both taps are added together. The block diagram of the asymmetric equalization is shown in Fig. 2.8(b) in which the rising and falling edges of the signal are equalized by different equalization ratios (α and β). Fig. 2.8(b) includes the main tap with an input, as well as the falling edge equalizer and rising edge equalizer taps. To apply a certain equalization ratio to either the rising or the falling edges, the input of both rising and falling edges

equalizers need to be connected to the edge detector. The main signal and the delayed version of the signal are the inputs to the edge detector to identify the edge type.

An example of an edge detector is shown in Fig 2.9. Both negative and delayed versions of the data are inputs to a NOR gate. The output of this NOR gate represents a high pulse at the position of the rising edge of the original data (i.e., from $2T_b$ to $3T_b$). When these two inputs are applied on a NAND gate, the output is a low pulse at the position of the falling edge of the original data (i.e., from $4T_b$ to $5T_b$).

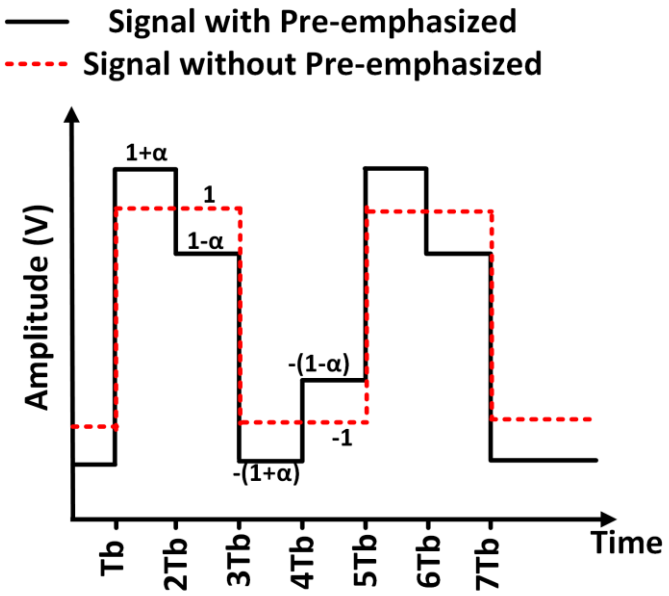
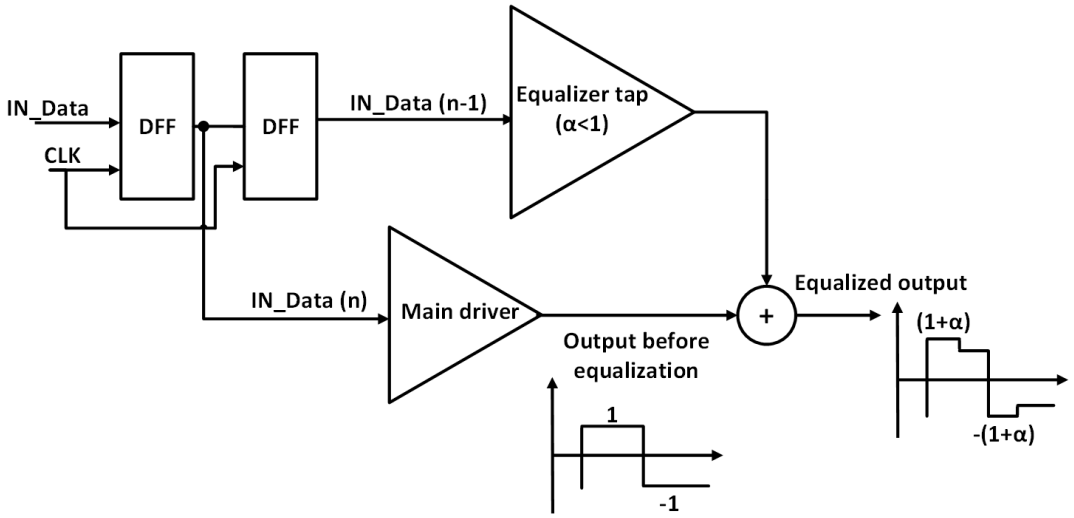
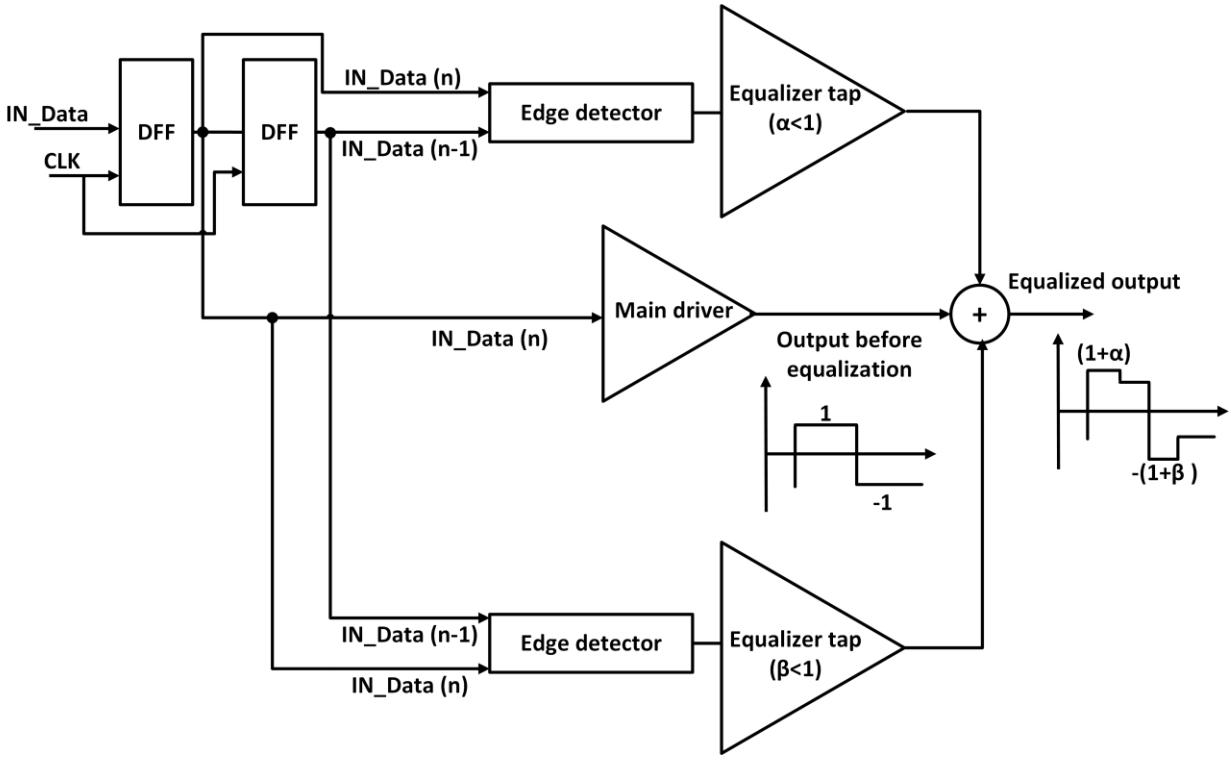


Fig. 2.7 The effect of the pre-emphasis FFE on the original data signal.



(a)



(b)

Fig. 2.8 Basic concept for the types of the transmitter side FFE: (a) symmetric equalization, and (b) asymmetric equalization.

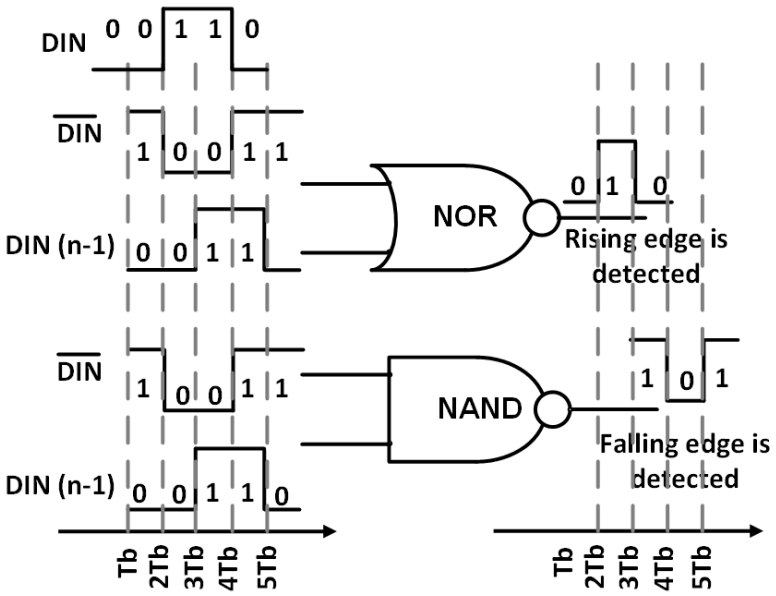


Fig. 2.9 Example for the rising and falling edge detectors.

Since the power consumption is an important parameter in designing either a VCSEL driver or electrical link driver, the driver energy efficiency is an essential metric to be calculated. The energy efficiency is the amount of the power consumed by the driver divided by the data rate of this driver, and it is measured in picojoule per bit (pJ/bit). The value of the energy efficiency equals to 1.5 pJ/bit or less [3,4,8,13,14].

2.2 Laser diode

Laser diodes are semiconductor devices which generate coherent photons when pumped with a current. Laser diodes have a narrow spectral line with the optical output power centered around one wavelength (λ_o), see Fig. 2.10. The input current of the laser should be greater than its threshold current to ensure carrier population inversion leading to stimulated emission. As shown in Fig. 2.11, when the current is less than the threshold, the output power is relatively small. However, when the current is above the threshold, the output power linearly increases until being saturated [10].

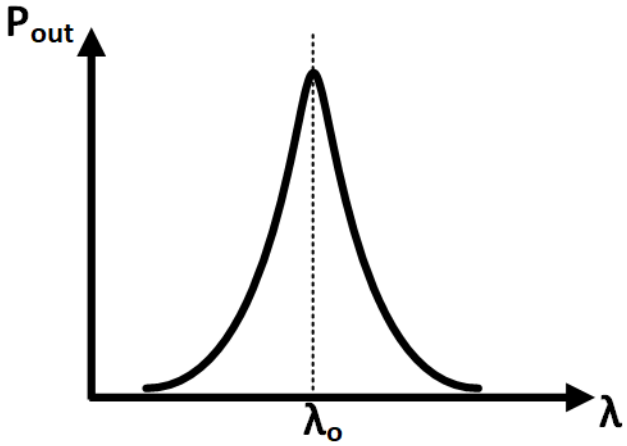


Fig. 2.10 The theoretical output spectrum of the laser.

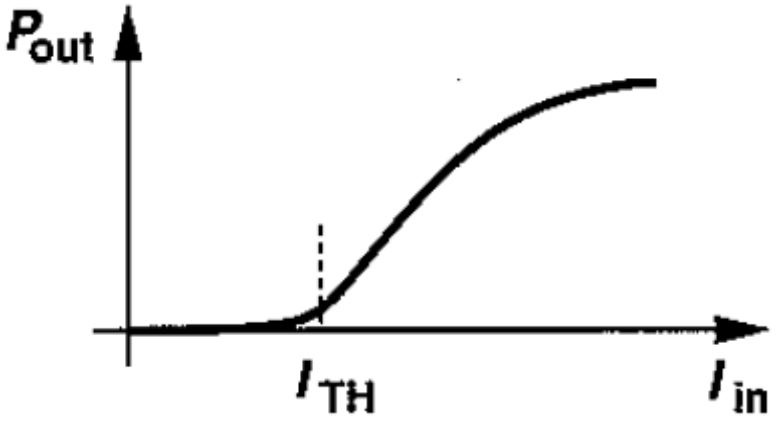
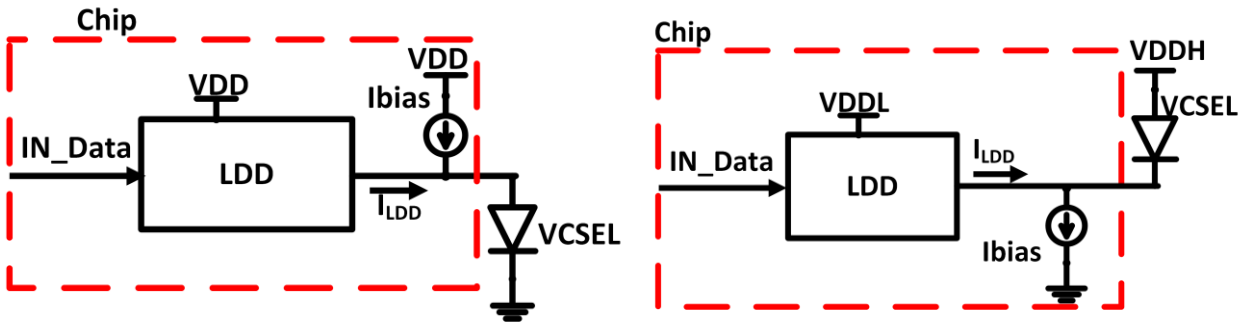


Fig. 2.11 Laser diode characteristics [10].

There are different laser types such as Fabry-Perot laser, distributed feedback laser, and VCSEL. The first two types are not practical for wafer-level testing; however, VCSEL can be used in this kind of testing, and it can be implemented at low cost. To simulate and optimize the VCSEL drivers, an accurate VCSEL model is needed considering the nonlinear behavior of the VCSEL diode towards binary “1” and binary “0”. The model and the nonlinear behaviour of the VCSEL diode will be discussed in detail in the following chapter.

2.3 Laser diode drivers

VCSEL diodes are used in short (< 100 m) and medium (< 300 m) reach data center interconnections as they offer low threshold current and can be implemented and fabricated at low cost [1]. A VCSEL diode has two contacts: a) anode (positive), and b) cathode (negative). VCSEL can be driven in a common anode configuration, or a common cathode configuration as shown in Fig. 2.12 [3,4]. In the common cathode configuration (see Fig. 2.12(a)), the driver and the VCSEL are biased via a high supply voltage (e.g., 3.3 V [2]). In the common anode configuration (see Fig. 2.12(b)), the driver is biased using a low voltage (1 V to 1.2 V). However, the VCSEL is forward biased using an external higher supply voltage (e.g., 2.75 V [3]). Another way to bias the VCSEL in a common cathode configuration is to use a low supply voltage for the driver and external negative supply voltage for the VCSEL diode.



(a) (b)

Fig. 2.12 VCSEL driving topologies (a) common Cathode, (b) common anode.

A VCSEL diode has different response towards binary “1” and binary “0” pulses (discussed in detail in Chapter 3). Therefore, asymmetric equalization should be used when implementing a VCSEL driver. Edge detectors are used with the asymmetric equalization to differentiate between the rising and falling edges.

Both the laser diode driver and electrical link driver can be designed based on two modes of operation, namely voltage mode logic (VML) or current mode logic (CML) [3,4]. VML schemes consume less power compared to CML schemes. The circuit implementation in VML is complex, especially when impedance matching is required [7]. The output impedance of VML drivers depends on the on-state resistance of the switches. This on-state resistance is nonlinear and more sensitive to process variations [9]. This is because the on-state resistance depends on certain parameters that can change during fabrication (e.g., the transistor's length, width, and oxide thickness) as shown in Eq. 2.5. CML-based drivers are easier to be designed when impedance matching is required. The CML output impedance depends on the drain resistor which is less sensitive to the process variations [9].

$$R_{ON} = \frac{1}{\mu_n * C_{ox} * \left(\frac{w}{l}\right) * (V_{GS} - V_{th})} \quad \text{Eq. 2.5}$$

2.3.1 Voltage mode VCSEL drivers

Conventional VML VCSEL drivers are based on the push-pull inverter scheme shown in Fig. 2.13(a). In this scheme, the current signal is injected to the VCSEL through the pull-up (PMOS), or the pull-down (NMOS) transistors. The inverter-based scheme can be replaced by a Thevenin-equivalent series termination as shown in Fig. 2.13(b). As shown in Fig. 2.13(b), to achieve a specific output swing at the output node (V_{OUT}), the required current (I) is equal to $\frac{V_{OUT}}{R_{Load}}$ (when R_{Load} and R_{ON_state} are matched). This current represents half the value of the CML schemes current which will be discussed in section 2.3.2. Therefore, the power consumption of the VML drivers is relatively low compared to the CML drivers. The output impedance of these drivers depends on the on-state resistance of the NMOS and the PMOS transistors which are sensitive to process variations [9].

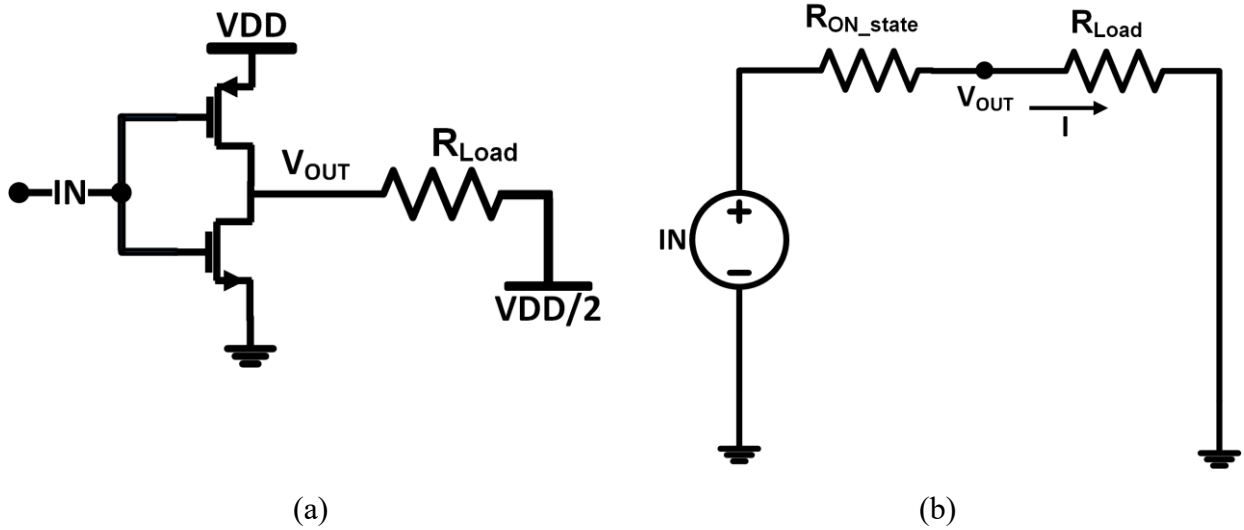
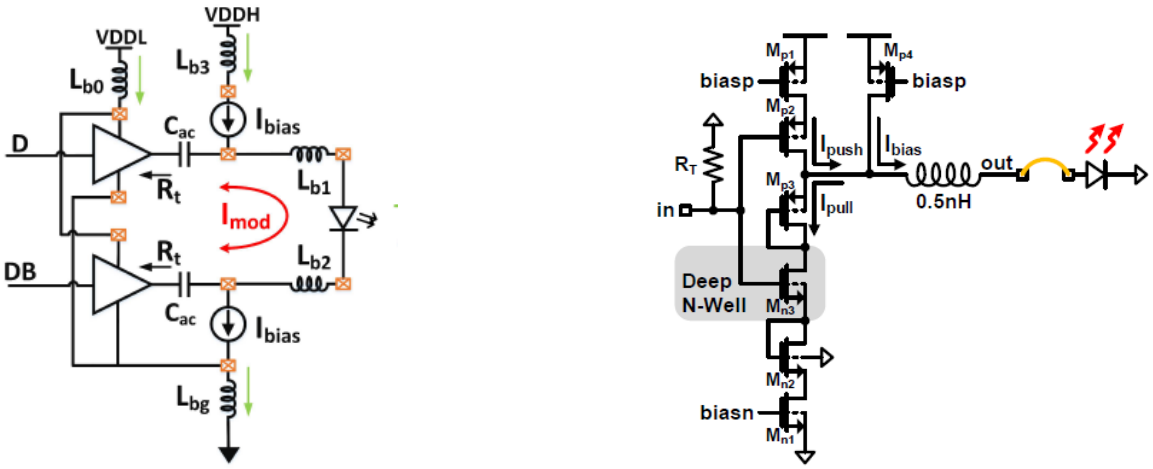


Fig. 2.13 Voltage mode logic (VML): (a) inverter-based scheme, and (b) the equivalent schematic of the VML inverter-based scheme.

In a pervious study [3], a 16 Gb/s differential VCSEL driver in 65 nm CMOS technology is proposed. As shown in Fig. 2.14(a), the differential circuit is based on the VML inverter scheme, and the VCSEL is biased in a common anode configuration (Fig. 2.12(b)). The design provides edge detectors and asymmetric equalization to compensate for the VCSEL nonlinear behavior. In this study, the VCSEL diode is connected to the driver via a large AC coupling capacitor (20 pF) such that the proposed driver is unaffected by the parasitic inductances from the supply voltage (VDDL). The usage of the AC coupling capacitors introduces a low cut-off frequency issue leading to bandwidth reduction. To mitigate such issue, a low-frequency driver is added to reduce the value of the AC coupling capacitor to 1 pF. The output impedance of this driver is about 100 Ω to reduce the ringing in the VCSEL output power. The design offers an energy efficiency of 1.52 pJ/b, and the supply voltages for this design are 1.05 V for VDDL and 2.75 V for VDDH.

In another work [4], a 35 Gb/s single-ended inverter scheme asymmetric VCSEL driver in 65 nm CMOS technology is introduced (Fig. 2.14(b)). The VCSEL diode is biased in a common cathode configuration (Fig. 2.12(a)). Inductive peaking is used to extend the driver bandwidth. The energy efficiency is 0.65 pJ/b, and the supply voltage is 3 V. No equalization is provided by this design, and the modulation current is about 1.5 mA.

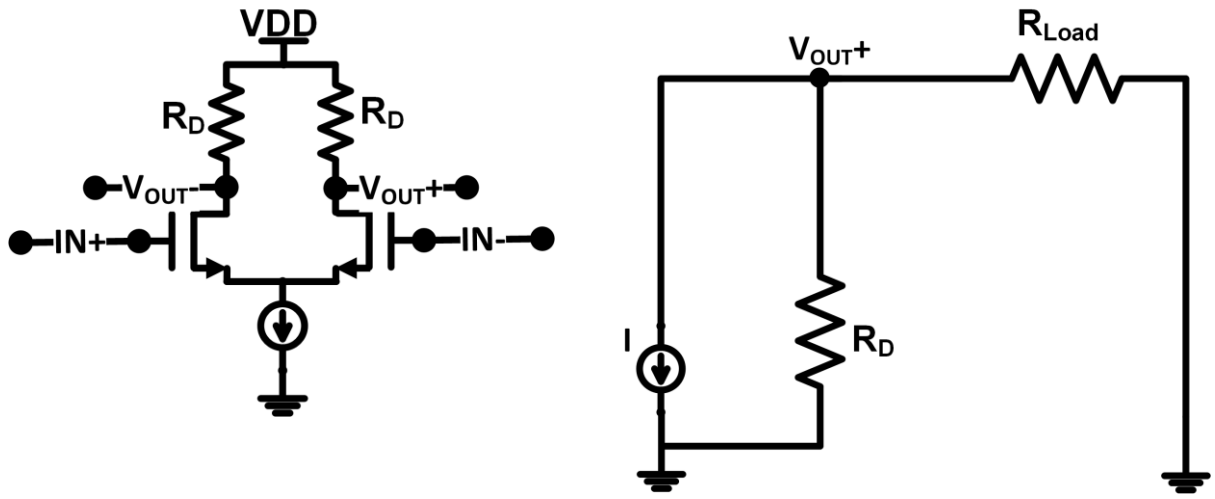


(a) (b)

Fig. 2.14 Two VML VCSEL drivers: (a) proposed driver in [3], (b) proposed driver in [4].

2.3.2 Current mode VCSEL drivers

CML VCSEL drivers are based on the differential pair amplifier schemes as shown in Fig. 2.15(a). This CML scheme can be replaced by the Norton equivalent parallel termination circuit as shown in Fig. 2.15(b). To achieve a specific output swing at the output node (V_{OUT}), the required current (I) is equal to $\frac{2\,V_{OUT}}{R_{Load}}$ which is two times the value of the current in the VML scheme.



(a) (b)

Fig. 2.15 Current mode logic (CML): (a) differential pair scheme, and (b) the equivalent schematic for half of the differential based scheme (small signal model).

In another work [1], a 50 Gb/s asymmetric 3-tap FFE VCSEL driver is described (Fig. 2.16(a)). The proposed design is implemented in a 130 nm SiGe BiCMOS technology with a supply voltage of 2.5 V. The VCSEL diode is biased in a common anode configuration (Fig. 2.12(b)) with an external supply voltage of 3.3 V. Asymmetric FFE is used to compensate the VCSEL nonlinear response towards binary "1" and binary "0". The power consumption is 150 mW (higher than the VML schemes) equivalent to energy efficiency of 3 pJ/b. The output impedance of the driver is 50 Ω. The equalization ratio and the output impedance are not tunable.

In a previous study [2], a 25 Gb/s VCSEL driver fabricated using IBM8HP BiCMOS technology is presented (Fig. 2.16(b)). The driver provides a sharper falling edge compared to the rising edge to compensate for the VCSEL nonlinear response. The presented driver provides tunable modulation current and tunable bias current. The VCSEL diode is biased in a common cathode configuration using a supply voltage of 3.3 V. It consumes 60 mW power, and its energy efficiency is 2.4 pJ/b.

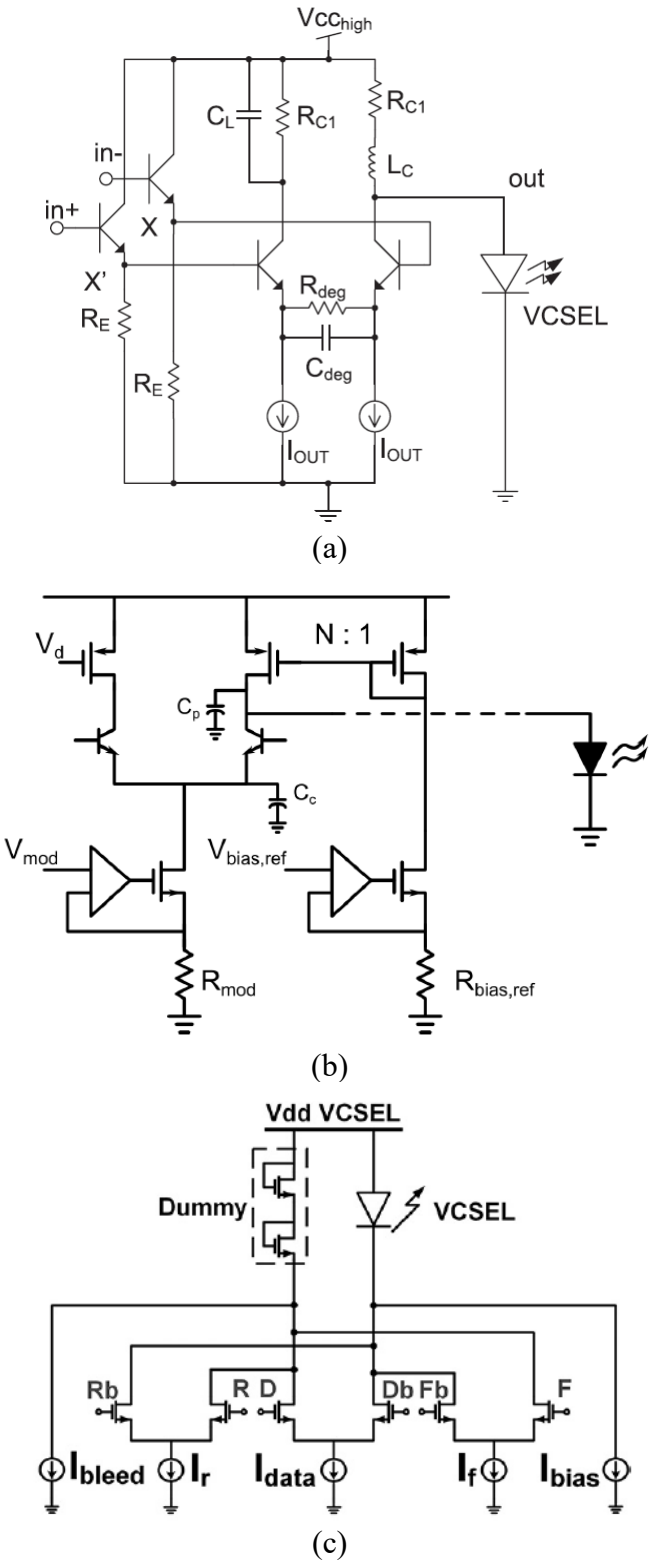


Fig. 2.16 CML schemes: (a) proposed scheme in [1], (b) proposed scheme in [2], and (c) proposed scheme in [12].

In another work [14], a 20 Gb/s CML VCSEL driver with asymmetric equalization is proposed (Fig. 2.16(c)). Edge detectors are used to provide asymmetric equalization. The output impedance of the driver is higher than 50 Ω. No tunability is provided for the equalization ratios nor the output impedance.

Based on the literature, in conventional VCSEL drivers, asymmetric equalization is used to compensate for VCSEL nonlinear behavior. The output impedance is below 100 Ω to reduce the ringing in the output optical power. However, neither the output impedance nor the modulation current is tunable. Also, the asymmetric equalization cannot be converted to a symmetric one.

2.4 Electrical links

The electrical link is an interconnect (i.e., cable or metal trace) which is used to carry a data signal between two points. It causes a delay (non-negligible) in data (see Fig. 2.17). This delay depends on the inductance and capacitance of the electrical link. There are three types of electrical links (transmission line), which are 1) lossless, 2) low loss, or 3) lossy. The lossless electrical link is only a theoretical notion, while the low loss and lossy electrical links are widely used in data transmission simulation. Electrical links are provided in various shapes such as coaxial cables, and parallel plates.

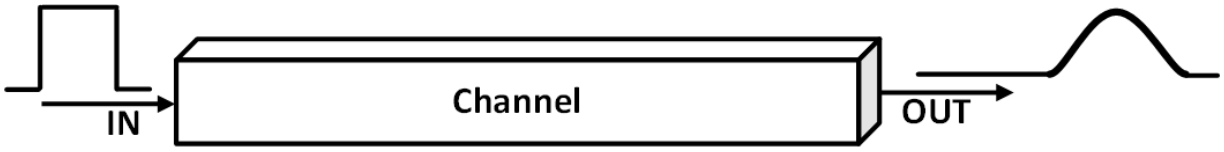


Fig. 2.17 The effect of a lossy channel on a pulse.

One of the widely used channels is the PCB electrical link (refer to Fig. 1.1). This channel is a microstrip channel (see Fig. 2.18) which consists of a conductor with width (*W*), fabricated on a dielectric substrate with a thickness (*H*). This substrate is on a ground plane as will be discussed in Chapter 3.

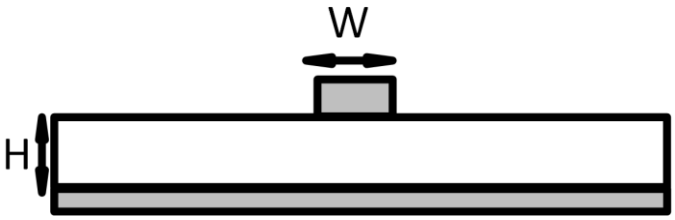


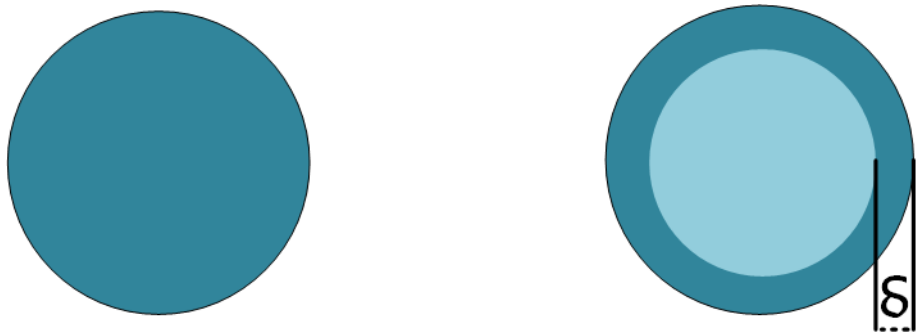
Fig. 2.18 The cross-section of the microstrip channel which consists of a conductor over a ground plane.

Ideally, the alternating current (AC) is equally distributed through the electrical link (Fig. 2.19(a)); however, lossy electrical links are affected by the skin effect. The skin effect is a phenomenon where the AC current is distributed within a conductor such that the largest current density is near the surface (skin) of the conductor. The current density decreases in the direction of the core of the conductor (Fig. 2.19(b)). The skin effect phenomenon increases with increasing signal frequency. The depth of the area where the density of the AC current is high and is called the skin depth (δ) and it can be calculated through the following equation.

$$\delta = \sqrt{\left(\frac{\rho}{\pi f \mu_r \mu_o}\right)} \qquad \text{Eq. 2.6 [17]}$$

where ρ is the resistivity (Ω*m), f is the frequency (Hz), μ_r is the relative permeability, and μ_o is the free space permeability ($4\pi*10^{-7}$ T.m/A).

Lossy electrical links are modeled as shown in Fig. 2.20. It consists of: (a) series resistance (R) which represents the conductor losses due to DC resistance of the skin effect, and (b) series inductor (L) which characterizes a reactive aspect of the skin effect and the self-inductance of the transmission line. In addition, the dielectric losses are modeled through a shunt capacitance (C) and a shunt admittance (G) [10].



(a) (b)

Fig. 2.19 The current distribution in a conductor: a) uniform distribution occurring at dc, and b) skin effect where the current density is reduced with the direction of the inductor core.

The characteristic impedance (Z_o) of the transmission line at high frequency is calculated as follows [10]:

$$Z_o = \sqrt{\frac{L}{C}} \qquad \text{Eq. 2.7}$$

To reduce the signal reflections, the output impedance of the transmitter, the characteristic impedance of the electrical link, and the input impedance of the receiver should be matched. Furthermore, to compensate for the losses of the electrical links, equalization is added to the circuit in the transmitter side and/or the receiver side. Table 2.1 shows the amount of losses due to the electrical channels presented in some previously published studies.

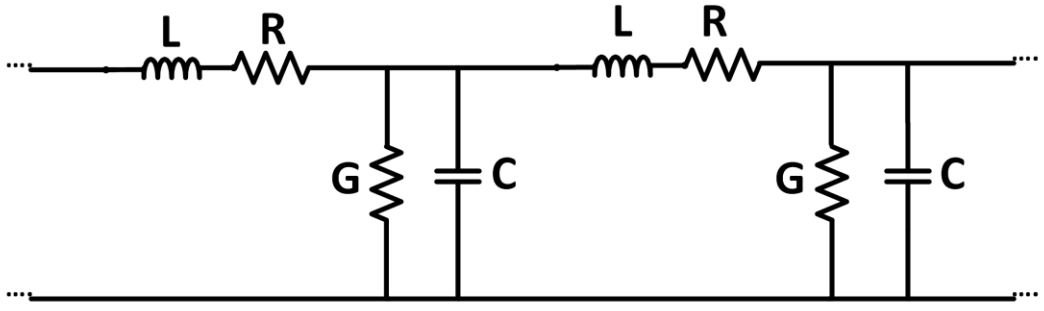


Fig. 2.20 Lossy transmission line model.

Table 2.1 The amount of the losses in different channels presented in the open literature.

Reference	Channel loss at Nyquist (dB)	Nyquist rate (GHz)	Channel length (mm)
[13]	12	10	-
[8]	13.6	10	3.5
[9]	16	-	3

2.5 Electrical link drivers

The target in the electrical link drivers is to achieve high data rates, consuming low power and compensating for the frequency-dependent channel losses. This compensation could be provided through the transmitter side FFE with symmetric equalization [10]. FFE in the electrical link drivers use more than one tap to mitigate the channel losses and reduce jitter [7, 13]. To recover the data with a low bit error rate (BER) (i.e., $< 10^{-12}$) at the receiver side, a large signal swing (e.g., 700 mV [8]) for the transmitted signal is desirable [7]. The bit error rate represents the number of the errored bits divided by the total number of bits.

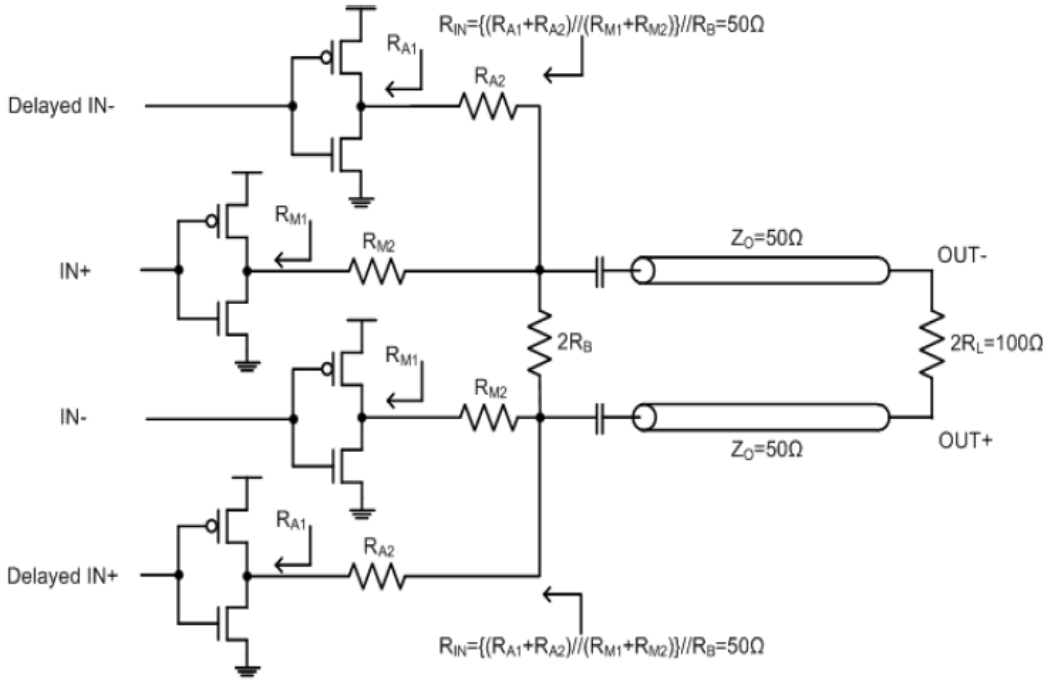
2.5.1 Voltage mode electrical link drivers

To reduce the power consumption of the transmitter, most electrical link drivers are based on VML (Fig. 2.13(a)) as discussed earlier in sections 2.3.1 and 2.3.2. In VML schemes, impedance matching is complex as it depends on the on-state resistance of the transistor in the inverter scheme. This on-state resistance is more sensitive to process variations compared to normal resistances. Matching the output impedance of the driver with the electrical link impedance is an essential requirement in any electrical link driver to reduce the reflections of the signal through the electrical link. Impedance mismatching leads to high reflections which cause a reduction in the signal power and increase BER. To facilitate impedance matching, extra circuits are added to the main driver as in [6] (see Fig. 2.21(a)), increasing the complexity of the design. The original circuit without equalization contains only the resistance R_B. After the addition of the equalizer tap, two resistances are added to the design (R_{M2}, and R_{A2}) to maintain a matched output impedance. The output

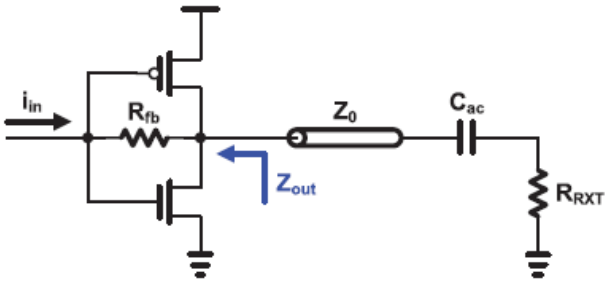
impedance before equalization depends on R_{A1} and R_B (i.e., R_{A1} // R_B). However, after equalization, the output impedance depends on R_{A1}, R_{A2}, R_{M1}, R_{M2}, and R_B.

In a previous work published in [13], a 20 Gb/s electrical link driver is proposed and fabricated in 65nm CMOS technology. The driver provides a differential output swing of 250 mV. Feedback resistance is added to maintain a matched output impedance and achieve a constant G_m value ($G_m = I_{OUT}/V_{IN}$) of the driver (see Fig. 2.21(b)). The driver energy efficiency is 0.4 pJ/b, while the total energy efficiency of the circuit is 1.52 pJ/b (i.e., including the pre-driver). A 2-tap FFE is used to compensate for a channel loss of 12 dB at Nyquist rate.

In another work [15], N-over-N driver (see Fig. 2.22) is used to drive a 60 Ω channel. This driver consists of cascoded NMOS transistors, and therefore this design is called "N-over-N". No PMOS transistors are included in the design. The presented design is a 5 Gb/s driver fabricated in 90nm CMOS technology with a 2-tap FFE equalizer to compensate for a channel loss of 6 dB. The output impedance calibration (OICC) circuit is used to maintain a matched output impedance. The OICC consists of comparators, memory elements, and 2-to-1 MUXs. The proposed driver can work in two modes of operation which are a) output impedance calibration or b) data transmission mode (based on the state of the CAL_EN signal).



(a)



(b)

Fig. 2.21 VML electrical link driver, (a) [6], and (b) [13].

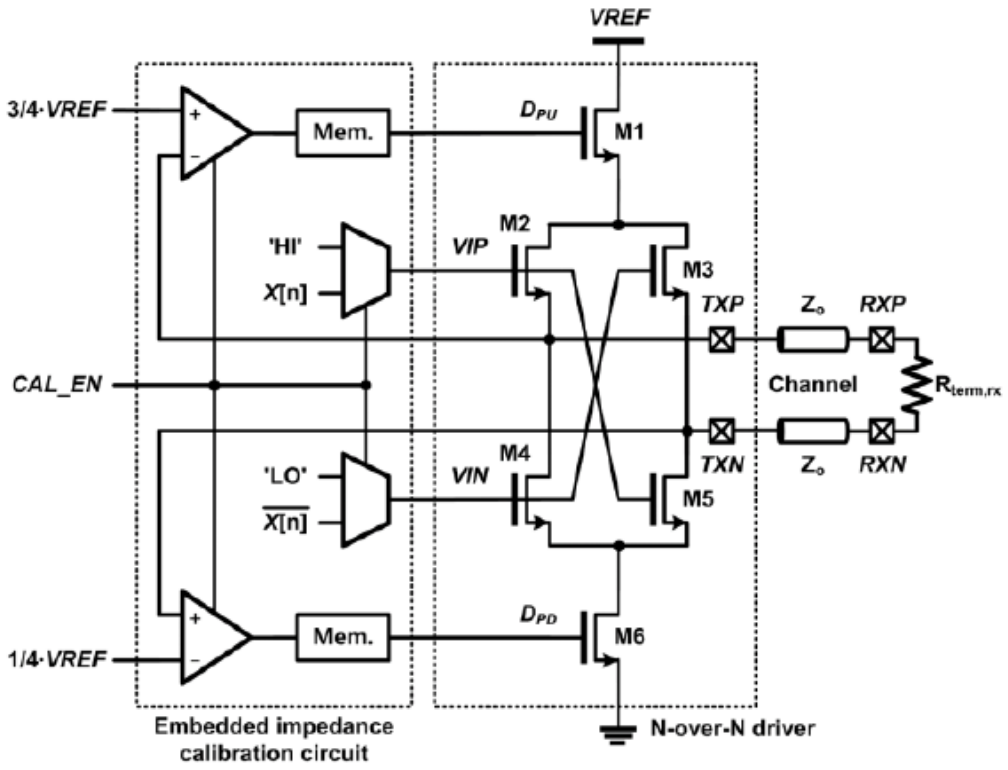


Fig. 2.22 N-over-N driver [15].

Voltage mode source-series-terminated scheme (SST) is an approach facilitating the impedance matching issues in the electrical link drivers. As shown in Fig. 2.23, SST consists of a pull-up PMOS transistor and a pull-down NMOS transistor connected via two series resistors [7]. These resistors are responsible for determining the output impedance of the circuit as they are relatively large compared to the on-state resistance of the NMOS and the PMOS (i.e., large transistors sizes as R_{ON} is proportional to $\frac{L}{W}$). In addition, reducing the value of the on-state resistancewhich is more sensitive to process variations compared to the normal resistance [9] of the NMOS and the PMOS transistors makes the output impedance more stable with the presence of PVT as previously discussed in the literature [9].

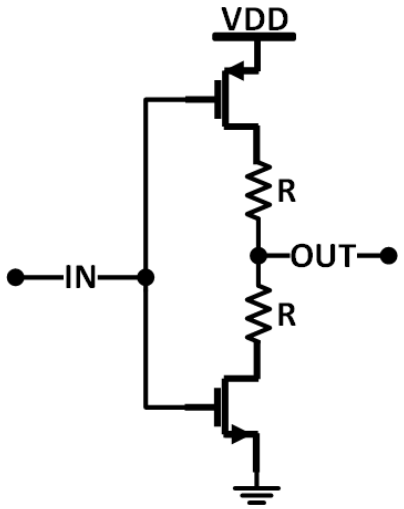


Fig. 2.23 VML SST scheme.

SST can be divided into slices connected in parallel. The slice is a SST circuit that offers a higher output impedance than required. Each slice can be enabled or disabled using logic [3] (see Fig. 2.24). The total output impedance is the output impedance of one slice divided by the number of the parallel enabled slices (*N*) [7]. Thus, the output impedance of the scheme is tunable as the output impedance changes with the number of enabled slices.

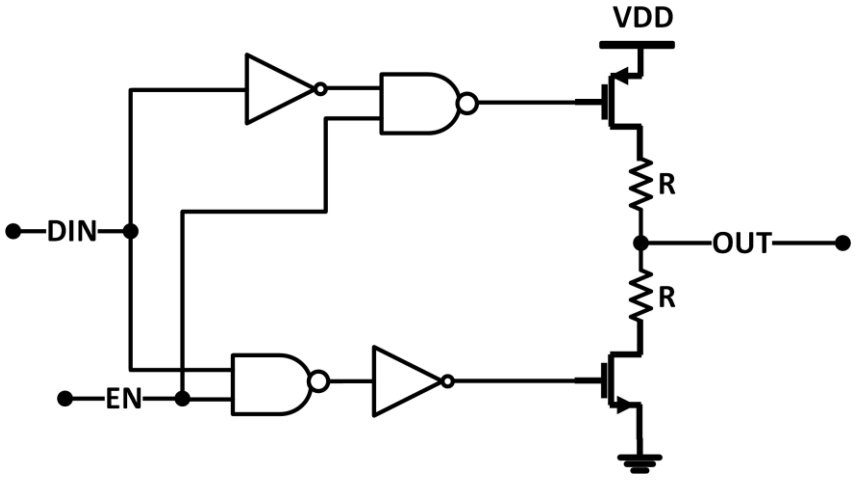


Fig. 2.24 An example of enable logic used to enable or disable the SST slices.

In a previous study [7], SST is used to drive an electrical link. This work offers a 1.28 Gb/s driver fabricated in 65nm CMOS technology. As the finite impulse response (FIR) equalization causes attenuation in the signal, the equalization strategy used in the presented driver is a combination of CML and VML-SST schemes (see Fig. 2.25). In addition, VM-SST allows the FIR equalization to use smaller tap coefficients (i.e., equalization ratios) compared to the case without pre-emphasis. This equalization strategy is used to compensate for a channel loss of 16 dB. This electrical link driver consumes a total power of 6.8 mW when using the hybrid equalization strategy. It is found that, when using a pure current mode equalization, the total power consumption is 16.1 mW.

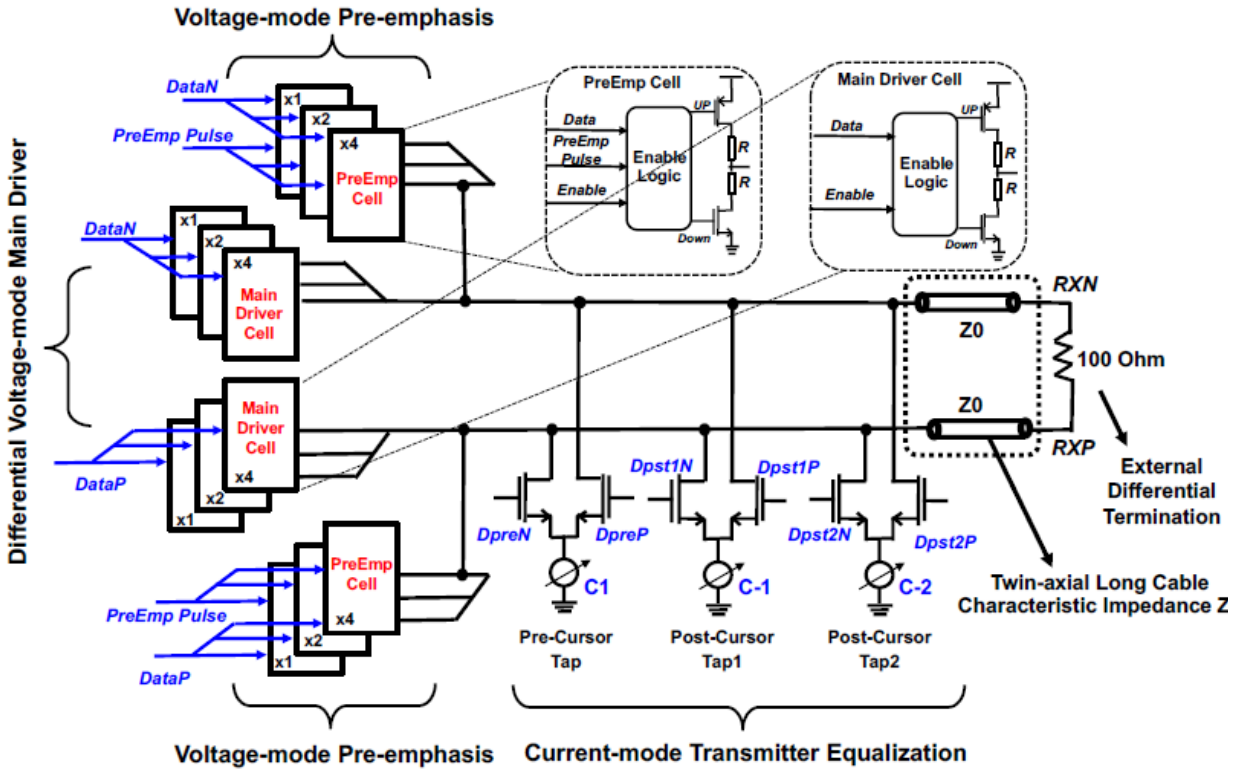


Fig. 2.25 Electrical link driver based on SST scheme and a combination of SST and CML for the equalizer taps taken from [7].

2.5.2 Current mode electrical link drivers

In CML electrical link drivers, the common source scheme is used as shown in Fig. 2.15(a). In this scheme, the output impedance depends on the drain resistor. Therefore, matching the output

impedance of the driver with the electrical link impedance is straightforward. The power dissipation in these types of drivers is relatively high compared to the VML drivers as discussed earlier in sections 2.3.1, and 2.3.2.

In a previous work [5], 8 Gb/s CML electrical link driver is presented. The main driver is an open drain differential pair (the drain is not connected to a drain resistor as shown in Fig. 2.26). No matching is required when designing such driver as the fraction of the current to the load is one. This fraction of the current depends on the output impedance and the load impedance $\left(\frac{R_{out}}{R_{out}+R_{load}}\right)$. Through this technique, the driver can inject all its current into the channel. This technique is used when having short lines (e.g., 5mm) or perfect receiver matching as receiver mismatching leads to signal' reflections. VML equalizer is used with an extra current path to tune the equalizer output swing. The energy efficiency for this driver is about 1 pJ/bit, and it is fabricated using IBM 130nm technology.

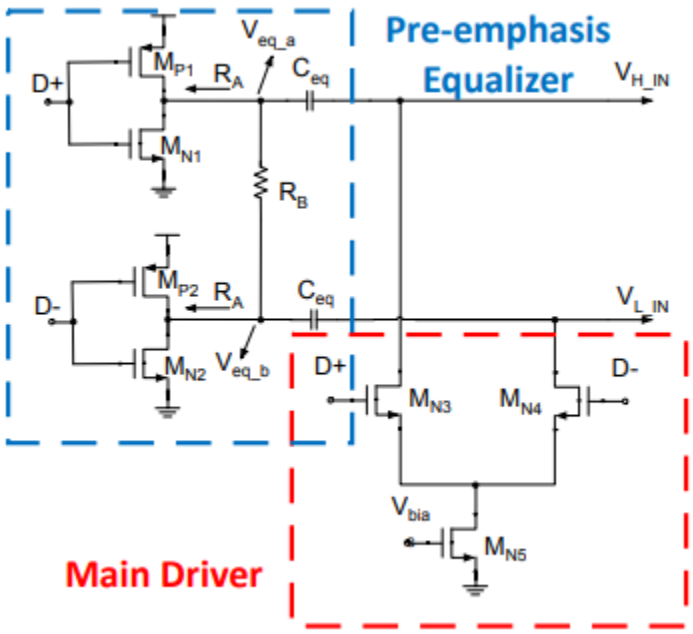


Fig. 2.26 Proposed driver in [5].

Based on the literature, in the conventional electrical link drivers, symmetric equalization is used to compensate for the frequency dependent loss. In addition, the output impedance is matched to

the electrical link impedance (50 Ω) to reduce the reflections in the signal power. The output impedance is not tunable, and no edge detectors are provided in the systems. Also, the symmetric equalization cannot be converted to asymmetric one.

2.6 Summary

Based on the discussion presented in this chapter, the research gap is concluded as follows:

- In the conventional VCSEL drivers:
    - 50 Ω impedance matching and output impedance tunability has not been achieved.
    - Asymmetric equalization cannot be converted to a symmetric one.
    - The DC current circuit that helps in forward biasing the VCSEL diode cannot be disabled.
    - The output swing is not tunable.
- In the conventional electrical link drivers:
    - Edge detectors are not used, and therefore applying asymmetric equalization to the data was not yet achieved.
    - High output swing is achieved, and it is not tunable.

Based on the research gap:

- Conventional VCSEL drivers cannot be used to drive electrical links.
- Conventional electrical link drivers cannot be used to driver VCSEL diode.

Accordingly, a modified driver is needed to drive a) VCSEL diode through an electrical link, b) Electrical link or c) VCSEL diode directly. This will be the subject of Chapter 4. The next chapter presents the models used to achieve a multi-operation mode driver.

Chapter 3 The models of the electrical link and the VCSEL diode

3.1 Introduction

This chapter introduces the electrical channel and VCSEL diode models which are used in simulating the proposed design. The electrical channel is a microstrip channel that models the area on the PCB between the proposed driver and the VCSEL diode. The electrical microstrip channel introduces a loss of 14.3 dB. Considering the ESD capacitance and the wire bonding parasitics, the total losses increase to be 16 dB. The VCSEL diode model used in the current work is a dynamic model and similar to the model mentioned in a previous study [11]. This dynamic model consists of electrical model and optical model. It considers the VCSEL nonlinear behavior towards binary "1" and binary "0" when biasing the VCSEL diode at a low bias current.

3.2 The electrical channel model and its issues

The electrical channel is used between the proposed driver and either the receiver side or the VCSEL diode (based on the mode of operation). This electrical channel is modeled using a microstrip link. The characteristic impedance (Z_o) of the electrical channel is designed based on the following equations [22]:

When $\frac{W}{H} \geq 1$

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 12\left(\frac{H}{W}\right)\right)^{-0.5} \quad \text{Eq. 3.1}$$

$$Z_o = \frac{120\pi}{\sqrt{\varepsilon_e} * \left(\frac{W}{H} + 1.393 + \frac{2}{3} ln\left(\frac{W}{H} + 1.444\right)\right)} \quad \text{Eq. 3.2}$$

When $\frac{W}{H} < 1$

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\left(1 + 12\left(\frac{H}{W}\right)\right)^{-0.5} + 0.04\left(1 - \frac{W}{H}\right)^2\right] \quad \text{Eq. 3.3}$$

$$Z_o = \frac{60}{\sqrt{\varepsilon_e}} * \ln 8\frac{H}{W} + 0.25\frac{W}{H} \quad \text{Eq. 3.4}$$

Where ε_e is the effective dielectric constant, H is the thickness of the dielectric substrate, W is the width of the conductor, ε_r is the conductor permittivity, and Z_o is the characteristic impedance.

A microstrip channel is used to model the area on PCB between the proposed driver and the VCSEL diode. This microstrip electrical channel consists of a conductor which has width (W), permittivity (ε_r = 3.66 [12]), and dissipation factor ($\tan\delta$ = 0.0037 [12]). This conductor is fabricated on a dielectric substrate of a thickness (H) on a ground plane (Fig. 3.1). The dielectric helps to concentrate the field lines in the region between the conductor and the ground plane. The field lines propagate in two different mediums: a) the air above the line, and b) the dielectric below the line. In the PCB, the dielectric substrate has a thickness (h) of 0.5 mm. From Eq. 3.1 and Eq. 3.2, to obtain a 50 Ω characteristic impedance for the electrical link, the width (W) of the conductor should be about 0.998 mm. In addition, based on Eq. 3.3 and Eq. 3.4, to obtain 85 Ω characteristic impedance for the electrical link, the width (W) of the conductor should be about 0.41 mm.

The model for the 50 Ω microstrip channel introduces a loss of 14.3 dB at the Nyquist rate of 10 GHz as shown in Fig. 3.2. The length of the link is chosen to be 5 cm to obtain a loss that matches the same range of losses presented in previously published studies [8,13]. In practice, the output of the proposed design is connected to the ESD diode. In addition, there are bond wires between the proposed driver and the electrical channel, and between the electrical channel and the VCSEL diode. These bond wires and ESD are modeled through an inductor of 1 nH and a capacitor of 150 fF, introducing more losses. The total loss of the channel is approximately 16 dB when parasitic losses are considered (Fig. 3.2). The length of the 85 Ω microstrip channel is 7 cm to

obtain the same losses of the 5 cm microstrip channel (16 dB) at the Nyquist rate. Table 3.1 summarizes the design parameters for the modeled microstrip lines.

Table 3.1 The microstrip link design parameters.

Parameter	50 Ω microstrip line	85 Ω microstrip line
ε_r	3.66	3.66
Dissipation factor at 10 GHz	3.7 mm	3.7 mm
W	998 μm	410 μm
H	500 μm	500 μm
Z_o	53.2 Ω	84.4 Ω
ε_e	2.83	2.67
Channel length	5 cm	7 cm
Total loss	16 dB	16 dB

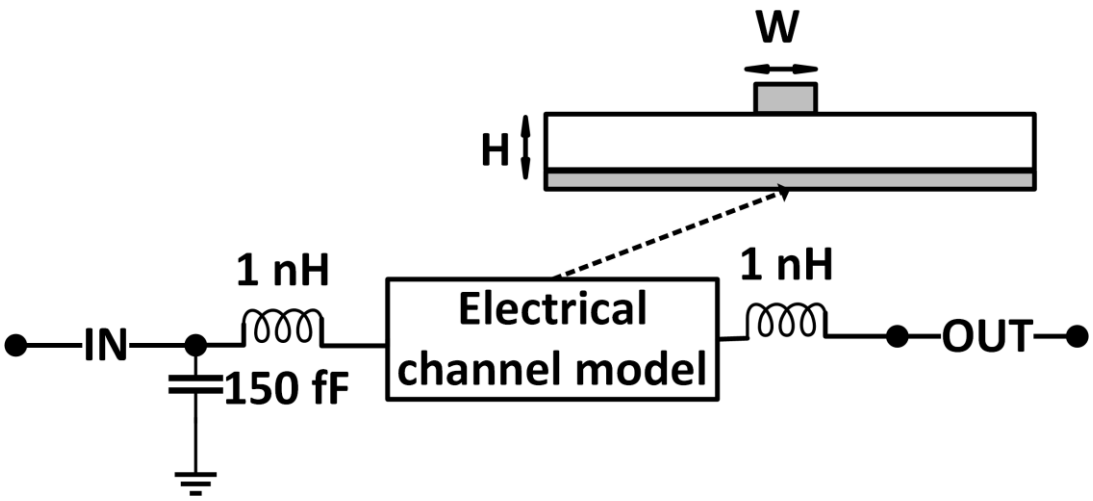


Fig. 3.1 The electrical channel model connecting to the ESD and wire bonding parasitics.

The electrical channels introduce some issues that should be handled while designing the transmitter. The first issue is the frequency dependent losses provided from the channel. Such losses should be compensated to mitigate ISI. ISI reduces the quality of the transmitted signals and causes a high BER. This issue can be handled by applying transmitter side equalization. The second issue is impedance matching. Both output impedance of the driver and the electrical link impedance

should be matched. When impedances are not matched, the reflections of the signal through the electrical link will be high, and that reduces the signal power and increases the BER. This issue can be handled by maintaining the output impedance of the proposed design to match the electrical channel impedance. In addition, providing tunability for the output impedance of the driver is a solution to guarantee the stability of the output impedance in the presence of the process and temperature variations (PVT).

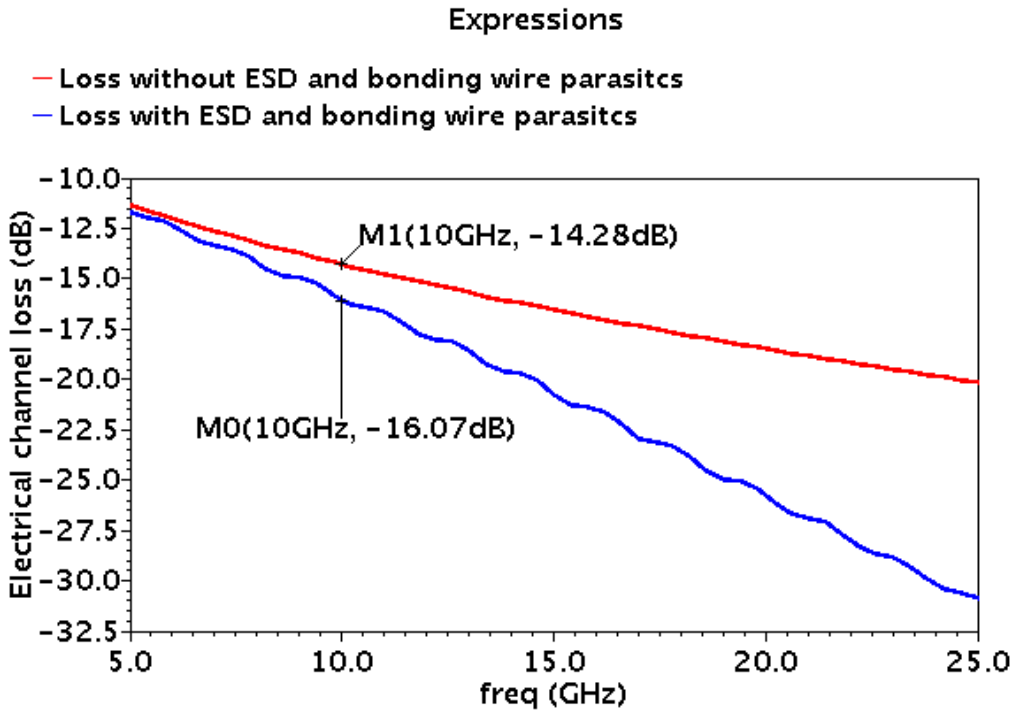


Fig. 3.2 The electrical channel loss at a range of frequencies with and without the ESD and bonding wire parasitics.

3.3 The VCSEL diode model

Vertical cavity surface emitting laser (VCSEL) is used in most of the short-reach (< 100 m) optical links in data centers. VCSEL is used in data centers, offering high data rates with relatively low cost. The VCSEL model mentioned in [11] is used in simulating the proposed design. This model is a dynamic model which consists of electrical and optical models as shown in Fig. 3.3. The electrical model is implemented via resistances and capacitors. The optical part is modeled via rate

equations mentioned in [11, 14] and implemented through a Verilog-A code. According to Eq. 3.3, and Eq. 3.4, with increasing I_{VCSEL}, the relaxation frequency (fr) is improved; however, the damping factor is increased (γv) [11, 14]. Therefore, improving the bandwidth of the VCSEL cannot be achieved by increasing I_{VCSEL} indefinitely as the bandwidth is limited by the damping factor [11].

$$f_r = D\sqrt{I_{VCSEL} - I_{th}} \qquad \text{Eq. 3.5 [11]}$$

$$\gamma_v = K * fr^2 + \gamma o \qquad \text{Eq. 3.6 [11]}$$

where *D*, *K*, and γo are the *D* factor, *K* factor and damping factor offset, respectively.

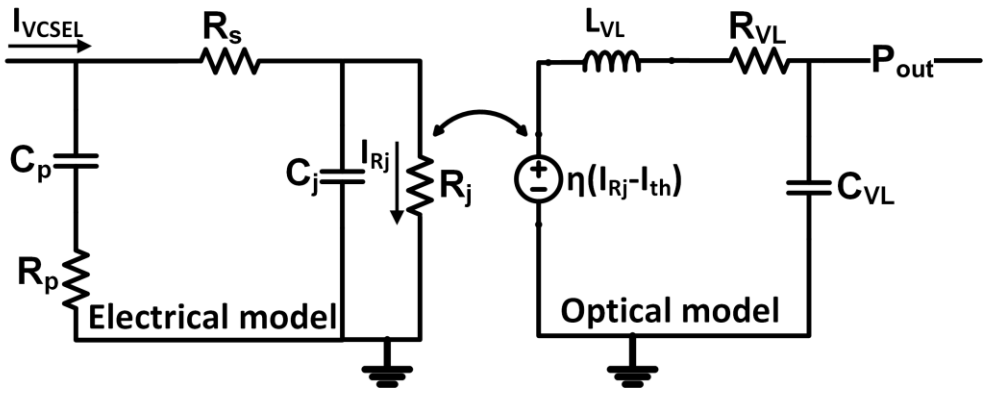


Fig. 3.3 The VCSEL model used in simulating the proposed design. (η is the slope efficiency)

The bandwidth is signal-dependent (not a fixed value) and varies with I_{VCSEL}. It should be stated that I_{VCSEL} changes from I_0 which is I_{bias} (i.e., transmit a binary "0") to I_1 (i.e., transmit a binary "1"). This change causes the nonlinear behavior of the VCSEL which is modeled through the optical part in previously published works [11, 14]. This nonlinear behavior is a different response towards binary "1" and binary "0" at low bias current as shown in Fig. 3.4. In Fig. 3.4, the pulse response of the isolated binary "1" and the flipped pulse response of the isolated binary "0" are plotted. The pulse response of the isolated binary "0" is flipped to compare between the two responses and highlight the nonlinear behavior.

The values of the VCSEL model parameters are mentioned in [11] (see Table 3.2). The VCSEL diode should be forward biased with a current higher than its threshold current (i.e., 0.6 mA). This forward biasing can be obtained through a DC current source connected to the VCSEL driver.

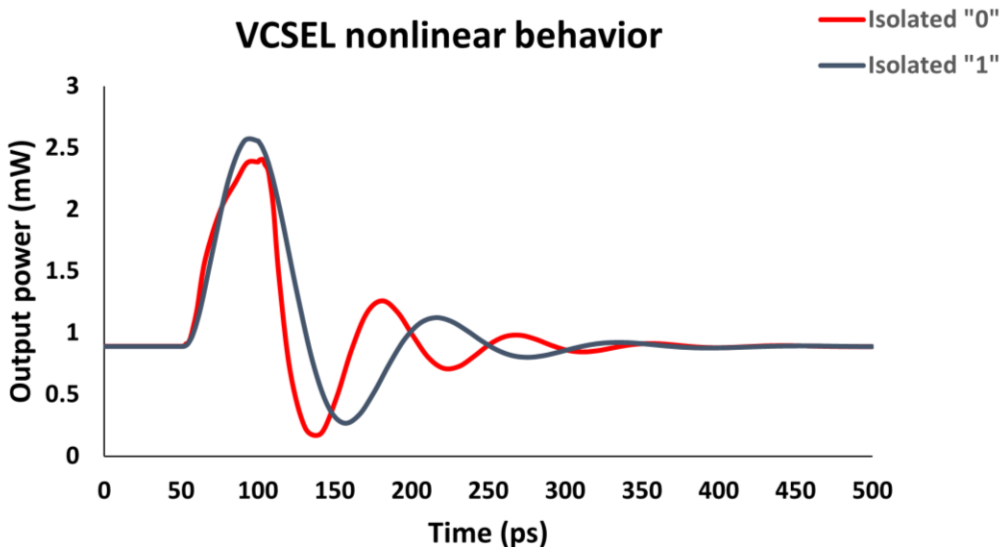


Fig. 3.4 The different responses of the VCSEL diode towards "1" and "0".

Table 3.2 VCSEL model parameters.

Parameter	Value	Parameter description
R_j	50-40 Ω	Junction resistance
C_j	270 fF	Junction capacitance
R_s	35 Ω	distributed Bragg reflector (DBR) mirror resistance
R_p	1 Ω	Pad resistance
C_p	10 fF	Pad capacitance
Ƞ	0.78 W/A	slope efficiency
I_{th}	0.6 mA	Threshold current
C_v	100 fF	RLC second-order circuit with signal-dependent oscillation frequency and damping factor, considering the VCSEL nonlinear behavior)
Lv	$\frac{1}{4\pi^2 C_v f_r^2}$	
Rv	$\frac{\gamma_v}{4\pi^2 C_v f_r^2}$	

Chapter 4 Design of the proposed triple mode driver

4.1 Introduction

This chapter introduces the design of a single-ended source-series-terminated voltage-mode driver in a 65 nm technology. The transmitted data is a non-return to zero (NRZ) format. Single-ended signaling is used to minimize the number of required signal traces and conserve I/O pins. A disadvantage of the single-ended signaling is that the signal is affected by common mode noise. To solve this problem, the proposed design exhibits a high output swing to provide sufficient noise margin when driving the electrical link. The driver operates in three driving modes. The first mode uses symmetric pre-emphasis feedforward equalization to drive a short electrical link. The modeled channel used in simulation introduces a total loss of 16 dB at 10 GHz including ESD and wire bonding losses. The second mode drives a VCSEL diode through the same electrical link exploiting asymmetric equalization. The third mode uses asymmetric equalization to drive a VCSEL diode wire-bonded to the driver. These three modes are shown in Fig. 4.1. The output current swing of the proposed design can be changed without affecting the output impedance of the circuit. Therefore, in the VCSEL driver mode of operation (mode II), the proposed design can work across a range of output current (i.e., modulation current). While in the electrical link driver mode (mode I), the design can work at high output swing, overcoming the channel's ISI. Through simulation, this proposed driver operates up to 20 Gb/s.

To design a driver that can drive either an electrical link or a VCSEL diode, there are some specifications and requirements that should be achieved. These requirements are listed as follows:

- Output impedance to match the 50 Ω electrical link impedance, reducing the signal reflections.
- Tunable output impedance between 50 Ω and 200 Ω to match the VCSEL impedance.
- Symmetric and asymmetric equalization based on the selected operation mode.

- Suitable modulation current when operating in the VCSEL driver mode (e.g., 1.5 mA to 4.5 mA).
- Implementation of a VCSEL bias current circuit that can be disabled when the proposed design operates in the electrical link driver mode (mode I).
- Tunable output current swing with constant output resistance.

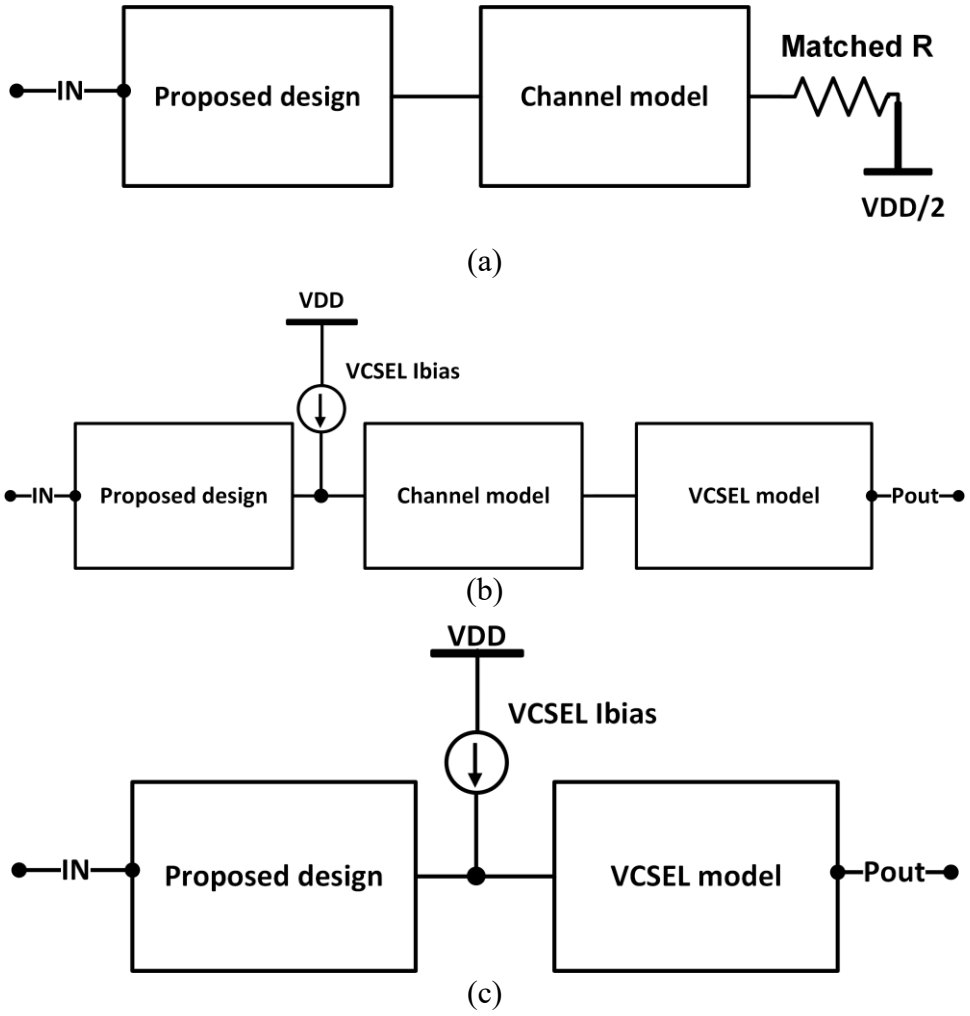


Fig. 4.1 The three modes of operations for the proposed design: (a) electrical link driver (mode I), (b) VCSEL driver through an electrical link (mode II), (c) VCSEL driver (mode III).

4.2 Preliminary design

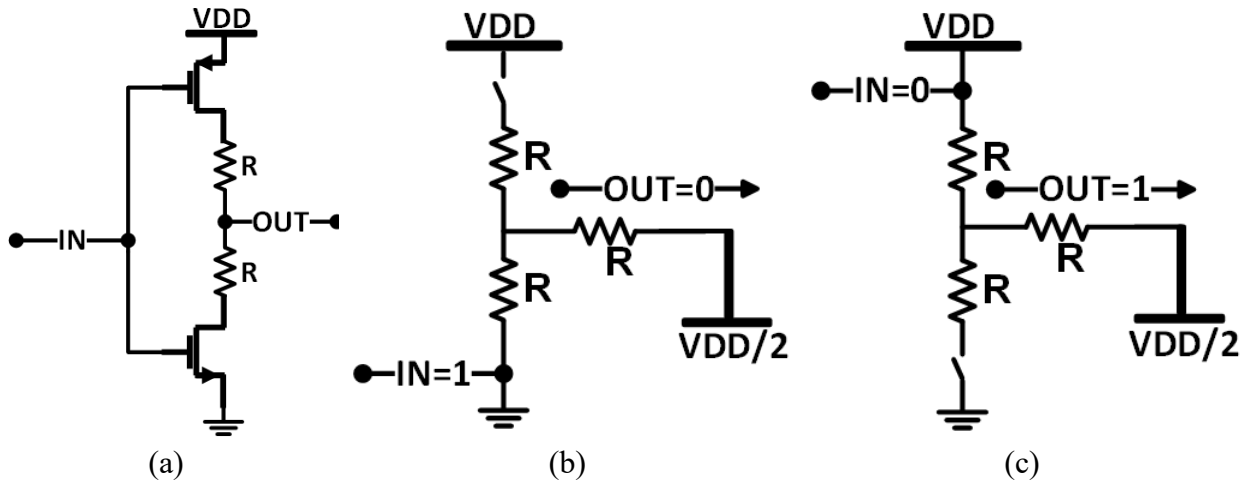
The current work started with a preliminary design which was presented in [19]. This preliminary design is a CMOS 1.2-V single-ended source-series-terminated voltage-mode electrical link driver in a 65 nm technology. It is a dual-mode driver that can drive either a VCSEL diode through an electrical link or an electrical link connected to another data processing unit. This driver has a simulated output impedance of 45 Ω to match the 50 Ω electrical link impedance. This deviation in the simulated output impedance is due to the output impedance of the current mirror which is used to forward bias the VCSEL diode. Although this deviation did not affect the output eye diagram as reported in [19], this issue is fixed in the final proposed design (triple mode driver) to match the 50 Ω electrical link impedance by reducing the number of the enabled SST slices when the current mirror is enabled. The preliminary proposed design provides toggling between symmetric and asymmetric equalization to compensate for the electrical channel loss and the VCSEL nonlinear behavior. The preliminary proposed design also reduces the power consumption and the overall system cost by eliminating the stand-alone laser diode driver. The simulations validate the preliminary proposed design up to 20 Gb/s for energy efficiency of 2 pJ/bit including the VCSEL biasing circuits.

As mentioned in the thesis objectives, VCSEL diode can be driven through a relatively low modulation current (i.e., 1.5 mA), and accordingly reducing the output swing can significantly enhance the preliminary design performance. Thus, a new proposed driver is designed (replacing the preliminary design) so that it is compatible with the tunability requirement of the driver output swing. A tunable output swing allows providing high and low output swings based on the application as will be presented and discussed in the upcoming sections.

4.3 The basic concept and system modeling

In this section, the basic concept of the scheme used in designing the proposed driver is presented and discussed. SST scheme, shown in Fig. 4.2(a), consists of a pull-down NMOS transistor (Fig. 4.2(b)) and pull-up PMOS transistor (Fig. 4.2(c)) connected via two series resistors. These resistors are responsible for determining the output impedance of the circuit as they are large compared to the on-state resistance of the NMOS and the PMOS transistors (i.e., large transistors sizes). In

addition, reducing the value of the on-state resistance of the NMOS and the PMOS transistors provides a stable output impedance in the presence of PVT as previously discussed in the literature [9].



(a) (b) (c)

Fig. 4.2 SST Scheme and its basic operation: (a) SST scheme, (b) pulled down SST scheme (the input of the slice is binary "1" and the output is binary "0"), and (c) pulled up SST scheme (the input of the slice is binary "0" and the output is binary "1").

To study the output current swing based on an ideal SST slice, the NMOS and PMOS transistors are replaced with ideal switches. These switches have on-state resistance of 0 Ω. The value of the series resistance (R) is 50 Ω to achieve a matched output impedance with the electrical link impedance. According to KVL, the pull-up (I_{PU}) and the pull-down (I_{PD}) currents can be calculated from the following equations, where V_{DD} is the supply voltage:

$$-I_{PD} * (R + R_{Load} + NMOS\ R_{On}) - \frac{V_{DD}}{2} = 0 \qquad \text{Eq. 4.1}$$

$$-V_{DD} + I_{PU} * (R + R_{Load} + PMOS\ R_{On}) + \frac{V_{DD}}{2} = 0 \qquad \text{Eq. 4.2}$$

When the on-state resistance for the PMOS equals to the on-state resistance of the NMOS, and the summation of the on-state resistance and "R" matches the load resistance, the peak-to-peak current can be calculated based on the following equation:

$$I_{P-P} = I_{PU} - I_{PD} = \frac{V_{DD}}{2R} \qquad \text{Eq. 4.3}$$

When the input of the SST slice is binary “1”, the NMOS transistor is ON (pull down slice). According to Eq. 4.1, the values of I_{PD} at supply voltages of 1.2 V, 1 V, 0.8 V, and 0.6 V are -6 mA, -5 mA, -4 mA, and -3 mA. When the input of the SST slice is binary “0”, the PMOS transistor is ON (pull up slice). According to Eq. 4.2, the values of I_{PU} at supply voltages of 1.2 V, 1 V, 0.8 V, and 0.6 V are 6 mA, 5 mA, 4 mA, and 3 mA. Knowing that R and R_{Load} are matched and equal to of 50 Ω. These values of I_{PD} and I_{PU} are validated by simulations as shown in Fig. 4.3.

The output current swing of the SST slice at different supply voltages is studied. According to Eq. 4.3, the output current swings ($I_{P\text{-}P}$) from the ideal scheme at supply voltages (V_{DD}) of 1.2 V, 1 V, 0.8 V and 0.6 V, and R of 50 Ω are 12 mA, 10 mA, 8 mA, and 6 mA, respectively. These values of the peak-to-peak current are validated by simulations as shown in Fig. 4.3.

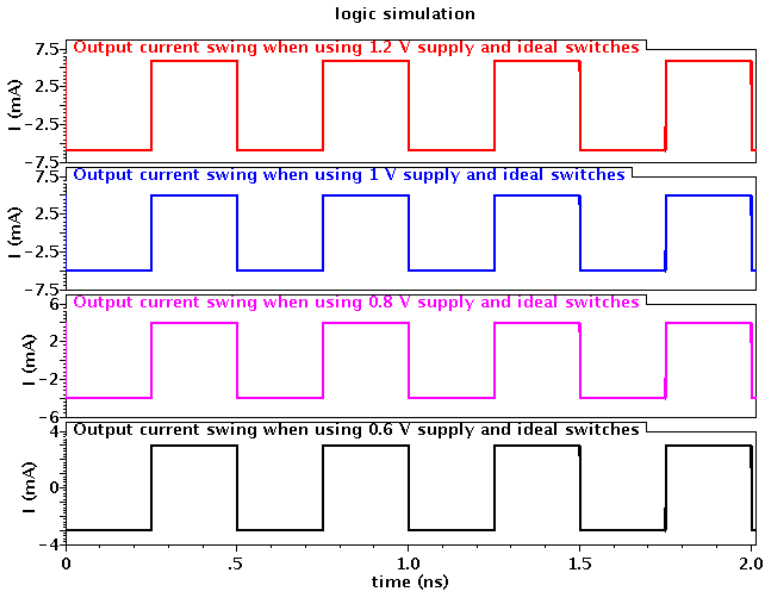


Fig. 4.3 Output current swing from 1 slice of SST scheme (50 Ω output impedance) with ideal switches at different supply voltages.

When changing the ideal switches with relatively very large transistors (i.e., achieving low on-state resistance but not 0 Ω), the output swings are reduced. This is because of the on-state resistance of both the NMOS and PMOS transistors, which is not 0 Ω as in the ideal switches. Table 4.1 shows the on-state resistance of both NMOS and PMOS transistors at different supply voltages. When using 1 V supply voltage (refer to Table 4.1), the values of the on-state resistances of the NMOS

and PMOS transistors are 4.23 Ω and 5.68 Ω, respectively. According to Eq. 4.1 and Eq. 4.2, the pull up and the pull-down currents (I_{PU}, I_{PD}) when using large transistors instead of ideal switches can be calculated as follows:

$$-I_{PD} * (50\ \Omega + 50\ \Omega + 4.23\ \Omega) - 0.5 = 0 \quad \text{Eq. 4.4}$$

$$-1 + I_{PU} * (50\ \Omega + 50\ \Omega + 5.68\ \Omega) + 0.5 = 0 \quad \text{Eq. 4.5}$$

Giving that, ($R = R_{Load} = 50\ \Omega, NMOS\ R_{On} = 4.23\ \Omega, PMOS\ R_{On} = 5.68\ \Omega, and\ V_{DD} = 1\ V$).

The results in this case show that I_{PD}= -4.79 mA and I_{PU}= 4.73 mA, which confirm the same values of the output current shown in Fig. 4.4. This reduction is due to the on-state resistance of the transistors. To avoid this reduction in the current (i.e., 5 mA to 4.73 mA), "R" in the SST scheme can be reduced so that the total output impedance equals to the load impedance. The new values of the resistor "R" are 45.77 Ω for the pull-down network, and 44.32 Ω for the pull up network. Accordingly, the summation of the on-state resistance and "R" provides an output impedance of 50 Ω for the SST scheme when using a supply voltage of 1 V. This approach provides an output current swing varied from 5 mA to -5 mA, similar to the approach applied on the ideal switches. In Fig. 4.4, there is an overshoot in the output current which is attributed to the large size ratio (length/width) of the transistors (250um/60nm), introducing parasitic capacitances (i.e., the gate to drain capacitances). These parasitic capacitances affect the waveform in the presence of fast transitions and increase the rising and falling times of the output waveforms. In addition, both parasitic capacitances and output resistance cause RC delay in the output waveform. The RC delay can be calculated as follows:

$$Delay = R * C_{out} = (R_{Load} + R) * (C_{DS}) \quad \text{Eq. 4.6}$$

According to Eq. 4.6, when the slice is pulled up, C_{DS} for the PMOS is 132 fF, and the delay is 13.2 ps. In case of pulling down, C_{DS} for the NMOS is 262 fF, and the delay is 26.2 ps.

It was found that the on-state resistance of the transistors affects the total output impedance at low supply voltages (i.e., 0.8 V, and 0.6 V) which accordingly affects the output swings as shown in Table 4.1. In addition, the on-state resistance of the PMOS changes significantly compared to the

on-state resistance of the NMOS as shown in Table 4.1 at low supply voltages (i.e., 0.8 V, and 0.6 V). This change leads to different values of the output impedance of the SST slice in case of pulling up or pulling down, which needs to be addressed in the current proposed design.

Table 4.1 On-state resistance of NMOS and PMOS at different supply voltages.

Supply voltage (V)	1.2	1	0.8	0.6
NMOS on-state resistance (Ω)	4.25	4.23	4.2	4.2
PMOS on-state resistance (Ω)	4.35	5.68	9.26	34.19
Output swing (I_{PU}, I_{PD}) (mA)	11.5 (5.75, -5.75)	9.5 (4.73, -4.79)	7.5 (3.66, -3.84)	5.1 (2.22, -2.87)

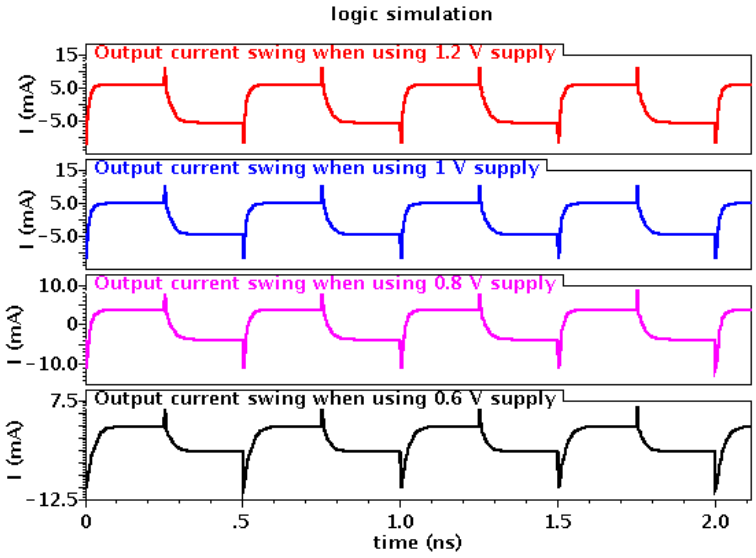


Fig. 4.4 The output current swing from 1 slice of SST scheme with large transistors at different supply voltages.

The change is attributed to the change in the input waveform voltage (from 0 to 1.2 V). It should be stated that this waveform is the output of the pre-driver (includes D-flip flops and logic gates) biased at a supply voltage of 1.2 V. Accordingly, V_{GS} of the NMOS is 1.2 V when the SST scheme is pulled down and V_{SG} of the PMOS is (V_{DD} - 1.2) when the SST scheme is pulled up, as shown

in Fig. 4.5. For example, if V_{DD} in Fig. 4.5 is 0.7 V, V_{GS} of the NMOS is 1.2 V when the circuit is pulled down (i.e., V_G is the input node of 1.2 V applied and V_S is connected to the ground). However, V_{SG} of the PMOS is limited to 0.5 V (i.e., V_S is connected to V_{DD} which is 0.7 V in the example, and V_G is still 1.2 V which is the input node), this leads to different on-state resistances for both NMOS and PMOS transistors. This issue leads to different output impedance when the circuit is pulled up and pulled down.

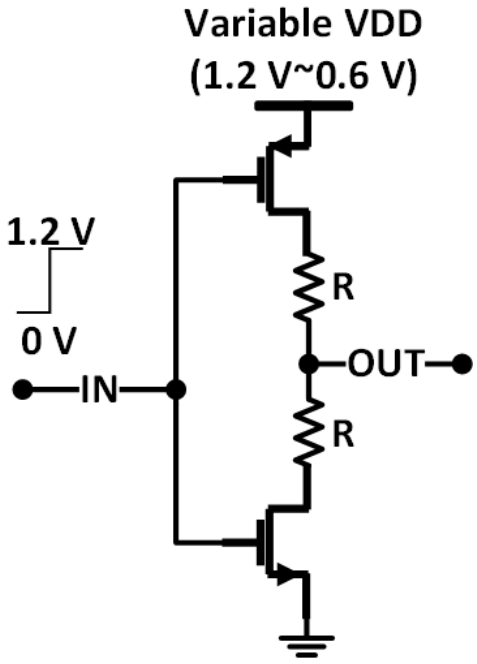


Fig. 4.5 SST scheme when using variable supply voltages, and the input is always 1.2 V for binary “1” and 0 V for binary “0”.

To forward bias the VCSEL diode, the modulated current should be in the positive direction with a value larger than the threshold current (0.6 mA [11,14]). To fulfill this requirement, the currents in Fig. 4.4 need to be shifted up using DC bias current. This bias current can be implemented using a PMOS current mirror, which consists of two branches (i.e., the reference branch and the mirroring branch) with setting a certain mirroring ratio for the mirroring branch (see Fig. 4.6).

The current mirror is connected to the output of the SST slice (i.e., the slice used to plot Fig. 4.4, which has an output impedance of 50 Ω). The output impedance of the overall circuit is reduced

due to the output impedance of the current mirror (i.e., parallel connection). To guarantee a 50 Ω output impedance of the slice, R in the SST scheme should be increased.

To design the current mirror, the reference transistor should be enabled (on) and in the saturation region. Accordingly, certain conditions on the gate-to-source and the drain-to-source voltages (i.e., $V_{SG} > V_{tp}$ and $V_{SD} > V_{DSAT}$) should be considered. To fulfill these conditions, the reference transistor is designed with a size of 5um/60nm. To forward bias the VCSEL diode, the current needed for this target requires the mirroring size ratio to be 20. Therefore, the size of the mirroring transistor is 100um/60nm. When using this transistor sizing, the output impedances of the current mirror at an output voltage of $V_{DD}/2$ are 186 Ω, 185 Ω, and 175 Ω when using supply voltages of 1.2 V, 1 V, and 0.8 V, respectively. Accordingly, R in the SST slice is required to be around 100 Ω instead of 50 Ω so that the output impedance is maintained to be 50 Ω.

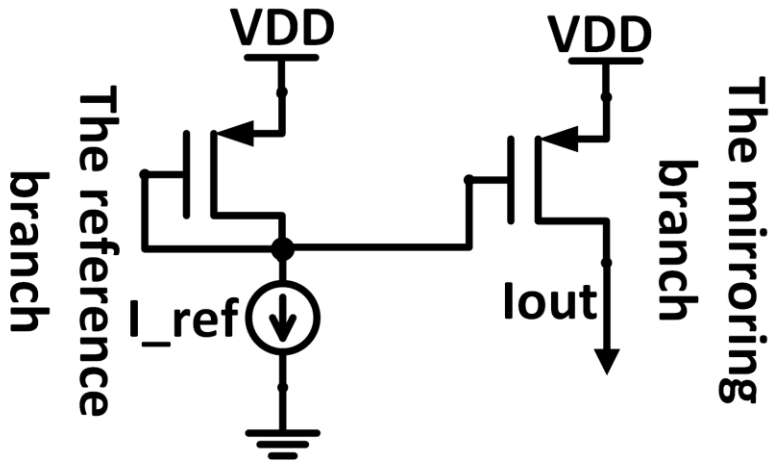
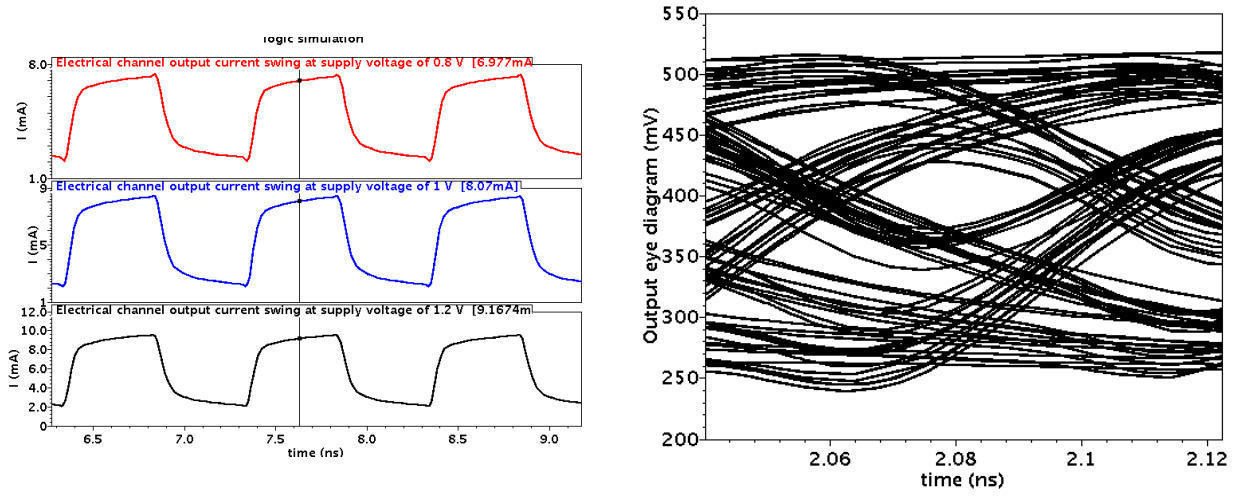


Fig. 4.6 CMOS basic current mirror.

As one of the functions of the proposed design is to drive a VCSEL diode through an electrical link, the modulation current requirements should be satisfied. The output current swing from the electrical link model is checked. As shown in Fig. 4.7(a), the output current swing from the electrical channel is 6.6 mA, 5.7 mA, and 4.5 mA when the supply voltages are 1.2 V, 1 V, and 0.8 V, respectively, meeting the desired requirements (i.e., the range of modulation current has a

minimum of 1.5 mA). It is observed in Fig. 4.7(a) that the current swing is reduced, and the output waveform includes ISI (i.e., no equalization is applied); This ISI is due to the frequency dependent losses of the electrical channel. This ISI is clear when plotting the output voltage eye diagram of the electrical link at a supply voltage of 0.8 V as shown in Fig. 4.7(b).



(a) (b)

Fig. 4.7 The 5 cm electrical link model connected to the SST slice and the DC bias current: a) output current swing at different supply voltages, and b) output eye diagram at a supply voltage of 0.8 V.

4.4 The proposed design

As previously discussed, the design drives either an electrical link or a VCSEL diode (directly or through the electrical link). Therefore, there are some design aspects (e.g., matched output impedance, symmetric and asymmetric equalization, etc.,) that should be considered within the proposed design.

The proposed system consists of several taps as shown in Fig. 4.8. Each tap includes a number of SST slices connected in parallel. Each SST slice has a relatively large value of R which is 1500 Ω. This value of "R" can solve the noticeable variation in the on-state resistance of the PMOS at low

supply voltage (till 0.9 V). This is because the on-state resistance of both transistors is negligible compared to R.

Each slice in the SST system contains a PMOS transistor with a size ratio of 3.8um/60nm, and a NMOS transistor with a size ratio of 1.8um/60nm. These sizes of the transistors are chosen to maintain the same value for the on-state resistances of both transistors. Therefore, the output impendence of the driver is the same when the slice is pulled up or pulled down. Using these selected sizes for the transistors in the proposed design, the on-state resistance of both transistors has an average value of 300 Ω which is relatively small compared to "R" which is 1500 Ω. The output impedance of each slice is about 1800 Ω. Thus, to achieve a 50 Ω output impedance, 36 slices should be connected in parallel. Each slice has an "enable-signal" that is used to enable or disable the slice function based on the mode of operation and the required output impedance, which will be discussed in the upcoming sections. Also, additional slices are available in each mode to compensate for the increase in the output impedance in the presence of the process variations; however, they are disabled in the simulated design. Furthermore, these additional slices in both main and the equalizer taps allow working within the range of the output impedances mentioned earlier from 50 Ω to 200 Ω to match the VCSEL impedance.

The current section presents the required steps towards the entire design shown in Fig. 4.8. The proposed design in Fig. 4.8 consists of a voltage regulator to allow tunability in the output swing, a main tap, and equalizer taps.

These taps consist of SST slices, D-flip-flops (to be used in the equalization delay), an enable logic for each slice, edge detectors (used in the equalizer taps), and a current mirror (used as a DC current source to forward bias the VCSEL diode). Table 4.2 shows the illustration for each signal abbreviation in Fig. 4.8. In this section, the voltage regulator is firstly discussed, and then the equalization strategy is introduced. After that, the design of the three modes is discussed. Finally, the power breakdown for each mode is presented and discussed.

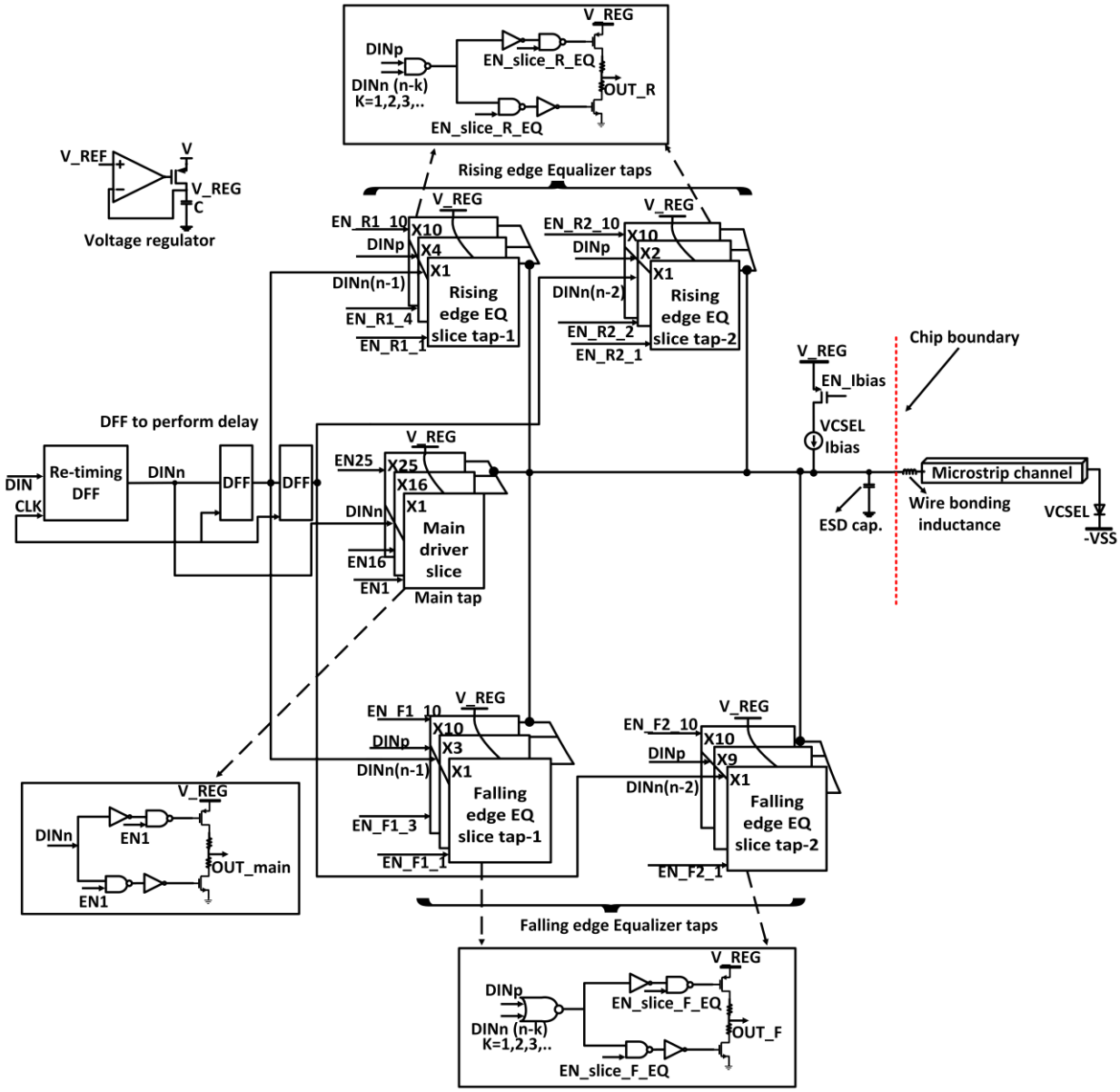


Fig. 4.8 The entire proposed system.

4.4.1 Voltage regulator

The proposed design is used to drive either an electrical link or a VCSEL diode. Thus, offering a tunable output swing (i.e., based on the application) is desirable to save power. Changing the output swing could be achieved in two ways. The first way is to change the number of slices in the SST scheme, affecting the output impedance.

Table 4.2 Illustration for each signal abbreviation presented in Fig. 4.9.

Abbreviation in Fig. 4.9	**The signal name**
V_REF	Reference voltage of the voltage regulator
V_REG	Regulated voltage of the driver
DIN	Input data
DINn	Negative version of the input data
DINp	Positive version of the input data
EN1~EN25	Enable signals for the 25 slices of main tap
EN_F1_1~EN_F1_10	Enable signals for the 10 slices of the first falling edge equalizer tap
EN_F2_1~EN_F2_10	Enable signals for the 10 slices of the second falling edge equalizer tap
DINn(n-1)	Delayed version of the negative version of the input data by 1 UI
DINn(n-2)	Delayed version of the negative version of the input data by 2 UI
EN_R1_1~EN_R1_10	Enable signals for the 10 slices of the first rising edge equalizer tap
EN_R2_1~EN_R2_10	Enable signals for the 10 slices of the second rising edge equalizer tap
EN_Ibias	Enable signal for the VCSEL bias current

The output impedance is an important design requirement, and it should match the electrical link impedance. Therefore, changing the number of slices in the SST scheme is not the appropriate way to tune the output swing. The second way is to change the supply voltage of the SST slices through a voltage regulator.

According to Eq. 4.1 and Eq. 4.2, changing the voltage values with maintaining the value of “R” in the SST slices changes the output current. Eq. 4.7 is obtained based on Eq. 4.1 and Eq. 4.2 (see

Fig. 4.2(b) and Fig. 4.2(c)). From Eq. 4.6, to achieve a low modulation current of 1.5 mA, V_{DD} should be 203 mV when the output impedance R is 50 Ω (i.e., matched with the electrical link impedance) and R_{VCSEL} is 85 Ω (i.e., the load resistance is the input impedance of the used VCSEL model).

$$I_{PU} - I_{PD} = I_1 - I_0 = I_{mod} = \frac{V_{DD}}{R + R_{VCSEL}} \quad \text{Eq. 4.7}$$

where I_{PU} is the pull-up current, I_{PD} is the pull-down current, and I_{mod} is the modulation current.

When the output impedance of the driver matches both the characteristic impedance of the electrical link and the VCSEL input impedance (matched impedances of 85 Ω), V_{DD} will be 0.255 V instead of 0.203 V.

The supply voltage of 203 mV or 255 mV could change the region of operation of the mirroring transistor (i.e., saturation region) in the current mirror (see Fig. 4.5). To guarantee working operation at the saturation region for the mirroring transistor, the following condition should be maintained:

$$V_{SD} > V_{SG} - |V_{tp}| \text{ (Saturation condition)} \quad \text{Eq. 4.8}$$

As the drain of mirroring transistor is connected to the output node of the driver, V_D is equal to $V_{DD}/2$. Also, the source of mirroring transistor is connected to the supply voltage (V_{DD}), and therefore the saturation condition can be expressed as follows:

$$V_G - |V_{tp}| > \frac{V_{DD}}{2} \quad \text{Eq. 4.9}$$

As shown in Fig. 4.9, the voltage regulator consists of an operational amplifier connecting to a PMOS transistor. This PMOS transistor is used to amplify the output voltage of the operational amplifier. By changing the reference voltage (V_REF), the regulated voltage (V_REG) will be changed. The regulated voltage biases the main and equalizers taps.

In Fig. 4.9, C is a 50-pF capacitor, and it is used to decrease the ripples in the regulated voltage. The ripple in the regulated voltage is about 5 mV as shown in Fig. 4.10. It should be stated that

decreasing the value of the capacitor C leads to an increase in the amplitude of the ripples in the regulated voltage. While increasing the capacitor value increases the die area.

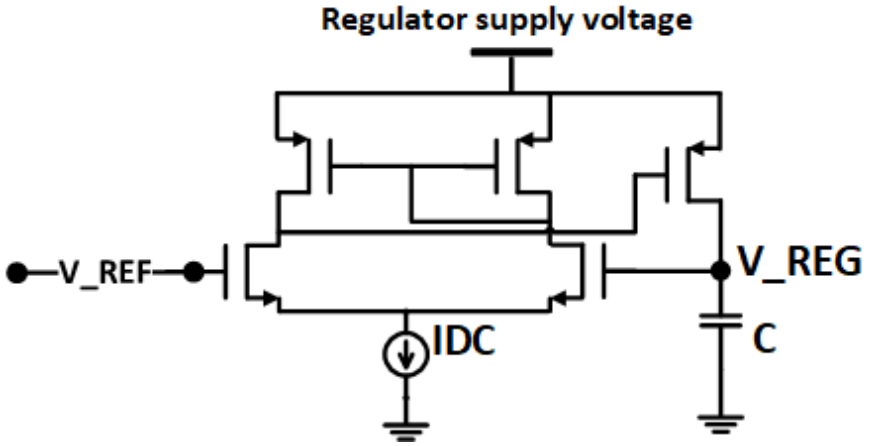


Fig. 4.9 The voltage regulator circuit.

4.4.2 The equalization strategy

Equalization is used to compensate for the electrical link losses, mitigating the ISI and/or the nonlinear behavior of the VCSEL diode. VML is used to design the equalizer taps to guarantee lower power consumption compared to CML equalizer taps. The voltage mode pre-emphasis FFE depends on enlarging the amplitude of the first transmitted bit compared to the second bit as discussed earlier in Chapter 2. Equalization is implemented using a certain number of taps connected to the main tap. The equalization delay used in the three modes of operation is one unit interval (1UI), and it is implemented via D-flip flops.

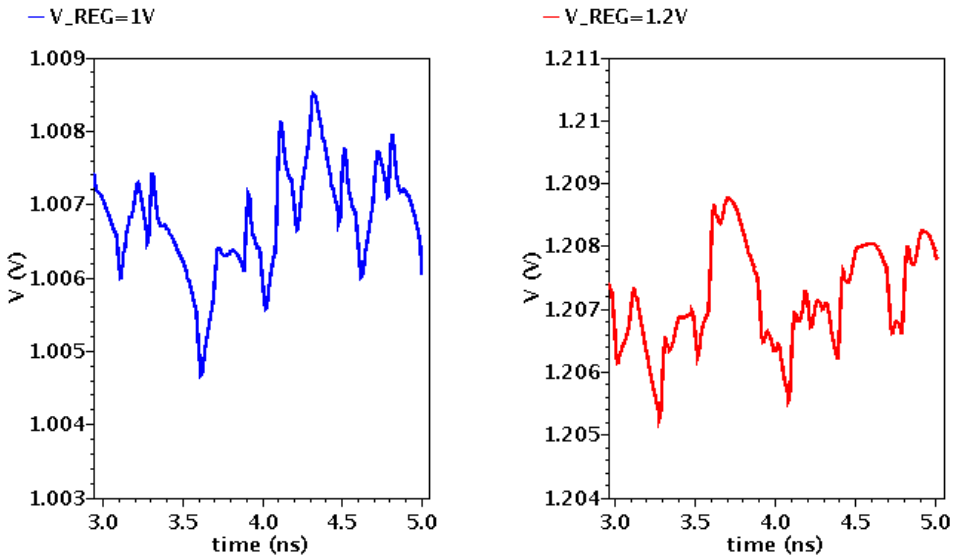


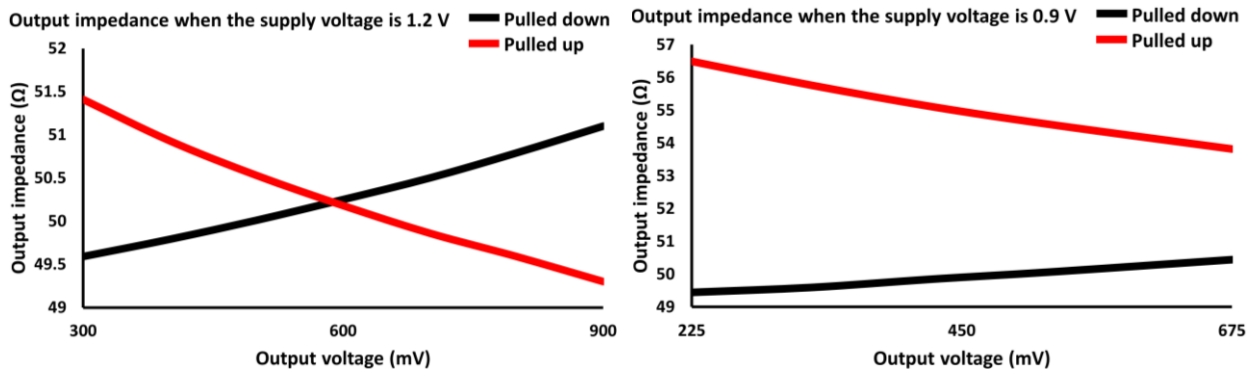
Fig. 4.10 The transient response of V_REG at different reference voltages.

4.4.3 The proposed electrical link driver

The proposed electrical link driver includes a single-ended VML main driver with voltage-mode pre-emphasis FFE. The main driver and equalizer are implemented based on the SST scheme to facilitate impedance matching. The proposed system includes 36 SST slices, where each slice has an output impedance of 1800 Ω. These slices can be enabled or disabled to achieve the required impedance in the presence of process variations, making the output impedance tunable. When connecting these 36 slices in parallel, a theoretical output impedance of 50 Ω is achieved. This result matches the 50 Ω electrical link impedance. During the chip testing phase, if the original output impedance (achieved from the 36 slices) is increased due to PVT, extra slices can be enabled in each tap to maintain a matched output impedance as shown earlier in Fig. 4.9. The simulated output impedance at a supply voltage of 1.2 V for the 36 parallel slices is almost 50 Ω (when the slices are either pulled up or pulled down), as shown in Fig. 4.11(a).

When the supply voltage is 0.9 V and the slices are pulled up, the output impedance of the 36 parallel slices becomes higher than 50 Ω (i.e., varies from 54 Ω to 56.5 Ω). In case of pulling down at the same supply voltage (0.9 V), the output impedance is almost 50 Ω, as shown in Fig. 4.11(b).

This difference in the output impedances is due to the change of the on-state resistance of the PMOS at lower supply voltages as discussed earlier in this chapter. The simulated output impedance (when pulling up) is still close to 50 Ω and it does not affect the output signal as will be discussed later in Fig. 4.15.



(a) (b)

Fig. 4.11 The output impedance of 36 SST slices connecting in parallel at different supply voltages: (a) at a supply voltage of 1.2 V, and (b) at a supply voltage of 0.9 V.

As shown in Fig. 4.12, the proposed electrical link driver consists of the main and the equalizer taps. The outputs of the main and equalizer taps are connected to the 50 Ω electrical channel model. The output of the electrical channel model is connected to a matched load that models the receiver side. There are 21 slices allocated to the main tap, and the remaining slices are allocated to the equalizer tap. The main tap consists of two inputs (data and enable signals). When the enable signal is a binary '1', the slice is activated. Accordingly, an 1800 Ω resistor is connected in parallel with the other slices, decreasing the output impedance and the output current swing. When the enable signal is a binary '0', the slice is disabled, and the disabled slice does not affect the output impedance or current swing.

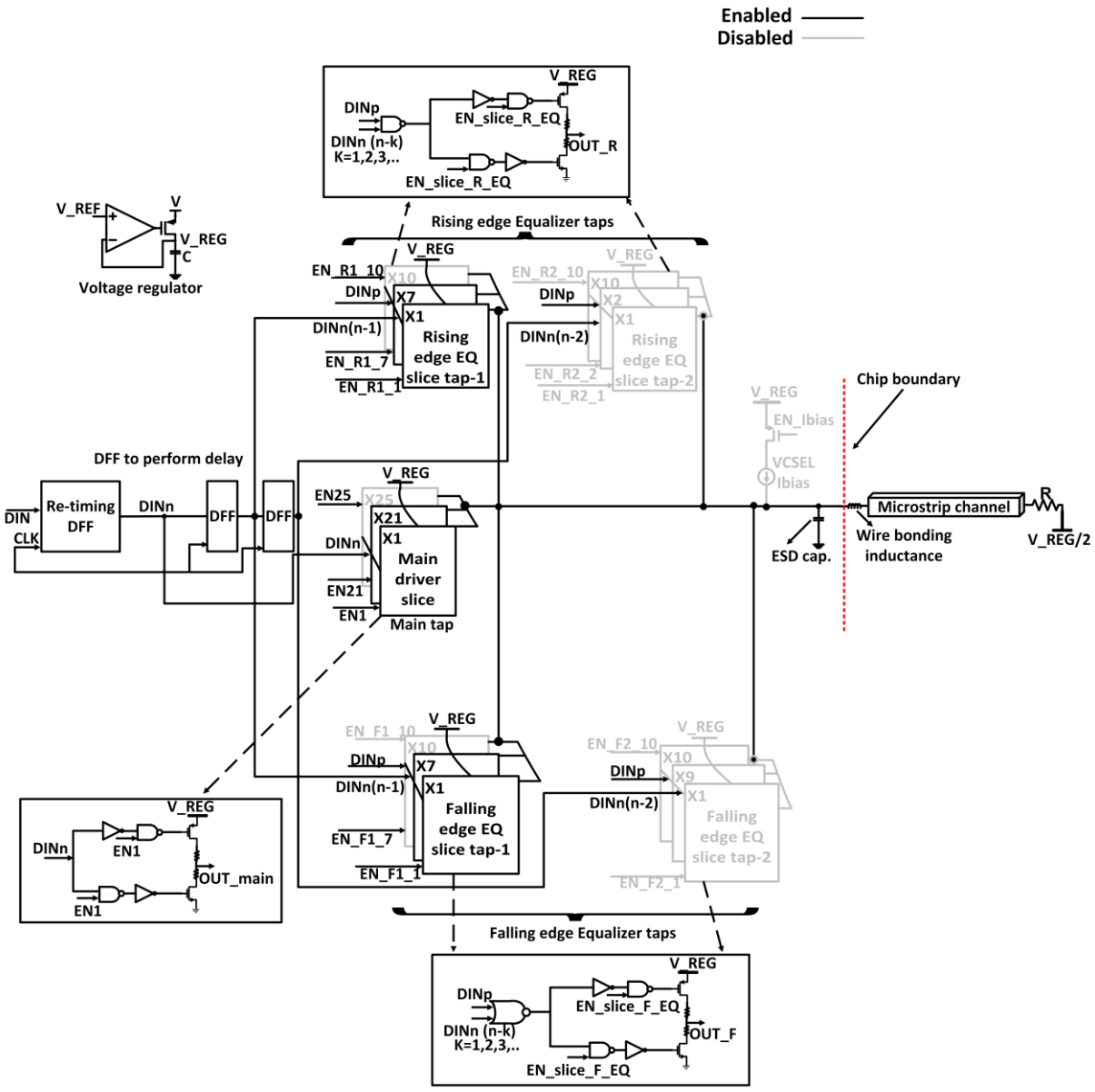


Fig. 4.12 Electrical link driver proposed design.

When working in the electrical link driver mode (mode I), symmetric equalization for both rising and falling edges should be used to compensate the channel loss. Equalization is implemented via a 1-tap equalizer including seven enabled SST slices. The usage of slices in the equalizer supports tuning the output impedance and the equalization ratios. These seven slices of the equalizer tap compensate for a 9.5 dB of losses as follows:

$$20\left(\log_{10}\frac{21}{7}\right) = 9.5\ dB \qquad \text{Eq. 4.9}$$

A separate equalization circuit is used for each edge (i.e., falling edge equalizer and rising edge equalizer) to facilitate toggling between the symmetric and asymmetric equalization when needed. To detect the type of the receiving edge, edge detectors based on logic gates are connected to the input of the equalizer slices.

An example of how the proposed design detects and equalizes the rising edge is shown in Fig. 4.13. To detect a rising edge, both the positive and the delayed versions of the data are connected to a NAND gate. The NAND gate generates a pulse when a rising edge is detected. This generated pulse is the input of the SST rising edge equalizer tap. Both outputs for the main and rising edge equalizer taps are added to generate an equalized signal.

Fig. 4.14 shows the output eye diagram of the electrical link driver (i.e., at the input node of the electrical channel) with and without applying equalization. Equalization reduces the “1” and “0” signal levels, reducing the height of eye opening. The jitter in the eye diagram is due to the used of high data rate.

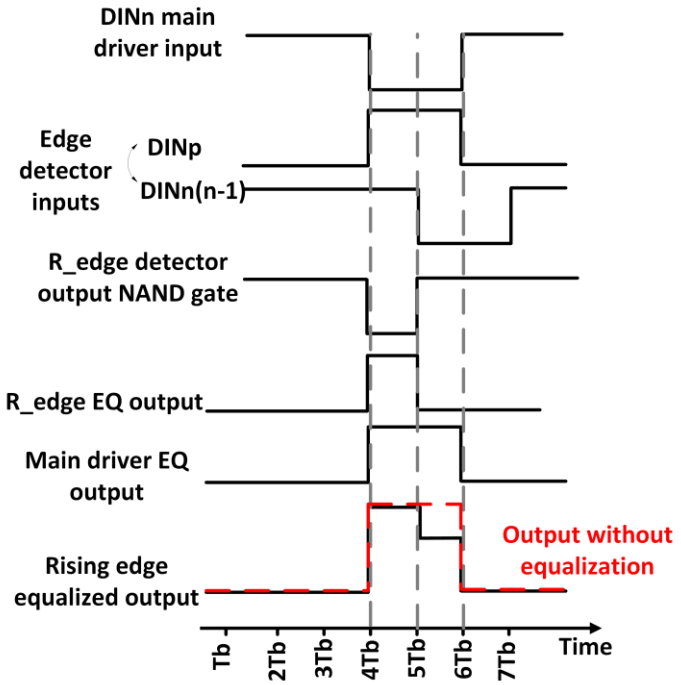


Fig. 4.13 An example showing the rising edge detection and equalization (the "1" level is reduced due to equalization).

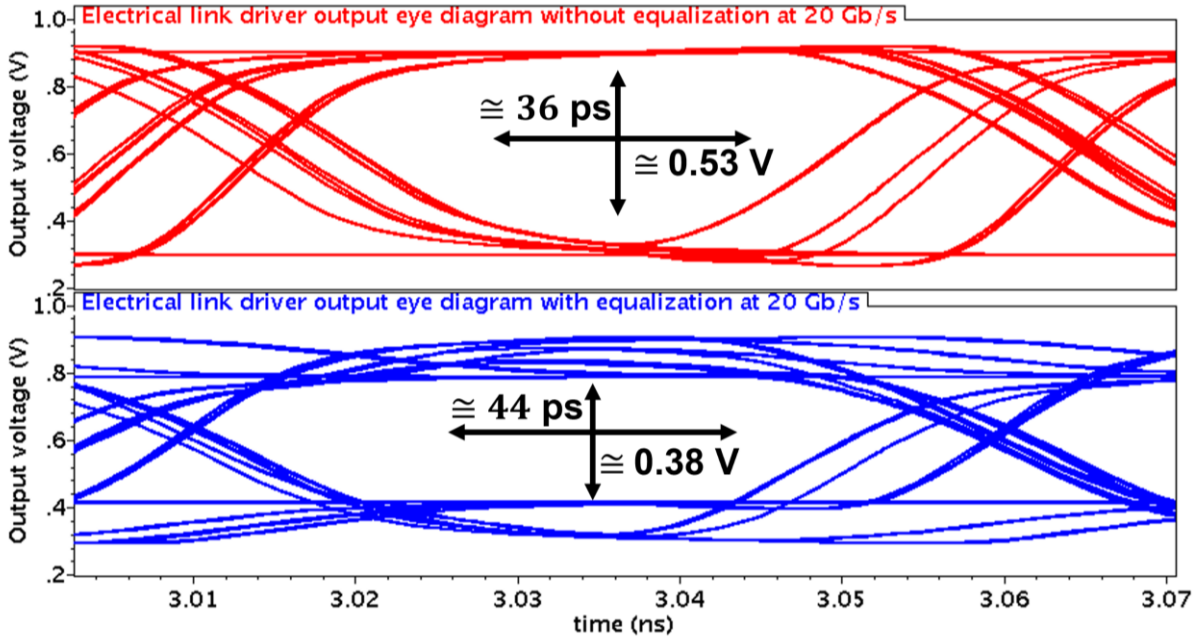


Fig. 4.14 A comparison between the output eye diagrams of the electrical link driver with and without equalization at 20 Gb/s.

The theoretical output peak-to-peak voltage (*Vp-p*) is V_REG/2 when assuming a lossless channel. However, when accounting for loss, the actual value of the peak-to-peak voltage is reduced. The electrical link losses of16 dB is partially compensated by approximately 9.5 dB when using the pre-emphasis FFE., When using different supply voltage of 1.2 V, 1 V, and 0.9 V, the calculated output peak-to-peak voltages from the electrical link are found to be 316 mV, 263 mV, and 240 mV, respectively.

The output swings of the electrical channel are simulated with the corresponding eye diagrams are plotted when using PRBS with a data rate of 20 Gb/s at different supply voltages with same amount of equalization (9.5 dB). The studied supply voltages are 1.2 V, 1 V, and 0.9 V, When the SST slice is pulled up, biasing the driver at voltage less than 0.9 V changes the PMOS transistor region of operation (entering the saturation region).

As shown in Fig. 4.15, at 1.2 V supply voltage, the output eye diagram is almost closed. However, after applying the equalization at the same supply voltage, the output eye diagram is improved with a VEO of 209 mV and a HEO of 45 ps (0.9 UI). The peak-to-peak output voltage is 342 mV.

To study the effect of the supply voltage on the equalized output eye diagram, the system is simulated when using supply voltages of 1 V and 0.9 V. At the supply voltage of 1 V, the VEO is found to be 148 mV, the HEO is 42.3 ps (0.85UI), and the peak-to-peak voltage is reduced to 305 mV. At the supply voltage of 0.9 V as a supply voltage, the VEO is found to be 138 mV, the HEO is 43.5 ps (0.87 UI), and the peak-to-peak voltage is reduced to be 279 mV.

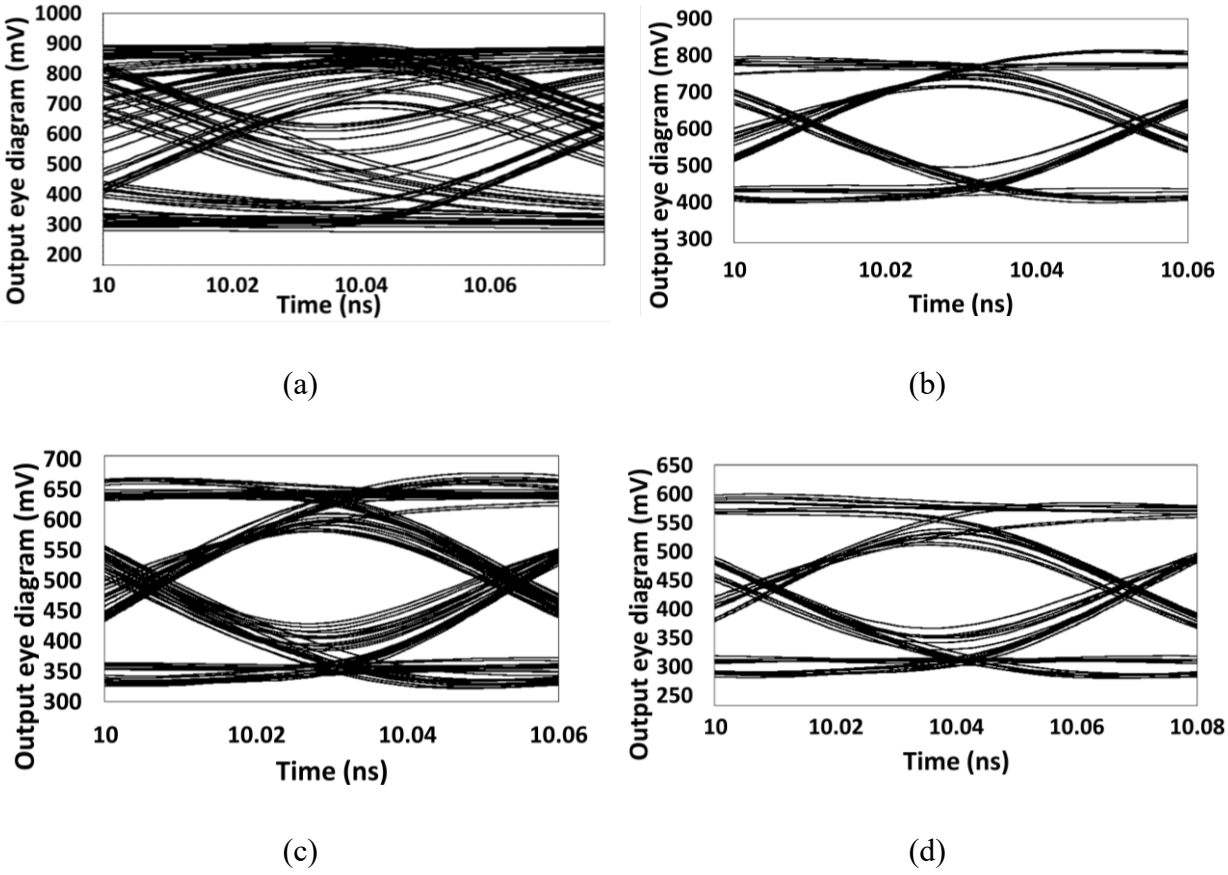


Fig. 4.15 Electrical link output eye diagrams: (a) at 1.2 V supply without applying EQ, (b) at 1.2 V supply after applying EQ, (c) at 1 V supply after applying EQ, and (d) at 0.9 V supply after applying EQ.

4.4.4 Operation mode as a VCSEL diode driver through an electrical link

To drive a VCSEL diode through an electrical link with Z_o of 50 Ω, an output impedance of 50 Ω of the driver should be maintained to reduce the reflections through the link. To guarantee a forward bias for the VCSEL diode, a DC bias current circuit is connected to the output of the proposed driver. The VCSEL diode is biased in a common cathode configuration as shown in Fig. 4.16, with an external negative supply voltage to maintain the turn-on voltage of the VCSEL diode from 1 V to 1.5 V, or higher.

As there is a need to forward bias the VCSEL diode, the current mirror is enabled in this mode of operation (mode II). The output impedance of the current mirror circuit reduces the total output impedance of the 36 parallel connected slices. This leads to reducing the number of the enabled slices from 36 slices to 24 slices using the enable signals, maintaining an output impedance of 50 Ω.

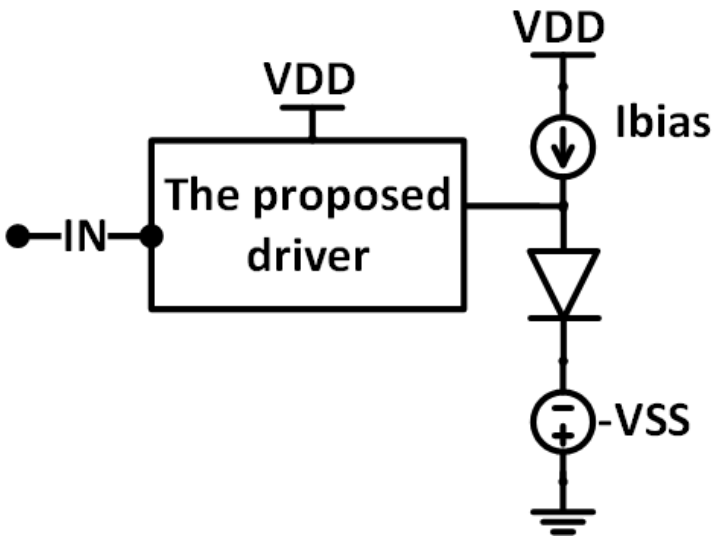
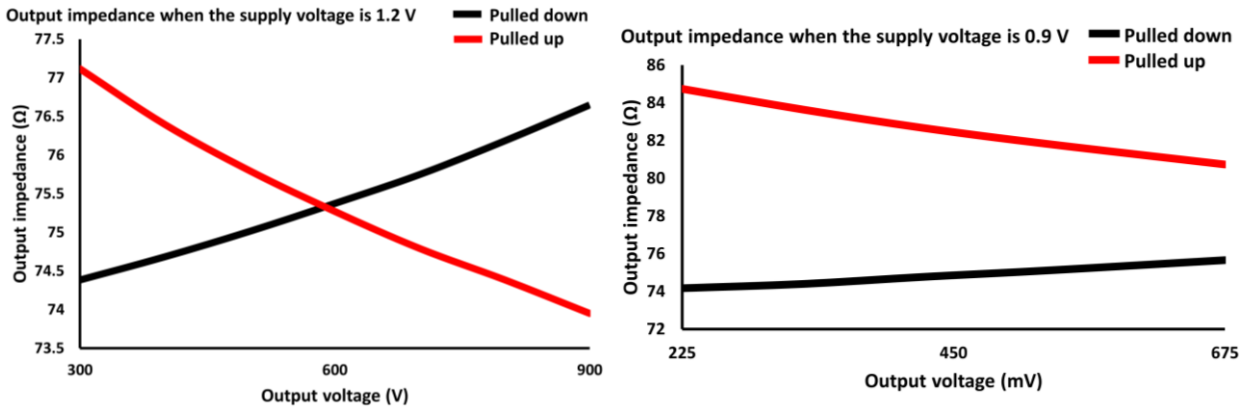


Fig. 4.16 VCSEL diode common cathode configuration biasing.

As shown in Fig. 4.17, the output impedance of the 24 slices (connected in parallel at different supply voltages) varies between 73.5 Ω and 77.5 Ω. This guarantees an output impedance of 50 Ω when connecting these 24 slices to the DC bias current circuit. As shown in Table 4.3 and Table

4.4, the total output impedances after connecting the 24 SST slices to the DC current circuit are almost 50 Ω at different supply voltages.

To drive a VCSEL diode through the electrical link (mode II), another strategy for the equalizer taps is proposed (i.e., asymmetric 2 taps FFE). Asymmetric equalization is used to compensate for the nonlinear behavior of the VCSEL diode. As shown in Fig. 4.18, the proposed design includes 12 SST slices in the main tap, while two taps are used to compensate for the channel loss and the VCSEL nonlinear response. In the rising edge equalizer, there are 4 slices in the first tap and 2 slices in the second tap. In the falling edge equalizer, there are 5 slices in the first tap and 1 slice in the second tap. As mentioned earlier, each slice has an output impedance of 1800 Ω.



(a) (b)

Fig. 4.17 The output impedance of 24 SST slices connected in parallel: (a) at a supply voltage of 1.2 V, and (b) at a supply voltage of 0.9 V.

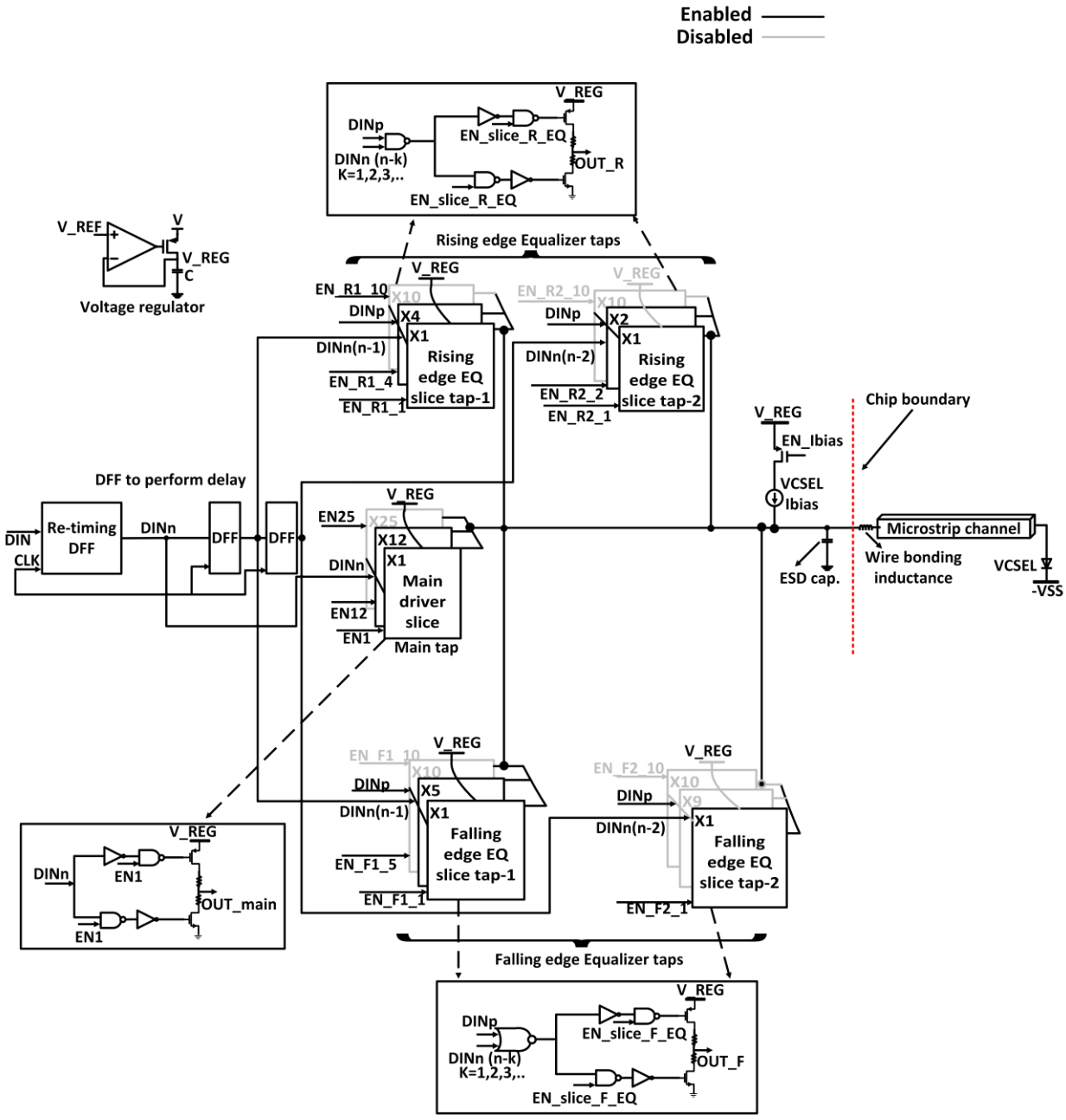


Fig. 4.18 The proposed design of the VCSEL diode driver (through electrical link).

Table 4.3 The current mirror output impedance and total output impedance (24 SST slices connected to the current mirror) at 1.2 V supply voltages.

Output voltage (V)	Current mirror output impedance (Ω)	Total output impedance (Ω)
0.6	182.2	53.6
0.4	184.5	53.1
0.3	186.4	52.8

Table 4.4 The current mirror output impedance and total output impedance (24 SST slices connected to the current mirror) at 0.9 V supply voltages.

Output voltage (V)	Current mirror output impedance (Ω)	Total output impedance (Ω)
0.45	188.4	53.3
0.3	195.5	54.0
0.2	195.7	54.0

As a DC current source is only used for the VCSEL diode driver mode, the current mirror circuit is disabled when working in the electrical link driver mode (mode I) by using a switch connected to the current mirror transistors, as shown in Fig. 4.19. When applying low voltage on the gate of the switch when the switch is enabled (on), the current mirror is enabled.

When applying a high voltage on the gate of the switch (i.e., switch is off), the current mirror is disabled. The mirroring ratio in the current mirror is 20 (i.e., applied on the enabling switches as well), and the size of the mirroring transistor size ratio is 100 um/60 nm (as discussed earlier in section 4.3). The on-state resistance of the switch is about 3.5 Ω (i.e., 400 um/60 nm) to avoid any significant effects on the supply voltage of the current mirror.

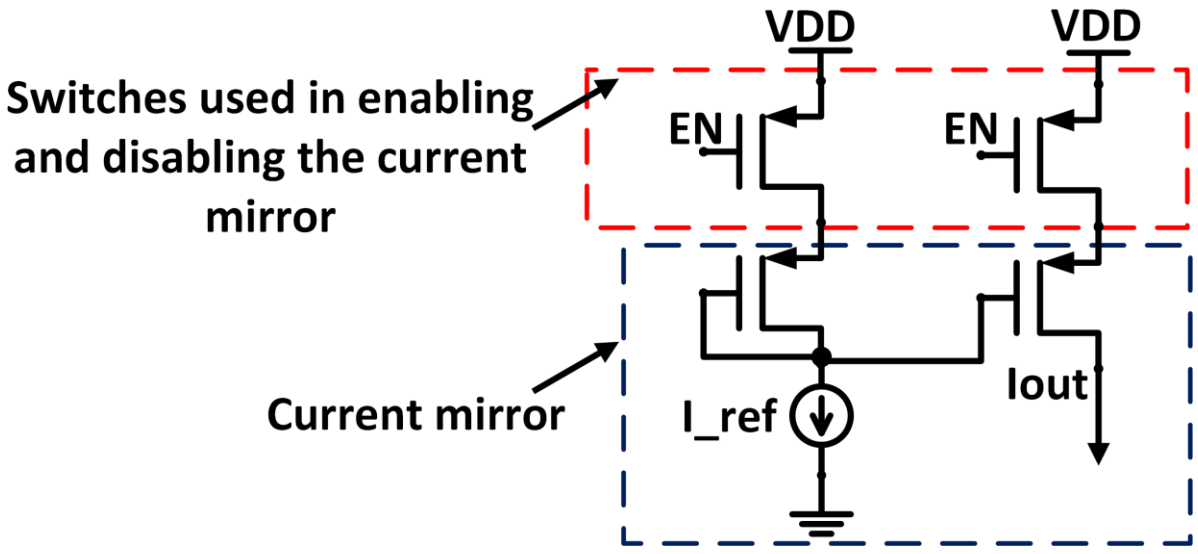


Fig. 4.19 DC current biasing circuit which can be enabled and disabled. (At EN = "0", the switch is enabled and V_{DD} is connected to the current mirror, and when EN = "1", the switch is disabled and V_{DD} is disconnected to the current mirror).

The proposed design is simulated using PRBS at data rate of 20 Gb/s and different supply voltage with same amount of equalization. The output optical power is simulated, and its corresponding eye diagram is plotted. As shown in Fig. 4.20, at 1.2 V supply voltage and without applying any equalization (i.e., 24 SST slices connected in parallel), the optical output eye diagram has a VEO of 0.97 mW, HEO of 26 ps (0.52UI), and OMA of -0.13 dBm. The values of OMA are determined from the internal VEO of the eye diagram.

After applying the proposed asymmetric equalization, the optical output eye diagram is enhanced, and it offers a VEO of 1.35 mW (i.e., improved by 39.2%), HEO of 41.5 ps (0.83 UI) (i.e., improved by 59.6%), and an OMA of 1.3 dBm.

To study the effect of the supply voltage on the equalized output eye diagram, the system is simulated when using supply voltages of 1 V and 0.9 V. At the supply voltage of 1 V, the optical output power offers a lower OMA of 0.79 dBm with VEO of 1.2 mW and HEO of 42.2 ps (0.84UI). At the supply voltage of 0.9 V with same amount of equalization, the optical output power showed the lowest OMA of 0.57 dBm with VEO of 1.14 mW and HEO of 43.7 ps (0.87 UI).

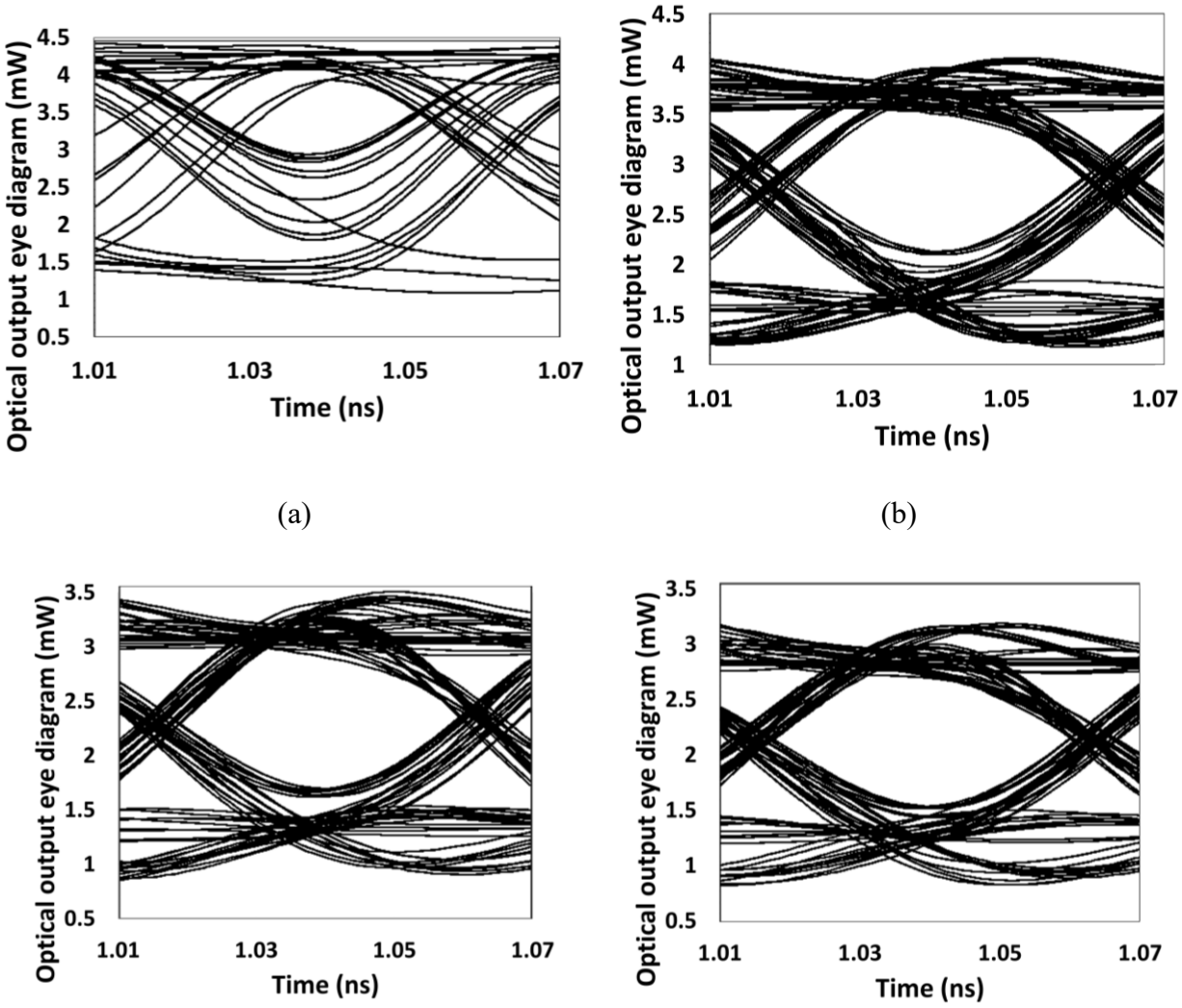


Fig. 4.20 Optical output eye diagrams when the proposed design is working as a VCSEL diode driver through an electrical link: (a) output eye diagram at 1.2 V supply without applying equalization, (b) output eye diagram at 1.2 V supply with applying equalization, (c) output eye diagram at 1 V supply with applying equalization, and (d) output eye diagram at 0.9 V supply with applying equalization.

The modulation currents (Fig. 4.21) when using different supply voltages produced from the proposed design are 3.5 mA, 2.5 mA, and 2.3 mA at 1.2 V, 1 V, and 0.9 V, respectively. The modulation current represents the maximum swing of the output current from the electrical link. The minimum current to bias the VCSEL diode is about 2.5 mA. To achieve a minimum bias

current of 2.5 mA, a negative supply voltage of 1.13 V, 1.2 V, and 1.25 V are used to bias the VCSEL diode with DC current of 6.5 mA, 5.6 mA, and 5.4 mA at supply voltage of 1.2 V, 1 V, and 0.9 V, respectively.

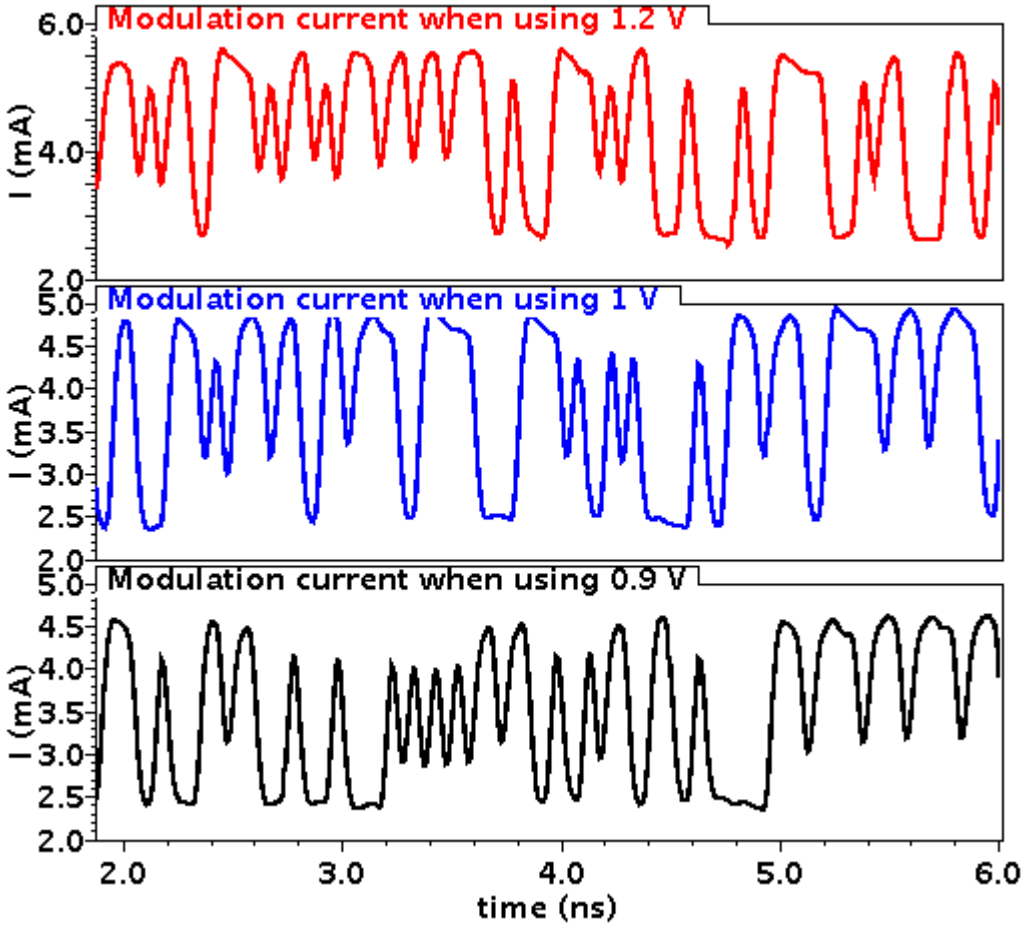


Fig. 4.21 The modulation currents at different supply voltages.

As the VCSEL input impedance is 85 Ω, the conventional characteristic impedance (Z_o) of the electrical link (50 Ω) is not the optimum value. To reduce the reflections as mentioned in Chapter 2, Z_o of the electrical link should be matched with the output impedance of the driver and the load impedance (i.e., VCSEL input impedance in this case). To achieve that, two main requirements are needed, (a) an electrical link with Z_o of 85 Ω, and (b) increasing the output impedance of the driver to 85 Ω.

To increase the value of the output impedance of the driver, a total number of 21 slices should be enabled out of 36 slices. However, the output impedance of the DC current source should be considered as discussed earlier (Tables 4.4, and 4.5). When considering the output impedance of

the current mirror, the number of slices is reduced to 12 slices so that the total output impedance of the driver is 85 Ω. As shown in Fig. 4.22, the proposed design contains seven slices in the main tap., For the rising edge equalizer, three slices are allocated to tap-1 and one slice is assigned to tap-2. While for the falling edge, two slices are allocated for tap-1 and one slice is assigned to tap-2.

The system is simulated at supply voltage of 1.2 V using a PRBS at 20 Gb/s. The eye diagram of the output optical power generated by the VCSEL diode is plotted (Fig. 4.23). Without applying equalization, the VEO is 1.1 mW (0.41 dBm as OMA), and the HEO is 34 ps (0.68UI). After applying equalization, no change is found in the value of the VEO, but the HEO is improved by 23.5% and it is equals to 42 ps.

To study the effect of reducing the supply voltage on the equalized output eye diagram, the system is simulated when using supply voltage of 1 V. The modulation current becomes almost 1.5 mA (i.e., the minimum modulation current in the targeted range). When using the same equalization ratios applied at 1.2 V supply, the OMA is -1.4 dBm, and the HEO is 41 ps (0.82UI) as shown in Fig. 4.24.

A comparison is performed between two cases of driving the VCSEL diode through electrical link, (a) matched electrical link driver (85 Ω), and (b) mismatched electrical link driver (50 Ω). The following observations are concluded based on this comparison:

- Without applying equalization, the OMA is higher when driving the VCSEL through a matched electrical link driver (i.e., 0.41 dBm for the 85 Ω electrical link driver vs. -0.13 dBm for the 50 Ω electrical link driver).
- The modulation current when using 85 Ω electrical link driver (2.2 mA) is lower compared to the 50 Ω electrical link driver (3.5 mA) at 1.2 V supply voltage. This observation is expected as the output impedance is increased.

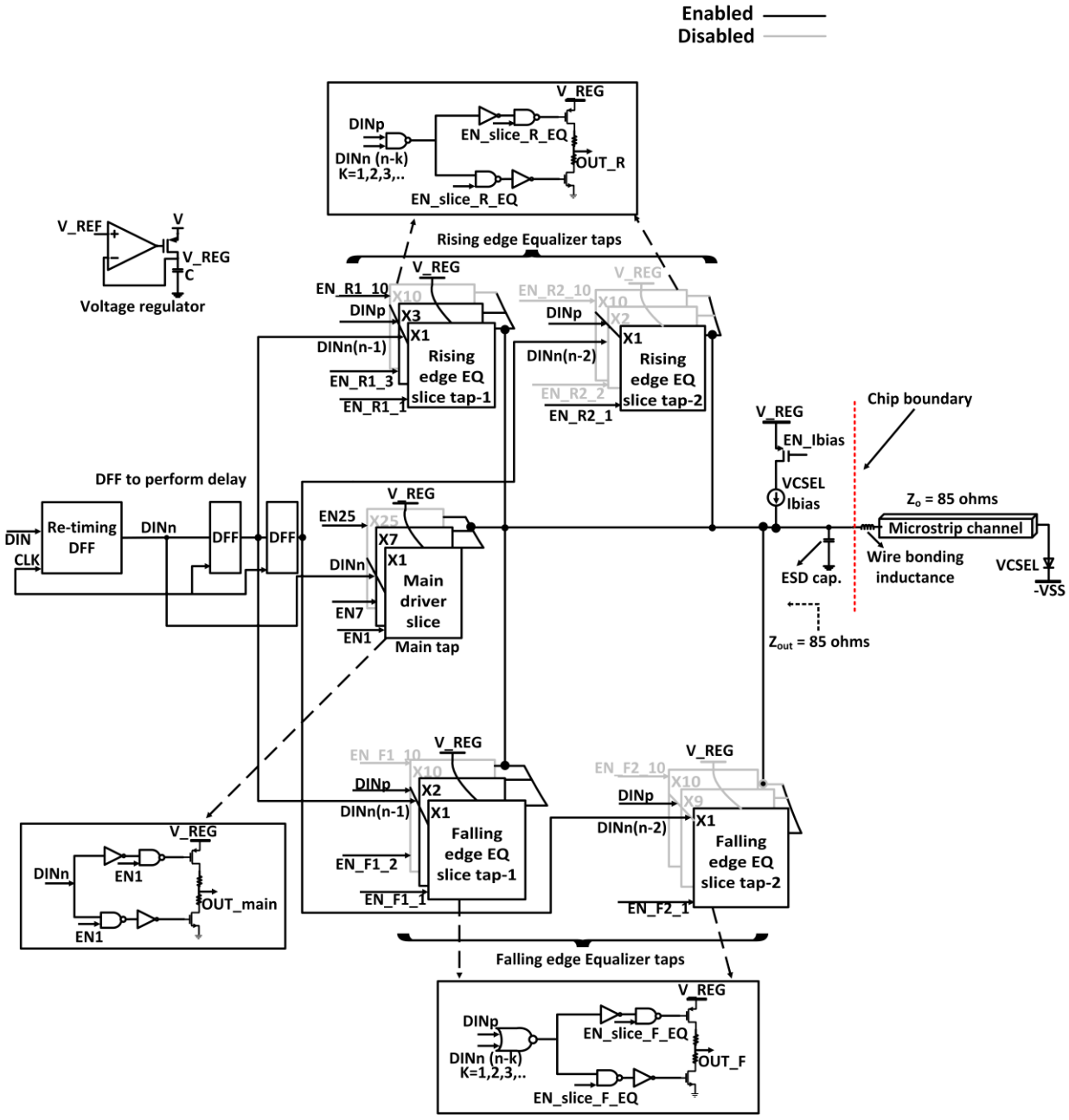
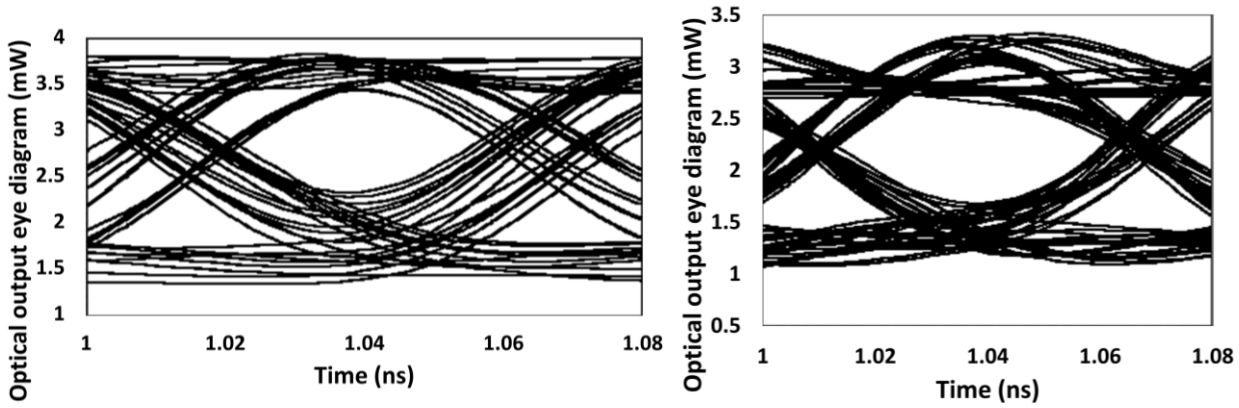


Fig. 4.22 The proposed VCSEL driver through electrical link (mode II) with matched impedance of 85 Ω.



(a) (b)

Fig. 4.23 The optical output eye diagram at 20 Gb/s and supply voltage of 1.2 V, (a) with no equalization, (b) with equalization.

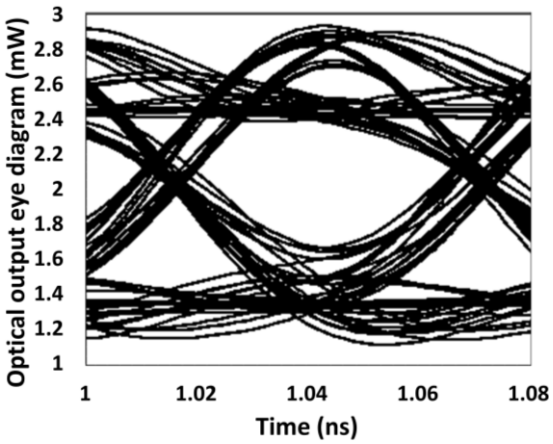


Fig. 4.24 The optical output eye diagram at 20 Gb/s and supply voltage of 1 V with equalization.

4.4.5 Operation as a VCSEL diode driver without electrical link

The proposed design can drive either an electrical link (mode I) or a VCSEL diode through an electrical link (mode II). Working in these two modes of operation requires achieving some design specifications, for example, maintaining a specific output impedance. When applying the proposed design to drive a VCSEL diode directly (i.e., no electrical link between the diode and the proposed driver), the output impedance is not required to match a certain value. However, the driver output impedance is preferable to be relatively low (i.e., below 100 Ω [3]) to reduce the ringing in the VCSEL output power [3]. In the proposed design, 23 of the SST slices are connected in parallel, providing an output impedance of 112.5 Ω. These slices are then connected to the DC biasing current to maintain a bias current for the VCSEL diode above the threshold current (0.6 mA). The total output impedance is almost 50 Ω at an output voltage of $V_{DD}/2$. As shown in Fig. 4.25, to directly drive a VCSEL diode, 16 slices are allocated to the main tap, four slices are allocated for the rising edge equalizer tap, and three slices are allocated for the falling edge equalizer tap.

The proposed design is simulated after connecting the VCSEL model directly to the output of the proposed design and using PRBS as an input. After that, the output optical power from the VCSEL diode is measured at different supply voltages with same amount of equalization, and their corresponding eye diagrams are plotted as shown in Fig. 4.26. The proposed design is simulated at two data rates (15 Gb/s and 20Gb/s) at supply voltage of 1.2 V. At 15 Gb/s, the OMA, VEO, and HEO are found to be 4.31 dBm, 2.7 mW, and 65.2 ps (0.98 UI), respectively. At 20 Gb/s, the OMA, VEO, and HEO are found to be 3.8 dBm, 2.4 mW, and 42.6 ps (0.85 UI), respectively.

Equalization at 20 Gb/s improves both VEO and HEO by almost 9% compared to the output eye diagram without applying any equalization at the same data rate and supply voltage, see Fig. 4.26(a). It is observed that at 15 Gb/s, the ringing in the optical output power is relatively small compared to the optical output power at 20 Gb/s.

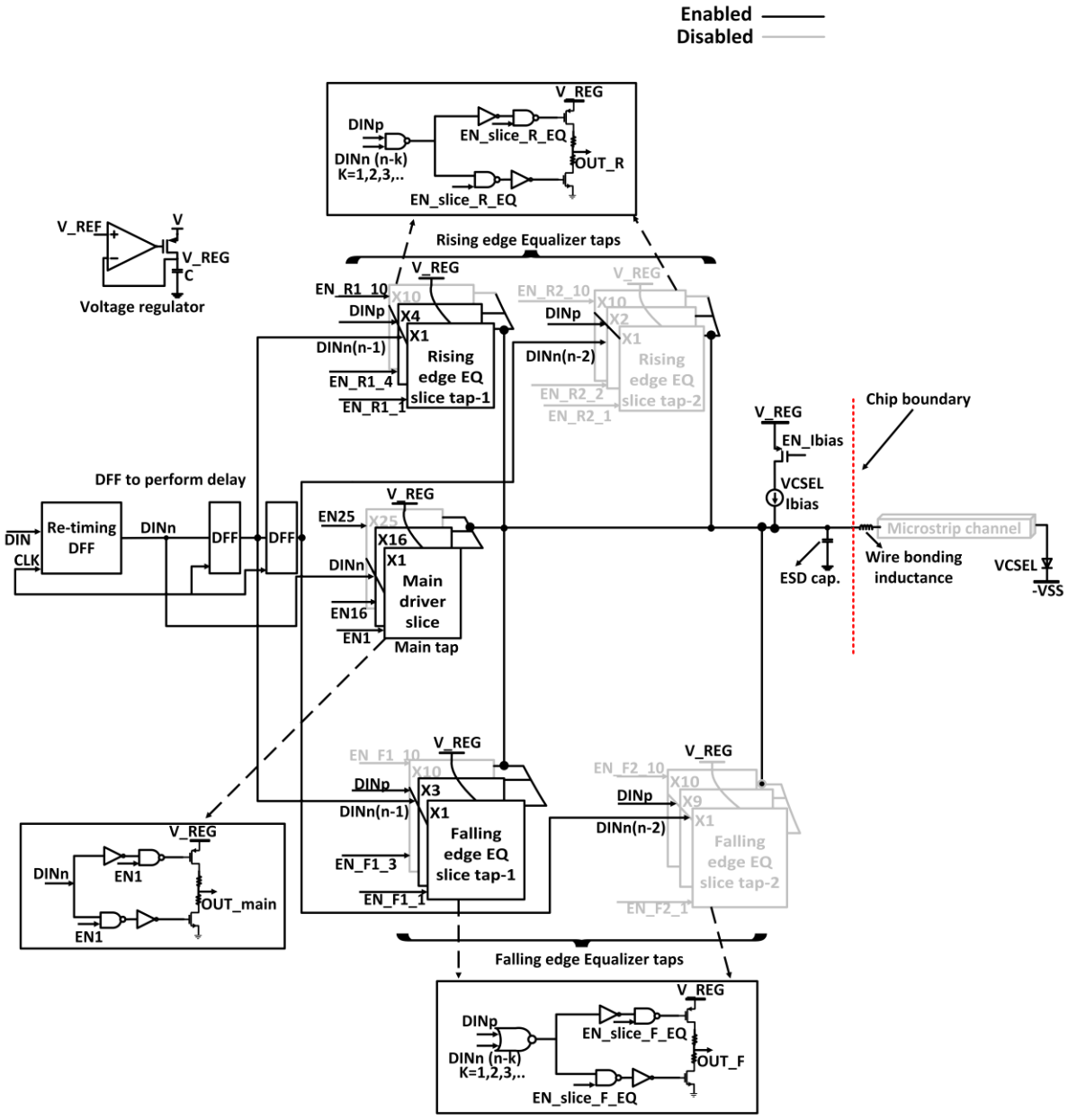


Fig. 4.25 The proposed design when direct driving the VCSEL diode (mode III).

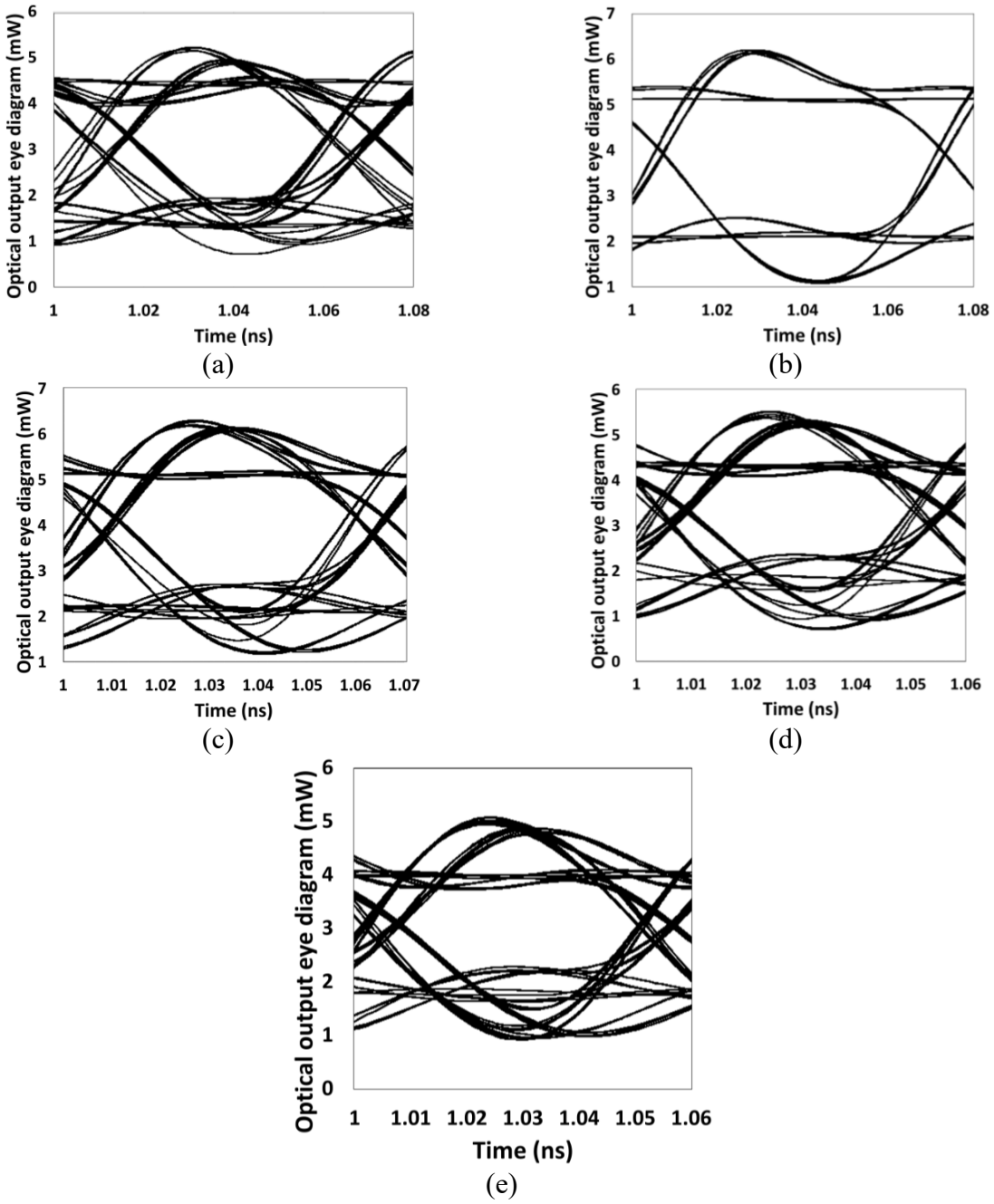


Fig. 4.26 Optical output eye diagram when the proposed design drives a VCSEL diode directly: (a) output eye diagram at 1.2 V supply and without applying EQ at data rate of 20 Gb/s, (b) output eye diagram at 1.2 V with applying EQ at data rate of 15 Gb/s, (c) output eye diagram at 1.2 V supply and applying EQ at data rate of 20 Gb/s, (d) output eye diagram at 1 V supply and applying EQ at data rate of 20 Gb/s, and (e) output eye diagram at 0.9 V supply and applying EQ at data rate of 20 Gb/s.

To study the effect of the supply voltage on the equalized output eye diagram, the system is simulated when using supply voltages of 1 V and 0.9 V. At a supply voltage of 1 V, the proposed design is simulated at data rate of 20 Gb/s with the same amount of equalization. It is found that the OMA is 2.5 dBm, the VEO is 1.77 mW, and the HEO is 42.7 ps (0.85 UI). When reducing the supply voltage to 0.9 V and using data rate of 20 Gb/s, it is found that the OMA is 1.88 dBm, the VEO is 1.54 mW, and the HEO is 42.5 ps (0.85UI).

The modulation currents when using different supply voltages (Fig. 4.28) produced from the proposed design are 4.5 mA, 4 mA, and 3.5 mA at 1.2 V, 1 V, and 0.9 V, respectively. The minimum current to bias the VCSEL diode is about 3 mA. To achieve a minimum bias current of 3 mA, a negative supply voltage of 1.21 V, 1.27 V, and 1.32 V are used to bias the VCSEL diode with a DC current of 9.2 mA, 7.9 mA, and 7.5 mA at supply voltages of 1.2 V, 1 V, and 0.9 V, respectively. Table 4.5 summarizes the performance of the proposed design operating in mode II and mode III. In case of driving the VCSEL diode through an electrical link (mode II), both OMA and modulation current are reduced due to the losses of the electrical link. However, the obtained OMAs in mode II are still better compared to the OMA obtained in other designs in the literature [1,4,16].

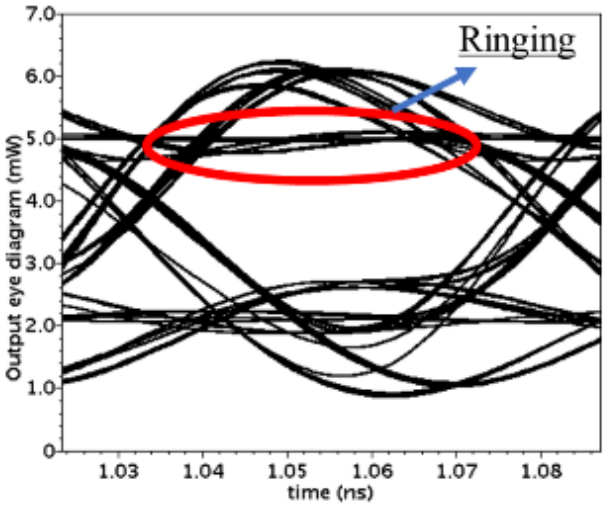


Fig. 4.27 Output eye diagram for the VCSEL diode when increasing the equalization ratio for both edges at 1.2 V and 20 Gb/s as a data rate, ringing start to appear in the “1” signal level.

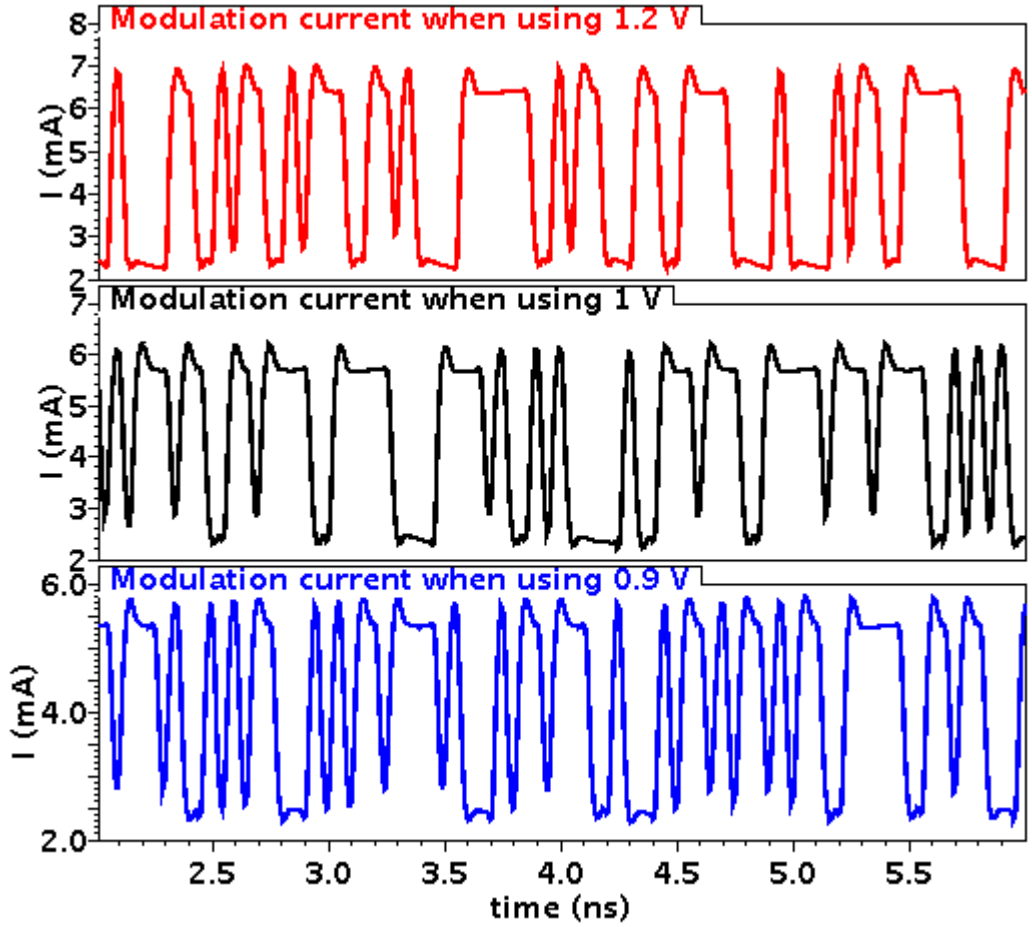


Fig. 4.28 The modulation current at different supply voltages.

Table 4.5 A comparison between driving VCSEL diode directly (mode III) and through electrical link (mode II) at different supply voltages (1.2 V, 1 V, and 0.9 V).

	With electrical link			**Without electrical link**		
Supply voltages	**1.2 V**	**1 V**	**0.9 V**	**1.2 V**	**1 V**	**0.9 V**
Modulation current (mA)	3.5	2.5	2.3	4.5	4.0	3.5
OMA (dBm)	1.3	0.79	0.57	3.8	2.5	1.88
Equalization	2-taps asymmetric FFE			1-tap asymmetric FFE		

4.5 A modified design when using a supply voltage below 0.9 V

At supply voltage of 0.9 V, the modulation current when operating mode II (i.e., drive VCSEL diode through 50 Ω electrical link) is 2.3 mA. This modulation current is far from the lower value in the range (i.e., 1.5 mA to 4.5 mA) mentioned in the thesis objectives. To solve this issue, the supply voltage needs to be reduced below 0.9 V. However, the on-state resistance of the PMOS transistor is significantly increased when lowering the supply voltage below 0.9 V (as mentioned before in Table 4.1 and section 4.3). In addition, the PMOS transistor enters the saturation region when lowering the supply voltage below 0.9 V. Also, at supply voltages are less than 0.9 V, the mirroring transistor in the DC bias current enters the triode region as V_{SD} becomes smaller than (V_{SG} - V_{tp}) when the output voltage of the driver is equal to $V_{DD}/2$. Therefore, two modifications in the proposed design are suggested to address the abovementioned problems.

- 1st modification: to solve the problem related to the region of operation and the on-state resistance of the PMOS transistor, another PMOS transistor is connected in parallel with the original PMOS transistor as shown in Fig. 4.29.

This parallel PMOS transistor acts as a variable resistor which has the same on-state resistance of the original one. By connecting this extra PMOS transistor, the on-state resistance of the original PMOS transistor of the SST slice is divided by 2. This solution should be enabled only when V_REG is below 0.9 V. This modification is valid only when using supply voltage below 0.9 V because the output impedance of both pull-up and pull-down networks are almost the same when using supply voltage above 0.9 V. Therefore, a two-input OR gate is used to control the status of the additional transistor. The first input is an enable signal (EN_PMOS), while the second input is the data needed to be transmitted. As shown in Table 4.6, when the enable signal is low, the parallel PMOS transistor is enabled; however, it is ON (i.e., SST slice is pulled-up) when the input data is binary “0”. When the enable signal is high, the parallel PMOS is disabled regardless of the value of the input data. This modification on the SST slice is applied to all slices used in the proposed design. Accordingly, all slices in the proposed design have two enable signals, one for the slice itself and the other one for the extra PMOS.

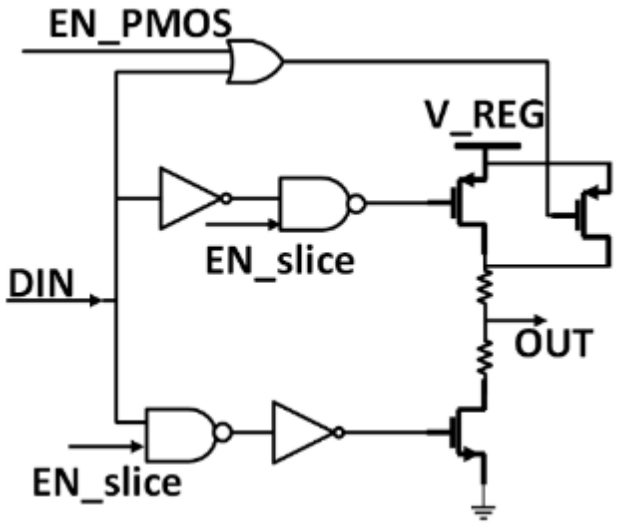


Fig. 4.29 Parallel PMOS transistor proposed solution (1st modification).

Table 4.9 summarizes the status of the enable signals (i.e., EN_Slice, and EN_PMOS) when using different supply voltages. As shown in Table 4.7, at any supply voltage, the EN_Slice signal can be high or low based on the required output impedance and equalization ratio. However, the EN_POMS signal is only enabled when working at supply voltage lower than 0.9 V.

Table 4.6 The effect of different input cases of the status of the parallel PMOS.

EN_PMOS	**DIN**	**OR gate output**	**Status of the parallel PMOS**
0	0	0	Enabled, but ON only when the data is 0
0	1	1	
1	0	1	Disabled
1	1	1	

Table 4.7 The status of the enable signals in each slice at different supply voltages.

Supply voltage	**1.2 V (> 0.9 V)**			**0.6 V (< 0.9 V)**		
Signal name	**EN_Slice**		**EN_PMOS**	**EN_Slice**		**EN_PMOS**
Status	1 (Enabled)	0 (Disabled)	1 (Disabled)	1 (Enabled)	0 (Disabled)	0 (enabled)

In order to guarantee that each slice is working properly, the inputs of NMOS and PMOS transistors (applied to the gate of the transistors) in the SST slice and the parallel PMOS transistor should have the same amount of delay for the input data. The gates used at the inputs of the three transistors have the same amount of delay. These gates are, a) NAND and NOT gate connected in between the data signal and the original SST slice (i.e., enable logic), and b) OR gate (i.e., NOT and NOR gate) connected between the data signal and the extra parallel PMOS. This approach is validated in Fig. 4.30.

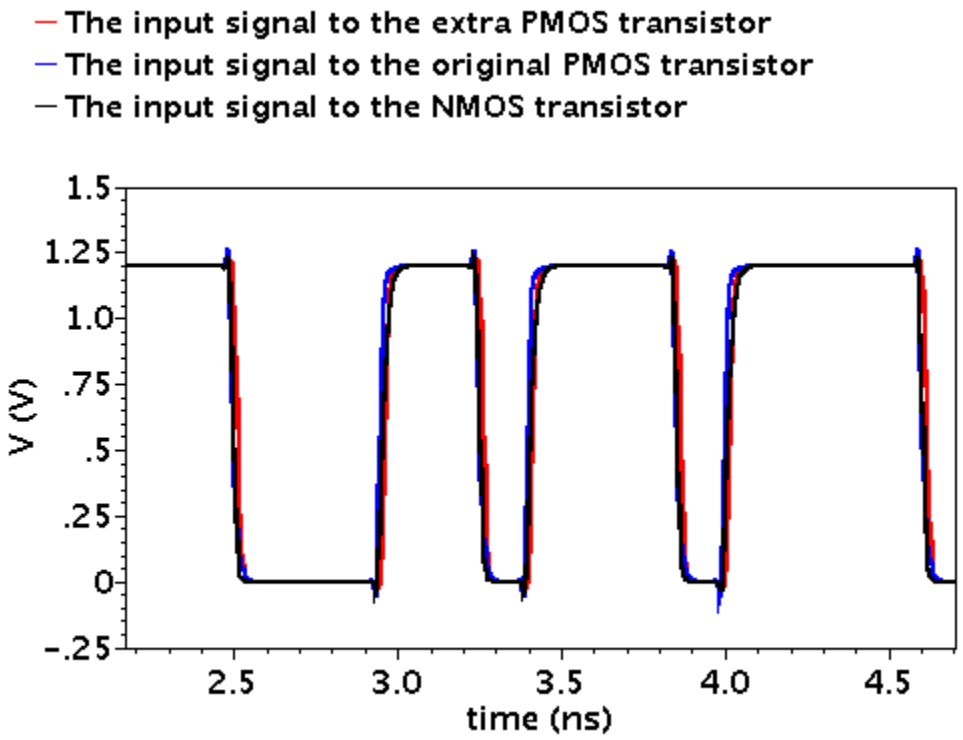


Fig. 4.30 The input signals for the three transistors overlapped on each other.

After applying the parallel PMOS transistor modification, the output impedance at 0.6 V for the entire system when operating in mode II (VCSEL driver through a 50 Ω electrical link) is provided as shown in Fig. 4.31. When the input is binary "0", the slices in the main tap are pulled up and the total output impedance of these slices varies between 160 Ω and 170 Ω. In addition, the slices of the falling edge equalizer are pulled up and their total output impedance varies between 320 Ω and 350 Ω. The total output impedance of the proposed system is almost constant at 58 Ω.

Without applying the parallel transistor modification, the output impedance from the driver varies between 34 Ω to 84 Ω at different output voltages when the input is binary "0". This high variation happens due to the variation in the output impedances for the main tap (884 Ω and 266 Ω) and the falling edge equalizer tap (1.8 kΩ and 0.5 kΩ).

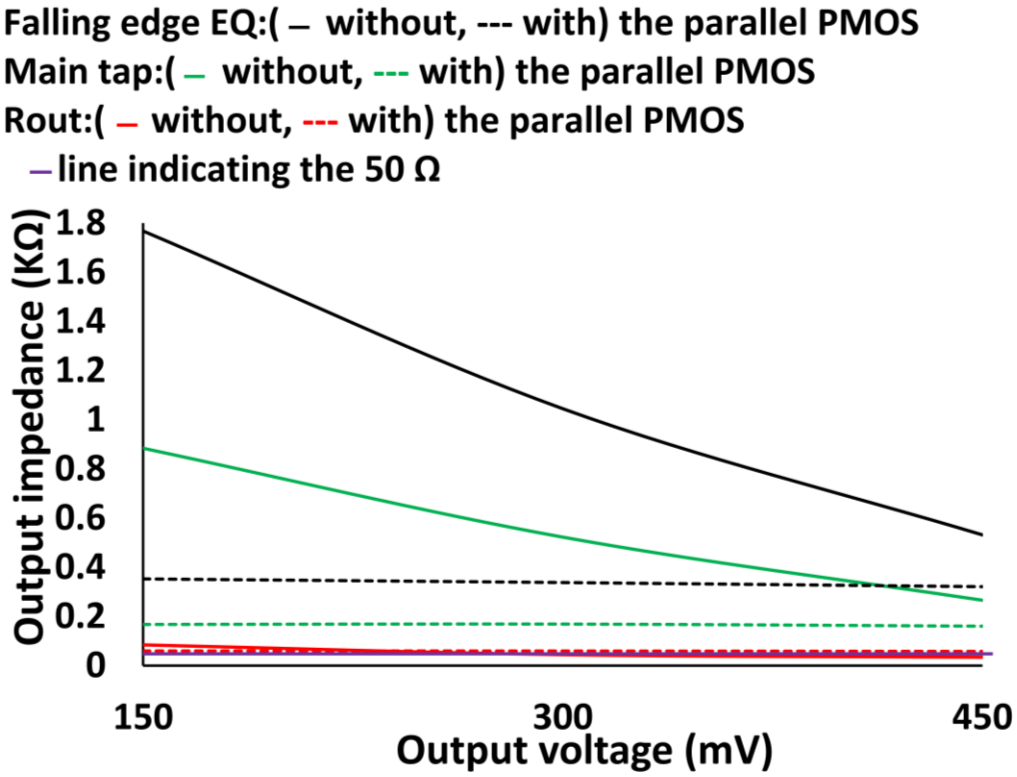


Fig. 4.31 The output impedance of the proposed design when operating in mode II at supply voltage of 0.6 V and the input is binary "0" with and without applying the parallel transistor modification.

- 2nd modification: for the problem of the DC current source, it can be solved through changing the bias supply voltage when working below 0.9 V. As shown in Fig. 4.32, instead of using one switch (with one enable signal) to enable and disable the DC current biasing, two switches are used to select the desired value of the supply voltage. The first supply voltage is the regulated voltage which can be selected when working at supply voltage of 0.9 V or above. The second supply voltage is 1.2 V which can be selected when working at supply voltage below 0.9 V.

By applying the above-mentioned modifications, the VCSEL driver through electrical link (mode II) is allowed to be biased at 0.6 V which leads to a modulation current of 1.5 mA (i.e., targeted modulation current). The entire system after applying these modifications is shown in Fig. 4.33.

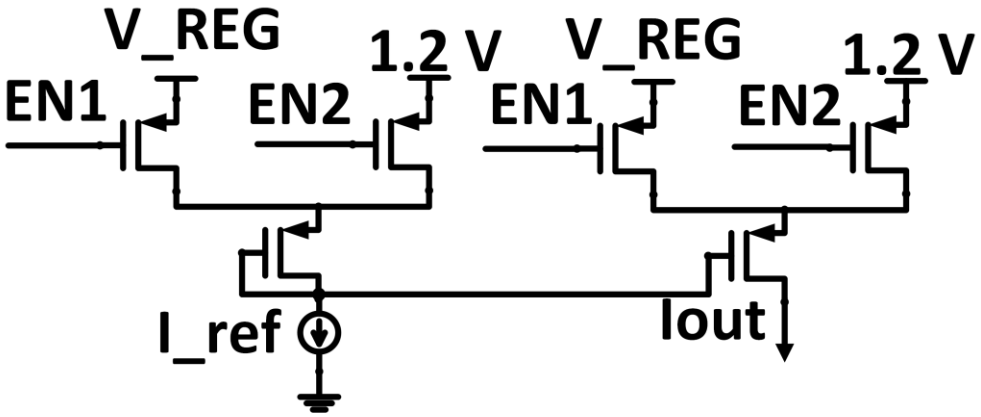


Fig. 4.32 The applied 2nd modification on the design of the current mirror.

The modified system (VCSEL driver through electrical link) is simulated at supply voltages of 0.7 V, and 0.6 V using PRBS and at a data rate of 20 Gb/s. The output optical power is obtained, and its corresponding eye diagram is plotted as shown in Fig. 4.34.

At supply voltage of 0.7 V, with same amount of equalization mentioned in section 4.4.3, the VEO is 0.75 mW, the HEO is 41.2 ps (0.83 UI), and the corresponding OMA is about -1.25 dBm. The modulation current at this supply voltage is 1.7 mA. When reducing the supply voltage to 0.6 V, with same amount of equalization mentioned in section 4.4.3, the OMA becomes -1.67 dBm with VEO of 0.68 mW and HEO of 40.4 ps (0.81UI).

If the receiver sensitivity is assumed to be -7.5 dBm as mentioned in [20], and the OMA is -1.67 dBm which was obtained when the supply voltage is 0.6 V, the link margin will be 5.83 dB. It is recommended that the link margin should be between 4.6 dB to 12.6 dB as mentioned in [21]. Based on that, the OMA value obtained when reducing the supply voltage to 0.6 V can be considered as a suitable value.

When the modulation current is 1.5 mA, the OMA in the 85 Ω VCSEL driver through electrical link (-1.5 dBm, see Fig. 4.24) is higher compared to the obtained value (-1.67 dBm, see Fig. 4.34(b)) in 50 Ω VCSEL driver through electrical link. This is excepted when using a matched impedance over the whole line.

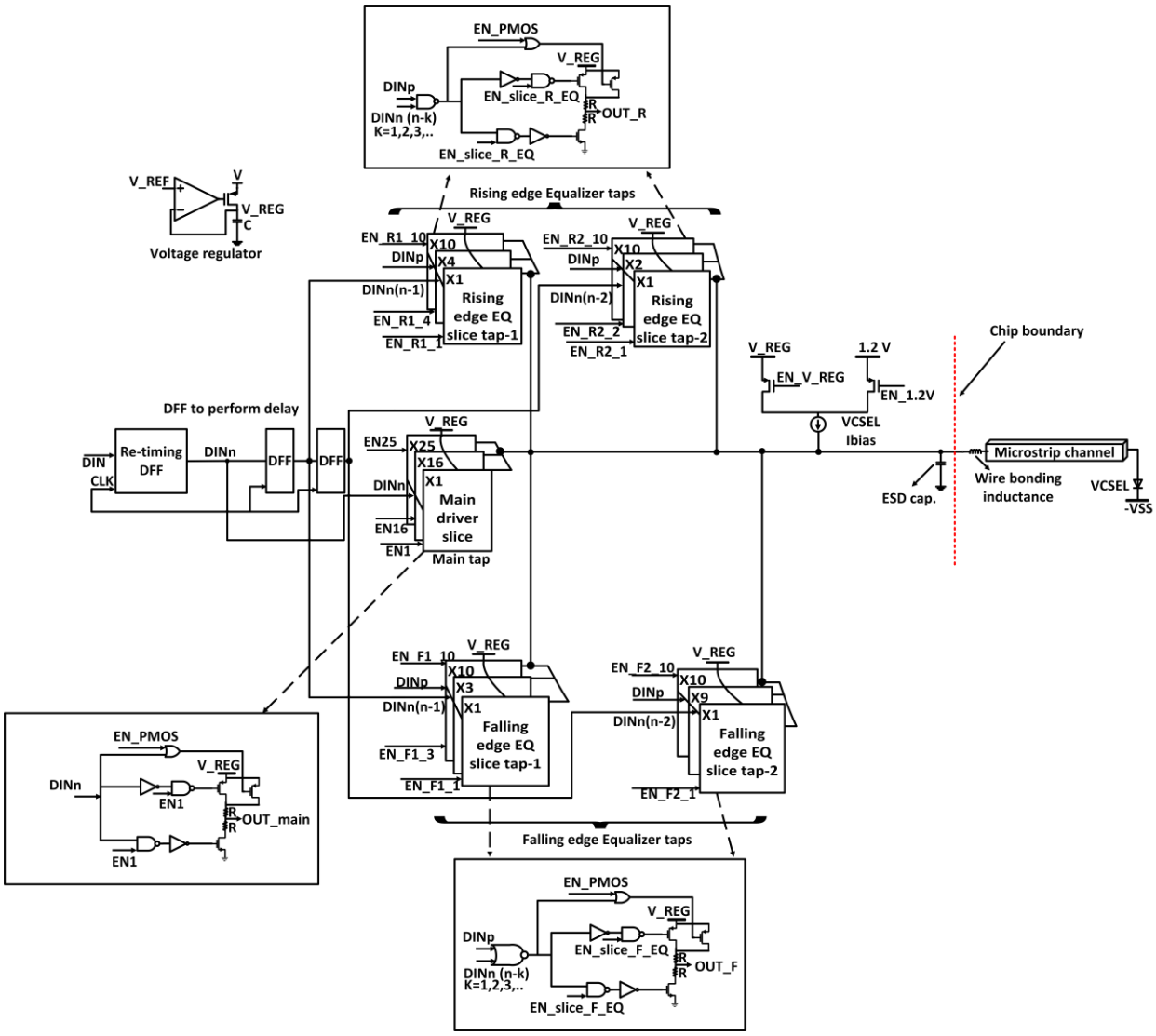
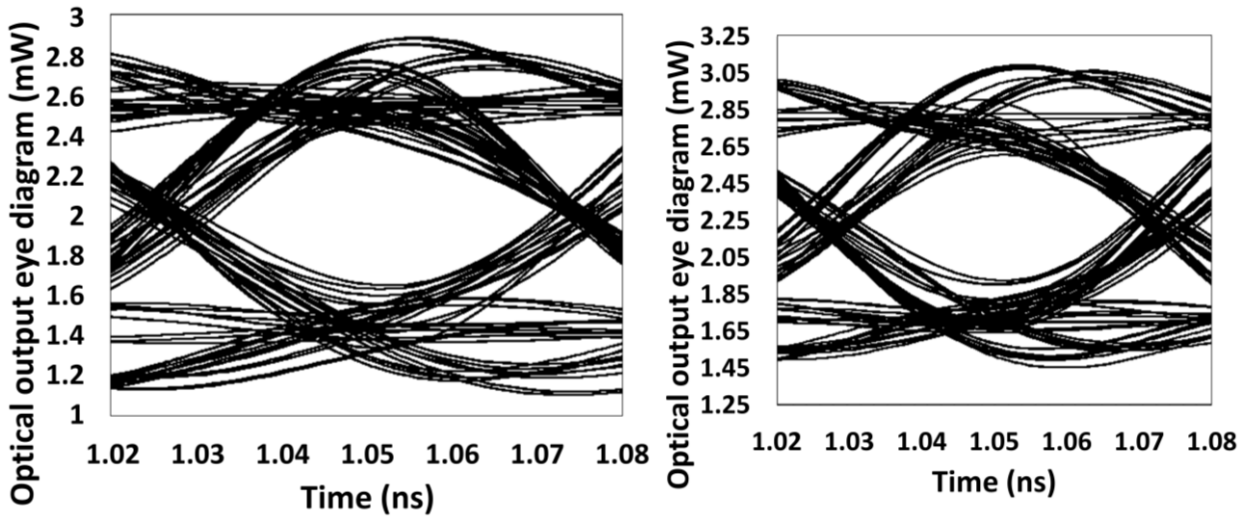


Fig. 4.33 The entire system after applying the two modifications.



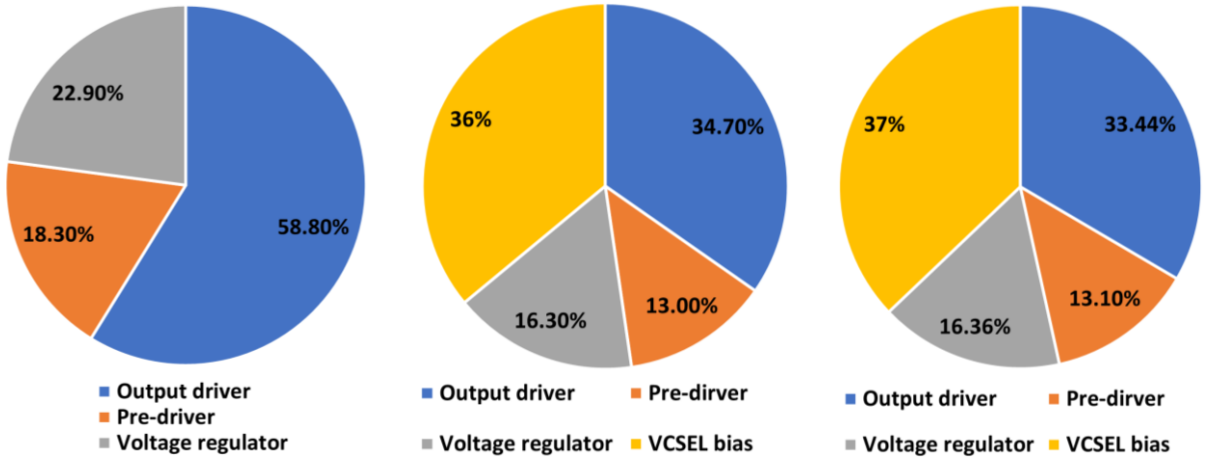
(a) (b)

Fig. 4.34 The output eye diagram of the VCSEL diode at a supply voltage of 0.7 V, and (b) at a supply voltage of 0.6 V.

4.6 Power breakdown for each mode

In this section, the power breakdown for each mode of operation is discussed. As the proposed system can work on different supply voltages, the worst-case scenario (highest supply voltage) in the power consumption is mentioned in each mode of operation. The maximum power consumption happens at the highest supply voltage. Accordingly, the power consumption is studied for all modes of operation when the system is biased at 1.2 V supply. The percentage of the power consumption of each sub-circuit for each mode is shown in Fig. 4.35.

In the first mode, it is found that the maximum power consumption is 19.66 mW which provides an energy efficiency of 0.98 pJ/bit (see Table 4.8). This energy efficiency is reasonably better than many other designs presented in the literature [7,9]. It should be stated that when reducing the supply voltage to 0.9 V, the power consumption is reduced by almost 27.2%.



(a) (b) (c)

Fig. 4.35 The power breakdown in each mode of operation: (a) electrical link driver mode of operation, (b) VCSEL driver through an electrical link mode of operation, and (c) drive a VCSEL diode directly at 1.2 V as a supply voltage.

Table 4.8 The maximum power consumption in the first mode (electrical link driver mode of operation).

Sub-circuit	**Power consumption (mW)**
Output driver (35 slice)	11.56
Pre-driver (edge detectors, enable logic…)	3.6
Voltage regulator	4.5
VCSEL bias	0 (disabled)
Total	19.66

In mode II (50 Ω driver), the maximum power consumption is 27.57 mW (see Table 4.9), which indicates an energy efficiency of 1.38 pJ/bit. This increase in the power consumption compared to mode I is due to the VCSEL bias current circuit, which is not enabled in mode I. This energy efficiency is almost 9.2% lower than the energy efficiency obtained in a previously published work [3] where the same logic (i.e., VML) was used. When reducing the supply voltage to 0.6 V, the total power consumption is reduced by 5.17 mW as shown in Table 4.10. Accordingly, there is

almost 18.75% power saving compared to the case when using a supply voltage of 1.2 V. However, the OMA is reduced by 49.6 % (i.e., from 1.35 mW to 0.68 mW).

Table 4.9 The maximum power consumption in mode II (VCSEL driver through an electrical link mode of operation).

Sub-circuit	**Power consumption (mW)**
Output driver (24 slice)	9.57
Pre-driver (edge detectors, enable logic…)	3.6
Voltage regulator	4.5
VCSEL bias	9.9
Total	27.57

Table 4.10 The power consumption in mode II when the supply voltage is 0.6 V (VCSEL driver through an electrical link mode of operation).

Sub-circuit	**Power consumption (mW)**
Output driver (24 slice)	2.45
Pre-driver (edge detectors, enable logic…)	3.6
Voltage regulator	4.6
VCSEL bias	11.7
Total	22.4

However, when the mode II driver has 85 Ω output impedance, the total power consumption reduced to be 24 mW. This is due to the reduction in the number of slices used in this case. Table 4.11 shows the power breakdown when using the 85 Ω driver.

Table 4.11 The power consumption in mode II when the supply voltage is 1.2 V, and the driver output impedance is 85 Ω (VCSEL driver through an electrical link mode of operation).

Sub-circuit	**Power consumption (mW)**
Output driver (14 slice)	4.9
Pre-driver (edge detectors, enable logic…)	3.6
Voltage regulator	4.6
VCSEL bias	11
Total	24

In terms of mode III, as shown in Table 4.12, the maximum total power consumption in the proposed design is 27.5 mW which represents 1.375 pJ/bit. This energy efficiency is almost 9.5% lower than the energy efficiency obtained in a previously published work [3]. However, it is higher than the energy efficiency obtained in [4] (i.e., 0.65 pJ/bit), but in [4], the studied power consumption was only based on the output driver.

Table 4.12 The maximum power consumption in mode III (Directly drive a VCSEL diode).

Sub-circuit	**Power consumption (mW)**
Output driver (23 slice)	9.2
Pre-driver (edge detectors, enable logic…)	3.6
Voltage regulator	4.5
VCSEL bias	10.2
Total	27.5

4.7 Comparison between the Proposed design and the state-of-art

In this section, a comparison between the proposed design and some of the previously published works is provided. Table 4.13 offers a performance comparison between the proposed design as an electrical link driver (mode I) and some published designs in the literature.

Table 4.13 A Comparison between the proposed electrical link driver (mode I) and some previously published works.

Ref.	**Output swing (mV)**	**Technology**	**Data rate (Gb/s)**	**Channel loss (dB)**	**V_{DD} (V)**	**Power consumption (pJ/b)**
[7]	220	CMOS 65 nm	1.28	13.3	-	5.3
[13]	250	CMOS 65 nm	20	12.0	1	1.53
[8]	700	28 nm STM FD-SOI CMOS	20	12.9	1	0.3
[15]	400	CMOS 90nm	5	6.0	1.2	0.94
The proposed design	279, 305, 342	CMOS 65 nm	20	16.0	0.9, 1, 1.2	0.98

From Table 4.13, it is found that the proposed driver offers lower energy efficiency compared to some previously published works [7,13] by at least 56%. In addition, the peak-to-peak output swing in the proposed design is relatively higher compared to some designs in the literature [7,13], given that the losses introduced by the used electrical link is the highest among losses in these published works.

Table 4.14 summarizes the performance of the proposed design as a VCSEL driver through an electrical link (mode II), and as a VCSEL diode driver (mode III). Also, Table 4.14 offers a comparison between the proposed design and some previously published works [1-4, 16, 18]. From Table 4.14, the energy efficiency of the proposed design in mode II and mode III is the lowest among the designs provided in [1,3,4,16,18] by at least 10%. In addition, the obtained OMA in mode II and mode III are relatively higher compared to the designs in [1,4,18,16].

Table 4.14 A performance comparison for the proposed design (mode II and mode III) versus other designs in the literature.

	The proposed design (Mode II)	**The proposed design (Mode III)**	**[4]**	**[3]**	**[18]**	**[1]**	**[16]**
Data rate (Gb/s)	20	20	35	16	26	50	45
Modulation current (mA)	3.5~1.2	4.5~3.5	1.5	7	8	8.5	7
OMA (dBm)	1.3~-1.5	3.88~1.88	0	2.1	0.82	0.7	1.2
Energy efficiency (pJ/b)	1.38	1.375	-	1.52	1.8	3.6	1.81
Technology	CMOS 65nm					SiGe 130nm	CMOS 14nm FinFET
Supply voltage (V)	1.2~0.6/ -1.13~-1.28	1.2~0.9/ -1.21~-1.32	3.0	1.05/2.75	1.0/3.0	2.5/3.3	2.0
Equalization technique	Asym. *	Asym. *	-	Asym.	Sym.**	Asym.	Sym.
Driver type	VML				CML		

* Asymmetric
** Symmetric

4.8 Summary and discussion

The proposed design can work in three modes of operation: a) electrical link driver, b) VCSEL driver through an electrical link, and c) VCSEL driver with wire bonded VCSEL. Table 4.15 summarizes the number of the enabled slices in each mode of operation. In the electrical link driver mode (mode I), the proposed design provides an output swing of 342 mV (i.e., 0.8 V_{P-P} as a channel input) at supply voltage of 1.2 V, and output swing of 279 mV (i.e., 0.484 V_{P-P} as a channel input) at supply voltage of 0.9 V.

When driving a VCSEL diode through an electrical link (mode II), the proposed design achieves a maximum peak-to-peak modulation current of 3.5 mA and a minimum peak-to-peak modulation current of 1.5 mA at supply voltages of 1.2 V and 0.6 V, respectively. These modulation currents provide an OMA range varied between 1.3 dBm to -1.67 dBm.

When removing the electrical link and driving the VCSEL directly (mode III), the proposed design provides a maximum peak-to-peak modulation current of 4.5 mA and a minimum peak-to-peak modulation current of 3.5 mA at supply voltages of 1.2 V and 0.9 V, respectively. These modulation currents provide a maximum OMA of 3.8 dBm, and a minimum OMA of 1.88 dBm.

Table 4.15 A summary of the enabled slices in each mode of operation.

	Electrical link driver	**VCSEL driver through 50 Ω electrical link**	**VCSEL driver through 85 Ω electrical link**	**VCSEL driver**
Main tap	21	12	7	16
Rising edge Tap-1	7	4	3	4
Rising edge Tap-2	-	2	1	-
Falling edge Tap-1	7	5	2	3
Falling edge Tap-2	-	1	1	-

When using supply voltage of 1.2 V, it is found that the OMA (3.8 dBm or 2.4 mW) in mode III is higher than the value obtained in mode II (1.3 dBm or 1.35 mW) Although the OMA in mode II is reduced by almost 43% compared to mode II under same conditions of biasing current (i.e., 2 mA)

and supply voltage, there is ringing noticed in the output eye diagram in mode III. This ringing is not existing in mode II (see Fig. 4.36(b)).

Also, it is observed that the signal levels for the constant "1" and "0" in Fig. 4.36(a) and Fig. 4.36(b) are different. This difference happens as the modulation current is not equal in both cases.

Same modulation current (3.5 mA) is achieved for both mode II and mode III when biasing at 1.2 V and 0.9 V, respectively. As shown in Fig. 4.37, at this same modulation current, it is found that mode II provides an OMA of 1.3 dBm and mode III provides an OMA of 1.88. These two values of OMA are supposed to be relatively close to each other. However, the effect of the ISI of the electrical channel reduces the OMA in mode II. Furthermore, it is observed that the ISI of the channel helps reducing the ringing in the optical output power when comparing Fig. 4.37(a) and Fig. 4.37(b).

To achieve same OMA for mode II and mode III (i.e., almost 1.3 dBm) as an output from the VCSEL diode, mode II should be biased at supply voltage of 1.2 V, while mode III should be biased at 0.8 V. Biasing mode III at 0.8 V saves power of almost 6.78% compared to biasing mode II at 1.2 V, see Table 4.16.

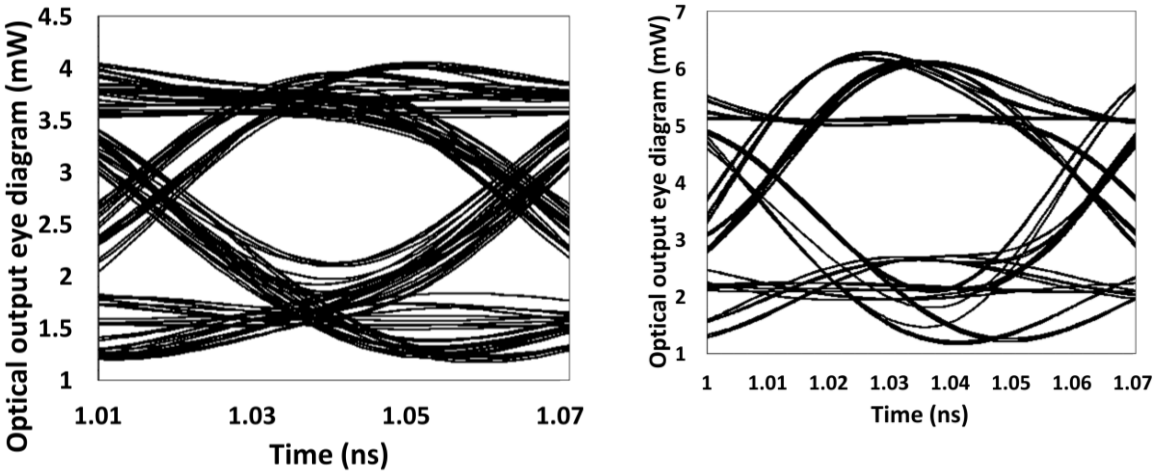


Fig. 4.36 VCSEL output eye diagrams at the same supply voltage of 1.2 V supply: (a) when using an electrical channel, and (b) without an electrical channel.

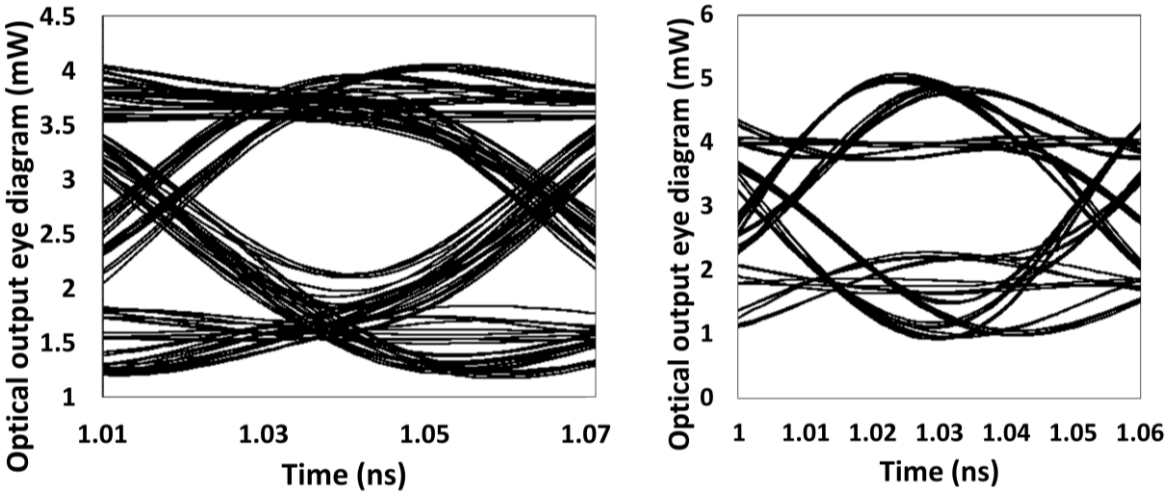


Fig. 4.37 VCSEL output eye diagrams when same modulation current injected to the VCSEL diode: (a) when using electrical channel at 1.2 V supply, and (b) with no electrical channel at 0.9 V supply.

Table 4.16 The power consumption for mode II and mode III when providing same OMA.

Sub-circuit	**Power consumption**	
	Mode II at 1.2 V	**Mode III at 0.8 V**
Output driver	9.57	4.2
Pre-driver	3.6	3.6
Voltage regulator	4.5	4.5
VCSEL bias	9.9	13.4
Total	27.57	25.7

It should be stated that the conventional VCSEL driver system consumes a total power of almost 3.33 pJ/bit. This power consumption represents two elements, 1.53 pJ/bit for the electrical link driver [13] and 1.8 pJ/bit [18] for the laser diode driver. The proposed design when working in mode II consumes about 1.38 pJ/bit when using 1.2 V as supply voltage (i.e., offering lower power

consumption by almost 58.6% compared to the conventional design). It also provides OMA of 1.3 dBm which is larger than the OMA obtained t in [18] as discussed earlier in Table 4.14. Also, the proposed design provides lowest power consumption when working in mode II compared to some previous designs in the literature [1-4,16,18].

Chapter 5 Conclusions and future work

5.1 Conclusions

This dissertation presents the research outcomes for the proposed design. The proposed design is a 20 Gb/s single-ended SST VML driver which can work in three modes of operations. The first mode uses symmetric pre-emphasis feedforward equalization to drive a 5 cm microstrip line which introduces a total loss of 16 dB at a Nyquist rate of 10 GHz. The second mode drives a VCSEL diode through an electrical link, exploiting asymmetric equalization. The third mode is a VCSEL driver with a wire bonded VCSEL diode that uses asymmetric equalization, compensating the nonlinear behavior of the VCSEL. The proposed design provides a matched output impedance to reduce the reflections of the signal through the electrical link. In addition, the proposed design provides a tunable output current swing without affecting the output impedance of the driver. This tunable swing is implemented through changing the supply voltage via a voltage regulator circuit. This tunable swing reduces the power consumption by almost 19% in the second mode of operation when working at a bias voltage of 0.6 V. It also reduces the power consumption by almost 27% in the first mode of operation when working at a bias voltage of 0.9 V. Furthermore, the proposed driver facilitates toggling between symmetric and asymmetric equalization, if needed. The proposed design reduces the overall power consumption of the transmitter by almost 58.6% compared to the conventional systems. This is due to eliminating the stand-alone LDD in the modified system. The highest power consumed in the driver occurs when working at mode II (i.e., drives a VCSEL diode through an electrical link), and it consumes a power of 27.57 mW, which leads to energy of efficiency of 1.38 pJ/bit (in this case the OMA is 1.3 dBm).

It is found that mode II of the proposed design provides lower OMA by almost 0.8 dBm compared to the design proposed in [3]. However, the energy efficiency in mode II is lower by almost 0.14 pJ/bit. the mentioned reduction in the OMA is attributed to the usage of the electrical link, introducing ISI. When excluding the electrical link from the currently proposed design (switching

from mode II to mode III), the proposed system provides a higher OMA by 1.7 dBm compared to [3], with achieving almost same power consumption obtained in mode II.

It is found that the mode I provides higher peak-to-peak voltage by almost 92 mV compared to the VML electrical link driver proposed in [13]. However, the proposed design in [13] has lower total energy efficiency by almost 0.08 pJ/b. When biasing the proposed design in mode I with lower supply voltage (i.e., 0.9 V), the output peak-to-peak voltage is still higher by almost 29 mV compared to the system presented in [13], and the proposed design provides lower energy efficiency by almost 0.185 pJ/bit.

It should be stated that developing such driver which offers high-speed and low-power characteristics can enhance the overall performance of many systems (i.e., large computer systems, internet access, and telecom networks) in data transmission.

5.2 Future work

The current work can be extended in the future in different directions, for example:

- Increase the data rate by using PAM-4 as a modulation format instead of NRZ:

  PAM-4 is a modulation format where each signal level can represent two logic bits (i.e., 00,10,01, and 11), offering four signal levels instead of two. This technique achieves two times the data rate offered by NRZ without increasing the bandwidth. PAM-4 is more sensitive to VCSEL nonlinearities (i.e., four current levels in each signal level). Also, PAM-4 is more sensitive to ISI, due to the reduction in the eye opening. To overcome these issues, the number of FFE taps should be increased to compensate for the VCSEL nonlinearities and ISI.

- Implement a cascode current mirror to act as a DC bias current for the VCSEL instead of using the basic current mirror.

  The method of cascading increases the output impedance of the current mirror such that the output resistance of the current mirror does not significantly affect the total output impedance of the driver. Accordingly, the total output impedance of the driver is not affected by the voltage dependent impedances.

- Fabricate and test the proposed design.

The proposed design should be fabricated in TSMC 65 nm CMOS technology which accommodates higher data rate and lower parasitic capacitances. After fabrication, the chip should be tested to validate the simulation results. The metals used to connect between the components in the fabricated chip lead to extra parasitic capacitances and resistances. These parasitics reduce the output peak-to-peak voltage, the output OMA, and the data rate.

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