A Single-Event Transient Tolerant Optical Receiver

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This is to certify that the thesis prepared

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Abstract

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Sami Sattar

Fiber optical communication systems have attained significant importance in space applications e.g. Satellites, Space stations, etc. The systems have remarkably lightweight characteristics, less frequency dependent loss, and provide high-speed data transmission in a power-efficient way. Satellites and space stations are exposed to a higher level of radiation due to energetic particles in space. Fiber optical links mainly consist of integrated semiconductor devices. When integrated circuits are exposed to radiation such as in space applications, they are influenced by high-energy ionizing particles. This radiation causes malfunctioning of electronic devices and reduces their life span. It also generates transmission errors which are classified as single-event transients (SETs), single event upsets, and single event latch-up, and also causes total ionization dose effects. This thesis proposes a radiation tolerant (SET tolerant) optical receiver using triple modular redundancy (TMR) in which a conventional receiver is split into three identical sub-receivers in parallel. Majority voting is performed at the outputs after the received analog signal has been thresholded.

To investigate the effectiveness of the proposed design, a conventional optical receiver is taken as a reference design, and its performance is compared with the proposed TMR-based radiation tolerant optical receiver. The proposed receiver uses an impedance scaling technique so that its overall power dissipation, gain, and bandwidth are the same as the reference design while providing SET tolerance. The proposed receiver removes SET errors with the limitation that only one sub-receiver experiences a SET in a given unit interval. By applying the impedance scaling technique, the proposed receiver is robust to SET errors with no increase in overall power dissipation but at the sensitivity cost of 0.8 dB.

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I am deeply indebted to many people for my success. I always feel speechless when it comes to the commitments my family made for me. My heartiest gratitude to my parents, bothers and my wife for their moral support and heartiest prayers to make me a successful person. It is an honor to acknowledge my most respectable grandparents and my uncle Saeed Zafar who always helped me morally and financially throughout my study career.

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List of Acronyms

MMF	Multimode fiber
CMU	Clock multiplication unit
Mux	Multiplexer
PAM	Pulse amplitude modulation
PD	Photodiode
TIA	Transimpedance amplifier
PA	Post amplifier
CDR	Clock and data recovery
Dmux	Demultiplexer
SET	Single event transient
TMR	Triple modular redundancy
DRC	Design rule check
LVS	Layout versus schematic
BER	Bit error rate
ISI	Inter symbol interference
VEO	Vertical eye-opening
PSD	Power spectral density
NTF	Noise transfer function
GBW	Gain-bandwidth product
LET	Linear energy transfer
SEU	Single event upset
SEL	Single event latch-up
TID	Total ionizing dose
SOI	Silicon on insulator
LVDS	Low voltage differential signal
AGC	Automatic gain control
LPF	Low pass filter
RMS	Root mean square
UI	Unit interval
SNR	Signal-to-noise ratio
OC	Offset compensation
TFIT	Transistor level failure in time

Chapter 1

Introduction

The continuous increase in data transfer rates between servers within data centers demands high-speed short-reach links. Electrical interconnect is unable to address this need in a cost and power-efficient way. As the distance goes up to a few 10's of a centimeter, frequency-dependent losses of copper wiring in electrical links become larger. Therefore, due to the negligible channel loss and robustness to electromagnetic interference, fiber optic interconnects have replaced electrical interconnects. Optical links are widely used to communicate data between servers within data centers for distances up to 300 m with multi-mode fiber (MMF).

With ultra-high bandwidth, low channel losses, ultra-low latencies, and low weight make fiber optical links the choice of satellite designers for intra-satellite communication. Analog circuits such as optical transceivers sent in space are bombarded by ionizing radiation due to solar flares and cosmic rays, including high-energy protons from the sun. Radiation-induced transient currents severely degrade the sensitivity of integrated circuits and cause malfunctioning of electronic components. So, the next challenging task is to design a highly reliable optical link that tolerates the harsh radiation environment of space.

1.1 Optical Communication Systems

Fig. 1.1 presents a block diagram of a conventional optical communication system [1]. It has two parts: a transmitter and a receiver. At the transmitter side, several low-speed parallel digital

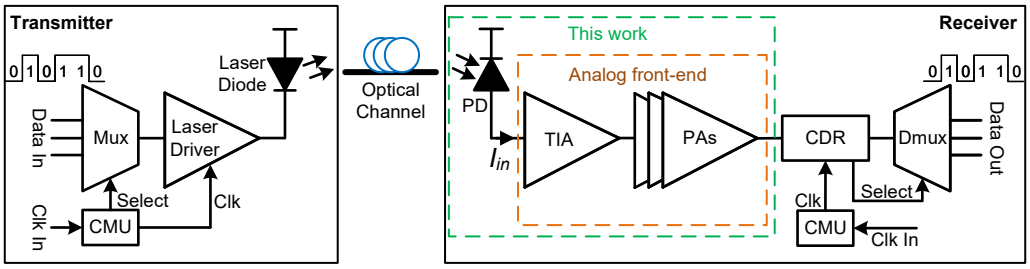


Figure 1.1: Optical Communication System

data inputs (Data In) are multiplexed into a high-speed serial data stream which is fed into the laser diode driver. A clock multiplication unit (CMU) generates a bit rate clock from the parallel data clock which is used to control the multiplexer (Mux). A laser driver modulates the current of the laser diode. At a high data rate, the laser driver may use the clock signal (Clk) to retime the data. Light emitted by the laser diode is transmitted to the receiver through an optical channel. The data is transmitted in a binary format. A binary "1" is transmitted when the signal has higher optical power for the entire bit period and the binary "0" is transmitted when the signal has lower optical power for the entire bit period. This format of data transmission is known as two-level pulse amplitude modulation (PAM2). On the receiver side, a photodiode (PD) converts the optical light into a current signal (I_{in}). This current signal is then further converted into a voltage signal with some amplification through a transimpedance amplifier (TIA). Due to the small input current and gain-bandwidth trade-off of the TIA, further amplification through post-amplifiers (PAs) is usually required. The PAs form a chain of gain stages to amplify the output voltage of the TIA. The combination of TIA and PAs is called receiver front-end. The output of the PA is supplied to the clock and data recovery unit (CDR) which synchronizes a clock to the incoming data and CDR uses the recovered clock to regenerate the data. CDR also provides the control signal (Select) to a demultiplexer (DMux). Finally, Dmux generates the low-speed parallel data stream (Data Out) from the high-speed serial data.

1.2 Radiation Effects on Integrated Circuits in Space

An optical receiver used in space applications encounters an interaction with high energetic ionizing particles. On interaction, the radiation particles transfer their energy to the target material. The strike of radiation particles on the electronic components (e.g transistors) disturb their functionality and also lead to device operation failure. Therefore, it has significant importance to evaluate the risks associated with electronic components in radiation exposure.

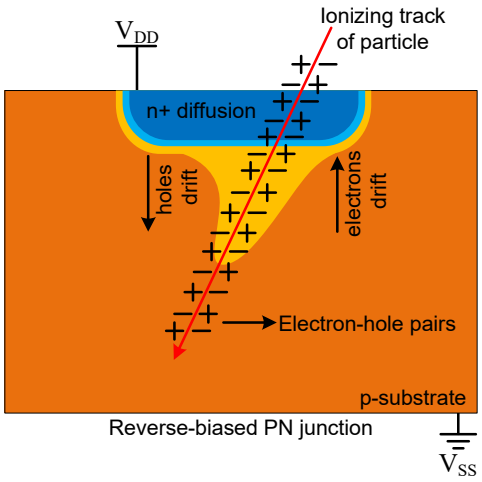


Figure 1.2: SET mechanism in NMOS transistor

In modern CMOS integrated circuits, the PN junctions are most sensitive regions to ionizing radiations. A high-energy particle deposits a temporary trail of charges (electron-hole pairs) through the target device along its path before stopping as depicted in Fig. 1.2. The collected charges drift and diffuse across the reversed biased PN-junction, resulting in a transient current [2] [3] [4]. Electrons are collected by the n+ diffusion and the holes are collected by the p- substrate, thus the induced current flow appears to be traveling out of the diffusion region towards VSS. As a consequence of this current flow, the voltage spike is produced across the circuit's struck node. This phenomenon is called a single event transient (SET) and it causes nondestructive functional errors (soft errors). This SET in the signal can flip the logical levels from 0 to 1 or 1 to 0, therefore it is important to study its effect on optical receivers that need radiation hardening (radiation hardening refers to electronic components designed to be less susceptible to radiation damage). The rest of the thesis is focused on the mitigation of radiation-induced SET in the optical receiver's front end.

1.3 Thesis Objectives

- ◇ The main objective of this thesis is to design an optical receiver that minimizes radiation-induced single-event transient errors.
- ◇ The proposed optical receiver must exhibit the performance in gain, bandwidth, and sensitivity, and an overall power dissipation comparable to the conventional optical receiver (reference design) while mitigating SET.
- ◇ To accomplish the layout of the proposed optical receiver.

1.4 Thesis Contribution

This work presents the new single-event transient tolerant optical receiver. The main contributions of this thesis are:

- ◇ Design and implementation of the proposed single event transient (SET) tolerant optical receiver using triple modular redundancy (TMR) in 65 nm CMOS technology.
- ◇ An overall power dissipation, gain, and bandwidth similar to the conventional design is achieved by the impedance scaling technique.
- ◇ Completed a DRC and LVS clean tape-out of the proposed SET tolerant optical receiver and submitted the chip for fabrication.

The proposed receiver has been submitted at IEEE International Symposium on Circuits and Systems (ISCAS), 2022. The tile of the paper is:

- ◇ Sami Sattar, Glenn Cowan, "Single-Event Transient Tolerant Optical Receiver Using Triple Modular Redundancy" $\{\mathrm{Accepted}\}$

1.5 Thesis Organization

The thesis is organized into five chapters. Chapter 1 is an introductory chapter. Chapter 2 discusses the general terms related to wireline communication systems, background related to radiation

effects on electronic components, and also the electrical models for single event transient simulations. Furthermore, an impedance scaling technique used in the proposed design is also explained. Chapter 3 demonstrates the complete circuit design procedure of a single event transient tolerant optical receiver. Chapter 4 presents the circuit simulation results and the chip tape-out. Finally, the conclusions and future work directions are provided in Chapter 5.

Chapter 2

Literature Review

2.1 Overview of the Optical Receiver

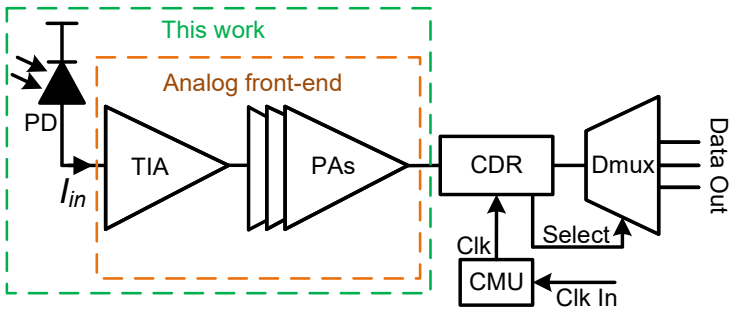


Figure 2.1: Symbolic diagram of the optical receiver

Fig. 2.1 shows the block diagram of the optical receiver. It consists of a photodiode (PD), transimpedance amplifier (TIA), post-amplifiers (PAs), clock and data recovery circuit (CDR), clock multiplication unit (CMU), and demultiplexer (DMUX). A photodiode converts the received light into a current signal (I_{in}). The transimpedance amplifier converts this current signal into a voltage signal with some amplification. However, the amplitude of the signal produced by the transimpedance amplifier is not high enough to be utilized by the clock and data recovery unit for further processing. Therefore, the output signal of the transimpedance amplifier is further amplified through post-amplifiers. The clock and data recovery circuit obtain the clock and data from the received signal once the amplitude level decision has been executed. Finally, parallel data stream

is produced by the demultiplexer. The clock signal to the CDR circuit is provided by the clock multiplication unit. The focus of this study involves PD and the combination of TIA and PAs which is also known as "receiver front-end". Table 2.1 tabulates the functionality of optical receiver circuit blocks.

Table 2.1: RECEIVER CIRCUIT BLOCKS AND THEIR FUNCTIONS

Circuit blocks	**Functions**
Photodiode	Converts the received light into current
Transimpedance Amplifier	Converts the current signal into voltage signal
Post-amplifiers	Amplifies the output voltage of TIA which helps in the process of decision making at the proceeding stage
Clock and Data Recovery	Recovers the clock and the data from the incoming serial data
Demultiplexer	Produce the original data in parallel data stream

2.2 Performance Specifications and Design Considerations of Front-end

The following design trade-offs might be considered by the designers while designing an optical receiver.

2.2.1 Sensitivity and Bit Error Rate

The receiver's sensitivity is one of the most widely used specifications of optical receivers in fiber-optic systems. It is defined as the minimum input signal's optical power required by the receiver to achieve the desired BER (A BER of 10^{-12} is frequently targeted). BER is the ratio of the number of errors received to the total number of bits. Since the input of TIA is a very small current, the input-referred noise of the TIA should be very low so that it can have a high sensitivity to sense the input current. For a receiver design, the ratio of the peak to peak current (Iin_{pp}) of a noiseless input and the input-referred noise current (In_{in}) should be at least 14 to get a BER of 10^{-12}, given by

$$\frac{Iin_{pp}}{In_{in}} = 14 \tag{1}$$

2.2.2 Bandwidth

The bandwidth of a TIA is typically in the range of 50 % - 70 % of the data rate. The bandwidth greater than this range causes an increase in input-referred noise and BER of the receiver. On the other hand, if the bandwidth is chosen less than this range then the receiver may suffer from inter-symbol interference in its output signal. For example, for an optical receiver to be employed in a 10 Gb/s system we need to have at least 5 - 7 GHz of bandwidth.

2.2.3 Inter-symbol Interference

Intersymbol interference (ISI) is caused by non-ideal channels that are not distortionless over the entire signal bandwidth. ISI occurs when a pulse spreads out in such a way that it interferes with adjacent at the sampling instant. When the bandwidth of the receiver is not enough or less than 70 % of the data rate, ISI occurs [5]. It reduces the output voltage swing and causes closure of vertical eye-opening as depicted in Fig. 2.2 (c).

2.2.4 Eye Diagram

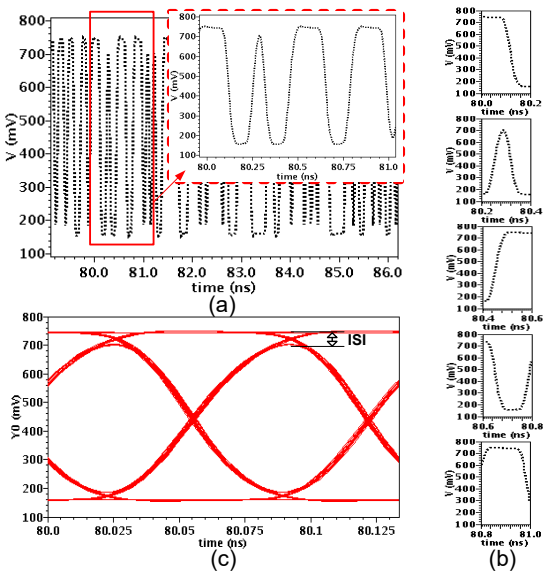


Figure 2.2: (a) Random bit sequence at 10 Gb/s, (b) slices of the data at every two unit intervals (2UI = 200 ps) to create an eye-diagram, (c) Eye diagram corresponding to the slicing interval over two unit intervals

An eye diagram folds the given bit sequence into small unit intervals. It carries a lot of information about the quality of the incoming signal and the state of the channel which is useful for the detection of the digital input. It is significantly used for visual examination of the severity of the ISI and accuracy of timing extraction of a received signal. Fig. 2.2 (c) shows the practical example of an eye diagram. It is plotted from the random bit sequence given in Fig. 2.2 (a) which is sliced for every two unit intervals as few slices are shown in Fig. 2.2 (b).

2.2.5 Gain

The gain of a TIA cannot be very high or very low. In literature, the gain for recent TIAs of between 40 – 60 dBΩ has been reported [6]. Since an input of the TIA is very small (ranges between tens of micro-ampere) and it must satisfy the input sensitivity of the post-amplifier, the TIA should exhibit at least a few mili-volts at its output. It is important to note that too-high gain may affect the circuit bandwidth which prevents the high-speed operation while the too-low gain may degrade the overall noise performance of the receiver. In this study, transimpedance gain (Z_T) is defined as the ratio of maximum output vertical eye-opening to an overall input current (I_{in}), given by

$$Z_T = \frac{VEO}{I_{in}} \tag{2}$$

From Fig. 2.1, an eye diagram is plotted at the output of PAs (two post amplifiers are taken in this

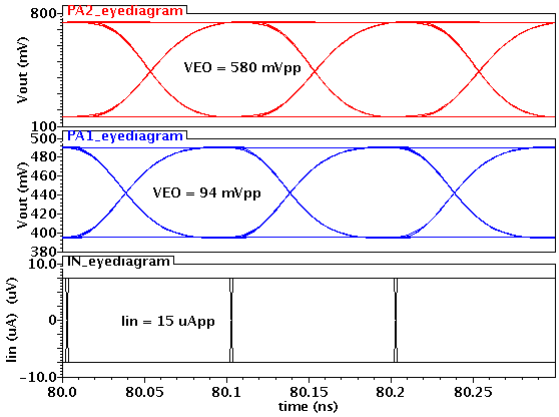


Figure 2.3: Eye diagram of input current and at the output of post amplifiers for the circuit shown in Fig. 2.1

example) along with the input current. The eye diagram at the output of the first PA has a VEO of 94 mV_{pp} which gives the gain of 6.2 kΩ while at the output of the second PA has VEO of 580 mV_{pp} which gives the gain of 38.6 kΩ with an input current of 15 μA_{pp} as depicted in Fig. 2.3.

2.3 Optical Receiver Front end

The symbolic view of an optical receiver front-end is presented in Fig. 2.4. Here TIA converts the input current to the output voltage signal which is then further amplified by the PAs. The analog output is taken through the buffer and the low pass filter gives the average of the output voltage V_{out}.

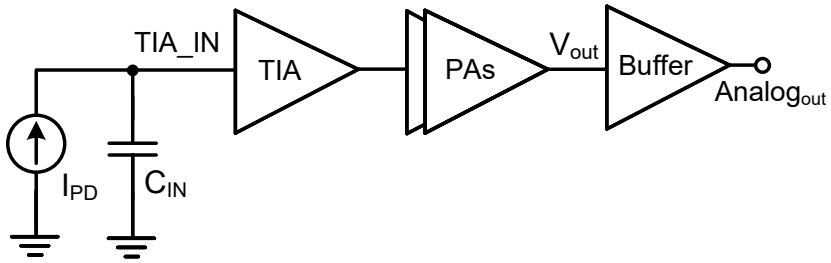


Figure 2.4: Complete symbolic diagram of the front-end

2.3.1 Transimpedance Amplifier (TIA)

Being the first circuit block in an optical receiver front-end, the TIA plays a significant role in the design trade-off among gain, bandwidth, noise, and overall power dissipation of the receiver. The bandwidth of TIA can be limited by the large input capacitance (parasitic capacitance of photodiode, bond pad, transistors) and the input impedance. Because there exists a trade-off between ISI and sensitivity, the bandwidth of the front-end is selected around 50 % - 70 % of the data rate [1], [7]. Furthermore, TIA receives a very small input current, and therefore it should have a high gain enough to produce an acceptable voltage level for the post-amplifier. Moreover, to achieve a high signal-to-noise ratio, the input-referred noise of TIA must be low. A high-performance TIA topology needs to have a low input impedance, high current-to-voltage gain, and a small input-referred current noise.

Inverter-based shunt-feedback TIA

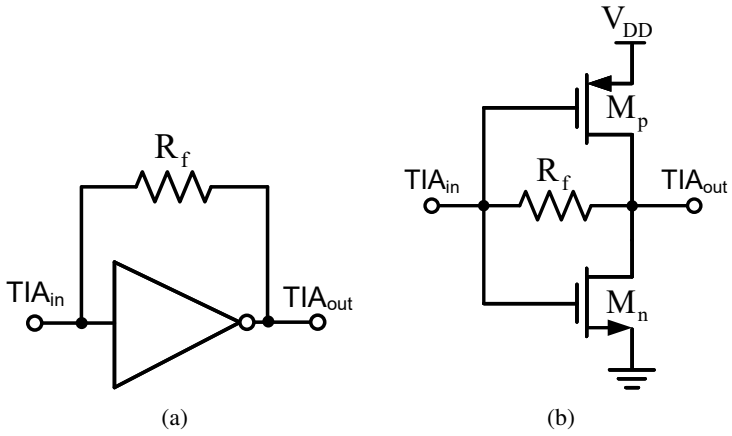


Figure 2.5: Inverter-based shunt-feedback TIA (a) Top view (b) Transistor level schematic view

Fig. 2.5 shows a well-accepted TIA topology called inverter-based shunt-feedback TIA. In this TIA, both NMOS and PMOS transistors are connected in a push-pull structure to provide larger overall transconductance resulting in a higher gain with the same amount of power dissipation and bias current as compared to the common source shunt-feedback TIA [8]. This TIA has low input impedance and the feedback network (due to feedback resistance) ensures the almost constant gain over the bandwidth of interest. Furthermore, this topology also offers low input-referred noise [9]. To conclude, the shunt-feedback TIA provides a reasonable balance between all the key parameters such as relatively large gain-bandwidth product and acceptable input-referred noise. The small-signal circuit of the shunt-feedback TIA is shown in Fig. 2.6 and its low-frequency analysis is carried out below by making the following assumptions:

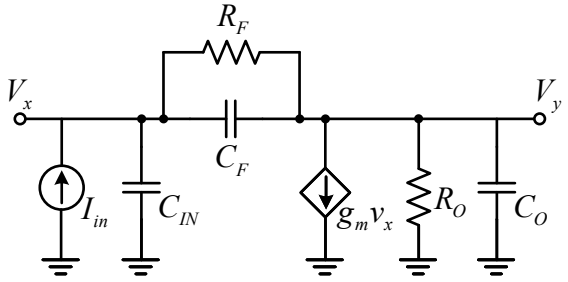


Figure 2.6: small-signal equivalent circuit of shunt-feedback TIA

◇ *output resistance* (R_O) *of NMOS and PMOS* $= 1/G_O = ro_n//ro_p$

◇ *feedback resistance* $(R_F) = 1/G_F$

◇ *input capacitance* $(C_{IN}) = C_{ESD} + C_{Pad} + C_{PD} + C_{GSN} + C_{GSP}$

◇ *output capacitance* $(C_O) = C_{Load} + C_{DBN} + C_{DBP}$

◇ *combined transconductance* (g_m) *of NMOS and PMOS* $= g_{mn} + g_{mp}$

From Fig. 2.6, applying KCL gives

$$G_F(V_x - V_y) = I_{in} \quad at\ node\ X \tag{3}$$

$$V_x(g_m - G_F) + V_y(G_O + G_F) \quad at\ node\ Y \tag{4}$$

where Eq. 3 and Eq. 4 in matrix form can be expressed as

$$\begin{bmatrix} G_F & -G_F \\ g_m - G_F & G_O + G_F \end{bmatrix} \quad \begin{bmatrix} V_x \\ V_y \end{bmatrix} = \begin{bmatrix} I_{in} \\ 0 \end{bmatrix} \tag{5}$$

Eq. 5 is solved to find the input impedance Z_{in} and transimpedance gain Z_T, given by

$$Z_{in} = \frac{V_x}{I_{in}} \approx \frac{1}{g_m} \tag{6}$$

and

$$Z_T = \frac{V_y}{I_{in}} = \frac{1 - g_m R_F}{g_m + 1/R_o} \tag{7}$$

if it is assumed that $g_m R_F$ and $g_m R_o$ are $\gg 1$, then the transimpedance gain is $\approx$ -R_F. Furthermore, using Eq. 5 and expand it to find the high frequency transfer function by including all the capacitors [10], gives

$$\begin{bmatrix} G_F + s(C_{IN} + C_F) & -G_F - sC_F \\ g_m - G_F - sC_F & G_O + G_F + s(C_O + C_F) \end{bmatrix} \quad \begin{bmatrix} V_x \\ V_y \end{bmatrix} = \begin{bmatrix} I_{in} \\ 0 \end{bmatrix} \tag{8}$$

$$Z_T = \frac{(sR_FC_F + 1 - g_mR_F)R_O}{s^2C_1R_FR_O + +s(R_FC_F(1 + g_mR_O) + C_{IN}(R_F + R_O) + R_OC_O) + g_mR_O + 1} \tag{9}$$

where $C_1 = C_{IN}C_O + C_{IN}C_F + C_FC_O$, from Eq. 9 the natural frequency and damping factor are given by

$$\omega_n^2 = \frac{g_mR_O + 1}{C_1R_FR_O} \tag{10}$$

$$\zeta = \frac{1}{2}\frac{R_FC_F(1 + g_mR_O) + C_{IN}(R_F + R_O) + R_OC_O}{\sqrt{C_1R_FR_O(g_mR_O + 1)}} \tag{11}$$

Noise analysis

The thermal noise sources due to feedback resistance R_F and transistors $M_{n/p}$ are responsible for the noise of the TIA. The noise equivalent small-signal circuit of the TIA is presented in Fig. 2.7. Here thermal noise current due to R_F and $M_{n/p}$ are represented by noise current sources $I_{n,Rf}$ and $I_{n,Mn/p}$ as shown in Fig. 2.7 (a) and (b), respectively. An overall noise contribution is the sum of the products of power spectral density (PSD) and magnitude squared noise transfer function (NTF) of the noise sources as listed in Table 2.2. In the table, *k* is the Boltzmann constant, γ is the noise factor of transistors, g_m is the combined transconductance of M_n and M_p, and T is the absolute temperature. Low-frequency noise analysis is carried out below to estimate the overall noise at the output of shunt-feedback TIA. Note that, all the capacitors are ignored and also it is assumed that $1/R_o \approx 0$ as $R_o \to \infty$. For the ease of analysis $G_F = 1/R_F$ is used.

Table 2.2: SUMMARY OF CIRCUIT COMPONENTS VALUES

Noise Sources	PSD [A^2/Hz]	NTF [Ω]	Contribution [V^2/Hz]
R_F	4 *k*T/R_F	H_{Rf}	4 *k*T/R_F $\lvert H_{Rf}\rvert^2$
M_n, M_p	4*k*Tγg_m	$H_{Mn/p}$	4*k*Tγg_m $\lvert H_{Mn/p}\rvert^2$
Total noise contribution = 4 *k*T[(1/R_F) $\lvert H_{Rf}\rvert^2$ + γg_m $\lvert H_{Mn/p}\rvert^2$]			

By applying KCL, NTF due to resistor ($H_{Rf} = \frac{V_y}{I_{n,Rf}}$) is determined as

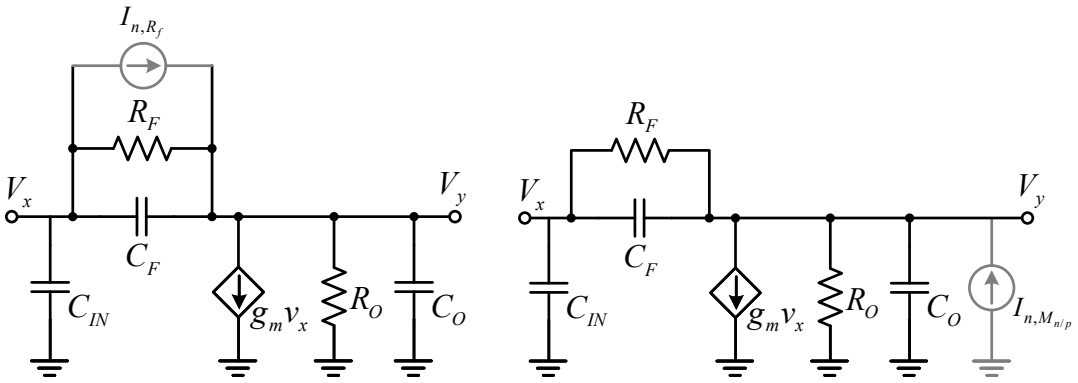


Figure 2.7: small-signal circuit of shunt-feedback TIA with thermal noise source due to (a) resistor R_F and (b) transistors $M_{n/p}$ [10]

$$\begin{bmatrix} G_F & -G_F \\ g_m - G_F & G_F \end{bmatrix} \quad \begin{bmatrix} V_x \\ V_y \end{bmatrix} = \begin{bmatrix} -I_{n,Rf} \\ I_{n,Rf} \end{bmatrix} \tag{12}$$

$$\frac{V_y}{I_{n,Rf}} = R_f \tag{13}$$

and NTF due to transistors ($H_{Mn/p} = \frac{V_y}{I_{n,Mn/p}}$) is given by

$$\begin{bmatrix} G_F & -G_F \\ g_m - G_F & G_F \end{bmatrix} \quad \begin{bmatrix} V_x \\ V_y \end{bmatrix} = \begin{bmatrix} 0 \\ I_{n,Mn/p} \end{bmatrix} \tag{14}$$

$$\frac{V_y}{I_{n,Mn/p}} = \frac{1}{g_m} \tag{15}$$

By substituting Eq. 13 and Eq. 15, yields total output noise contribution as

$$\textit{Total noise contribution} = 4kT\left(R_F + \gamma\frac{1}{g_m}\right) \quad V^2/Hz \tag{16}$$

From Eq. 16, an input referred noise current ($I_{n,rms}$) is given by

$$I_{n,rms} = \frac{4kT}{R_F}\left(1 + \frac{\gamma}{g_m.R_F}\right) \quad A^2/Hz \tag{17}$$

It can be noticed that the input-referred noise current of the shunt feedback TIA is inversely proportional to the feedback resistance and an overall transconductance.

2.3.2 Post-Amplifiers

A single stage amplifier (TIA) can not fullfill the need of high gain and the larger bandwidth because of the design trade-off between gain and bandwidth. Hence, few post-amplifier stages are mostly used after the TIA to enhance the gain of front-end. For example, if first order amplifier with a gain of A_o and bandwidth of BW_o is cascaded in n identical stages, it will provide the total gain of $A_t = A_o^n$. This shows that the product of the gain of each stage gives the total gain at the final output. On the other hand, the total bandwidth of n cascaded amplifiers is given as $BW_t = BW_o \times \sqrt{\sqrt[n]{2} - 1}$, which shows that an overall bandwidth is smaller than the bandwidth of each stage. Hence, it is convenient to find the gain-bandwidth product $GBW_o = A_o \times BW_o$ of each stage in terms of A_t and BW_t which leads to achieve the desired GBW_t of the front-end. The gain-bandwidth product of each stage is given by [1]

$$GBW_o = \sqrt[n]{A_t} \times \frac{BW_t}{\sqrt{\sqrt[n]{2} - 1}} \tag{18}$$

Therefore, the number of post-amplifier stages is limited to five in literature, beyond this number the gain-bandwidth product gets worst and it degrades the overall performance of the front-end [1].

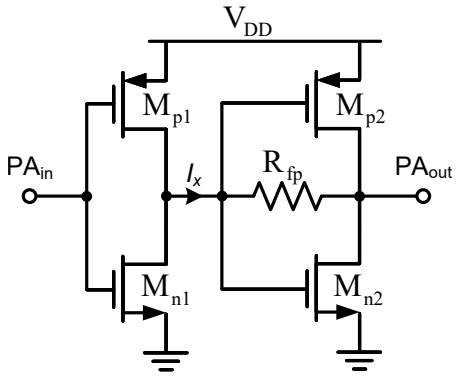


Figure 2.8: Transistor level design of Cherry-Hopper amplifier

Fig. 2.8 shows the transistor level design of a widely adopted Cherry Hooper amplifier topology.

It is made by a cascade of two inverters, where the second inverter incorporates feedback resistance R_{fp}. The first inverter converts an input voltage to the output current I_x through a transconductance (g_{mp1} + g_{mn1}) while the second inverter converts the input current I_x to the output voltage with a transimpedance gain of R_{fp}. This topology achieves similar gain with wide bandwidth as compared to common source topology which makes it a favorable choice for various data rates [11] [12] [13]. In addition, the push-pull arrangement of transistors can achieve higher gain and better input-referred noise than the common source amplifier topology [9].

2.4 Radiation Effects on Integrated Circuits

When integrated circuits are exposed to a radiation environment such as in space applications, they experience a very high concentration of ionizing radiations from particles like protons and neutrons, etc.

2.4.1 Charge Collection Mechanism due to a Particle Strike

The charge collection mechanism explains how an ionizing strike affects the drain of a transistor and the parasitic current can be deduced. When an ionizing particle hits the reverse-bias PN junction, it leaves a cloud of electron-hole pairs along its ionizing track. These electrons and holes drift and diffuse across the PN junction, resulting in a transient current. This phenomenon occurs in three stages as shown in Fig. 2.9.

At stage-1, particle strike creates a track of electron-hole pairs before stopping. Then a funnel is created in stage-2, here the electrons are collected by n+ diffusion while the holes are collected by p-substrate. As a result, a current pulse appears traveling out of the diffusion region towards ground terminal due to the drift motion of charges. Finally, charged particle diffuses in stage-3. This phenomenon of ionization generates a parasitic current depending on the polarization of the transistor. The resulting current has three components x, y, and z, here x and y show the drift current that appears during the funnel creation, and z is the current of the remaining diffusion charges. The funnel-shaped electric field enhances the efficiency of drift collection by extending the depletion region deeper into the substrate, thus rapidly collecting the carriers through the drift process.

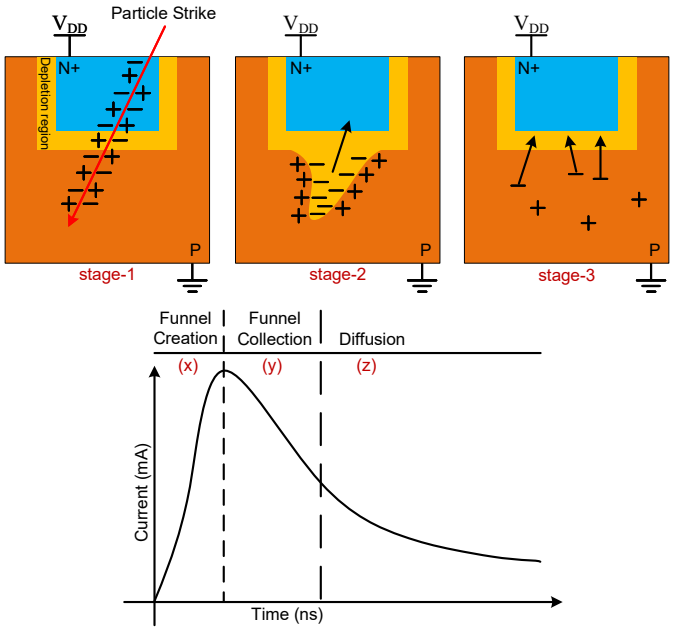


Figure 2.9: Resulting current of an ion passing through the space charge region of a PN junction. (a)Ionized track creation, (b) Funneling, (c) Diffusion of the remaining charges.

The remaining charges are collected and recombined through the diffusion process. The diffusion process is much slower than the drift process [14] [15].

2.4.2 Linear Energy Transfer

When an ionized energetic particle interacts with a material, it transfers its energy to that material. With direct ionization, a particle's ability to generate single-event charge depends how much energy it can deposit in the semiconductor as it passes through. The process of energy transfer is known as linear energy transfer (LET). LET is related to the energy, mass of the incident particles and the material struck by the particles [16]. The LET of a given particle incident on a material of density ρ is the measure of the energy loss per unit path length in the material and is given by

$$LET = \frac{dE}{dL} \times \frac{1}{\rho} \tag{19}$$

where E represents Energy with the unit MeV (The energy of ionizing radiation is measured in electronvolts (eV) but one-electron Volt is an extremely small amount of energy. Therefore, multiple

units kilo-electron Volt (keV) and mega-electron Volt (MeV) are commonly used), L is Length with the unit cm, $\frac{dE}{dL}$ is the energy loss per unit length, and ρ is the material's density with the unit mg/cm^3 [15]. LET is expressed in Mev· cm^2/mg.

Radiation causes malfunctioning of electronic devices and also reduces their life span. Radiations cause transmission errors which are classified as soft errors (single event transients, single event upsets), hard errors (single event latch-up, single event gate rupture), and also causes degradation mechanisms such as total ionizing dose [14], [17] as listed in Fig. 2.10. Such types of errors caused by the radiations are discussed below.

2.4.3 Radiation Induced Errors

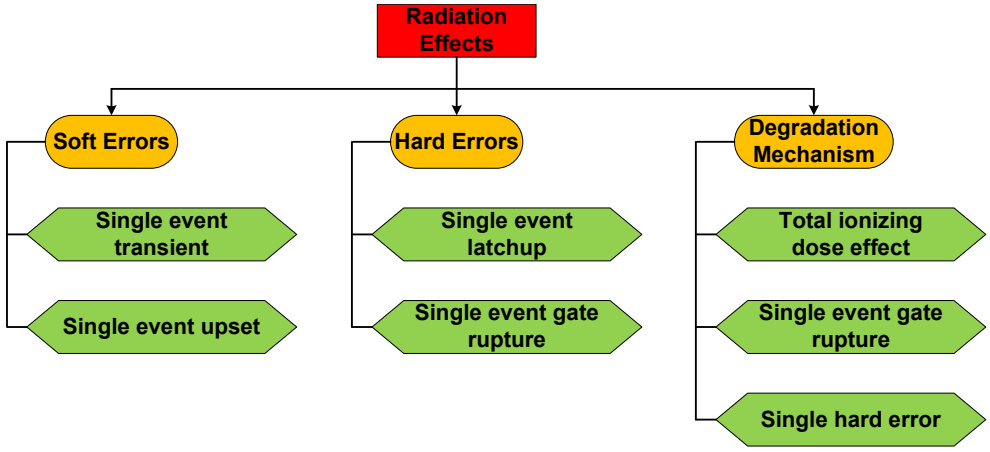


Figure 2.10: Radiation induced effects

Single-event transients (SET)

A single event transient is a voltage spike (a voltage glitch of short duration) in a transistor's drain terminal caused by the charge collection mechanism after a high-energy particle creates an ionization track. The minimum amount of charge collected by a struck node due to an energetic particle strike which is necessary to produce a node voltage value over a switching threshold is called as SET critical charge. For example the digital circuit has the supply voltage of VDD and at the output it has decision threshold of VDD/2, then the voltage spike due to particle strike at

the output node is high enough to cross this decision threshold will result in a SET. Furthermore, downsizing in the technology has increased the sensitivity of CMOS circuits to SETs.

Single-event upset (SEU)

Single-event upsets are different from SETs in their affected target as they take place in memory elements e.g latch, flip-flop, etc, and also differ in time duration as a consequence of an ionizing particle hitting the memory element. Unlike SETs, SEU is no longer transient because SEU is stored in memory elements causing an error for several clock cycles. If a SET occurs in a combinational logic and is clocked to the memory element, then the SET will be converted into SEU as shown in Fig. 2.11.

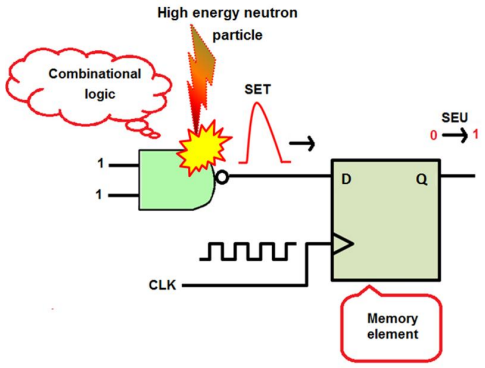


Figure 2.11: Presentation of SET and SEU [18]

Single-event latchup (SEL)

It is a high current state induced by an energetic particle that travels through sensitive regions of the device structure and causes the failure of device functionality. A heavy-ion, or other charged particle, may penetrate the surface of a device and deposit or create a charge in or near the n-well. The electron-hole pairs created by this excess charge produce a transient current extending spike through the n-well/substrate junction as depicted in Fig. 2.12. The current spike produced by a particle strike activates the parasitic bipolar transistors inherent in CMOS technologies and as a result, SEL occurs [19]. Thereby, the current through the high well/substrate resistances may develop a sufficient voltage drop to appear between the p+ diffusion and the n-well, which leads

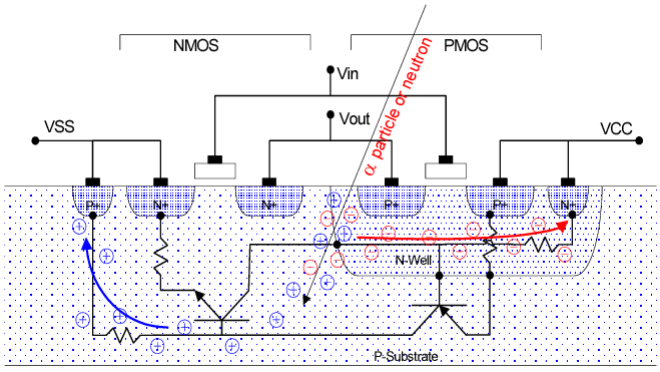


Figure 2.12: An energetic particle causing a SEL condition in a CMOS structure [19]

to the injection of holes at the p+ diffusion to counter this effect. This process triggers one of the two bipolar transistors, which combine into a circuit with large positive feedback. As a result the circuit turns fully ON and causes a short across the power supplies until the device burns up, or the power to it is cycled down. It may or may not damage the device permanently. If the device is not permanently damaged, a removal of power supply is required to recover the normal operation.

Single event gate rupture

Single event gate rupture refers to the formation of a conducting path induced by a single ionizing particle in the gate oxide. It mainly occurs in the power MOSFETs. When a particle strikes near the interface of the gate, the electric field across the gate oxide is increased to its dielectric breakdown due to the collection of holes under the gate from an ion strike. And the resulting leakage current causes a thermal failure of the gate oxide.

Total ionizing doze (TID)

Ionizing radiation generate trapped charges in a dielectric CMOS transistor. These trapped charges disturb the threshold voltage of transistors. These charges drive an increase in leakage currents and degradation of the switching performance, hence leading to the degradation of the lifespan of the device.

2.5 Electrical Modeling of Ionization Process in CMOS Technology

The ionizing particle produces a current pulse after an interaction with a reversed biased junction of a device. The current pulse is traditionally represented using a double exponential waveform and its expression is given by

$$I(t) = \frac{Q}{\tau_\alpha - \tau_\beta}(e^{-t/t_\alpha} - e^{-t/t_\beta}) \tag{20}$$

where Q is the charge (positive or negative) deposited by the particle strike, τ_α is the collection time constant of the p-n junction, τ_β is the ion-track establishment time constant.

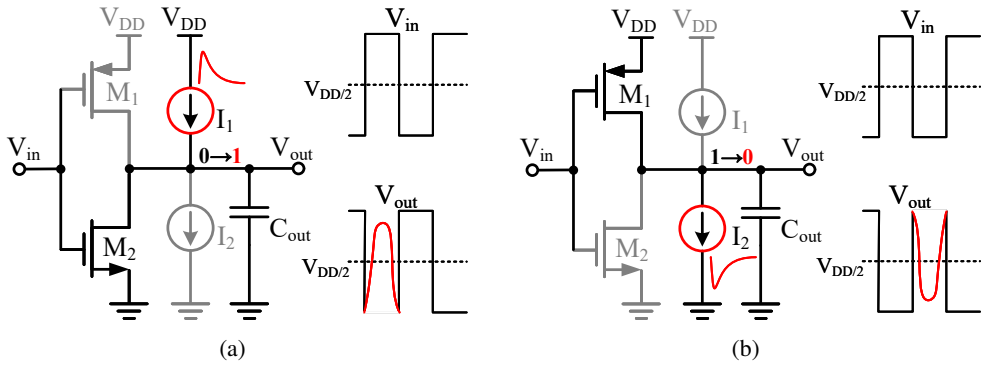


Figure 2.13: (a) When PMOS transistor is OFF: Transition from 0 to 1 (b) When NMOS transistor is OFF: Transition from 1 to 0

A SET event is modelled by a current source for electrical stimulation in Cadence to analyze the phenomenon of ionization [20] [21] [22] [23] [24]. The current source must be connected between the drain and the bulk of each transistor. Fig. 2.13 shows the schematic of the inverter used as a test circuit for the preliminary analysis. When the input voltage (V_{in}) of the inverter is logic high, NMOS transistor is ON and PMOS transistor is OFF, and the expected output voltage (V_{out}) is logic low. The current source I_1 simulates an ionization impact on the PMOS transistor that generates a transition from 0 to 1 at the output as shown in Fig. 2.13 (a). On the other hand, in Fig. 2.13 (b), when V_{in} is logic low, NMOS is OFF and PMOS is ON, and the expected V_{out} is logic high. The current source I_2 simulates an impact on the NMOS transistor that generates a transition from 1 to 0 at the output [14]. This model is used for the analysis of the proposed design. Note that, the impedance of the node converts the current into voltage therefore if the node has large capacitance

then an injected current must be high enough to realize the SET.

Furthermore, it is important to mention that the electrical model used to analyze the phenomenon of ionization comes with some limitations such as lack of information about the orientation of the ion track, what happens if two or more drains are affected by the same impact. Therefore a three-dimensional model is required to have a more realistic model of the ionization phenomenon [16] [25] [26].

2.6 Radiation Hardening Techniques

To overcome radiation effects, radiation hardening techniques were introduced and classified as technological hardening (silicon on insulator, enclosed layout transistors, layout guard ring) and radiation hardening by design (transistor sizing, transistor folding, hardware redundancy, or triple modular redundancy) as listed in Fig. 2.14. Most radiation hardening techniques are used in the digital circuit domain. However, they are also applicable in analog circuit designs. A few of the hardening techniques are discussed in this section.

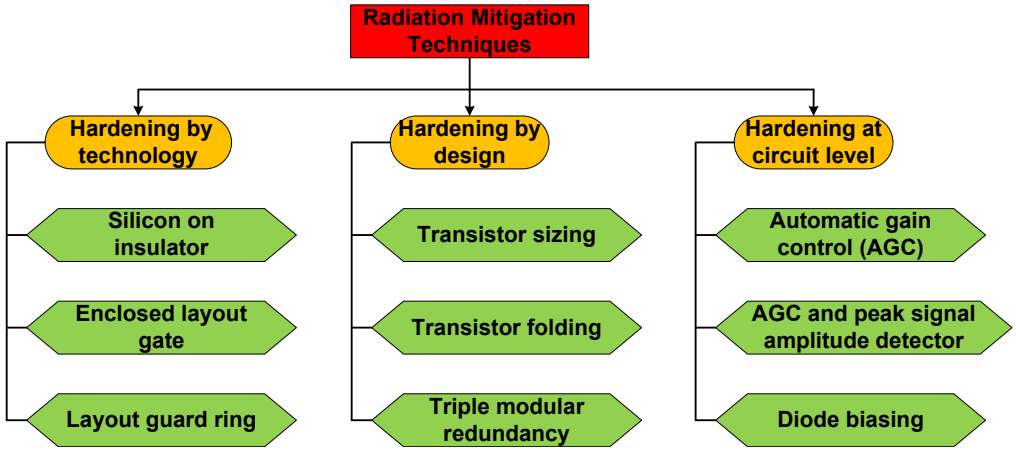


Figure 2.14: Radiation hardening techniques

Silicon on insulator

Silicon on insulator (SOI) technology is characterized by an insulator layer between the silicon wafer substrate and the PN junction as shown in Fig. 2.15. The insulation layer is typically made

up of silicon dioxide. In an SOI transistor, the charge decomposition path is shorter relative to the bulk transistor. This technology significantly reduces the sensitive volume to ionization, hence it is inherently radiation hardened at the cost of an increase in substrate cost.

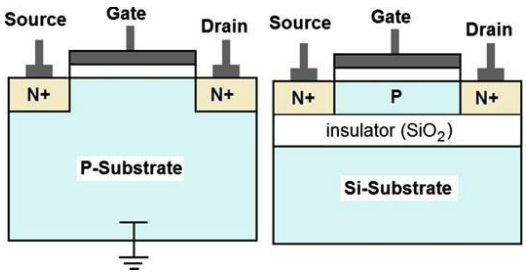


Figure 2.15: Bulk transistor versus SOI transistor [27]

Transistor sizing

The simplest technique for SET mitigation is transistor sizing. The idea is to increase the capacitance so that the charge required to generate a SET has to be more significant. Therefore, there is an increase of the critical charge. For example, doubling the W/L of transistor, increase the node capacitance, decreases SET voltage spike amplitude by half. It requires twice the injection current to cause the SET. The main drawback of this technique is that it causes an increase in propagation delay, delay in frequency response due to large capacitance, and also costs more power dissipation.

Enclosed layout transistor

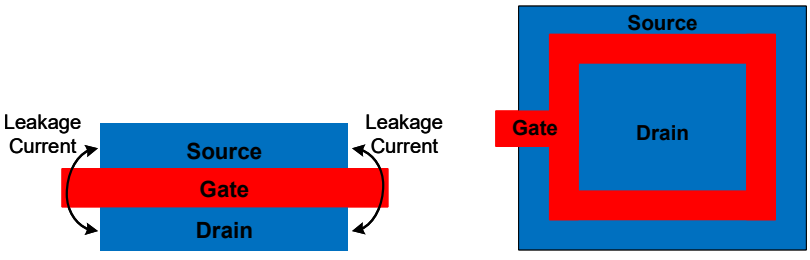


Figure 2.16: (a) Standard CMOS structure with leakage current caused by TIA (b) Enclosed layout structure

This technique focuses on radiation hardening against total ionizing dose effects. It is used

to prevent the parasitic leakage currents between the drain and the source of the standard CMOS transistor [28] [29] [30]. It is a layout approach that encloses the drain of a transistor by the gate and the source as shown in Fig. 2.16. The countered effects are the parasitic leakage current between the drain and the source of a standard CMOS structure. This technique has few drawbacks such as it is difficult to model, W/L ratio of the transistor is no longer straight forward and it also offers more parasitic capacitance than the standard transistor.

Layout guard ring

Layout guard ring provides the electrical and spatial isolation which reduces the risk of SEL and intra-device leakage. Each type of transistor can be surrounded by a protection ring such as NMOS transistor by a P+ ring and PMOS transistor by a N+ ring, an example shown in Fig. 2.17. The main drawback of this technique is an area overhead. Note that, a combination of enclosed layout structure and layout guard ring technique can be implemented to mitigate against SEL and TID effects.

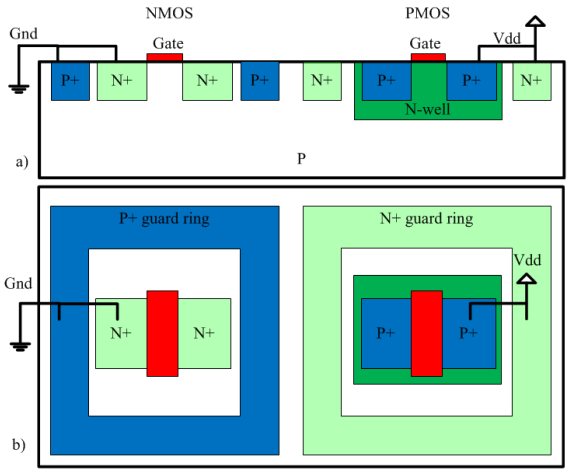


Figure 2.17: NMOS and PMOS transistor with their respective guard ring: (a) cross sectional view (b) top view [14]

Transistor folding

The transistor folding technique is used to divide the sensitive nodes of a transistor into several small nodes according to the number of parallel folded transistors. This local redundancy helps to keep the logical state in case one of the replicas is hit by ionization. The idea is the drain is shared between two transistors in the way that the size of the drain is reduced by half. Hence, reducing the size of the drain also reduces the chance of being hit by ionization. The main drawback of this technique is that smaller transistors have a smaller critical charge. An extra hardening like transistor sizing is also required with this technique.

Triple modular redundancy

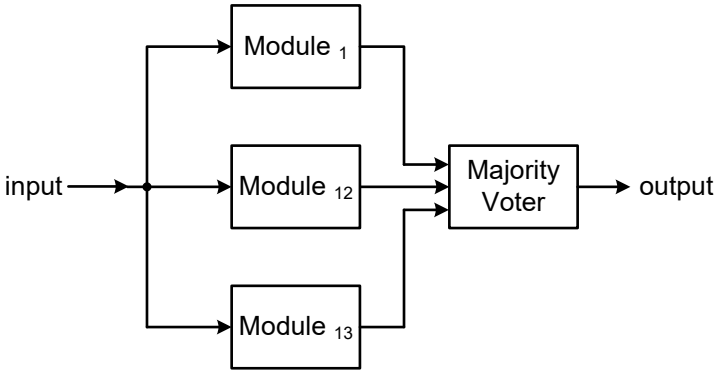


Figure 2.18: Principle of Triple Modular Redundancy

It is the most well-known radiation hardening technique. The idea of this technique is to replicate a combinational logic module and the output is taken through the majority voter. For example Module_{12} and Module_{13} are the exact copies of Module_1 (original module) as shown in Fig. 2.18. A common input signal is applied to all the modules and if any one of the three modules faces an error caused by radiation, the correct output is recovered through the majority voter [31]. The main drawback of this technique is area overhead and more power consumption.

2.6.1 Radiation Hardening at Circuit Level

Fig. 2.19 shows the block diagram of the optical receiver which consists of a photodiode, pseudo-differential pre-amplifier, Limiting amplifier, and the low voltage differential signal (LVDS)

driver. The first element in the optical receiver front-end is the transimpedance amplifier. The amplifier converts the photocurrent delivered by the photodiode (PIN) into voltage with amplification. Since photodiode is a commercial component, thus its performance is affected by radiation by degradation in the quantum efficiency of the photodiode. Therefore, to compensate for radiation-induced degradation, the amplifier should have a wide dynamic range (input current between 10 μA to 500 μA). The amplifier is required to tolerate upto a total integrated ionizing dose of 10 Mrad [32]. The use of an automatic gain control mechanism ensures the constant output signal irrespective of the input current. The radiation hardening circuit technique known as automatic gain control (AGC) is applied in the pre-amplifier block and discussed in detail in the proceeding subsection.

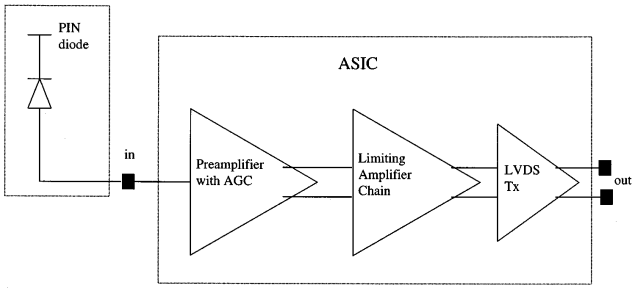


Figure 2.19: Schematic view of the optical receiver, which includes the PIN diode and the receiver ASIC [32]

Automatic gain control (AGC)

The AGC is implemented by the parallel combination of a transistor and a resistor as depicted in Fig. 2.20. The gate voltage of the transistor is controlled by a feedback loop (sf). The feedback loop is designed to be very slow as negligible at the frequency of operation. Its function is only to compensate for the radiation-induced drop in the quantum efficiency of the photodiode during the life cycle of 10 years (Life cycle of Large Hadron). For high input currents (caused by radiations), the AGC block detects a minimum signal below a fixed reference voltage and decreased the feedback transresistance by controlling the gate of the feedback transistor [32] [33].

A dummy circuit is used in parallel with the true signal path to provide the differential inputs for the Limiting amplifiers. Moreover, the outputs from the dummy signal path and the pre-amplifier are sent to the leakage block which detects the leakage current by comparing both the outputs. In

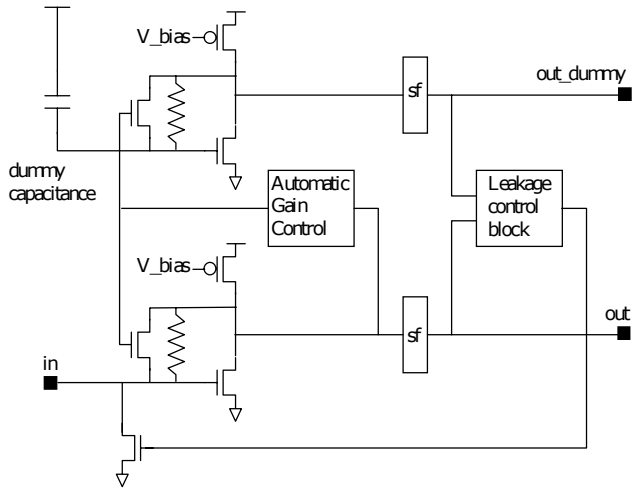


Figure 2.20: Architecture of the transresistance preamplifier [32]

the presence of any leakage current, the maximum output of the true path will drop so the leakage block will detect this leakage and feedback to the gate of the sink NMOS transistor that will drive this leakage current to the ground and re-establish the balanced outputs.

AGC and peak signal amplitude detector

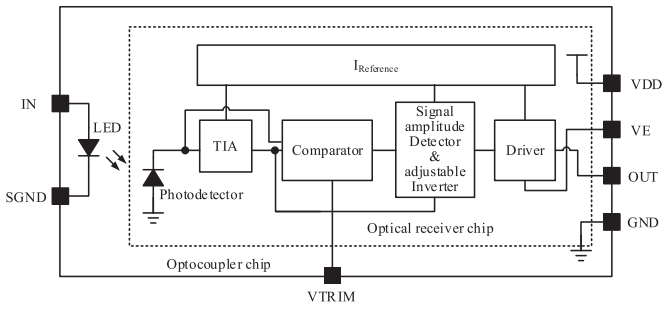


Figure 2.21: Block diagram of optocoupler chip [34]

The radiation hardening technique to mitigate TID and SET effects caused by ionizing radiation at circuit level is adopted by [34] while designing an optocoupler for space applications. The main element in the optocoupler is the optical receiver which consists of a photodiode, TIA, comparator, a signal amplitude detector with an adjustable inverter, and a driver as shown in Fig. 2.21. In a radiation environment, the heavy ions may hit the photodetector and lead to ionization. These

charges are transmitted and collected, resulting in transient fluctuations in voltage and current at the incident node which may cause an optical receiver to transmit an error signal. The proposed radiation tolerant optical receiver implements the combination of AGC to mitigate the TID effect, a peak signal amplitude detector with an adjustable inverter to tolerate SET. Since the first technique is described in the last section hence the explanation of the latter one will be continued. The SET hardened circuit composed of a narrow pulse amplitude detector and a charging current adjustable inverter is presented in Fig. 2.22.

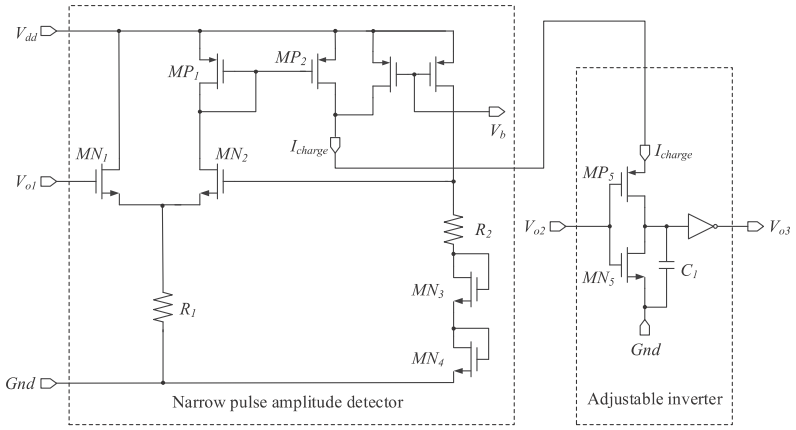


Figure 2.22: A narrow pulse amplitude detector and an adjustable inverter [34]

V_{o1} is the output of TIA, I_{charge} is the current to monitor an adjustable inverter, V_b is the biasing voltage, V_{o2} is the output of a comparator which compares the output of TIA with photodiode's output. In normal signal transmission MN_1 remains off and I_{charge} (IMP_2 + IMP_3) maintains the high value through the inverter. However, when the output signal of the photodiode has a large amplitude, TIA converts this current to a large output voltage as a result MN_1 turns ON. Hence, MN_2 will go to the cut off so the minimum current will flow through the MP_1 and MP_2. As a result, I_{charge} will have a smaller value that prevents the transmission of Vo_2 to Vo_3. Simulation results of the SET hardened circuit are depicted in Fig. 2.23. As SET causes an instantaneous rise in the photo-current I_{pd} of the optical receiver, which is realized by a narrow pulse of large amplitude. After the SET hardened circuit, the output at Vo_3 shows that this narrow pulse of large amplitude is successfully filtered out and wrong signal transmission is prevented. Therefore, this circuit design approach enhances the tolerance to the SET.

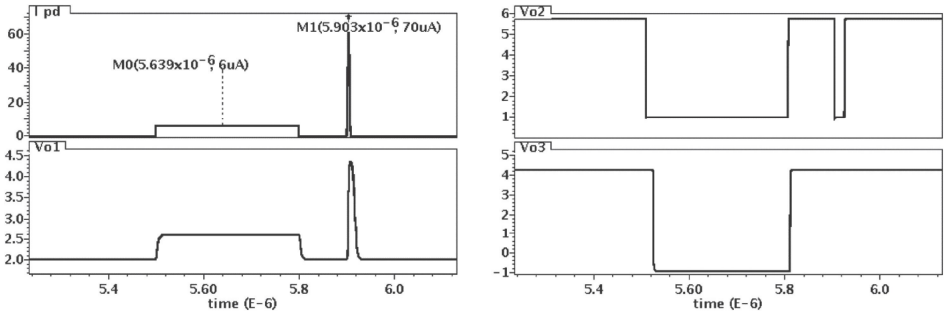
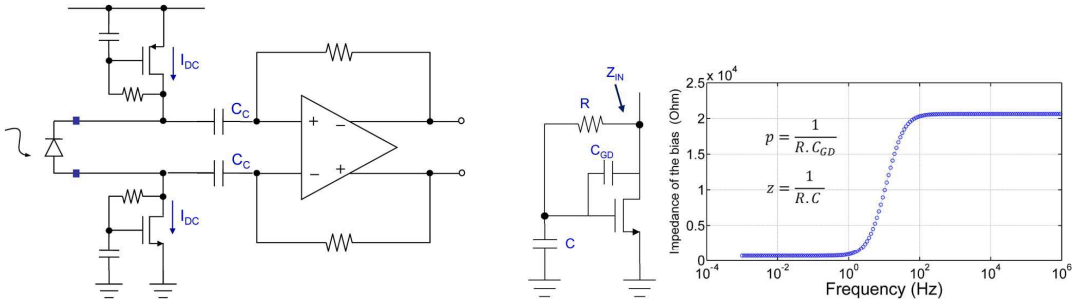


Figure 2.23: SET circuit simulation results [34]

Biasing circuit of photodiode

Another approach is introduced in the literature to mitigate the ionizing radiation effects (total ionizing dose up to 2 MGy) on the photodiode in an optical receiver. As explained in the previous section, the radiation effect in the PIN photodiode is the appearance of a large leakage current. The photodiode leakage current can cause degradation in the optical receiver's sensitivity. The large DC leakage current causes the photodiode bias voltage to decrease due to voltage drop in the biasing circuit. However, the reverse bias voltage across the photodiode should maintain above a minimum level (0.7 V) for high sensitivity and high bandwidth operation. Therefore the biasing circuit of the photodiode is designed which is capable of maintaining a sufficient voltage across a photodiode in the presence of a large leakage current up to 1 mA [35]. Fig. 2.24 (a) shows the photodiode



(a) (b)

Figure 2.24: (a) photodiode bias circuit, (b) Impedance of the PD bias circuit [35]

biasing circuit which consists of a PMOS and NMOS transistors used as a current source and current sink respectively. Both the transistors are diode-connected so they automatically monitor the wide range of photodiode leakage currents (pA to mA) [35]. Biasing circuit maintains sufficient voltage

across the photodiode even in the presence of a large range of leakage currents. Furthermore, a resistor (active resistor- PMOS) connected between gate-drain and the capacitor between gate-vdd/ground execute a low pass filter response. Its function is to provide a high impedance at the signal frequencies and pushes all the photodiode signal current to flow through the TIA as depicted in Fig. 2.24 (b).

2.7 Impedance Scaling

In circuit analysis, it is sometimes convenient to work with non-realistic values such as 1 Ω, 1 F, 1 H, and then transform them to realistic values by using the impedance or frequency scaling technique. The use of convenient values makes the circuit analysis easier. Our work also benefits from the impedance scaling technique. Therefore, a few main features of impedance scaling are discussed below.

Impedance scaling is the process of scaling all the impedances in the network by a factor but the frequency response remains unchanged. It does not alter the voltage transfer function of the network [36]. The scaling factor used in this thesis is denoted by M. For example, the RC low pass filter (LPF) circuit with resistor R and capacitor C, shown in Fig. 2.25 (a) is taken under consideration for the analysis of impedance scaling technique.

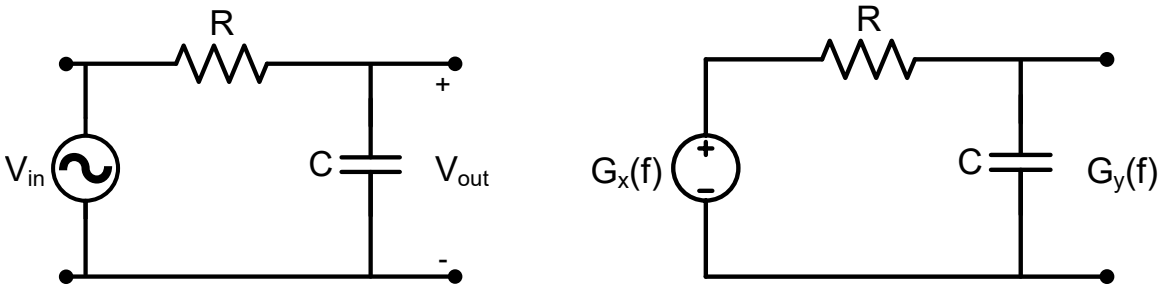


Figure 2.25: (a) RC low pass filter circuit, (b) Noise equivalent model of RC low pass filter

The voltage transfer function of RC LPF is given by

$$\frac{V_{out}}{V_{in}} = H(s) = \frac{1}{1 + \frac{s}{\frac{1}{RC}}} \tag{21}$$

where $\frac{1}{RC} = \omega_o$, is the cut-off frequency of the LPF and it can be re-written as

$$f_{-3dB} = \frac{1}{2\pi RC} \tag{22}$$

Now, if an impedance scaling is applied in Fig 2.25 (a), R will be replaced by R $\times$ M and C will be replaced by C $\times$ $\frac{1}{M}$. From Eq. (22) it is observed that even after applying the impedance scaling the frequency response of the filter does not alter.

Fig. 2.25 (b) shows the noise equivalent model of RC LPF. The noise generated by the resistor R has the power spectral density G_x(f) of 4 kTR V^2/Hz, where k is the Boltzmann constant, T is the temperature in Kelvin. This noise voltage gets applied to the noiseless RC low pass filter having the magnitude squared transfer function of

$$|H(f)|^2 = \frac{1}{1 + (\frac{f}{f_{-3dB}})^2} \tag{23}$$

and the power spectral density of the output signal is given by

$$G_y(f) = G_x(f)|H(f)|^2 \tag{24}$$

By integrating the output power spectral density over the range of frequencies from 0 to ∞ will give the noise voltage at the output, that is

$$E[y^2] = \int_0^\infty G_x(f)|H(f)|^2 \, df \tag{25}$$

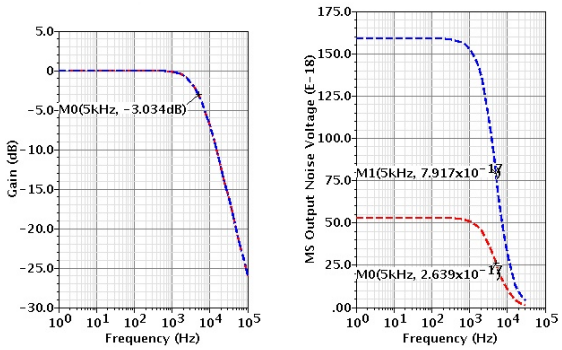
$$E[y^2] = 4kTR.\frac{1}{4RC} \tag{26}$$

which yields the mean squared noise voltage at the output of RC LPF filter as

$$E[y^2] = \frac{kT}{C} \quad V^2/Hz \tag{27}$$

From Eq. (27), it is noticed that the mean squared (MS) output noise voltage of the RC LPF filter is inversely proportional to the capacitance C and it does not depend on R. Therefore, if C

Table 2.3: Frequency and Noise Response of RC LPF before impedance scaling (Red) and after impedance scaling (blue)

Circuit Elements and Performance Summary	Frequency and Noise Response
Before Impedance Scaling ◇ R = 3.2 kΩ, C = 10 nF ◇ f_{-3dB} = 5 kHz ◇ MS output noise = 26.39 aV^2/Hz ◇ RMS output noise = 610.8 nV	
After Impedance Scaling (M = 3) ◇ R = 9.6 kΩ, C = 3.34 nF ◇ f_{-3dB} = 5 kHz ◇ MS output noise = 79.17 aV^2/Hz ◇ RMS output noise = 1.058 μV	

is decreased by M then MS output noise will increased by M and similarly root mean squared (RMS) output noise voltage of the RC LPF filter will be increased by $\sqrt{M}$. The impedance scaling does change the impedance of every node. Therefore, current (input of the receiver) to voltage (output of the receiver) transfer functions are scaled. If the impedance is scaled up by three, then the current to voltage transfer functions will also be scaled up by three. As a result the noise transfer function increases by three. Table 2.3 shows the frequency and noise simulations response of the circuit shown in Fig. 2.25. It can be noticed that the frequency response of the filter remains the same before and after applying the impedance scaling by 3. The RMS output noise voltage of the filter is 610.8 nV but it is increased by $\sqrt{3}$ (1.058 μV) after applying the impedance scaling. To conclude, an impedance scaling technique can be used in an optical receiver's design as it does not alter the voltage transfer function, frequency response, bandwidth, and overall power dissipation of the system.

2.8 Conclusion

This chapter involves the discussion of optical receiver systems and their exposure to radiation environments such as in space. An optical receiver's circuit blocks and the performance specifications of the front-end are discussed. The effects of radiation on the integrated circuits are studied. Furthermore, radiation-induced errors in CMOS devices and radiation mitigation techniques are also presented. In addition, an electrical model to analyze the phenomenon of ionization through the Cadence simulations is also introduced. Finally, an impedance scaling technique is reviewed which is an asset for the proposed work.

Chapter 3

Circuit Design

This chapter explains how the proposed single-event transient tolerant optical receiver was designed and implemented. The proposed receiver is designed to meet the following specifications: data rate of 10 Gb/s, the bandwidth of 5 - 7 GHz, transimpedance gain of $\geq$ 75 dB, the power dissipation of $\leq$ 30 mW, and tolerance to SETs.

Firstly, we designed a conventional optical receiver which was taken as a reference design discussed in Section 3.1.1. Then we proposed a hypothesis for a SET tolerant receiver that applies TMR along with an impedance scaling technique described in Section 3.1.2. To proceed, the performance in gain, bandwidth, power dissipation, and noise of the reference design is compared with the proposed hypothesis. The comparison between two designs verified the behavior similar to the theoretical analysis, hence it promised satisfactory and acceptable results. Therefore, the new SET tolerant optical receiver presented in Section 3.2 was design based on the proposed hypothesis.

3.1 Optical Receiver Front-end Design

3.1.1 Optical Receiver Front-end: Reference Design

Fig. 3.1 shows a conventional optical receiver consisting of a shunt-feedback transimpedance amplifier (TIA), photodiode current $I_{IN_{pp}}$, input capacitance C_{IN} and load capacitance C_L. The effect of a particle's strike at circuit node V_o is modeled by a double exponential current pulse I_{inject} [37] with an amplitude $<$2 mA. In this example, the voltage at node V_o has a decision threshold

of 435 mV while the voltage spike is caused by the SET at T = 60 ns has a greater amplitude of 492 mV. The voltage spike appeared due to SET will cause the transition of the data bit from logic 0 to logic 1 after analog to digital conversion through the decision circuit at the output.

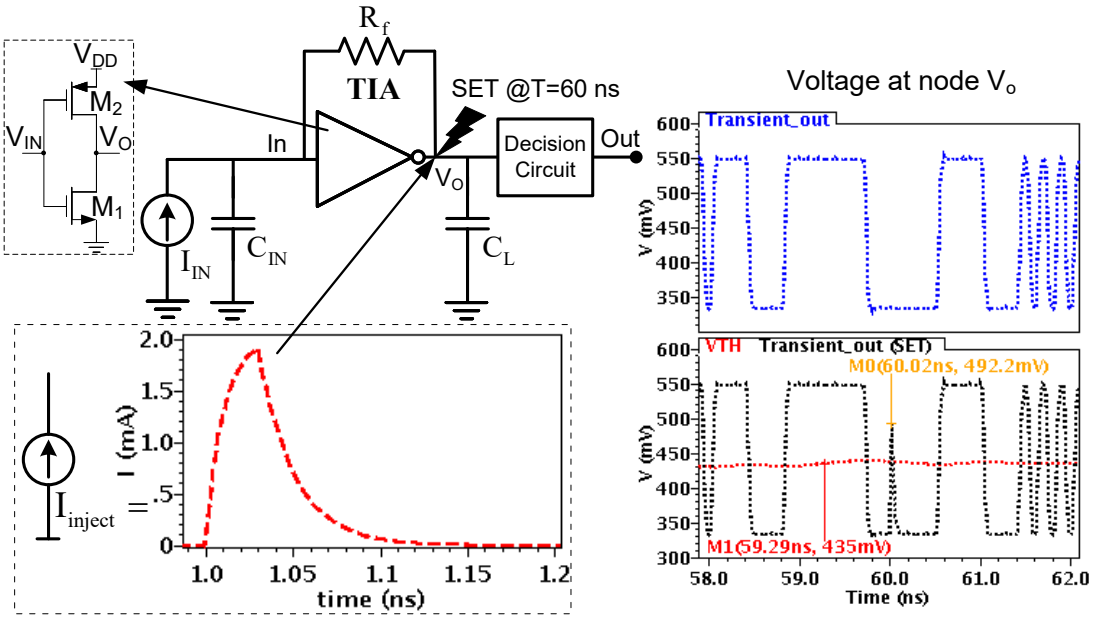
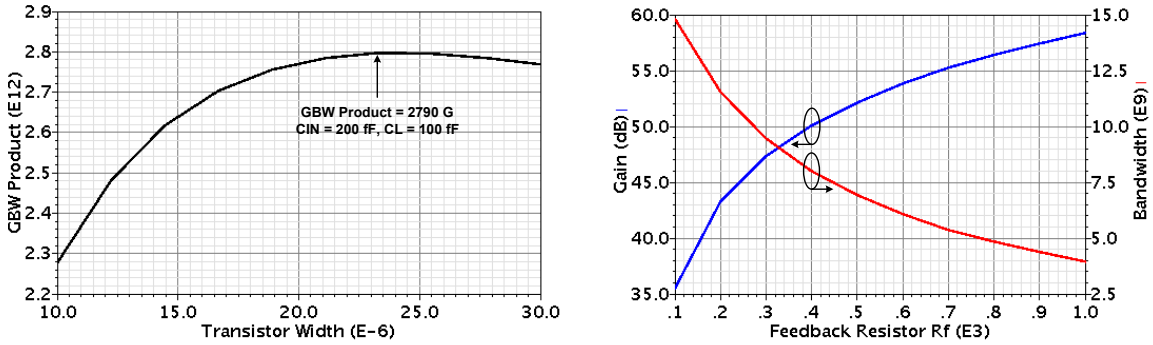


Figure 3.1: Simplified schematic of the reference design



(a) (b)

Figure 3.2: (a) Magnitude of Gain-Bandwidth product of TIA with variable transistor width (W_n = W_p = W), (b) Comparison of Gain and Bandwidth of the TIA with variable feedback resistance

Fig. 3.2 shows the graphs which helped to find the size of transistors while designing the TIA. In this design, an input capacitance (C_{IN}) of 200 fF and load capacitance (C_L) of 100 fF (when the comparator and analog buffer are not connected at the output) are used. Here C_{IN} is the

combination of capacitance associated with a photodiode (150 fF), bond pad, ESD, and gate-source capacitance of TIA transistors M_1 and M_2. It is assumed that the combination of input capacitances is represented by a single capacitor (C_{IN}), however in actual the only capacitance due bond pad and ESD remain fixed. Fig. 3.2 (a) represents that the transistor width ($W_{M1} = W_{M2}$) is swept from 10 μm to 30 μm on x-axis and y-axis gives the magnitude of gain-bandwidth (GBW) product. It is observed that the GBW product has a maximum value at the transistor width of approximately 23 μm. It is important to note that the width of both transistors NMOS (M_1) and PMOS (M_2) is kept the same as it is claimed that having an equal width of transistors, TIA exhibit optimum performance with larger gain-bandwidth product [8]. And an overall transconductance is the sum of each transistor's transconductance ($g_m = g_{m1} + g_{m2}$). Once the transistor's width is found, the next step is to find the value of feedback resistor R_f that gives the desired gain at the bandwidth of interest. Fig. 3.2 (b), y-axis shows gain and bandwidth of the TIA with respect to different values of R_f varying along x-axis. It is noticed that by increasing R_f, the gain of the TIA also increases but the bandwidth drops. In our design, the objective is to achieve the TIA's gain of 50 Ω with bandwidth approximately 50 % - 70 % of the data rate. Therefore, the value of R_f is set to 400 Ω. The summary of values of the circuit components is tabulated in Table 3.4.

Table 3.1: VALUES OF CIRCUIT COMPONENTS

Components	Values	Unit
C_{IN}	200	[fF]
$W_1 = W_2$	23	[µm]
R_f	400	[Ω]
C_L	100	[fF]

Note that, in the reference design an incoming data signal flows through a single path from an input node to the output node. If the data bit is flipped due to a particle strike at any node of the circuit during transmission, an erroneous bit will be transmitted to the output. Therefore, to solve this problem a new design was proposed which transmits the copies of incoming data into three independent identical paths. If anyone's path has an erroneous data signal, the remaining two paths are still error-free, and hence the actual data is obtained through a majority voter.

3.1.2 Proposed Hypothesis using TMR and Impedance Scaling

An idea behind the proposed design is based on the diagram shown in Fig. 3.3. Fig. 3.3 (a) shows that the reference photodiode (used in the reference design) is illuminated by a light source which produces an overall photo-current that flows through the photodiode. On the other hand, Fig. 3.3 (b) shows that the reference photodiode is divided into three equivalent sub-photodiodes (used in the proposed design). When illuminated by the same light source, each sub-photodiode has a flow of one-third of the overall photo-current through it. Therefore, the sum of photo-currents flowing through each sub-photodiode is equivalent to the overall photo-current. This gives us the motivation to design the new optical receiver using TMR which can facilitate radiation tolerance.

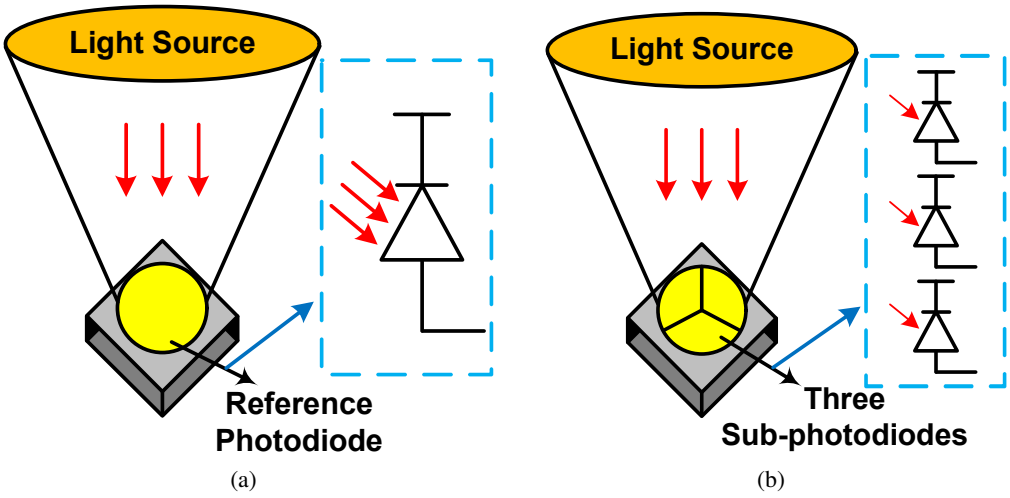


Figure 3.3: (a) Reference Photodiode, (b) Three sub-photodiodes

A SET tolerant optical receiver using a TMR is presented in Fig. 3.4. It consists of three identical sub-receivers in parallel and the final output is taken through the majority voter. Note that, each sub-receiver is an impedance scaled duplicate version of the reference design, hence it shows the similar behavior in gain and bandwidth as the reference design. The majority voter outputs the logic level appearing across the majority of the three sub-receivers outputs. In our analysis, it is considered that the circuit nodes V_{01}, V_{02}, and V_{03} are sensitive to SETs. For example, if a SET occurs in sub-receiver$_1$ at time $t = t_3$, sub-receiver$_2$ at time $t = t_1$, and sub-receiver$_3$ at time $t = t_{2,4}$. The time span of every instant $t = t_1$, $t = t_2$, $t = t_3$, and $t = t_4$ is equal to one unit interval (UI). The SET events flip the logical states on the struck nodes from 0 to 1 or from 1 to 0

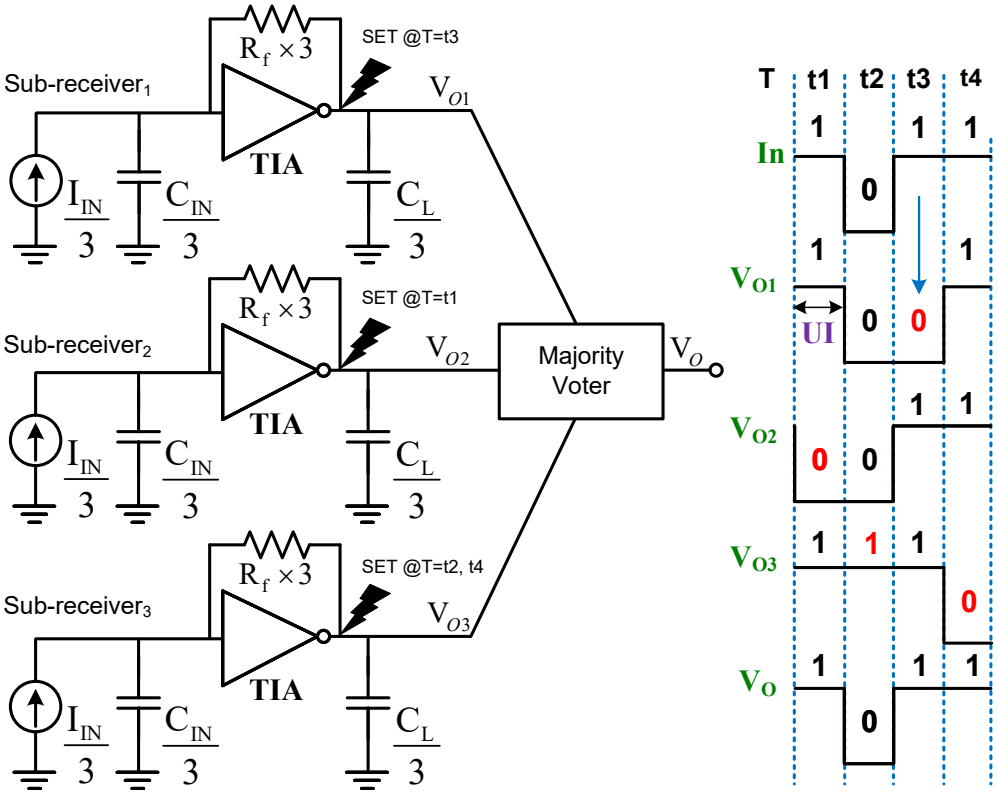


Figure 3.4: Simplified schematic of proposed approach

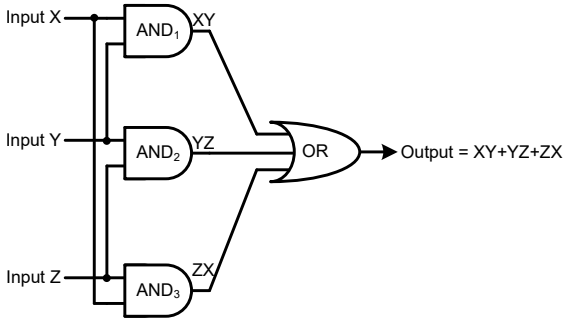


Figure 3.5: Symbolic diagram of Majority Voter

but the majority voter produces the original logical state at the output. In this example, at $t = t_2$ and $t = t_4$ the bits are flipped from 0 to 1 and 1 to 0 at node V_{03} respectively. However, the original signal is achieved by the majority voter at node V_0.

The symbolic view of the majority voter is shown in Fig. 3.5. The majority voter circuit consists of three AND gates and one OR gate. It obtains the original data at the final output node V_0 as tabulated in Table 3.2. It shows the bits which are flipped due to SETs in bold text.

Table 3.2: PERFORMANCE SUMMARY OF THE MAJORITY VOTER

Combinations	**X (V_{01})**	**Y (V_{02})**	**Z (V_{01})**	**XY**	**YZ**	**ZX**	**MV. Out (V_0)**
1	0	0	**1**	0	0	0	**0 at T = t2**
2	**0**	1	1	0	1	0	**1 at T = t3**
3	1	**0**	1	0	0	1	**1 at T = t1**
4	1	1	**0**	1	0	0	**1 at T = t4**

To establish a fair comparison of performance, the conventional optical receiver in Fig. 3.1 is taken as a reference. Fig. 3.6 shows the small-signal model of the reference receiver where overall transconductance $g_m = g_{m1}+g_{m2}$ and total output resistance $R_o = r_{o1} \parallel r_{o2}$. $I_{n,M_{1/2}}$ is the thermal noise current source of M_1 and M_2. I_{n,R_f} is the thermal noise current source of R_f. The power spectral density (PSD) of the noise from R_f is equal to $4kT/R_f$ and PSD of the noise from $M_{1/2}$ is equal to $4kT\gamma g_m$, where k is the Boltzmann constant, T is the temperature in Kelvin and γ is the excess noise factor. In Fig. 3.4, the receiver from Fig. 3.1 is divided into three sub-receivers

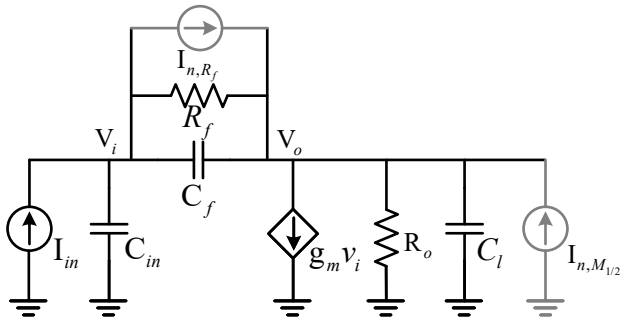


Figure 3.6: Small signal model of shunt-feedback TIA

where each sub-receiver is an impedance scaled version of the reference receiver. The photodiode is divided into three sub-photodiodes assumed to be illuminated by the same overall optical power as the reference receiver. Impedance scaled design facilitates rapid analysis since the overall power

dissipation and the frequency response of the proposed triplicated receiver are preserved. It also allowed us to easily estimate the noise of the sub-receiver relative to the reference design. According to the impedance scaling technique, if M is defined as a scaling factor, then resistors are scaled by M, and capacitors are scaled by 1/M. Voltage transfer functions remain the same [36]. M is equal to 3 in this work. To estimate the gain, bandwidth, and noise performance of each of the sub-receivers relative to the reference design, the following assumptions are made as listed in Table 3.3.

Table 3.3: SUMMARY OF ASSUMPTIONS MADE IN PROPOSED HYPOTHESIS

Circuit Elements	Labels	Assumptions
Input current	I_{IN}	$\div$ by 3
Input capacitance	C_{IN}	$\div$ by 3
Load capacitance	C_L	$\div$ by 3
Overall transconductance	g_m	$\div$ by 3
Feedback resistance	R_f	$\times$ by 3
Output resistances	R_o	$\times$ by 3

Table 3.4: SUMMARY OF CIRCUIT COMPONENTS VALUES

Component/ Parameters	Reference Design	Proposed Hypothesis	Triplicated Design
C_{IN} [fF]	200	$C_{IN}/3$	66.67
$W_{1,2}$ [µm]	23	$W_{1,2}/3$	7.67
R_f [Ω]	400	Rf $\times$ 3	1200
C_L [fF]	100	$C_L/3$	33.34

An input current, input capacitance, overall transconductance, and load capacitance are divided by 3 while the feedback and output resistances are multiplied by 3 as listed in Table 3.4. If impedances are increased by M, the gain becomes three times larger however each sub-receiver receives one-third of the optical input so it is expected that the gain from the overall input will remain the same. The phenomenon of impedance scaling is explained in the previous chapter. According to [36], applying an impedance scaling to the system does not alter the voltage transfer functions of the system. It changes the impedance of the circuit nodes, therefore current to voltage transfer functions also change. For example, if the impedance is scaled up by three then current to voltage transfer functions are also scaled up by three. On the other hand, to find the mean-squared output noise of the sub-receiver it is observed that each noise current PSD decreases by three. However, the

noise transfer functions (impedances) increase by three. Thus, the mean-squared output noise increased by three, leading to an increment of $\sqrt{3}$ times in root-mean-squared output noise voltages as tabulated in Table 3.5. Therefore the output referred noise voltage, bandwidth, and transimpedance gain of the proposed design is given by

$$\begin{aligned} v_{n,prop} &= \sqrt{3} \times v_{n,ref} \\ f_{-3dB,prop} &= f_{-3dB,ref} \\ Z_{TIA,prop} &= Z_{TIA,ref} \end{aligned} \tag{28}$$

Table 3.5: RMS NOISE VOLTAGE OF THE TIA AFTER IMPEDANCE SCALING, M = 3

Noise Sources	PSD [A^2/Hz]	NTF [Ω]	Contribution [V^2/Hz]
R_F	$4kT\frac{1}{R_F \cdot 3}$	$R_F \cdot 3$	$4\ kTR_F \cdot 3$
M_1, M_2	$4kT\gamma \cdot \frac{g_m}{3}$	$\frac{3}{g_m}$	$4kT\gamma \cdot \frac{3}{g_m}$
Root-Mean-squared (RMS) Output Noise Voltage $Vn_{rms} = \sqrt{3} \cdot [4kT(R_F + \gamma\frac{1}{g_m})\ ]$ V/$\sqrt{Hz}$			

The transimpedance gain (Z_{TIA}) is the ratio of TIA output voltage to the overall input current. It is noticed that the gain and bandwidth of the proposed and reference design are approximately the same. However, the output referred noise voltage of the proposed design is $\sqrt{3}$ times the output referred noise voltage of the reference design. Furthermore, the current sensitivity $I_{in,p}$ of an optical receiver is measured in terms of the input-referred noise current $I_{in,rms} = \frac{v_{n,ref}}{Z_{TIA}}$ and calculated as

$$I_{in,p} = SNR \times I_{in,rms} \tag{29}$$

where SNR is the signal-to-noise ratio. The value of SNR is calculated by the formula of "Q function" valid for SNR > 3 [1]

$$Q(x) = \frac{1}{x\sqrt{2\pi}} e^{\frac{-x^2}{2}} \tag{30}$$

where x in Eq. 30 is SNR of the receiver. Let us consider that the reference design required the BER of 10^{-12}. To achieve the required BER, the ratio of input peak current to input referred noise current should be equal to 7 (SNR). However the triplicated design has the output noise voltage of

$\sqrt{3} \times v_{n,ref}$, which degrades the SNR of the triplicated design, it is given by

$$SNR_{triplicated} = \frac{SNR_{ref}}{\sqrt{3}} = 4.04 \tag{31}$$

A triplicated receiver rejects SETs as well as bit errors at the output of a single sub-receiver. From

Table 3.6: PROBABILITY OF ERROR

b_0	b_1	b_2	Majority Voter Output/Error	Probability of an Error
0	0	0	0	$(1\text{-}z)^3$
0	0	1	0	$z(1\text{-}z)^2$
0	1	0	0	$z(1\text{-}z)^2$
0	1	1	1	$z^2(1\text{-}z)$
1	0	0	0	$z(1\text{-}z)^2$
1	0	1	1	$z^2(1\text{-}z)$
1	1	0	1	$z^2(1\text{-}z)$
1	1	1	1	z^3

Table 4.2 an overall probability of an error in the triplicated receiver is estimated. The probability of occurrence of a non-error bit is expressed by (1-z) and an error bit is represented by z. Note that, the probability that all three sub-receivers face a bit error simultaneously is very less hence z^3 can be ignored. The overall receiver suffers a bit error if at least two sub-receivers generate a bit error. Therefore, the overall probability of an error in a triplicated receiver is given by $3z^2$. In other words, the overall BER of the triplicated receiver is approximated as $3\times(\text{BER}_{\text{sub}})^2$. Therefore, for the overall BER of 10^{-12}, the required BER of each sub-receiver is calculated as

$$\begin{aligned} 3 \times (\text{BER}_{\text{sub}})^2 &= 10^{-12} \\ \text{BER}_{\text{sub}} &= 5.773 \times 10^{-7} \end{aligned} \tag{32}$$

The required SNR to meet the requirement of $\text{BER}_{\text{sub}} = 5.773 \times 10^{-7}$ can be calculated by using Eq. 30. Table 3.7 shows that each sub-receiver requires the SNR of 4.87. Therefore, the triplicated receiver requires more optical input compared to the reference designed to meet the

Table 3.7: SNR TO GET TARGET BER

x	Q(x)
4.04	2.82×10^{-5}
4.40	5.66×10^{-6}
4.60	2.20×10^{-6}
4.80	8.25×10^{-7}
4.86	6.10×10^{-7}
4.87	5.78×10^{-7}
4.88	5.51×10^{-7}

requirement of desired BER. The optical power penalty in triplicated design is given by

$$\text{Optical Power Penalty} = 20 \log_{10} \frac{4.87}{4.04} \text{ dB} = 0.8 \text{ dB} \tag{33}$$

3.2 Overall SET Tolerant Optical Receiver Design

Fig. 3.7 shows the overall circuit diagram of the proposed SET tolerant optical receiver. The proposed design has three equivalent receivers Rx_1, Rx_2 and Rx_3 where each receiver contains a photodiode current (I_{PD}), input capacitance (C_{IN}), TIA, post-amplifiers (PAs), offset-compensation loop (OC), low pass filter (LPF), comparator, and SR-Latch. Table 3.8 summarizes the design goals of the proposed SET tolerant optical receiver.

Table 3.8: DESIGN GOAL OF THE PROPOSED OPTICAL RECEIVER

Transimpedance Gain	≥ 75 dB
Data Rate	$10\,\text{Gbit}\,\text{s}^{-1}$
-3 dB Bandwidth	≈ 5 - $7\,\text{GHz}$
Power Dissipation	$\leq 30\,\text{mW}$
Single-Event Transient Tolerant	Yes

A conventional inverter-based shunt-feedback TIA converts the photodiode's current into a voltage. Two Cherry-Hopper post-amplifiers follow the TIA to achieve a high gain. The offset-compensation loop is employed to overcome the dc offsets due to device mismatch and remove the average value of the input signal. The analog outputs of the receivers are taken at the PAs output nodes $V_{1/2/3}$. Furthermore, the differential input voltage of the comparator is provided by the output of PAs ($V_{1/2/3}$) and the passive low pass filter ($V_{avg1/2/3}$), where V_{avg1}, V_{avg2}, and V_{avg3} are

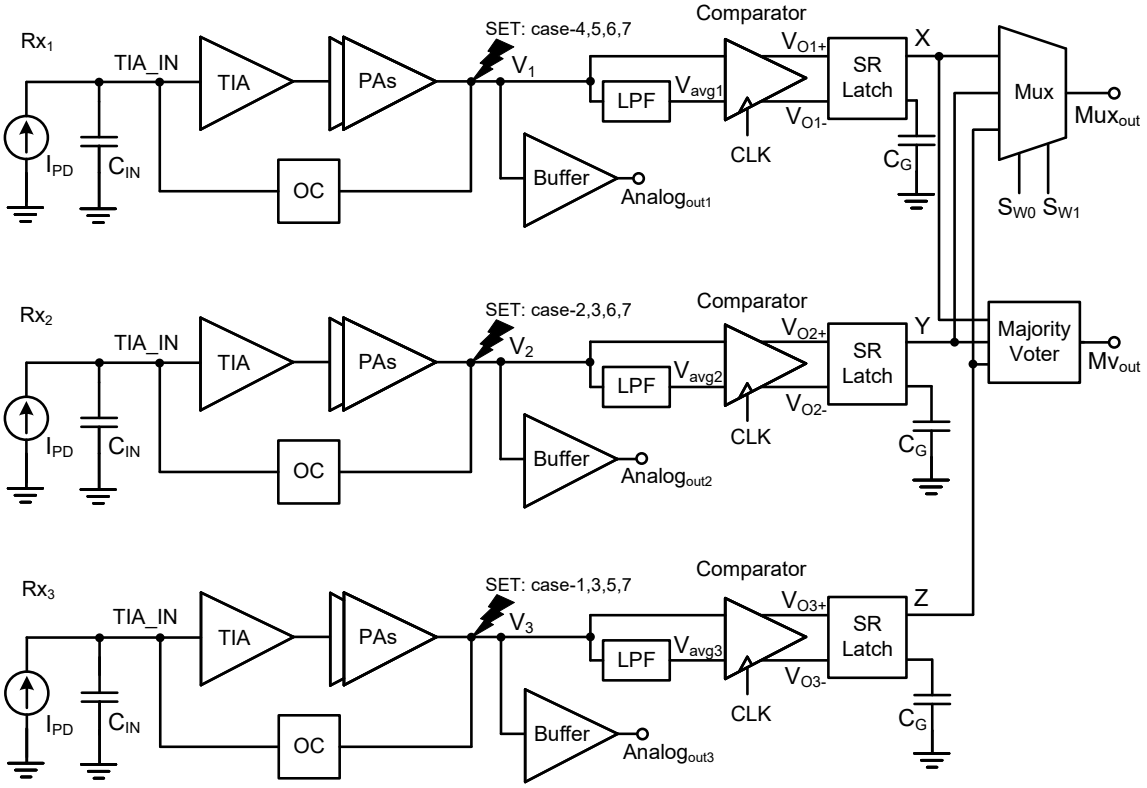


Figure 3.7: Complete design of SET tolerant optical receiver using TMR technique

the average voltages of V_1, V_2, and V_3 respectively. The combination of a comparator and SR-latch produces the digital outputs of Rx_1, Rx_2 and Rx_3 at node X, Y and Z respectively.

The input capacitance C_{IN} = 200 fF, is the combination of capacitance associated with photo-diode, bond pad, ESD, and gate-source capacitance of TIA transistors. The feedback capacitance C_{oc} in the OC loop is 1 pF, and C_G at the unused output of the SR-latch is 10 fF. The resistances used in TIA (R_f) and PAs (R_{fp}) are equal to 400 Ω and in OC loop R_{oc} is 440 kΩ. The NMOS and PMOS transistors used in the TIA and PAs have the width (W) of 23 µm while those in offset-compensation (Inv,1) are 2.5 µm wide. Equal size transistors are used in TIA inverter which increases the total transconductance for an input capacitance and maximizes its gain-bandwidth product [8]. An optimum gain-bandwidth product is found by the sweep of transistors width as shown in Fig. 3.2. The inverter (Inv,2) in the offset compensation loop consists of 200 nm wide transistors. Note that, an impedance scaling is not applied in the offset compensation loop. The offset compensation loop removes the DC offsets due to device mismatch and it is designed to give the low cut-off frequency

of 1 MHz [35]. The analog buffer (used for post-layout simulations and chip measurements) consists of a common source amplifier with a resistive load of 50 Ω to provide the 50 Ω impedance matching to the load for the purpose of measurements. Furthermore, due to device mismatches in a fabricated receiver and a low-frequency noise, an offset voltage may introduce and saturate the output swing and change the bias voltages of the optical front end. Hence, an offset compensation loop is usually used which reduces the low-frequency gain and also generates a low cut-off frequency. An offset compensation loop employs a low pass filter, which is used to compensate for the offset voltage. To avoid the large power penalty due to the baseline wander during the transmission of long runs, its low cut-off frequency should be small. The effective time constant of this filter is τ = $R_{oc}C_{oc}(1+gm_{inv,1}r_o)$, where $gm_{Inv,1}$ is the total transconductance of inverter $(\mathrm{Inv}, 1)$ and r_o is the total resistance at the output of inverter (Inv,1) [13]. Fig. 3.8 shows the complete schematic of the optical receiver front end along with the value of its components.

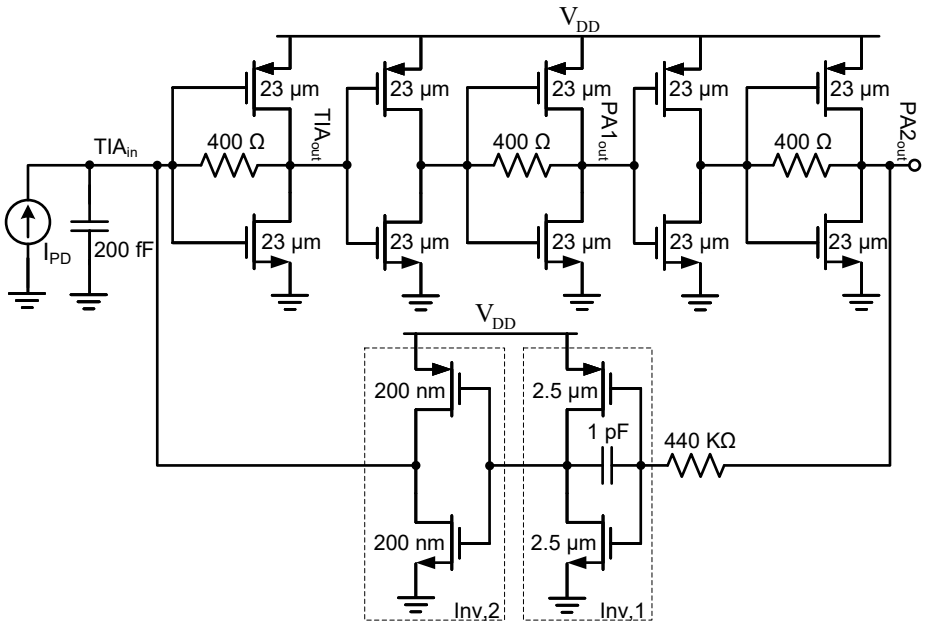


Figure 3.8: Schematic of optical receiver front-end

Fig. 3.9 shows the schematic of the low pass filter (LPF) consists of a resistor R_{LPF} $(10\,\mathrm{k}\Omega)$ and a capacitor C_{LPF} $(1\,\mathrm{pF})$, where output is taken across the C_{LPF}. It gives an average voltage V_{avg} of the front end's output at node (Out), V_{avg} sets the threshold voltage for the comparator circuit to make logical decisions on the incoming signal. Note that, a comparator and the SR latch

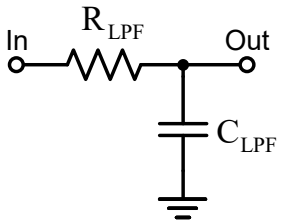


Figure 3.9: Schematic of low pass filter (LPF)

circuits are designed by the former student (Shamita Tabassum Nur, ID: 1125168) of this group under the supervision of Prof. Glenn Cowan. A multiplexer (MUX) is used to obtain an output of the individual sub-receiver when needed. In this study, the circuit nodes V_1, V_2, and V_3 are considered sensitive to single-event transient events. Seven cases are taken under consideration to see the effect of SETs. Each case has a different time of occurrence and it indicates the event of particle strike. The double exponential independent current sources are used which model the ionization process caused by the strike of energetic particles on the struck node.

3.2.1 Limitations of the Proposed Design

The proposed optical receiver tolerates Single-event transients with a certain limitation. The proposed receiver consists of three identical sub-receivers, it removes an error if a given particle strike only effects one sub-receiver or two separate particles strike effect one sub-receiver but do not occur in the same unit interval. In other words, if two or more sub-receivers face a particle's strike simultaneously in the same unit interval then the proposed receiver does not remove an error. Therefore, in such a scenario an error propagates to the final output. It is assumed that only a single sub-receiver is irradiated in a one unit interval.

3.3 Conclusion

A conventional receiver is designed first which is taken as a reference design in this thesis. Then a hypothesis of a SET optical tolerant receiver is proposed. It consists of three identical sub-receivers in parallel which transmits the copies of original data in three independent paths. In case, if data error occurs in any of the three paths, correct data can be obtained through the majority

voter because the other two paths still have error-free transmission. Note that, the sub-receivers are impedance scaled versions of the reference design. The theoretical analysis of the proposed hypothesis is also verified with the circuit simulations. Finally, a SET tolerant optical receiver using triple modular redundancy and an impedance scaling technique is completely designed and presented. It achieves the performance parameters such as gain, bandwidth, and an overall power dissipation similar to the reference design at the cost of 0.8 dB optical power penalty relative to the reference design.

Chapter 4

Simulation Results and Layout

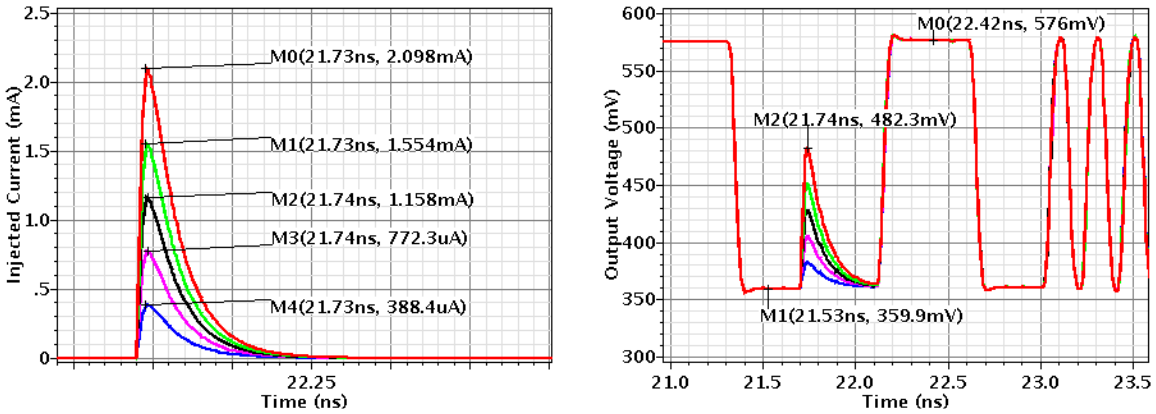
This chapter shows the simulation results and layout of the proposed receiver. All the simulations presented in this chapter are performed in a 65 nm CMOS process using Cadence at an input random data rate of $10\,\mathrm{Gbit\,s^{-1}}$ with 1 V of the supply voltage.

4.1 Simulation Results

4.1.1 Circuit Simulations of the Proposed Hypothesis

This section discusses the circuit simulations of the proposed hypothesis and a comparison between the simulation results of reference design and the triplicated design is made. Fig. 4.1 represents the profile of injected currents with magnitude range between $0.4\,\mathrm{mA}$ to $2.1\,\mathrm{mA}$. An injected current ranging from $0.4\,\mathrm{mA}$ to $1.5\,\mathrm{mA}$ is not sufficient for the switching threshold ($\approx 468\,\mathrm{mV}$) of the output voltage, hence the output voltage maintains its logical state. But with an injected current of $2.1\,\mathrm{mA}$, the spike of $482\,\mathrm{mV}$ is observed in the output voltage which is larger than the switching threshold. It causes the logical state of the output signal to flip from 0 to 1. This phenomenon occurs because an injected current of $2.1\,\mathrm{mA}$ transfers sufficient charge at the struck node which is greater than the critical charge of the struck node which results in SET. Note that, the circuit simulations are done while considering that the circuit itself is noiseless and it bears only injected noise due to particles strike.

Fig. 4.2 represents the simulation results of the reference design (shown in Fig. 3.1) and the



(a) (b)

Figure 4.1: (a) Magnitude of injected currents, (b) Output signal state changed from Logic 0 to 1 due to an injected current

triplicated design (shown in Fig. 3.4). The eye diagram and transient output voltage of the reference and the triplicated design are presented. Based on the proposed hypothesis, an overall input current is equally split into three. Each sub-receiver gets one-third of an overall optical input and exhibits the transimpedance gain of $400\,\Omega$ similar to the reference design with a minor DC shift. Note that, the transimpedance gain is the ratio of TIA output voltage to the overall input current.

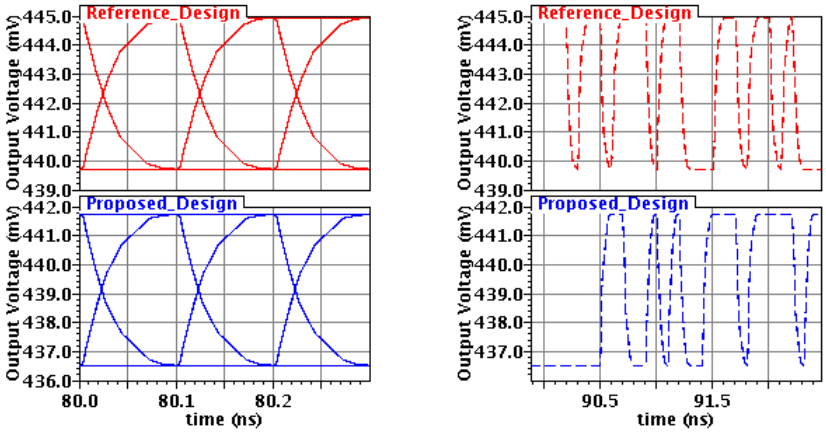


Figure 4.2: Transient response of the reference and triplicated design

Fig. 4.3 shows the simulation results of BER as a function of Q-factor which is a signal-to-noise ratio. It can be noticed that the reference design has input current sensitivity of 12.89 μA_{pp} which gives the required BER of 10^{-12}. However, the triplicated design gives BER of 10^{-9} with

the same amount of an overall input current. Therefore, the triplicated design requires 2.35 μA_{pp} more overall input current with SNR of 4.87 to produce the required BER of 10^{-12} at the cost of 0.8 dB optical power penalty. Apart from the sensitivity degradation of $0.8\,\mathrm{dB}$, the triplicated design benefits from the impedance scaling technique and exhibits relatively similar bandwidth, gain, and overall power dissipation as of the reference design. The performance summary of the reference and the triplicated design is tabulated in Table 4.1. It is observed that simulation results agree with the proposed hypothesis with 2.3 $\%$ error in $v_{n,rms}$ between the calculated and the simulated results. The complete design of the triplicated SET tolerant optical receiver is discussed in the next section.

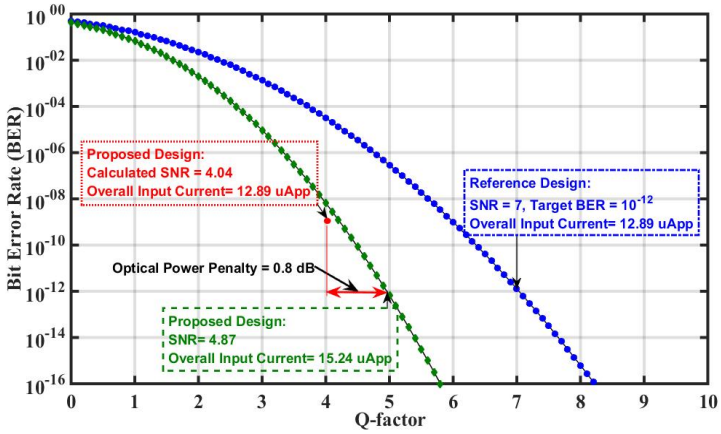


Figure 4.3: BER simulation results with respect to Q factor at 10 Gb/s with input PRBS 2^7-1

Table 4.1: RESULTS SUMMARY OF REFERENCE AND TRIPLICATED DESIGN

Parameters	Reference Design	Proposed Hypothesis	Triplicated Design[b]
Data Rate [Gbps]	10	10	10
Z_{TIA} [Ω]	400	$Z_{\mathrm{TIA,ref}}$	400
BW [GHz]	7.31	$\mathrm{BW_{ref}}$	7.25
Pdc [mW]	2.20	$\mathrm{Pdc_{ref}}/3 = 0.734$	0.73
$v_{n,rms}$ [μV]	372.8	$\sqrt{3}\times v_{n,ref} = 645.7$	631.1
Iin_{pp} [μA]	12.89	$\mathrm{Iin_{ref}}/3 = 4.296$	4.29
VEO_{pp} [mV]	5.216	$\mathrm{VEO_{ref}}$	5.19
SNR	7.0	4.04	4.1
SNR[a]	7.0	4.87	4.87
Power penalty [dB]	-	0.8	0.8

[a]SNR required to achieve the BER of 10^{-12}, [b]Values of a single sub-receiver

4.2 Simulation Results of the Proposed Receiver

The proposed receiver consists of three parallel identical sub-receivers, so they exhibit identical performance in terms of gain, bandwidth, and vertical eye-opening in the absence of SETs. Therefore, frequency response and transient response of one of the three sub-receivers is presented.

4.2.1 Frequency and Transient Response

The frequency response shown in Fig. 4.4 is taken at the outputs of TIA, PA1, and PA2 (node V_1). The optical receiver front-end achieves the overall transimpedance gain of 83.18 dB, a bandwidth of 7.2 GHz, and an input-referred noise current of 0.93 μA_{rms} which is comparable to [38].

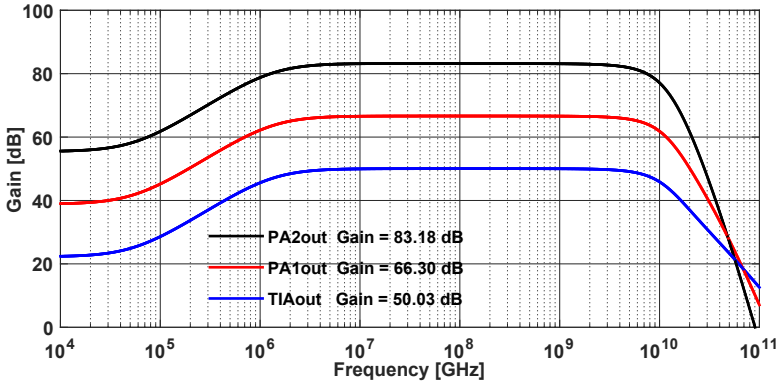


Figure 4.4: Frequency response of the overall receiver front-end

For the transient response, a random bit-stream is generated by using a pseudorandom binary sequence (PRBS) 2^7-1 at a bit period of 100 ps. From Fig. 4.5, 4.6, and 4.7, the simulation results show that the front-end has a maximum vertical eye-opening of 207 mV_{pp}, 321 mV_{pp}, and 400 mV_{pp} with an input current of 15 μA_{pp}, 25 μA_{pp} and 35 μA_{pp} respectively. Fig. 4.5 also shows the relative time delay of approximately 51 ps from analog front-end's input to the PA2's output. The proposed optical receiver has a minimum input current sensitivity of 13.4 μA_{pp} for the BER of 10^{-12} at a data rate of 10 Gb/s. The complete receiver dissipates 33 mW of power, a jitter of 0.8 ps, and a peak-to-peak inter-symbol interference of 6 mV.

Fig. 4.8 shows the eye diagrams of the receiver when it is simulated for the 1.5 (15 Gb/s) and 2 (20 Gb/s) times more the operational data rate. Since the receiver has a bandwidth of 7.2 GHz,

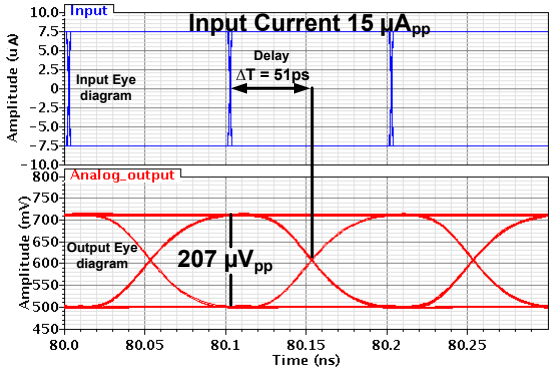


Figure 4.5: Eye-diagram of the overall receiver from a PRBS of $2^7 - 1$ at 10 Gbps with delay from input to the front-end's output

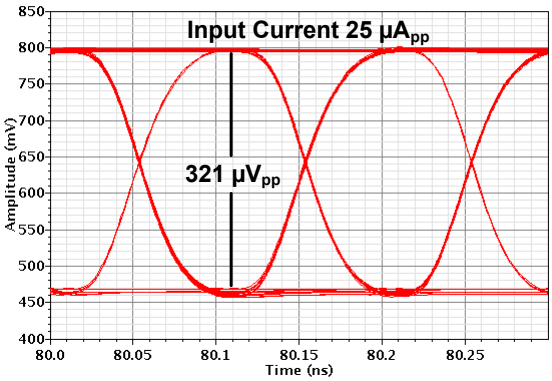


Figure 4.6: Eye-diagram with peak-peak input current of $25\,\mu A_{pp}$

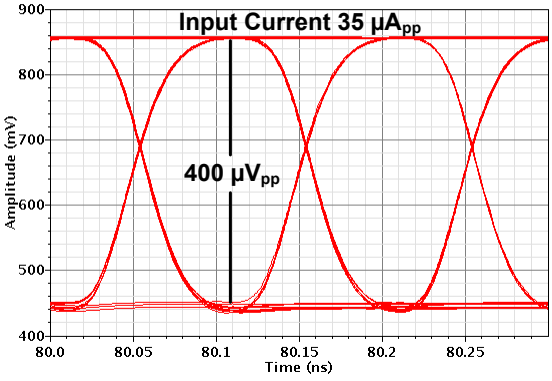
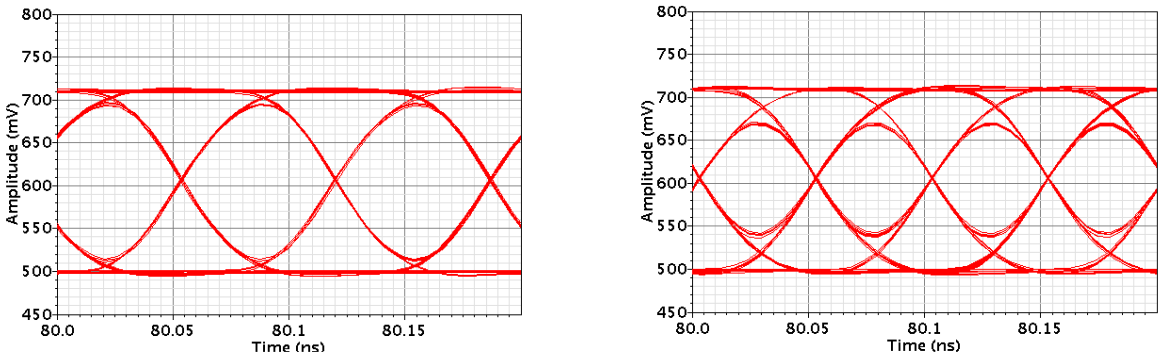


Figure 4.7: Eye-diagram with peak-peak input current of $35\,\mu A_{pp}$

therefore this range of bandwidth is even less than the 50 % of these data rates. Hence, one would expect a significant inter-symbol interference in an eye diagram. At a data rate of 15 Gb/s, an ISI of 18 mv_p and at 20 Gb/s an ISI of 46 mv_p is observed which notably reduces the vertical eye-opening.



(a) (b)

Figure 4.8: Eye Diagram at (a) data rate of 15 Gb/s , (b) data rate of 20 Gb/s

A transient output of the front-end at node V_1 and output of the low pass filter at node V_{avg1} is shown in Fig. 4.9. The LPF produces an average of the coming signal, which sets the threshold voltage for the decision circuit to decide on the received signal. The signal with amplitude above the threshold is taken as logic high (bit 1) and below the threshold is considered as logic low (bit 0).

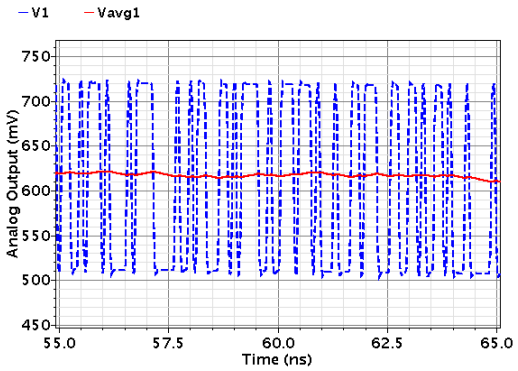


Figure 4.9: Transient output of the front-end (blue waveform), Average of the transient output (red waveform)

The multiplexer produces a digital output of the individual sub-receiver based on the configuration of switches S_{W0} and S_{W1}. Fig. 4.10 shows the multiplexer inputs from each sub-receiver

and an input_1 is outputted at node Mux_{out} when both the switches are OFF. Note that, the output signal has a delay of $\approx$ 220 ps which is caused by the logic gates in the multiplexer and the digital buffer. Finally, the performance summary of the proposed SET tolerant optical receiver is tabulated in Table 4.2.

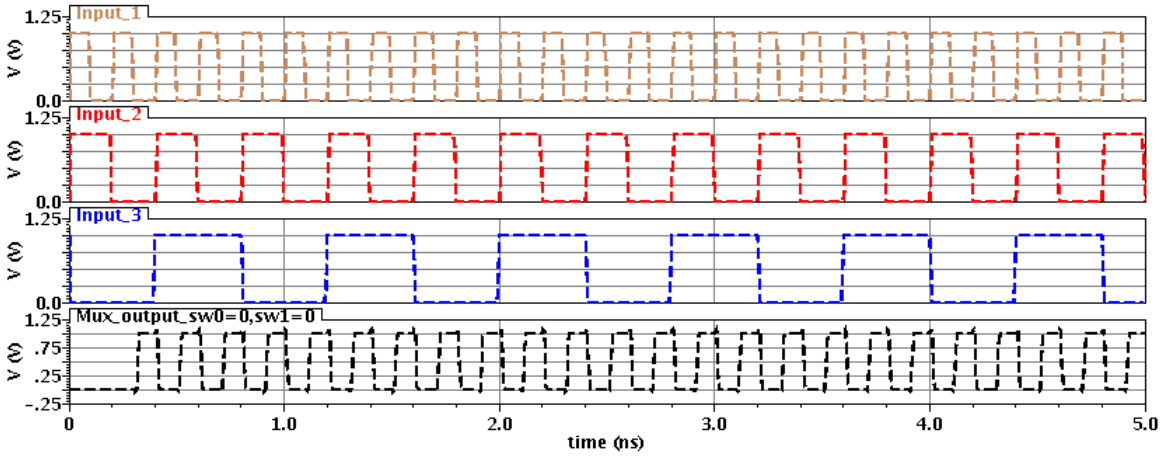


Figure 4.10: Simulation results of the multiplexer with S_{W0} = 0 and S_{W1} = 0

Table 4.2: PERFORMANCE SUMMARY OF THE PROPOSED RECEIVER

Parameters	Units	Value
Transimpedance Gain	dB Ω	83.18 (14.4 kΩ)
3-dB Bandwidth	GHz	7.2
$I_{in,rms}$	μA	0.93
Bit Rate	Gbps	10
Maximum eye opening	mV_{pp}	207.0
Current Sensitivity for BER = 10^{-12}	μA_{pp}	13.4
Total Power Dissipation	mW	33: TIA(2.1), PAs(8.4), OC Loop(0.5)

4.2.2 SET Simulations and Majority Voter Output

SET simulation results are presented in Fig. 4.11 and Fig. 4.12 respectively. The proposed receiver can overcome the errors caused by SETs if and only if only one sub-receiver suffers a particle strike in a given unit interval (UI). However, if more than one sub-receiver experiences SETs concurrently then an erroneous bit will transfer to the output of the majority voter (Mv_{out}). In other words, an overall receiver suffers a bit error if at least two sub-receivers generate a bit

error. To validate the functionality of a proposed SET tolerant receiver seven cases are taken into consideration. Case-1, case-2, and case-4 show that each sub-receiver faces one SET event non-concurrently while case-3, case-[5-7] show that more than one sub-receiver has synchronous SET events.

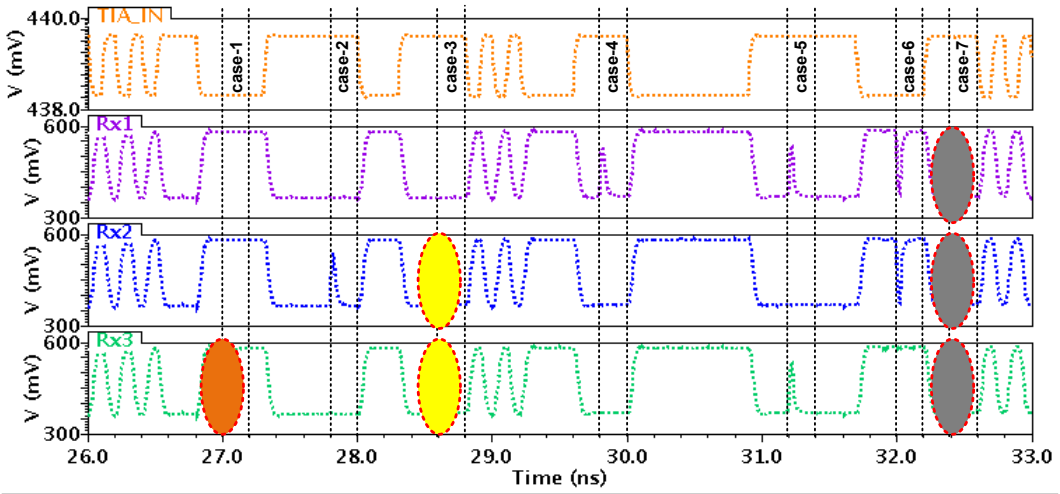


Figure 4.11: SET simulations results at TIA input and at nodes V_1, V_2, V_3 with cases-[1-7]

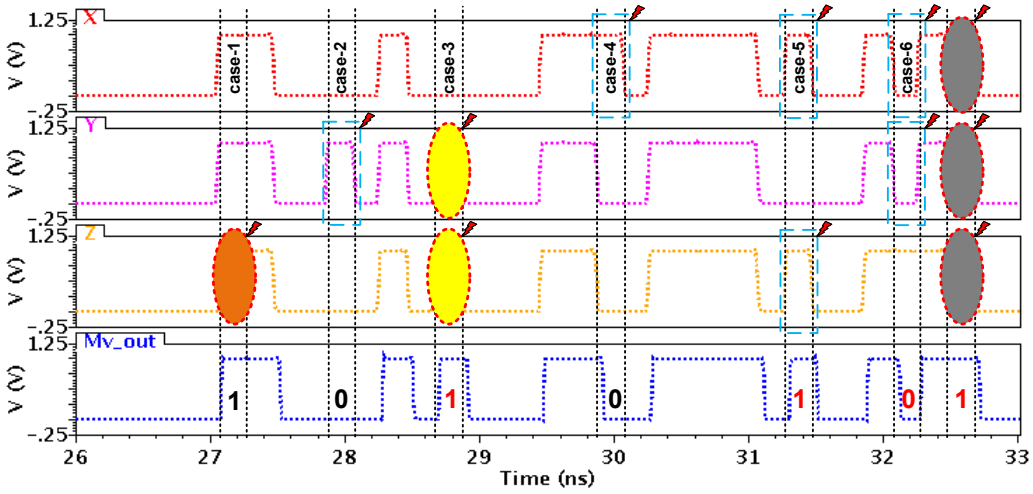


Figure 4.12: SET simulations results: digital outputs at nodes X, Y, Z and final output at Mv_{out} with cases-[1-7]

Fig. 4.11 shows the transient signals at the input of TIA, nodes V_1, V_2, and V_3 in the presence of SET events. The voltage at nodes V_1, V_2, and V_3 are the inverted versions of the TIA input signal.

The spikes produced by SETs are responsible for the transmission of flipped bits to circuit nodes X, Y and Z, as shown in 4.12. Furthermore, the red ellipse shows that only one sub-receiver has SET (case-1) at a time while the yellow ellipses indicate that two sub-receivers have synchronized SETs (case-3). The grey ellipses highlight that all three sub-receivers have SETs concurrently (case-7) which leads to an error. The blue dashed rectangular box shows the rest of the unit intervals which suffer from bit flipping due to SETs. The majority voter removes the error and recovers the correct data for case-1, case-2, and case-4 while in case-3 and case-[5-7], the erroneous bit is propagated to Mv_{out}. The overall propagation delay from the TIA input (TIA_{IN}) to the Mv_{out} (including buffer after the majority voter) is approximately $240\,ps$. The performance of the SET tolerant optical receiver is summarized in Table 4.3.

Table 4.3: SET SIMULATIONS AND MAJORITY VOTER RESULTS

Case	TIA_{input}	V1	V2	V3	Mv_{out}	Error	Comments
1	0	1	1	0	1	1	error removed
2	1	0	1	0	0	1	error removed
3	1	0	1	1	1	2	error propagated
4	1	1	0	0	0	1	error removed
5	1	1	0	1	1	2	error propagated
6	0	0	0	1	0	2	error propagated
7	1	1	1	1	1	3	error propagated

The SET simulations are also performed by injecting a current on other nodes of the triplicated receiver. A current of 55 µA is injected at the output of the TIA and the current of 0.45 mA is injected at the output of PA1. The amplitude of the injected current is sufficient to produce SETs as the transient output signal crosses the decision threshold of 470 mV. The current is injected on six different occasions and it causes SETs which are highlighted by small yellow circles in Fig. 4.13. The black dashed boxes shown in Fig. 4.14 indicate flipped bits due to SETs. However, the correct error-free signal is recovered through majority voter as listed in Table 4.4.

Table 4.5 shows the comparison of the proposed receiver with other works. To the best of the authors' knowledge, the proposed approach of SET tolerance has not been implemented before in optical receivers. The performance of the proposed receiver is comparable to [38] in bandwidth and input-referred noise current but has significantly less power consumption. An optical receiver designed in [17], [35] are tolerant to total ionizing dose radiation impact while in [38] is not radiation

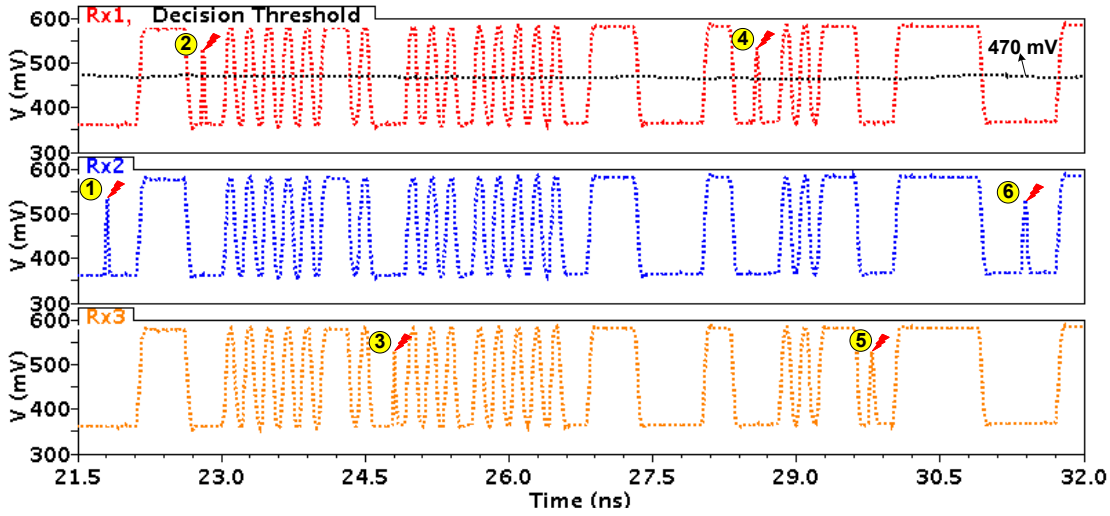


Figure 4.13: SET simulations results of triplicated receiver at nodes V_1, V_2, V_3

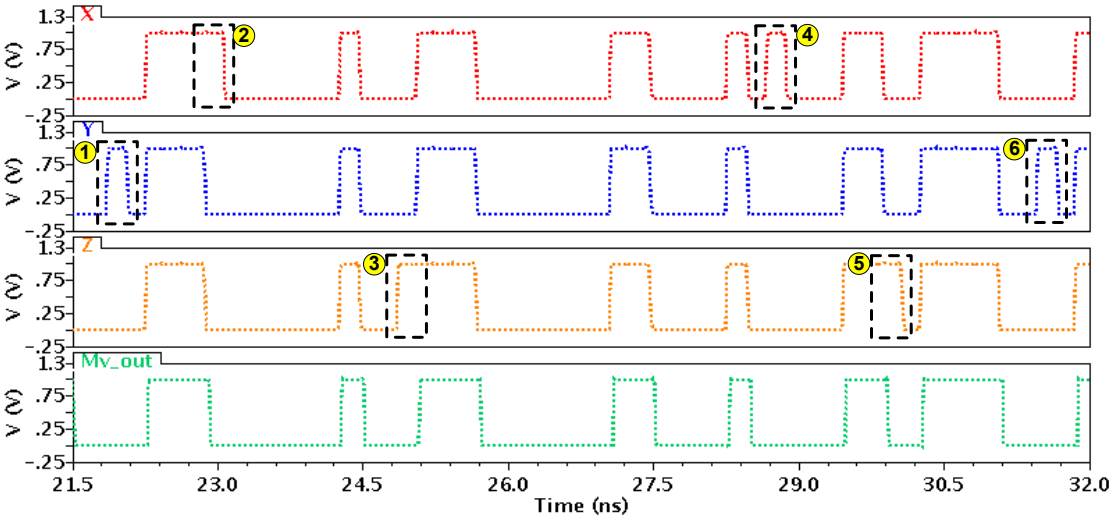


Figure 4.14: SET simulations results of triplicated receiver at nodes X, Y, Z and Mv_{out}

Table 4.4: SET SIMULATION RESULTS ON DIFFERENT CIRCUIT NODES

SETs	Injected Current	Circuit Nodes	Receiver Path	comments
1	55 µA	TIA_{out}	Rx_2	error removed
2	55 µA	TIA_{out}	Rx_1	error removed
3	55 µA	TIA_{out}	Rx_3	error removed
4	0.45 mA	$PA1_{out}$	Rx_1	error removed
5	0.45 mA	$PA1_{out}$	Rx_3	error removed
6	0.45 mA	$PA1_{out}$	Rx_2	error removed

tolerant.

Table 4.5: RESULTS COMPARISON SUMMARY

References	This Work	[17]*-2019	[35]*-2013	[38]*-2019
Bit Rate [Gb/s]	10	2.56	5	10
Gain [$\mathrm{dB}\,\Omega$]	83.18	-	86	68.3
Bandwidth [GHz]	7.2	-	-	7.0
$I_{in,rms}$ [µA]	0.93	-	-	0.97
Power Dissipation [mW]	33	70	120	81
Type of Tolerance	SET	TID	TID	None

*Measurement results

4.3 Layout

The layout of proposed receiver front-end is completed in $65\,\mathrm{nm}$ CMOS technology and it utilized a total area of $1\,\mathrm{mm}^2$ and an active area of 0.2 mm $\times$ 0.5 mm. Figure 4.15 shows the overall schematic diagram that is used for fabrication. The schematic contains TIAs, PAs, offset compensation, source follower buffers for analog output, passive low pass filters (LPF), comparator/SR-latch, serial shift register, differential clock input, multiplexer, buffer for digital output, and majority voter. The serial shift register is used to provide the control bits for the offset compensation of latch and also control switches used in the multiplexers. The tape-out of the proposed receiver chip covers an area of $1\,\mathrm{mm}^2$ and it is shown in Fig. 4.16 and the layout of different sub-blocks used in the complete receiver's design and the majority voter are shown in Figure 4.17. The layout of the comparator/SR-latch was designed by Shamita Tabassum Nur and the serial shift register by Michael Segev with the help of Dr. Glenn Cowan.

An overall layout of the proposed receiver is done carefully because it consists of three identical sub-receivers. It is expected that each sub-receiver exhibits similar results in the frequency and the transient responses. Therefore, the effect of layout parasitics on the circuit nodes must be equal in each sub-receiver. All the significant paths have the same dimensions of metal layers. The significant paths include sub-receivers input signals pad to TIAs input, analog buffers output to the analog output pads, latches output to the input of multiplexer and majority voter. Furthermore, the sub-receivers are placed on the left side closed to the input pad at a distance of 100-micron meters

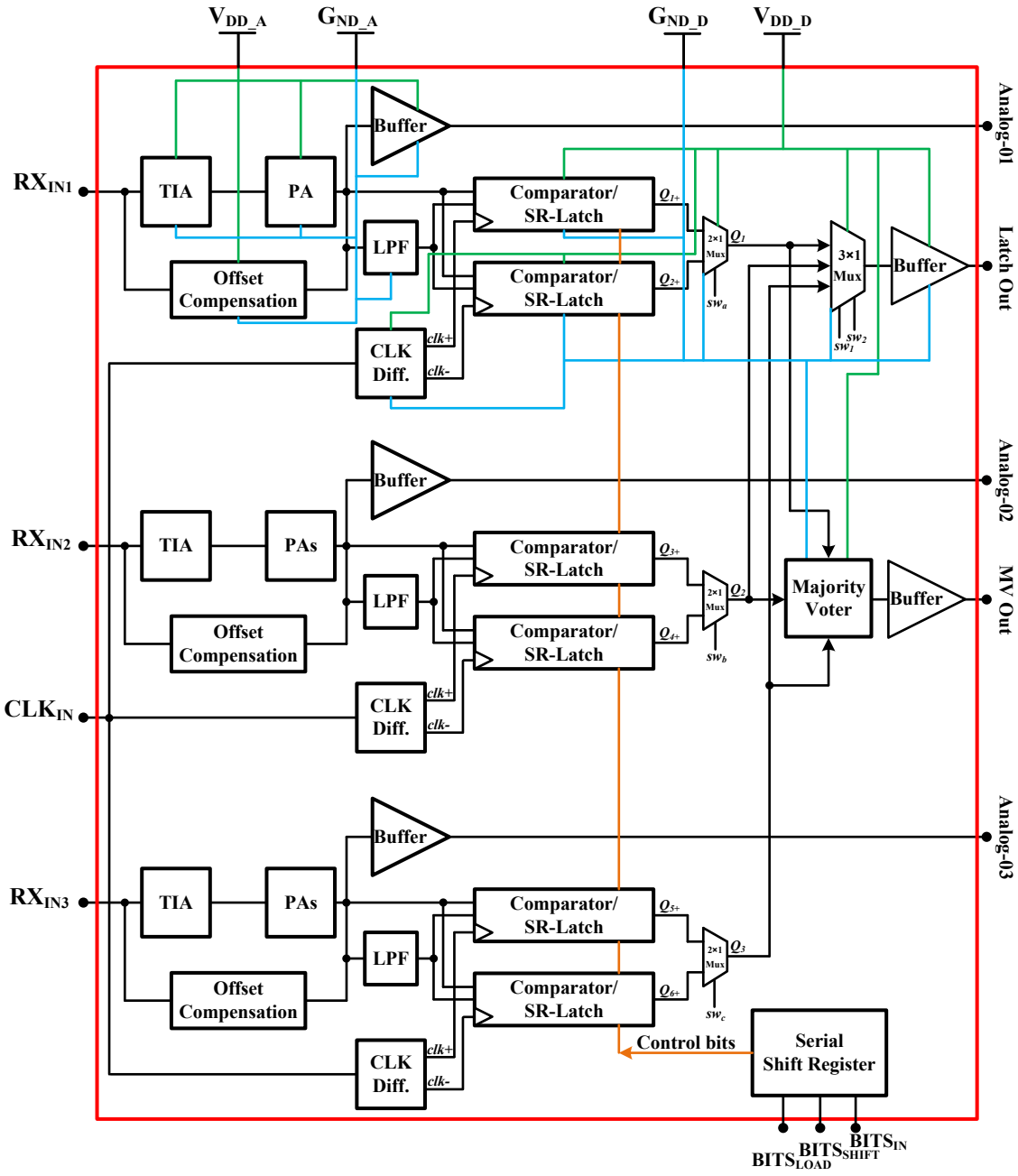


Figure 4.15: Overall schematic of the chip used for fabrication

which results in a distance of almost 400-micron meters between the sub-receivers digital output to the digital output pads on the right side of the chip. Therefore, buffers are used at every 100-micron meter to make sure the accurate signal reaches the output pad.

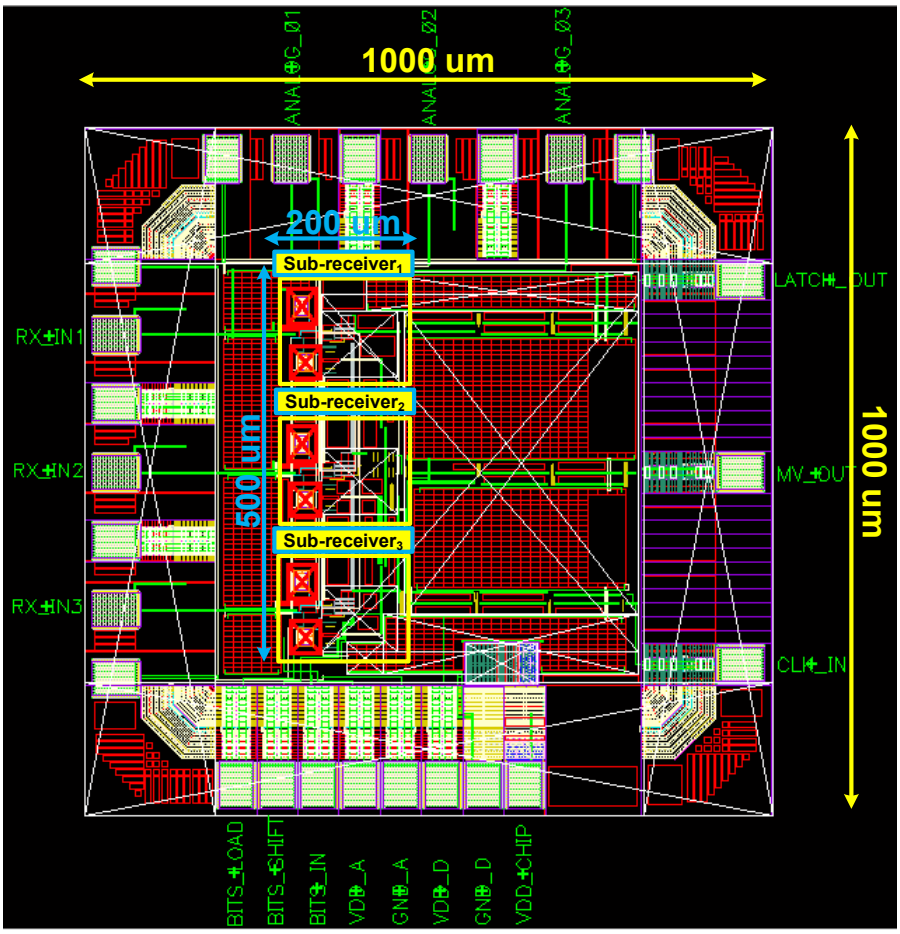
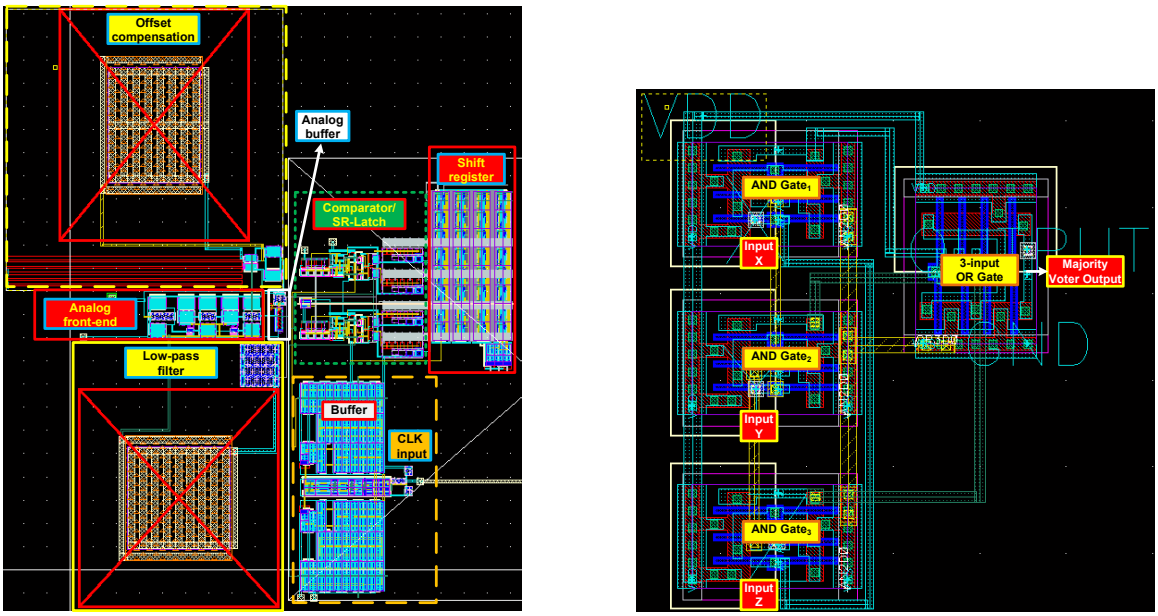


Figure 4.16: Tape-out of the proposed receiver

Since the proposed receiver contains three identical sub-receivers, each sub-receiver's latch must get well-synchronized clock input so that all the sub-receivers produce perfectly matched output signals in time. Therefore, the layout of the clock input is done very carefully to make sure that each sub-receiver receives well synchronized clock input as shown in Fig. 4.18. The length of the connecting wire from the Clk input to each individual sub-receiver is equal to $200\,\mu\mathrm{m}$. Buffers are used after every $100\,\mu\mathrm{m}$ of distance as the total distance from the chip's clock input pad (Clk In) to the latch's clock input is more than $400\,\mu\mathrm{m}$. Simulation results of the latch's clock input signal



(a) (b)

Figure 4.17: (a) Layout of the receiver sub-blocks , (b) Layout of the majority voter

clk+ (CLK-1, CLK-2, CLK-3) and clk- (CLK-INV1, CLK-INV2, CLK-INV3) are shown in Fig. 4.19 and 4.20, respectively. The delay from the chip's clock input pad to the latch's clock input is 178.6 ps.

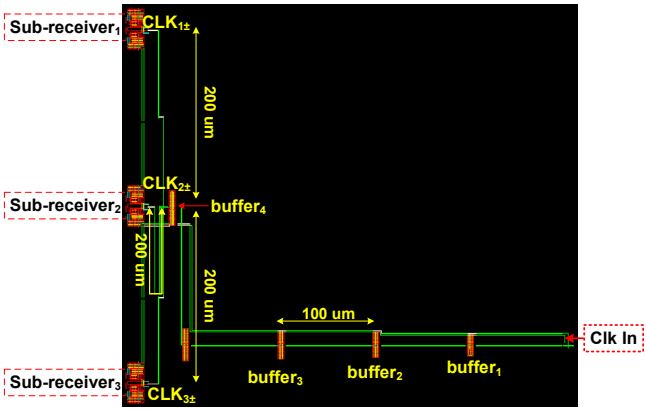


Figure 4.18: Layout of synchronized clock input for each sub-receiver

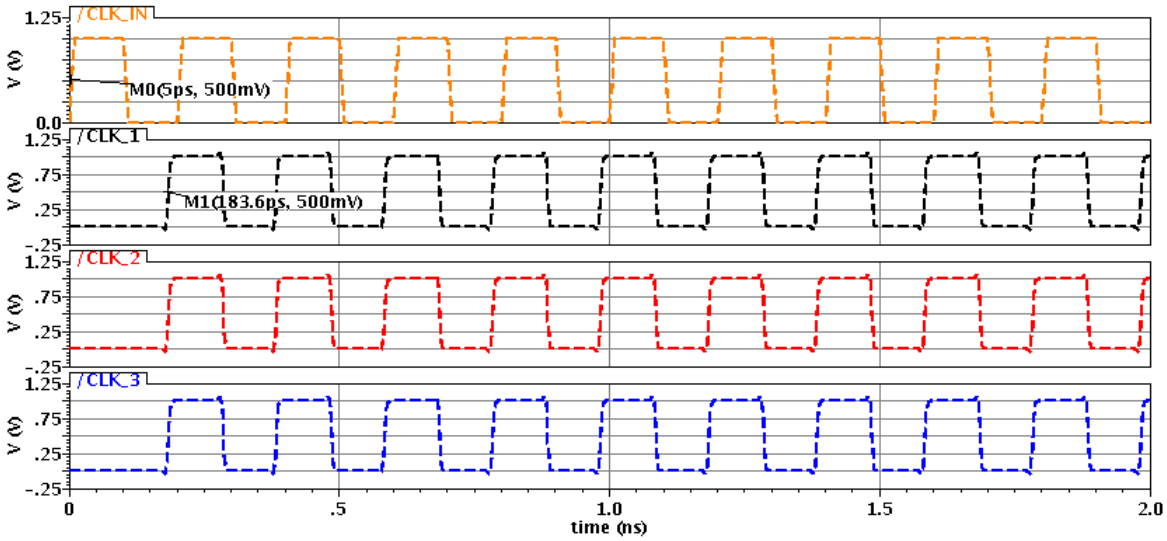


Figure 4.19: Simulation result of clock input signal clk+

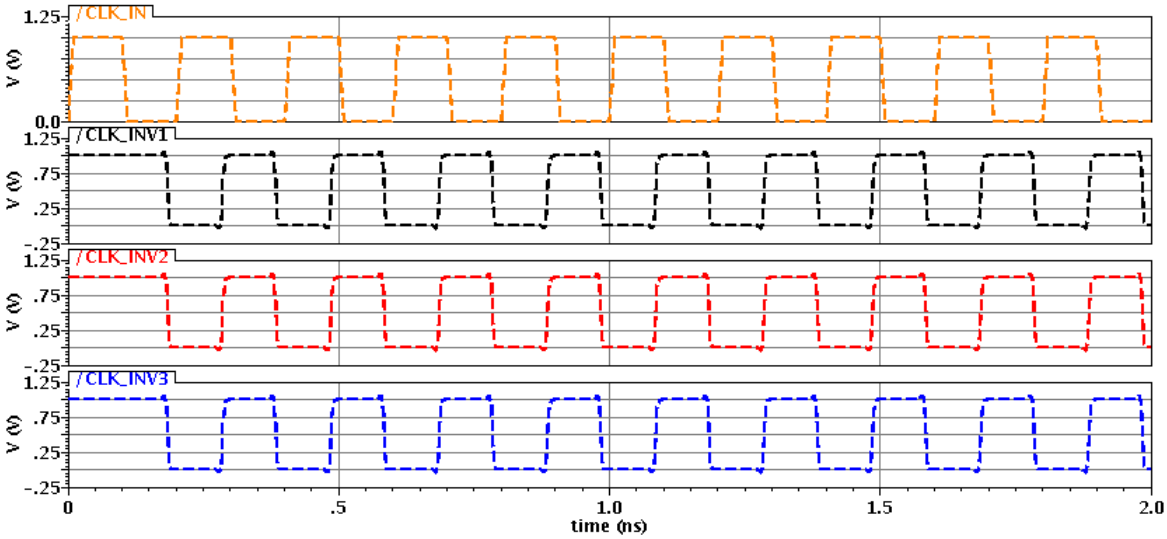


Figure 4.20: Simulation result of clock input signal clk-

4.4 Conclusion

A comprehensive discussion of the simulated results of the reference design and the proposed design is presented. The proposed receiver using a triple modular redundancy and an impedance scaling technique is successfully implemented. It achieved the transimpedance gain of 83.18 dB, the bandwidth of 7.2 GHz, input-referred noise current of 0.93 μA_{rms}, and consumed total power of 33 mW. It obtained a vertical eye-opening of 207 mV_{pp} with an input current of 15 μA_{pp}. Furthermore, the proposed receiver achieved a minimum input current sensitivity of 13.4 μA_{pp} for the BER of 10^{-12} at a data rate of 10 Gb/s. The originality of the proposed receiver is shown by SET simulations where an error caused by SETs is successfully removed with a limitation that only one sub-receiver experiences a particle strike at a given unit interval. By applying an impedance scaling, the proposed receiver is robust to SET errors, with no increase in power dissipation but at the cost of 0.8 dB optical power penalty relative to the reference design. To the best of the authors' knowledge the proposed idea of SET tolerance has not been implemented before in optical receivers. Finally, the layout design of the fabricated chip is also presented and discussed.

Chapter 5

Conclusion

5.1 Thesis Highlights

A new single event transient tolerant optical receiver is proposed and implemented in a $65\,\mathrm{nm}$ CMOS process at data rate of $10\,\mathrm{Gbit\,s^{-1}}$ for intra-satellite communication. The proposed receiver used a triple modular redundancy technique with a majority voter for radiation hardening. An idea of TMR is applied by splitting a reference photodiode into three sub-photodiodes. Thus an overall optical input is equally divided into three. Similarly, a conventional (reference) optical receiver is also split into three identical sub-receivers in parallel where each sub-receiver gets 1/3rd of an overall optical input and a final output is obtained through a majority voter. An impedance scaling technique is used to maintain the gain, bandwidth, and overall power dissipation similar to the reference design.

The conventional optical receiver exhibits bit errors caused by SET when it is exposed to ionizing radiation while the proposed receiver rejects SET and removes the bit errors at the output of the majority voter. The effectiveness of the proposed receiver comes with a limitation that only one sub-receiver experiences a SET in a given unit interval. The overall receiver suffers a bit error if at least two sub-receivers generate a bit error as the erroneous bit propagates to the output. By applying the impedance scaling technique, the proposed receiver is robust to SET errors with no increase in power dissipation but at the cost of $0.8\,\mathrm{dB}$ optical power penalty relative to the reference design. The DRC and LVS clean layout of the proposed SET tolerant optical receiver is also designed in

$65\,\mathrm{nm}$ CMOS technology. The chip is fabricated in an area of $1\,\mathrm{mm}^2$.

5.2 Future Work

This section presents several future directions to extend the study presented in this thesis.

(1) The proposed optical receiver was SET tolerant but at the cost of $0.8\,\mathrm{dB}$ sensitivity degradation. It provides an opportunity to proceed with the research work for an improvement of the receiver's sensitivity.

(2) The circuit-level triple modular redundancy radiation hardening technique is used in the proposed design. The combination of the circuit level hardening method and layout-based hardening techniques such as enclosed gate layout transistor is a promising work to improve the robustness of integrated circuits.

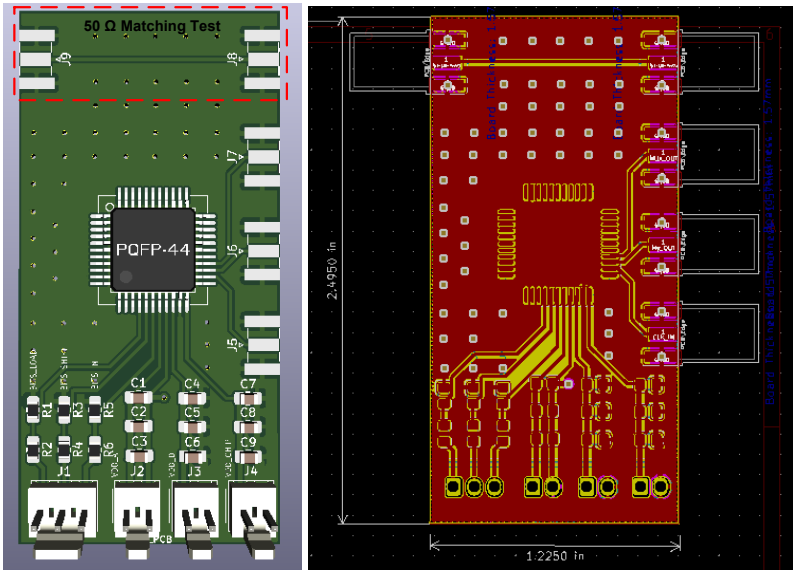
(3) The SET tolerant optical receiver is designed, simulated, and fabricated in the $65\,\mathrm{nm}$ CMOS process. The research can proceed in the future to carry out the real-time SET measurements of the chip to evaluate its immunity to radiation particles.

(4) The SET simulations of the proposed receiver used an ideal current source with a double exponential current pulse. However, it does not provide sufficient information such as the total charge deposit on the node and LET by the radiation particles. Therefore, it could be a good approach to use the 3D simulation tools such as TFIT (Transistor level Failure In Time) which provides the facility for the analysis of components sensitivity to the soft errors.

Appendix A

A.1 PCB Board and Wire-Bonding Diagram

The design of four layers (Signal, $\mathrm{GND}_{\mathrm{analog}}$, $\mathrm{GND}_{\mathrm{digital}}$, Signal) printed circuit board is shown in Fig. A.4 and the wire-bonding diagram of the chip packaging is presented in Fig. A.1. The chip is packaged in a 44-pin Ceramic Quad Flat Pack (CQFP). A GSGSGSG probe will be used to provide the input signals on the chip while the clock input and digital signal will be obtained through Sub-Miniature version-A (SMA) connectors. Furthermore, bypass capacitors of values $1\,\mu\mathrm{F}$, $1\,\mathrm{nF}$, and $1\,\mathrm{pF}$ are connected between supply voltage and ground while resistors of 1 KΩ and 4 KΩ are used in parallel to provide the 50 Ω impedance matching to micro-controller's output.



(a) (b)

Figure A.1: Printed circuit board Design (a) Top View, (b) footprint

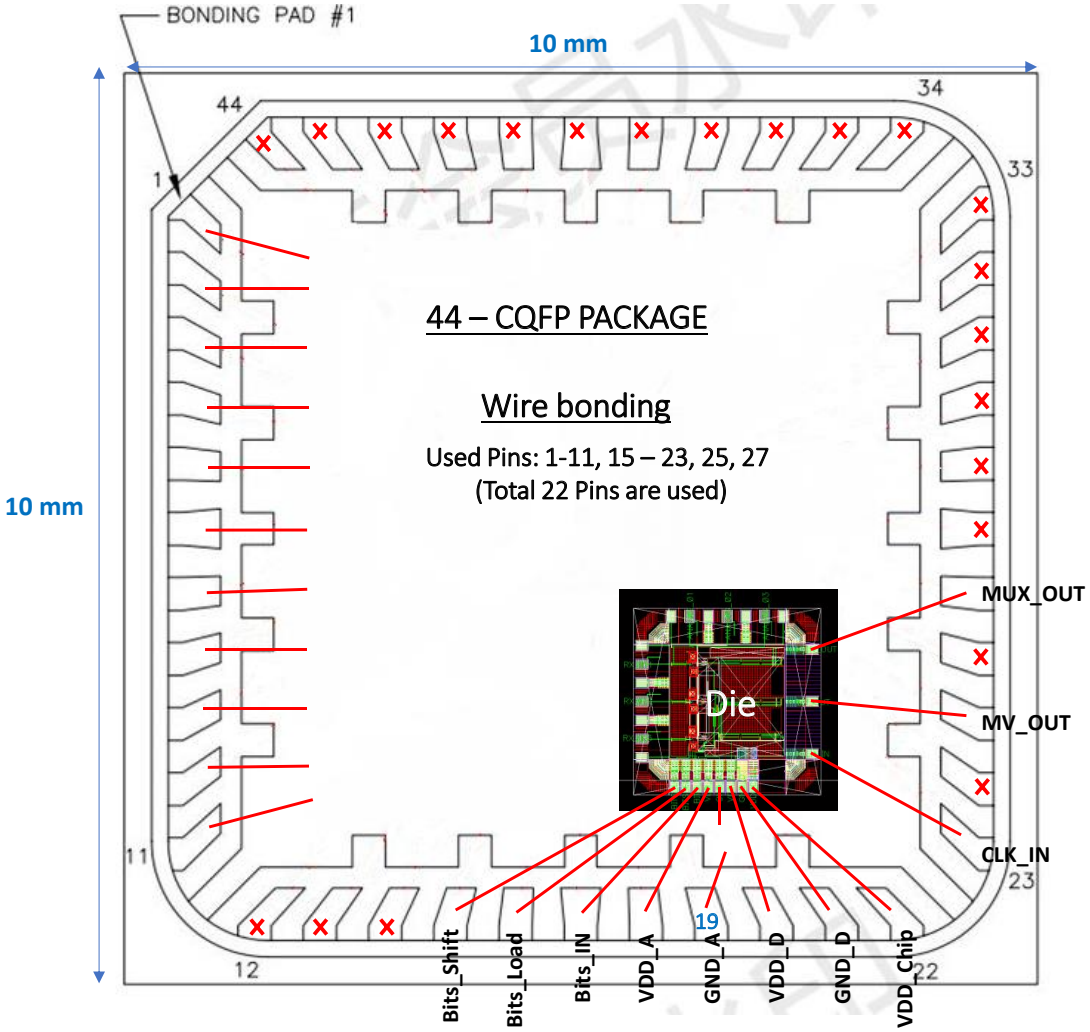


Figure A.2: Wire bonding diagram of the chip package

A.2 DRC and LVS Check

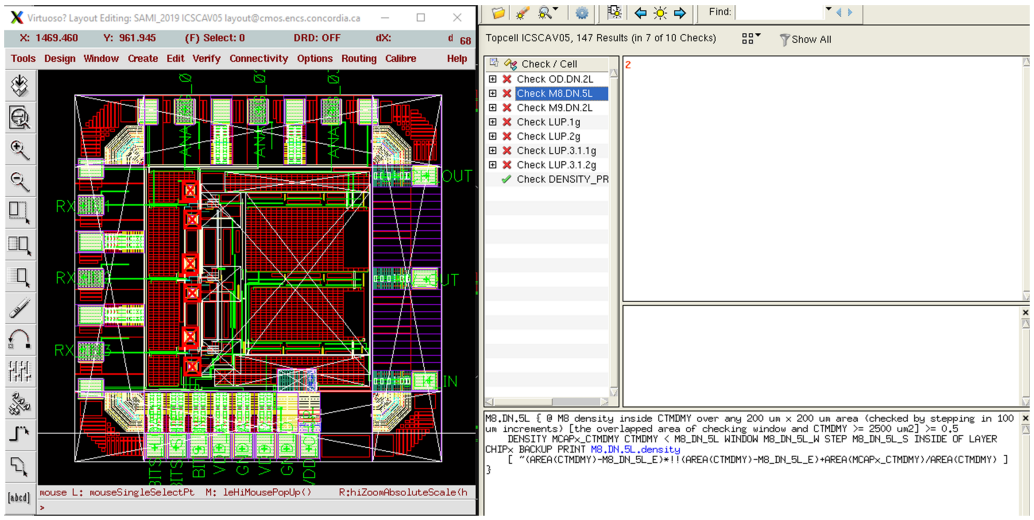


Figure A.3: DRC check of the fabricated chip

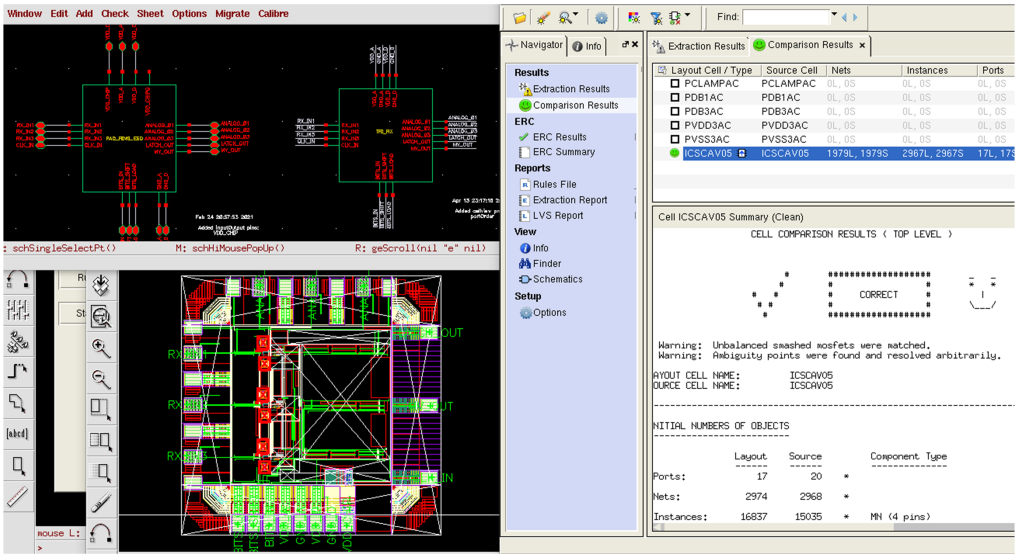


Figure A.4: LVS check of the fabricated chip

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