Induction Machine Emulation for Supply Faults

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ABSTRACT

Induction Machine Emulation for Supply Faults

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Power hardware-in-the-loop (PHIL) is increasingly being recognized as an effective real time emulation technique to mimic electrical dynamics of machines with the help of real time digital systems using real time simulator like Opal-RT, RTDS, D-space etc. In PHIL machine emulation, a power electronic converter or a linear amplifier emulates the behavior of electrical machines which are used in several applications such as Transportation, Aerospace / Military, Automotive, e-vehicle, Grid and motor Applications. Using these emulation techniques, various complex control algorithms or different configurations of controllers/drives for electrical machines can be tested, and also allows the testing of complex control strategies of an ac microgrid with critical industrial machines.

The emulation techniques can be used to represent new machine prototypes thus reducing the time to market of the complete drive system significantly. That is prior to the installation of a physical machine, testing of an electric drive or micro grid can be done with the help of a real time machine emulator. Therefore, if the drive controller fails, it will not jeopardize the life of a costly machine. Different loading profiles can be tested. In addition, a PHIL based machine emulation can be particularly useful to emulate faulted machine behavior. A machine undergoes wear and tear and may develop faults such as winding faults, bearing faults, or rotor eccentricity etc. If such machines are being emulated, their corresponding impact on the driving inverter, controller and power system can be studied without implementing these faults on a healthy motor. In fact, these emulation related research areas explore the feasibility of employing a real machine under such atypical conditions. Furthermore, machine emulation also provides an idea of detecting specific faults in advance.

The main research areas focused on this research are development of machine models of high accuracy, development of an emulator controller to attain dynamic current/voltage tracking capability and research in emulator configuration. Several atypical conditions are considered including short circuit faults, open circuit faults and switching faults. The mathematical models

are developed considering the machine steady state and transient behavior under starting and different fault operating conditions of the machine. The emulator chosen is a linear amplifier, because of its high bandwidth and performance. However, in comparison to a low bandwidth switched power amplifiers, it also possesses maximum current limitations. The emulator control strategies consider the abnormal conditions to which the machine is exposed. Hence, the emulator in this research work can replace the real machine effectively. Also, this method of emulation can be applied to any machine such as permanent magnet synchronous machine, synchronous reluctance machine, wound rotor induction machine etc. Especially, when the machine is rated in the MW power range, the developed emulator can be used with scaled down parameters.

In this PhD work, the main components in the emulator test bench include a real time system, back-to-back converters or linear amplifiers, link filters, required sensors and the grid. The developed IM emulator test bench can be used for studying the performance of the grid or drive control system for various grid faults, drive faults and other severe transient conditions. To validate the designed machine emulator system and its control philosophy, results are taken with a real 5 hp machine under same transient conditions.

On the other hand, this PHIL technology is also employed for grid emulation. An interface algorithm in the power hardware in the loop determines the accuracy and stability of emulation. Conventionally, this PHIL setup uses the ideal-transformer-method (ITM) as an interface algorithm between the device-under-test (DUT) and the real-time grid simulation model. The closed-loop PHIL interface with the DUT is usually stabilized using low-pass filters in the feedback path. Such filters stabilize the closed-loop PHIL interface, but with compromised accuracy. To improve the accuracy of the PHIL interface, this research work presents a method to design an optimal feedback compensator. This method depends on the type of physical filter topology used for the device under test.

To summarize, this research work represents 1) different induction machine emulators for different conditions of the grid and drive converters. This includes grid faults and test drive faults. 2) A grid emulator is designed with PHIL technology to test balanced and unbalanced resistive loads, islanding and grid connected modes of a distributed energy source (DER). The results obtained from the analysis and simulation for machine emulation and grid emulation are validated experimentally.

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Chapter 1 Introduction

The Industrial -sector largely depends on induction motors because of its robustness, high-power density, high-torque density, shock resistance, reduced acquisition and maintenance costs, safe operation, low vibration, and acoustic emissions. Over the past 15 years, Permanent Magnet Synchronous Machines (PMSMs) are being replaced by Induction Machines (IM) in newer rail vehicles like the Tokyo metro [1]. This is due to several disadvantages posed by PMSMs such as demagnetization of magnets by high currents and/or temperature, the need of one traction inverter per motor, and special care to handle faults [2], [3]. Similarly, the other motors specified in the Table 1.1, also cannot overcome the ranking of IM especially in case of rolling stock architectures and electric railway traction systems. Table 1.1 compares various types of motors for railway traction and each of them is graded from one to five points, where five points is the highest [4].

Table 1.1. Comparison of traction motors for rolling stock [4]

Parameter	**DC**	**SM**	**IM**	**PMSM**	**SRM**	**SynRM**
Maximum Speed	3	3.5	5	3.5	4.5	4
Torque Density	3	4	3.5	5	3.5	4
Efficiency	3.5	4	3.5	5	3.5	4
Controllability	5	4	5	4	3	3.5
Reliability	2	4	4.5	4	5	5
Cost	4	3.5	5	3	4	4.5
Σ Total	20.5	23	27	24.5	23.5	25

For high power applications such as traction, the controller of the drive, the drive inverter and the traction motor need to be tested before commissioning. Hence conventionally, the real machine drive is tested is with an associated risk of damaging the real machine. Therefore, the concept of 'machine emulation' is brought in this research.

"Emulation" is the process of mimicking the outwardly behavior of a system under target, while this emulation mechanism does not have to accurately reflect the internal state of the target necessarily. However, the concept of simulation involves modelling the underlying state of the target. The final result of good simulation essentially emulates the target which it is simulating, but in non-real time platform (Example: Matlab /Simulink, PSCAD, PSIM etc.,).

Earlier in 1960s the conventional process of emulation was to perform emulation with a prototype of machine is chosen by laws of similitude [5] but owing to its difficulty in scaling the mechanical parameters such as moment of inertia and coefficient of friction the process became obsolete. Hence allowing the present trend to choose power electronic systems as emulators to mimic electrical dynamics in emulators because of their speed and accuracy leading to power-hardware-in-the-loop (PHIL) technology based machine emulator system.

1.1 Literature Overview

In this section, a detailed review of comparison between the classical and evolving methods of drive system testing with PHIL emulation technique is discussed. The objectives of testing grid with the emulator are also detailed. Further, a comprehensive study of testing severe source fault transients with the machine emulator is presented. Finally, in contrast to the machine emulation, emulation of grid and its necessity is elaborated.

1.1.1 Testing Strategies of Electric Drives

Electric drives are usually tested with electrical motors or generators. For example, manufacturers of inverters will normally test prototype and preproduction equipment with an induction motor. This, motor may not always have the desired characteristics for a particular test. The same arguments apply for generation applications which utilize power electronic conversion equipment. It is also the case that, in some testing situations, the manufacturer may wish to include additional characteristics of the mechanical load or prime mover [6]. It can reduce the life of the machine. Another disadvantage of this orthodox testing is it needs a longer time to gather all the

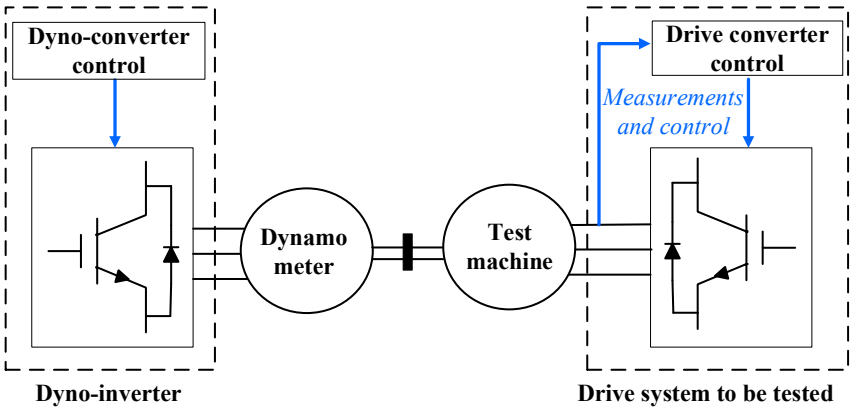


Fig. 1.1. Conventional drive system testing.

subsystems of the entire drive system of Fig. 1.1, namely IM, dynamometer machine, and drive, the variable speed drive and the drive inverter controller, which could be manufactured at different locations by different companies, and with different lead times. Furthermore, sometimes, it is needed to have a compromise with the ratings of the various subsystems such that the full rated conditions of the drive are not tested.

Hence, to overcome the above difficulties presented by the conventional testing methodology, a new technique called PHIL based electric drive testing was discussed in [6]-[14]. This PHIL simulation is an emergent method for emulation experimentation, wherein a power electronic converter is used to emulate an electrical machine simulated in real time and interfaced to a device under test. The feedback response from the physical device, such as voltage or current and the corresponding control signals given by real time system (RTS), are then used to complete the PHIL loop, providing a means for the physical device (which is power electronic converter here) to fully interact with the simulated machine/environment shown in Fig. 1.2.

The significant subsystems of the emulator test bench include a real time system processing the machine's mathematical model and an emulator control algorithm, back-to-back converters or linear amplifiers and link filters, which together form a virtual machine coupled to the test inverter or the test grid with required sensors. The RL link filter in the emulator setup plays its important role to allow a power flow between the voltage source and voltage source emulating converter or linear amplifier output terminals (set in voltage control mode) in order to draw the required amount of current. The resistance (R) in the RL link filter is the internal resistance of the inductor (L).

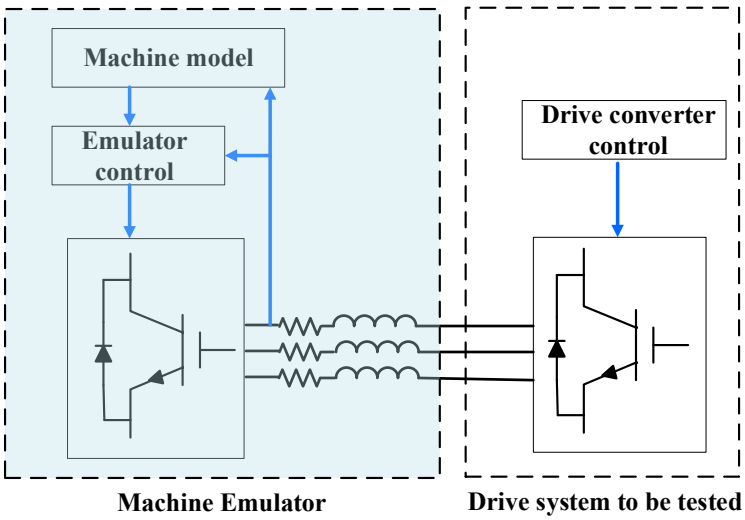


Fig. 1.2. Emerging PHIL based emulation for supply system testing [6].

The test setup with the virtual machine includes the above-mentioned subsystems shown in Fig. 1.2 called an "emulator" in this report, enables one to test the drive and its control thoroughly for early detection of defects in its control and operation.

The link inductors shown in Fig. 1.2 have two major effects on the performance of the virtual machine [6]. First, as they are considered while designing the current control loops, they will affect the transient response of the virtual machine. At the same time, the inductance value also affects the level of ripple in the current drawn from the test inverter. Therefore, higher values of link inductance results in more effective decoupling of the switching effects of the virtual machine's power converter and the test drive inverter.

With the use of such a PHIL based machine emulator test bench, several machine mathematical models can be emulated. Literature review shows emulation of induction machines [7]-[10], permanent magnet synchronous machines [11], [12], and switched reluctance machines [13], [14]. In addition, several emulators for those different machines can also be developed under common conditions namely starting, loading etc., and uncommon conditions such as grid faults, machine faults, and test drive faults, etc.

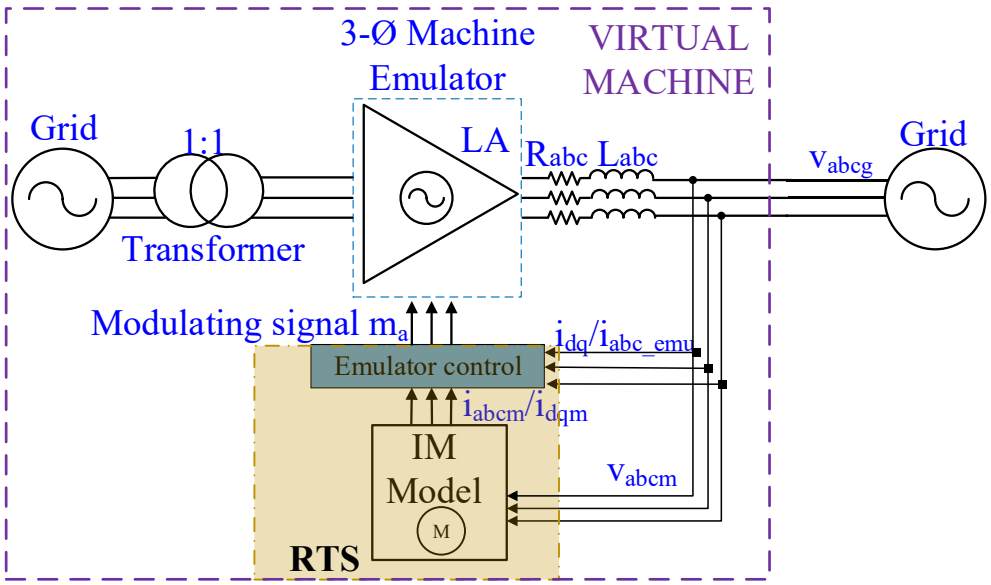


Fig. 1.3. Emulator configuration for testing grid.

1.1.2 Test Grid

A similar concept of drive system testing is applicable to testing the grid. The machine emulator in Fig. 1.2 is essentially interfaced with the grid. In an isolated grid or remote grid operations, this type of emulation helps in testing the performance of the grid. Especially, ac microgrids are increasingly popular now and are becoming a way of integrating renewable energies. They are usually operated in remote locations. It is discussed in detail in [15], that the control of microgrid involves complex control strategies under various transient conditions such as fault or loading transients. The emulator developed in this research work would enable the distribution system network operators to check or improve the implemented control techniques of the microgrid (during severe or common electromagnetic transients). The emulation can check the suitability of the machine at a particular bus in a chosen operating mode (islanding or grid connected mode).

The emulator configuration for testing the resilience of the grid/ micro grid control, is shown in the Fig. 1.3. High performance linear amplifiers (LAs) of a bandwidth of 200 kHz are used in this research replacing the bidirectional converter in the machine emulator of Fig. 1.2. However, the LAs do not possess high current/ power rating relatively.

1.1.3 Machine Emulation to test severe source fault transients

The machine emulator system in this work (Fig. 1.3) is used to test the performance of the grid or drive controller and drive inverter's performance for several operating conditions, thus proving the utility of machine emulation. The present thesis considers several source side faults into account. The main criteria for selecting the faults are based on the experience by the operators in the industries and power generation and transmission systems [16], [17], [18].

In industries/factories or especially in the traction industry, the induction machines are prone to several faults namely short circuit or open circuit grid faults and drive inverter faults and internal machine faults which may lead to severe damage to the system. The transient behavior of the machine is sometimes unpredictable. At the same time, restoration of the complex system is accompanied with time consuming fault diagnosis. It sometimes incurs heavy loss to the industry.

Hence, the PHIL emulation techniques in this context would help power system engineers or industrial engineers to come up with new control strategies for continued operation. These emulation techniques can also help to provide, identify, and memorize the respective fault signatures of currents, voltage, speed or torque, power etc. [19], [20], [21] for identification of faults (Fault diagnosis).

In this thesis, the faults at the source side of the emulator considered are grid faults and converter switch faults. source faults in this research include:

1. Shunt faults: asymmetric short circuit grid fault transients such as line to line, line to neutral, double line to neutral.
2. Harmonic grid voltages for 5, 7, 11, 13 orders and their combination with different proportion of THDs.
3. Series faults: asymmetric series impedance grid faults, asymmetric and symmetric open circuit grid faults.
4. Drive inverter switch faults: malfunctioning of gate driver for a single switch, multiple switch faults.

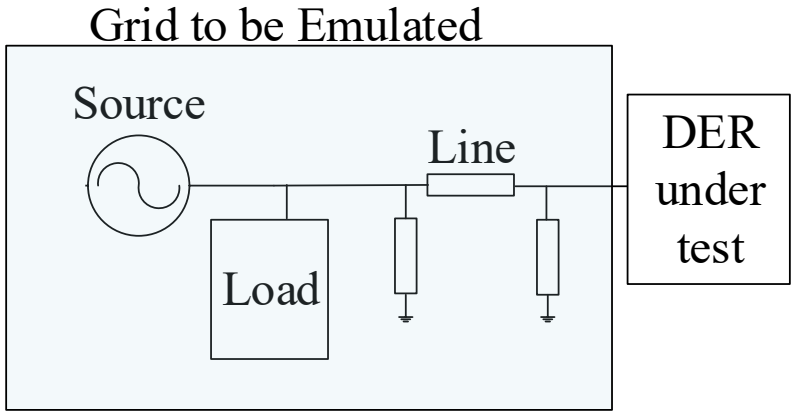


Fig. 1.4. Grid to be emulated with DER interface.

These faults are applied externally to the emulator to test the resiliency of the grid or drive inverter control. At the same time, the machine emulator efficacy is also verified in this research work. However, in contrast to the machine emulation to test the supply source for various unbalances, testing of critical loads is also necessary by emulating the source. It will enable the management of power to the load for continued operations. This will be discussed in the next section.

1.1.4 Grid Emulation

With the increasing penetration of industrial loads and distributed energy sources in the power grid, the grid characteristics alter and sometimes gets complicated. In case of running the industrial critical loads with an isolated/ micro grid, many factors must be taken into account for continued operation. Adding a distributed energy source (DER) to an existing grid/microgrid running a critical load can have significant impact on the DER. Especially in case of any unbalanced loads the impact on the DER is significant and needs to be studied. In order to investigate the performance of DERs, it is becoming necessary to emulate the grid behavior.

Fig. 1.4 describes the layout of the grid to be emulated with a DER interfacing. The emulation of the grid can be basically done in the following ways [22].

1. Scaling down the source, load, and line parameters of Fig. 1.4, by physical devices. It requires space to accommodate the three devices.

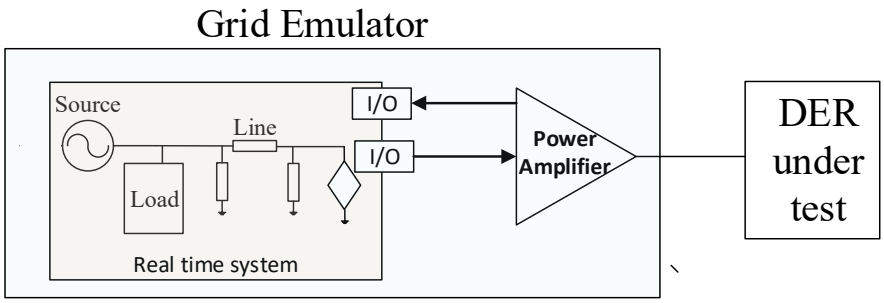


Fig. 1.5. PHIL interface algorithm-based grid emulation.

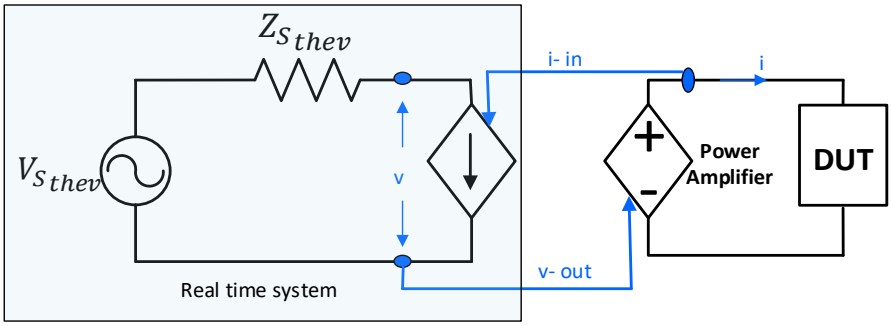


Fig. 1.6. Ideal transformer method interface algorithm with DER as device under test (DUT).

2. Using power electronics converters to emulate the electrical characteristics of source, load, and line impedances parameters. Here, each component is replaced by a separate power electronic converter. It therefore requires three control inputs.
3. Another concept is PHIL, in which the three grid components are realized in the real time system as shown in Fig. 1.5. In this case, the reference voltage output signal given by the real time system (RTS), controls the power amplifier. The sensed current signal at the DER is given back to the RTS which updates the simulation model. Therefore, the type of 'in and out' signals are chosen based on the adopted interface algorithm. There are several interface algorithms briefly discussed as follows:

A. Interface algorithms

An Interface Algorithm (IA) defines the types of the transmitted signals (e.g., voltage, current, power, torque, etc.) in a PHIL system and the ways in which the signals are being processed. An ideal interface algorithm with unity gain, infinity bandwidth, zero-time delay is not achievable or

affordable in practice. As the result, all PHIL simulations contain errors caused by the imperfection of the interface. Here are several interface algorithms [23],[24] listed below:

1. Ideal transformer method (ITM, v-type (VITM))
2. Ideal transformer method (ITM, i-type (IITM))
3. Time-variant First-Order Approximation (TFA)
4. Transmission line model (TLM)
5. Partial Circuit Duplication (PCD)
6. Damping Impedance Method (DIM)

The ideal transformer method (ITM) algorithm is one of the most conventional and straightforward methods of implementing a PHIL simulation. Depending on the type of the signals being amplified, it is categorized as either voltage-type ITM shown in (Fig. 1.6) or current-type ITM. The voltage-type (v-type) interface algorithm sends voltage out signals from the RTS to the amplifier and takes in current signals from the amplifier to the RTS as shown in Fig. 1.6. The current-type (i-type) is exactly converse to the v-type interface algorithm. In general, a PHIL system architecture can be illustrated as a Thévenin equivalent. Therefore, as depicted in Fig. 1.6, the grid voltage and the line impedance are the Thevenin voltage and impedance. In order to test the DER, the grid emulation with balanced and unbalanced loads are considered in this thesis. The ratio $\frac{Z_{Sthev}}{Z_{DUT}}$ is critical in analyzing the closed loop stability of ITM interface algorithm [24]. However, some modifications made to the control loop will enlarge the margins of stability.

Table 1.2. Comparison of different interface algorithms [25]

Interface Algorithm	Accuracy	Stability	Implementation ease
ITM	High	Low	High
TFA	High	Very low	Very Low
TLM	Low	High	Low
PCD	Very low	High	Medium
DIM	High	Medium	Medium

A comparative analysis is made for the mentioned interface algorithms [25] and is illustrated in Table 1.2, with high, medium and low standards. Considering the factors of ease of implementation and accuracy, with a reasonable compromise in stability, the ideal transformer method (v-type) is considered in this research for PHIL emulation of the grid. A detailed discussion of the interface algorithms other than ITM are discussed in [25].

1.2 Research Objectives

The fundamental objective of this thesis is to propose 1) a new induction machine emulator to test different source faults and 2) a novel grid emulator to test DER with unbalanced loads.

To accomplish these objectives, the research proposes, (i) improved mathematical models, improved emulator control structures, and new emulator configurations for machine emulation accuracy. (ii) change in the device under test (DUT) filter structures, addition of novel compensator transfer function in the control loop, for grid emulation stability and accuracy.

The objectives of this thesis are detailed as follows:

1) *Development of machine emulator:*

   This research work will aim to develop multiple machine emulator setups. Two configurations of machine emulator are targeted; (i) to emulate symmetrical transient conditions such as sudden speed change, sudden load change and asymmetrical shunt faults in the grid (ii) to emulate open circuit faults in the grid and drive converter. With the different emulator configurations proposed, investigations can be performed on the emulation with several induction machine models, and various emulator control strategies.

2) *Investigation of emulator control:*

   The emulator control methods change with respect to the conditions the machine emulator is exposed to. The objective of this thesis is to investigate (i) step by step improvements made to the emulator control strategies and (i) total elimination of the emulator control, with respect to the chosen source fault conditions and the machine model employed. For example, to emulate current during short circuit fault conditions, a voltage in| current out model (VICO) in the emulator configuration requires current control. To emulate voltage during open circuit fault conditions, a current in| voltage out model (CIVO) can directly input the voltage to the voltage-controlled power amplifier and can omit the emulator controller.

3) *Machine model accuracy:*

Machine model accuracy plays a key role in emulation accuracy. This work looks into different linear and nonlinear models of induction machines. VICO and CIVO type models for different source faults are discussed. The machine model accuracy is improved by integrating an accurate 'integration technique' into the modelling equations. Due to use of these detailed machine models, the machine emulator developed is capable of representing machine behavior even under severe transients.

4) *Emulation of machine behavior for fault transients:*

The developed machine emulator system is used to test various grid fault transients and drive converter fault transients. Modifications to the emulator control, machine models, and emulator configuration are proposed to ensure emulation accuracy. Fault signatures and fault reclosing operation strategies are presented.

5) *Emulation of grid:*

A new PHIL emulator configuration is proposed for the emulation of the grid. The closed loop stability improvement is made by adding a novel compensator in the control loop. The influence of change in DUT filter structure on grid emulation is detailed. The discussed ITM interface algorithm performance is investigated by considering various loading conditions and various short circuit ratios of the grid. A detailed mathematical analysis with validating results is made to ensure grid emulation accuracy.

1.2.1 Research Contributions:

The contributions of this PhD research work are summarized below.

- Development of a linear amplifier-based machine emulator system with grid interface.
- Investigation of a machine emulator control strategy.
- Emulation of different types of induction machine model with such as voltage in current out and current in voltage out linear and nonlinear models
- Emulation of various grid fault transients.
- Development of a linear amplifier-based machine emulator system with drive converter interface.
- Emulation of various converter switch fault transients.

- Development of interface algorithm-based grid emulator system interfacing DER.

Journal papers:

1. **G. Tanuku** and P. Pillay, "Emulation of an Induction Machine for Unbalanced Grid Faults," in IEEE Transactions on Industry Applications, vol. 57, no. 5, pp. 4625-4635, Sept.-Oct. 2021, doi: 10.1109/TIA.2021.3086083.
2. **G. Tanuku** and P. Pillay, "Induction Machine Emulation for Open Circuit and Short Circuit Grid Faults," in IEEE Transactions on Energy Conversion, 2022, doi: 10.1109/TEC.2022.3196850.
3. **G. Tanuku** and P. Pillay, "Induction Machine Emulation for Variable Frequency Drive Converter Faults," in IEEE Journal of Emerging and Selected Topics in Industrial Electronics, 2022, doi: 10.1109/JESTIE.2022.3195094.

Conference papers:

4. **G. Tanuku** and P. Pillay, "Induction Machine Emulation under Asymmetric Grid Faults," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2020, pp. 2351-2356, doi: 10.1109/ECCE44975.2020.9235830.
5. **G. Tanuku** and P. Pillay, "Emulation of induction machines subject to industrial grid harmonics," 2022 IEEE International Conference on Power Electronics, Smart Grid, and Renewable Energy (PESGRE), 2022, pp. 1-6, doi: 10.1109/PESGRE52268.2022.9715819.
6. **G. Tanuku**, P. Pillay "Induction machine emulation for extreme weather conditions" in IEEE PES,2022, accepted and presented for IEEE PES, 2022.
7. **Gayatri Tanuku**, K. S. Amitkumar, Jean-Nicolas Paquin, Syed Ahmed Raza Naqvi, Marija Stevic, Ravinder Venugopal "Ideal Transformer Method Optimization for Power Hardware-in-the-Loop Simulations of Grid-Connected Inverters" accepted and presented for PCIM Europe 2022.

1.3 Thesis Outline

Chapter 2 presents emulation of a 5 hp induction machine with a linear amplifier-based emulator. Different asymmetrical grid fault transients and loading transients are studied. It also proposes a methodology to implement emulation of a MW machine by a scaling down procedure. The accuracy improvement of a voltage in| current out mathematical model is proposed. A systematic

upgrade of the emulator control strategy is presented. The experimental emulation results presented are validated with a real machine.

Chapter 3 presents emulation of an induction machine for industrial grid harmonics. Different odd order harmonics that commonly occur are considered for emulation. The combination of the harmonics with different THD percentages in the grid is given to the emulator. The improvement in emulator control strategy, which is robust to the grid harmonics considered, is proposed. Finally, experimental results which validate the proposed concept are presented.

Chapter 4 presents induction machine emulation for open circuit grid faults. Two induction machine models are discussed to emulate the stator back-emf. A current in| voltage out induction machine model-II is proposed for emulating back-emf under open circuit. A change in emulator configuration with respect to model –II is also proposed. The experimental results to validate the proposed theory are presented for different open circuit faults.

Chapter 5 presents induction machine emulation for variable frequency drive converter faults. In this chapter, a comparison is made between a voltage in| current out model and a current in voltage out model. The appropriateness of using them is checked for different converter switch faults. The current in| voltage out model proposed is suitable for emulating various converter switch faults. The model also incorporates the physical emulator parameters. A change in emulator configuration is also proposed. Finally, the experimental results are presented to validate the robustness of the emulator.

Chapter 6 presents the grid emulation with the help of PHIL technology, using interface algorithms. An ideal transformer method interface algorithm is considered, and an improvement is proposed. A detailed mathematical analysis is presented. Performance improvement with different DUT structures and with different compensators are presented. Experimental result analysis for different balanced and unbalanced loads is presented.

Chapter 7 discusses the conclusion and future scope of this work.

Chapter 2 Emulation of an Induction Machine for Unbalanced Grid Faults

2.1 Introduction

Induction machines (IMs) are prevalent in several industrial sectors such as design or manufacturing, transportation, electrical power generation, etc. They are robust and reliable under various operating conditions and offer numerous advantages namely high power and torque densities, good controllability, low maintenance, and cost. Because of the absence of brushes and permanent magnets, induction machines offer safe operation even in hazardous environments as there is no sparking of brushes, unlike dc machines. The full-load efficiency for medium and large machines can range from 85 to 97% [26]. In the electric vehicle sector, induction machines are competitive owing to their advantages in comparison with the other machines namely permanent magnet synchronous machines and switched reluctance machines [4]. However, in contrast to the above advantages, they possess a low power factor during light load conditions and can require considerable reactive power. They also have high inrush currents during starting or fault transients which can affect the supply voltage. The time required for various electromagnetic transients to decay is high thus placing an additional burden on the supply source.

The IM drive capability or performance of the grid needs to be checked/tested for various contingencies before the intended machine is installed. This testing needs a physical machine [27], responding to various transients applied namely converter faults or controller faults, or grid faults. Such testing may damage an expensive machine. For testing specific loading conditions [27], different lead times exist to gather all the subsystems. Sometimes, full-rated conditions of the drive cannot be tested with insufficiently rated subsystems. Hence this shortcoming leads to the concept of development of a ‘virtual machine’ which is essentially called an ‘emulator’ in this research.

A power-hardware-in-loop (PHIL) system is an effective real time emulation technique to re-create a virtual machine. The power hardware in this technique is power electronic converters or linear amplifiers (LA) which are coupled to link filters as shown in Fig. 2.1. This hardware is controlled by real time control signals processed in real time systems (RTS) such as Opal-Rt, RTDS, D-space, etc., to mimic the electrical dynamics of a real machine. The control signal

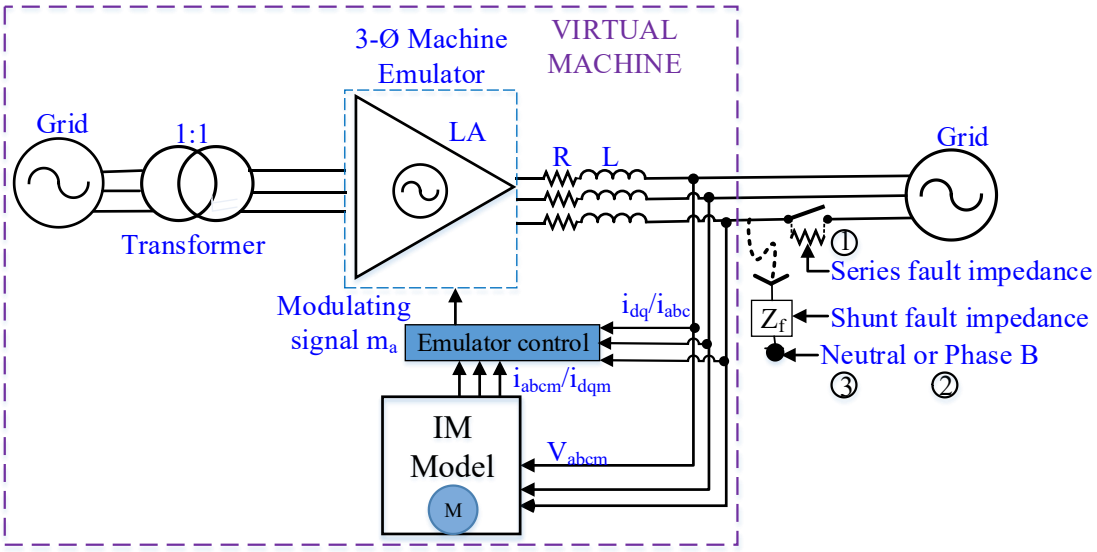


Fig. 2.1. Schematic diagram of machine emulator for grid faults.

Fault-1: Series-impedance fault; *Fault-2*: L-L fault with shunt-impedance; *Fault-3*: L-N fault with shunt-impedance.

generation is done by the emulator controller, processing the real time currents drawn by the power hardware, with respect to reference currents given by an accurate mathematical model of the machine [6]. There are numerous applications associated with this type of PHIL emulation such as transportation, aerospace and military, electric vehicles, grid, and motor applications [12], [15], [28], [29].

Considering grid applications, ac microgrids are increasingly popular and are becoming a way of integrating renewable energies. They are usually operated in remote locations. In this chapter, the induction machine emulation is chosen to be done with a grid interface. This allows testing ac microgrids which are very sensitive to fluctuations in load and generation. It is discussed in detail in [30], that the control of microgrids involves complex control strategies under various transient conditions. The microgrid control aims to maintain constant voltage and frequency while meeting real and reactive power demands. The emulator developed in this chapter can enable the distribution system operators (DSOs) to check or improve the implemented control techniques of the microgrid.

As per the literature survey on fault emulation, IM emulation for drive inverter faults is discussed in [31]. Emulation is also done for detection of stator inter-turn, broken bar faults, etc., with motor

current signature analysis (MCSA) in [32] and [33]. But the emulation of machines for grid faults has not been reported yet.

The distribution grid side faults are categorized as 'symmetrical' (balanced) or 'asymmetrical' (unbalanced) faults. Unbalanced faults such as line to neutral/ground have approximately 70% of occurrence while it is 15% for line to line and 10% for double line to neutral [34]. Series faults often occur because of a broken line or changed impedance level in one or more lines. In this chapter, unbalanced series faults and shunt faults are considered, during the emulation of the induction machine.

A comprehensive literature review has also been done on the emulation of different machines to choose the components of the emulator i.e., power hardware, coupling filter, type of controller, dynamic model of the machine, out of various possibilities as follows. [27] discusses induction motor emulation with a power electronic converter with an LCL filter and a transformer based complex coupling. Therefore, high frequency switching ripples, traveling, and reflected waves are eliminated. Nevertheless, [35], [36] employed a simple RL-coupling interface with bidirectional power converter with better accuracy. Three phase linear power amplifiers (LAs) are chosen as the emulator in [37] for high-speed tracking accuracy because of the high open-loop bandwidth. However, it is observed that the LAs can only be operated at a lower power range compared with that of the bidirectional converters employed in [27], [35], and [36] with operating power in kW. A proportional-integral (PI) control-based emulator is connected to drive converters in [27], [31], [35], [37] to control the direct and quadrature currents. In [36], a proportional resonant (PR) control-based emulator is directly coupled to the grid to control the three sinusoidal currents, but the usage of PR control is not justified. Even though the emulator is connected to the grid, no other transients are discussed except for direct online startup. In [35], [36] and [38], improvements in the accuracy of the dynamic machine models are done with the inclusion of effects of nonlinearities given by finite element analysis methods during motor starting. It is also observed that in all the emulation related reference papers, emulation of different machines under different transients is done at laboratory power level (kW) but not in terms of megawatt (MW). But many machines used in industries are MW sized machines and also require testing, before they are prototyped. But the MW machines cannot be easily emulated with laboratory power equipment. Testing of such machines poses a challenge and incurs huge wastage of power.

In view of the highlights and challenges from the above literature survey, a three-phase squirrel cage induction machine emulator test-bench is developed with a grid interface [39] as shown in Fig. 2.1. An RL-link filter of 3 mH and high-performance linear amplifiers of 200 kHz bandwidth are chosen. An Opal-Rt real time system with an accurate mathematical model, along with an appropriate controller is implemented to control LAs. For galvanic isolation between the grid and emulator to avoid circulating currents, an isolation transformer is also included. Resistive load banks are chosen for application of unbalanced faults impedances.

With respect to the maximum current rating limitation of LAs (20 A), the virtual machine operates at a reduced voltage during the test for the machine's faulty conditions. The series and shunt fault impedances for asymmetrical faults are chosen deliberately to protect the grid and linear amplifiers under high short circuit currents. A standard SOGI phase-locked-loop [40] is chosen for generating the phase-grid angle required for abc to dq transformations.

The center of attention of this research is to design an emulator which serves as a tool for testing cage induction machines under different asymmetric grid fault transients. This has been done by

(i) Choosing an accurate mathematical model which is described in section 2.2.

(ii) Enhancing the emulator control with combination of PI and PR controllers. The control addresses the causes and effects of the negative sequence components in the motor currents during asymmetric grid faults. An in-depth mathematical analysis and design concepts are demonstrated with necessary suggestions in section 2.3.

(iii) Addressing the testing of MW machines with this proposed emulator by scaling down the MW machine parameters to laboratory machine's power level with the help of per unit transformation is elucidated in section 2.4.

(iv) Comparison of the experimentally obtained electrical fault dynamics of the emulator with that of the real machine to check the capability of the emulator is shown in section 2.5. Thus, the emulator efficacy is verified for all different combinations of series and shunt impedance grid faults.

2.2 Mathematical modeling of the induction machine

In this section, dq modeling of the induction machine is used in the synchronous reference frame. The machine stator windings are star connected with isolated neutral. Hence the zero-sequence component of current does not find a path to flow.

The generalized dq mathematical model of an induction machine is given by the following equations from Fig. 2.2.

$$v_{qs} = r_s i_{qs} + \omega\lambda_{ds} + p\lambda_{qs} \tag{2.1}$$

$$v_{ds} = r_s i_{ds} - \omega\lambda_{qs} + p\lambda_{ds} \tag{2.2}$$

$$v'_{qr} = r'_r i_{qr} + (\omega - \omega_r)\lambda'_{dr} + p\lambda'_{qr} \tag{2.3}$$

$$v'_{dr} = r'_r i_{dr} + (\omega - \omega_r)\lambda'_{qr} + p\lambda'_{dr} \tag{2.4}$$

where $v_{qs}, v_{ds}, i_{qs}, i_{ds}, \lambda_{qs}, \lambda_{ds}$ are quadrature and direct axis voltages, currents, and flux linkages, respectively.

The discretized state-space model integrated with trapezoidal integration is employed in this chapter, by rearranging the generalized equations (2.1) to (2.4). This would lead to a voltage-in current-out state-space model represented in Fig. 2.3. It is described by the following equations (2.5) to (2.8).

$$\bar{I}(k) = A_{IM}\bar{I}(k) + B_{IM}\bar{U}(k) \tag{2.5}$$

To attain the correct current output from the state-space model, choosing an accurate integration method plays a role [10]. The input to the integrator in Fig. 2.3 ($\dot{\bar{I}}(k)$) is time-dependent and operated at a larger time step. This is predominant when the model is employed in the stationary reference frame or when $\bar{I}(k)$ becomes oscillatory in the synchronous reference frame. Therefore, from the popular integration methods such as forward Euler, backward Euler, and Trapezoidal, the best integration method is Trapezoidal [41], [42] and is explained below.

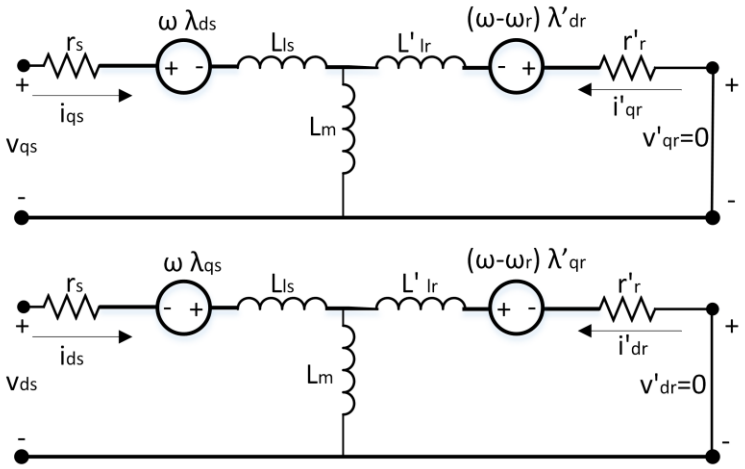


Fig. 2.2. The dq equivalent circuit of IM.

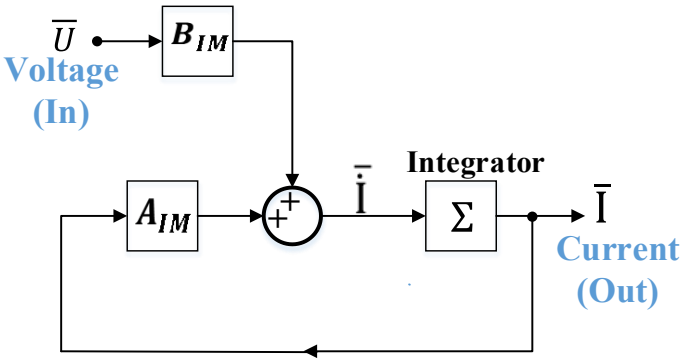


Fig. 2.3. Voltage-in Current-out configuration of state space model.

For the output of the integrator $\bar{I}(k)$ and for the input $\dot{\bar{I}}(k)$, the output of Euler's integrator is given by (2.6) and that of the Trapezoidal integrator is given by (2.7), for a sampling period T_S. In the Trapezoidal method, the output depends on the average of present and past samples of input unlike in the Euler's which depends on the past sample of input. This improves the integration accuracy.

$$\bar{I}(k) = \bar{I}(k-1) + T_s\dot{\bar{I}}(k-1) \tag{2.6}$$

$$\bar{I}(k) = \bar{I}(k-1) + \frac{T_s}{2}\left(\dot{\bar{I}}(k) + \dot{\bar{I}}(k-1)\right) \tag{2.7}$$

By substituting (2.5) for sample instants k and $k-1$, in the above equation (2.7), gives (2.8).

$$\bar{I}(k) = \left(1 - \frac{A_{IM}T_s}{2}\right)^{-1}\left(1 + \frac{A_{IM}T_s}{2}\right)\bar{I}(k-1) + \frac{\left(1 - \frac{A_{IM}T_s}{2}\right)^{-1} B_{IM}T_s}{2}[\bar{U}(k) + \bar{U}(k-1)] \tag{2.8}$$

$$A_{IM} = \begin{bmatrix} -\frac{L_r R_s}{D} & \frac{\omega_s L_s L_r - \omega_r L_m^2}{D} & \frac{L_m R_r}{D} & \frac{\omega_s L_r L_m - \omega_r L_r L_m}{D} \\ \frac{-\omega_s L_s L_r + \omega_r L_m^2}{D} & -\frac{L_r R_s}{D} & \frac{-\omega_s L_r L_m + \omega_r L_r L_m}{D} & \frac{R_r L_m}{D} \\ \frac{R_s L_m}{D} & \frac{-\omega_s L_s L_m + \omega_r L_s L_m}{D} & \frac{-L_{ss} R_r}{D} & \frac{-\omega_r L_s L_r - \omega_s L_m^2}{D} \\ \frac{\omega_s L_s L_m - \omega_r L_s L_m}{D} & \frac{R_s L_m}{D} & \frac{\omega_s L_m^2 - \omega_r L_s L_r}{D} & \frac{-L_{ss} R_r}{D} \end{bmatrix}$$

$$B_{IM} = \begin{bmatrix} \frac{L_r}{D} & 0 & -\frac{L_m}{D} & 0 \\ 0 & \frac{L_r}{D} & 0 & -\frac{L_m}{D} \end{bmatrix}$$

where, $D = \left((L_s L_r - L_m^2)\right)$, $L_s = L_{ls} + L_m$ and $L_r = L_{lr} + L_m$

Equation (2.8) is an amalgamation of Trapezoidal integration with state-space modeling. This mathematical model is claimed to give accurate results even for a larger time step of $T_s = 20\ \mu s$, when compared to other simple state-space models with Euler's integration. Especially, it is more compatible with real time simulators having constraints with high sampling periods for the process of emulation.

2.3 Asymmetric grid fault emulator and its control

2.3.1 Production of negative sequence components

In this chapter, unbalanced conditions are created safely on the grid side considering the maximum current capability of the chosen emulator. Therefore, shunt faults such as line to line, line to neutral and double line to neutral are applied with a selected shunt fault impedance. To attain sufficient voltage-drop during shunt faults, a series impedance fault is applied prior to the shunt faults. These asymmetrical series and shunt faults numbered 1, 2, and 3 respectively in Fig.

2.1, create imbalances in the applied voltages and currents. These imbalances can be realized mathematically into a positive sequence, negative sequence and zero sequence components.

The extent of the rise in the magnitude of negative sequence components along with the positive sequence current, calculated by equations (2.9) to (2.10), represents the level of asymmetry or unbalance.

$$I_{\ominus} = \frac{V_{\ominus}}{Z_{\ominus}} \tag{2.9}$$

$$I_{\oplus} = \frac{V_{\oplus}}{Z_{\oplus}} \tag{2.10}$$

$$\begin{bmatrix} V_{\oplus} \\ V_{\ominus} \\ V_0 \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \\ 1 & 1 & 1 \end{bmatrix} * \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{2.11}$$

where $V_{\oplus}$, $V_{\ominus}$, $I_{\oplus}$, $I_{\ominus}$, $Z_{\oplus}$, $Z_{\ominus}$are the positive sequence and negative sequence components of voltages, currents, and impedances for $\alpha = 1\angle 120^0, \alpha^2 = 1\angle -120^0$.

The sequence voltages are obtained by three-phase unbalanced voltages, according to (2.11). The magnitude of the negative sequence impedance during fault transients is the sub-transient reactance of the induction machine [43] which is equal to the locked rotor reactance and the magnitude of positive sequence impedance is taken as the quasi-steady state impedance during faults which depends on the magnitude of slip.

Therefore, the rise in asymmetry is indicated by an increase in the magnitude of negative sequence voltage from series to shunt fault transition. This increases the negative sequence current as well. This mathematical analysis will be validated in the result analysis done in section 2.5.

2.3.2 Effects of negative sequence components

During asymmetrical fault transients, the negative sequence stator currents rotate opposite to the direction of positive sequence stator currents at the fundamental frequency (f).

For the positive stator sequence currents, the rotor voltages and currents attain fractional-order frequencies (f_r) when the rotor is rotating at a slip (s) (2.12), (2.13).

$$f_r = sf \tag{2.12}$$

$$s = \frac{n_s - n}{n_s} \tag{2.13}$$

where n_s is the synchronous speed and n is the speed of the rotor in rpm.

But for the negative sequence stator currents, f_r will have almost twice the fundamental frequency, because the direction of rotor is opposite to the direction of rotation of negative sequence current which is rotating at a speed $(-n_s)$. This will result in torque and speed oscillations at double the supply frequency. However, the magnitude of speed oscillations is filtered out by the extent of the moment of inertia that the machine possesses.

Just like the rotor, the direct and quadrature axis currents in the imaginary synchronous reference frame rotate at the synchronous speed (n_s) in the direction of positive sequence components. This will have zero-relative speed, between the positive sequence currents and dq frame. Hence, i_d and i_q currents attain constant values i.e., with zero frequency. However, with respect to negative sequence components rotating at synchronous speed $(-n_s)$ during asymmetric faults, the $i_d$and $i_q$currents attain double the synchronous frequency (f). This can be mathematically derived with the abc/dq transformation (K_1) from the stator's sinusoidal positive and negative sequence currents.

$$K_1 = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta-\delta) & \cos(\theta+\delta) \\ \sin\theta & \sin(\theta-\delta) & \sin(\theta+\delta) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2.14}$$

where $\delta = 120^0$.

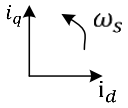
$$i(t) = i_1(t) + i_{h'}(t) + i_{h''}(t) + i_{h'''}(t) + \cdots \tag{2.15}$$

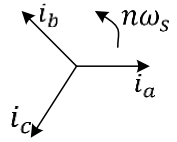
Additionally, the imbalance in the symmetry of voltages would result in distortion of the shape of the sinusoidal stator current. The reason behind this is the appearance of harmonics in addition to the fundamental given by (2.15).

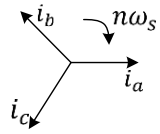
Table 2.1. Harmonics and their respective sequence

Sequence	**Harmonic order**			
+	1	7	13	19
-	2	8	14	20
0	3	9	15	21
+	4	10	16	22
-	5	11	17	23
0	6	12	18	24

Table 2.2. Behavior of $\boldsymbol{i_d}$, $\boldsymbol{i_q}$ currents for positive and negative sequence currents

<table>
<tr><td colspan="2"> 

Synchronous dq reference frame</td></tr>
<tr><td> 

n^{th} harmonic positive sequence current</td><td>Relative speed is
$n\omega_s - \omega_s = (n-1)\omega_s$
Therefore from (2.14),
$i_d = \hat{I}_{\oplus} \cos(n-1)\theta$
$i_q = \hat{I}_{\oplus} \sin(n-1)\theta$
Where $\hat{I}_{\oplus}$ is peak positive sequence current</td></tr>
<tr><td> 

n^{th} harmonic negative sequence current</td><td>Relative speed is
$n\omega_s + \omega_s = (n+1)\omega_s$
Therefore from (2.14),
$i_d = -\hat{I}_{\ominus} \cos(n+1)\theta$
$i_q = \hat{I}_{\ominus} \sin(n+1)\theta$
Where $\hat{I}_{\ominus}$ is peak negative sequence current</td></tr>
</table>

As depicted in Table 2.1, each individual harmonic current has its individual phase of rotation with respect to the fundamental. However, because of the unbalanced fault, a harmonic being considered as a positive sequence will also have its negative sequence and vice versa.

This opposite phase of rotation for each harmonic in the stator current results in the appearance of harmonics in i_d and i_q based on the relative speed between the sequence currents and the synchronous dq reference frame as illustrated in Table 2.2.

Therefore, the positive sequence current for $n = 1$ from Table 2.1, produces $i_d = \hat{I}_{\oplus}$, $i_q = 0$ as per Table 2.2. Similarly, the opposite (negative) sequence current of the same order $(n = 1)$ produces 2^{nd}order harmonics i.e., $i_d = -\hat{I}_{\ominus} cos2\theta, i_q = \hat{I}_{\ominus} sin2\theta$.

Similarly, for the harmonics of order 2, 4, and 5, 7 in the stator abc current with their natural sequence of rotation (Table 2.1) gives 3^{rd} and 6^{th} harmonics in dq currents, respectively. But the opposite sequences of the same harmonics (2, 4, 5 and 7) gives $1^{st}, 5^{th}, 4^{th}$ and 8^{th} harmonics in dq currents, respectively.

If the stator current during a fault is symmetrical about the x-axis but has a distortion in shape from that of the pure sine wave, it represents odd-order harmonics 3, 5, 7, 9, etc., in addition to the fundamental. The multiples of third-order harmonics are zero sequence currents according to Table 2.1 and do not possess any phase of rotation. Hence, they do not affect i_d and i_q currents. But the remaining odd harmonics result in $2^{nd}, 4^{th}, 6^{th}, 8^{th}$, ... harmonics in the i_d and i_q currents.

2.3.3 Emulator control approach

The real time emulator chosen in this project is a three-phase linear amplifier as shown in Fig. 2.1. As its main function, the emulator draws real time currents from the grid just like a physical machine. The emulator essentially tracks the reference currents given by the accurate machine model with proper control.

1) During symmetrical conditions

The dc input reference currents (i_d^* and i_q^*) to the emulator from the machine's mathematical model are produced by fundamental positive sequence stator currents. Hence, to control the emulator's real currents with respect to the reference dc currents, the proportional-integral control

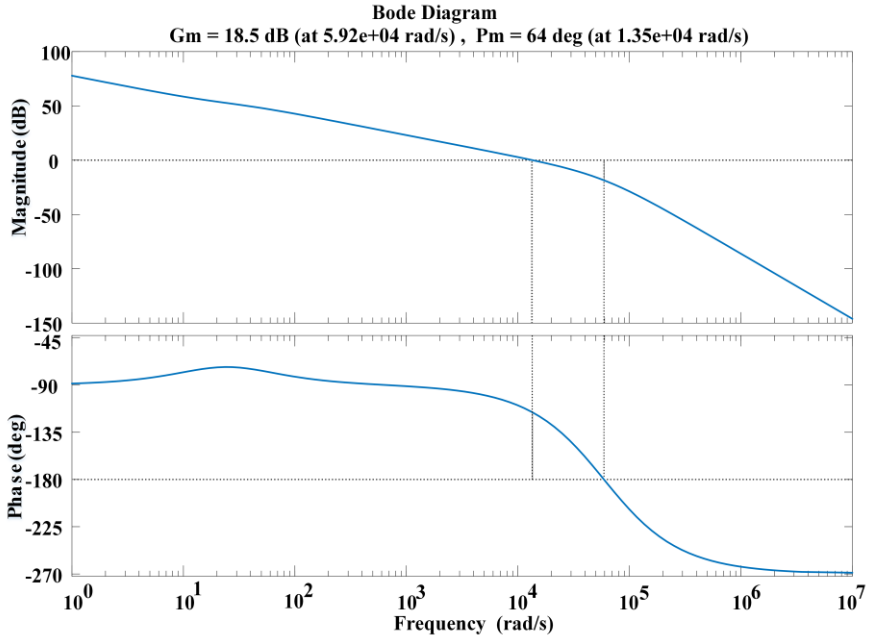


Fig. 2.4. Bode plot for the PI controller design.

approach is only chosen with sufficient closed-loop bandwidth in Fig. 2.4. This gives good transient and steady state tracking accuracy under symmetrical conditions.

The PI controller gains in (2.16) are tuned for the following open-loop transfer function $\big(G(s)H(s)\big)$. This involves, the first-order transfer functions of the emulator (T_1), RL link filter (T_2) , and current sensor (T_3) given by (2.17)-(2.19), with the linear amplifier and current sensor gains of K_{LA} and K_c with respective delay times τ_{LA} and τ_c and link filter parameters of resistance (R) and inductance (L) (refer to appendix).

$$G_{PI} = K_p + \frac{K_I}{s} \tag{2.16}$$

$$G(s)H(s) = T_1 * T_2 * T_3 \tag{2.17}$$

$$T_1 = \frac{K_{LA}}{1 + s\tau_{LA}} \tag{2.18}$$

$$T_2 = \frac{\frac{1}{R}}{1 + s\left(\frac{L}{R}\right)} \tag{2.19}$$

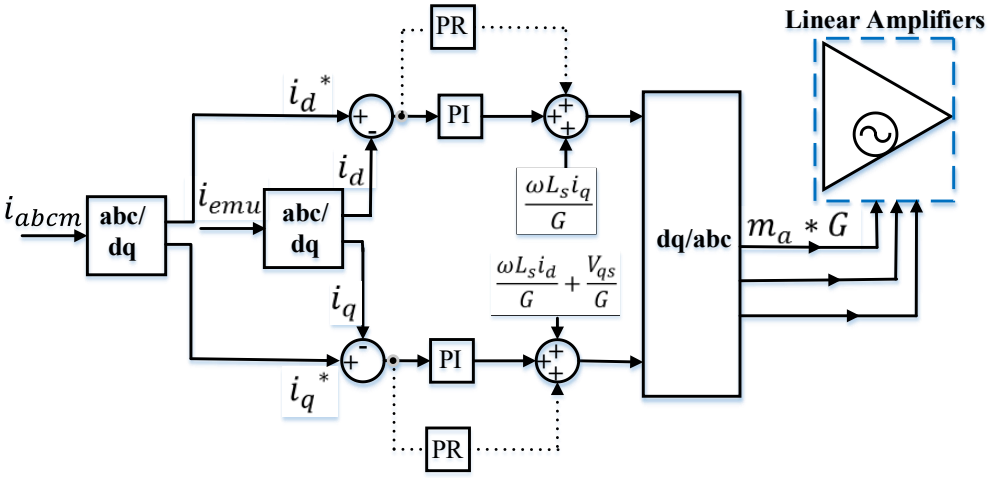


Fig. 2.5. Emulator control architecture.

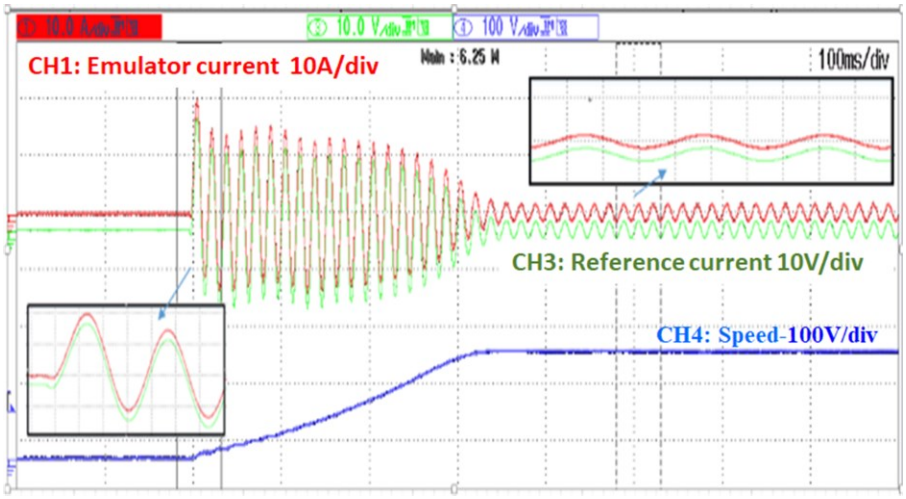


Fig. 2.6. PI based emulator tracking symmetrical conditions.

$$T_3 = \frac{K_c}{1 + s\tau_c} \tag{2.20}$$

The proportional and integral gains of the emulator are tuned in compliance with BIBO stability conditions. An appropriate bandwidth (ω_n) is chosen to respect the maximum bandwidth limitation imposed by the delay times of the linear amplifier, current sensor, and sampling time step (T_s) (2.21). Equation (2.21) is derived by comparing the present closed-loop transfer function

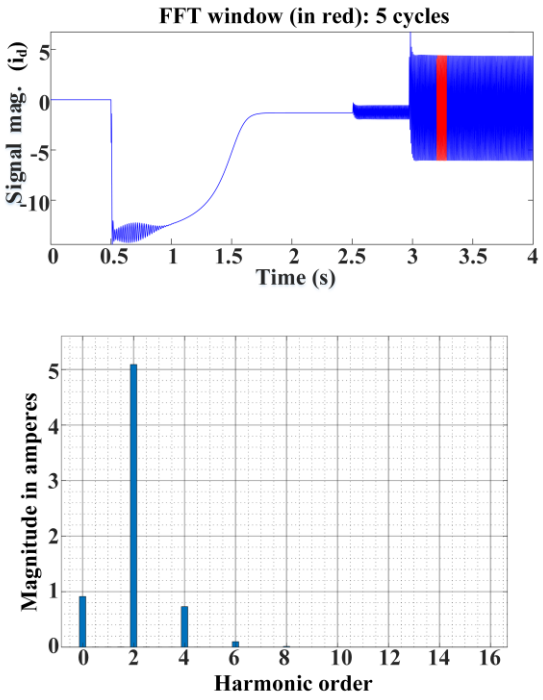


Fig. 2.7. Machine current $\boldsymbol{i_d}$ and corresponding FFT analysis respectively after shunt fault at instant 2.9 seconds.

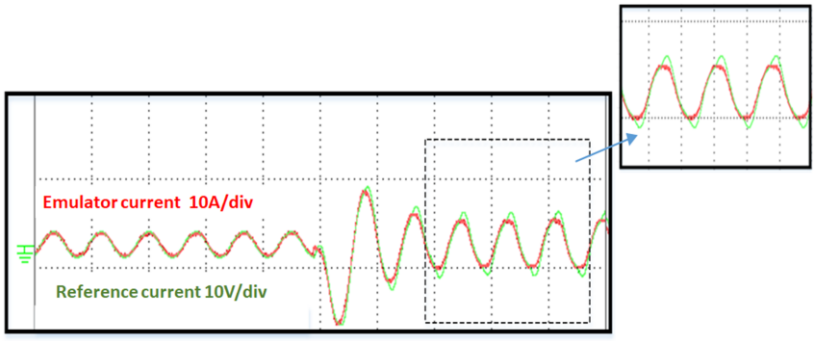


Fig. 2.8. PI based emulator tracking asymmetrical conditions during series impedance fault to shunt impedance fault transition.

$\big(1 + G(s)H(s)\big)$with the standard second order closed-loop transfer function for a damping ratio (ζ) (refer appendix).

$$2\zeta\omega_n = \frac{1}{\tau_{LA} + \tau_c + T_s} \tag{2.21}$$

The tuning of the PI controller is done and proportional and integral gains $\big(K_p \; and \; K_i\big)$ are obtained with the help of Bode plot analysis as shown in Fig. 2.4. The gain margin of 18.5 dB, phase margin of 64^0 are obtained for a bandwidth of 1350 Hz. This bandwidth does not exceed the maximum bandwidth (1800 Hz) which is calculated from (2.21). The resultant gains are

incorporated in the PI controllers of the emulator controller shown in Fig. 2.5. The designed PI control-based emulator current can track the reference current under symmetrical conditions namely during starting and the steady state as shown in Fig. 2.6.

2) Asymmetrical conditions

The introduction of negative sequence currents and distortion in the shape of the sinusoidal stator current under unbalanced conditions, lead to multiples of 2^{nd} order harmonics in dq currents (Fig. 2.7). Therefore, the PI controller alone is not enough for good tracking accuracy. Fig. 2.8 depicts asymmetric fault transients where the emulator current could not follow the reference signal with good accuracy. Here the mathematical model giving reference current is employed with Euler's integration.

It is evident in Fig. 2.8, that the asymmetry by the series fault is tracked by the emulator PI controller alone. The increase in asymmetry by shunt fault cannot be tracked by PI control alone.

Hence this chapter proposes the use of a proportional resonant (PR) controller in addition to the PI controller. The dq currents corresponding to the multiples of second-order frequencies are addressed by the PR controller. The transfer function of the PR controller for gain 'K_r', cutoff frequency constant 'β', oscillating frequency 'ω_f'in rad/sec is given by (2.22) [44].

$$G_{PR} = \frac{K_r \beta s \omega_f}{s^2 + \beta S \omega_f + \omega_f^2} \tag{2.22}$$

The control signal by the PR controller is added to that of the PI's and finally given to the control input of linear amplifier driven in voltage control mode. The PR controller gain (K_r) is tuned as follows:

1. The Bode plot of the emulator system with PI control alone is considered in Fig. 2.4. The gain(G_{2n}) corresponding to the $2n$ order frequency $(\omega_f\ rad/s\ )dq$ currents for $n = 1,2,3, \ldots etc.,$ is identified.
2. The same system with only PI controller is later tuned to achieve maximum tracking accuracy for severe asymmetric faults. This is done in simulation, by ideally increasing the system bandwidth to 50.265 k-rad/sec violating the maximum practical bandwidth limitation discussed before (2.21).

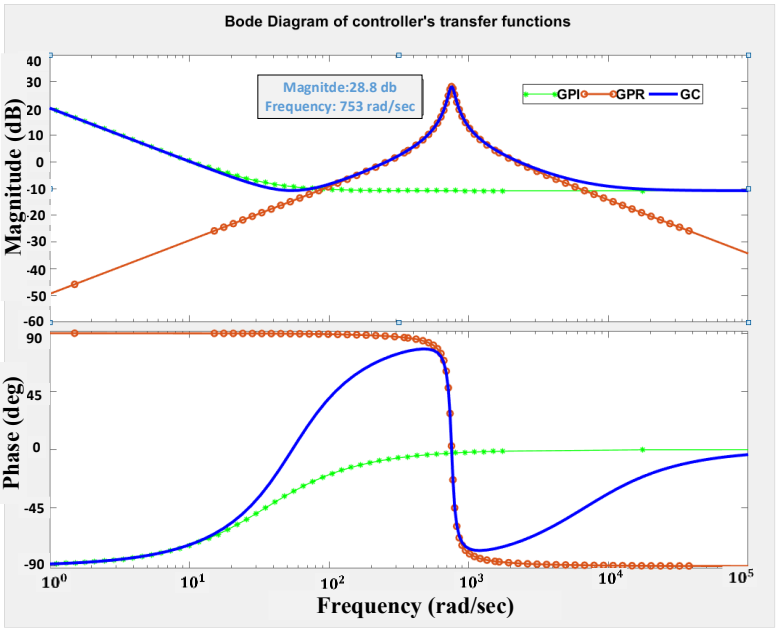


Fig. 2.9. Bode plots of open loop transfer functions of PI, PR and PI+PR controllers.

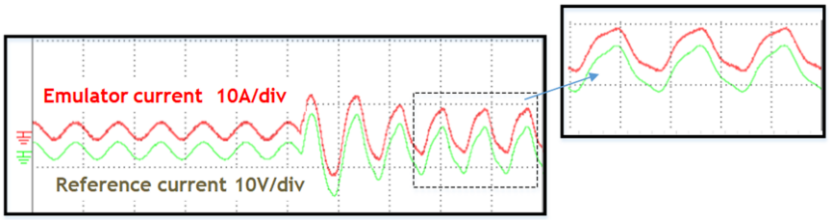


Fig. 2.10. Proposed emulator (PI+PR) tracking asymmetrical conditions during series impedance fault to shunt impedance fault transition.

3. Identify the gain(G_{2n}^{*}) corresponding to the $2n$ order frequency $(\omega_f\ rad/s)dq$ currents for $n = 1,2,3, \ldots etc.$, in the Bode plot of the emulator system with ideal bandwidth PI.

4. The incorporated gain (K_r) of the PR controller is obtained from the difference of the above-identified gains and is calculated as in (2.23).

$$20\log|K_r| = |G_{2n}^{*} - G_{2n}| \tag{2.23}$$

The constant β determines the bandwidth of the PR controller (refer to appendix). The individual and combined bode plots of the practical bandwidth PI and PR controllers for transfer functions G_{PI}, G_{PR} and G_C (2.24) are shown in Fig. 2.9.

$$G_c = G_{PI} + G_{PR} \tag{2.24}$$

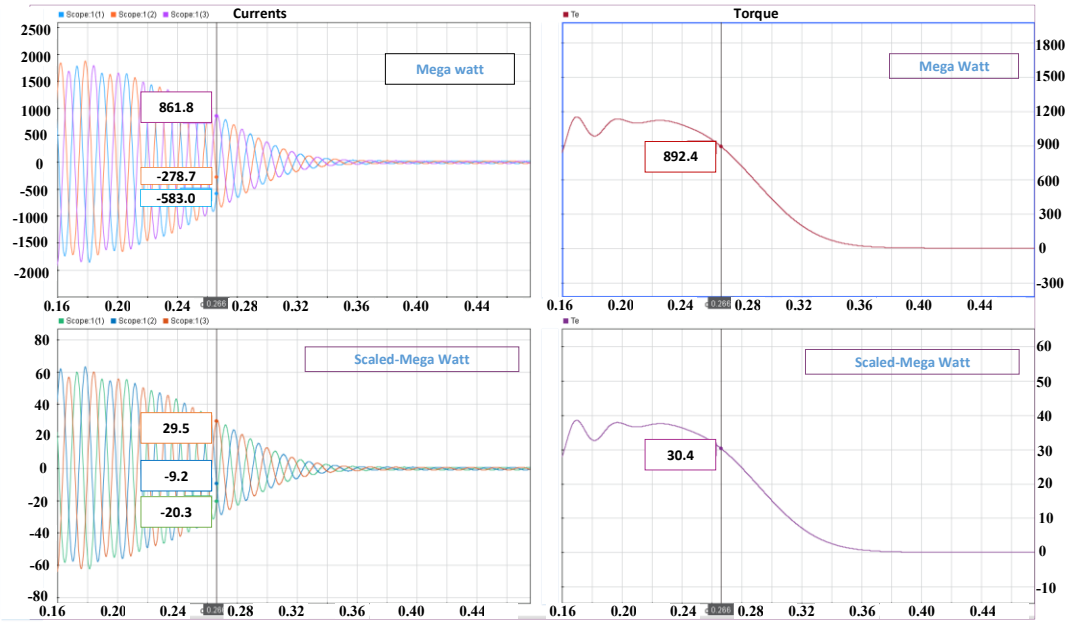


Fig. 2.11. Current and torque envelopes for MW (top) and scaled MW machines (bottom).

The proposed emulator with PI and PR controllers addressing the second harmonic $(with\ n = 1)$ alone achieves good tracking accuracy with the reference current as shown in Fig. 2.10.

Fig. 2.7 shows that, even though there are frequencies of order 4, 6, and 8, the magnitudes of them are small compared to the 2^{nd}. Hence this chapter suggests an optimized approach to address the harmonic which has the largest magnitude initially. If sufficient accuracy is not met, the other harmonics $(n = 2,3,4)$ with the next higher magnitude could also be addressed from (2.22), (2.23). This adjusted approach reduces the burden on the real time processor.

Hence, the developed virtual machine test bench (emulator), serves the purpose of mimicking the electrical dynamics of a squirrel cage machine for any asymmetrical conditions. The proposed control strategy is robust for any unbalanced current. Therefore, emulation for different asymmetrical faults can be done based on the maximum current, voltage, and power limitations of the test bench. This concept offers scope of mimicking even a MW power level machine with the same developed emulator at the laboratory power level. Hence scaling down the MW induction machine to laboratory power level with the help of per unit transformation enables one to get the job done.

2.4 Process of Scaling Down MW Machine

The mega-watt level squirrel cage induction machine can be scaled down to test laboratory power range with the help of per unit (p.u) transformation. This procedure essentially forms a replica of huge machine realized at very low power level. Initially, the p.u quantities of resistances, inductances, inertia, and friction constants of the giant machine are obtained with MW base values as per the equation (2.25).

$$(P.U)_{MW} = \frac{(actual\ value)_{MW}}{(Base\ value)_{MW}} \tag{2.25}$$

Then the obtained p.u values are multiplied with the base values of laboratory power level (KW) machine to get the replicated machine parameters as per the equation (2.26).

$$(P.U)_{MW} * (Base\ value)_{KW} = (Scaledown\ values)_{KW} \tag{2.26}$$

However, the MW replica would certainly have the same electrical and mechanical dynamics as that of the real MW machine, but with reduced or scaled down magnitudes which is illustrated clearly in the following Fig. 2.11, where the envelope for currents for MW machine are replicated at lower power level for a period of starting conditions.

2.5 Result Analysis

This section presents experimental results for asymmetric grid faults namely series impedance faults and shunt impedance faults i.e., line to line (LL), line to neutral (LN), and line to line to neutral (LLN). As described in section 2.3.1, the series impedance faults are applied initially to have the necessary voltage drop. Later shunt faults are applied to the same phase. These faults essentially create voltage unbalance at the stator input terminals of the real machine and/or the physical emulator. The emulator is developed by a high-performance linear amplifier with its maximum phase current rating of 20 A and voltage rating of 208 V and maximum open-loop bandwidth of 100 kHz. The results obtained with the 5 hp emulator for different asymmetric fault transients are validated with the real machine. An analysis is also made regarding positive and negative sequence components and the appearance of harmonics during faults with the help of simulation results in Matlab/Simulink.

The validating results in Fig. 2.12 for the 5 hp machine emulator, not only prove the tracking accuracy with respect to the reference current but also with respect to the real machine's current. The tracking ability is obtained by (i) upgrading the mathematical model as per section 2.2, (ii) Enhancement in control concept as per section 2.3.3.

Considering the maximum current limitations of the linear amplifier emulator, the reduced input line voltages applied to the 5 hp machine is 90.5 V. The machine emulating accuracy is not only verified for fault and fault transitions, but also for pre-fault and post fault conditions.

Fig. 2.12 and Fig. 2.13 shows the quasi-steady states of the emulator, real machine, and simulation results for 5 hp machine during series fault and shunt faults conditions namely LL fault, and LN fault respectively. The first channel, CH-1, indicates the faulty phase-A current where a series fault of 10 Ω is being introduced initially. CH-2, CH-3 represent corresponding phase voltage, reference phase–A current, respectively. The reference nodes of CH-1 and CH-3 are slightly shifted to give a clear picture of tracking capability. CH-4 represents the fault current from phase A to phase B or the fault current from phase A to neutral through the shunt fault impedance. It is observed here that not only the emulator's current in (CH-1) tracks the reference current (CH-3) with high accuracy in section (a) but also tracks the real machine's current in section (b).

Section (c) shows the results obtained for offline simulation of emulation also underlines the tracking capability of the proposed emulator.

An FFT analysis is done for the asymmetrical stator current of faulty phase in Fig. 2.12, and it is shown in Fig. 2.14. The presence of $1^{st}, 3^{rd}$ and 5^{th} harmonics are identified. These harmonics with their natural sequence of rotation will have opposite sequence currents during asymmetry as explained in section 2.3.2.

Fig. 2.15 presents the appearance of negative sequence components, positive sequence components for fundamental line currents and voltages during a series fault at 2.5 seconds, and a shunt fault at 3 seconds. It is identified that the magnitude of zero sequence current is zero. The magnitude of the sequence currents calculated from (2.9), (2.10) could also be identified in Fig. 2.15 for the sub transient reactance of 3.42 Ω and quasi-steady state impedance of 20.13 Ω (based on the quasi-steady state slip). Similarly, for 5^{th} harmonics, the opposite sequence components are identified along with its own sequence (negative) in Fig. 2.16. The magnitudes of sequence

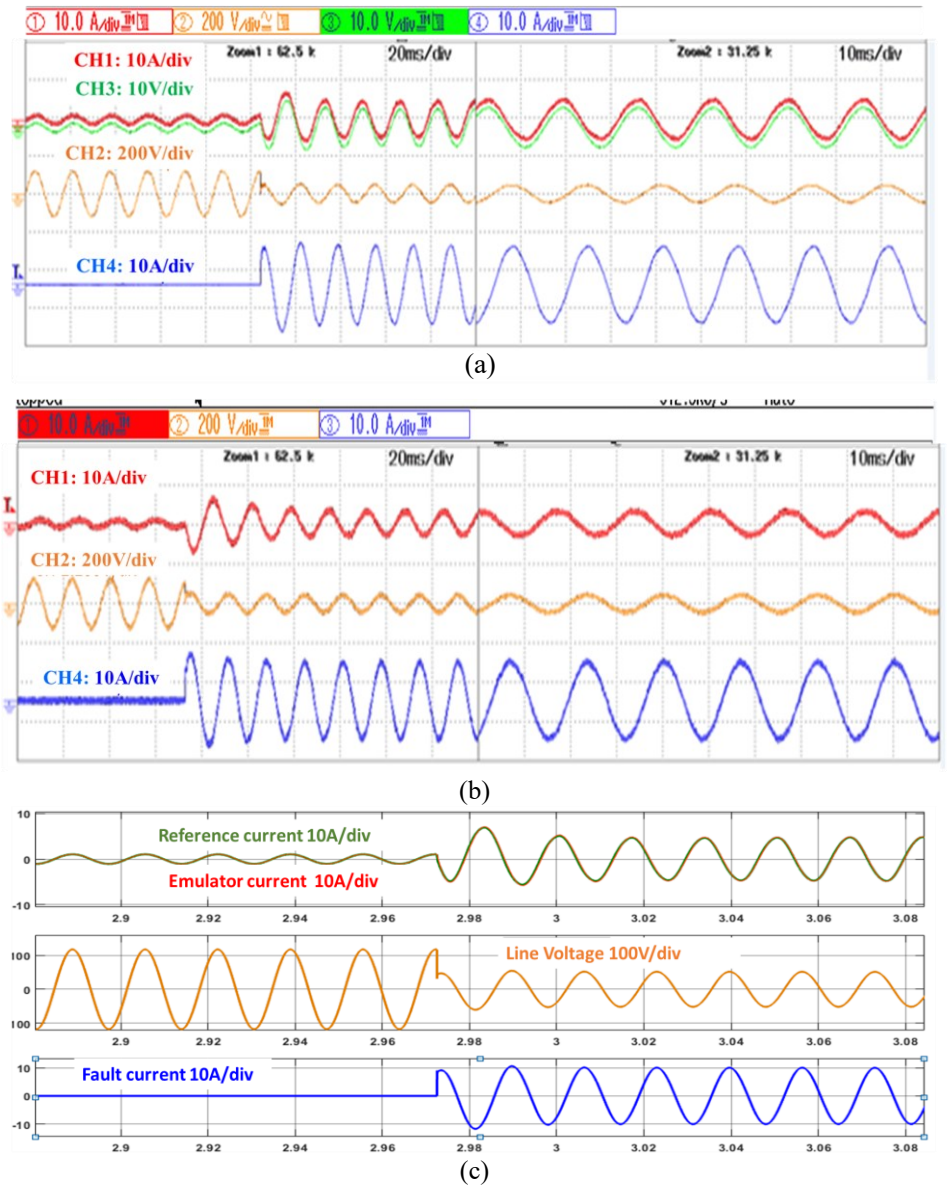


Fig. 2.12. Experimental results for L-L fault: section (a) Emulator (b) real IM (c) simulated IM with actual current (red), reference current (green), machine input voltage (orange) and fault current (blue) zoomed at the instants of fault and steady fault state.

currents calculated from (2.9), (2.10) are matched but possess very low magnitudes and hence may be neglected.

However, the presence of harmonics identified in Fig. 2.14, introduces $(n \pm 1)$ harmonics in direct and quadrature currents for $n = 1,5,7,.etc.,$ (as explained in Table 2.2, Fig. 2.7). The 2^{nd} order harmonic in dq currents have considerable magnitude while $4^{th}, 6^{th}$ harmonics, introduced by 5^{th} are low. This is because of the low magnitude of 5^{th} harmonic. Hence, the

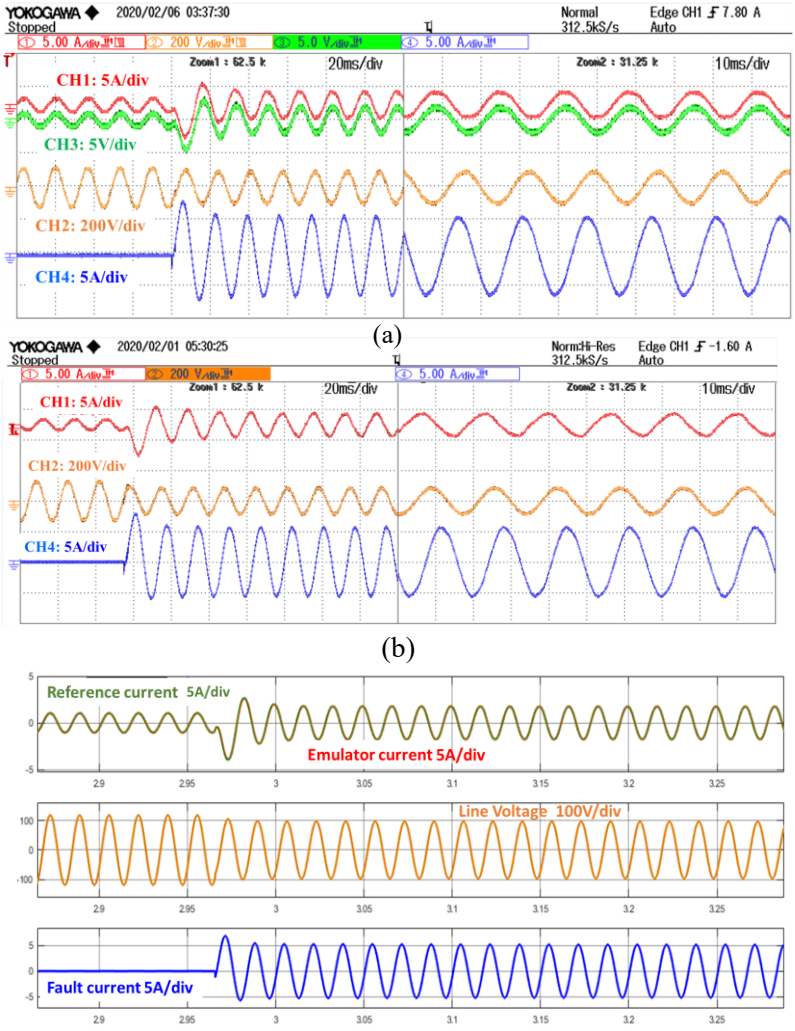


Fig. 2.13. Experimental results for L-N fault: section (a) Emulator (b) real IM (c) simulated IM with actual current (red), reference current (green), machine input voltage (orange) and fault current (blue) zoomed at the instants of fault and steady fault state.

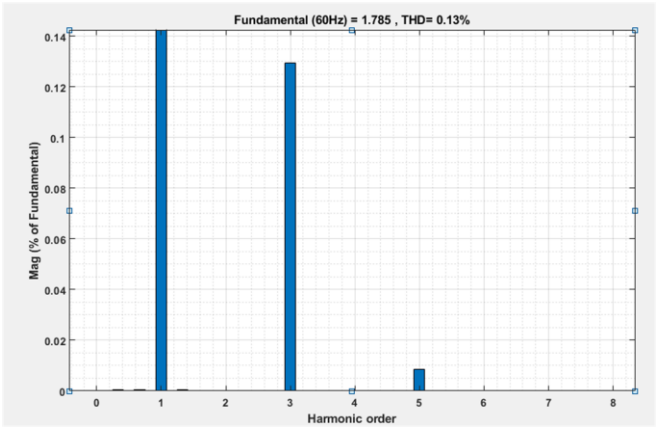


Fig. 2.14. FFT analysis of stator current during LN fault for 5 hp machine.

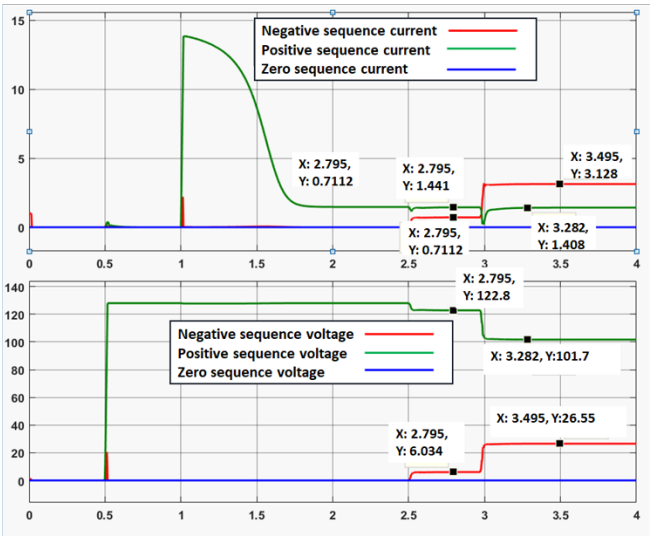


Fig. 2.15. Appearance sequence currents and voltages for fundamental.

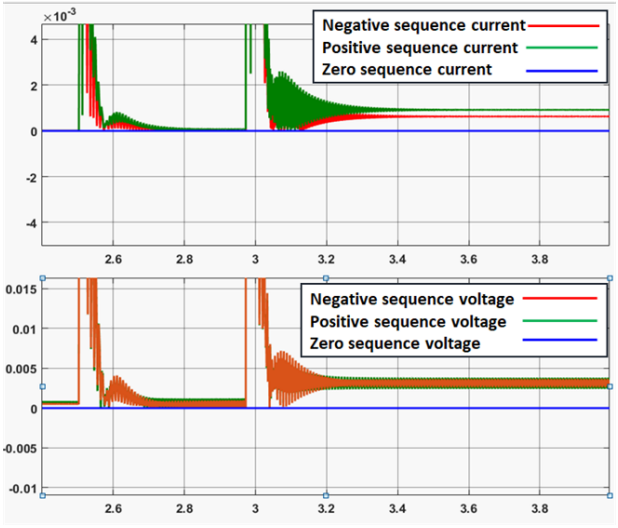


Fig. 2.16. Appearance of 5th harmonic sequence currents and voltages (zoomed at fault instants).

inclusion of the PR controller designed only for 2^{nd}order harmonic is justified.

In addition to the fault condition, considered quasi-steady state, the pre-fault to post-fault transition conditions is also emulated. The dynamic behavior of the emulated system is observed under various transients at a lower power level and the performance of the emulator is verified.

2.5.1 Pre-fault to post- fault Transients

This emulation of the 5 hp machine proves that it is good enough in following reference currents in all transitions from pre-fault to the post-fault condition in Fig. 2.17. The notations of all the channels remain the same as per Fig. 2.12. This is explained in detail with four transition states as below:

T1: pre-fault steady state to series fault state.

T2: series fault state to shunt fault state.

T3: shunt fault state to series fault state.

T4: series fault state to normal steady state (fault resuming state).

The corresponding real time speed and torque waveforms for one of the severe asymmetric faults (LLN) are also recorded in Fig. 2.18. Channels CH-1, CH-2, and CH-4 represent torque, line voltage, and speed, respectively. It is observed that during unbalanced fault conditions, the second

harmonic oscillatory content in torque is noticed indicating negative sequence components of current and voltage. The transient spike in torque when a severe shunt fault occurs is also observed. In experiment a sudden rise in the noise of the physical machine was observed.

The emulator's efficacy is not only validated for shunt asymmetric faults but also for multiple series impedance faults. Fig. 2.19 denotes the application of series fault impedances of 10 **Ω** in phase-A and 8 **Ω** in phase-C for T1 and T2 transitions respectively. The fault resuming states by removal of fault impedances in phase-C and phase-A is represented by T3 and T4 transitions. However, T1 and T4 transitions have already been shown in Fig. 2.17 for the series fault of 10 **Ω** in phase-A. Hence the transitions T2 and T3 for 8 **Ω** fault impedance in phase-C are magnified in Fig. 2.19. The emulator's performance is identified in T2' and T3' transitions with that of the physical machine in T2 and T3 transition. The corresponding unbalanced phase voltages are represented at the bottom section of Fig. 2.19. The black-headed arrows indicate the point of transition in the transition phase.

Therefore, the experimental results obtained above prove that the machine emulator is robust in its performance for different kinds of asymmetrical shunt and series impedance fault transients considered.

The quasi-steady state conditions observed for the machine in Fig. 2.19, zoomed at T3 and T3', respectively possess fractional-order harmonics in addition to the fundamental because of grid voltage unbalances. Therefore, it is clearly witnessed that the emulator tracks even the distorted stator currents.

2.5.2 Starting and loading transients

The loading and unloading transients are also observed in Fig. 2.20 for MW machine replica, (zoomed at T1 and T3 periods respectively) for a load torque of 1 Nm,which is equivalent to 297.7 Nm without violating the maximum torque constraint of $\tau_{max} = 2.99\ Nm$ equivalent to 893.1 Nm, for operating voltage of 26.3 V phase voltage and respective MW scaled down machine parameters. Hence it can be seen that the electromagnetic torque (CH-2 in orange) also rises to meet the load torque with a corresponding fall in speed (CH-4 in blue) and rise in stator reference current (CH-1 in red) and thus emulator current (CH-3 in green). The steady state behavior of the

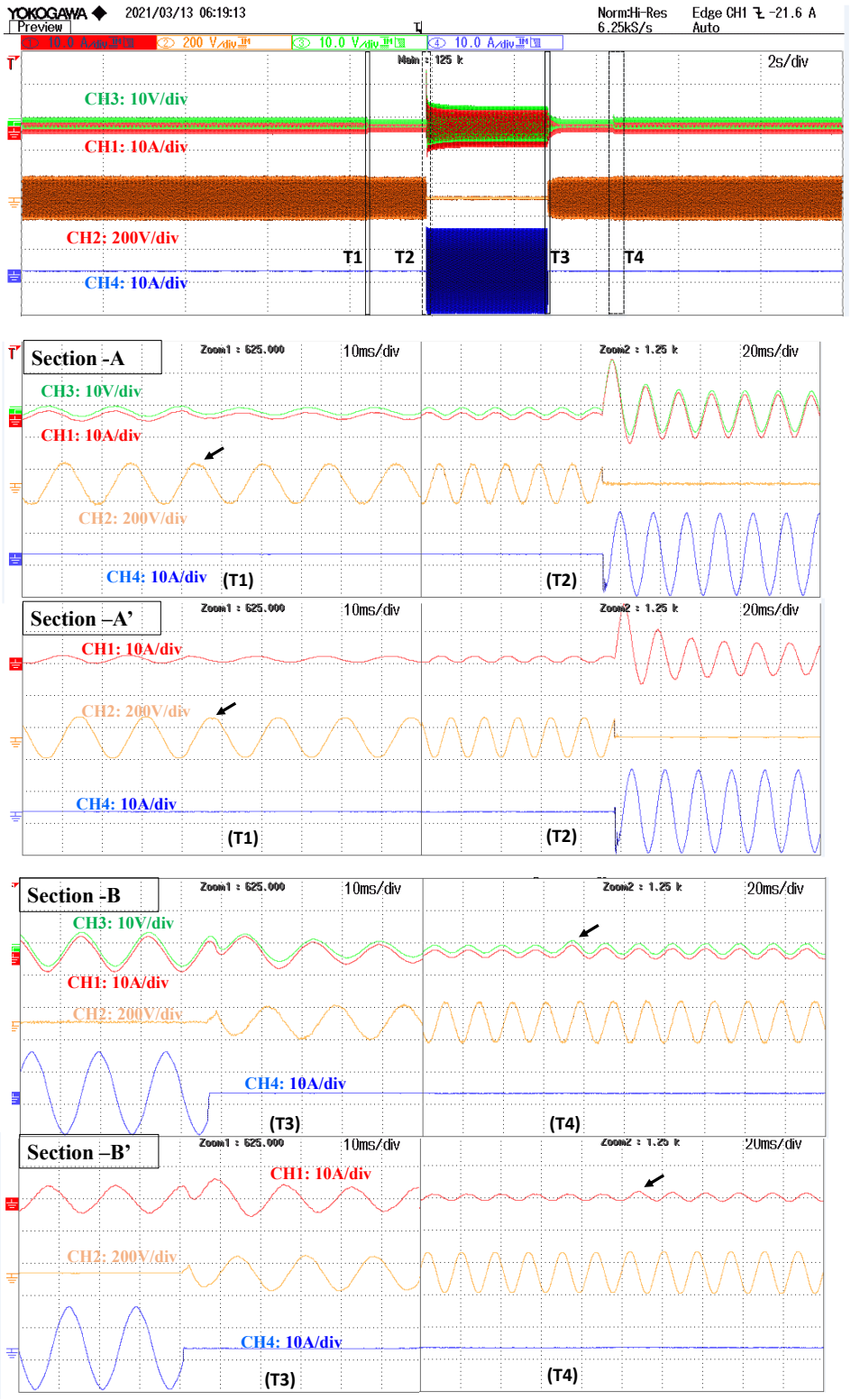


Fig. 2.17. LLN fault transient emulation and validation done with a real 5hp machine. *Note*: The black arrows represent point of transition from one state to another.

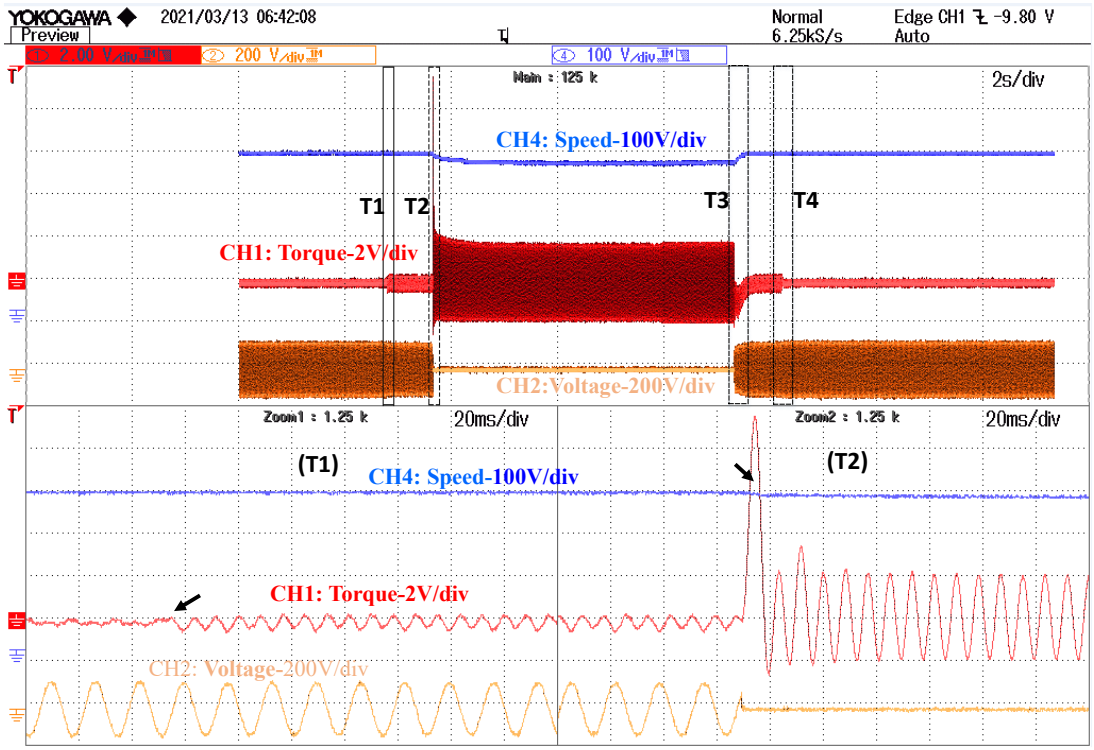


Fig. 2.18. Real time speed and torque characteristics for LLN fault transients. *Note*: The black arrows represent point of transition from one state to another.

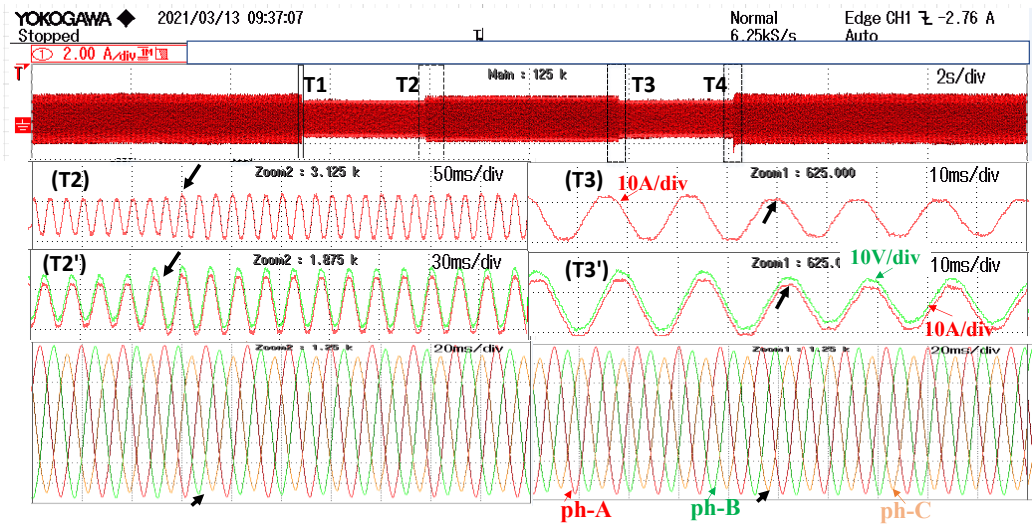


Fig. 2.19. Series impedance fault transient of real machine at T1: With 10 Ω in phase- A, T2: Additional 8 Ω in phase-C, T3 & T4: Post fault transients with the removal of 8Ω and 10 Ω fault impedances. Emulated and reference currents with respective unbalanced three-phase voltages below. *Note*: The black arrows represent point of transition from one state to another.

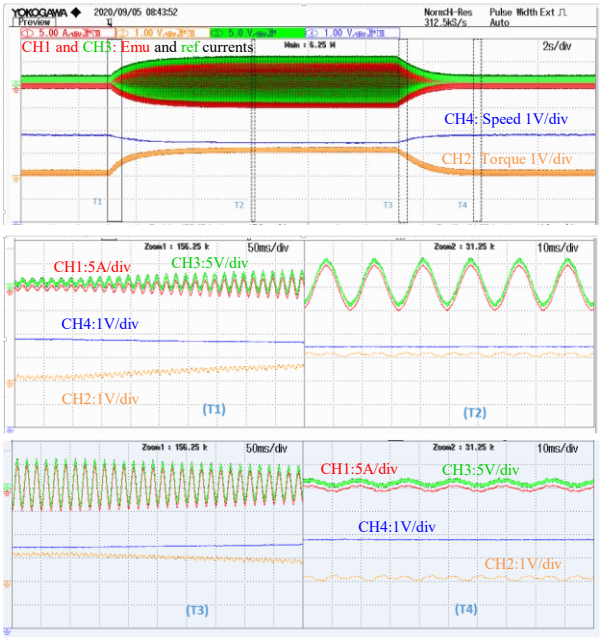


Fig. 2.20. Loading and unloading transient emulation for T1, T2, T3 and T4 transitions.

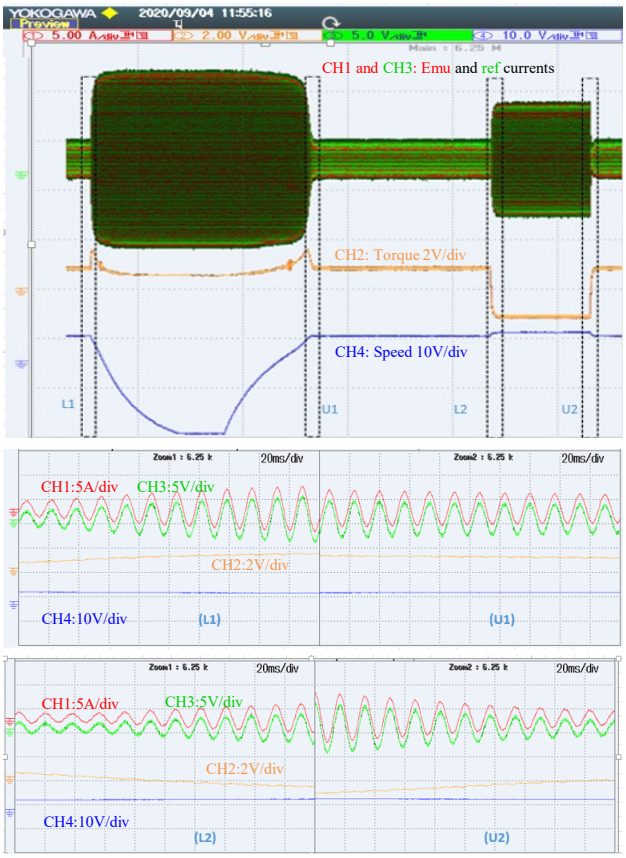


Fig. 2.21. Loading and unloading transient emulation for L1, U1, L2 and U2 transitions.

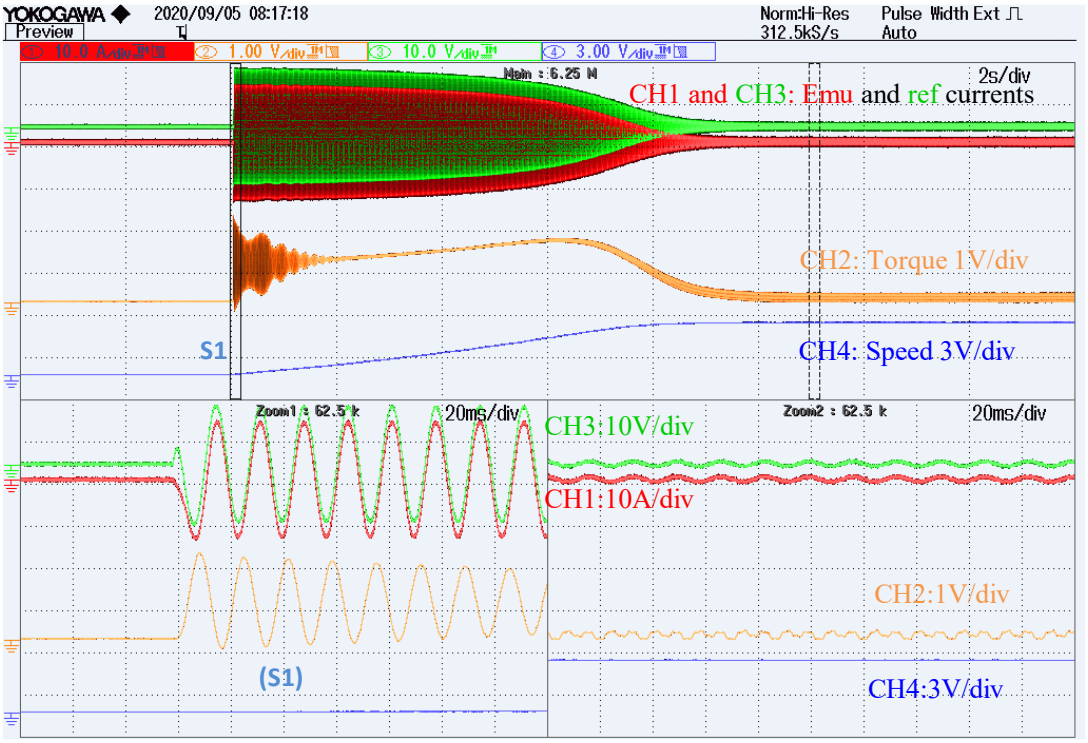


Fig. 2.22. Emulation of the scaled down machine for starting and steady states.

machine emulation after application and removal of the load are also observed in detail for T2 and T4 periods magnified.

Similarly, for the 5 hp machine considered, for a reduced operating phase voltage of 30.33 V, the maximum operating torque would be $0.62\ Nm$, a load torque of $1Nm$, which is greater than the maximum torque is applied, the machine speed reverses indicating that it is driven by load. These overloading and respective unloading transients are zoomed and are indicated with L1 and U1 respectively in Fig. 2.21.

Later, a negative torque of $1\ Nm$ is also applied when the machine is running in normal no-load condition shown in the same Fig. 2.21. The corresponding rise in speed indicates that the machine is driven by load torque in positive direction. Its loading and unloading transients are indicated with L2 and U2 respectively. Therefore, the machine emulator is working well for both the replicated MW machine and 5 hp machine under all types of loading and unloading transients considered.

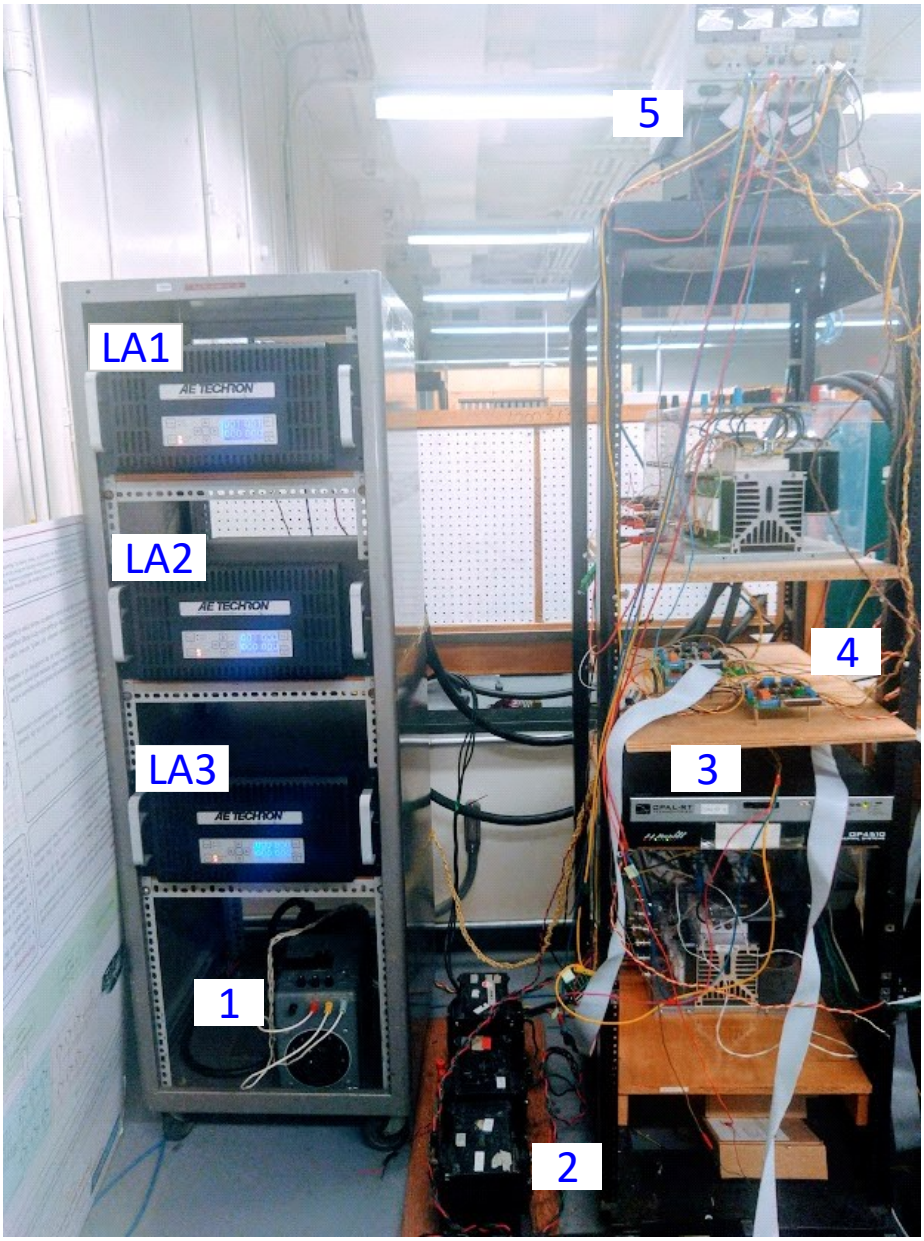


Fig. 2.23. LA1, LA2, LA3 – three-phase Linear Amplifiers, 1- three-phase variac, 2 - link filters, 3 - Opal-Rt, 4 - protection circuit and sensors, 5 - DC power supply.

The starting transient and steady state conditions is also observed for scaled down machine in Fig. 2.22, zoomed at time periods S1 and S2, respectively. The steady state current of 1.875 A peak is observed which possess fractional order harmonics in addition to the fundamental because of minor grid voltage imperfections (clearly visible Fig. 2.19 (T4)). These imperfections are

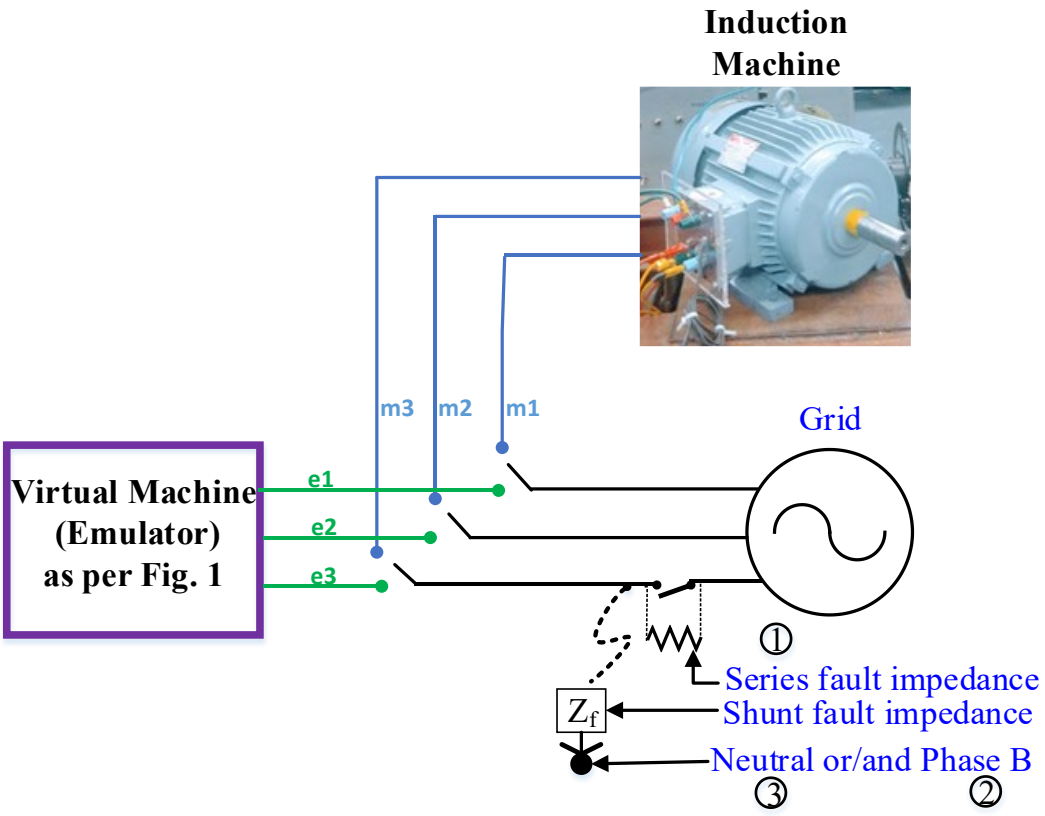


Fig. 2.24. Manner of implementation of emulation and validation for asymmetric grid fault testing.

expected to be caused by nonlinear loads operating in parallel to the distribution level bus which distort the grid voltage [44]. Therefore, it can be clearly witnessed that the emulator absolutely tracks very well even for the distorted shape of the grid waveform.

Fig. 2.23 shows the experimental setup used for a linear amplifier-based emulator to implement the different asymmetrical faults on the squirrel cage machine. Fig. 2.24 represents the testing of the physical machine and emulator for asymmetric grid faults. The series and shunt faults are applied with the help of a resistive load bank. The implementation procedure for testing with the emulator can be done by utilizing e1, e2, e3 terminals. The validation with the real machine can be done by utilizing m1, m2, m3 terminals.

2.6 Summary

The designed physical emulator system can be realized for any asymmetrical grid fault transients to test the electrical dynamics of the squirrel cage induction machine. The reason for multiples of second-order harmonics in emulator controller currents during asymmetric faults is explained and corresponding control logic is suggested. Since the higher bandwidth linear amplifier emulator tracks the symmetrical pre-fault conditions, symmetrical faults can also be tested with relevant fault impedance (owing to the current limitation of the linear amplifiers).

The linear amplifier emulator with a maximum current limitation of 20 A can be overcome by a bidirectional converter, which can possess a higher current rating, for testing various transient conditions at an enhanced power level. Hence it can be concluded from the results in the preceding section, the developed emulator test bench is proved to be robust and works similar to the real machine for different grid faults. The tracking performance is noted to be good enough for not only pre-fault to fault transition but also for the fault to fault and fault to post-fault transitions.

Chapter 3 Emulation of induction machines subject to industrial grid harmonics

3.1 Introduction

Induction machines are considered the workhorse in several industrial sectors. They offer good reliability owing to several advantages such as good controllability, low maintenance, safety, and performance. When such machines are interfaced with a grid, anomalous behavior can result due to imperfections of the grid. Although the space harmonics, slotting harmonics, etc., in induction machine will affect the power quality of the grid [45], the chapter focuses on an in-depth understanding of the effects of grid harmonics on the induction motor.

The machine's dynamic behavior can be tested with a real induction machine. This method of testing is considered orthodox [39], and it is quite time consuming to gather associated subsystems of the machine. Sometimes testing reduces the life expectancy of the machine. This disadvantage leads to the development of a "virtual machine" or "machine emulator" which uses PHIL technology. It uses power electronic hardware interfacing the grid, to mimic the electrical dynamics of the intended machine in a real-time control loop. The performance of this emulation technique lies in the tracking accuracy regarding actual machine electrical dynamics. This can be achieved with an accurate mathematical model and precise emulator control. In this chapter, the emulator accurate dynamic tracking ability is improved and tested with respect to the real machine in an environment of industrial grid harmonics.

Harmonics are a major concern to electrical utilities and consumers. They occur due to grid voltage distortions, interconnection of renewable sources, and the usage of nonlinear loads in industries such as electric arc furnaces, fluorescent lighting, rolling mill loads, converter-based consumer loads, etc. Generally, the majority of electronic and power electronic equipment connected in parallel to the grid causes lower order harmonics [17], [18]. They result in the heating of the electromagnetic core of the machine. In addition, active-controlled devices such as IGBTs, MOSFETs, etc., activated with different PWM techniques are a source of higher-order harmonics as well. The higher-order harmonic currents can cause the failure of capacitors and the tripping of circuit breakers [46]. The effects of harmonics in the majority of cases of a plant or process are

degradation of individual component efficiency, reduced torque in rotating equipment, increased stress in the equipment insulation, increased noise, maloperation of sensitive relays, interference between power and communication circuits, increased losses and thus reduced life expectancy [17]. Finally, it can lead to a decline in overall process quality.

When the system or plant has power quality issues, their impact on the loads needs to be examined prior to the equipment damage or production loss. This enables the power system operators to develop corrective measures in advance. Therefore, with the help of emulation techniques, the effects on the plant/process output can be investigated in terms of quality and/or quantity prior to the installation of the machine. This method incurs no power losses while testing and will maintain the life of the machine.

A detailed literature survey has been done for emulating grid harmonics. The reasons for the production of voltage harmonics based on harmonic measurement in manufacturing industries are identified in [17], [18], [47], and [48]. The influence of poor power quality has been studied in steel plants, automotive industries, and different industries [49]-[51]. In an industrial grid, the onsite investigations for 3 months in [46] reveal the average value of THD is approximately less than 10% for major voltage harmonics of order 5, 7, 11, and 13. These harmonics are produced due to rectifiers and electric arc furnaces. According to case studies in IEEE 3002 [17] for an adjustable speed drive, the individual harmonic current spectrum shows 18.24% and 4.01% as the maximum and minimum values. Investigation of grid harmonic effects have been studied on wound rotor induction machine using simulation techniques such as FEA and CDF [45]. These methods will not enable one to observe the cumulative effects on the system assembly practically. Experimental evaluation of the harmonic impacts is discussed with a practical machine in [52], but lower values of THDs are considered to avoid the energy losses. Harmonic compensation techniques have been emulated for an electrostatic precipitator load [53]. However, there is no reported literature on emulating impact of grid harmonics on induction machines.

Therefore, this chapter contemplates the extreme values of THDs for such major voltage harmonics to emulate the effects on induction machine. The combination of harmonics for maximum (20%) and minimum (5%) percentage of the nominal value are considered. High-performance linear amplifiers (LAs) of bandwidth 200 kHz are chosen as emulators [37], [39], so

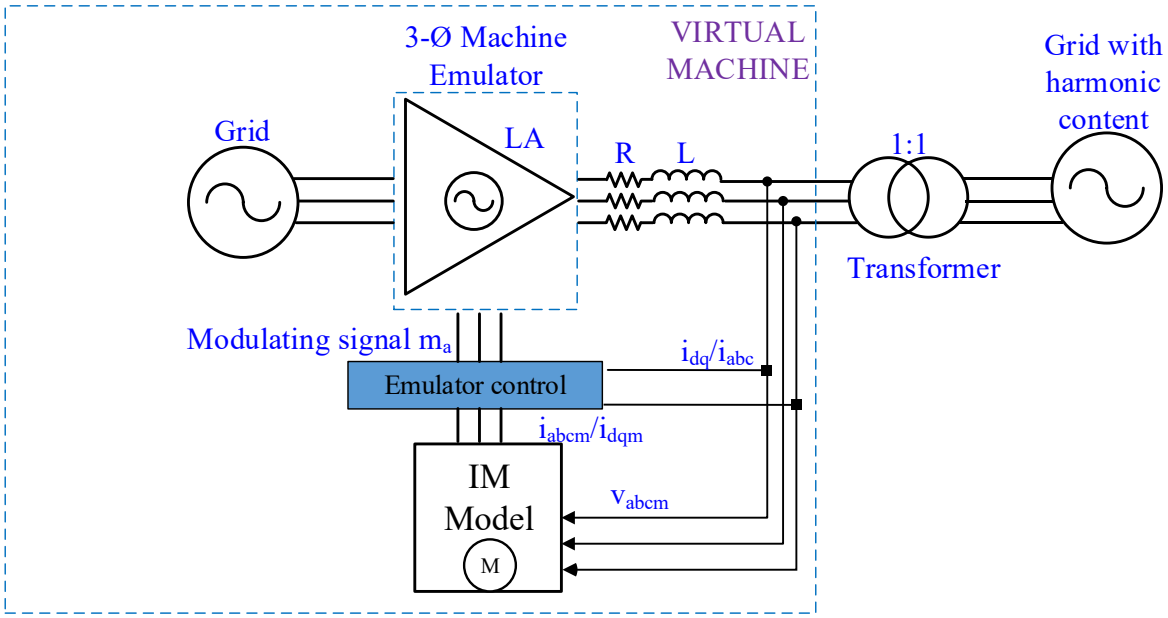


Fig. 3.1. Schematic diagram of the machine emulator for grid harmonics.

that the emulator possesses good tracking accuracy for lower and higher-order harmonics in machine currents. The real-time modulating signals to the LAs are given by an Opal-RT real-time processor. The machine model that is employed is an accurate discrete linear dq-model which is realized with the trapezoidal method of integration [31]. A detailed mathematical and FFT analysis has been shown for accurate emulator control design in section 3.2. Experimental results for grid harmonics are provided with the LA-based emulator and are validated on a real 5 hp machine during steady-state, starting and loading transients proving the efficacy of the proposed emulator. The experiments have been done at a reduced voltage owing to current limitations of the LAs. Finally, the last section discusses the conclusion and future scope.

3.2 Emulator Arrangement and its Control Technique

3.2.1 Components of Emulator

Fig. 3.1 shows the induction machine emulator for grid-side harmonics. The LAs are significant components in forming a virtual machine. The isolation transformer avoids circulating currents between the grid and the emulator. The (D/D or Y/Y) isolation transformer retains the shape of the harmonic grid voltage at the emulator terminals. The emulator control and mathematical model are implemented in real-time with the help of real-time processor Opal-RT.

3.2.2 Mathematical Model

The mathematical model is implemented in the synchronous reference frame to give constant dq currents. The trapezoidal integration integrated linear mathematical model is chosen for improved accuracy at larger sampling times in Opal Rt. The discrete dq state space modelling is described in (3.1) - (3.5).

$$\dot{I}(q) = A_{IM} I(q) + B_{IM} U(q) \tag{3.1}$$

$$\text{where,} \quad I(q) = \left[i_{ds}^{s} \quad i_{qs}^{s} \quad i_{dr}^{s} \quad i_{qr}^{s} \right]^{T} \tag{3.2}$$

$$U(q) = [v_{ds}^{s} \quad v_{qs}^{s} \quad 0 \quad 0 \ ]^{T} \tag{3.3}$$

$$A_{IM} = \begin{bmatrix} -\frac{L_r R_s}{D} & \frac{\omega_s L_s L_r - \omega_r L_m^2}{D} & \frac{L_m R_r}{D} & \frac{\omega_s L_r L_m - \omega_r L_r L_m}{D} \\ \frac{-\omega_s L_s L_r + \omega_r L_m^2}{D} & -\frac{L_r R_s}{D} & \frac{-\omega_s L_r L_m + \omega_r L_r L_m}{D} & \frac{R_r L_m}{D} \\ \frac{R_s L_m}{D} & \frac{-\omega_s L_s L_m + \omega_r L_s L_m}{D} & \frac{-L_{ss} R_r}{D} & \frac{-\omega_r L_s L_r - \omega_s L_m^2}{D} \\ \frac{\omega_s L_s L_m - \omega_r L_s L_m}{D} & \frac{R_s L_m}{D} & \frac{\omega_s L_m^2 - \omega_r L_s L_r}{D} & \frac{-L_{ss} R_r}{D} \end{bmatrix} \tag{3.4}$$

$$B_{IM} = \begin{bmatrix} \frac{L_r}{D} & 0 & -\frac{L_m}{D} & 0 \\ 0 & \frac{L_r}{D} & 0 & -\frac{L_m}{D} \end{bmatrix} \tag{3.5}$$

$$\text{where, } D = \left((L_s L_r - L_m^2) \right)$$

The output current from the state space model is obtained by integrating (3.1) with an accurate trapezoidal integration method. This method considers the present and past samples of derivative input shown in (3.6).

$$I(q) = I(q-1) + \frac{T}{2} \left(\dot{I}(q) + \dot{I}(q-1) \right) \tag{3.6}$$

Therefore, by substituting state space equation (3.1) for sampling instants q and $(q-1)$, in the trapezoidal integration equation (3.6), gives accurate sampled output current (3.7).

$$I(q) = \left(1 - \frac{A_{IM} T_s}{2} \right)^{-1} \left(1 + \frac{A_{IM} T_s}{2} \right) I(q-1) \tag{3.7}$$

$$+\frac{\left(1-\frac{A_{IM}T}{2}\right)^{-1}B_{IM}T_s}{2}\left[U(q)+U(q-1)\right]$$

3.2.3 Emulator Control Strategy

The real-time emulator control strategy demonstrated in Fig. 3.2, controls the error between actual currents drawn by LAs and reference currents by machine model. The dq current control is done with proportional-integral (PI) and proportional resonant (PR) controllers with the help of $\frac{abc}{dq}$ transformation and grid phase-locked loop. The feed forward terms in dq emulator current control involves LA amplification gain $(G)$and the link filter inductance (L_s). The PI controllers are tuned for a high bandwidth of 2.15 kHz for a stable gain and phase margins. The PI controller controls dc components in dq currents and are accurate for a sinusoidal input grid voltage. The damped oscillatory nature of dq currents during starting is addressed by high bandwidth PI controllers. This is not the case when the grid voltage is imperfect sinusoidal due to the nonlinear loads. This leads to high frequency oscillatory content in the dq currents of the machine. For instance, the odd order-negative-sequence -stator harmonic voltages such as the fifth and/or eleventh induces the same order stator harmonic currents in (3.8) - (3.10). The equations for corresponding i_d and i_q currents derived with $\frac{abc}{qd}$ transformation (K) in (3.11) are shown in (3.12) - (3.15).

$$i_a = i_{a\left(h_1+\frac{h_{5,7}}{h_{11}},13\right)}\angle\theta \tag{3.8}$$

$$i_b = i_{a\left(h_1+\frac{h_{5,7}}{h_{11}},13\right)}\angle\theta + 120^0) \tag{3.9}$$

$$i_c = i_{a\left(h_1+\frac{h_{5,7}}{h_{11}},13\right)}\angle\theta - 120^0) \tag{3.10}$$

$$K = \frac{2}{3}\begin{bmatrix}\cos\theta & \cos(\theta-\delta) & \cos(\theta+\delta)\\ \sin\theta & \sin(\theta-\delta) & \sin(\theta+\delta)\\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2}\end{bmatrix} \tag{3.11}$$

where $\delta = 120^0$

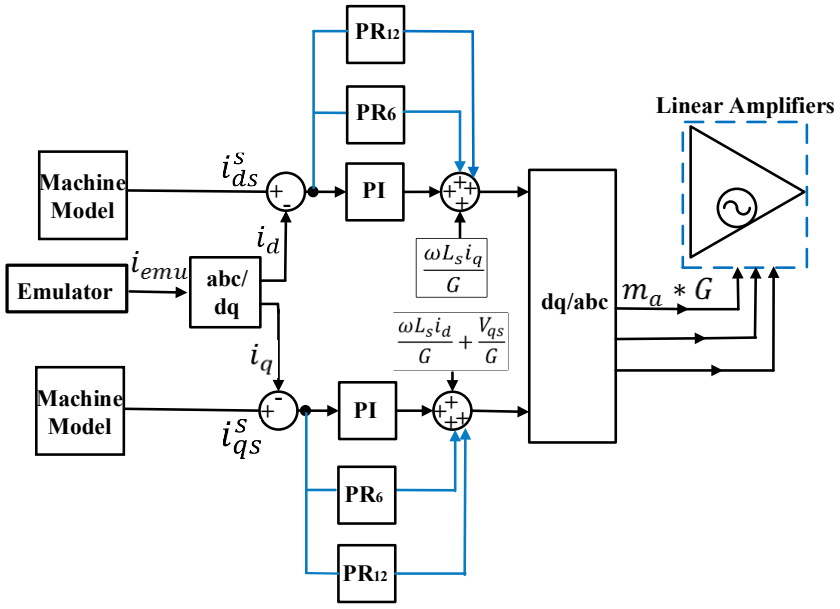


Fig. 3.2. Emulator control strategy for harmonics.

$$gives \qquad i_{d5} = I_{m1} - I_{m5}cos6\theta \tag{3.12}$$

$$i_{q5} = I_{m1} + I_{m5}sin6\theta \tag{3.13}$$

$$i_{d11} = I_{m1} + I_{m11}cos12\theta \tag{3.14}$$

$$i_{q11} = I_{m1} + I_{m11}cos12\theta \tag{3.15}$$

where I_m is the peak value of respective harmonic current.

Equations (3.12), (3.13) indicate the sixth harmonic content in dq currents due to fifth harmonic input current component. Similarly, equations (3.14), (3.15) indicate twelfth harmonic content in dq currents due to eleventh harmonic input current. I_{m1} represent the dc components due to fundamental. The same analysis is valid for the other order harmonics with their respective sequence of rotation. That is seventh and thirteenth harmonics being positive sequence, also injects sixth and twelfth in dq currents (3.16) - (3.19).

$$i_{d7} = I_{m1} + I_{m7}cos6\theta \tag{3.16}$$

$$i_{q7} = I_{m1} + I_{m7}sin6\theta \tag{3.17}$$

$$i_{d13} = I_{m1} + I_{m12}cos12\theta \tag{3.18}$$

$$i_{q13} = I_{m1} + I_{m12}sin12\theta \tag{3.19}$$

$$T_{PR} = \frac{G_{PR}\varepsilon s\omega_h}{s^2 + \varepsilon s\omega_h + \omega_h^2} \tag{3.20}$$

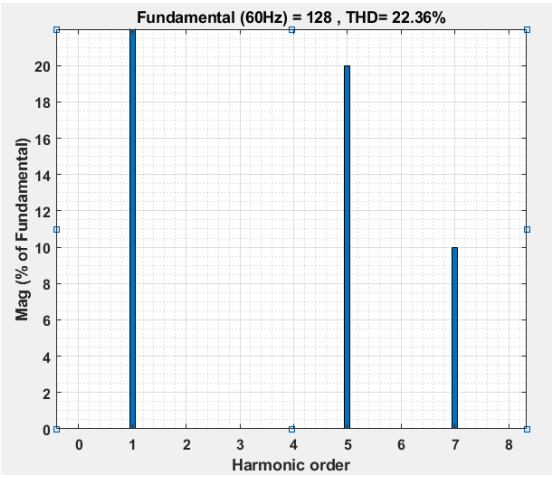
$$THD = 100.\frac{\sqrt{\left(\sum_{h\neq1}^{n} \mathrm{I}_{\mathrm{sh}}^2\right)}}{I_{s1}} \tag{3.21}$$

This mathematical investigation authenticates the FFT simulation analysis for dq currents shown in Fig. 3.3. Hence, the chosen PI controllers alone are no longer feasible for precise current control. Henceforth this chapter proposes a novel approach to deal with this problem by adding PR controllers corresponding to the harmonic frequencies in i_d and $i_q$currents (Fig. 3.3).

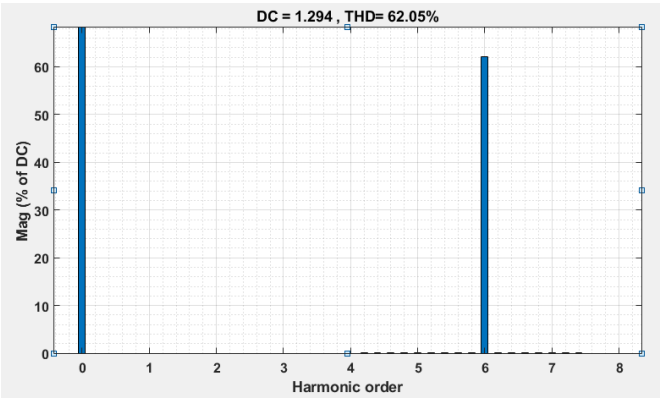
The second order transfer function of the PR controller for gain 'G_{PR}', cut off frequency constant 'ε', oscillating frequency due to harmonics 'ω_h' is given in equation (3.20). The PR controller gain G_{PR} is tuned in Matlab/Simulink with a starting gain value of G_{PI} (PI controller gain). The gain is gradually increased till the error between the actual and reference value becomes less than 1%. The cut off frequency constant (ε) is taken as 10% considering the side band frequencies around the resonant harmonic frequency.

3.3 Experimental Results

Fig. 3.4, 3.5 shows the experimental results for harmonic voltages and currents of the real machine and the proposed emulator during steady state. The experiment has been done for a reduced phase voltage of 52.5 V to protect the LA emulator from currents crossing a 20 A limit. Section- 1 (b) in Fig. 3.5, represents the emulator current during 20% of THD (3.21) of the 5th harmonic voltage and is exactly tracking the reference value. The emulator also behaves like a real induction machine with respect to Section-1(a). The same is proved in Section-2: for combination of 20% of 5th and 10% of 7th harmonic voltage, Section-3: for combination of 20% of 11th and 10% of 13th harmonic voltage, Section-4: for combination of 20% of 5th, 15% of 7th, 10% of 11th, 5% of 13th harmonic voltages. The mean reference nodes in the sections (a) and (b) are slightly different from each other. However, the currents trends and magnitudes have a good match with good accuracy under steady state. The behavior of the machine and emulator tracking accuracy for



(a)



(b)

Fig. 3.3. FFT analysis for (a) stator harmonic voltage (5^{th}+7^{th}) and (b) corresponding '$\boldsymbol{i_d}$' current.

fifth harmonic alone during starting and steady state are also verified along with speed, torque characteristics in Fig. 3.6. The overall and zoom-in profiles for starting and steady state of the real machine are in line with that of the emulator. However, the dynamic tracking accuracy is further verified by overlapping the machine and emulator currents in Fig. 3.7. During starting conditions for 5^{th} + 7^{th} harmonics, the emulator current and reference current overlap each other after a fraction of the first half cycle in section (a). In section (b), the emulator current overlaps the real machine's current with a slight compromise in accuracy. This slight mismatch at peaks of the current waveforms is due to the non-consideration of saturation nonlinearity within the machine.

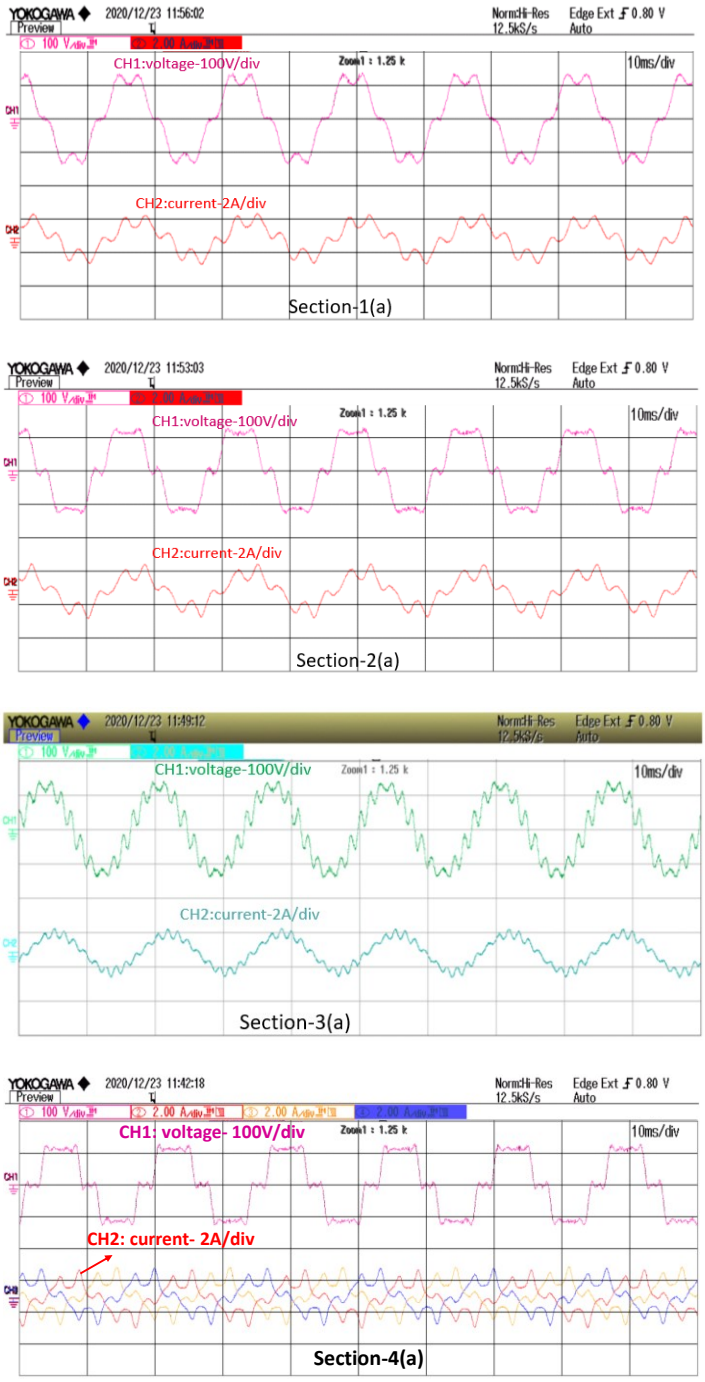


Fig. 3.4. Section-(a): steady state voltages and currents for real induction machine where machine input line voltage in CH1, actual current in CH2, reference current in CH3 and Section-1: 5^{th} harmonic, Section-2: 5^{th} + 7^{th} harmonics, Section-3: 11^{th} + 13^{th} harmonics, Section-4: 5^{th} +7^{th} +11^{th} +13^{th} harmonics.

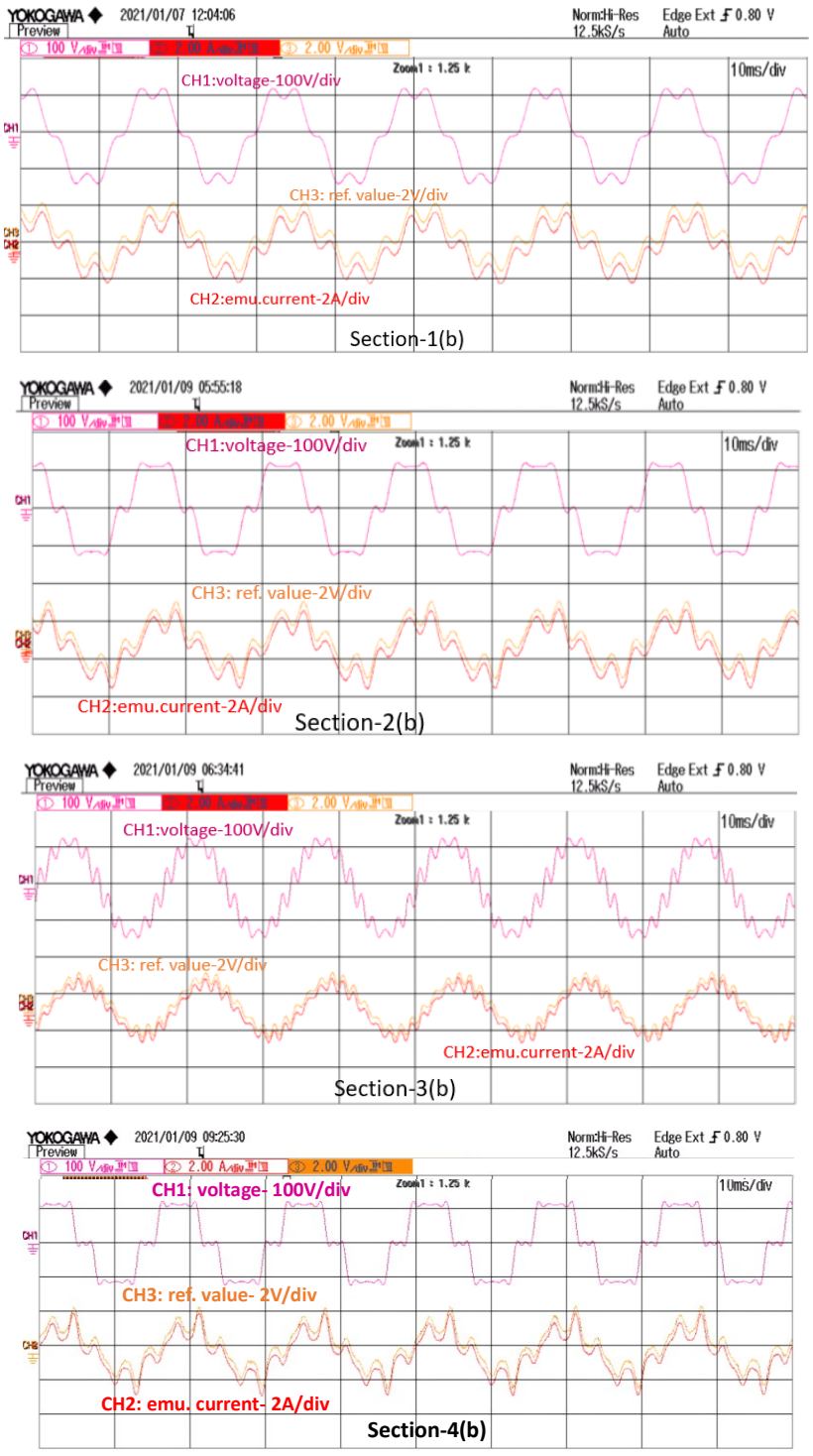
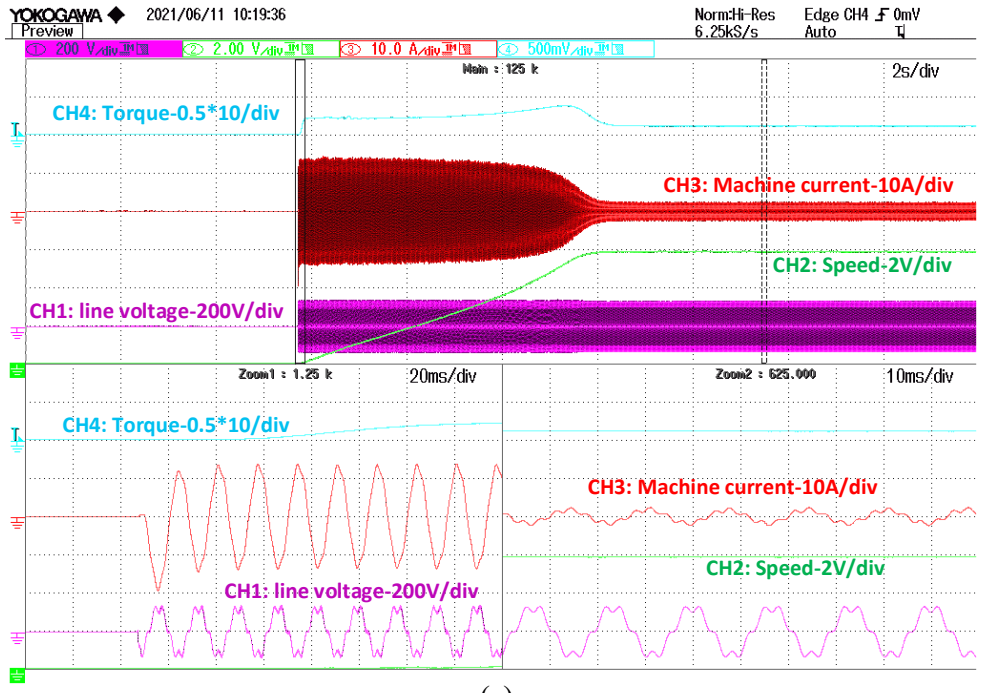
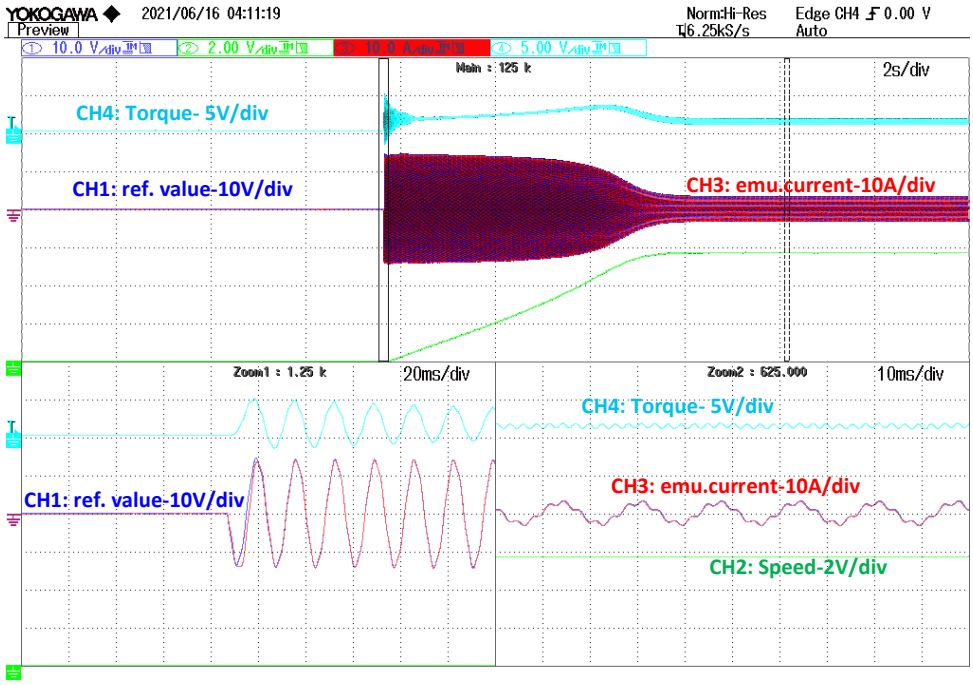


Fig. 3.5. Section-(b): steady state voltages, reference and emulator currents of proposed emulator where machine input line voltage in CH1, actual current in CH2, reference current in CH3 and Section-1: 5^{th} harmonic, Section-2: 5^{th} + 7^{th} harmonics, Section-3: 11^{th} + 13^{th} harmonics, Section-4: 5^{th} +7^{th} +11^{th} +13^{th} harmonics.



(a)



(b)

Fig. 3.6. During starting and steady states for 5th harmonics Section-(a): for real machine. Section-(b): for emulator.

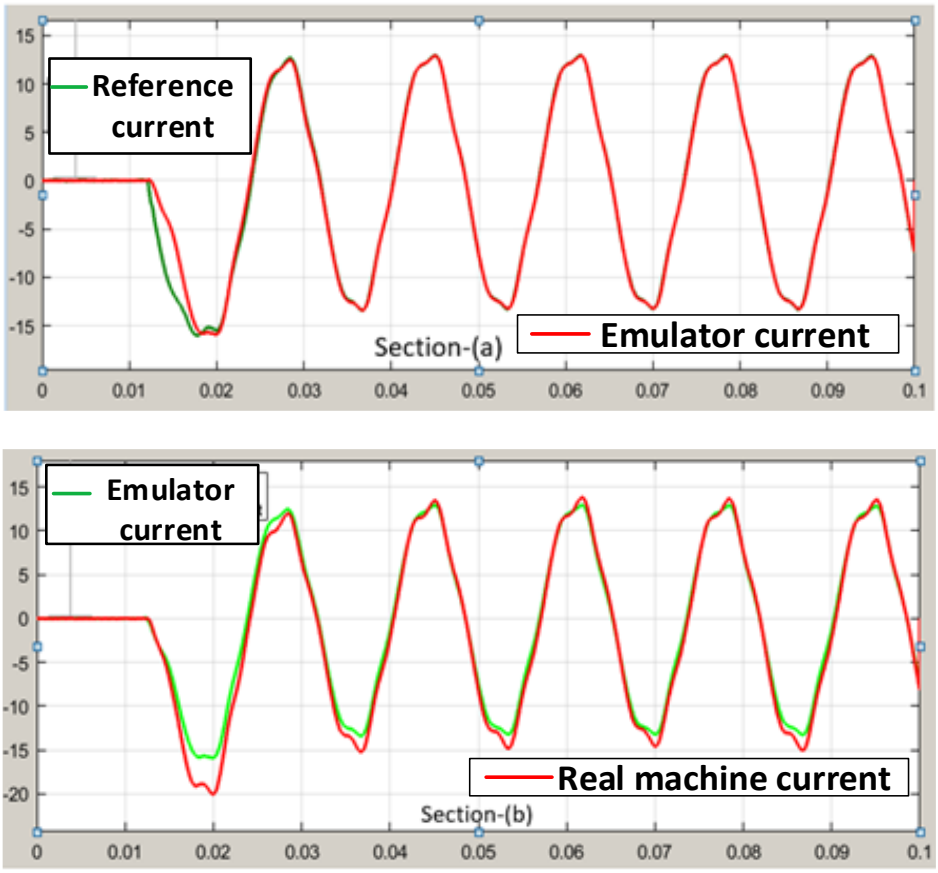
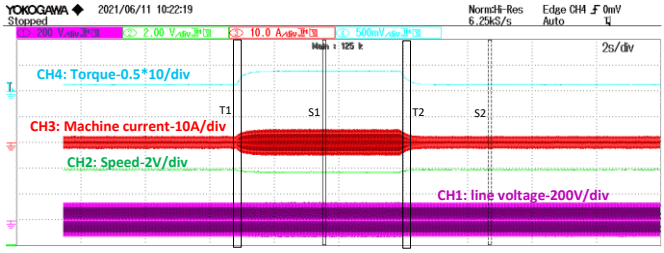
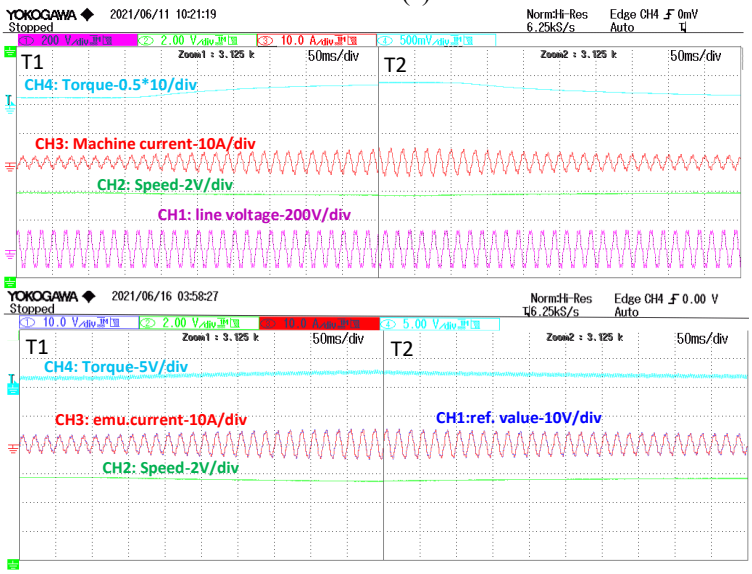


Fig. 3.7. During starting for 5th +7th combination of harmonics, Section-(a): reference and emulator currents, Section-(b): emulator and real machine currents.

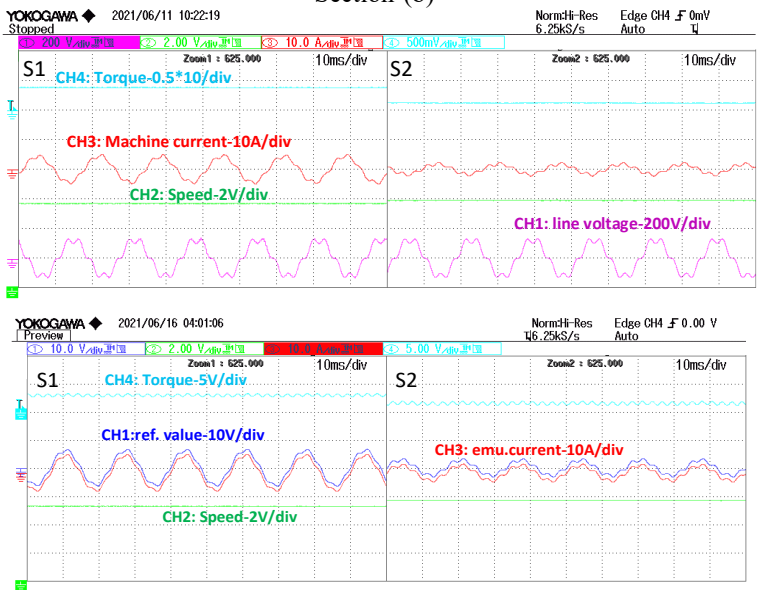
A load torque of $T_L = 2.5\ Nm$ is applied with the help of dyno mechanism. The efficacy of the emulator with respect to real machine is verified as shown in Fig. 3.8. The torque transducer displays the average value with its amplifying gain of '10'. The same is represented in the torque waveforms of Fig. 3.8. Both the loading and unloading conditions are checked for both the transient and steady states. The emulated torque shows accurate dynamic waveforms with oscillations unlike the real machine's torque transducer which gives only average values. The torque oscillations obtained for harmonic voltages are clearly seen in Fig. 3.6 and Fig. 3.8. The speed characteristic for the different harmonics is observed to be steady for both emulator and real machine. This due to the high mechanical inertia of the machine. Fig. 3.9 shows the experimental



Section-(a)



Section-(b)



Section-(c)

Fig. 3.8. Section-(a): Overall loading and unloading profile for $\boldsymbol{T_L}$ = 2.5 Nm Section-(b): loading (T1) and unloading (T2) transient profiles, Section-(c): loading (S1) and unloading (S2) steady state profiles for real machine and emulator.

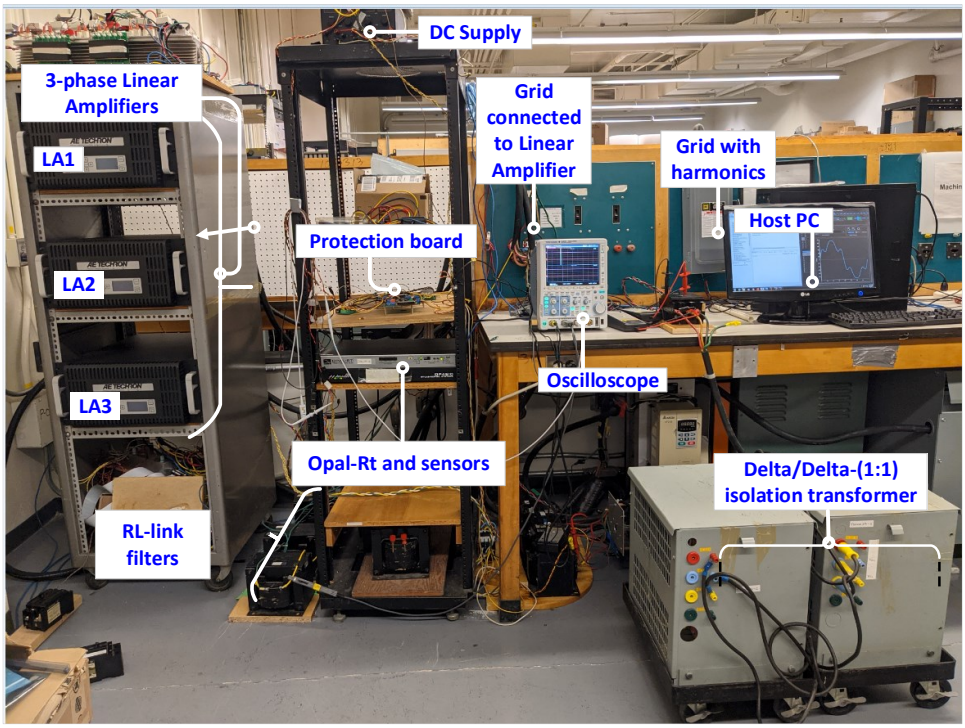


Fig. 3.9. Experimental setup for IM emulator with 3-phase linear amplifiers (LA1, LA2, LA3) for grid harmonics.

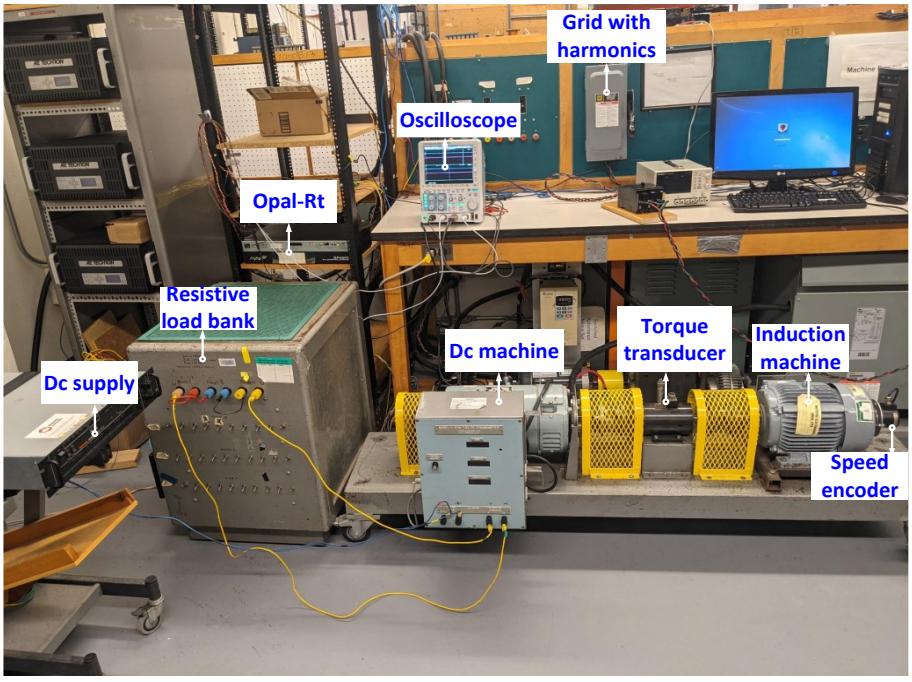


Fig. 3.10. Laboratory setup for validation with real machine interfaced with a dc machine during loaded conditions.

arrangement with a LA emulator, programmable power supply used for the introduction of grid harmonics and the other associated components (as per Fig. 3.1).

The real machine set up to obtain the results for validation is shown in Fig. 3.10. Since the machine is aligned with a dc machine for application of load in Fig. 3.10, the machine inertia (J) and friction constant (B) is found to an increase. Therefore, new values of J and B (refer appendix) are incorporated in the real time machine model during loading transients for dynamic accuracy of the emulator.

3.4 Summary

The experimental results with the real machine and emulator validate the accuracy of the novel emulator performance during grid harmonics. The resultant harmonics in dq currents due to grid harmonics are mathematically assessed and validated with simulation. Proper emulator control logic is suggested accordingly for good emulating accuracy. The higher bandwidth linear amplifiers used are effective enough to track the reference currents dynamically during starting and loading transients. Hence it is evident that the grid voltage harmonic emulation for the induction machine has been done with good accuracy. Dynamics of electromagnetic core saturation can also be included in the mathematical model for increased accuracy. This emulation can also be realized at high powers or with further increase in load with power electronic converters, but higher-order harmonics cannot be emulated with good accuracy. This is due to the bandwidth limitations offered by switching frequency of switches.

Chapter 4 Induction Machine Emulation for Open Circuit and Short Circuit Grid Faults

4.1 Introduction

Machine Emulation is the concept of imitating the electrical behavior of the machine by another power device in real time. The power hardware can be a switching amplifier or linear amplifier connected to physical RL-link filters in the real time control loop with the help of real time systems such as RTDS, D-space, Opal-RT etc. This essentially forms a power hardware in the loop (PHIL) system configuration [6] shown in Fig. 4.1. Over time, the challenging global goals demands this type of emulation technique since it is a risk-free alternative for field tests or preliminary testing. This type of virtual realistic simulation is also considered cost effective especially during the testing of various fault transients. Therefore, PHIL emulation is in demand for several applications including aerospace, military, electric vehicles, and grid applications [12], [15], [28], [54].

The present chapter considers induction machine emulation, as the machine is considered as a workhorse in several industries because of its rugged, cost-effective, and less hazardous nature [54]. The induction machines are prone to external fault transients (by supply systems, loads, etc.) along with internal faults.

For the internal faults such as stator inter-turn, rotor inter turn, broken bar faults etc., PHIL emulation techniques can be used for detecting such faults with motor current signature analysis (MCSA) in [32] and [33]. The detection of internal open circuit faults in the stator is discussed in [55].

In case of inverter supply systems, open circuit faults mainly occur due to lifting and crack of bonding wires in the module [56], and [57]. IM emulation for drive inverter faults is discussed in [31] for a single switch failure in one leg.

In consideration of external grid fault transients, typical network events such as open circuit faults and short circuit faults occur in the supply systems. Especially in distribution grids, about 78 to 88% of faults in the power system would arise generally [16]. This would greatly affect the

efficiency and performance of a plant or system employing machines. They impact other interconnected loads as well.

The influence of the induction machine on the grid under various shunt fault transients has been studied in detail in [54]. However, emulating a machine with series fault transients (open circuit faults) has not yet been reported in the literature. Normally open phase grid faults are evolving faults from bolted phase faults. They also occur from joint failures in overhead lines, cables etc., and the melting of fuse in one or more phases. They lead to extensive change of resistance and thus current severely drops.

After an open circuit fault of a few cycles, a reclosing operation leads to intense transients in current and electromagnetic machine torque. Such operations potentially can damage the load and shaft of the motor. In the process industries critical motors whose failure even for short periods can affect the entire plant non-operative for many hours and even days [58]. Therefore, the study of out of phase restarting with corresponding remedial measures is required to improve the ride through capability of the machinery. This capability allows the machine to stay connected to the grid terminals for few seconds even though the fault exists. Machine emulation can aid such studies and can potentially improve the performance of critical motors in many industries/plants.

Hence, considering the literature survey, it is significant to evaluate the response of the system under different open circuit fault transients with the help of emulation techniques.

In this chapter, the authors chose to emulate open circuit faults, auto reclosing transients, and short circuit grid faults with the help of the proposed induction machine PHIL emulator. The emulator is robust for all type of faults discussed. One of the important elements in the real time control loop of PHIL configurations (Fig. 4.1) is an accurate and precise mathematical model. The model is essentially executed in real time system. The mathematical model that is used in [6] is a dynamic linear dq model and in [54] the model is integrated with trapezoidal integration. Reference [36] shows a more accurate mathematical model which includes saturation of machine inductances. However, all the models that are discussed gives current as an output with a voltage input (I-out V-in). These models are suitable for testing transients such as unbalanced short circuit faults, loading transients, converter short circuit faults, voltage sag and swell etc., and especially for short circuit faults with voltage zero input. However, I-out V-in models are not suitable for open circuit fault transients. Because as the current drops to zero, the open circuited stator

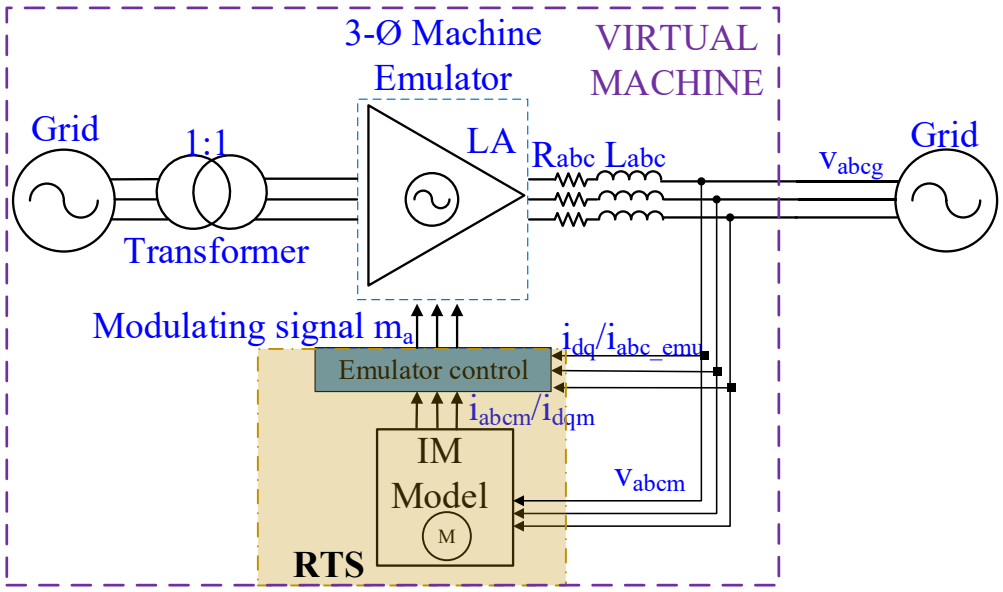


Fig. 4.1. Generic configuration of emulator.

terminals should essentially possess the back-emf of the machine. The back-emf is the induced emf in the stator terminals because of the decaying rotating magnetic field produced by the slowing down rotor.

Hence for such open fault transients V-out I-in models enables one to enter zero current to acquire V-out (i.e., back-emf) of the machine. The details are discussed in section 4.2. Fig. 4.1, shows the arrangement of the components of a generic PHIL test bench for executing grid faults. In addition to mathematical model, emulator control is also implemented in the Opal-rt real time system. The other physical components of the emulator are a) three phase linear power amplifiers b) RL link filters, c) Isolation transformer to isolate the grid and the emulator circuit which avoids circulating currents. The use of switching power amplifier promises high power operations but, the three phase linear power amplifiers are chosen in this chapter because of their high open loop bandwidth of 200 kHz, which ensures fast tracking accuracy. A LCL link filter with a transformer-based coupling avoids high frequency switching ripples, traveling, and reflected waves [27]. However, usage of simple RL link filters avoids complexity and provides good accuracy [6], [31], [36].

The focus of this chapter is to develop a robust PHIL test bed, which tests different asymmetrical open circuit, short circuit source faults in addition to different starting and loading transients.

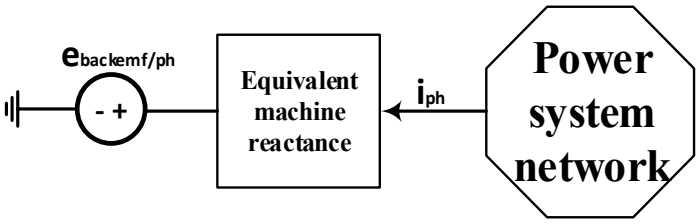


Fig. 4.2. Schematic of network interface modelling.

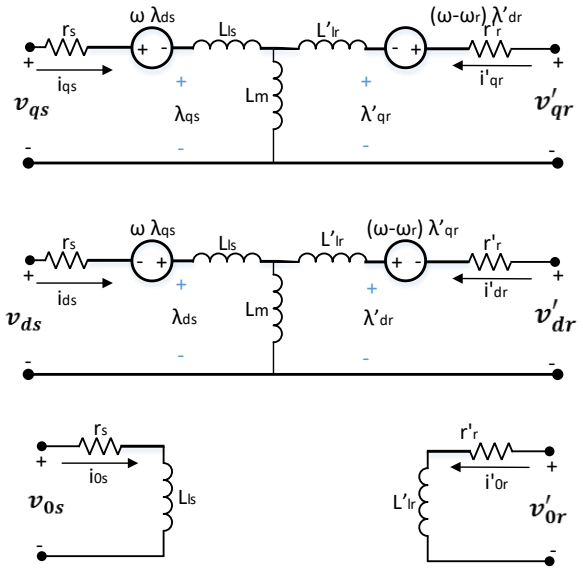


Fig. 4.3. The *dq* equivalent circuit of IM.

Detailed analysis of auto reclosing strategy is made. Identification of fault signatures is also done to aid fault diagnosis. This essentially requires,

a) Choosing an accurate mathematical model

b) Upgrade of mathematical model.

c) Finally, comparing the dynamics with that of the real machine for single phase, three phase open circuit faults and asymmetrical short circuit faults.

d) Enhancing the model for auto reclosing operation.

e) Identification of fault signatures for fault diagnosis.

4.2 Mathematical Modeling of Induction Machine

To access the V-out available at the terminals of the machine after an open circuit, the present research proposes to choose network interface modelling as shown in Fig. 4.2. This is basically called as voltage behind reactance (VBR) mathematical formulation [59]. References [60], [61] discuss VBR modeling in Electromagnetic Transient Program (EMTP) providing an interface with an external network comprising resistances and inductances.

The Opal-rt real time system chosen for the PHIL test bed, uses Matlab/Simulink. Hence, this chapter considers the voltage behind reactance formulation for the machine network interface in Matlab/Simulink and makes it adaptable for the emulation test bench configuration. For this, the chapter considers two types of models i.e., model-I and model-II in section 4.2.1and 4.2.2.

4.2.1 Induction machine model-I

In the case of open circuit grid faults, a real induction machine would reproduce a back-emf at the stator terminals. The same phenomenon can be replicated with the induction machine model - I. The modelling of it is a mathematical reformulation of equations derived from Fig. 4.3. Unlike the conventional voltage in current out models [6]-[14], [54] mathematical model-I employs a three-phase power simulation circuit as shown in Fig. 4.4. The values of the active and passive elements $\left(eabc, r^{d}_{abc}\ and\ L^{d}_{abc}\right)$ in the power circuit are very precise. Open circuit faults can be simulated with enable/disable circuit breakers in the model. The voltage ($v_{abcs} = e^{1}_{abc}$) after open circuit represents the back-emf of the machine. The equations governing the mathematical model-I are (4.1) to (4.13). The model considers a squirrel cage induction machine with rotor terminals short-circuited.

$$v_q^s = r' i_q^s + \omega L' i_d^s + pL' i_q^s + e'_q \tag{4.1}$$

$$v_d^s = r' i_d^s - \omega L' i_q^s + pL' i_d^s + e'_d \tag{4.2}$$

$$v_{0s} = r_s i_{0s} + L_{ls} p i_{0s} \tag{4.3}$$

$$\text{where, } L' = L_{ls} + \frac{L_m L_{lr}}{L_m + L_{lr}} \tag{4.4}$$

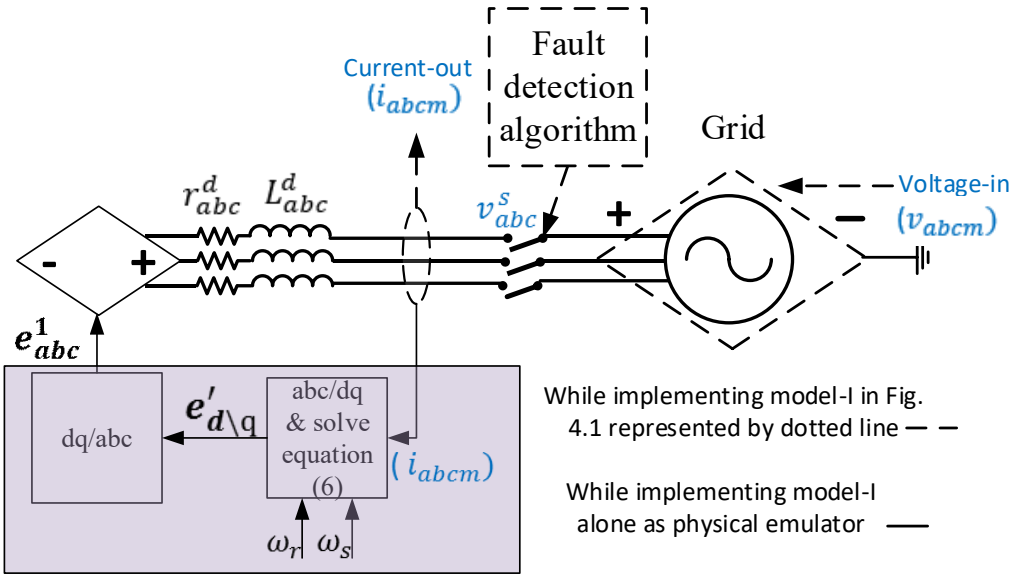


Fig. 4.4. Three phase power simulation circuit of model-I.

$$r' = r_s + \frac{{L_m}^2 r_r}{(L_m + L_{lr})^2} \tag{4.5}$$

$$e'_{d\backslash q} = \mp\omega_r \lambda''_{q\backslash d} + \frac{L_m r_r}{L_{lr}(L_{lr} + L_m)} \left(\lambda''_{d\backslash q} - \lambda'_{dr\backslash qr}\right) \tag{4.6}$$

$$\lambda''_{d\backslash q} = \frac{L_m \lambda'_{dr\backslash qr}}{L_m + L_{lr}} \tag{4.7}$$

The terms v^s_q, v^s_d, $\lambda''_{d\backslash q}$, L', r', $e'_{d\backslash q}$ are derived from fundamental dq modelling equations $v_{ds}, v_{qs}, v_{0s}, v'_{dr}, v'_{qr}, v'_{0r}, \lambda_{ds}, \lambda_{qs}, \lambda_{0s}, \lambda'_{dr}, \lambda'_{qr}, \lambda_{0r}$ of the induction machine from Fig. 4.3 [59]. Applying a *dq0-abc* transformation for (4.1) - (4.3) and (4.6), results in a three-phase circuit based equation (4.8).

$$v^s_{abc} = r^1_{abc} i^s_{abc} + L^1_{abc} p i^s_{abc} + e^1_{abc} \tag{4.8}$$

where,

$$r^1_{abc}\ or\ L^1_{abc} = \begin{bmatrix} R\ or\ L & M_r\ or\ M_l & M_r\ or\ M_l \\ M_r\ or\ M_l & R\ or\ L & M_r\ or\ M_l \\ M_r\ or\ M_l & M_r\ or\ M_l & R\ or\ L \end{bmatrix} \tag{4.9}$$

$$\text{where } R = r_s - 2M_r; \tag{4.10}$$

$$M_r = -\frac{1}{3}\frac{{L_m}^2 r_r}{(L_m + L_{lr})^2}\ ; \tag{4.11}$$

$$L = L_{ls} - 2M_l; \tag{4.12}$$

$$M_l = -\frac{1}{3}\frac{L_m L_{lr}}{L_m + L_{lr}} \tag{4.13}$$

However, equation (4.9) is a non-diagonal matrix, hence it is quite difficult to realise (4.8) into an independent per phase power circuit. Hence, to diagonalize the resistance and inductance matrix, equation (4.14), (4.15) are taken into account considering symmetry and the magnitude of zero sequence current is zero. This is because of isolated neutrals of the machine and grid due to presence of an isolation transformer.

$$\sum i_{abs} = 3i_{0s} = 0 \tag{4.14}$$

Differentiating the equation (4.14),

$$\sum \frac{d}{dt} i_{abs} = \frac{3d}{dt} i_{0s} = 0 \tag{4.15}$$

Therefore, the per phase algebraic manipulations in equation (4.8) is shown in (4.16) - (4.20) which results in (4.21).

$$\text{From (4.14) and (4.15), } i_a = -i_b - i_c \tag{4.16}$$

$$\text{and } \frac{di_a}{dt} = -\frac{di_b}{dt} - \frac{di_c}{dt} \tag{4.17}$$

By substituting (4.16) ad (4.17) in the per phase equation of (4.8) i.e., (4.18) gives (4.19)

$$v_a = Ri_a + M_r i_b + M_r i_c + \frac{Ldi_a}{dt} + \frac{M_l di_b}{dt} + \frac{M_l di_c}{dt} + e_a^1 \tag{4.18}$$

$$v_a = (R - M_r)i_a + (L - M_l)\frac{di_a}{dt} + e_a^1 \tag{4.19}$$

Similarly, equation (4.20) is derived for other phases as well.

$$v_{abc}^s = r_{abc}^d i_{abc}^s + L_{abc}^d p i_{abc}^s + e_{abc}^1 \tag{4.20}$$

$$r_{abc}^d \; or \; L_{abc}^d = \begin{bmatrix} R' \; or \; L' & 0 & 0 \\ 0 & R' \; or \; L' & 0 \\ 0 & 0 & R' \; or \; L' \end{bmatrix} \tag{4.21}$$

where $R' = (R - M_r)$;$L' = (L - M_l)$ and $i_{abc}^s = i_{abcm}$

The diagonal matrices r_{abc}^d and L_{abc}^d (from (4.21)) essentially forms a network interface model. The equivalent circuit derived from (4.20) is shown in Fig. 4.4.

The network interface model-I (Fig. 4.4) is employed in the "IM model" of generic emulator configuration circuit of Fig. 4.1. This serves as voltage-in current-out model. The grid voltages (v_{abcm}) in Fig. 4.1 are sensed and given to the "IM model" which is a network interface model- I shown in Fig. 4.4 (in dotted line)). The currents i_{abcm} sensed from model-I (Fig. 4.4) are taken out and given to the "emulator control" in Fig. 4.1. Aiming for robustness, model-I is initially checked for emulating 1) short circuit faults at the grid terminals and later for 2) open circuit faults shown in Fig. 4.1 in the present section.

1. Implementation of short circuit faults

Asymmetrical short circuit faults such as line to line and line neutral and double line to neutral at the emulator terminals in Fig. 4.1, are implemented with model-I. The asymmetric voltages (v_{abcm}) in Fig. 4.1 are fed into the dependent voltage source in Fig. 4.4 and the currents passing through r_{bac}^d, L_{abc}^d are taken as the reference output currents (i_{abcm}) from the model-I (Fig. 4.4).

a. Emulator control for model-I

The emulator PI controller regulates the emulator currents (i_{emu}) with respect to the reference currents(i_{abcm}). The dc input currents to the proportional integral controller are obtained by

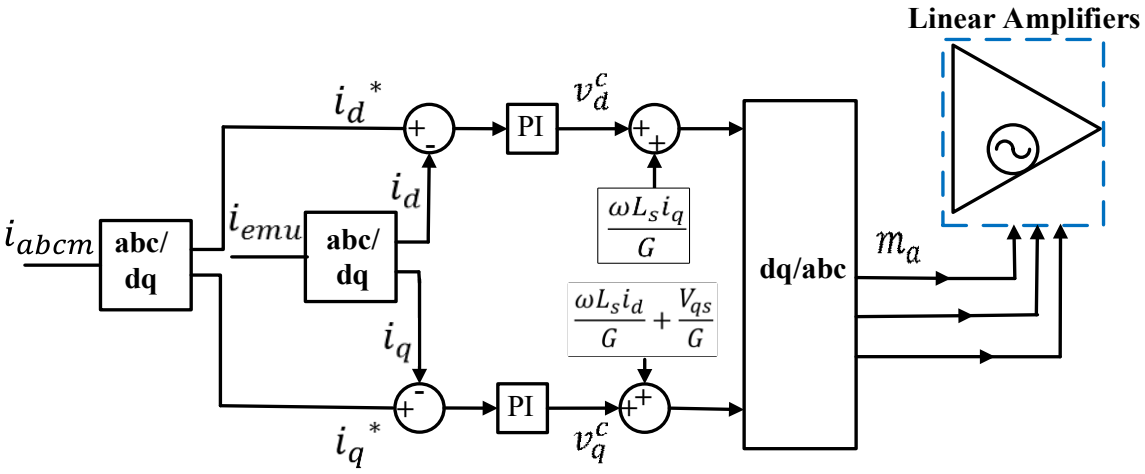


Fig. 4.5. Emulator control for model-I.

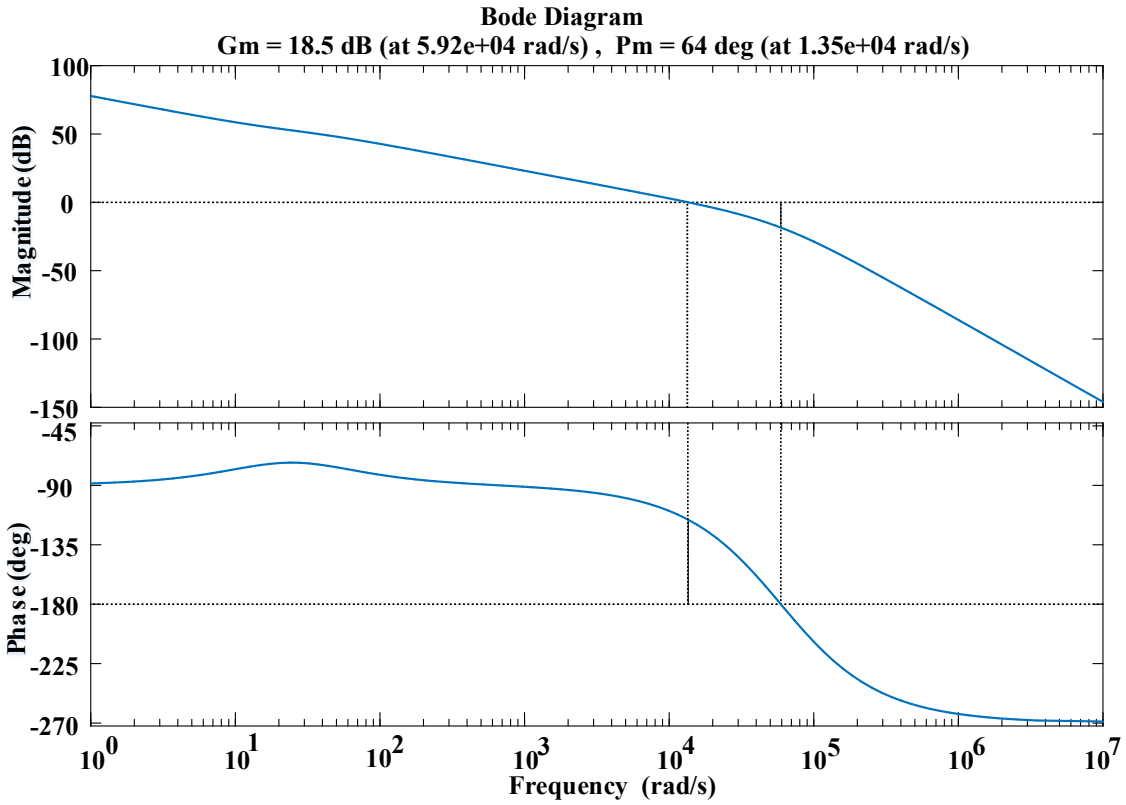


Fig. 4.6. Bode plot of the closed loop control system.

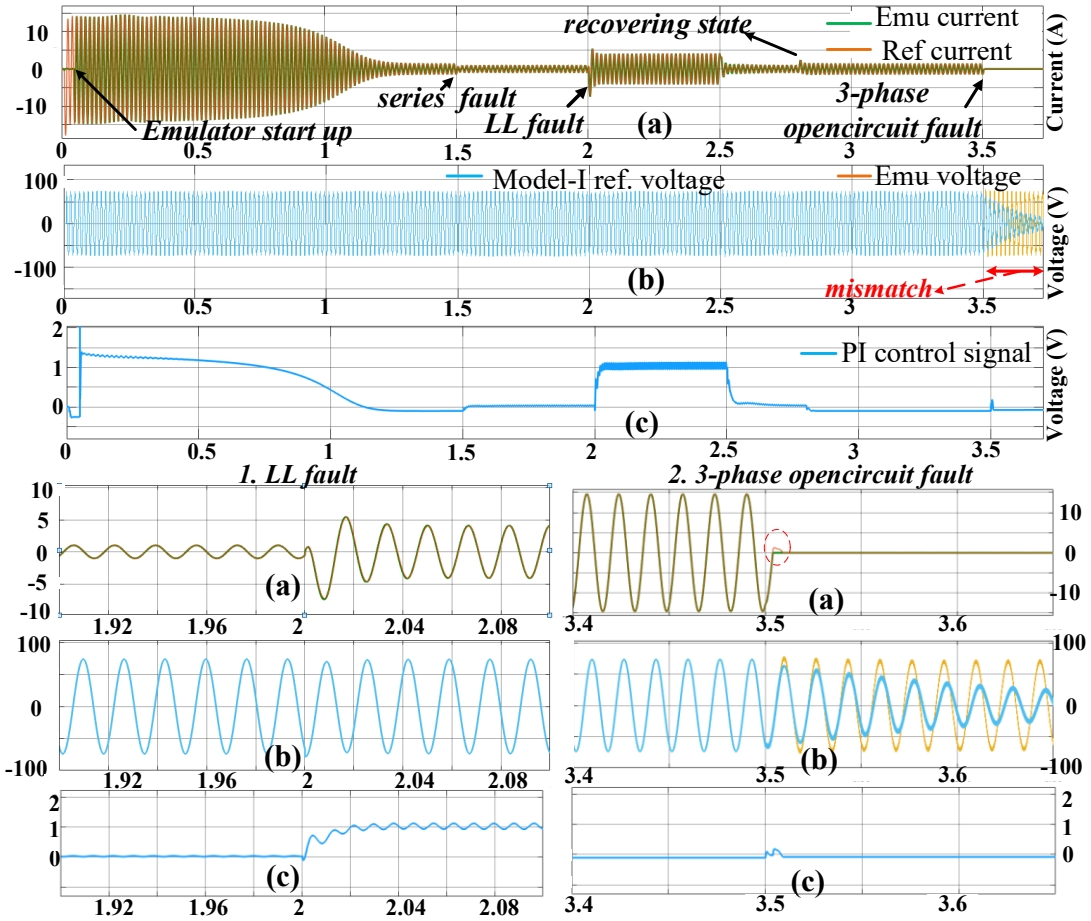


Fig. 4.7. Simulation results for emulator employing machine model-I for startup, series impedance fault, LL fault and their fault recovering states and final application of 3- phase open circuit fault (a) emulator and reference currents (b) emulator and reference voltages (c) Control signal of PI controller. The results are zoomed for 1. Line to line fault (zoomed for 0.2s) 2. Three phase open circuit fault (zoomed for 0.25s).

$abc\frac{}{dq}$ transformation. For a decoupled d-axis and q-axis current control, feed-forward terms (4.18), (4.19) are added to v_d^c and v_q^c voltages (Fig. 4.5). The resultant dq voltages (4.18) are transformed into abc modulating voltages (m_a).

$$v_d = v_d^c + \frac{\omega L_s i_q}{G} \tag{4.22}$$

$$v_q = v_q^c + \frac{\omega L_s i_d}{G} + \frac{V_{qs}}{G} \tag{4.23}$$

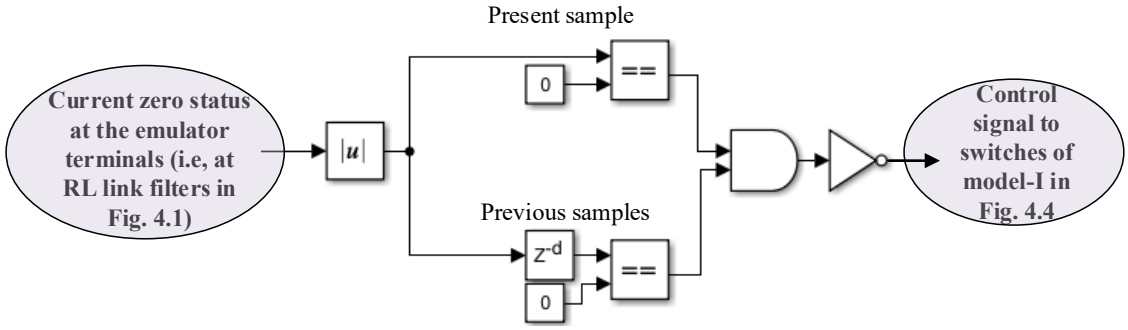


Fig. 4.8. Fault detection algorithm.

The PI controller gains are tuned considering the three main hardware components in the control loop. They are amplifier, RL-link filter, and the current sensor. The cascaded first order transfer functions of the amplifier, RL-link filter and the current sensor in time constant form are taken into account. The dominant pole of the system out of the three transfer functions is formed by the RL link filter. This is because of its comparative high time constant (0.03 s). The time constants of the linear amplifier are in the range of microseconds. Adding a PI transfer function to the system will nullify the effect of this dominant pole by the zero of the PI. The proportional and integral gains of the PI controller are tuned for a bandwidth of 1350 Hz and corresponding gain and phase margins of 18.5 dB and 64^0 respectively as per Fig. 4.6.

However, the asymmetrical short circuit faults produce second harmonic oscillations in the dc currents i_d and i_q [54]. In this case, the simple PI controller with the designed bandwidth is not enough for emulator control. Therefore, a proportional resonant controller corresponding to the second harmonic frequency (ω_h) is added to the PI for better tracking accuracy (4.24).

$$T(s)_{controller} = K_p + \frac{K_I}{S} + \frac{K_{PR} s\omega_h}{s^2 + s\omega_h + \omega_h^2} \tag{4.24}$$

Fig. 4.7 shows the simulation result analysis with model-I for start-up, series impedance fault and LL fault and later from shunt to series and series to post fault conditions. The emulator current and voltage possesses good tracking accuracy with respect to reference values.

1. Implementation of open circuit faults

During the emulation of induction machine for open circuit grid faults, the open circuit fault status (current zero status) in the emulation circuit (Fig. 4.1) is detected by the fault detection algorithm in Fig. 4.8 and sent to the machine model-I (Fig. 4.4). This opens the breakers in the respective phase/phases of the simulation circuit of model-I shown in Fig. 4.4. The voltage at the open terminals in the machine model-I (v_{abc}^{s} in Fig. 4.4) essentially called as back-emf. However, this back-emf cannot be replicated at the terminals of the RL- link filter in Fig. 4.1. This is because, by default the reference currents from model-I and the actual emulator currents are equal (to zero) during open circuit without interference of any controller action. Therefore, the control function of the PI controllers abruptly stops at the fault instant. The magnitude of the control signal settles at the previous steady state value shown in Fig. 4.7 (c). Consequently, modulating signal (m_a) controlling the power amplifier voltage is not proportional to the back-emf of the machine. This difference can be clearly seen in Fig. 4.7 (b). This implies the status of back-emf (e_{abc}^{1}) is attained only from machine model-I as reference voltage but not from the emulator.

One way to solve the problem is to replace the emulator current control with emulator voltage control. This requires the change of series RL link filter to LC link filter [14] to access the actual common mode voltage of the emulator. This increases further complexity of the emulator circuit. In addition, there are also some disadvantages associated. They are 1) complexity in emulator control, and 2) fault detection.

The implementation of emulator voltage control results in complexity in obtaining stability. Knowledge of the complex physical emulator system parameters and their individual delay times is required. The detection of faults can be done with zero rms current status. The rms current evaluation of the alternating current would need at least a fraction of a cycle (in milli seconds). Hence, a better approach to reduce the time delay is presented in Fig. 4.8, which compares the absolute value of the current for the present and previous samples of delay 'd' with zero. The usage of the logic gates greatly reduces the time delay from milli seconds (fraction of cycle) to microseconds (few samples), but still the emulator accuracy suffers because of (z^{-d}). The current and back-emf waveforms of the emulator for open circuit faults with the proposed fault detection approach are shown in Fig. 4.7 (a) and (b).

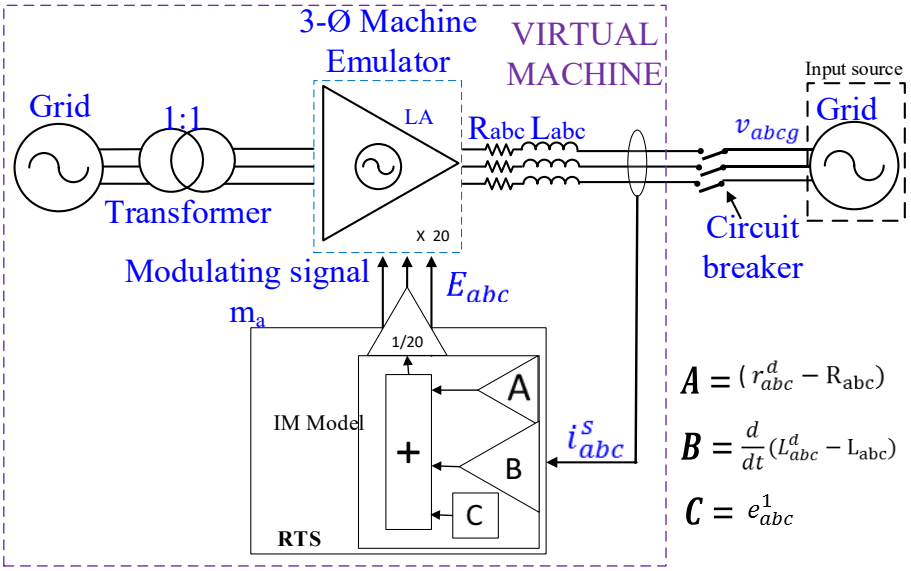


Fig. 4.9. The emulator configuration employing model-II.

The simulation result analysis shows that the emulator with model-I is robust in tracking the reference signal (current) for start-up and shunt fault conditions. The emulator voltage also replicates machine stator voltage given by model-I. The emulator inaccuracy is found only during the open circuit fault at 3.4 s. The reference current of model-I goes to zero after few delay samples of the actual emulator current (encircled in Fig. 4.7). The actual emulator voltage is no more tracking the decaying reference voltage (back-emf) of the model-I. The PI control signal is the same as before the open circuit fault followed by a transient. It indicates that control action is done to adjust the amplifier voltage as per previous steady state. Therefore, the emulator voltage is the same as before the open fault which is not the intended response.

Hence, it is concluded that emulation accuracy obtained with model-I for different grid faults is partial. The conventional emulator configuration with model-I bestows better performance and is robust for the different symmetrical and asymmetrical conditions in the grid, except for open circuit faults.

To emulate open circuit faults, another way of solving the problem is to alter the emulator configuration. Model-I in Fig. 4.4 can be practically executed as it is with physical elements. It can be briefly explained as: the terminals v^s_{abc} in Fig. 4.4, can be connected to the physical grid and the dependent voltage source generating e^1_{abc} can be replaced with a three-phase linear power

amplifier. The remaining system in the shaded region can be processed in real time. The r^d_{abc} and L^d_{abc} can act as RL-link filters. However, such physical emulator configuration faces challenges such as difficulty in obtaining the physical link filters with such precision. Even if the precision is obtained, the designed emulator setup is only valid for one specific machine with such r^d_{abc} and L^d_{abc}. This emulator setup is not adaptable for other induction machines with different r^d_{abc} and L^d_{abc}.Therefore, the present research proposes a robust emulator configuration with mathematical model –II, which avoids all the disadvantages mentioned for mathematical model-I.

4.2.2 Proposed induction machine model-II

Induction machine model- II is proposed to overcome the above difficulties for open circuit fault emulation and makes the emulator robust for any squirrel cage induction machine. Unlike model-I, it is a current-in voltage-out model as illustrated in Fig. 4.9. This modelling is done by considering the KVL equations of the machine model-I of Fig. 4.4, and that of the physical emulator with RL link filter in Fig. 4.1 as represented in (4.25), (4.26) respectively.

$$v_{abcm} = v^s_{abc} = r^d_{abc} i^s_{abc} + L^d_{abc} p i^s_{abc} + e^1_{abc} \tag{4.25}$$

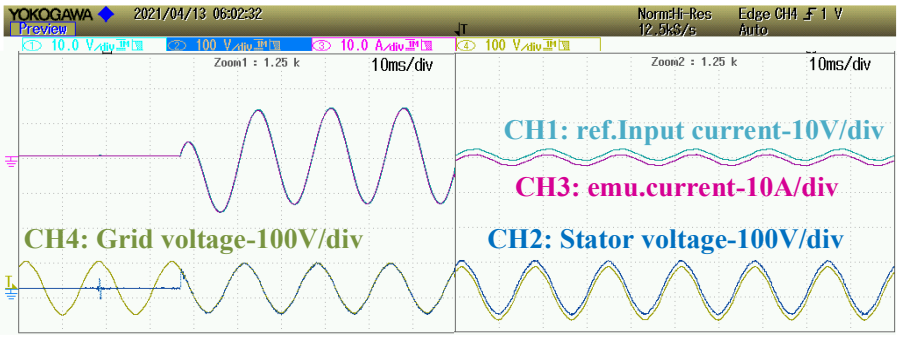
$$v_{abcm} = v_{abcg} = R_{abc} i^s_{abc} + L_{abc} p i^s_{abc} + E_{abc} \tag{4.26}$$

where R_{abc} and L_{abc} are three phase RL link filter parameters and E_{abc} is the linear amplifier terminal voltage.

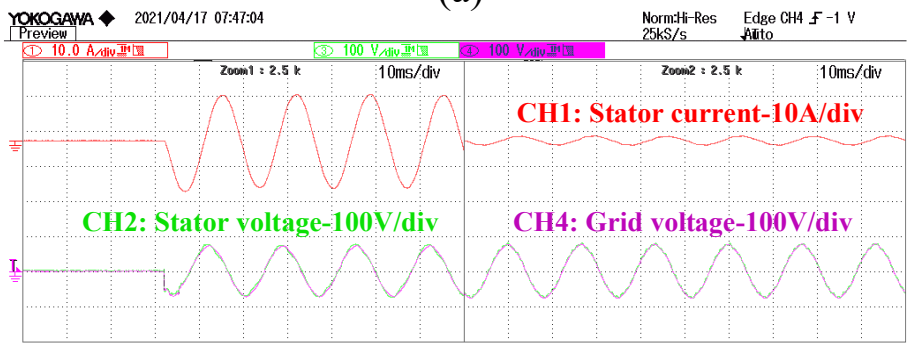
The main function of the physical emulator in Fig. 4.1 is to carry the same amount of stator current (i.e., $i_{abc_{emu}} = i_{abcm} = i^s_{ac}$), as drawn by network interface model-I, for the same input grid voltage (v_{abcm}) (4.17). Therefore, equating (4.21) and (4.22) gives the linear amplifier voltage representing back-emf (E_{abc}) (4.27). This emf represents the available voltage behind the reactance of the stator terminals during an open circuit as shown in Fig. 4.9.

$$E_{abc} = \left(r^d_{abc} - R_{abc}\right) i^s_{abc} + \left(L^d_{abc} - L_{abc}\right) p i^s_{abc} + e^1_{abc} \tag{4.27}$$

The voltage out signal of the proposed model (E_{abc}) directly feeds the power amplifier as shown in Fig. 4.9. Unlike in Fig. 4.1, it bypasses the need of emulator control and thus its complexity. In this model, the sensed current in the physical emulator circuit is directly given to model-II. It



(a)



(b)

Fig. 4.10. Starting and steady state conditions of the (a) proposed machine emulator and (b) real 5 hp machine.

neither needs rms evaluation nor the logic gates with sample delays. The input current in Fig. 4.9 is then multiplied with gains ‘A’,’B’ and ‘C’ which are mathematically modelled in contrast to the network interface modelling in Fig. 4.4. The emulation tracking accuracy is also not compromised. A good tracking accuracy of emulator voltage with respect to the reference voltage is obtained as shown in the result analysis section.

4.3 Result Analysis

The emulator test bench is developed as per the emulator configuration with the proposed model in Fig. 4.9. The high-performance linear amplifiers (LAs) of 100 kHz open-loop bandwidth are used for the chosen emulator configuration. The LAs possess maximum current and voltage ratings of 20 A and 208 V. This section presents the experimental results for open circuit grid faults, namely single phase and three phase open circuit faults. A brief overview of auto reclosing and fault diagnosis strategies for open circuit faults are discussed. The present research also validates starting and loading conditions. Finally, the proposed emulator robustness is proven not only for open circuit grid faults but also for short circuit faults.

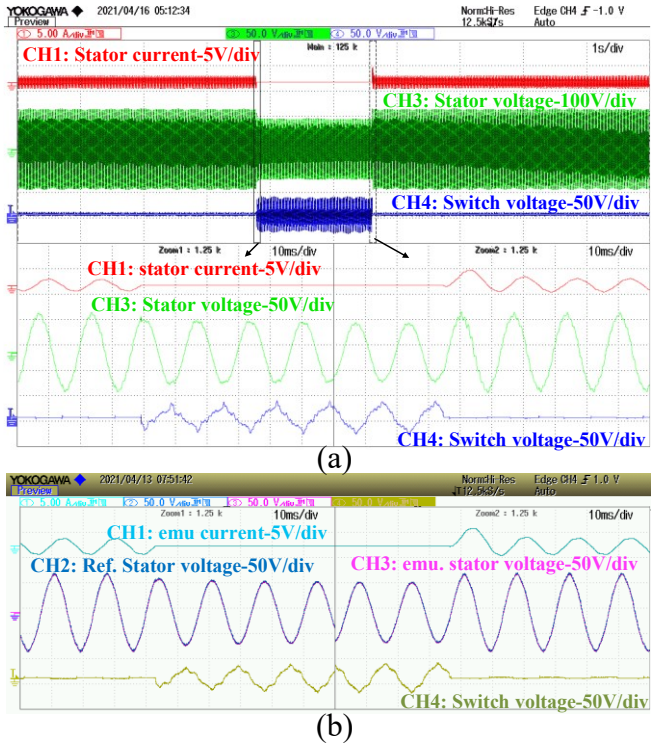


Fig. 4.11. Validation of emulation accuracy for single-phase open circuit fault with (a) real machine (b) proposed emulator.

The validating results for the 5 hp machine emulator not only prove the tracking accuracy with respect to the stator reference voltage (4.20) but also with respect to the real machine's voltage. The tracking ability is obtained by upgrading the mathematical model to current in voltage out type as discussed in section 4.2.2.

4.3.1 Starting transients

Fig. 4.10 illustrates, the startup transients and steady state conditions of the motor for an input line voltage of 90.5 V. Since the proposed model-II is a current in voltage out, Fig. 4.10 depicts that, when the current starts flowing in the emulator, the model-II reference stator voltage (4.20) starts to appear. It is observed that the induction machine emulator reference and grid voltages overlap at the instant of current input during starting conditions. The magnitude of the voltages matches the real machine as well in both transient and steady state conditions for the same input current profile. Thus, the proposed induction machine emulator has good voltage tracking accuracy during starting and steady states. During the experiment, proper care is taken to ensure that the physical emulator current is same as the model-II input current (ref. current).

4.3.2 Open circuit grid faults

For implementing open circuit grid faults, diac based solid state relays of voltage range 24 V-280 V are used. The experimental results obtained with the proposed induction machine emulator for different open circuit fault transients are validated with a physical machine. A fault diagnosis analysis is made with respect to positive and negative sequence components, the dq- current circles and the appearance of harmonics during faults with the help of simulation results in Matlab/Simulink.

A single-phase open circuit fault on Phase A of a real machine is shown in Fig. 4.11(a). The zero current results in the reduction of stator voltage in the respective phase. The increase in the voltage across the terminals of the opening switch is also observed. The machine emulator in Fig. 4.11(b) repeats the same trends in magnitudes of voltages and currents with respect to real machine. The fault is resumed and the transient states of back-emf and currents are validated with real machine results.

Fault application and recovering conditions for three phase open circuit faults are shown in Fig. 4.12. The waveforms of the stator phase current, voltage across the terminals of the solid-state relay and stator phase voltage are recorded for the real machine (Fig. 4.12(a)) and the emulator (Fig. 4.12(b)). The fault application is magnified in zoom-1 and its recovering is magnified in zoom-2. Both set of waveforms have good match proving the robustness of the emulator for such severe faults. Harmonics are observed in the stator voltage of the real machine during recovering state. This could be due to rotational nonlinearities, which are not considered in the machine model.

1. *Auto reclosing on load*

A load of 1.8 Nm is applied before application of an open circuit fault. A run-down test is performed on the emulator and the droop in stator voltage magnitude with respect to time/phase angle is observed in terms of spirals in Fig. 4.13. The spirals are essentially the polar plots. A three-phase open circuit fault is applied to the real machine. The fall in stator voltage of the real machine is recorded by polar plot in Fig. 4.14. It is observed that the polar plots of the emulator and the real machine follow the same trend. Therefore, the analysis of auto reclosing transients can be explained with the help of one of these spirals. During an open circuit fault in Fig. 4.15, when speed reduces to 1500 rpm from 1770 rpm, the breaker resumes its normal state. The stator terminal

voltage in Fig. 4.15 is considered for the polar plot in Fig. 4.14. and an analysis of the reclosing transient current is validated with the waveforms in Fig. 4.15. The stator voltage while applying the fault is 47.13V∠240.5^0. When speed of the machine falls to 1500rpm, the stator voltage reaches 6.756V∠210^0 after 21.5 cycles. The grid voltage during recovering state is observed to be approximately 47.15V∠307.1^0. The instants of fault and recovering can be exactly plotted in Fig. 4.14 with good accuracy. Therefore, the transient current spike magnitude can be assessed with the knowledge of machine impedance Z_m (4.28), (4.29).

$$I_{reclosing} = \frac{(V_{stator}\angle\theta_s - V_{grid}\angle\theta_g)}{|Z_m|\angle\theta} \tag{4.28}$$

$$Z_m = r^d_{abc} + j\omega\, L^d_{abc} \tag{4.29}$$

The reclosing current is calculated to be -17.96 A∠4.63^0 with a peak current of -25.405 A. Since the zero-crossing enabled for switches allow the current to flow at the next zero crossing, the positive peak current would be lower than |25.405| A. The same is observed in Fig. 4.14 with a positive peak current. Therefore, this graphical and mathematical analysis can be done in the emulator in prior to installation of machine.

The transient spike of the torque is considered for auto reclosing strategies as well. In Fig. 4.16, the average torque given by the real machine's torque transducer, filters the transient oscillations of the torque. Moreover, the bandwidth of the average torque transducer limits the sharp rise and fall in the torque during the fault and its recovery. However, the emulated torque maintains almost the same average value but clearly shows the transient spike in torque during reclosing operation. The transient torque oscillations are almost double that average torque. Therefore, considering the transient states of current and torque gives sufficient knowledge to the operator for automated safe re-closures.

2. Short circuit grid faults:

The proposed emulator not only emulates open circuit faults of the grid but also with short circuit faults. A line-to-line shunt fault is chosen for a fault impedance of 5 Ω. A series fault impedance of 10 Ω is applied before application of the shunt fault. It is evident from Fig. 4.17, that the emulator able to replicate the results for both series and shunt impedance faults. The emulated

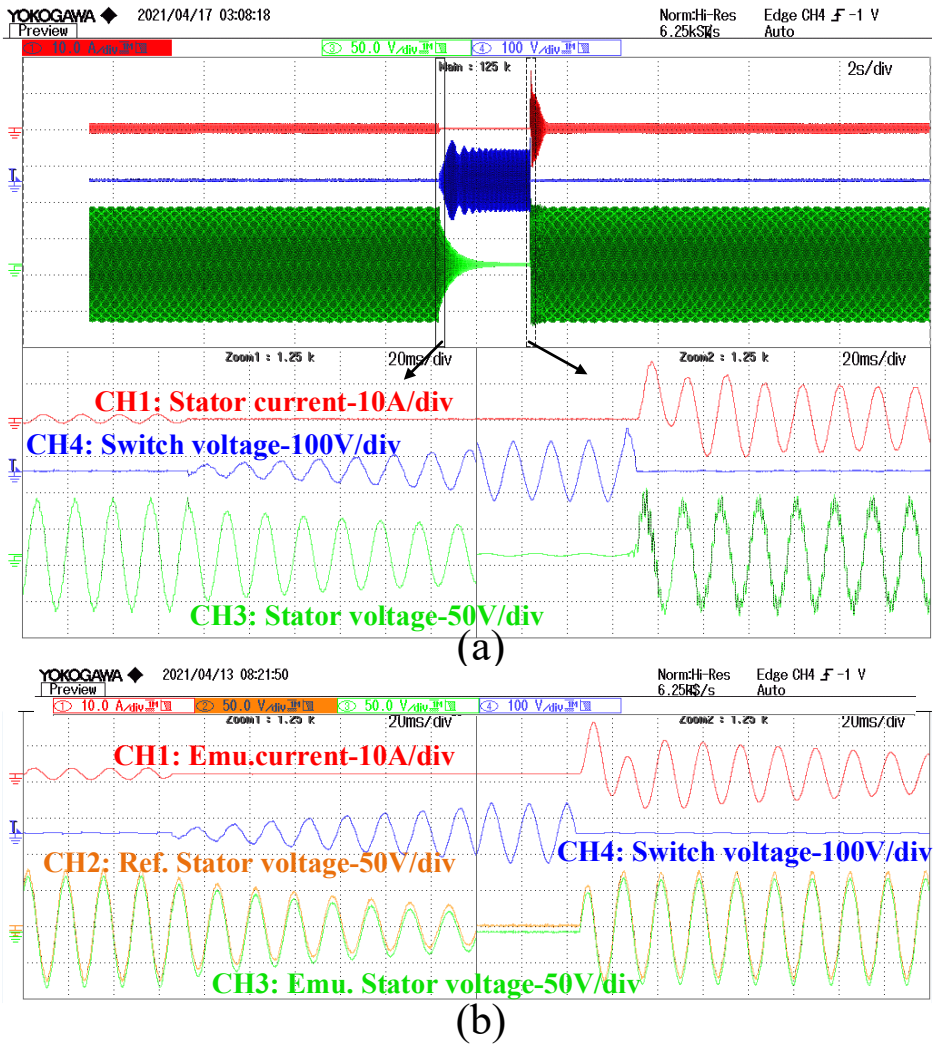


Fig. 4.12. Validation of emulation accuracy for three-phase open circuit fault with (a) real machine (b) proposed emulator.

voltage is very similar to the reference input voltage for short circuit faults, which proves the robustness of the proposed emulator for grid faults.

3. *Fault diagnosis:*

The purpose of developing an emulator test bed not only serves the purpose of testing grids or connected loads but also can be used in fault diagnosis. This is possible by identifying fault signatures of the machine emulator for several test applications of faults. The fault signatures that are identified from the results are $i_d - i_q$ current circles and negative sequence components. Theasymmetry in the current due to impedance faults result in elliptical $i_d - i_q$ plots [55]. The

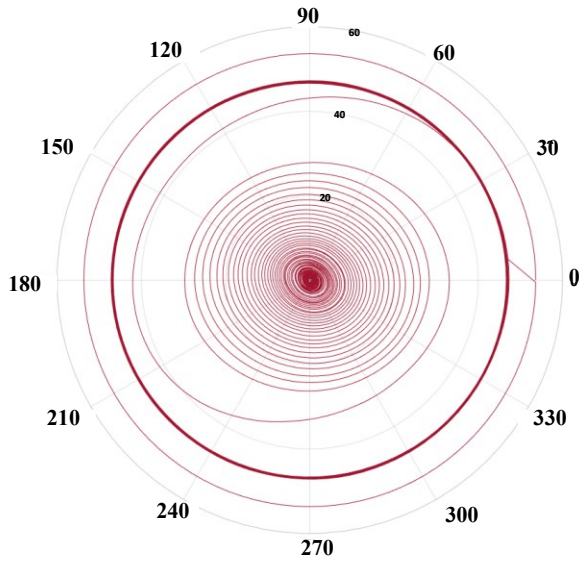


Fig. 4.13. Fall in stator voltage of the proposed emulator during run down test

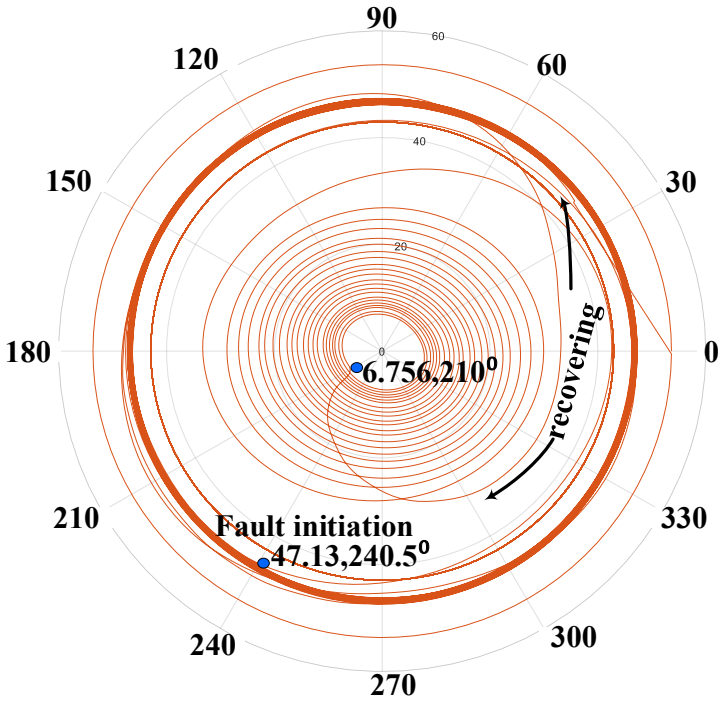


Fig. 4.14. Fall and rise in stator terminal voltage during fault and auto reclosing of the real machine.

same phenomenon is observed for the discussed short circuit and open circuit faults as shown in Fig. 4.18 (a). Initially the machine is under balanced steady state condition for a voltage of 52.5 V. Therefore, the dc content of synchronously rotating i_d and i_q currents is shown with a single

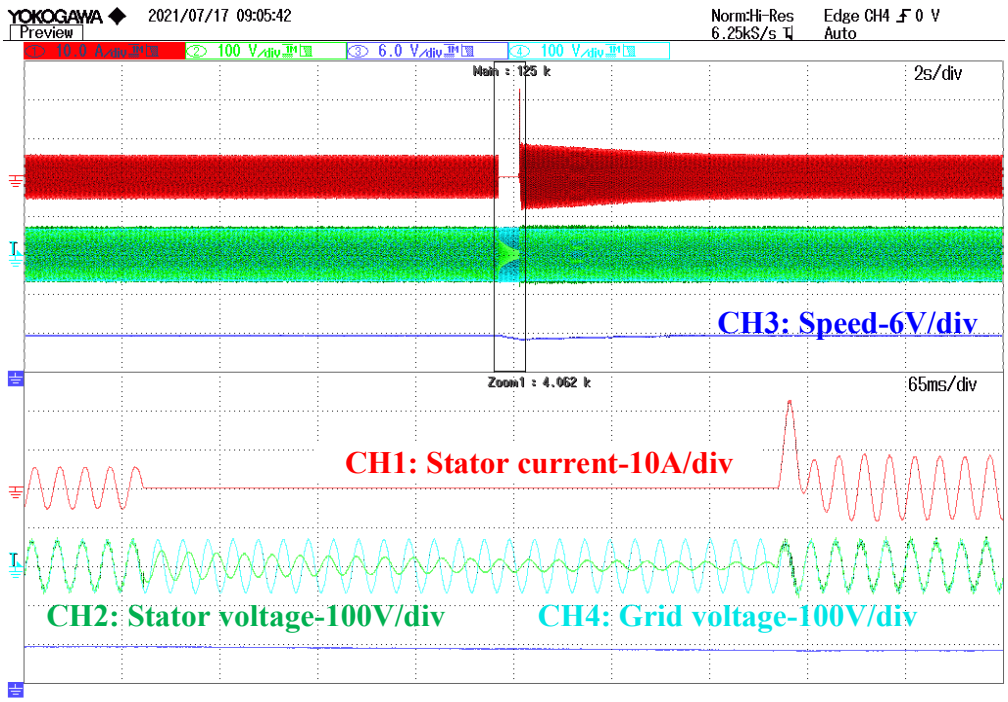


Fig. 4.15. Fault and auto reclosing profiles of the real machine

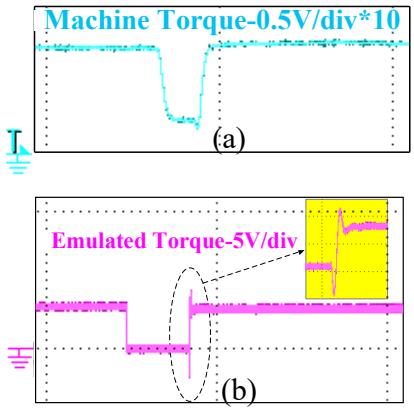


Fig. 4.16. Torque profile during fault and recovering state for (a) machine (b) emulator.

"dot" (red) (Fig. 4.18 (a).). Later a series impedance asymmetrical fault results in an ellipse (orange) encircling the "dot" under "no fault-steady state" as its center. A single-phase open circuit grid fault (series fault) also results in an ellipse with its major axis parallel to the x-axis with the same center. The application of an asymmetrical line-to-line fault (shunt fault) also leads to an ellipse but with its center, shifted. Reference [54] discusses, that asymmetry leads to a rise in

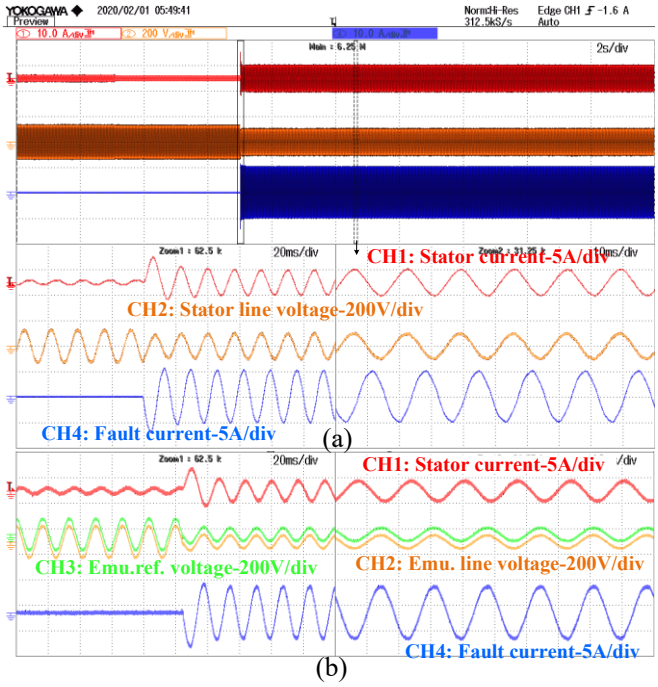


Fig. 4.17. Validation results for testing series impedance fault to LL fault and during LL fault (a) for real machine (b) with the proposed emulator.

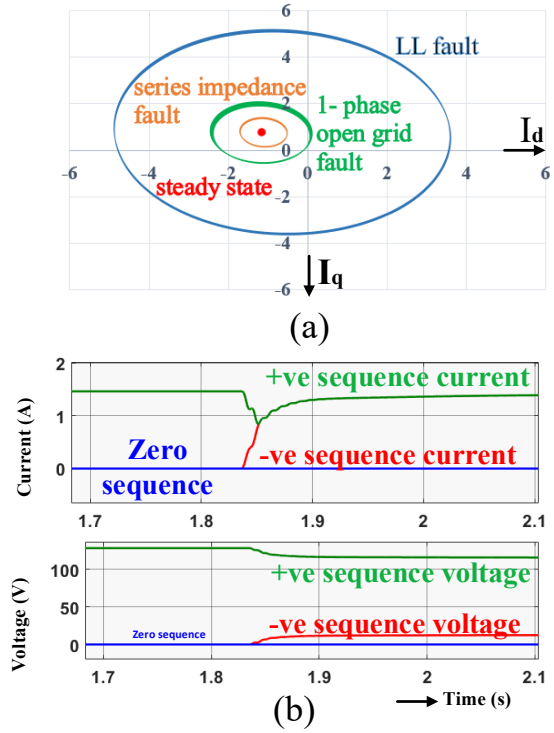


Fig. 4.18. post-processed (a) i_d, i_q plots for grid faults (b) sequence components of emulator current and voltage for 1-ø open circuit grid faults.

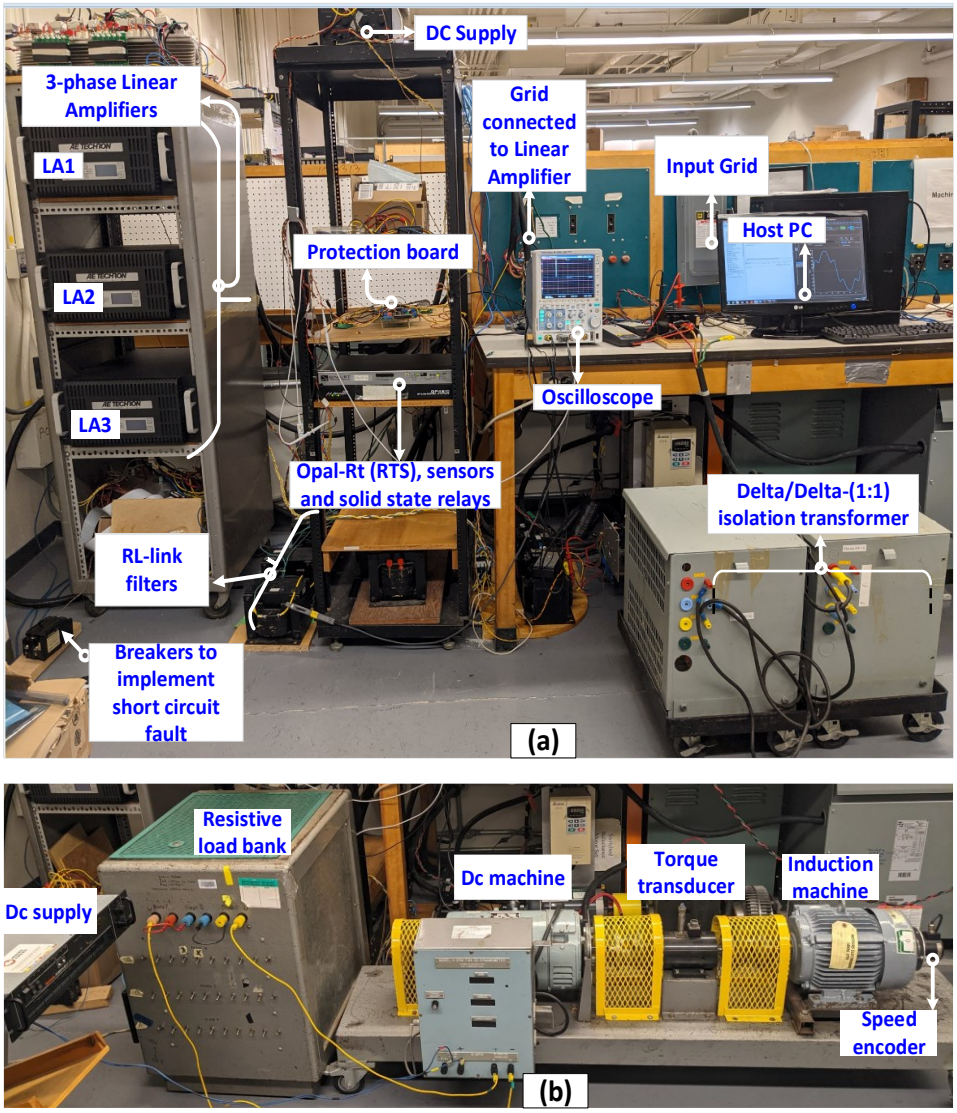


Fig. 4.19. Experimental setup for (a) proposed emulator (b) real machine.

negative sequence components in current. The same signature is observed for the emulator voltage also for single-phase open circuit fault in Fig. 4.18 (b). Hence, identification of the fault signatures with the same trends for a physical machine in a complex plant (in Fig. 4.18) leads to easy, fast and less expensive fault diagnosis. Fig. 4.19 shows the experimental set-up for emulator and real machine.

4.4 Summary

The proposed emulator test bench is shown to be robust for all series and shunt asymmetrical grid faults. This type of testing has no net power loss, since the power drawn from the grid will be sent back to the grid. The complexity of the emulator configuration has been reduced by eliminating the emulator controller. The emulator test results for single phase and three phase open circuit faults and asymmetrical short circuit fault, series impedance fault and finally for starting and loading conditions, possess high tracking accuracy with respect to the real 5 hp machine. The developed test bench helps in testing and developing better algorithms for auto reclosing operations. The operators in a plant can easily diagnose the type of the fault during a machine mal functioning with fault signatures from the emulator. The proposed emulator can be used to develop fault remedial strategies for different types and combinations of faults. Machine ride through capabilities can be assessed. Since the LAs in the machine emulator limits the maximum current to 20 A, the fault severity can be increased by increasing the power amplifiers bandwidth and power.

Chapter 5 Induction Machine Emulation for Variable Frequency Drive Converter Faults

5.1 Introduction

In the area of electric drives and traction, the probability of failure is higher for drive converters. The failure occurs mostly on account of excessive voltages and currents. Heating is also a major reason due to high frequency operation, and high ambient temperatures [62]. If the converters are designed for high power, the failure of the components in the converter module poses a serious problem. Various converter faults include, rectifier diode short circuit fault, dc bus fault (i.e., capacitor short circuit fault or an earth fault on dc bus), short circuited transistor switch fault and open circuited transistor switch fault, line to line or line to ground faults at the machine terminals [63].

In order to handle the faults, the converters are employed with various protection strategies [64], [65], fault detection algorithms [66], fault diagnosis approaches [62], [67] and fault tolerant control strategies [68] for safe and continued operation. Before commissioning the drive inverter for electric vehicles, the discussed strategies or control algorithms, need to be tested with a prototype. Testing the control algorithms for drive converter faults at higher power, risks the life of the machine. This type of testing demands more time, effort and resources.

Therefore, to overcome the testing disadvantages, the present research work focuses on emulating a real machine for testing drive converter faults in real time. It omits the need of a physical machine unlike in [62], [64]- [68]. Electric machine emulation is the process of imitating the dynamic behavior of electric quantities. It is done by another electric power device. In [69] the induction machine (IM) emulation is done by a three-phase transformer. However, the motor and the transformer parameters must match which is practically not feasible for drive testing. Another method of emulation of naval propulsion unit is done with a low power machine [70] which incurs power loss. Therefore, a power electronic amplifier controlled by emulator control mechanism in real time serves as emulator. This emulation method requires no net power loss as the power drawn from the grid is given back to the grid. A power hardware in loop technology is used for this machine emulation [6], [10], [31], [39], [54], [71]. It requires power electronic devices and RL link

filters as the power hardware or emulating hardware in the real time emulator control loop. This type of virtual realistic simulation uses real-time systems such as RTDS, D-space, Opal-RT etc. The emulator controller employed in the real-time system requires the reference quantities from the machine mathematical model. The accuracy of the model plays an important role in the emulator accuracy. The PHIL configuration layout is shown in detail in section 5.3 of the chapter.

This chapter considers testing a two-level voltage fed drive converter supplying an induction machine emulator for testing different converter faults. The converter faults that are considered in this chapter, are chosen based on the literature survey. A simulation analysis is made in [72] for short circuit faults on a diode of a diode bridge rectifier and short circuit faults on a transistor of a three-phase multi-level converter. The former test on the diode blows the input power supply fuses due to high currents and shuts off power to the rectifier. The later test on the transistor turns into a symmetrical short circuit fault. However, to experimentally implement the short circuit faults on the converter module or on the dc bus, involves high risk. The line-to-line and line-to-ground faults at the supply terminals resemble asymmetric grid faults, which are emulated in [39], [54] with a VICO model. An open circuit transistor switch fault on a converter leg clamps the positive or negative peak of the current of that particular phase current which is simulated in [10] and emulated in [39] with a VICO machine model. An open circuit switch fault generally results from the mal operation of the gate driver (transistor base drive). However, multiple open switch faults of all legs or one leg means an open circuit of all phases or a single-phase respectively. This fault is tested with an emulated PMSM drive in [31]. A PMSM produces back-emf because of the presence of the permanent magnetic field and motion of the rotor. This concept is emulated in [71] with a VICO model which also has the information of the back-emf. A fault detection algorithm used in [71] switches the current out signal to back- emf out signal to the emulator controller to emulate voltage. A similar concept for back-emf during open switch faults is also applicable for induction machines, because of its residual magnetism. The IM back-emf information mainly depends on the rotor, stator currents and rotor speed. However, this is not the case with a PMSM as its back-emf is only dependent on the rotor's constant flux and speed. Hence, to emulate open circuit faults for an induction machine, the status of currents and speed is essential.

From the literature survey, the emulation of an induction machine for open circuit switch faults has not yet been reported. Hence, the present research work considers emulation of an induction machine for open circuit transistor switch faults in the converter. An open loop v/f control is chosen

to emulate this condition. Reference [27] discusses induction machine emulation with high-fidelity RTDS linear model. [31], [10], [73] and [74] discusses IM emulation with an Opal-Rt real time simulator with linear machine model. [74] uses a nonlinear VICO mathematical model for emulating a self-excited induction generator. However, a VICO model (conventional model) [10], [27], [31], [71], [73], [74] is no longer feasible for this emulation because of a lack of information of back-emf. The concept of the CIVO model in machine emulation is used to extract the rotational back-emf of the machine. The Voltage Behind Reactance (VBR) models discussed in [59], [60], [61], [76] are of CIVO type with external network interfacing using ATP, and EMTP programs. Reference [60] discusses the inclusion of magnetic nonlinearities in the VBR model and proposed a backward differential formula approach to avoid algebraic loop errors. [76] discusses a nonlinear five-phase induction machine VBR model and proposed to incorporate high core loss resistance in the model to rule out algebraic loop errors. The present chapter discusses a nonlinear VBR model (CIVO type), variation of reactances during an open circuit fault and change of emulator configuration in contrast with the classical emulator configuration [6], [10], [31], [39], [54], [71]. The nonlinearities of the machine are found from [10] and incorporated into the CIVO model. The algebraic loop errors that occur during the process of emulation of the model are overcome by employing a low pass filter with sufficient bandwidth at the input of the model. Fault signatures are identified for a single switch and multiple switch gate driver faults with the help of emulation techniques. This aids in the fault diagnosis, localization, and fault isolation procedures in a complex drive with the help of artificially intelligent algorithms discussed in [55], [77], [78].

The main contributions of the present research include: (1) developing a high-performance PHIL test bed for converter open circuit switch faults, (2) proposing a novel emulator configuration adaptable to CIVO models, (3) identification of dynamic variation of nonlinear machine reactances during an all-switch open circuit fault, (4) checking the emulator robustness against a real 5 hp machine for different single switch faults, multiple switch faults, starting and speed changing conditions (6) Identifying the fault signatures for the faults. The overall structure of the chapter is organized as follows: Section 5.2.1, describes the difficulty associated with the VICO model for open circuit fault emulation and section 5.2.2 discusses the CIVO model suitability, section 5.2.3 discusses the upgrade of the model with inductance nonlinearities and their effect

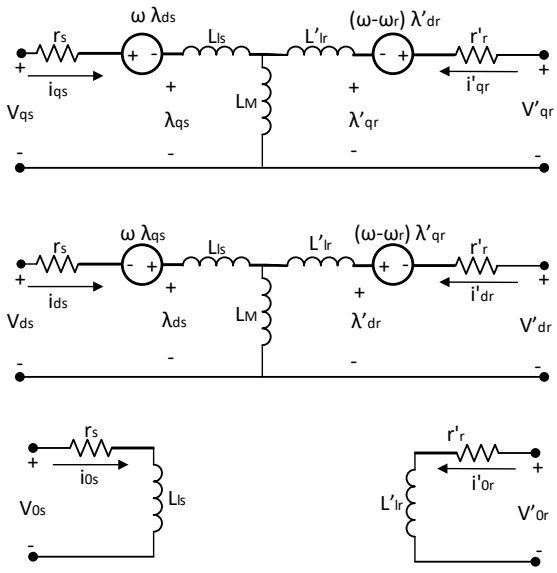


Fig. 5.1. The *dq* equivalent circuit of IM.

during an open circuit. Section 5.3 discusses the reorganized emulator structure and its considerations. Section 5.4 discusses experimental results with the emulator validated with the real induction machine and fault signatures. Finally, the chapter ends with the conclusion and future scope.

5.2 Modeling constraints for drive converter switch faults

5.2.1 Voltage-in Current-out model

A dq equivalent circuit for the VICO model is shown in Fig. 5.1 and is considered for implementation of drive converter faults. The power source for the model is a drive converter as shown in Fig. 5.2 (a). The faults that are considered in the drive converter are an open circuit-single switch and multiple switch faults (Fig. 5.2 (b)).

A single switch fault on the top side of a leg clamps the positive half-current and similarly, a single bottom switch fault clamps the negative half current under steady state as shown in Fig. 5.3. However, a complete gate driver unit failure resembles an all-switch open circuit fault at the input

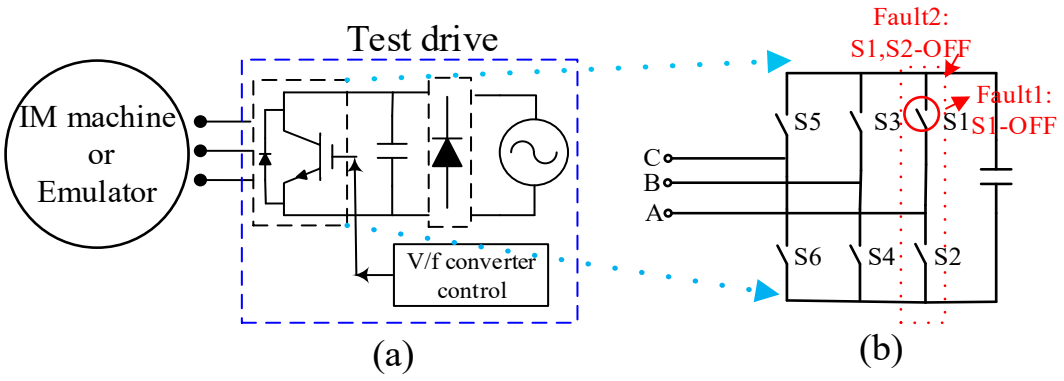


Fig. 5.2. V/f input drive for induction machine emulation (a) drive converter configuration (b) converter faults.

terminals. A sudden open circuit at the three phase line terminals leads the machine's speed to decay and the slip gradually reaches to unity. Therefore, the rotational back-emf associated with the slip of the machine, is decaying. This back-emf equals the stator terminal voltage. This leads the stator current going to zero instantaneously. However, this phenomenon is not exactly replicated for a VICO (signal-based) model (of Fig. 5.1) for a complete gate driver unit fault. As shown in Fig. 5.4, the model stator current is not abruptly zero at the instant of fault. Instead, there is a sudden spike in current with an abrupt zero input voltage. This is because, at the instant of all-switch fault, the input phase voltage signal measured becomes zero (which is not the reality). Therefore, the zero-input voltage signal to the model is interpreted as a short circuit across the stator terminals. The PLL for the zero-input voltage gives the synchronous speed (ω) zero. As per Fig. 5.1, the dependent voltage sources in the circuit are no more dependent on $'\omega'$. A sample d-equivalent circuit for the total gate drive fault is shown in Fig. 5.5 (drawn from Fig. 5.1). Therefore, it can be inferred from Fig. 5.5, that an instant of all-switch fault results in a current spike in the stator circuit (i.e., for i_{ds} and i_{qs}). This result contrasts with the zero current reality.

Hence, this chapter considers the voltage behind reactance formulation for the machine network interface in Matlab/Simulink. The misinterpretation of zero voltage for an all-switch fault is corrected with the improved mathematical formulation, which results in a CIVO model. The

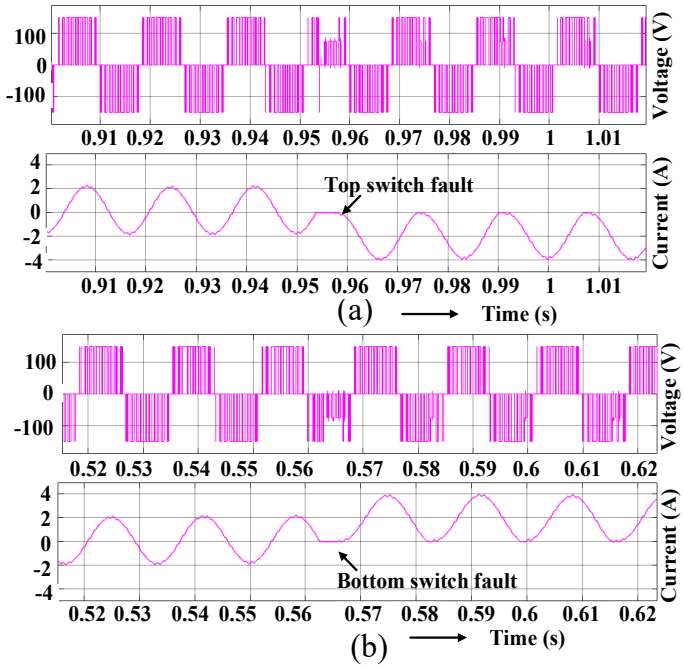


Fig. 5.3. Line voltage and stator current waveforms for a single switch fault in one leg for a VICO model (a) Top switch fault (b) Bottom switch fault.

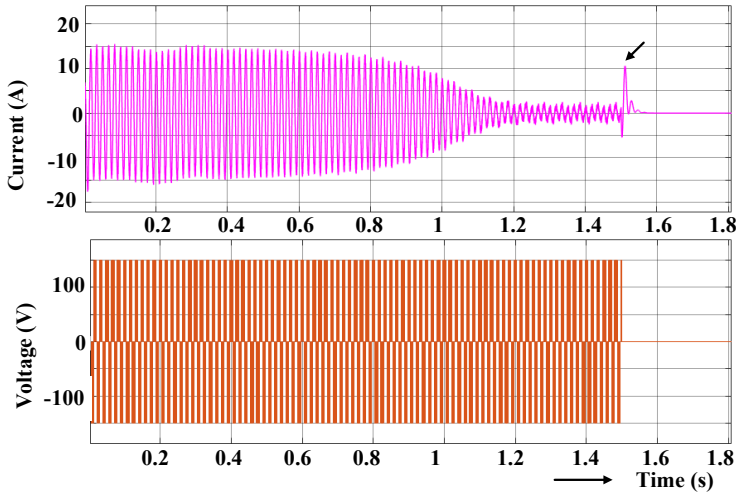


Fig. 5.4. VICO model stator current and input line voltage for starting and all-switch fault conditions.

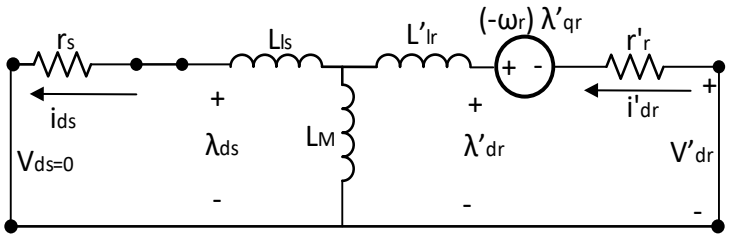


Fig. 5.5. Sample *d*-equivalent circuit for zero voltage signal under full gate-drive unit fault.

suggested model is also made adaptable for emulation test bench configuration, which is discussed in detail in section 5.2.2.

5.2.2 Current-in Voltage-out model

The chapter discusses a voltage behind reactance (VBR) mathematical formulation [59] to access the voltage available at the machine terminals. VBR modeling in Electromagnetic Transient Program (EMTP) is discussed in [21], [24]. VBR modeling provides an interface with an external power network consisting of passive elements such as resistances and inductances as shown in Fig. 5.6.

The values of the active and passive elements $\left(e^1abc, r^d_{abc}\ and\ L^d_{abc}\right)$ in the power circuit are very precise. The voltage after open circuit represents the back-emf of the machine ($v^s_{abc} = e^1_{abc}$). The equations governing the mathematical model are (5.1) to (5.13) for per phase values of resistances '$r'_s$and 'r'_r , leakage inductances 'L'_{ls} and 'L'_{lr}, mutual inductance 'L'_m .The superscripts and subscripts with 's' denotes stator and with 'r' denotes rotor. The modelling considers a squirrel cage induction machine with rotor terminals short-circuited. The reformulated dq modeling equations of induction machine [23] are derived from Fig. 5.1 and are given in (5.1) to (5.7). The voltages are denoted by 'v', emf is denoted by 'e' and currents are denoted by 'i'.

$$v^s_q = r^1 i^s_q + \omega L^1 i^s_d + pL^1 i^s_q + e^1_q \tag{5.1}$$

$$v^s_d = r^1 i^s_d - \omega L^1 i^s_q + pL^1 i^s_d + e^1_d \tag{5.2}$$

$$v^s_0 = r_s i_{0s} + L_{ls} p i_{0s} \tag{5.3}$$

$$\text{where, } L^1 = L_{ls} + \frac{L_m L_{lr}}{L_m + L_{lr}} \tag{5.4}$$

$$r^1 = r_s + \frac{{L_m}^2 r_r}{(L_m + L_{lr})^2} \tag{5.5}$$

$$e^1_{d\backslash q} = \mp\omega_r \lambda^1_{q\backslash d} + \frac{L^1_m r_r}{L^2_{lr}} \left(\lambda^1_{d\backslash q} - \lambda_{d\backslash qr}\right) \tag{5.6}$$

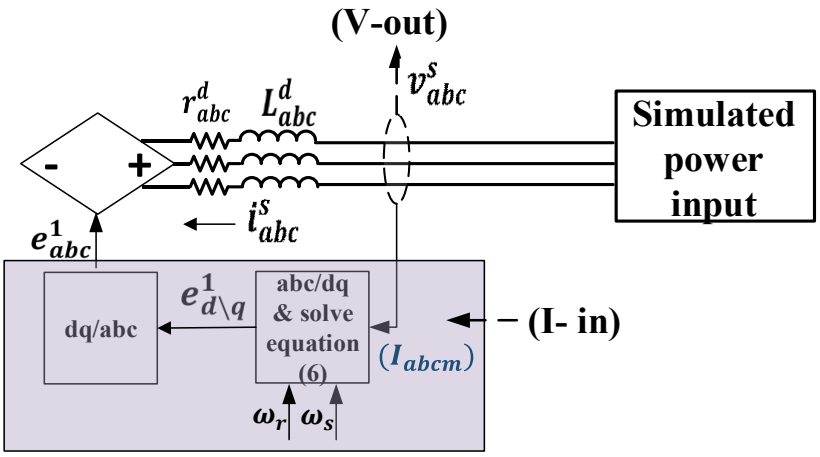


Fig. 5.6. Network interface modelling of induction machine.

$$\lambda^1_{d\backslash q} = \frac{L_m \lambda_{d\backslash qr}}{L_m + L_{lr}} \tag{5.7}$$

where, $\lambda_{d\backslash qr}$ can be obtained from Fig. 5.1.

A per phase circuit-based equation (5.8) is obtained by applying the *dq0-abc* transformation for (5.1) to (5.3) and (5.6).

$$v^s_{abc} = r^1_{abc} i^s_{abc} + L^1_{abc} p i^s_{abc} + e^1_{abc} \tag{5.8}$$

where,

$$r^1_{abc} \; or \; L^1_{abc} = \begin{bmatrix} R \; or \; L & M_r \; or \; M_l & M_r \; or \; M_l \\ M_r \; or \; M_l & R \; or \; L & M_r \; or \; M_l \\ M_r \; or \; M_l & M_r \; or \; M_l & R \; or \; L \end{bmatrix} \tag{5.9}$$

where $R = r_s - 2M_r$; (5.10)

$$M_r = -\frac{1}{3}\frac{{L_m}^2 r_r}{(L_m + L_{lr})^2}\ ; \tag{5.11}$$

$$L = L_{ls} - 2M_l; \tag{5.12}$$

$$M_l = -\frac{1}{3}\frac{L_m L_{lr}}{L_m + L_{lr}} \tag{5.13}$$

Equation (5.8) is difficult to realize into a circuit, because of the cross-coupling terms M_r, M_l. Hence, considering symmetry,

$$\sum i_{abs} = 3i_{0s} \tag{5.14}$$

Differentiating equation (5.14),

$$\sum \frac{d}{dt} i_{abs} = \frac{3d}{dt} i_{0s} \tag{5.15}$$

By substituting equations (5.14) and (5.15) in equation (5.8) results in (5.16) with diagonalized resistance and inductance matrices r^d_{abc} *and* $L^d_{abc}$with $R = r_s - 3M_r$ and $L = L_{ls} - 3M_l$ respectively. It essentially eliminates the coupling terms M_r and M_l unlike in (5.9) and forms a network interface modelling as shown in Fig. 5.6.

$$v^s_{abc} = r^d_{abc} i^s_{abc} + L^d_{abc} p i^s_{abc} + e^1_{abc} + 3M_r i^s_{0s} + 3M_l \frac{d}{dt} i^s_{0s} \tag{5.16}$$

5.2.3 Consideration of saturation nonlinearities

The real induction machine is subjected to a no-load test by varying the input voltage till 125% of the rated voltage and the magnetization characteristics are obtained. The variation of magnetising reactance (imaginary part of the impedance) for different sets of voltages and currents are recorded. The magnetising reactance (X_m) obtained is high at low current operations and low for higher currents (5.17). A blocked rotor test is conducted as per [10] to determine the nonlinearities in the machine leakage reactances. The induction machine stator and rotor leakage reactances are given in (5.18) and (5.19).

$$X_m = -108.9 * \mathrm{e}^{-2.3 * i_m} \quad + 113.9 * e^{-0.1097 * i_m} \tag{5.17}$$

$$X_{ls} \approx 1.919 \tag{5.18}$$

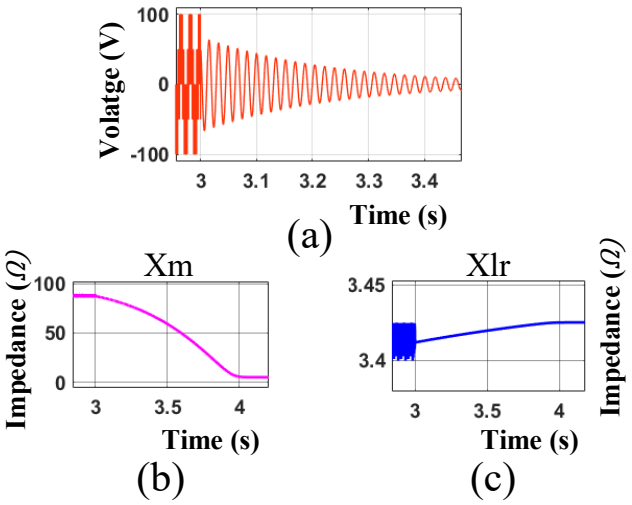


Fig. 5.7. Variation of (a) line voltage, (b) magnetizing inductance, and (c) rotor leakage reactance of IM at the instant of "complete gate driver ("all-switch") fault.

$$X_{lr} = 0.54 * e^{-0.008363*i_r} + 2.885 * e^{-0.004108*i_r} \tag{5.19}$$

The calculation of corresponding inductances at a specific control frequency is given by (5.20).

$$L_{m\backslash ls\backslash lr} = \frac{X_{m\backslash ls\backslash lr}}{2 * pi * f} \tag{5.20}$$

Therefore, the values R or L in r^d_{abc} and L^d_{abc} of (5.16) are no more constant but dynamic. This is because the values of L_m and L_{lr} in M_r (5.10) are current dependent. Hence, employing these variable resistances and inductances in the equation (5.16) results in a non-linear CIVO model.

The simulated nonlinear model is tested for "all-switch faults" of the input drive converter at 60 Hz for a dc bus voltage of 150 volts. After the instant of fault, the nature of the output line voltage given by the model changes from switched to sinusoidal which is observed in Fig. 5.7 (a). The nonlinear variation of machine's inductances towards zero value of currents is also clearly observed in Fig. 5.7(b) and (c). The magnetising inductance X_m settles at a nonzero value indicating remanence of the stator core. The X_{lr} slightly rises with gradual fall in rotor current. This is because the unsaturated areas of the T shaped iron laminations at the circumference of the rotor results in high leakage flux. Stator leakage reactance X_{ls} is almost constant. This is due to uniform and symmetrical air gap between stator and rotor teeth.

5.3 Emulation difficulties and Considerations

To emulate the induction machine's dynamic behaviour for drive converter faults, a conventional emulator configuration in Fig. 5.8 (a) [6], [10], [31], [39], [54], [71] is taken as a reference. The discussed CIVO model in Fig. 5.6 can replace the VICO model in the real time system (RTS). The voltage controlled linear power amplifiers in the Fig. 5.8 (a) can be directly controlled by the proposed model's output voltage (v^s_{abc}), (of Fig. 5.6) eliminating the emulator current controller. However, this scheme of emulation suffers from the following difficulties:

1. The network arrangement of Fig. 5.6 replicates the external network of the emulator in Fig. 5.8 (a). Therefore, the "simulated power input" to the model in Fig. 5.6 should exactly replicate the voltage characteristics of the test drive of the emulator (in Fig. 5.8(a)). Hence, for the discussed switch fault applications, the instant of the switch fault at the emulator input must be first identified by some 'fault detection scheme' and later imitated by the "simulated power input" of network interface model in Fig. 5.6. This complicates the emulation procedure and emulation accuracy is affected by the delay in fault detection.
2. The values of resistances $\left(r^d_{abc}\right)$ and inductances $\left(L^d_{abc}\right)$ in the model (Fig. 5.6) must also replicate the resistances and inductances of the emulator link filter (R and L). For the machine model employing nonlinearities, this is not possible, as the model resistances and inductances $\left(r^d_{abc}\right)$, $\left(L^d_{abc}\right)$ becomes dynamic (i.e., variable).

Therefore, to eliminate the difficulties, the machine model is upgraded with respect to the emulator hardware configuration. This is done by considering the KVL equation of the emulator network in Fig. 5.8 (a) given by (5.21). Also, the KVL equation of the network interface model in Fig. 5.6 is given by (5.22).

$$V_{abcg} = R_{abc} i^s_{abc} + L_{abc} p i^s_{abc} + E_{abc} \tag{5.21}$$

$$v^s_{abc} = r^d_{abc} i^s_{abc} + L^d_{abc} p i^s_{abc} + e^1_{abc} \tag{5.22}$$

Since, the internal network of the machine model must replicate the external network, the input voltages and currents drawn for both the networks must be same. Therefore, considering (5.23), the equation for the voltage out signal representing back-emf is given by (5.24).

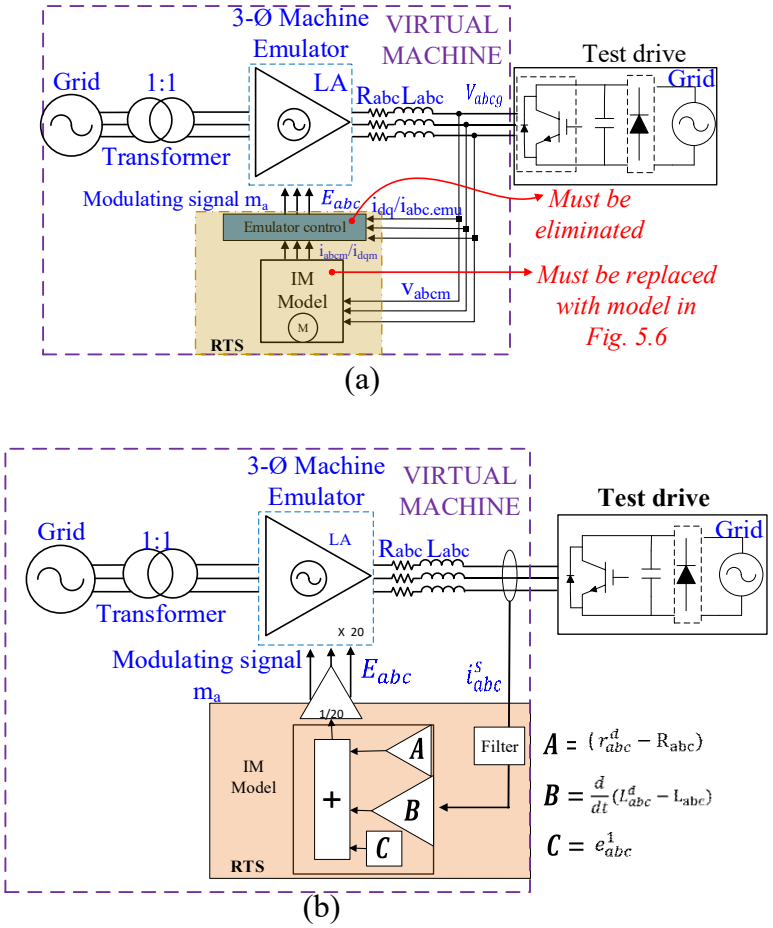


Fig. 5.8. (a) Conventional emulator configuration and (b) Proposed emulator configuration.

$$V_{abcg} = v^s_{abc} \tag{5.23}$$

$$E_{abc} = \left(r^d_{abc} - R_{abc}\right) i^s_{abc} + \left(L^d_{abc} - L_{abc}\right) p i^s_{abc} + e^1_{abc} \tag{5.24}$$

The network interface machine modelling structure is reformulated mathematically for current input (i^s_{abc}) and voltage output (E_{abc}). This mathematical reformulation would eliminate the need of a 'fault detection algorithm' while applying faults. Thus, a new emulator configuration is shown in Fig. 5.8 (b). The voltage out signal (E_{abc}) by the machine model is scaled down by the amplifier gain and is directly given to the control input of the amplifier. The emulator controller in the proposed configuration is eliminated. However, a first order filter with a bandwidth of 2.5 kHz is placed at the model input for closed loop stability. This is to avoid algebraic loop errors and the

convergence issues of the computational algorithms in Matlab/Simulink with the proposed closed loop control.

The proposed emulator configuration shown in Fig. 5.8 (b) is tested for different drive converter faults, starting and speed variations. The validation results and a brief overview of identifying fault signatures for the drive converter faults is also given in the result analysis section 5.4.

5.4 Result analysis

The proposed induction machine emulator is tested for different drive converter switch faults. The input source in the proposed emulator configuration dc-ac converter. The output of the diode bridge rectifier in the converter module is maintained at 150V with the help of a three-phase autotransformer. A variable frequency input is fed to the induction machine emulator for a desired speed. This is done by maintaining the v/f ratio constant considering saturation of the core. During the speed control mechanism, failure of one or more switches due to malfunctioning of the gate driver or wire disconnections is considered. Thus, the resulting fault transients in the machine are analyzed. For example, any irregularity in a phase current lead to a rise in current of the other phases by the law of symmetry. For an all-switch fault with sudden zero gating pulse, leads to a voltage at the three phase terminals of the converter.

The drive converter is tested for different switch fault transients and speed variations with the help of the emulator. The dynamic accuracy of the voltage, current and speed waveforms obtained from the emulator test bench is validated against a real 5 hp machine.

The faults that are considered for malfunctioning of gate driver are, fault-1: malfunctioning of top switch in the leg for phase A, fault-2: malfunctioning of top switch in the leg for phase B along with fault-1, fault-3: malfunctioning of both switches in the leg for phase A and fault-4: malfunctioning of all the switches in all legs.

Initially the simulation of emulation with the proposed emulator configuration is done to examine starting and steady state conditions in Fig. 5.9. The no load current has a high amount of variation from pure sinusoid. The starting current of higher magnitude has comparatively less variation. It can be seen that the reference voltage for the emulator is lacking in purity of a sharp-edge pulse because of the usage of a low pass filter in the feedback loop. The same can be observed in the experimental emulation results which shows a good match even at 2ms time axis for steady

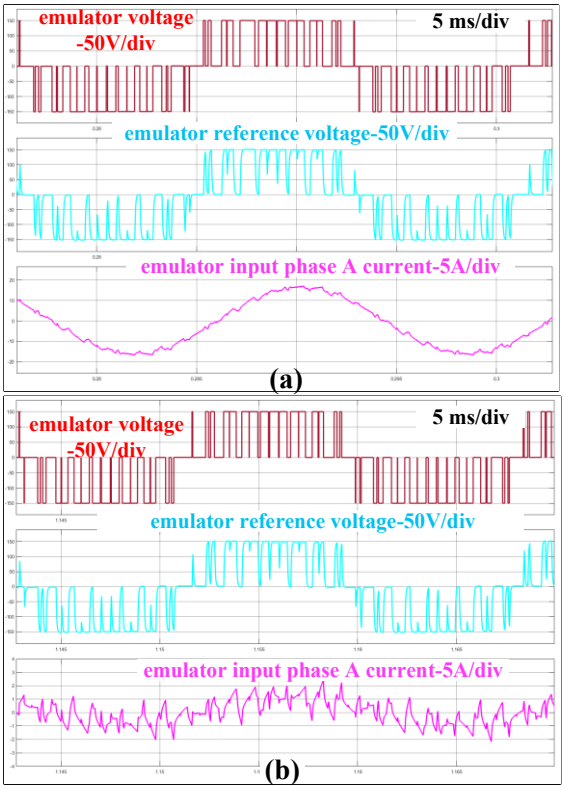


Fig. 5.9. Simulation of emulation result analysis for voltages and currents during (a) starting and (b) steady state.

state in Fig. 5.10. The emulated terminal voltage and the real machine stator terminal voltages of the induction machine for drive converter switch faults are presented in Fig. 5.11, 12, 13 and 14. For application of switch faults, the malfunctioning operation is artificially done with zero gating pulses. It is shown in Fig. 5.11, faults-1 and 2, are applied to the real machine which are indicated by T1 and T2 transitions. Fault recovery for both the faults is also done step by step, indicated by T3 and T4 transitions. The positive peak currents are clipped off for both the faults and the switched voltages appear to be distorted at the instant of fault indicated by arrow marks in Fig. 5.11. The same strategy of fault application and recovery is repeated for the emulator represented by T1', T2', T3' and T4' transitions. It is observed that the actual emulator voltage has a good match with the reference voltage as well as with the real machine.

Similarly, for application of fault-3, the respective phase current becomes zero, and the other phase currents are 180^0 out of phase with each other. This phenomenon is shown by simulation results in Fig. 5.12. In addition, the experimental result analysis in Fig. 5.13 shows transitions from fault-1 to fault-3, and fault recovery from fault-3 to fault-1 as well. The induction machine stator

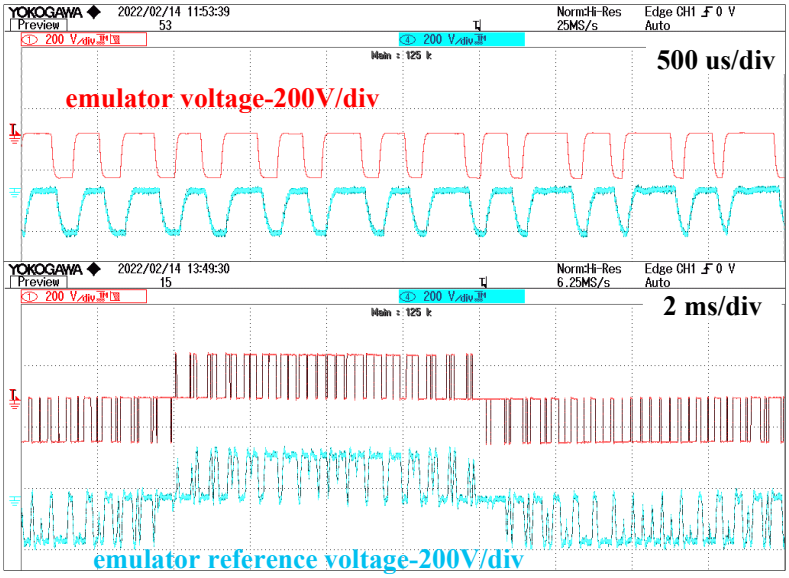


Fig. 5.10. Experimental emulation results for steady state voltages and currents.

voltage, emulator and the reference line voltages are in line with each other indicating tracking performance of the emulator. A complete gate driver fault i.e., fault-4 gives a decay in speed and back-emf of the machine. This is because all three phase currents go to zero instantly with zero gating signal as shown in Fig. 5.14. One of the important observations in Fig. 5.15 is that the switched input voltage at the instant of fault disappears abruptly and converts into a pure sine wave. The sine voltage is the induced voltage (back-emf) due to rotation of the rotor. The decay in this back-emf is due to the slowing down rotor. Fig. 5.15 (a) shows the experimental result for the emulator employing a linear model. Fig. 5.15 (b) shows the experimental result for a real machine. Fig. 5.15 (c) shows the experimental result for the emulator employing a non-linear model. It can be clearly seen that the voltage decay is faster for the emulator with a linear model when compared with the real machine. Hence, the emulator is employed with nonlinear model discussed in section 5.2.3. The voltage response with the upgraded emulator has improved accuracy for a complete gate driver fault. The results are magnified for a time period of 100 ms/div and are displayed in Fig. 5.15 (a), (b) and (c).

The overall response for starting, steady state and step change in speed is also presented in Fig. 5.16 for the real machine and the upgraded emulator. It is observed that the speed response and the emulated voltage trends have a good match with that of the real machine.

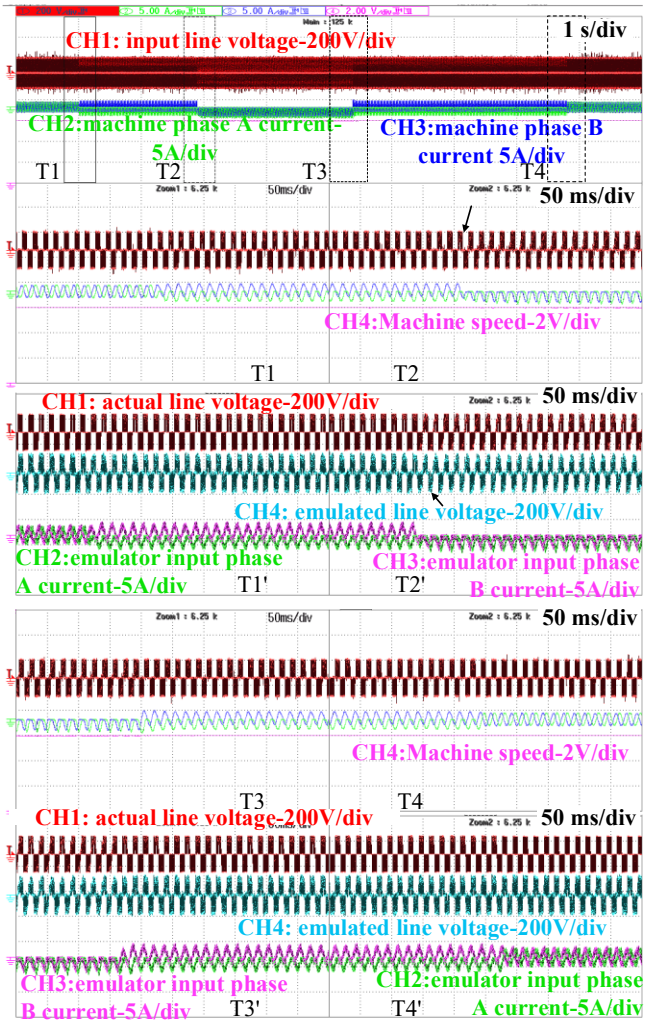


Fig. 5.11. Experimental results for fault-1 to fault-2 transitions and fault recovery transitions with real machine (T1, T2, T3 and T4 transitions) and with emulator (T1', T2', T3' and T4' transitions).

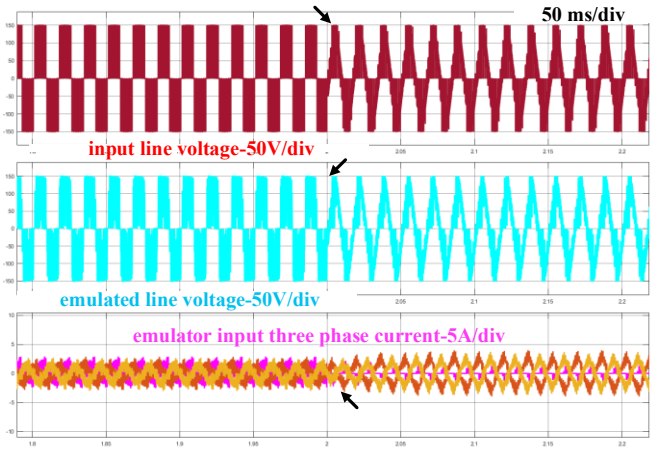


Fig. 5.12. Simulation of emulation result analysis for voltages and currents for fault-3.

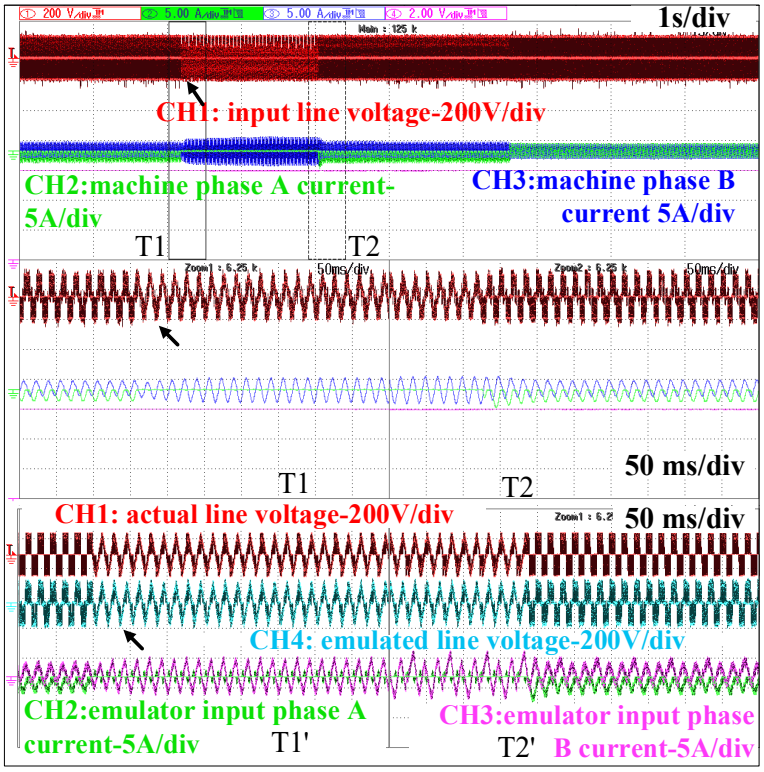


Fig. 5.13. Experimental results for fault-1 to fault-3 transition and vice versa for the real machine (T1, T2) and for the emulator (T1',T2').

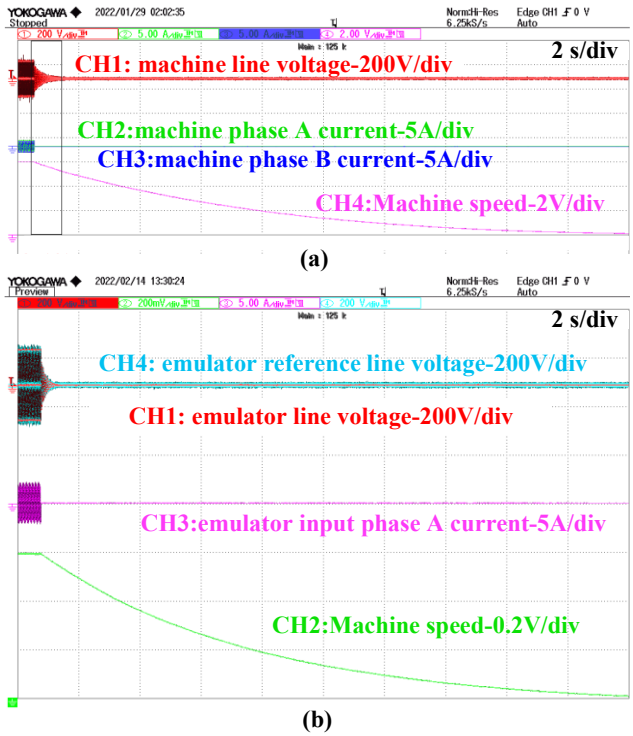


Fig. 5.14. Voltage, current and speed characteristics for complete gate driver fault (fault-4) for (a) real machine (b) emulator with linear model.

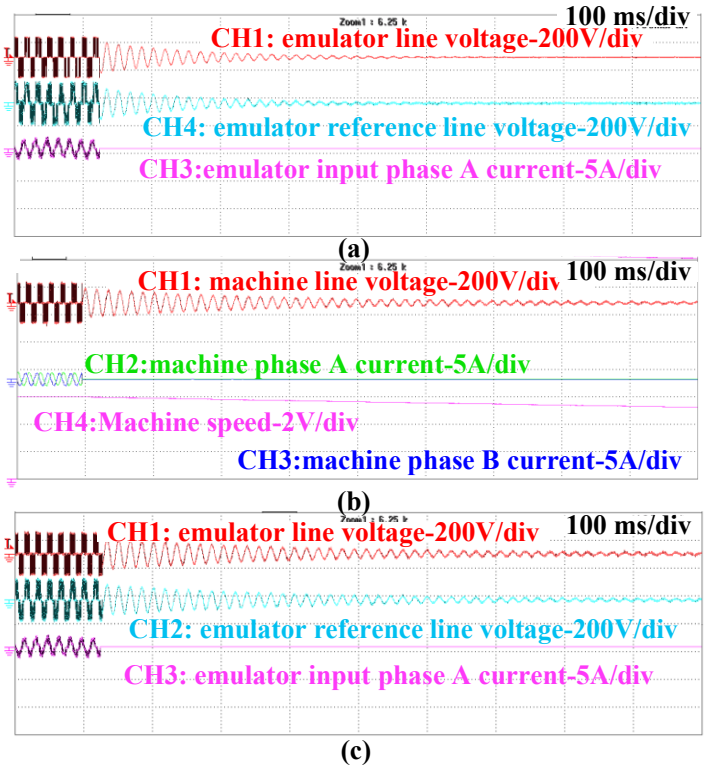


Fig. 5.15. Line voltage and current characteristics for a gate driver fault (magnified for 100 ms/div) (a) emulator with linear model (b) real machine (c) emulator with non-linear model.

5.4.1 Fault signatures

The purpose of developing an emulator test bed is not only for testing the drive converter but also serves in identifying the fault signatures for several test application of faults. These signatures would further help fault diagnosis, fault localization and fault isolation procedures. The fault signatures that are identified from the obtained results are $i_d - i_q$ current circles, negative sequence components, torque ripple. The asymmetry in the current due to faults result in ellipses in $i_d - i_q$ plots [55]. The same phenomenon is observed for the discussed converter faults as shown in Fig. 5.17 (a). The converter switch faults i.e., fault-1 and fault-3 results in asymmetrical and symmetrical ellipses about the origin as displayed in Fig. 5.17 (a). The clipping of the positive peak in stator current for single switch fault (fault 1) leads to an imperfect ellipse as shown.

However, it is discussed in [54], that asymmetry in stator currents lead to a rise in negative sequence components in current. The same signature for emulator voltage is observed for a single

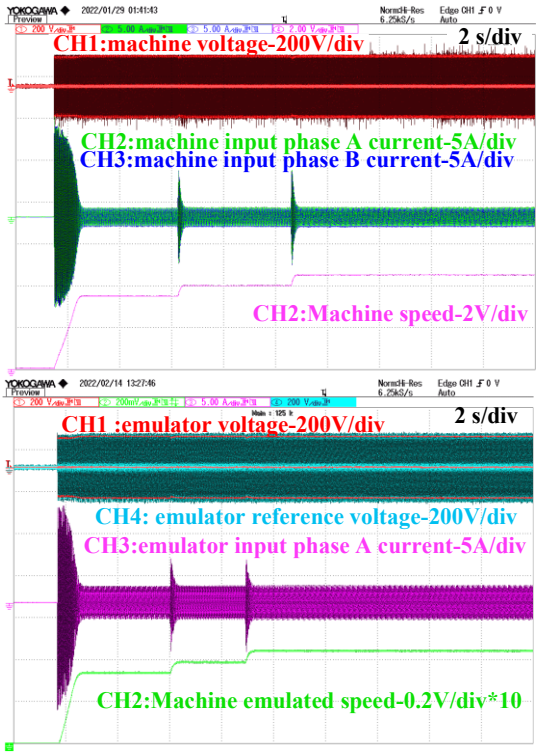


Fig. 5.16. Voltage, current and speed characteristics for starting and change in speed command for (a) real machine (b) proposed emulator.

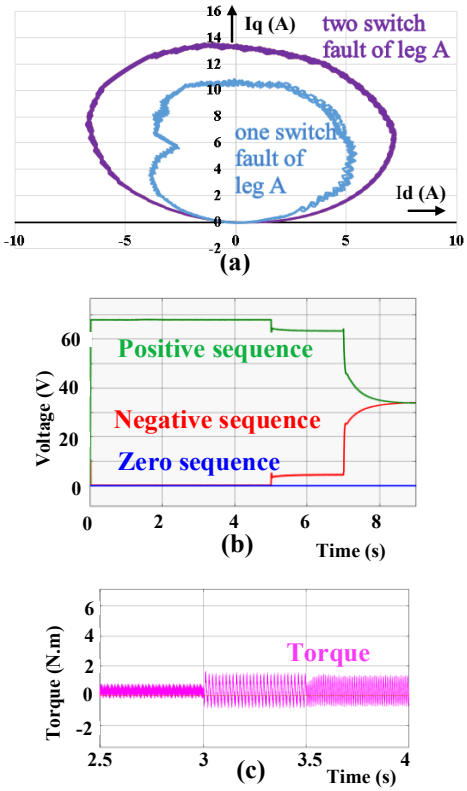


Fig. 5.17. (a) i_d, i_q plots for converter switch faults; (b) sequence components of emulator terminal voltage and (c) torque ripples for converter switch faults.

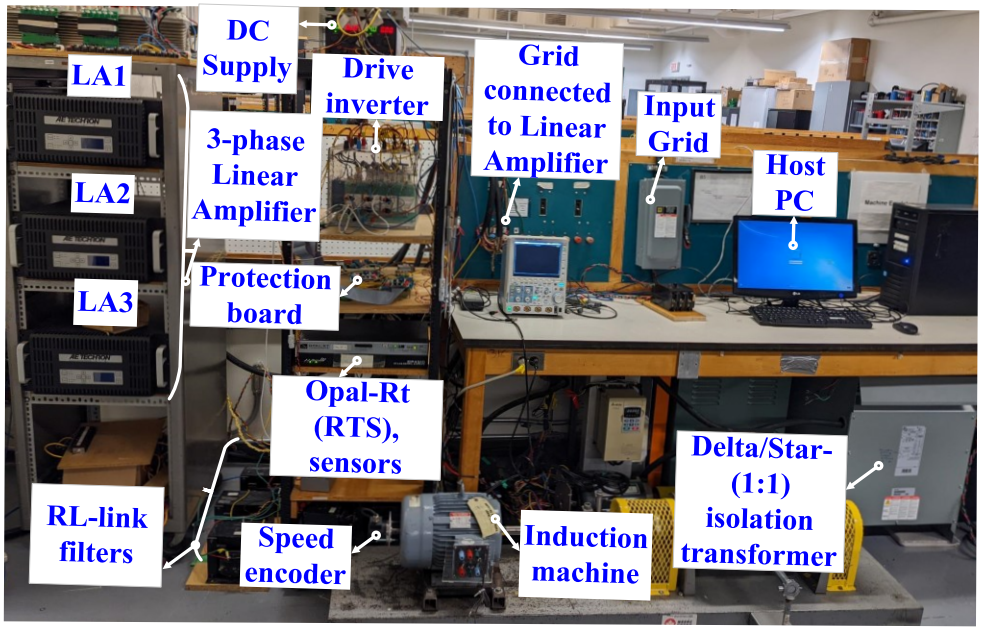


Fig. 5.18. The proposed emulator test bed for drive converter switch faults along with the 5 hp induction machine used for validation.

switch fault at 5 s and two switch faults at 7 s as shown in Fig. 5.17(b). The emulator torque acquires fundamental frequency oscillations during the single switch fault and second harmonic oscillations during two switch faults represented in Fig. 5.17 (c). During mal operation of the electric drive at any time, the identification of the fault signatures with the same trends (in Fig. 5.17) leads to easy, fast and less expensive fault diagnosis.

Fig. 5.18 shows the experimental setup for implementing drive converter open switch faults on emulator and on the real machine.

5.5 Summary

PHIL based emulation procedures are gaining more attention in recent times especially in the field of electric vehicles. The emulator test bed helps in testing various control algorithms of the electric drives before commissioning the real machine. The proposed emulator in this present research work helps to test the effects of a single switch fault and multiple switch faults due to mal operation of the gate driver. The multiple switch faults that belong to the same leg, different legs and to all the switches of all the legs are investigated with the help of the proposed emulator. Finally, the emulation results are validated with a laboratory sized 5 hp machine to prove the

performance of the emulator. In contrast to the difficulties associated with the VICO model for an open circuit fault, the suitability of CIVO model is detailed. The model is upgraded with saturation nonlinearities and proved its robustness for an all-switch fault. A new emulator configuration eliminating the need of an emulator controller is proposed. The emulation results while testing different drive converter faults also helps to record the fault signatures. These signatures can help in online fault diagnosis of electric vehicle. As a future scope, various fault tolerant and fault remedial strategies can also be investigated and explored with the developed emulator.

Chapter 6 Ideal Transformer Method Optimization for Power Hardware-in-the-Loop Simulations of Grid Connected Inverters

6.1 Introduction

Power hardware-in-the-loop (PHIL) simulations have been increasingly used for testing and for performing studies related to distributed energy resource (DER) integration into electric power systems [79], [80]. A block diagram of a typical PHIL testbed for DER testing is shown in Fig. 6.1. PHIL simulations require an interface algorithm (IA) to connect the power hardware being tested with the simulation running on a real-time simulator (RTS). The IA forms a critical part of the closed-loop PHIL system as shown in Fig. 6.1. The simulated system and the interface algorithm in Fig. 6.1, emulate a grid with a specific short-circuit ratio [22].

The stability and accuracy of the closed-loop PHIL depends on the transfer function of the power amplifier, the transport and feedback delays in the loop, the IA used, the impedance of the device-undertest (DUT) and the impedance of the source. Various types of IAs and stabilization methods have been reported in the literature [80], [81], [82]. The Ideal-Transformer-Method (ITM) is among the most commonly used IAs [80], [81]. This chapter focuses on the ITM IA due to its simplicity and ease of implementation. However, ITM IA applied alone imposes challenges with ensuring stability of the closed-loop PHIL system. The simplest and most economical method of stabilizing an ITM-based closed-loop PHIL interface is by adding a low-pass filter (LPF) represented by a transfer function H(s) (of higher order if needed) in the feedback path in Fig. 6.1 [23], [83]. However, adding such filters reduces the overall bandwidth of the system and compromises the accuracy of the PHIL simulation. Since for a given PHIL testbed, the power amplifier, and the associated delays, remain constant, the combination of the type of IA and the DUT are the key determinants of the stability of the PHIL closed loop. The authors in [84] introduced a complex compensator design for a grid connected system with an LC filter.

The present research work discusses that physical filter topology (L, LCL) plays an important role in selecting the order and type of an optimal compensator $H(s)$ to be included in the feedback

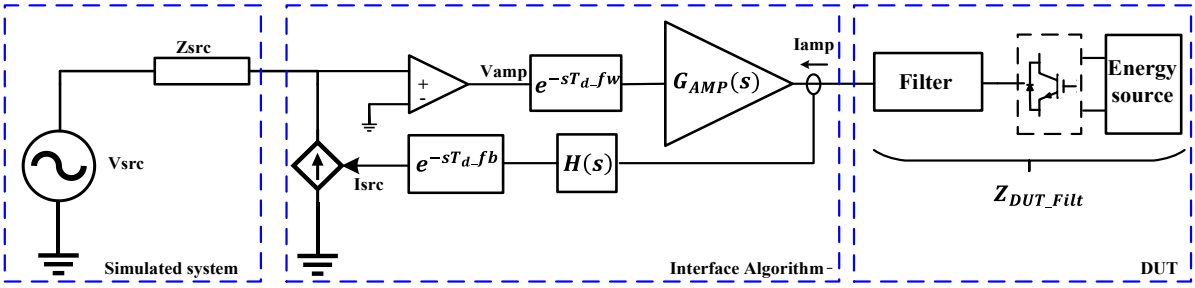


Fig. 6.1. Closed loop PHIL system.

path for stabilizing closed-loop PHIL system. While for the case of an L filter topology, a first order lowpass filter is a suitable solution, for the case of an LCL filter topology an alternative approach is recommended. In addition to analyzing stability, this chapter studies the effect of different filter structures (L, LCL) of power electronics interfaced DUTs on the dynamic accuracy of a PHIL simulation. The accuracy analysis in this work considers error functions in the frequency domain [85]. Limitations of the compensator design, effects of the power amplifier transfer function and transport delays are also presented. The effect of the variation in source-to-load impedance ratio [86] is also discussed with the help of experimental results. Finally, the chapter proposes an improved method for designing a compensator for these cases.

Experiments have been performed with the closed loop PHIL configuration as presented in Fig. 6.1. The simulated system and compensator $H(s)$ are implemented in an OP4510 real-time simulator (RTS). The three-phase four quadrant, soft switching power amplifiers in a commercial OP1420 test-bench are used to supply voltage to the DUT. The DUT is chosen to be a Lucas-Nuelle solar photovoltaic (PV) inverter coupled with a PV emulator supplying DC power. A three-phase filter is coupled to the PV inverter at the point of common coupling.

The rest of the chapter is organized as follows. A detailed mathematical stability analysis is made in Section 6.2 with the help of frequency response Bode plots while designing compensators for the corresponding physical filter topologies. The design and the overall closed-loop PHIL system is simulated, and the results of time-domain simulations are provided in Section 6.2 as well. The experimental result analysis is discussed in Section 6.3. Conclusions of the research work are presented in Section 6.4.

6.2 PHIL Closed-Loop Modeling and Compensator Design

The block diagram of the closed-loop PHIL system with ITM IA is shown in Fig. 6.1. Each component shown in the figure influences the closed-loop stability of the system, which can be analyzed with the help of the open-loop transfer function of the system $G_{OL}(s)$ given by (6.1). The objective of an IA is to ensure stability of the closed-loop system. The DUT in Fig. 6.1 consists of a PV inverter coupled with a filter structure.

$$G_{OL}(s) = \frac{Z_{src}}{Z_{DUT-Filt}} G_{AMP}(s).e^{s(T_{d-fw}+T_{d-fb})}H(s) \tag{6.1}$$

$$\text{Where } Z_{src}(s) = R_{src} + sL_{src} \tag{6.2}$$

where, $Zsrc$ is the source impedance, $Z_{DUT-Filt}$ is the DUT impedance, $G_{AMP}\ (s)$ is the amplifier transfer function, T_{d-fw} and T_{d-fb} are the forward and backward path delays and H(s) is the compensator transfer function.

Two cases are considered for DUT impedance, they are: 1) DUT with an L filter, and 2) DUT with an LCL filter. Note that even if the DUT consists of a filter of LC topology, the equivalent filter interfacing the inverter is of LCL topology because of the inductance within a power amplifier. Therefore, the DUT impedance for the case of L filter is given by $Z_{DUT_{L-Filt}}$ in (6.3), while for the case of LCL filter, it is given by $Z_{DUT_{LCL-Filt}}$ in (6.4).

$$Z_{DUT_{L-Filt}}(s) = R_{1f} + R_{2f} + s\left(L_{1f} + L_{2f}\right) \tag{6.3}$$

$$Z_{DUT_{LCL-Filt}}(s) = sL_{1f} + \frac{R_{1f}}{s^2 L_{1f} C_f + R_{1f} C_f s + 1} + \left(sL_{2f} + R_{2f}\right) \tag{6.4}$$

where L_{1f} , R_{1f} , C_f are the inverter side filter parameters and L_{2f} , R_{2f} are the amplifier side filters. From (6.1), it is seen that the filter topology affects the impedance of the DUT $\left(Z_{DUT-Filt}(s)\right)$ and consequently affects the stability of the entire closed-loop system. The following section 6.2.1 provides an analysis of the closed-loop system for the cases of L filters and LCL filters.

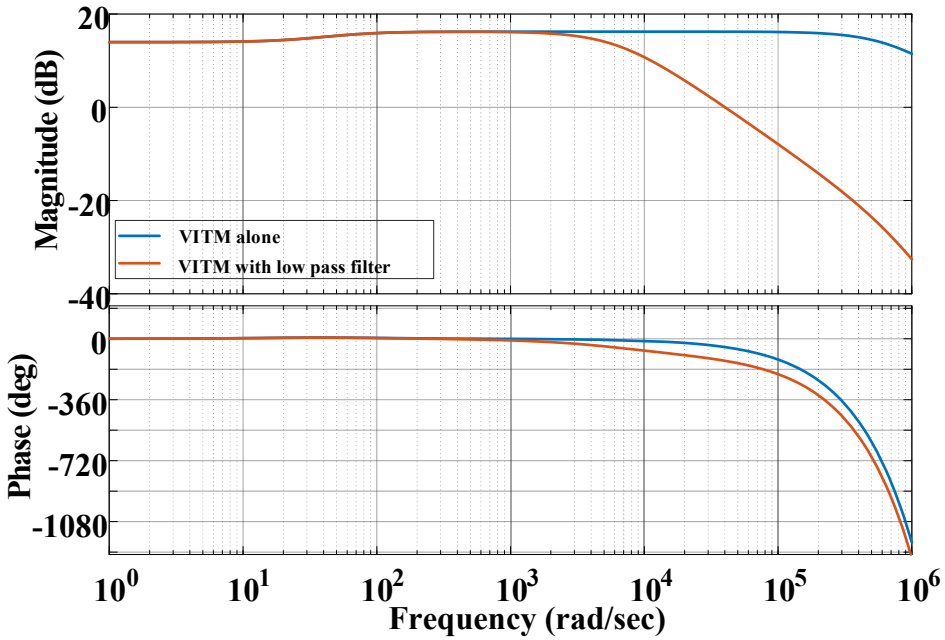


Fig. 6.2. Magnitude and phase plots for a low pass filter-based compensator being used for DUT with L-filter.

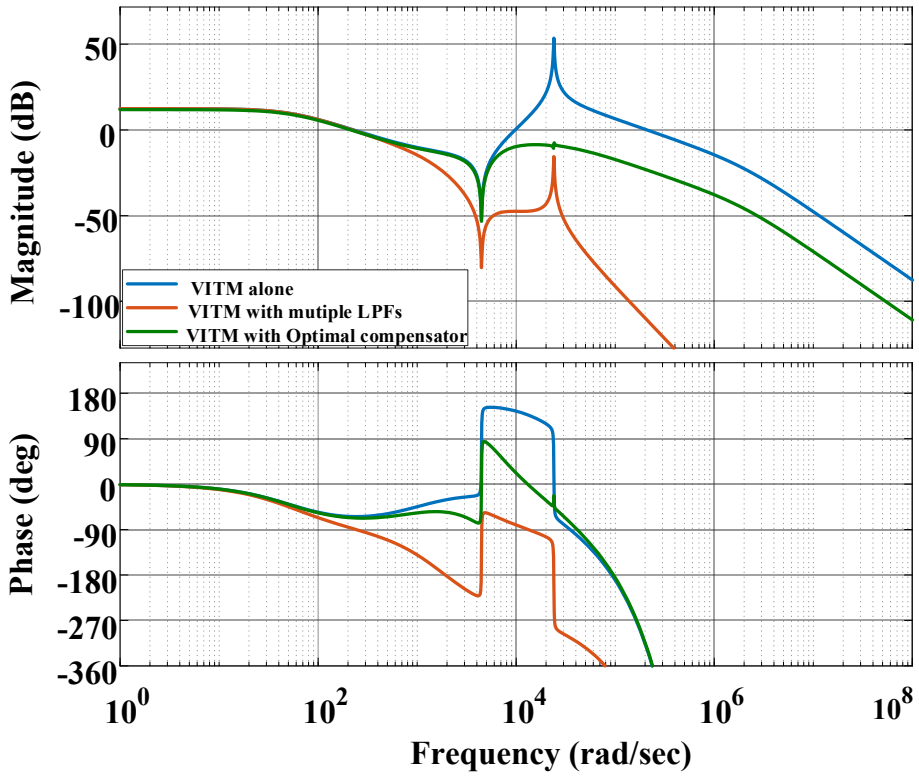


Fig. 6.3. Magnitude and phase plots for comparison of multiple LPFs and optimal compensator for DUT with LCL filter.

6.2.1 L-filter and LCL-filter

First, a DUT with a simple L-filter is considered for closed-loop stability analysis of the ITM-IA. Equation (6.1) defines the open-loop transfer function of the PHIL system. The source/grid impedance $Z_{src}(s)$ and the DUT filter impedance $Z_{DUT_{L-Filt}}(s)$are presented in (6.2) and (6.3), respectively. Bode plot analysis is done for G_{OL} as illustrated by Fig. 6.2. Closed-loop instability with a gain over 0 dB at the -180° phase point is observed in Fig. 6.2 (in blue).

Second, an LCL-filter in the DUT is considered. The change in $Z_{DUT_{LCL-Filt}}(s)$ of Eq. (6.4) is reflected in the shape of the Bode plot and affects closed loop stability. Fig. 6.3 (in blue) indicates that the closed-loop PHIL system is unstable with negative gain margin.

Therefore, there is a necessity to design a compensator in both the cases to ensure stability of the closed-loop PHIL system. The system parameters considered are described as follows: the value of L_{2f} is chosen to have the same value as the optional internal interface inductance provided by the amplifier, that is 75 μH. The simulated voltage source has a short-circuit ratio (SCR) of 10 and an $\frac{X}{R}$ ratio of 10.6. The value of L_{1f} is 0.1 pu with a quality factor of 16 (4.21 mH). The value of C_f is chosen to have a cutoff frequency of 700 Hz (24 μF). The forward and backward path time delays are 10 μs each.

6.2.2 Compensator Design

In designing a compensator, the simplest choice is a low-pass filter. A low-pass filter provides attenuation in the magnitude response thereby ensuring positive gain margin and hence closed loop stability. The cut-off frequency of the low-pass filter however has implications on the stability and the accuracy of the PHIL simulation.

In the case of a DUT with an L-filter, it is relatively easy to design a low-pass filter. As can be seen in Fig. 6.2 in orange, a low pass filter at a relatively high cut-off frequency (1 kHz) with respect to the frequency of interest (50 − 60 Hz fundamental) ensures stability, whilst maintaining PHIL accuracy. This is due to the fact that the error associated with the addition of a low-pass filter will be low as well.

However, in an LCL filter based DUT, this is not the case. The PHIL open-loop transfer functions of such LCL filter based DUTs result in resonant peaks in the magnitude response, which possess

negative margins as shown in Fig. 6.3 (in blue). Therefore, multiple LPFs at a relatively low cut-off frequency (compared to the L-filter based DUT) in (6.5), are needed to stabilize the PHIL closed loop system as shown in Fig. 6.3 (in orange). This would result in an inaccuracy of the PHIL system because of its lower cutoff frequency, as will be discussed in the next section.

$$H(s) = \left(\frac{1571}{s + 1571}\right)^3 \tag{6.5}$$

Therefore, in order to retain the accuracy of the system and to suppress the resonant peaks, this chapter proposes an optimal compensator for DUTs with LCL filters to have improved accuracy.

A. Optimal compensator

The objective is to design an optimal compensator which cancels the resonant pole of the system. The open loop transfer function (OLTF) derived from (6.1) is given by (6.6), with an assumption of H(s) = 1. It is a fifth order transfer function, which has two complex conjugate poles $1.0 \times 104 \cdot (-0.0132 \pm 2.3913i)$ leading to a resonant peak in Fig. 6.4 (in blue). Hence a compensator $H(s)$ is added in such a way to cancel these resonant poles, as shown in (6.7). The compensator incorporates two complex zeros at the same locations as the resonant poles in (6.6) and also a complex pole at $1.0 \times 103 \cdot (-4.4435 + 4.6963i)$. The complex pole in (6.7) provides sufficient attenuation $(-40\ dB/dec)$ to higher frequencies after the resonant peak cancellation, which can be observed in Fig. 6.4 (in green). The orange trace in Fig. 6.4 shows the frequency response of the compensator alone and shows a resonant valley which is designed to cancel the resonant peak of the uncompensated OLTF. The green trace is the resulting frequency response with compensation. The resonant peak being suppressed implies the possibility of having an LPF with a higher cut-off frequency and hence higher PHIL accuracy.

$$G_{OL}(s) = \frac{(6.048.10^{-13}.s^3 + 6.336.10^{-10}.s^2 + 1.203.10^{-5}.s + 0.012).e^{-s.2.10^{-5}}}{(1.444.10^{-24}.s^5 + 2.935.10^{-18}.s^4 + 9.252.10^{-18}.s^3 + 1.717.10^{-9}.s^2 + 5.232.10^{-5}.s + 0.002881)} \tag{6.6}$$

$$H(s) = \frac{(0.06855s^2 + 18.1s + 3.926.10^7)}{(s^2 + 8887s + 4.182.10^7)} \tag{6.7}$$

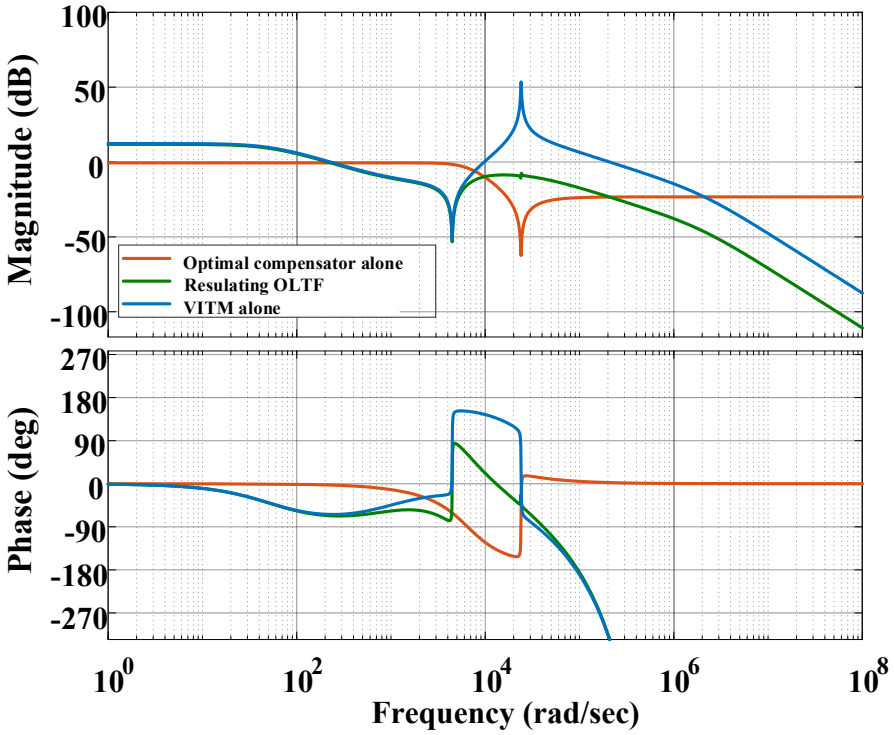


Fig. 6.4. Magnitude and phase plots for optimum compensator for DUT with LCL filter.

B. Damping resistor

A damping resistor in series with the capacitor C_f of the LCL filter can be placed [87], [88]. This essentially damps the resonant peak of the system as shown in Fig. 6.5. To have a positive gain margin the optimal compensator in (6.7) is used additionally. This method will have further attenuation to specific resonant frequencies only, as shown in Fig. 6.5. This analysis is validated in section 6.2.3.A with relevant time-domain simulations for transient scenarios. The value of the damping resistance R_d is chosen to be one-third of the capacitive reactance at the resonant frequency ω_{res} of Eq. (6.8). The details of choosing the minimum value of R_d are detailed in [12] to minimize resistive power losses. The equation of power loss is shown in Eq. (6.9), for a voltage V_{RC} across the RC branch and for a fundamental frequency ω_f .

$$Rd = \frac{1}{\left(3\,\omega_{res}\,C_f\right)} \tag{6.8}$$

$$P_{R_{dLoss}} = (R_d.\omega f.Cf.V_{RC})^2 \tag{6.9}$$

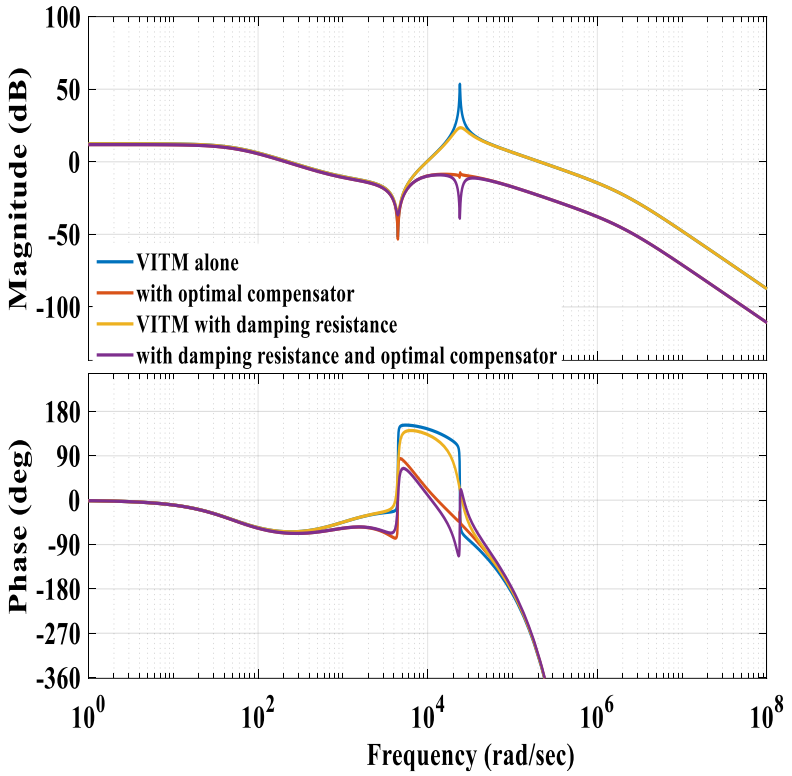


Fig. 6.5. Comparisons of with and without damping resistor for DUT with LCL filter with optimal compensator.

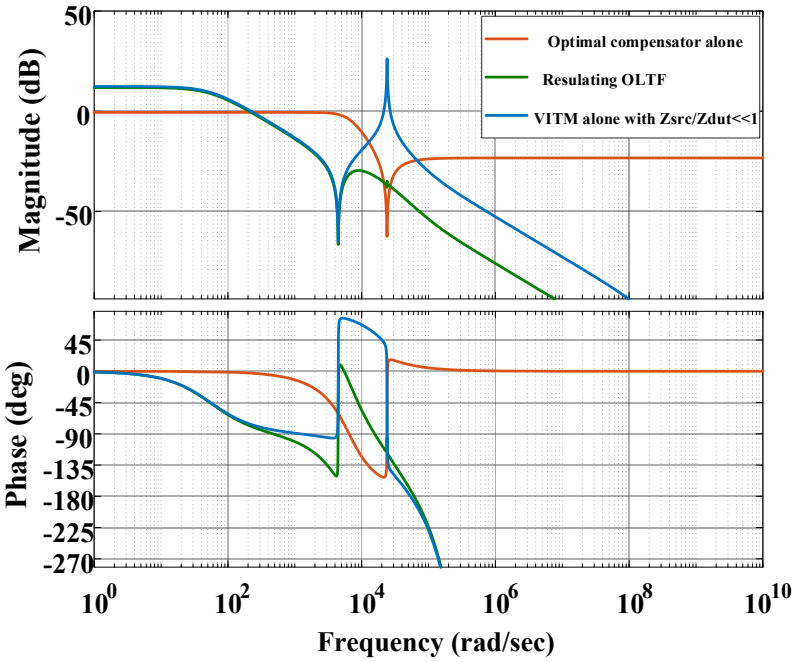


Fig. 6.6. Magnitude and phase plots for optimum compensator for DUT with LCL filter for very low source to DUT impedance ratio.

C. Variation of impedance ratio

The objective is to make the $\left(\frac{Z_{src}}{Z_{DUT-Filt}}\right)$ ratio far less than the critical value of 1 [86]. This is illustrated in Fig. 6.6, where the resonant peak magnitude is suppressed to 21.2 dB from 53.5 dB as shown in Fig. 6.4 (in blue). It can be seen in Fig. 6.6, that the instability of the closed loop system still exists. Hence, the inclusion of the proposed optimal compensator H(s) attenuates the new resonant peak and makes the system stable. It can also be observed that the attenuation rate of higher frequencies is increased with the new $\left(\frac{Z_{src}}{Z_{DUT-Filt}}\right)$ ratio in comparison to Fig. 6.4. This results in the system being both more accurate and more stable. It is noted that using these compensation methods, the stability of the closed loop is enhanced. However, adding these components in the loop has an impact on the accuracy of the PHIL simulation. Thus, the accuracy must be explicitly evaluated for the proposed compensators to complement the Bode plot stability made in this section.

6.2.3 Accuracy Evaluation

Two aspects are of importance when selecting and designing interface algorithms for a PHIL system. First, stability of the closed-loop PHIL system must be ensured. Second, a sufficient degree of accuracy with respect to the reference system is required to provide valid results for PHIL testing. The reference system is a direct connection between the grid and the DUT which does not employ any interface algorithm. In this section, accuracy metrics in the frequency domain are introduced to assess the level of accuracy obtained with different interface algorithms. The method for evaluating accuracy proposed in [85] is applied. The method is based on the non-ideal interface Transfer Function Perturbation (TFP) approach. TFP refers to all effects that characterize a non-ideal interface, such as time-delays and amplifier dynamics. The authors derive an error function in the frequency domain as defined in (6.10).

$$E_{TFP} = \frac{\left(G_{sys-OL} . \Delta Gint\right)}{1 - G_{sys_{OL}} . (1 + \Delta Gint)} \tag{6.10}$$

where G_{sys-OL} is system open-loop transfer function defined in (6.11).

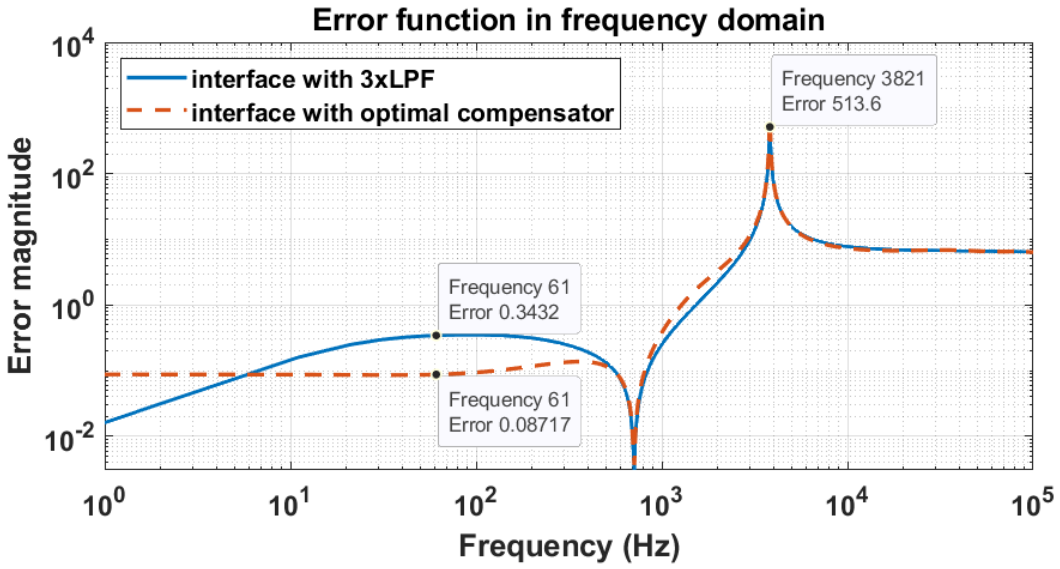


Fig. 6.7. Error function based on transfer function perturbation.

$$G_{sys-OL} = \left(\frac{Z_{src}}{Z_{DUT-Filt}}\right) \tag{6.11}$$

and ΔG_{int} is the interface TFP defined by (6.12) and (6.13)

$$\Delta G_{int} = G_{int} - 1 \tag{6.12}$$

$$G_{int} = G_{AMP}(s)e^{-s(Td-fw+Td-fb)}H(s) \tag{6.13}$$

The previous section introduced methods to stabilize the PHIL system that is not stable if the ideal transformer method alone is adopted. First, a solution based on multiple LPFs in the feedback path is applied. Second, an optimal compensator is derived and applied in the feedback path of the interface. The magnitude of the error function for both cases is illustrated in Fig. 6.7. While the error is reduced at the fundamental frequency of 60 Hz with the interface based on optimal compensator, there is a resonant peak at frequency of 3820 Hz for both cases.

A. Time-Domain Simulations

Two cases are considered: 1) DUT with LCL filter; and 2) DUT with L filter. A simulation for the ITM V-type interface algorithm is considered with parameters as given in Section 6.2. The

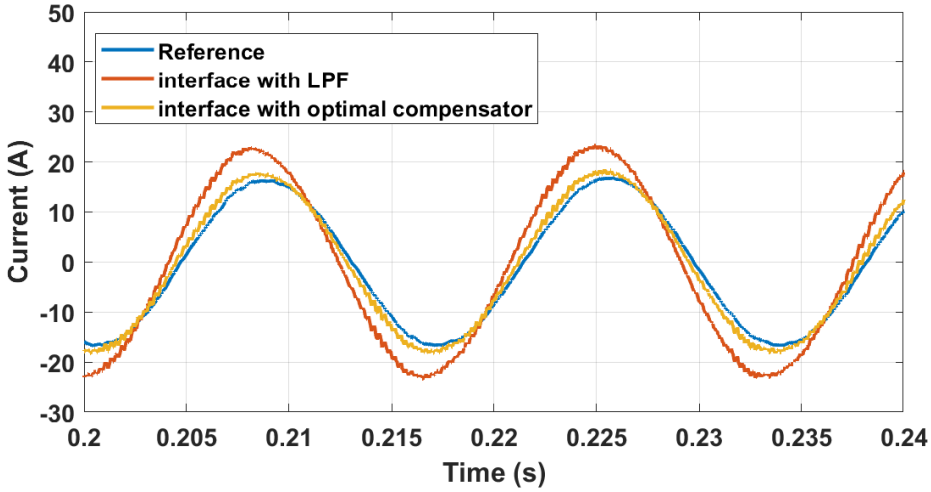
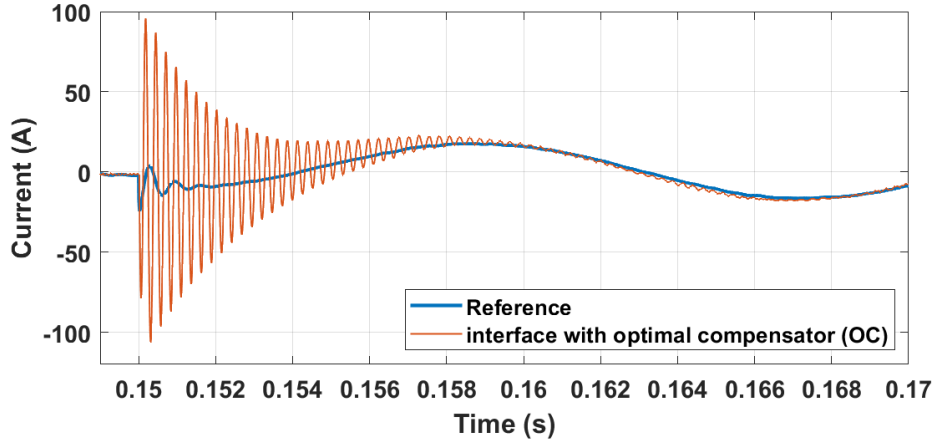
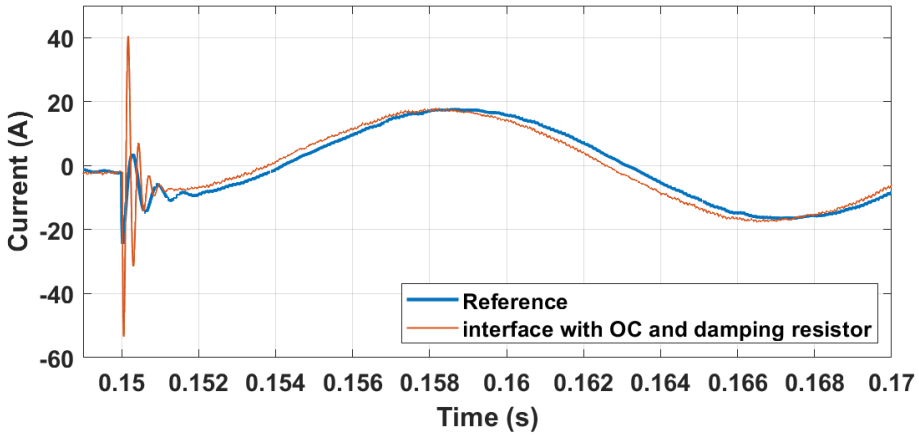


Fig. 6.8. Accuracy evaluation for multiple LPF and optimal compensator during steady state.



(a)



(b)

Fig. 6.9. Accuracy evaluation for (a) optimal compensator and (b) optimal compensator with damping resistance respectively during transient state.

simulation time step is chosen to be 10 μs and the hardware side is simulated at a time step of 1 µs. The simulated inverter system is rated at 10 kVA, with a switching frequency of 10 kHz. The test case simulated is one where the PV inverter injects 0A in steady state and a load is switched on at 0.15 s. Time-domain simulations are conducted for the reference model, PHIL setup with multiple LPFs and with the optimal compensator in the feedback path to compare waveforms. While the interface based on multiple LPFs ensures stability of the PHIL system, accuracy is compromised as indicated by the time-domain simulations shown in Fig. 6.8. It is also seen that the interface based on the optimal compensator improves the accuracy at the fundamental frequency i.e., during steady state. However, a significant error is observed following the step change of the load, as shown in Fig. 6.9. The transient oscillatory response at 3800 Hz possesses high error with respect to the reference. This reflects the resonant peak in the error magnitude in Fig. 6.7.

High frequency oscillations during loading transients with the optimal compensator can be diminished by introducing a damping resistor in series with the capacitor of the LCL filter. This would significantly damp the high frequency transient and improve the dynamic accuracy. This is proved with the simulation result shown in Fig. 6.9. The disadvantage with introducing a damping resistance is the associated power loss and is observed to be 2.6 W/ph for 400V line voltage.

Simulation results are presented for a DUT with an L-filter in Fig. 6.10. It can be seen that an LPF with a high cut-off frequency is sufficient to stabilize the PHIL simulation.

6.3 Experimental Results

An experimental test setup is developed with a 10 kVA, OP1420-OPAL-RT three-phase Microgrid Test-Bench. The amplifiers in OP1420 feed a Lucas-Nuelle Solar PV inverter via a 208/400V transformer. The PV emulator is set for providing maximum values of 1000V, 1500W. Fig. 6.11 portrays the experimental test setup. The soft-switching power amplifiers in the commercial OP1420 test-bench have a 10 kHz open-loop bandwidth and a signal transfer delay of 10 μs. The simulated system in an OP4510 real-time simulator (RTS) commands the power amplifiers. The communication between the RTS and the power amplifier is established with a high-speed fiberoptic SFP link. The three-phase DUT filter and Y/Y transformer are coupled to the point of common coupling. The experiment for validation of the ideal transformer method has been done in different stages.

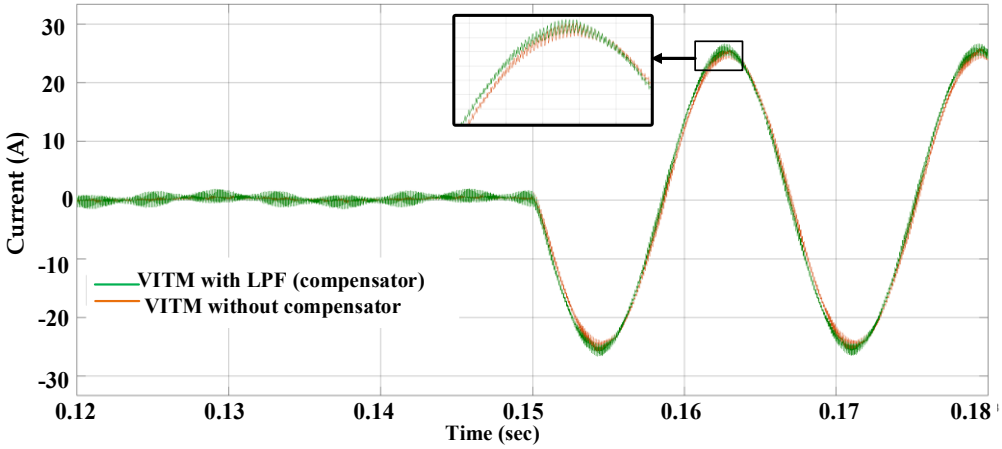


Fig. 6.10. Simulation results showing DUT current with L filter.

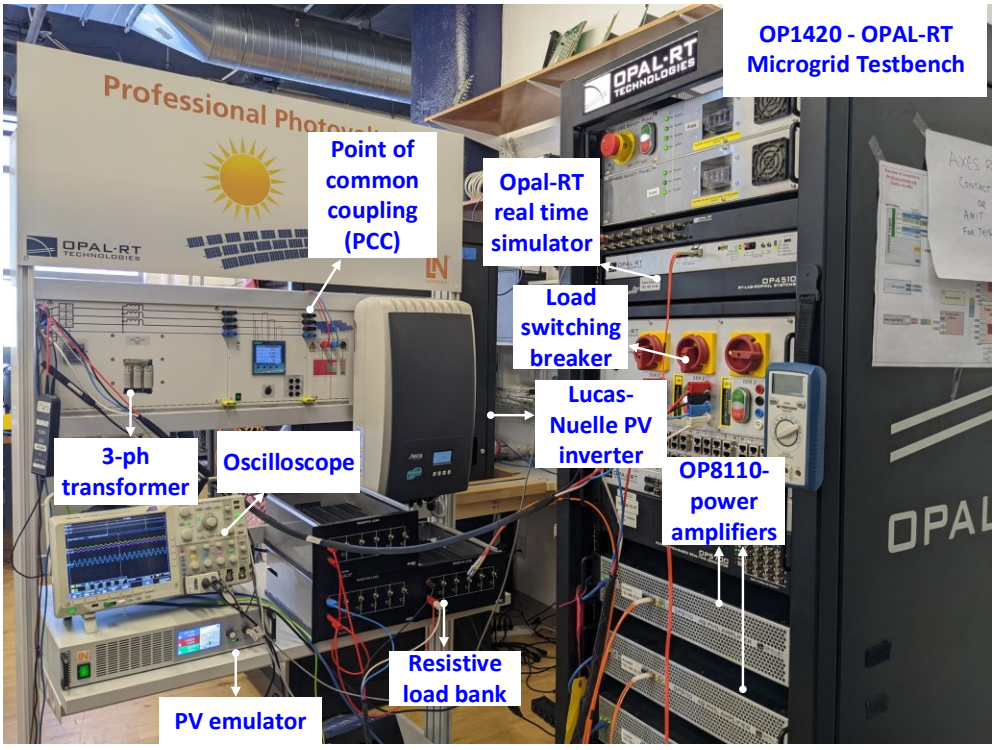


Fig. 6.11. Experimental set setup with OPAL-RT real time simulator with Lucas-Nuelle Solar PV inverter and emulator.

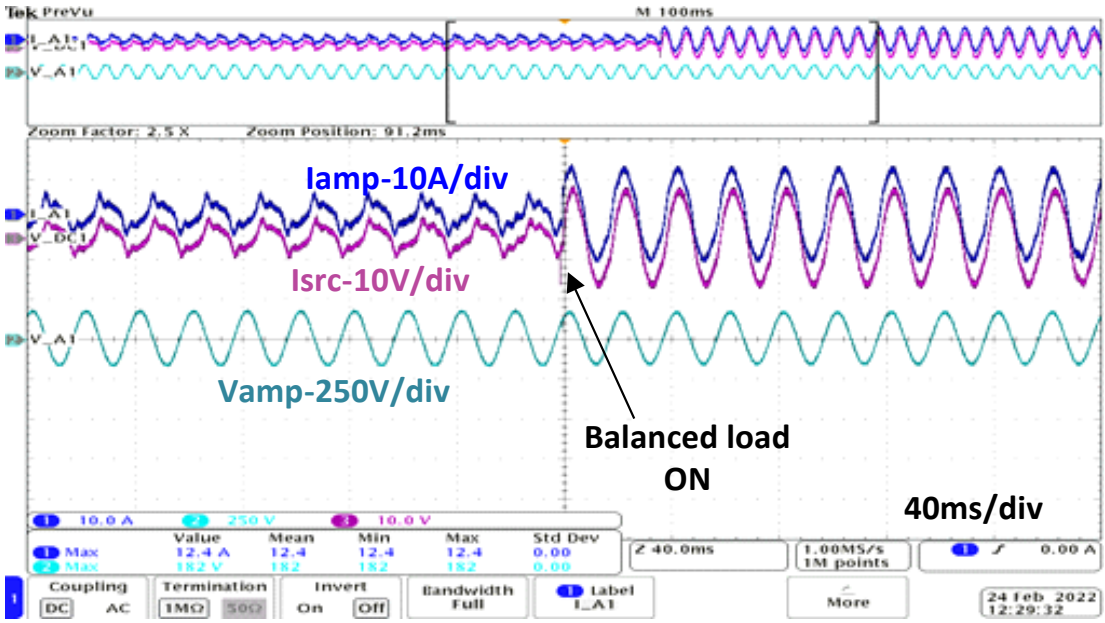


Fig. 6.12. Accuracy of the ITM for a balanced load under 208V operation with transformer for impedance ratio ≪ 1.

Initially, the experiment has been realized at low power of 700W for the PV emulator with $\frac{Z_{src}}{Z_{DUT-Filt}}$ ratio ≪ 1. A single three phase power amplifier running in independent mode is used to supply 208V line voltage(V_{amp}). The voltage is stepped up to 400V by the Y/Y transformer. The PV inverter gets connected to the point of common coupling (PCC) with a gradual rise in voltage. It is initially in grid-islanding mode, and it then transitions to a grid-connected mode at the instant of synchronization in terms of the magnitude and phase angle of the voltage at the PCC. In the grid-connected mode, the PV inverter draws some reactive power and supplies real power to the power amplifier. The current supplied by the PV inverter to the power amplifier (I_{amp}) is peaky with some harmonics representing the significant contribution of magnetizing current of the transformer, as seen in Fig. 6.12.

The closed loop is enabled by feeding back the sensed physical current to the real time simulation circuit employing the optimal compensator. Then, a balanced physical resistive load of 12.6 Ω is applied. This can be observed by the rise of input current (in amperes) to the PV inverter, as shown in Fig. 6.12. The source current that is simulated in real time also has the same transient and steady-state characteristics. This proves that the ITM with the proposed compensator possesses good

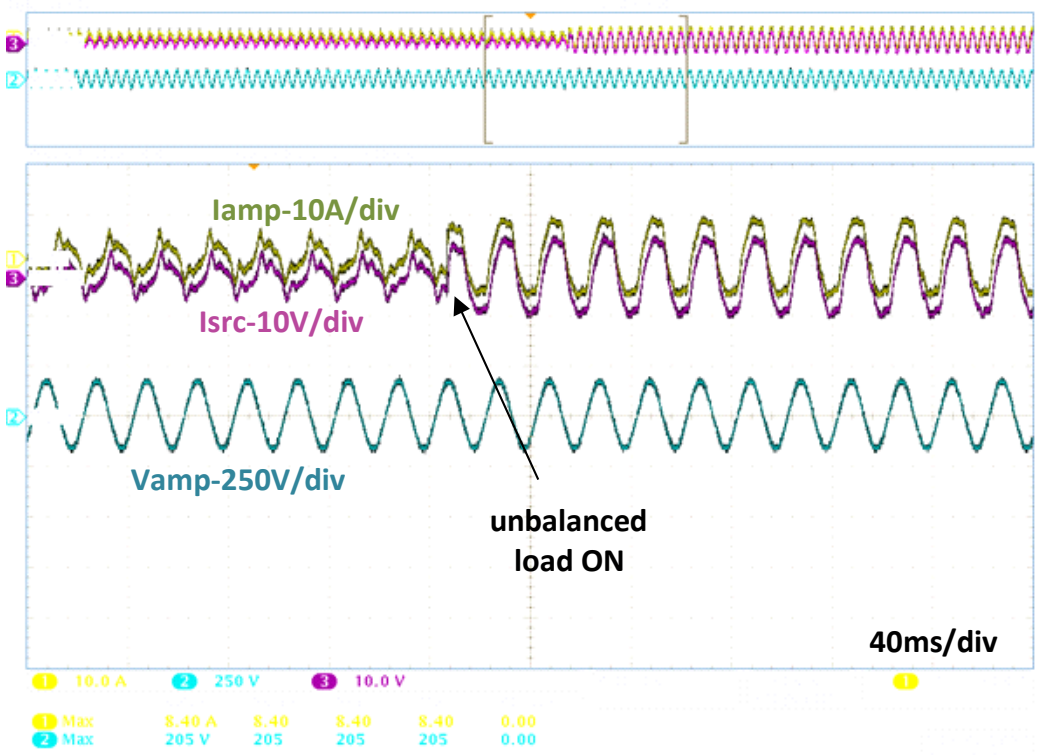


Fig. 6.13. Accuracy of the ITM for an unbalanced load under 208V operation with transformer for impedance ratio $\ll 1$.

stability and accuracy. The accuracy of the ITM is also verified for an unbalanced load as shown in Fig. 6.13. The robustness of the closed loop stability of ITM interface algorithm is achieved by maintaining a very low $\frac{Z_{src}}{Z_{DUT-Filt}}$ ratio of 0.25.

In the secondary stage, the source impedance is increased making $\frac{Z_{src}}{Z_{DUT-Filt}}$ ratio equal to 0.6. To avoid the distortion in the current due to magnetization, the transformer is omitted. The rated voltage of 400V is supplied by the OP1420 Microgrid Test-Bench. This is done by running the power amplifiers in differential mode. This strategy improves the amplifier current waveform, making it a cleaner sinusoid. A balanced load of 15 Ω and then 30 Ω is applied to verify the stability of ITM. The transient spike and oscillations in current at the loading instants show the system drifting from stability, as seen in Fig. 6.14.

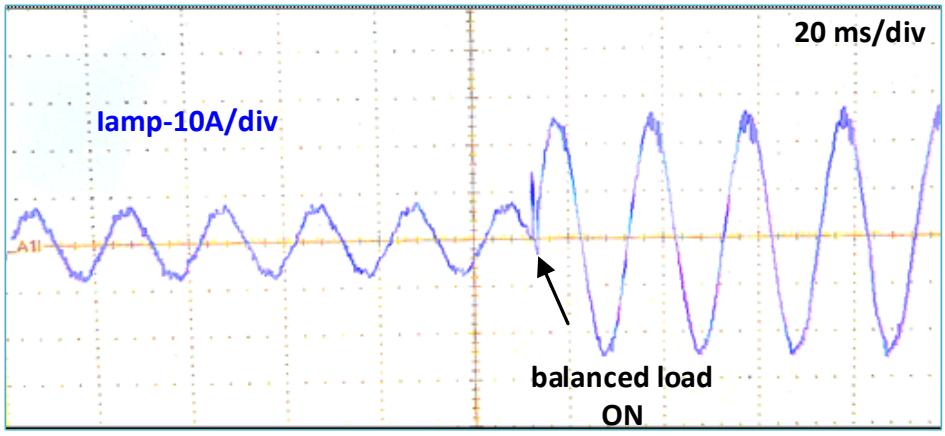


Fig. 6.14. Amplifier current with the optimal compensator based ITM for a balanced load under 400V operation eliminating the transformer for impedance ratio of 0.6.

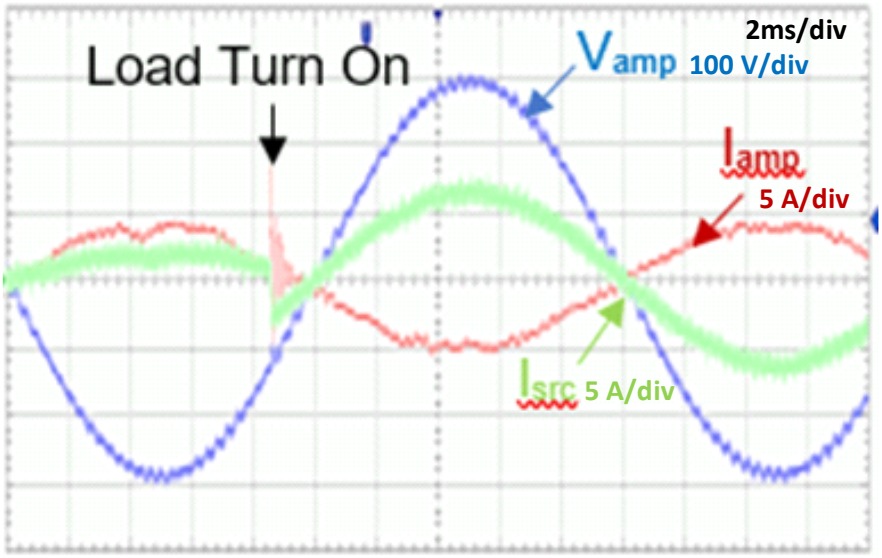


Fig. 6.15. Accuracy of the for 500 Hz multiple LPF based ITM for a balanced load under 400V operation eliminating the transformer for impedance ratio of 0.93.

In the tertiary stage, the source impedance is further increased to make the $\frac{Z_{src}}{Z_{DUT-Filt}}$ ratio equal to 0.93 which is close to the critical value (one). High power (1000W) is realized from the PV emulator. The currents for the cases of using a 500 Hz and a 1.5 kHz feedback filter are shown in Fig. 6.15 and Fig. 6.16, respectively. As the LPF cut-off frequency increases, the oscillations at the instant of a transient event increases as well, indicating a system on the verge of instability.

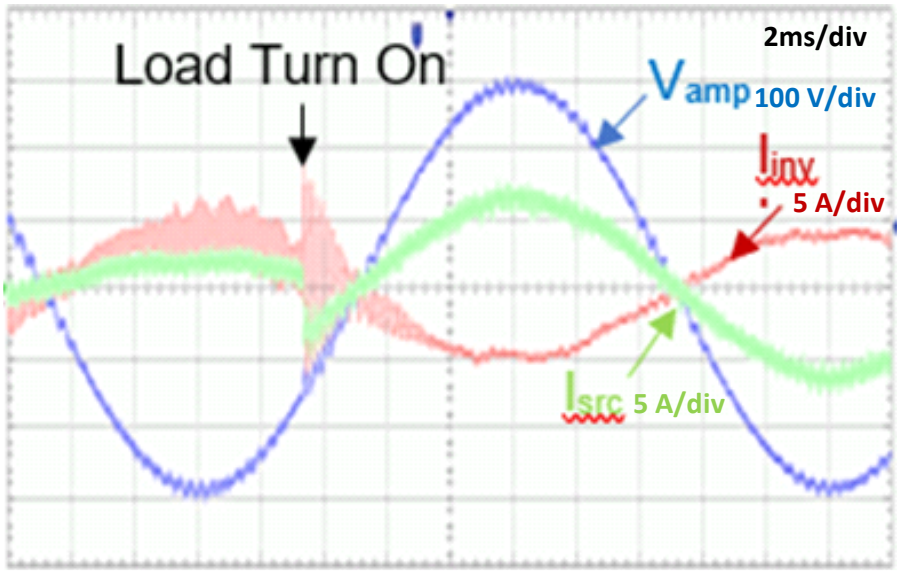


Fig. 6.16. Accuracy of the for 1500 Hz multiple LPF based ITM for a balanced load under 400V operation eliminating the transformer for impedance ratio of 0.93.

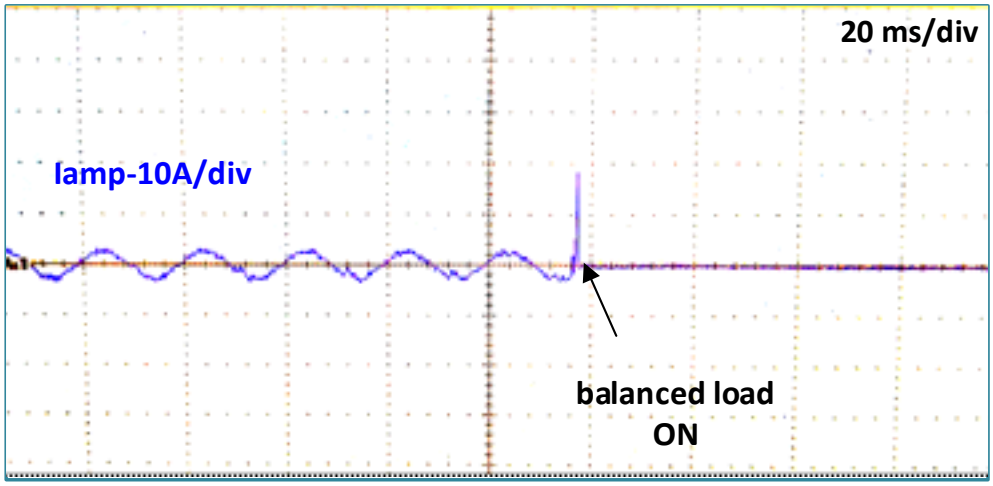


Fig. 6.17. Instability with optimal compensator based ITM for a balanced load under 400V operation eliminating the transformer for impedance ratio ≫ 1.

Thus, it can be inferred that the oscillations during the loading transients can be damped by taking a $\frac{Z_{src}}{Z_{DUT-Filt}}$ ratio far less than the critical value. However, as discussed in section 6.2.2.B, an alternative is the usage of a damping resistance to damp the oscillations but doing so increases resistive power losses, which is not desirable.

Finally, the value of Z_{src} is further increased to make the $\frac{Z_{src}}{Z_{DUT-Filt}}$ ratio much greater than 1. When the loop is closed, the system undergoes instability with large currents as shown in Fig. 6.17. However, the rise in magnitude of unstable current is limited by maximum current setting of the PV emulator.

6.4 Summary

The chapter presents a compensator design method to stabilize an ideal-transformer-method interface algorithm for PHIL testing while ensuring high degree of accuracy. Analysis of the DUT transfer function based on different filter topologies are presented. Stability analysis are detailed for proposed compensators using Bode plots. The impact of the optimal compensator on PHIL accuracy is analyzed and quantified with the help of error functions and error plots. The ITM interface with the optimal compensator is validated by simulations and hardware experiments. The chapter proposes that the dynamic accuracy can be further improved by introducing a damping resistor in the LCL filter structure and is validated with time domain simulations. Resistive damping essentially damps high-frequency oscillations during sudden transients but causes power losses. The minimal power loss introduced by the damping resistance is noted and can be disregarded if accuracy is the main concern. Different source-to-load impedance ratios are considered for the ITM with optimal compensator to experimentally analyze the stability and current characteristics during load transients.

Chapter 7 Conclusions and Future Research

The focus of this PhD research work is the emulation of Induction machines. The main conclusions of this thesis corresponding to each chapter and the future works are presented below.

7.1 Conclusions

7.1.1 Development of induction machine emulator test bench for testing asymmetrical short circuit grid faults

The machine emulator developed as part of this thesis consisted of linear amplifiers with RL link filters to form a machine emulator, which can operate in all four quadrants. This type of testing only draws net losses, since the power drawn from the grid will be sent back to the grid less the losses. The main conclusions are as follows:

- The developed linear amplifier emulator interfacing grid has power sinking capability up to 1.2 KVA, at 120 V with a maximum per phase current of 20A. The high performance linear amplifiers possess an open loop bandwidth of 200 kHz.
- Various asymmetrical short circuit grid faults are considered for machine emulation. This is to test micro grid control algorithms or grid resiliency and to test the electrical dynamics of the squirrel cage induction machine. The higher bandwidth linear amplifier emulator tracks the symmetrical pre-fault conditions, symmetrical faults with relevant fault impedance (owing to the current limitation of the linear amplifiers).
- Though the LAs have high open loop bandwidth, the emulator current control closed loop maximum bandwidth achievable is approximately equal to 2.4 kHz. This is because of the time delays introduced by the linear amplifiers and sensors and real time system sampling time.
- The developed emulator system was shown to use a linear, trapezoidal integration integrated mathematical model for emulation accuracy.
- Experimental results were also presented to showcase the benefits of using accurate machine models and better emulator control to improve performance of emulation. The

tracking performance is good enough for not only pre-fault to fault transition but also for the fault to fault and fault to post-fault transitions.

7.1.2 Emulation of grid harmonics

This chapter presented the development of a machine emulator suitable to test grid harmonics. The conclusion of this chapter are as follows:

- The developed machine emulator can emulate the grid harmonics of order 5, 7, 11, 13. A programmable power supply of 30kVA induces harmonics to the machine emulator terminals.
- Proper emulator control logic is suggested accordingly for good emulating accuracy. The higher bandwidth linear amplifiers used are effective enough to track the reference currents dynamically during starting and loading transients.
- The experimental results with the real machine and emulator validate the accuracy of the novel emulator during grid harmonics. The higher bandwidth linear amplifiers used are effective enough to track the reference currents dynamically during starting and loading transients.

7.1.3 Emulation open circuit fault transients

This chapter presented an emulator setup to emulate open-circuit grid faults on induction machines. The main conclusions are as follows:

- The developed emulator system was capable of emulating open circuit grid faults on IM machines of up to 5 hp, with an emulating bandwidth of approximately equal to 2.4 kHz.
- An open circuit at the stator terminals essentially reflects a diminishing back-emf. Hence, this chapter illustrated the importance of using a current in voltage out model. Unlike in the previous chapters, the emulation of voltage is done in this chapter.
- A voltage behind reactance model can provide induction machine back-emf. However, the direct usage of the model in the machine emulator configuration does not serve the purpose for back-emf emulation. Hence, improvement in the machine modelling with respect to the emulator configuration is made. The new model served is a current in| voltage out model to emulate the machine back-emf.

- The emulation of stator terminal voltage in this chapter also changes the emulator configuration structure. The proposed emulator not only emulates open circuit faults but also short circuit faults in the grid proving its robustness.
- The experimental results obtained with the proposed emulator structure validated the proposed model.
- The developed test bench helps in testing and developing better algorithms for auto reclosing operations. The operators in a plant can diagnose the type of the fault during a machine mal functioning with fault signatures from the emulator.

7.1.4 Emulation of variable frequency drive converter faults

The emulator system developed in Chapter 5 was used to emulate machine behavior in the event of driving inverter faults. The main conclusions of this chapter are as follow

- Emulation of machine behavior was presented for gate-drive faults of the driving inverter. It was shown that a voltage in current out model can be used sustain for a fault in one switch or two switches of different legs in the driving inverter. However, this model did not withstand an all-switch or a complete gate drive fault.
- Hence, the current in| voltage out model in the previous chapter is also used here to emulate various single switch and multi switch open circuit faults. However, a linear current in| voltage out model could not exactly replicate the diminishing back-emf for a complete gate drive fault. Hence the magnetic saturation nonlinearities are included in the model for better emulation accuracy.
- The emulation results are validated with a laboratory sized 5 hp machine to prove the performance of the emulator. The drive converter switch fault signatures are recorded which will help in online fault diagnosis of electric drive.

7.1.5 PHIL emulation of grid using interface algorithms

In contrast to the machine emulation, a grid emulator system is developed in Chapter 6. It was used to emulate the grid behavior in the event of balanced and unbalanced loads. The main conclusions of this chapter are as follows:

- An experimental test setup is developed with a 10 kVA, OP1420-OPAL-RT three-phase Microgrid Test-Bench. The amplifiers feed a Lucas-Nuelle Solar PV inverter via a 208/400V transformer. The PV emulator is set for providing maximum values of 1000V, 1500W. The soft-switching power amplifiers in the commercial OP1420 test-bench have a 10 kHz open-loop bandwidth and a signal transfer delay of 10 μs.
- The chapter presents a compensator design method to improve an ideal-transformer-method interface algorithm for PHIL testing while ensuring high degree of accuracy.
- Analysis is done for the proposed compensators using Bode plots. The impact of the optimal compensator on PHIL accuracy is analyzed and quantified with the help of error functions and error plots.
- The chapter proposed that the dynamic accuracy can be further improved by introducing a damping resistor in the LCL filter structure and is validated with time domain simulations. Resistive damping essentially damps high-frequency oscillations during sudden transients but causes power losses. The minimal power loss introduced by the damping resistance is noted and can be disregarded if accuracy is the main concern.
- Different source-to-load impedance ratios are considered for the ITM with optimal compensator to experimentally analyze the stability and current characteristics during load transients.
- The experimental results validate the robustness of the grid emulator for a DER converter.

7.2 Future Research

- This emulation can also be realized at high powers or with further increase in load with power electronic converters, but higher-order harmonics cannot be emulated with good accuracy. This is due to the bandwidth limitations offered by switching frequency of switches.
- In addition to the upgrade of the model for magnetic non-linearities, the geometric, rotational, and thermal non-linearities can also be included for further improvement in emulation accuracy.
- The developed test bench for open circuit faults helps in testing and developing better algorithms for auto reclosing operations.

- Recording various fault signatures from the emulator can help the operators in a plant to diagnose the type of the fault during a machine mal functioning.
- The developed test bed for drive converter switch faults can be investigated with a closed loop speed or torque control with the help of field-oriented control or direct torque control.
- In closed loop controls with drive converter, sensor faults such as speed sensor or torque transducer, voltage or current sensor faults can be investigated.
- Only a few driving inverter faults were considered in this thesis. Emulation of machine behavior for other driving inverter faults can also be considered.
- Various fault tolerant and fault remedial strategies in the drive controller can also be investigated and explored with the developed emulator.

Appendix

Induction machine parameters for 220V, 16 A			**Base values of the machine**		
Parameter	**5 HP**	**0.111 MW**	**Parameter**	**5 HP**	**0.111 MW**
$R_s(\Omega)$	0.9649	0.0314	$V_{base}(V)$	265.5	460
L_s(H)	0.00387	0.796 µ	$I_{base}(A)$	4.68	139.31
$R_r(\Omega)$	1.08	0.02	$Z_{base}(\Omega)$	56.73	1.906
$L_r(H)$	0.00906	0.796 µ	$L_{base}(H)$	0.15	0.005
$L_m(H)$	0.148	0.01726	$\omega^e_{base}\left(\frac{rad}{sec}\right)$	377.14	377.14
$H(sec)$	0.0138	1.45	$T_{base}(N-m)$	19.78	588.63
$B\left(Nm\frac{sec}{rad}\right)$	0.00209	0.0155	$B_{base}\left(Nm\frac{sec}{rad}\right)$	0.105	3.121
P	4	4	$\omega^m_{base}\left(\frac{rad}{sec}\right)$	188.57	188.57
Emulator control system parameters					
$k_{LA} = G = 20; \tau_{LA} = 25\ \mu s; R = 0.1\ \Omega; L = 3\ mH; k_c = 1;\ \tau_c = 14\ \mu s; T_s = 20\ \mu s$					
Machine parameters when dynamometer is coupled					
$J_{new} = 0.0558; B_{new} = 0.00632;$					

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