Exploration of the Effects of Isolation-feature Geometry on the Off-state Breakdown Voltage of AlGaN/GaN HFETs

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ABSTRACT

Exploration of the effects of isolation-feature geometry on the off-state breakdown voltage and gate leakage of AlGaN/GaN HFETs

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Over the past two decades and specially more recently, AlGaN/GaN heterojunction field effect transistors (HFETs) have drawn a great deal of attention due to their excellent performance in high-frequency power amplifiers and RF switches explored in the 5G-LTE applications. Since the ability to operate at high voltages is crucial in delivering both the large RF gain/output power and the high voltage switching capabilities, boosting the already high off-state breakdown voltage (BV_{off}) of these transistors to much higher values has been of substantial importance.

While a number of techniques have already been developed for realization of high breakdown voltage AlGaN/GaN HFETs, in addition to imposing certain challenges to the fabrication procedure, these techniques impose strain on satisfying high frequency response requirements. Among these techniques, the field-plate (FP) is the most widely used. As an alternative to this mainstream technique, this thesis presents a novel concept of field plating without incorporation of any physical plate. In this approach, I have assessed the suitability of isolation feature geometry and existence of surface states in modifying the profile of the longitudinal electric field, and enhancement of the off-state breakdown voltage. This approach while using a simple fabrication process, is capable of limiting the degradation of the frequency response commonly observed with FP implementation.

In order to explore the limitations of this technique and to formulate guidelines for achieving high BV_{off} values, I have experimentally and theoretically studied the effects of alternative isolation feature geometries on high voltage device characteristics of AlGaN/GaN

HFETs. According to our explorations on three different categories of isolation features (including conventional mesa, non-slanted fin, and slanted fin), the peak of the electric field at the drain edge of the gate, which is responsible for impact ionization, is reduced as a result of tailoring its profile when a more resistive path is imposed on the drain access region by shrinking the width of the isolation feature geometry. While HFETs realized on fins of smaller widths benefit more from the depleting effect of acceptor sidewall surface states and consequently a higher BV_{off}, they suffer from a lower current density in the on-state. The slanted fin isolation feature geometry that I have proposed, while maintaining high breakdown voltage in the off-state, reduces the resistance in the on-state which is represented by its highest Baliga's figure of merit (BFOM) among the three categories of isolation feature geometries.

In addition, in this thesis I have explored the effect of isolation feature geometry on the reverse gate leakage, which is considered as one of the main problems limiting the full-scale commercialization of these HFETs. In this exploration, I have studied the significance of room temperature leakage from the top surface gate as well as gated-sidewalls to the 2-D electron gas (2DEG) for a wide range of gate-source voltages (V_{GS}) (i.e. below and above the threshold voltage) and at zero drain-source bias. I have proved that in the explored fin-type HFETs that are sub-micrometer-wide, for all values of V_{GS} leakage through the gated sidewalls is more significant than the leakage from the top surface gate. This is while in the mesa category, the sidewall leakage is of substantial importance only at more positive values of V_{GS}, and leakage from the top surface gate takes over at more negative V_{GS} values. I have demonstrated that the discrepancy in the dominance of the aforementioned leakage paths at more negative V_{GS} values among the explored fin and mesa-type HFETs is due to the larger amount of the electric field across the barrier in the gated region of the mesa-type HFET for this range of V_{GS}.

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List of Abbreviations

Abbreviation	Description
2DEG	Two-dimensional electron gas
HFET	Hetero-junction field effect transistor
UID	Unintentionally doped
TAT	Trap-assisted-tunneling
PF	Poole-Frenkel
FN	Fowler-Nordheim
TFE	Thermionic field emission
FOM	Figure of merit
JFOM	Johnson figure of merit
BFOM	Baliga figure of merit
DIBL	Drain induced barrier lowering
EBL	Electron beam lithography
NPGS	Nanometer pattern generation system
SEM	Scanning electron microscope
UV	Ultra violet
IPA	Isopropyl alcohol
DI water	Deionized water
MERIE	Magnetically-enhanced reactive ion etching
PECVD	Plasma enhanced chemical vapor deposition
RTA	Rapid thermal annealing

Chapter 1

Introduction

1.1 Overview of III-nitride technology

Due to its excellent electronic properties such as large bandgap (3.4 eV) [1], high low-field electron mobility (1500 $cm^2/V/s$) [1], high critical electric field (>3 MV/cm) [1],[2],[3],[4], superb saturation velocity (2.5×10^7 cm/s) [5], and acceptable thermal conductivity (1.3 W/cm/K) [6], GaN has been extensively investigated as the semiconducting channel in transistors of high-power/high-frequency amplifiers and RF switches, in addition to switches of power electronic circuitry. As a result of these properties, GaN-channel transistors have demonstrated a record of 8 W/mm power density with an associated power-added efficiency of 28.8% at 94 GHz [7], f_T/f_{MAX} of 454/444 GHz [8], current densities in excess of 1 A/mm, and breakdown voltages (V_{BR}) exceeding 2000 V [9].

Among GaN-based field effect transistors (FETs), AlGaN/GaN heterostructure FETs (HFETs) have so far played a significant role in high power, high frequency and high temperature applications such as power-generation, wireless-communication, aerospace, automotive and petroleum industry [10]. For instance, in aerospace industry bulky hydraulics and mechanical control systems can be replaced by such wide bandgap power electronic devices to reduce the aircraft weight [10]. In automotive industry, implementation of these heat-tolerant electronics has been shown to improve the performance and reliability of the automobiles [10].

In a wide range of applications from automotive to telecommunications, the ability to operate at high voltages has been crucial in delivering both the large RF gain/output power and the high-voltage switching capabilities.

1.2 Physics and mechanisms of breakdown

Depending on the application, breakdown mechanisms need to be considered in all the present junctions and under different bias conditions. As for the bias conditions, the on- or off-state breakdown mechanisms are studied in correlation with the selection of gate-source bias either greater or smaller than the threshold voltage (V_{th}), respectively.

Among two-terminal devices, generally speaking there are two breakdown mechanisms, namely: Zener (tunneling) breakdown and avalanche breakdown. In Zener breakdown a high electric field rips electrons from covalent bonds, directly creating an electron-hole pair and contributing to a rush of current. The transition of electron from the valence band to the conduction band involves electron tunneling through the energy barrier. In contrast, in avalanche breakdown, the electric field provides sufficient energy to free carriers to break covalent bonds and to create additional free carriers keen in participating in further avalanching collisions. This is also known as impact ionization. In order to identify the dominant breakdown mechanism among these two, temperature-dependent measurements are implemented. As the temperature increases, in the avalanche breakdown V_{BR} increases, while the opposite temperature dependence is valid for the Zener breakdown. This is because, by increasing the temperature electron mean free path becomes shorter and as a result electrons do not acquire sufficient energy to trigger impact ionization if a stronger electric field is not provisioned at higher temperature. However, for the case of Zener breakdown, raising the temperature increases the thermal velocity and the flux of valence band electrons available for tunneling, which considering the temperature independence of the tunneling

probability, consequently reduces the breakdown voltage. In devices of more complexity and larger number of terminals, while these mechanisms are still relevant, in certain modes of breakdown, the device breakdown is observed when still at a given junction the onset of either of the aforementioned two mechanisms has not been met.

In all breakdown events, breakdown is marked by a steep increase in the current (i.e. either exponential or sub-exponential, referred to as hard- or soft-breakdown, respectively). As an example, in an n-channel HFET the off-state breakdown voltage (BV_{off}) is the drain voltage marking an exponential increase in the drain current when the gate-source voltage is selected smaller than the threshold voltage. This is one of the most significant figure of merits (FOMs) of a power device. This is because, the maximum output power for class "A" amplifiers is determined by the off-state breakdown voltage ($P_{max} = BV_{off} \times I_{max}/8$) [11]. To maximize BV_{off}, intensive work has been done to investigate the physical origin of the off-state breakdown and to identify the dominant breakdown mechanism, with the aim of proposing technical solutions for increasing BV_{off} and enhancing the robustness of the transistor.

Historically, the off-state breakdown mechanisms of AlGaN/GaN HFETs has been a controversial issue. While it is shown by many groups that the off-state breakdown in AlGaN/GaN HFETs is linked to the presence of the surface states [12] and that it can be improved by surface passivation with SiN and other dielectric materials [13], it is demonstrated by other researchers that the main mechanism responsible for the off-state breakdown in AlGaN/GaN HFETs is the impact ionization in the channel [14], [15] and that the surface passivation degrades the breakdown characteristics [16], [17]. Such seemingly contradictory observations are levied by the complex physics of the underlying mechanism of the breakdown in AlGaN/GaN HFETs.

As mentioned earlier, breakdown has been studied both under a variety of bias conditions and at different junctions of an HFET. Based on the existing body of work, physical mechanisms responsible for the breakdown in GaN-based power transistors include drain-source breakdown, drain-gate breakdown, drain-bulk breakdown and channel breakdown.

1.2.1 Drain-source breakdown

Meneghini *et al.* [18] have claimed that at gate voltages close to the threshold voltage, the drain-source leakage, which is due to the short channel effects and/or punch-through, is the dominant breakdown mechanism. This leakage current is strongly dependent on the gate voltage and can be minimized by shifting the gate voltage towards more negative values. Apart from varying the doping density in the buffer [19], drain-source leakage current can be mitigated by implementing a double heterostructure configuration, which can improve the depletion in the buffer and suppress the punch-through current components [20].

1.2.2 Drain-gate breakdown

In addition to the drain-source leakage, the reverse current of the gate Schottky junction is one of the components that affects the drain current. One of the mechanisms that can lead to gate breakdown is the drain-gate leakage via the surface states. In broad terms, in the off-state and at high drain voltages, electrons can tunnel through the gate to the surface states and cause leakage current and consequently power dissipation, which can result in thermal run away[1] and breakdown [12]. This type of breakdown that has a negative temperature coefficient, can be improved by surface passivation [21]. In addition to hopping through the surface states, other mechanisms including defect assisted tunneling [22], thermionic emission at the Schottky gate [22], Poole–Frenkel emission [22] and leakage via the extended defects [23] have been reported to contribute

[1] That is, an uncontrolled positive feedback in which an increase in temperature changes the conditions in a way that causes a further increase in temperature.

to drain-gate leakage through the AlGaN barrier. The general remedy to reduce the gate-related leakage is implementing a metal–insulator– semiconductor (MIS) structure as an alternative to the conventional Schottky-gate [24].

1.2.3 Drain-bulk vertical breakdown

Bulk leakage current is another leakage mechanism, which can be reduced by replacing the GaN buffer layer with a semiconductor material of larger band gap such as AlGaN [24] or implementing thicker GaN layers [24]. The former solution improves the breakdown by enhancing the insulating properties of the buffer layer, while the latter does this by decreasing the density of dislocations. Removal of the Si substrate and transferring the HFET to an insulating carrier wafer such as polycrystalline AlN or glass has been demonstrated to improve the breakdown voltage by suppression of the vertical leakage current in GaN-based HFETs on Si substrate [25], [26].

1.2.4 Channel breakdown

Nakao *et. al.* [15] have claimed that the impact ionization in the channel near the drain-edge of the gate, where the electric field peak is located, dominates the off-state breakdown voltage. This breakdown mechanism is reported by other groups, where they have observed a positive temperature coefficient in the breakdown voltage [14]. In some works, the carriers initiating the impact ionization are suggested to originate from the gate injection [15]. This is because, an improvement in the breakdown voltage is observed with post-gate thermal annealing and reduction of the thermionic emission component of the gate leakage-current [27]. However, Wang *et al.* [4] have stated that in AlGaN/GaN HFETs upon presence of a high quality AlGaN barrier layer, gate injection is not substantial due to a large Schottky barrier height (e.g. 1.1 eV for Ni/AlGaN contact), conduction band offset at the heterointerface and absence of doping in the AlGaN barrier layer. They have argued that due to the high level of unintentional *n*-type doping in the buffer layer of AlGaN/GaN epilayer, source injection through the buffer can also induce impact ionization.

In light of the outlined mechanisms, Ohno *et al.* [11] have investigated the effect of surface passivation on the breakdown characteristics of AlGaN/GaN HFETs to understand which breakdown mechanism limits the off-state breakdown voltage among these devices. To this end, they have performed temperature dependent measurements on AlGaN/GaN HFETs with and without surface passivation. These devices had gate length (L_G) of 1.5 µm and gate-source (L_{GS}) and gate-drain (L_{GD}) spacing of 1.5 µm and 2 µm, respectively. The gate width was 20 µm and the threshold voltage was about -3V. Results show a positive temperature dependence of the off-state breakdown voltage. Observing this signature allows stablishing a link to impact ionization in the channel. It is shown in Figure 1. 1 that, although the off-state breakdown voltage in these devices is not related to the surface breakdown, it is improved with surface passivation. In order to understand why surface passivation increases the breakdown voltage, electroluminescence distribution of both devices (i.e. with and without surface passivation) has been studied by a microscope and a charge-coupled-device camera. As demonstrated in Figure 1. 2, in the device without surface passivation electroluminescence is observed close to the gate-edge of the drain electrode suggesting that the peak electric field is formed there. This observation is in contrast with our understanding of the behavior of standard III-V HFETs, in which the electric field peaks at the drain-edge of the gate electrode. They have attributed this to the so-called virtual gate effect.

As depicted in Figure 1. 3 (a), they have claimed that the virtual gate, which forms between the gate and drain electrodes by injection of electrons through the gate to the surface states, has almost the same potential as the gate electrode. As a result, a large potential-drop occurs at the drain-edge where electroluminescence intensity is the maximum. However, for the case of devices with surface passivation, the maximum electroluminescence intensity is observed at the drain-edge of the gate (Figure 1. 3 (b)). The shift of electric field peak from the gate-edge of the drain towards

the drain-edge of the gate electrode as a result of surface passivation can be explained by the modified potential distribution across the channel between the gate and drain electrode. In broad terms, the change in the potential distribution as a result of surface passivation might be due to the suppression of the electron trapping at the surface.

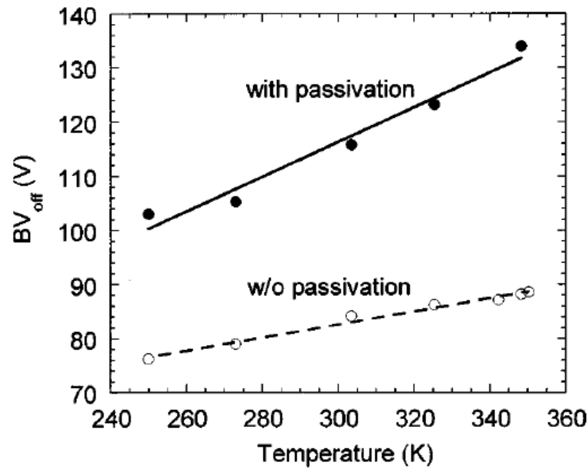

Figure 1. 1 Temperature dependence of off-state breakdown voltage in AlGaN/GaN HFETs [11].

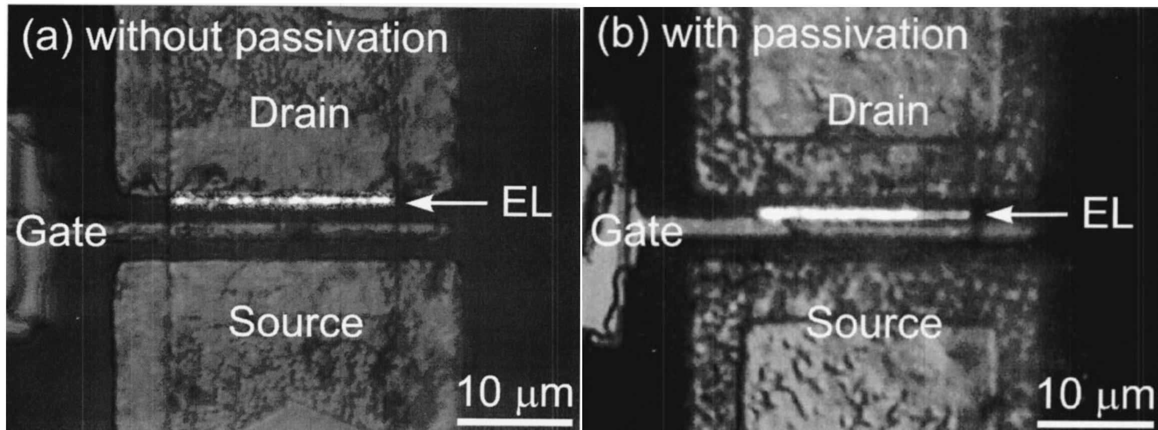

Figure 1. 2 Electroluminescence distribution in AlGaN/GaN HFETs biased at V_{GS}= -2 V (a) without surface passivation and biased at V_{DS}= 70 V (b) with surface passivation and biased at V_{DS}= 100 V [11].

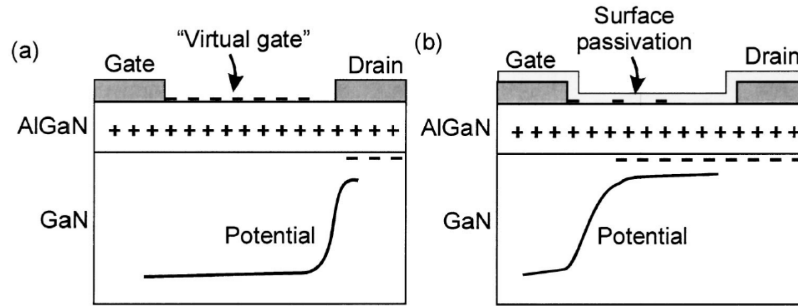

Figure 1. 3 Schematics of charge distribution and potential profile between the gate and drain electrodes; (a) without surface passivation (b) with surface passivation [11].

The reported ambiguity and even inconsistency among the published records suggest that there is no unique mechanism that can describe the off-state breakdown in AlGaN/GaN HFETs. Therefore, determination of the dominant breakdown mechanism requires consideration of the device structure, bias condition, channel temperature and operating conditions [28].

1.3 Literature review of the explored avenues for increasing the breakdown voltage

Over the past few years, enormous progress has been made in improving the breakdown voltage of GaN-based HFETs. For instance, GaN HFETs exhibiting record breakdown voltage over 2000 V have been recently reported [29]. Nevertheless, in much of the reported literature while improving the off-state breakdown voltage of HFETs, some of the other FOMs are neglected. For instance, in much of the reported literature a large gate-drain spacing along with a field-plate[2] (FP) is adopted to improve the breakdown voltage, which adversely affects the on-resistance and high frequency response characteristics of the devices [29][30]. Incorporation of FPs also adds additional steps to the fabrication process, which brings about more complexity,

[2] A field-plate is a gate- or source-connected metallic plate provisioned over the gate-side of the drain access region of an HFET, distanced further away from the channel than the gate. The effect of this sheet of metal is to form a more distributed electric field profile along the channel and to lower the peak of the electric field profile.

reliability and yield concerns. Improving the epitaxial layer structure, which is another approach to enhance the breakdown voltage through mitigation of the bulk leakage, also requires fabrication facilities not available in most clean rooms. Therefore, in realization of high breakdown voltage HFETs, maintaining a trade-off between the FOMs and developing a fabrication technique which is neither expensive nor complex, is necessary. In the following, some of the main reported techniques that have so far been used to improve the breakdown voltage, are presented.

Xing *et al.* [31] have achieved high breakdown voltage AlGaN/GaN HFETs by implementing multiple FPs over dielectric passivation layers (as shown in Figure 1. 4). In their work, a 4 nm-thick layer of SiN has been deposited on top of AlGaN barrier layer to reduce the gate leakage. The AlGaN/GaN HFETs had a T-shape gate layout with gate width of 2 × 25 µm, L_G of 1.5 µm and L_{GD} in the range of 4 to 28 µm. After mesa etching and deposition of Ohmic (Ti/Al/Ni/Au) and Schottky (Ni/Au) electrodes, surface passivation was performed by deposition of approximately 180 nm SiN by plasma enhanced chemical vapor deposition (PECVD). The first FP was formed by depositing a 1.5 µm long Ni/Au layer on top of the passivation layer. The FP was connected to the gate at the gate pad and the overlap between the gate and FP metal was about 0.8–1 µm. Another roughly 180 nm-thick layer of SiN was then deposited by plasma enhanced chemical vapor deposition (PECVD) and a substantial increase in the breakdown voltage up to 700 V was observed at L_{GD} of 24 µm. The second FP was formed by depositing another 1.5 µm long Ni/Au layer on top of the second layer of SiN. This metal line was shifted toward the drain side by another 0.5–0.7 µm. Finally, the last 180 nm-thick SiN layer was deposited by PECVD, which resulted in a breakdown voltage of 900V compared to a breakdown voltage of 250 V of the standard passivated devices with no FPs and at L_{gd} of 24 µm. The schematic cross section of the completed device is illustrated in Figure 1. 4. Although the so-called multiple FP technique has

shown to be effective in improving the breakdown voltage, it involves multiple dielectric and metal deposition steps, which add to the complexity of the fabrication procedure. Furthermore, this technique degrades the high frequency performance of the device due to the high gate capacitance, which is a result of multiple FP configuration.

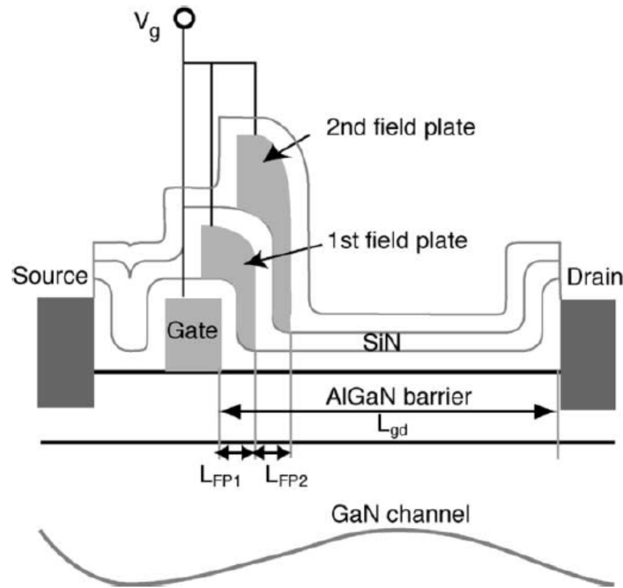

Figure 1. 4 Schematic of an AlGaN/GaN HFET with multiple FPs [31].

In comparison with the discrete multiple FPs, the so-called slanted FP offers higher breakdown voltages, while being easier to fabricate due to its self-aligned nature [32]. In order to achieve the slanted FP, Dora *et al.* [33] have deposited the gate metals inside SiN_x trenches with sloped side walls (shown in Figure 1. 5). A double layer lithography was implemented to produce a lift-off overhang (shown in Figure 1. 6), which is used in the etching process as a tool to yield the sloped sidewalls of the SiN_x trenches. This is because the etch rate of SiN_x beneath the lift-off overhang is lower than that of areas exposed to the direct gas flux. SiN_x was removed at the openings using a CF_4 reactive ion etching (RIE) at a pressure of 20 mT with a gas flow of CF_4/O_2:20/2 sccm. The slope of the sidewalls was engineered by varying the pressure in the RIE,

the over-etch time and the CF_4/O_2 ratio. In order to obtain self-aligned slanted FPs, gate metals were e-beam evaporated on the samples rotating at an angle of 15˚ to the incident metal flux. For suppressing the parasitic air breakdown, which occurs at air regions adjacent to the gate-drain area, after the passivation, AlGaN/GaN HFETs with slanted FPs were immersed in Fluorinert FC-77 (which is a high dielectric strength liquid). This resulted in devices with breakdown voltages as high as 1900 V, while the breakdown voltage of devices with the same geometry and epilayer structure but with a conventional gate (i.e. without FP) was around 200 V.

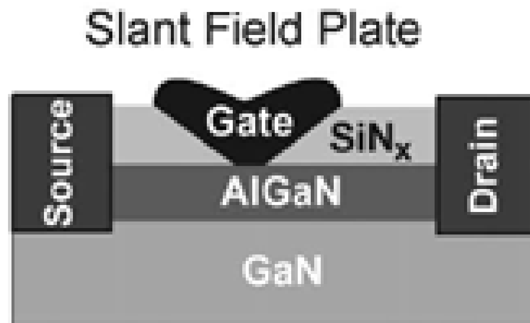

Figure 1. 5 Schematic cross section of an AlGaN/GaN HFET with a slanted FP [33].

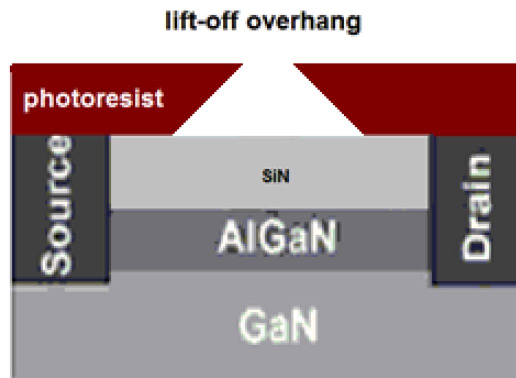

Figure 1. 6 Schematic of an overhanging structure [33].

Deguchi *et al.* [34] have fabricated a linearly graded FP by PECVD of two layers of 3.0 μm-thick SiO_2 and 100 nm-thick phosphosilicate-glass (PSG) on the AlGaN/GaN epilayer. The top deposited insulating layer was then coated with the photoresist, patterned and dipped in BHF for the wet etching of the underlying layers. As shown in Figure 1. 7, due to the difference in the etching rate of the SiO_2 and PSG, a linearly graded pattern is developed. The slope of the graded SiO_2 was engineered with altering the phosphorus concentration in PSG layer. It is shown in this work that as the phosphorus concentration increases the slop (θ) of the SiO_2 layer reduces. Results from I-V characteristics demonstrate R_{on} and V_{BR} of 4.2 mΩcm^2 and 830 V at gate-drain spacing of 10 μm, respectively. Figure 1. 8 shows a schematic cross section of a fabricated AlGaN/GaN HFET with a linearly graded FP and coated with polyimide, which is used to prevent surface breakdown.

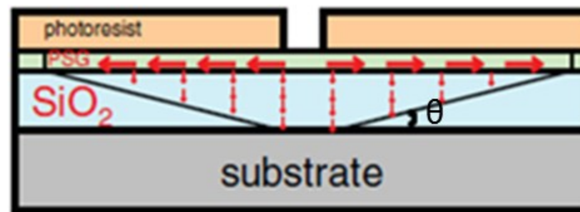

Figure 1. 7 Schematic of the wet etching of SiO_2/PSG [34].

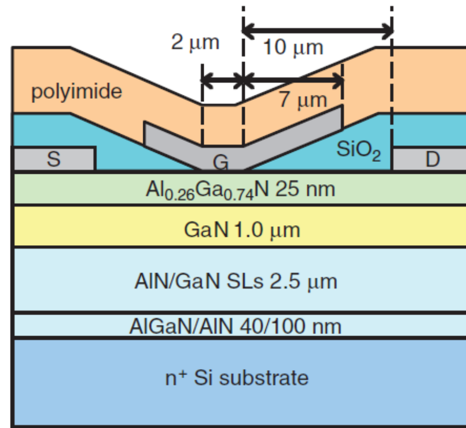

Figure 1. 8 Schematic cross section of an AlGaN/GaN HFET with graded FP [34].

Suemitsu *et al.* [35] have developed slanted FPs using multi-step SiCN. The composition ratio of C and N in the 200 nm deposited SiCN layer is dependent on the flow rate of the carrier gasses (i.e. H_2 and NH_3) in the PECVD reactor. As shown in Figure 1. 9, this composition ratio affects the cross-sectional shape of the etched SiCN. Based on secondary ion mass spectroscopy (SIMS) analysis, carbon/nitrogen composition ratio was 3:1 (1:3) in the SiCN samples with the carrier gas of H_2 (NH_3). Due to the dependence of the etching rate on carbon/nitrogen composition, by gradually (10 steps and more) varying the mixture ratio of the carrier gasses (i.e. H_2 and NH_3) in the PECVD reactor, a slant SiCN sidewall was obtained. After SiCN layer deposition, an e-beam lithography was performed to define the gate pattern, after which SiCN was etched by C_2F_6 RIE at 2 Pa with an RF power of 100W, followed by SF_6 RIE at 5 Pa with an RF power of 50W. As illustrated in Figure 1. 10, Ni/Au (20/170 nm) was evaporated normal to the sample for the gate metal and for FP metallization the sample was tilted so that the deposition was performed only at the drain side of the SiCN sidewall. At the end, contact holes were opened on Ohmic electrodes followed by evaporation of Ti/Pt/Au as pad metals (20/20/350 nm).

One key element in examining the efficiency of a FP is to investigate the quality of the interface between the dielectric and the semiconductor, which is made possible by evaluating the density of traps at this interface. To this end, Suemitsu *et al.* have characterized threshold voltage instability of sample metal insulator HFETs with the same epitaxial structure as the HFETs with FP. Results show that the trap density value estimated for the SiCN/AlGaN interface is smaller than those reported for SiN/AlGaN and Al_2O_3/AlGaN. The low trap density at the SiCN/AlGaN interface is attributed to the hydrogen annealing at 350°C (i.e. during SiCN deposition in the PECVD reactor), which improves the surface morphology and eliminates surface contaminations [36]. Results from I-V characterization of the devices with FP deposition in 3,4 and 10 steps show that by increasing the number of steps in SiCN deposition, a higher transconductance, breakdown voltage (from 84 V (3 steps) to 134 V (10 steps)) and suppression in the current collapse is observed. In addition, by increasing the number of deposition steps an enhancement in the maximum current gain cutoff frequency is achieved, which is partially due to the improved transconductance.

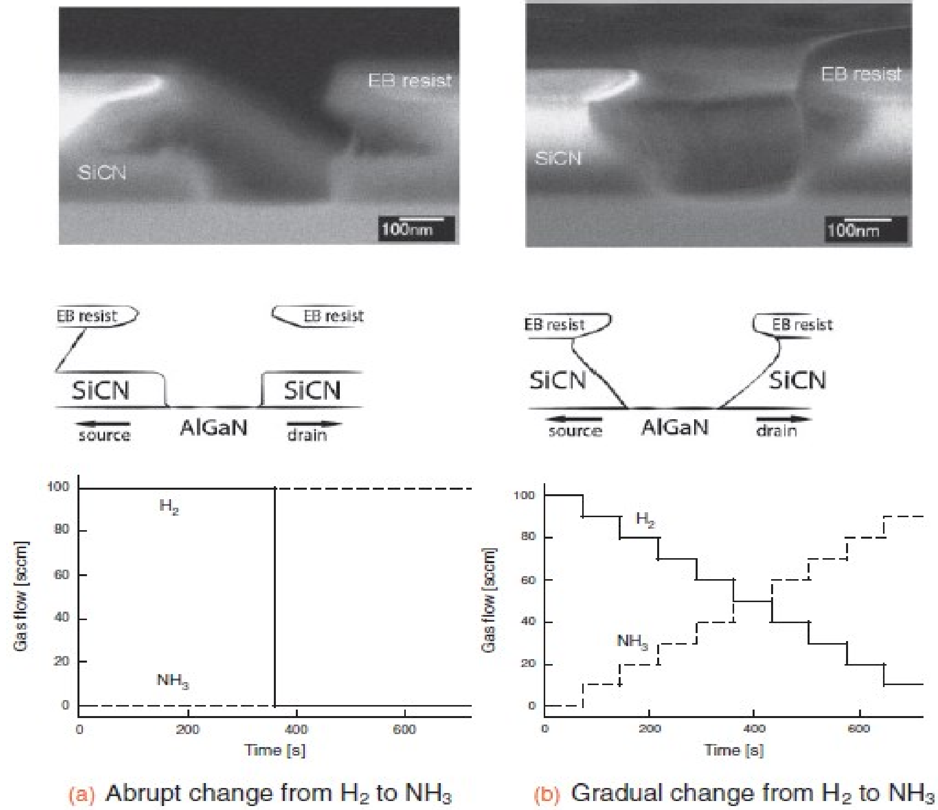

Figure 1. 9 Cross-sectional SEM images of the etched SiCN (upper panels), cross-sectional sketches of the etched SiCN (middle panels) and illustration of the flow rate of the carrier gases during PECVD (lower panels). The carrier gas is (a) abruptly changed from H_2 to NH_3 and (b) gradually changed over 10 steps from H_2 to NH_3 [35].

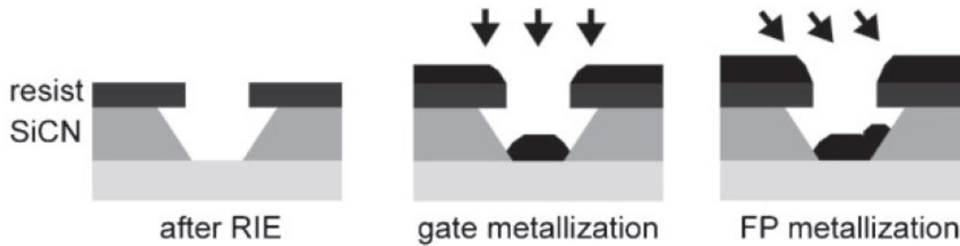

Figure 1. 10 Schematic of the gate and FP metal deposition [35].

Ma *et al.* [37] have proposed a new concept of field-plating, which instead of variation in the slope of the gate metal or the dielectric layer, modulates the pinch-off voltage by varying the

width of the triple-gate 3D HFET. They have illustrated that, by smoothly changing the width of the channel the pinch-off voltage changes gradually and the breakdown voltage improves. In this work, slanted tri-gate devices were fabricated by first etching the AlGaN/GaN epitaxial layer into mesas with a slanted width and a depth of ~160 nm. This step was followed by deposition of 20 nm of Al_2O_3 by atomic layer deposition as the gate dielectric and then gate metallization. These devices offer a high breakdown voltage of 1350 V at gate-drain spacing of 10 μm, which is an increase of about 500 V in V_{BR} compared to the counterpart planar devices. Top-view SEM image and cross-sectional schematic of the slanted tri-gate metal-oxide-semiconductor high electron mobility transistor (MOSHEMT) is shown in Figure 1. 11.

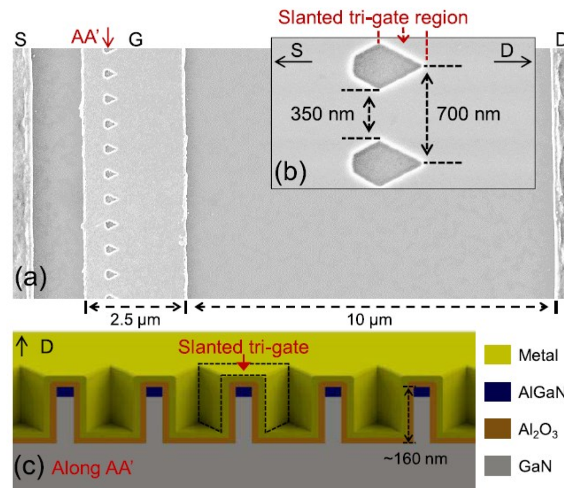

Figure 1. 11 (a) and (b) Top-view SEM images of the slanted tri-gate MOSHEMT. (c) A cross-sectional schematic of the slanted tri-gate along the arrow AA’ [37].

1.4 Research objective

Due the significance of high voltage operation of the transistors used in high-power/high-frequency applications and based on the drawbacks of field-plate implementation as the mainstream technique for improving the breakdown voltage, the goal of this research is to enhance the breakdown voltage in GaN-channel HFETs without adding to the gate capacitance and the

additional steps required in the fabrication process. Considering the depleting effect of the negatively charged sidewall surface states in engineering the two-dimensional electron gas (2DEG) density and hence channel resistivity [38][39], the present work has assessed the suitability of isolation feature geometry and surface states in improving the breakdown voltage, via the simulation and device fabrication. In addition, I have compared high power and high frequency figures of merit of these HFETs to identify the effectiveness of the proposed device structure for these applications. As a part of this thesis, the effect of isolation feature geometry on the reverse gate leakage, which is considered as one of the impeding factors in full-scale commercialization of these HFETs, has been explored.

Chapter 2

Correlation between sidewall surface states and off-state breakdown voltage of AlGaN/GaN HFETs

The contributions of this chapter have been already published and most of the materials are taken from [40].

2.1 Introduction

As mentioned in chapter 1, over the past few years enormous progress has been made in improving the off-state breakdown voltage of GaN-based HFETs by formulating solutions based on diminishing the peak of the drain induced electric field at the drain edge of the gate electrode. In most of these solutions a large gate-drain spacing along with a field-plate is adopted to improve BV_{off} [41],[42],[43]. So far, implementing multiple field-plates [31], 3-D field-plates [44], and slanted variety field-plates [3],[33],[37],[45], have been demonstrated to be capable of smoothening the electric field profile and boosting the breakdown voltage to values even well exceeding 1 kV. Although employing FP is effective in realization of high breakdown voltage HFETs, the resulting augmented gate capacitance has been demonstrated to limit the high frequency figures of merit of these transistors. This is less of a problem for those transistors with slanted field-plates, since due to their geometry the size of the added capacitance is smaller

[3],[33], [37],[45]. However, obtaining slanted FP configuration requires precise control over the thickness and slope of the dielectric material layer, maintaining which is extremely difficult and challenging.

Recently, many attempts have been made to improve the off-state breakdown voltage of III-nitride HFETs without laborious engineering of the slope and thickness of the dielectric material layer under the field-plate. These techniques mainly rely on the so-called perforated channel layout [46] in which the channel is partially removed in the gated region [37],[46],[47],[48],[49],[50],[51],[52]. While these techniques can realize field-plates with a simpler fabrication process, they still suffer from the parasitic effect of FP implementation, which degrades the high frequency response.

In addition to exploring field-plates, the asymmetric definition of the 2DEG channel (i.e., higher source-side compared to the drain-side 2DEG concentration) has been also attempted through using the local contribution of strained passivation layers to engineer the in-plane strain and piezoelectric polarization at the III-Nitride heterojunction [53],[54]. This approach has its roots in the polar nature of the 2DEG induction in Wurtzite c-plane III-Nitride heterostructures [55]. This latter solution, which relies on only adding to the resistance of the drain access region, is expected to have a much better chance in preserving the frequency response, while at the same time improving BV_{off}. Presence of p-GaN cap which is not self-aligned to the gate electrode is also capable of increasing the resistance of the source and drain access regions and partially depleting the 2DEG channel, hence boosting the BV_{off} [56]. Employing such a cap layer that has been successfully demonstrated to deliver AlGaN/GaN HFETs of positive threshold voltage, or in other words enhancement-mode operation, has nonetheless certain disadvantages compared to another

alternative technology for realization of such transistors by simply adjusting the width of isolation feature geometry [57]. One of those disadvantages is that for achieving a transistor of depletion-mode (i.e. of negative threshold voltage) that is often used as a current source side-by-side of the enhancement-mode transistor, the p-GaN cap should either be etched away or to begin with only selectively overgrown in the gated-channel section of the enhancement-mode transistor. As an alternative to the use of strained passivation layers and p-GaN cap, relying on acceptably deterministic set of information on pinning of the fermi level of the non-polar a- and m-planes of Wurtzite III-Nitrides towards inducing a depletion region [38],[58], a novel way of securing the asymmetric definition of 2DEG is expected to yield a reliable design framework. This design framework, nicely fits with the aforementioned technology developed for side-by-side realization of enhancement-/depletion-mode pair of AlGaN/GaN HFETs through properly adjusting the width of the isolation feature geometry.

To the best of the author's, while the possibility of using the correlation between the status of the states on the exposed top surface of the AlGaN barrier and the breakdown voltage has been suggested in [33], investigating the existence and use of such a correlation between the breakdown voltage and the proximity of the channel to the pinned non-polar facets has been overlooked. In this chapter, accordingly I present a novel concept of field plating without incorporation of any physical plate. In this approach, while using a simple fabrication process which unlike FP implementation does not require any additional steps to the fabrication process of a conventional HFET, I take advantage of the large surface to volume ratio of fin isolation features already explored and popular among GaN-based HFETs, in which case surface states play a substantial role in shaping of the electrical characteristics of these devices. Considering the fermi level pinning at sidewall surfaces of GaN grown in <0001> direction and channel depletion in proximity of the

non-polar m- and a-planes of GaN [38],[39],[59], for the first time the suitability of isolation feature geometry and existence of surface states in modifying the profile of the longitudinal electric field, and enhancement of the off-state breakdown voltage, has been assessed.

2.2 Device fabrication

I have performed the fabrication of the devices at McGill University Nano-tools Micro-fab facilities. The epitaxial layer structure used in this work is a Ga-face Wurtzite $Al_{0.25}Ga_{0.75}N$/GaN heterostructure composed of a 25 nm thick barrier and 1.7 µm thick GaN buffer (which was Fe doped away from the channel) grown on a 4-inch 4-H SiC substrate. As in this project realizing sub-micron gate AlGaN/GaN HFETs of submicron isolation features is attempted and because optical lithography cannot yield such small dimensions, electron-beam (e-beam) is adopted as the mode of lithography. Modifying the previous process recipe and device layout developed by former members of our group, in compliance with the feature sizes of the fin HFETs, was an important step towards fabrication of high breakdown voltage devices. The following steps are accomplished in modifying the previous fabrication process into a process recipe (Appendix I) capable of realization of AlGaN/GaN HFETs explored in this project:

- Designing new pattern layouts compatible with electron beam lithography (EBL) (i.e., specifications of the e-beam resist and the writing machine) and improving the registration process

- Choosing the appropriate resist in correlation with the specifications of the writing machine (i.e. beam intensity, spot size, accelerating voltage and working distance) and patterns' feature sizes

- Improving source and drain Ohmic contacts by engineering the metal stack (i.e., type of metal and its thickness for each layer) and annealing conditions.

While e-beam lithography is more precise in realization of sub-micron feature sizes in comparison with optical lithography, obtaining a very accurate alignment through this process was challenging in the beginning. In order to improve the alignment between the masking layers during the process of e-beam lithography, I have implemented a variety of registration marks in terms of size and shape as well as distance from the main pattern. Although adding smaller size registration marks is one way to fine tune the alignment, this requires a larger number of registration marks, which leads to higher dosage of electron beam and consequently accumulation of electrons at the surface of the sample, which causes deviation of the electron beam from its designated path. In order to alleviate this problem, one of the remedies that I explored was minimization of the exposure time by reducing the SEM resolution during the alignment. Although this solution was quite a bit useful in alleviating the electron beam deviation, I needed to entertain solutions to rule out this problem. In order to minimize the exposure dosage and consequently accumulation of the electron beam during the registration of gate fingers and gate pad, in addition to reducing the gate pad surface area, which provides a larger separation between the registration marks and gate pad, I have adopted an anti-charging agent (DisCharge H_2OX2 from DisChem), which was very useful in mitigating the deviation of the electron beam during the gate finger registration.

Due to the small feature sizes of the fins proposed in this work, I have used Ma-N 2403 negative resists, which generates a thin layer of 300 nm with a high resolution of 50 nm.

2.2.1 Pattern generation and registration (EBL)

DesignCAD Express 16 is used for generating the patterns required for EBL. The maximum pattern area including the registration marks is limited to 120 μm×120 μm, which is the maximum

dimension of EBL writing field. This restriction limits the number of registration marks and consequently the accuracy of the alignment. Once a pattern was designed, I generated a run file in a nanometer generation pattern system (NPGS) to record the exposure conditions for each drawing element in the pattern. NPGS software is used for performing EBL by controlling the position of the electron beam of the scanning electron microscope (SEM) in accordance with a desired writing pattern.

During the first step of the EBL process, the mesa, fins, and the L-shaped registration marks were registered on the clean and resist-covered sample. In this step a negative resist was used because, all of the surface area of the sample except a small portion (i.e., the mesa/fin and registration marks) was to be etched. The printed registration marks are used as a reference for alignment during the second and third steps of EBL, which is registration of the patterns for the source and drain Ohmic contacts and gate Schottky contact, respectively. After the exposure with the 20 KeV e-beam, the sample was developed in Ma-D 525 to remove the resist from the unexposed area.

2.2.2 Etching process

The magnetically-enhanced reactive ion etching (MERIE) by using Cl_2/Ar plasma in an Applied-Materials P5000 MERIE system was used for etching these patterns followed by removing the resist from the sample with acetone. Table 2. 1 summarizes the adopted parameters in etching based on the previous works in the group [60], [61]. Then the sample was coated with MMA(8.5)MAA-EL11/PMMA-A2 co-polymer positive resist followed by coating with the anti-charge agent (DisCharge H_2OX2) for the second step of EBL, which is registration of Ohmic contacts. Following the exposure of the sample with e-beam at areas defined for the Ohmic

contacts, the sample was immersed in DI water for 2 min to remove the anti-charging agent and then developed in MIBK/IPA 1/3 for 30 s to remove the resist from the exposed area.

Table 2. 1 Etching parameters.

Step	Cl_2 flow (sccm)	Ar flow (sccm)	Magnetic Field (Gauss)	Power (W)	Pressure (mTorr)	Time (s)
1) Stabilize	20	10	70	0	100	10
2) Etch	20	10	70	170	100	110
3) Ramp down	0	60	0	50	0	10

2.2.3 Metallization and annealing process

Prior to the Ohmic contact deposition, the native oxide was removed by dipping the sample in HCl:H_2O (1:4) solution for 2 minutes. The NEXDEP electron-beam evaporator was used for the metal deposition. The metal stack of Ti/Al/Ni/Au (200Å/1400Å/550Å/450Å) was deposited under the base pressure of 9×10^{-6} Torr. This step was followed by the lift-off in the acetone using ultrasonic bath and rapid thermal annealing (RTA) at 830°C for 30 sec using JetFirst 200 to form the alloyed Ohmic contact to the 2DEG.

Followed by the third step of EBL, which is registration of gate contacts, NEXDEP electron-beam evaporator was used for depositing the Schottky metal stack of Ni/Au (200Å/200Å) for the gate contact. Finally, a standard lift-off process in acetone using ultrasonic bath was performed to remove the resist.

2.2.4 Optical lithography

Since the required size of the pads are larger than the maximum writing field of SEM, optical lithography is used for this step. EVG620 mask aligner was used to align the optical mask of the pads with the previously generated patterns and image-reversal lithography using AZ5214

(and developer AZ726) was implemented. The metal stack of Ni/Au (200Å/500Å) was used for the pads using NEXDEP electron-beam evaporator.

SÜSS MicroTec PM5 probing station and Keithley 4200-SCS semiconductor characterization system provided by Concordia University nano-devices lab, was used for on-chip characterization of the fabricated AlGaN/GaN HFETs.

2.3 Results and discussion

On the basis of the research presented in [39] on the role of sidewall surface states in engineering the 2DEG among AlGaN/GaN HFETs, in this work I have conservatively approached the exploration of the role they can play in improving the off-state breakdown voltage of these transistors. To this end, I have investigated the electrical characteristics of HFETs with three different isolation feature geometries, including conventional mesa, non-slanted fin, and slanted fin (Figure 2. 1). Whereas in the slanted fin structure, the tapering angle and the position from which the sidewall tapering starts seem to be parameters worthy of proper selection, as indicated in the inset of Figure 2. 1 (c), in the present study I have quite arbitrarily taken these values as 15° and 2 μm away from the drain-edge of the gate, respectively. Since in this stage of the study, the primary target was the evaluation of the relevance of surface states as a non-physical field-plate to improving the off-state breakdown characteristics, and, by the same token, to a lesser extent assessing the degree of improvement in device linearity, I did not entertain the idea of tapering the fins also on the source side of the channel.

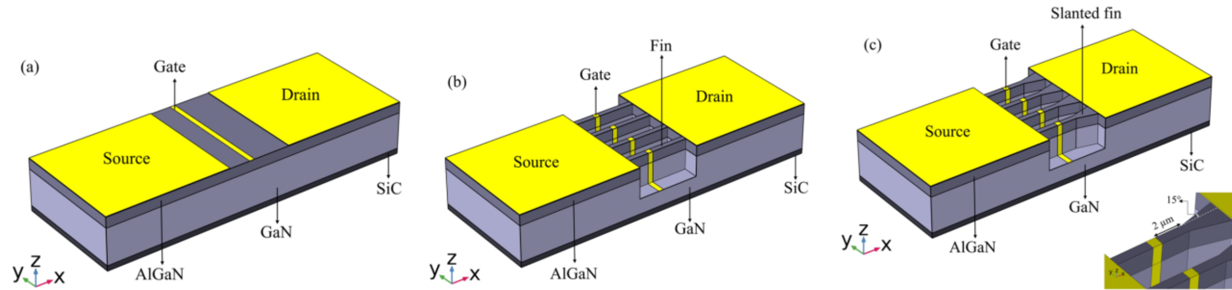

Figure 2. 1 3-D schematic illustration of the transistors built on (a) conventional mesa, (b) non-slanted fin, and (c) slanted fin, inset: close-up around a slanted fin indicating the tapering angle and the position from which the sidewall tapering starts.

2.3.1 Experimental results

In proving the concept of surface states as a non-physical field-plate, in the present study I have adopted dimensions that are relatively conservative (i.e., I have neither aggressively minimized the isolation feature width nor the gate length). Among the fabricated transistors, the width of the channel is respectively 44 µm and 0.8 µm in the conventional mesa and in the gated region of each fin of the non-slanted/slanted fin HFETs. As indicated in Figure 2. 1 (c), in slanted isolation features fin is tapered 2 µm away from the drain edge of the gate towards the drain where its width reaches 2.4 µm. In the HFETs of the fin-type (either slanted or non-slanted) there are 10 fins with a separation of 4 µm from one another in the gated-part of the fins. All of the fabricated devices have L_G (gate length) of 1 µm, L_{GS} of 3 µm, and L_{GD} of 5 µm.

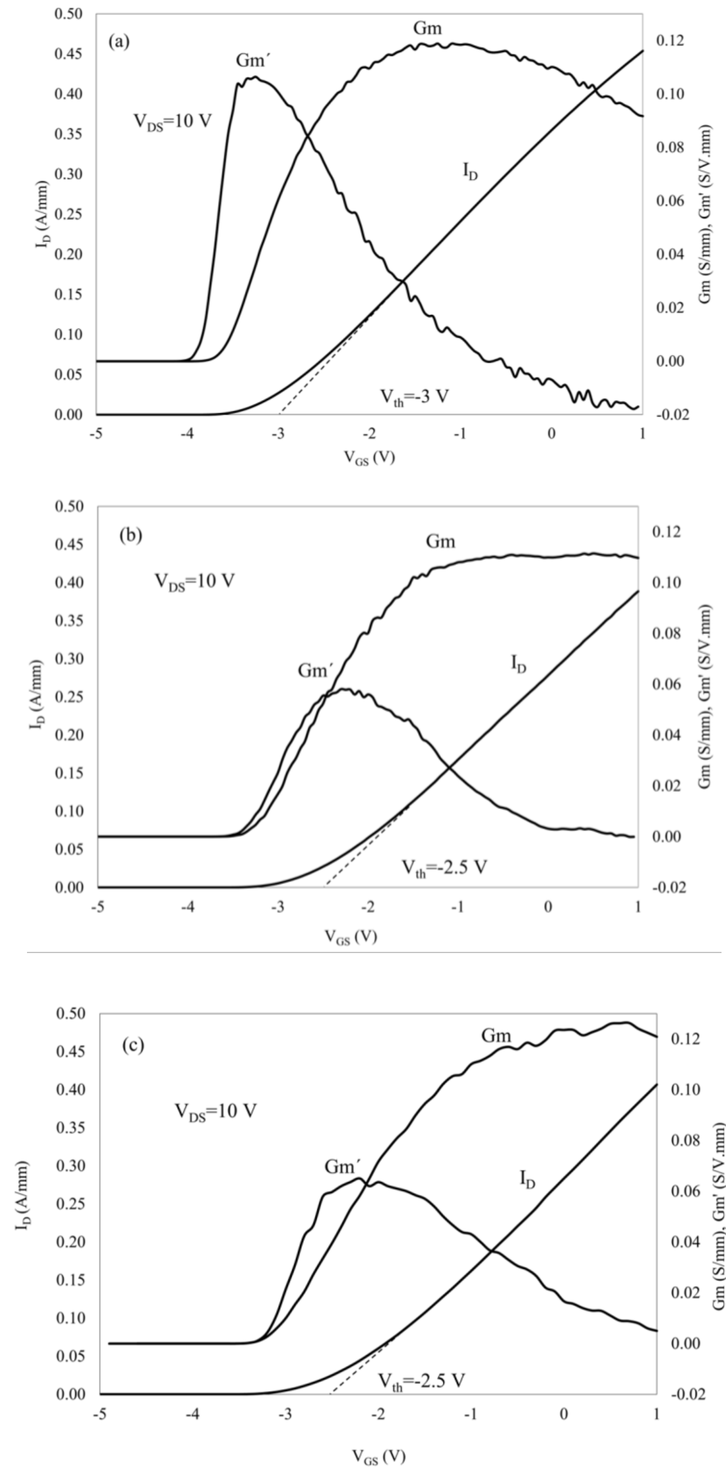

Figure 2. 2 Normalized transfer characteristics and variation of gate transconductance (G_m) and its first derivative versus V_{GS} for (a) conventional mesa, (b) non-slanted fin and (c) slanted fin HFETs.

Consistently observed (i.e. among 4 identical HFETs) normalized gate transconductance and transfer characteristics of the HFETs with isolation features depicted in Figure 2. 1, are presented in Figure 2. 2. The threshold voltage is -3 V, -2.5 V, and -2.5 V for the conventional mesa, non-slanted fin, and slanted fin HFETs, respectively. The less negative threshold voltage of the two fin varieties, which have the same fin width in the gated area, shows that a better electrostatic control is offered over the intrinsic gated channel of HFETs realized on fins of smaller widths. Probable causes of the positive shift at mesas of smaller widths are the triple-gate effect [57], peel force development (hence, strain minimization) [62], and the presence of surface states at the sidewall facets, which is believed to be the dominant mechanism for this positive shifting [39]. In [39] where the variation of threshold voltage with geometry is investigated, it has been shown that for isolation feature geometries that provide sidewalls of very close proximity to the center of the channel in the gated area, even in absence of sidewall covering gate electrodes, due to fermi level pinning of the sidewalls the experimentally observed positive shift in the threshold voltage of AlGaN/GaN HFETs can be replicated.

In Figure 2. 2, it is also observed that in fin-type devices, although to different degrees, the peak of the extrinsic gate transconductance (G_m) is broader and its first derivative versus gate-source voltage (V_{GS}) (i.e., G_m') is smaller in comparison with the conventional mesa HFET, which is an indication of better device linearity of the explored fin isolation feature geometries. This could be owing to the role played by the sidewall gating in reducing the possibility of leaking the 2DEG wave function to the low-mobility AlGaN barrier at less negative V_{GS} values and the effect of the higher resistance of the source access region in serving as a negative feedback loop (essentially leading to improved device linearity in common source measurement configuration). The same role played by the larger source access resistance of the fin type devices, as expected

causes a degradation in the extrinsic gate transconductance at V_{GS} values where the G_m of the mesa type device shows a peak. At this point in the analysis, I leave the description of the possible causes for the observed differences among the G_m-V_{GS} characteristics of the two fin-type devices for a more appropriate place towards the end of this section.

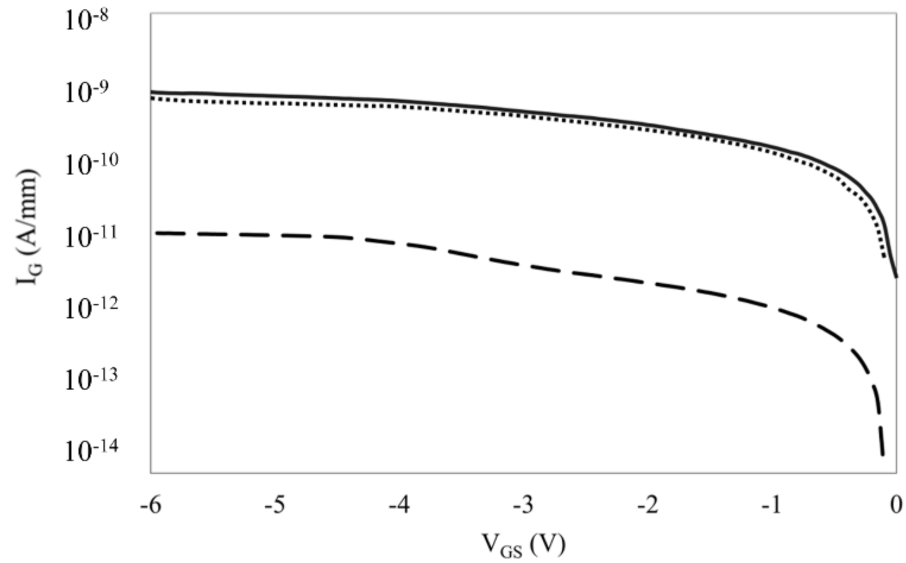

Figure 2. 3 Log-scale normalized gate current versus gate-source voltage of the conventional mesa (dashed line), non-slanted fin (solid line), and slanted fin HFET (dotted line) at V_{DS} = 0 V.

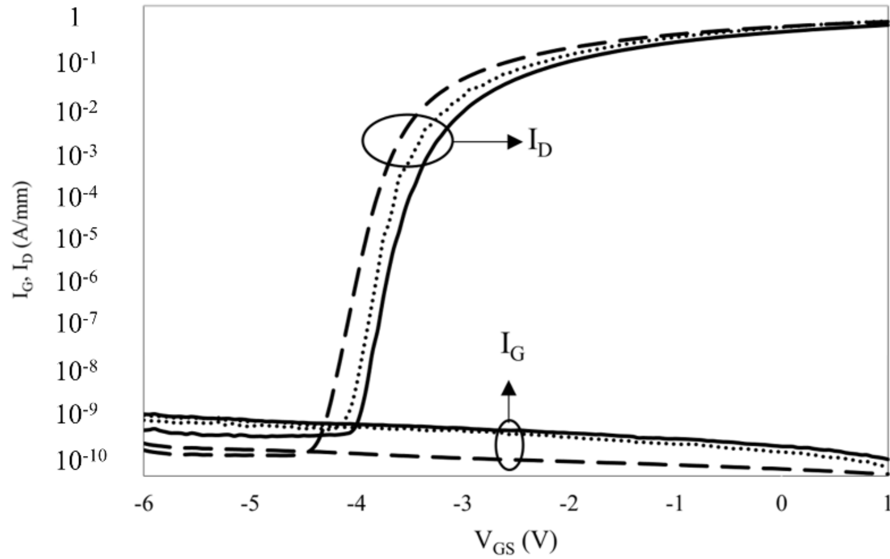

Figure 2. 4 Log-scale normalized drain current and gate current versus gate-source voltage of the conventional mesa (dashed line), non-slanted fin (solid line), and slanted fin HFET (dotted line) at V_{DS} = 10 V.

As shown in Figure 2. 3, while all devices demonstrating a low level of normalized gate leakage, the gate leakage is higher in the fin-type devices in comparison with the mesa type device. This is in agreement with the observations of [63] and chapter 4, which attribute this to the sidewall leakage. The subthreshold characteristics is presented in Figure 2. 4. As shown in this figure, the subthreshold swing (SS) is 80 mV/dec for the slanted and non-slanted fin structures, and 100 mV/dec for the conventional mesa device. The better SS value of the fin-type devices is due to the better channel controllability of these structures. The I_{on}/I_{off} ratio is about 1.7×10^9, 3.8×10^8 and 2.3×10^8 for the conventional mesa, non-slanted fin, and the slanted fin HFETs, respectively. This figure also shows that at higher values of V_{DS}, not unlike the observations made in Figure 2. 3, the amount of gate leakage is higher in slanted and non-slanted fin HFETs compared to the conventional mesa HFET. This can explain the small degradation of the I_{on}/I_{off} ratio among fin-type devices.

As illustrated in Figure 2. 1-Figure 2. 4, among the explored fin-type devices, since they are of identical geometry in the gated part of the fin, the device characteristics such as gate-leakage and threshold voltage, which are rooted in the gated part of the channel, are virtually same.

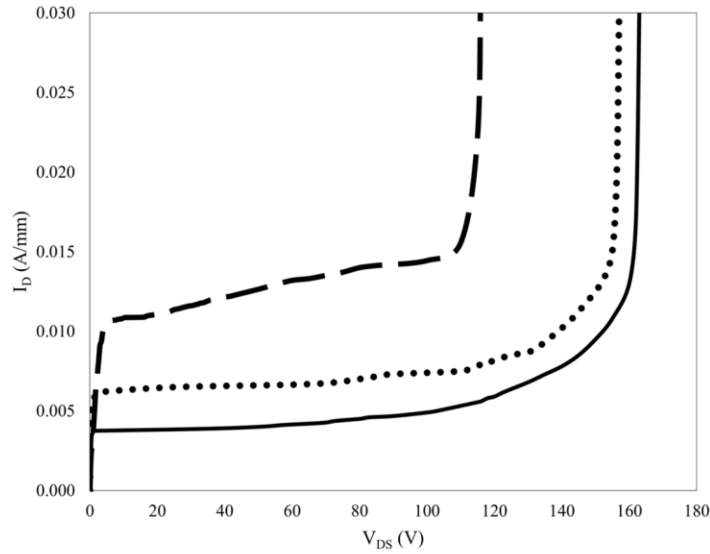

Figure 2. 5 I_D-V_{DS} at $V_{GS,Eff}$ = -0.5 V of the conventional mesa (dashed line), non-slanted fin (solid line), and slanted fin (dotted line) HFETs.

Appreciating the difference among the threshold voltages of the different explored device types, in order to investigate the effect of isolation feature geometry and sidewall surface states on the off-state breakdown characteristics, drain current-voltage (I_D-V_{DS}) characteristics of the conventional mesa, non-slanted fin, and slanted fin HFETs are explored at $V_{GS,Eff}$= - 0.5 V (Figure 2. 5), where $V_{GS,Eff}$ is defined as V_{GS} - V_{th}. Here I have defined breakdown voltage as the drain voltage at which the onset of an exponential increase in the drain current occurs. Based on this definition, as indicated on Figure 2. 5, the off-state breakdown voltage is 116 V, 163 V, and 157 V for the conventional mesa, non-slanted fin, and slanted fin HFETs, respectively. In these measurements, the devices were observed to undergo avalanche destructive breakdown. Providing evidence for channel and not barrier breakdown, during the measurements no exponential increase

in I_G and physical damage to the gate electrode was noted. The choice of the value of $V_{GS,Eff}$ was made due to the authors' limited measurement capacity to a maximum of 200 V. Biasing the gate further below the threshold voltage has been observed to boost the breakdown voltage to values beyond this measurement capacity. This is probably due to scarceness of electrons in the depleted channel, which is a requirement of impact ionization to inflict avalanche breakdown.

Following an earlier work of the group [39], I speculate that the substantial enhancement of the breakdown voltage obtained by mere shrinking of the mesa width from tens of micrometers (in the conventional mesa) to sub-micrometer (in the fin isolation feature) has its roots in the depleting effect of the negatively charged surface states at the sidewalls, which becomes more dominant when the distance between the isolation feature sidewalls is smaller. Accordingly, I speculate that when the width of the mesa is reduced, due to the increase of the resistance imposed on the drain access region of the transistor, the drain induced electric field along the channel is redistributed in a form that the peak of the electric field at the drain-edge of the gate, which is responsible for the channel breakdown, is substantially reduced at a given drain-source voltage. Therefore, by minimizing the width of the isolation feature for the same vertical device structure and overall lateral dimensions, it will be a higher drain voltage that triggers the impact ionization process.

Since the explored Ga-face Wurtzite AlGaN/GaN epilayer is a polar material in which the high concentration 2DEG yields a very small sheet resistance, if not for the pinning at the sidewalls and partial channel depletion due to that, for increasing the resistance of the drain access region to arrive at the same goal, I will be needing to reduce the width of the isolation feature in these parts of the channel very aggressively (probably down to just a few nanometers).

It is worthwhile indicating that the respective 40% and 35% enhancement of the breakdown voltage quite consistently observed and reported in Figure 2. 5 for the non-slanted and the slanted

fin HFETs are achieved without incorporation of any field-plate and the associated addition to the gate capacitance and fabrication complexity. Evidently, the sidewall gating in the fin isolation features produces a larger gate capacitance. However, owing to the major advantages of this topology, this additional gate capacitance is a price that has been already afforded in realizing AlGaN/GaN HFETs [57]. What the presented results are showing is that further addition to this capacitance by incorporating 3-D field-plates in the drain access region can be avoided.

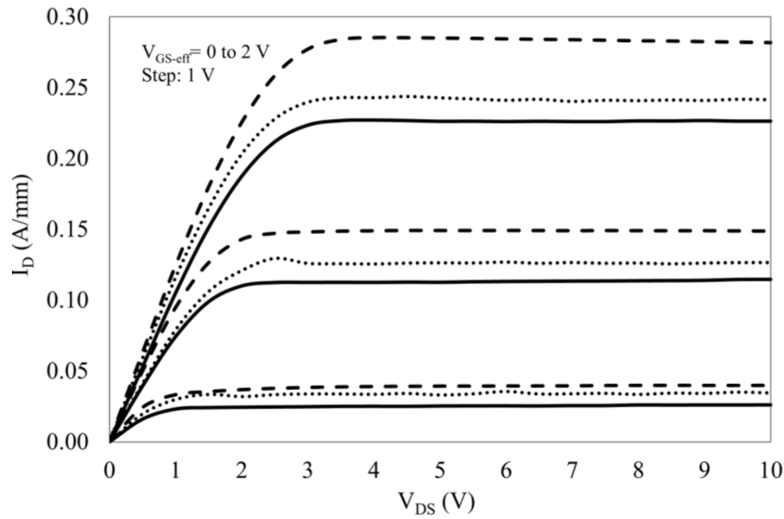

Figure 2. 6 Normalized, output characteristics of the conventional mesa (dashed line), non-slanted fin (solid line), and slanted fin (dotted line) HFETs.

Since power devices require simultaneous superior breakdown voltage and output current, I have investigated the on-state characteristics of the HFETs with the aforementioned isolation feature geometries. Based on Figure 2. 6, the on-resistance at $V_{GS,Eff}$ = 2 V is 8 Ω-mm, 9.6 Ω-mm and 8.5 Ω-mm for the conventional mesa, non-slanted fin, and slanted fin HFETs, respectively. I speculate that the smaller value of the on-state resistance among the HFETs with slanted fins compared to those of non-slanted fins has roots in the tapered structure and the less pronounced effect of negatively charged sidewall surface states in depleting the channel where there is further separation between the sidewalls of the fin towards the drain end of the channel of a slanted fin.

This speculation is compatible with the one made earlier on the topic of the observed improvement to the off-state breakdown voltage.

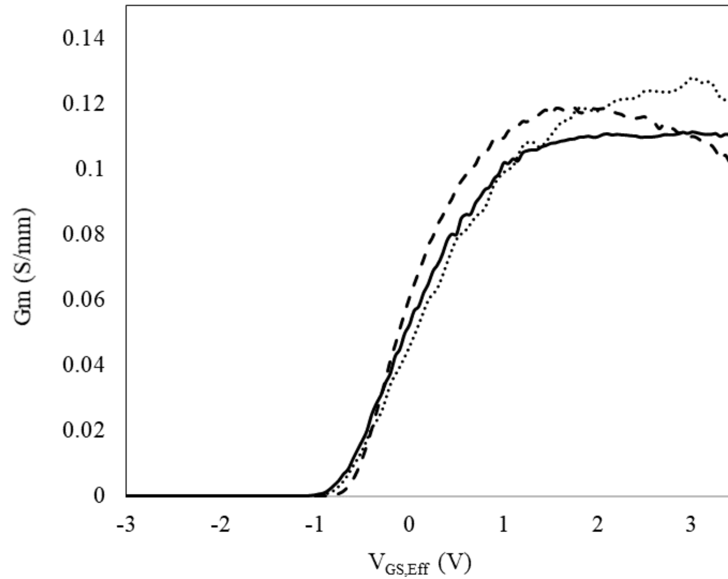

Figure 2. 7 Normalized gate transconductance (G_m) versus $V_{GS,Eff}$ for conventional mesa (dashed line), non-slanted fin (solid line), and slanted fin (dotted line) HFETs at V_{DS}=10 V.

Based on these observations, I can now revisit the data presented in Figure 2. 2. Figure 2. 7 depicts the transconductance content of the three panels of Figure 2. 2 superimposed on each other, while to present a more convenient basis of comparison between the three normalized G_m-V_{GS} characteristics, the horizontal axis instead of V_{GS} has been changed to the effective gate-source voltage. For the two fin type devices, what I am observing is that up until $V_{GS,Eff}$ of about +1 V, the two devices virtually follow the same characteristics. However, as for higher values of $V_{GS,Eff}$ and essentially I_D, the gate transconductance of the slanted fin variety surpasses that of the other. As for this observation, in this chapter whose focus is not on the gate transconductance but the breakdown characteristics, I can only speculate that a possible reason for this observation can be found in the explanation linked to drain-induced barrier lowering phenomenon (known as DIBL).

Accordingly, for a given V_{DS}, the higher the I_D, a relatively larger part of V_{DS} is dropped across the drain-access resistance of a transistor that has a higher value of this resistance (i.e. for the non-slanted fin). Hence, for the slanted variety (where the drain-access region resistance is smaller), the drain-induced channel potential will be higher, and so is the chance for lowering the barrier between the source-access region and the channel. The difference in the amount of lowering of the barrier, which is expected to be more pronounced at higher $V_{GS,Eff}$, can be expected to cause an easier population of the channel and improved transconductance in the device that has been relatively more exposed to DIBL. So, while some DIBL seems to be present at a high enough V_{DS} among both devices, I speculate that the slanted fin-type due to the aforementioned reason would have more of its presence felt at higher values of I_D.

Since one of the possible applications of the non-physical FP concept that is being explored here is power electronics, in order to quantitatively assess the output power performance, I have investigated the Baliga's figure of merit (BFOM) [41] :

$$BFOM = BV_{off}^{2} / R_{on}, \tag{2.1}$$

where R_{on} (Ω.cm^2) is the specific on-resistance.

Using Eq. (2.1), BFOM among a number of identical devices is consistently calculated as 33 MW/cm^2, 55 MW/cm^2, and 58 MW/cm^2 for the conventional mesa, non-slanted fin, and the slanted fin HFETs, respectively. Thus, HFETs with the slanted fin isolation feature geometry can offer better characteristics in terms of output power performance. Having said that, it must be appreciated that there are pros and cons to every new alternative technology. When AlGaN/GaN HFETs are made on array of fins instead of a wide mesa isolation geometry, the normalized current is going to suffer. Without changing the epilayer in the case of power transistors, overcoming the problem of lowered current-drive when current density is deteriorated would mean using larger

arrays of fins between the drain and source (and incurring the cost of larger chip size). But not all is negative, since such a problem can be addressed by implementing the proposed idea instead of on a single channel epilayer on a multi-channel epilayer structure [64].

Whereas the reported fabrication technology purposefully did not take advantage of any of the surface passivation techniques popular among III-Nitride HFETs, the studied devices did not show any sign of gate-lag, shifting of the threshold voltage, and frequency dispersion in gate-transconductance and output resistance both before and after the indicated tests. While the measurements were all performed under room light (hence with no substantial UV exposure), lack of these observations indicate the absence of dominant trapping/de-trapping processes at the exposed surfaces. This observation corroborates the deep nature of the abovementioned sidewall surface states, and consistent fermi level pinning at those states.

It should be noted that the presented experimental data here, is based on the average value of the measured transfer and output characteristics of 4 identical HFETs of each type and the maximum variation from the average is 4%.

2.3.2 Simulation results

To substantiate the speculations presented in the previous section, I have conducted device simulations employing COMSOL Multiphysics [65] to calculate the electric field responsible for the channel breakdown (i.e. in order to investigate the effect of sidewall surface states and suitability of isolation feature geometry on improving the off-state breakdown voltage). The layer structure of the simulated HFETs consists of 25 nm thick $Al_{0.25}Ga_{0.75}N$ barrier layer with UID donor concentration of 10^{15} cm^{-3}, 50 nm thick GaN channel layer with UID donor concentration of 10^{14} cm^{-3}, and 150 nm GaN buffer layer with acceptor concentration of 5×10^{16} cm^{-3}. The three isolation feature geometries that I have simulated (shown in Figure 2. 8) include two relatively narrow non-slanted fins with widths (W) of 100 nm and 50 nm, and a slanted fin with width of 50

nm extending from the source contact through the gated channel which tapers to 100 nm at the drain end of channel. For the three simulated device categories L_G=0.7 µm, L_{GS}=0.7 µm, and L_{GD}=2 µm. The choice of much smaller lateral and vertical dimensions of the simulated devices compared to the fabricated HFETs is due to the long computation time of the required 3D simulations.

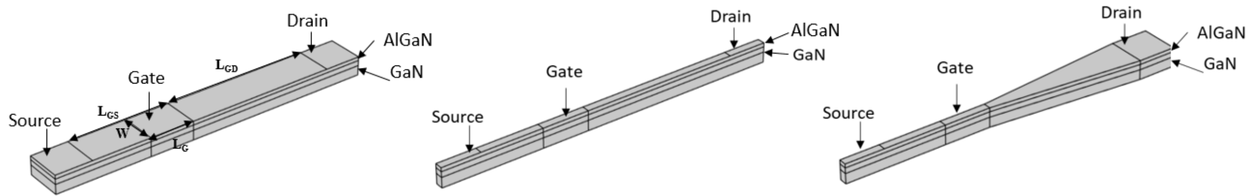

Figure 2. 8 3-D schematic illustration of the simulated devices (a) 100 nm-wide fin, (b) 50 nm-wide fin, and (c) slanted fin.

According to the literature, at non-polar facets of GaN due to the presence of acceptor sidewall surface states, the fermi level is pinned 0.6 eV below the conduction band edge [38], [66]. The density of the sidewall surface states that causes fermi level pinning at this level is $>10^{13}$ cm^{-2}. However, incorporation of this high density of surface states requires an ultra-fine mesh which due to 3D nature of our simulations renders the computations long and inhibiting. Therefore, I have assumed a smaller value of 2×10^{12} cm^{-2} (in all simulations unless otherwise stated), which produces the onset of pinning at AlGaN/GaN HFET sidewalls. A surface charge density of 0.028 C/m^2 was added to the AlGaN and GaN interface to induce a 2DEG concentration of 1.15×10^{13} cm^{-2} to the channel of the $Al_{0.25}Ga_{0.75}N$/GaN heterostructure [67].

In the simulations, I have assumed source and drain contacts as ideally Ohmic and the gate as a Schottky contact with metal work function of 5.2 eV. The transport characteristics that I have implemented in our simulations is based on the drift-diffusion formalism in which I have adopted

the field-dependent electron mobility ($\mu_n(E)$) using Caughey and Thomas model [68] represented by Eq. (2.2):

$$\mu_n(E) = \frac{\mu_{n,low}}{(1+\frac{\mu_{n,low}\times|E_x|}{v_{n,sat}})}, \quad (2.2)$$

where $\mu_{n,low}$ is the low-field electron mobility, E_x is the longitudinal electric field, and $v_{n,sat}$ is the electron saturation velocity. The relevance of consideration of the well-known peak of electron velocity and also presence of inflection points in the steady-state drift transport characteristics of AlGaN/GaN channel in modeling these HFETs has been already investigated [69],[70],[71]. Whereas for short-channel and short-gate HFETs, enjoying very small drain and source contact resistances, such an undertaking has been reported to have tangible impacts, considering the conservative dimensions of the experimentally and theoretically explored transistors, overlooking these effects and adopting the Caughey and Thomas field-dependent mobility model is deemed reasonable. Device parameters used in the simulations are summarized in Table 2. 2 [72].

To study the breakdown behavior, I have incorporated the effect of impact ionization using the following equations:

$$\alpha = 4.48\times 10^8 exp\left(-\frac{3.39\times 10^7}{|E_x|}\right), \quad (2.3)$$

$$\beta = 7.13\times 10^6 exp(-\frac{1.46\times 10^7}{|E_x|}), \quad (2.4)$$

in which α represents the electron and β represents the hole ionization rates [73].

Table 2. 2 Material properties of $Al_{0.25}Ga_{0.75}N$ and GaN used in simulations.

Parameter	Value ($Al_{0.25}Ga_{0.75}N$)	Value (GaN)
Static relative permittivity (ε_r)	8.8	8.9
Bandgap (E_g)	3.9 (eV)	3.39 (eV)
Electron affinity (χ_0)	3.2 (eV)	4.1 (eV)
Effective density of states, Valance band (N_{V0})	4.6×10^{19} ($\mathrm{cm^{-3}}$)	4.6×10^{19} ($\mathrm{cm^{-3}}$)
Effective density of states, Conduction band (N_{C0})	2.3×10^{18} ($\mathrm{cm^{-3}}$)	2.3×10^{18} ($\mathrm{cm^{-3}}$)
Electron mobility ($\mu_{n,low}$)	10 ($\mathrm{cm^2V^{-1}}s^{-1}$)	1000 ($\mathrm{cm^2V^{-1}}s^{-1}$)
Hole mobility ($\mu_{p,low}$)	5 ($\mathrm{cm^2V^{-1}}s^{-1}$)	200 ($\mathrm{cm^2V^{-1}}s$)
Electron saturation velocity ($v_{n,sat}$)	1.1×10^7 (cm/s)	1.5×10^7 (cm/s)

Figure 2. 9 shows that the breakdown voltage is 74 V, 90 V, 114 V, and 103 V for the 50 nm-wide fin with no sidewall surface states, 100 nm-wide fin, 50 nm-wide fin, and the slanted fin HFETs, respectively, where for the last three cases acceptor sidewall surface states are assumed. While in simulations the density of surface states that I assumed (which is 2×10^{12} $\mathrm{cm^{-2}}$) is almost one order of magnitude less than the actual value at non-polar facets of AlGaN/GaN HFETs (which is $>10^{13}$ $\mathrm{cm^{-2}}$), the breakdown voltages of simulated HFETs are in the same range as those of the fabricated ones. This is because the width of the fin of the simulated devices is much smaller than that of the fabricated HFETs. Therefore, the effect that a smaller density of surface state can have on the breakdown voltage of an HFET with narrow fins is similar to the effect that a higher density of surface states can have on the breakdown voltage of an HFET with wider fins. Based on these results, the breakdown voltage of the 50 nm-wide fin HFET improves by 35% compared to the

same device but with the assumption of no pinning. Among the above-referenced observations, the low breakdown voltage of the HFET with 50 nm-wide fin for which case no pinning was considered, demonstrates that the observation of the improvement in breakdown voltage cannot be seen in association with the triple gating effect of the fin structure. Since in the simulations I was not bound to the aforementioned measurement capacity limitation, they were run at a variety of gate biases where the same conclusion was made. As a representative set, for $V_{GS,Eff}$ = -1 V, Figure 2. 9 illustrates the breakdown characteristics of the numerically explored transistors.

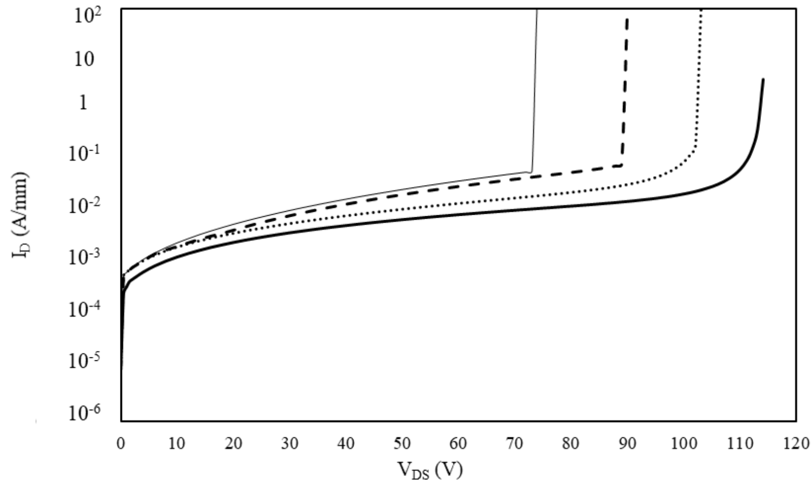

Figure 2. 9 Normalized I_D-V_{DS} at $V_{GS,Eff}$ = -1 V of the 50 nm fin with no sidewall surface states (thin solid line), 100 nm fin (dashed line), 50 nm fin (thick solid line), and slanted fin (dotted line) HFETs, where for the last three cases acceptor sidewall surface states are assumed.

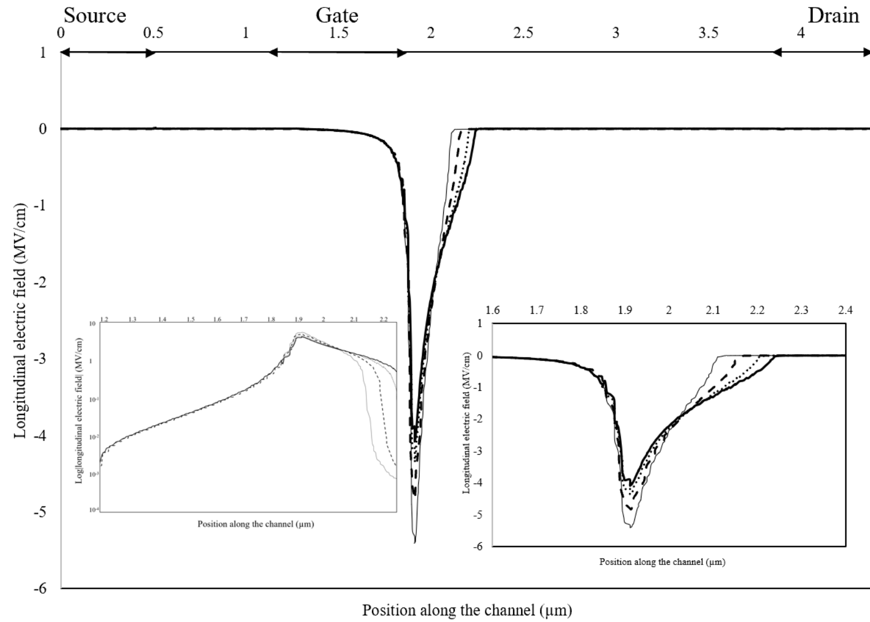

Figure 2. 10 Electric field profile of the 50 nm fin with no sidewall surface states (thin solid line), 100 nm fin (dashed line), non-slanted fin (thick solid line), and slanted fin (dotted line) HEFTs along the channel and 1 nm below the heterointerface at V_{DS}=74 V, where for the last three cases acceptor sidewall surface states are assumed. Left inset: Log-scale around the gate electrode. Right inset: close-up around the gate electrode.

As shown in Figure 2. 10 at V_{DS} of 74 V (i.e., the breakdown voltage of the 50 nm-wide fin with no sidewall surface states) the peak of the electric field, which is located at the drain-edge of the gate, is 5.4 MV/cm while it is 4.8 MV/cm, 4 MV/cm, and 4.3 MV/cm for the 100 nm-wide fin, 50 nm-wide fin, and the slanted fin HFETs, respectively (where for the last three cases acceptor sidewall surface states are assumed). Furthermore, it is demonstrated that the electric field profile is more distributed towards the drain in fins of narrower widths. These observations clearly show that the electric field peak is reduced by shrinking the width of the fins when the presence of acceptor surface states is assumed on the sidewalls. This is because in narrower fins which benefit

more from the depleting effect of the negatively charged sidewall surface states, a more resistive path is imposed on the drain access region.

2.4 Conclusion

A new approach for enhancing the breakdown voltage of AlGaN/GaN HFETs was presented. Measurements on the HFETs of 3 different isolation feature geometries demonstrate that sidewall surface states can play a significant role on the breakdown characteristics. This effect is more pronounced in devices built on isolation features with smaller widths. Although the non-slanted fin isolation feature geometry takes further advantage of the sidewall surface states in terms of channel depletion, it can fall short of satisfying the high current density in the on-state, which is also a requirement for high power applications. The slanted-fin isolation feature geometry which I presented here, while fulfilling a higher breakdown voltage in comparison to the HFETs of conventional mesa isolation feature geometry, can deliver a current density more than what is acquired from the non-slanted fins of equal dimensions in the gated channel. According to the presented results, the technique of reducing the mesa width for arriving at the very popular and heavily pursued enhancement-mode AlGaN/GaN HFETs has been shown to yield at the same time the possibility of boosting the breakdown voltage if the mesa width is not shrunk just in the gated part of the channel, but also in the drain access region.

Chapter 3

Comparative investigation of the impacts of isolation feature geometry and field-plate as techniques used in improving the off-state breakdown voltage on the frequency response of AlGaN/GaN HFETs

3.1 Introduction

Due to the superb material and device characteristics such as high breakdown voltage, high saturation velocity, low carrier effective mass, high thermal conductivity, and high two-dimensional electron gas (2DEG) density, GaN-based HFETs have emerged as excellent choices for millimeter-wave high-power applications [74]. While even from very early on AlGaN/GaN HFETs have demonstrated excellent power performance at relatively lower frequencies (e.g. 30 W/mm at 4 GHz [75]), despite the growing interest they have continued to show limitations in sub-millimeter wave applications such as satellite, advanced radar, and broadband wireless communication [76]. Due to the often observed trade-off between the high frequency figures of merit such as unity current-gain cutoff frequency (f_T) and the breakdown voltage, thus far simultaneous improvement in BV_{off} and f_T (among other high frequency FOMs) has been found challenging. Accordingly, much research is being conducted to improve among others the

Johnson's figure of merit (JFOM=$f_T \times BV_{off}$), which is a metric for comparing high power microwave devices. Just to name a few records, Johnson *et al.* have reported a JFOM of 3.6 THz.V (=18 GHz $\times$ 200 V) for AlGaN/GaN HFETs on Si substrate [77], Yang *et al.* have realized a high JFOM of 10.4 THz.V (=69 GHz $\times$ 151 V) for T-gate thin barrier AlGaN/GaN HFETs with a TiN-based source ledge [78]. In addition, employing a field-plate Ando *et al.* have achieved a JFOM of 3.2 THz.V (=2 GHz $\times$ 160 V) on SiC substrate [79].

In this chapter, employing COMSOL Multiphysics [65] I have investigated the effect of isolation feature geometry and field-plate on the off-state breakdown voltage and unity current-gain cutoff frequency of the AlGaN/GaN HFETs to compare the JFOM among these devices.

3.2 Physics and material properties used in simulations

Device parameters used in the simulations have been already summarized in Table 2. 2, while the transport and ionization rates have been also presented in section 2.3.2.

The mesh is an important component of any numerical model and as a sign of proper convergence it is always important to ensure that the results do not change significantly when the mesh is refined. In this work, I have adopted a triangular mesh for the top plane and swept this mesh into the depth of the structure. I have noticed that in 3-D simulations this is the proper meshing particularly for the gate region. In order to optimize the mesh its density is increased further only in the vicinity of the important junctions and where the structure is slanted and the electric field variation is sharper.

3.3 Specifications of the simulated devices

Not unlike the device presented in section 2.3.2, the layer structure of the simulated HFETs consists of 25 nm thick $Al_{0.25}Ga_{0.75}N$ barrier layer with UID donor concentration of 10^{15} cm^{-3}, 50

nm thick GaN channel layer with UID donor concentration of 10^{14} cm^{-3}, and 150 nm GaN buffer layer with acceptor concentration of 5×10^{16} cm^{-3}. In all of the present simulations, I have assumed a 2DEG concentration of 1.15×10^{13} cm^{-2} and a negative sidewall charge density of 2×10^{12} cm^{-2}, which as indicated in chapter 2 produces the onset of pinning at AlGaN/GaN HFET sidewalls.

The source and drain contacts are considered to be ideally Ohmic and a metal work function of 5.2 eV is adopted for the Schottky gate contact. In this study, I have explored BV_{off}, gate capacitance (C_g), gate transconductance, and finally JFOM of AlGaN/GaN HFETs with five different isolation feature geometries, including two non-slanted fins that are 50 and 200 nm wide and three slanted fin categories that are 50 nm wide at the source and gate regions and 200 nm wide at the drain side. Among the slanted fin categories, the position at which the tapering of the isolation feature occurs is a varying parameter which with respect to the drain-edge of the gate are adopted to be 0, 0.5 and 1 μm. Among these, the values of L_G, L_{GS} and L_{GD} are 0.6, 0.8 and 2 μm, respectively.

In addition, I have investigated the effect of implementing FPs with different specifications (including length (L_{FP}), thickness (t_{FP}) and relative permittivity (ε_r) of the dielectric material layer under the FP), on the BV_{off} and C_g of the 200 nm-wide non-slanted fin HFET.

In these simulations, I have considered the 3D configuration of the gate and FP and the total calculated gate capacitance is the combination of the 3D gate and FP capacitances. Furthermore, in all simulations the gate length, gate-drain and gate-source spacings are identical while the isolation feature width and FP specifications are varying parameters. Table 3. 1 and Table 3. 2 represent the summarized specifications of the simulated devices.

Table 3. 1 Specifications of the slanted and non-slanted narrow fin HFETs without FP.

Type of HFET	L_G, L_{GD}, L_{GS} (µm)	Gate width (nm)	**Fin width at the drain edge (nm)**	**Tapering position with respect to the drain-edge of the gate (µm)**
Non-slanted narrow fin	0.6, 2, 0.8	50	**50**	**NA**
Slanted fin I	0.6, 2, 0.8	50	**200**	**0**
Slanted fin II	0.6, 2, 0.8	50	**200**	**0.5**
Slanted fin III	0.6, 2, 0.8	50	**200**	**1**

Table 3. 2 Specifications of the wide fin HFETs with and without FP.

Type of HFET	L_G, L_{GD}, L_{GS} (µm)	Gate width (nm)	ε_r	**L_{FP}, t_{FP} (µm)**
Wide fin without FP	0.6, 2, 0.8	200	**NA**	**NA**
Wide fin with FP I	0.6, 2, 0.8	200	**4**	**0.5, 0.1**
Wide fin with FP II	0.6, 2, 0.8	200	**4**	**0.5, 0.05**
Wide fin with FP III	0.6, 2, 0.8	200	**4**	**0.5, 0.2**
Wide fin with FP IV	0.6, 2, 0.8	200	**8**	**0.5, 0.1**
Wide fin with FP V	0.6, 2, 0.8	200	**4**	**1, 0.1**
Wide fin with FP VI	0.6, 2, 0.8	200	**4**	**1.5, 0.1**

3.4 Transfer characteristics

As shown in Figure 3. 1, the threshold voltage and the gate transconductance of the narrow non-slanted fin are -0.3 V and 6.5 µS, respectively. I have also assessed the transfer characteristics of the slanted fin I, II, and III and observed that the value of V_{th} and G_m are the same as the non-slanted fin demonstrated in Figure 3. 1. Figure 3. 2 demonstrates that V_{th} and G_m of the wide fin HFET are -3.2 V and 24 µS, respectively. Note that the wide fin HFETs with FP I, II, III, IV, V and VI have the same V_{th} and G_m values as the wide fin HFET without FP, shown in Figure 3. 2. It is worth mentioning that, the normalized value of the simulated G_m of the wide fin HFET is 120

mS/mm which is the same as the normalized measured value of G_m of the fabricated HFETs presented in chapters 2 and 4.

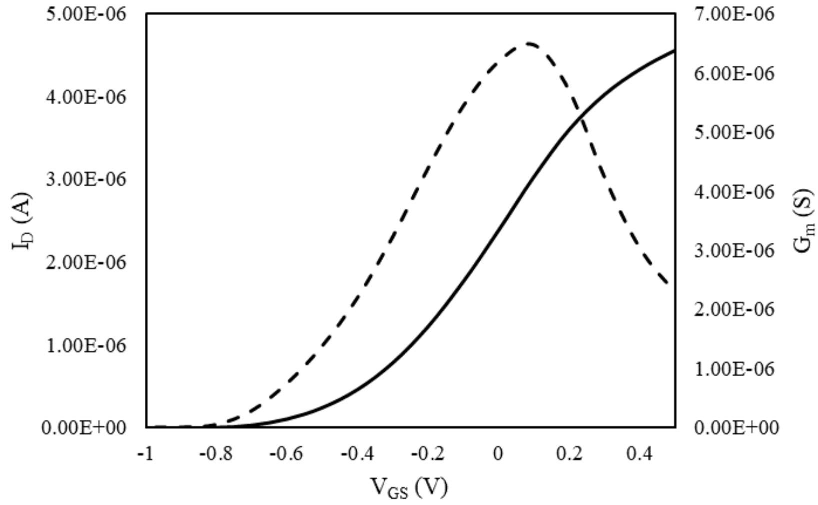

Figure 3. 1 I_D (solid curve) and G_m (dashed curve) versus V_{GS} of the narrow fin HFET.

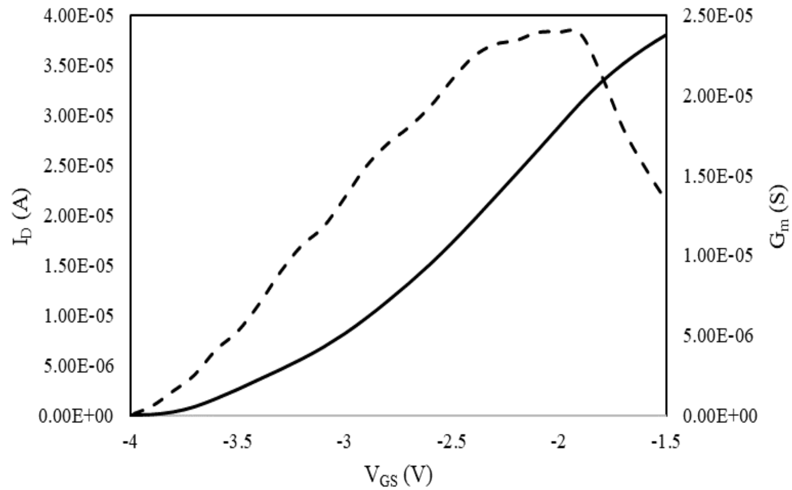

Figure 3. 2 I_D (solid curve) and G_m (dashed curve) versus V_{GS} of the wide fin HFET.

The positive 2.9 V shift of the threshold voltage observed between Figure 3. 1 and Figure 3. 2 is due to the triple gate and the depleting effect of the negatively charged sidewall surface states.

3.5 Off-state I_D-V_{DS} and electric field profile

In order to compare the effect of isolation feature geometry and FP on BV_{off} of the AlGaN/GaN HFETs, as summarized in Table 3. 1 and Table 3. 2, I have simulated the I_D versus V_{DS} characteristics of the non-slanted fin HFETs of two different widths, slanted fin HFETs of three different tapering angles, and non-slanted wide fin HFETs with six different FP specifications at $V_{GS\text{-}Eff}$ of -0.5 V. It is worth mentioning that while I have adopted three values of L_{FP}, three values of t_{FP} and two values of ε_r, instead of simulating eighteen (i.e. $3 \times 3 \times 2$) HFETs with different FP specifications, I have simulated only six combinations of these variables. The reason behind this selection is explained further below in section 3.5.2.

3.5.1 Effect of isolation feature geometry on the off-state breakdown voltage

As demonstrated in Figure 3. 3-Figure 3. 6, following the definition of the off-state breakdown voltage presented in chapter 2, BV_{off} is 101 V, 69 V, 100 V, and 100 V for the non-slanted narrow fin, slanted fin I, II, and III, respectively. This observation shows that the breakdown voltage of the slanted fin HFETs increase by shifting the tapering point from the drain-edge of the gate to a further distance toward the drain. As shown in Figure 3. 5, the breakdown voltage of the slanted fin HFET whose tapering position is 0.5 μm away from the drain-edge of the gate approaches that of the non-slanted narrow fin HFET with the same gate width. As demonstrated in Figure 3. 6, there is no more improvement in BV_{off} by further shifting this point toward the drain.

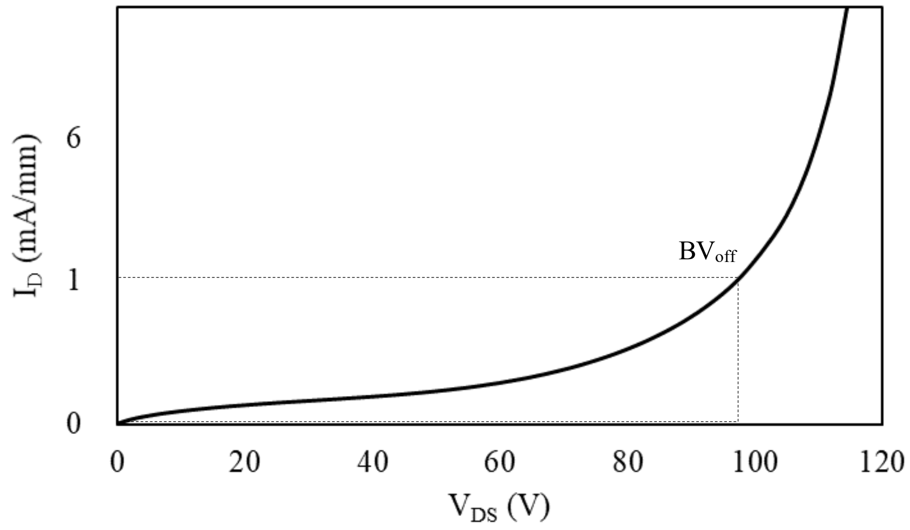

Figure 3. 3 Log-scale I_D-V_{DS} at $V_{GS\text{-}Eff}$=-0.5 V of the non-slanted narrow fin HFET.

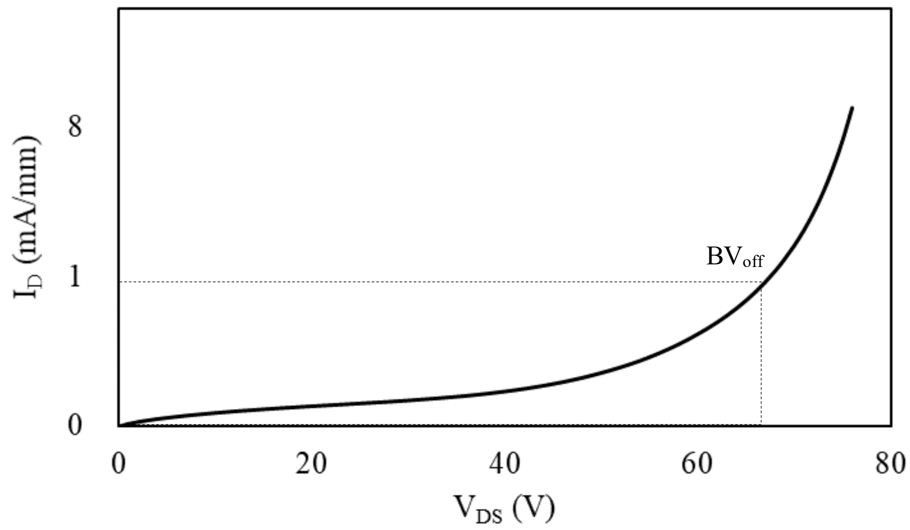

Figure 3. 4 Log-scale I_D-V_{DS} at $V_{GS\text{-}Eff}$=-0.5 V of the slanted fin I HFET.

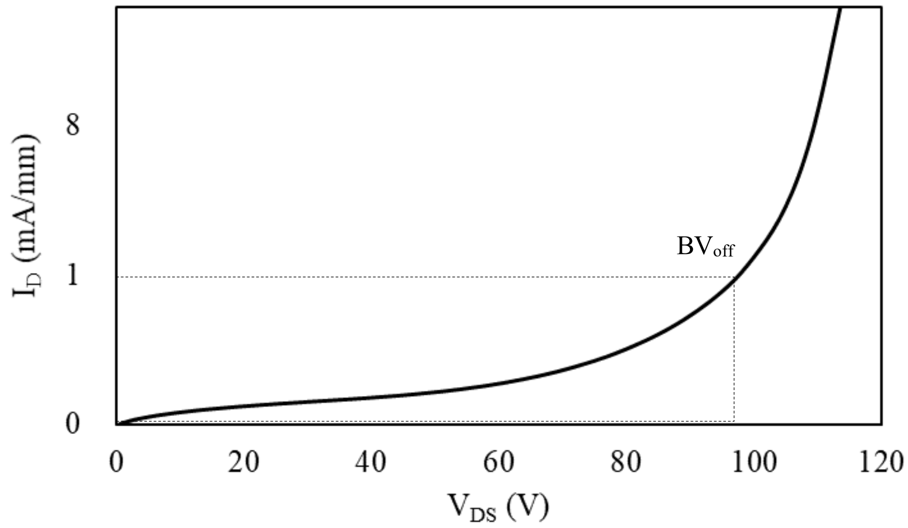

Figure 3. 5 Log-scale I_D-V_{DS} at $V_{GS\text{-}Eff}$=-0.5 V of the slanted fin II HFET.

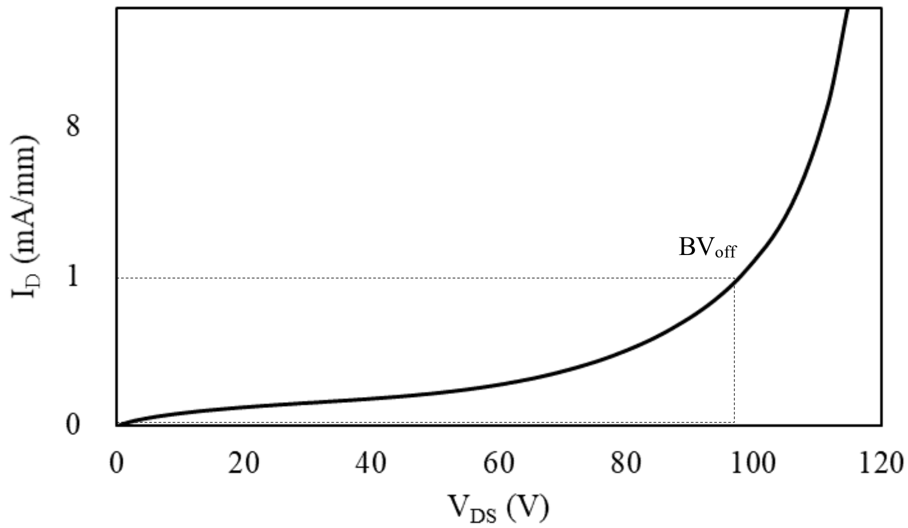

Figure 3. 6 Log-scale I_D-V_{DS} at $V_{GS\text{-}Eff}$=-0.5 V of the slanted fin III HFET.

Supporting the observations of chapter 2, as demonstrated in Figure 3. 7 the breakdown voltage of the wide fin HFET is 52 V which is almost 48% smaller than the narrow fin HFET. This indicates that, due to the larger separation of the sidewalls, in the HFET with the wider isolation

feature negatively charged sidewall surface states do not deplete the channel as effectively as in the narrower counterpart thus, its breakdown voltage is smaller.

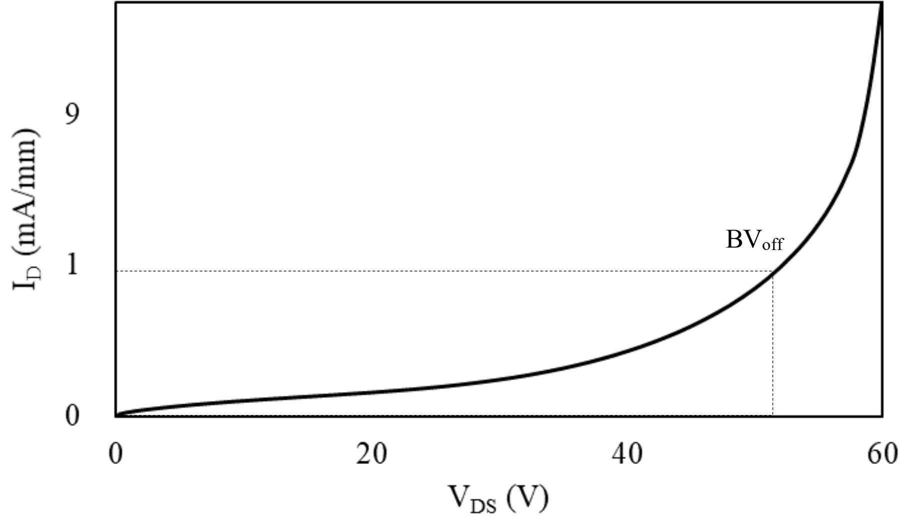

Figure 3. 7 Log-scale I_D-V_{DS} at $V_{GS\text{-}Eff}$=-0.5 V of the wide fin HFET without FP.

3.5.2 Effect of field-plate on the off-state breakdown voltage

In this section, I have investigated the effect of FP on the BV_{off} of the HFET with the wider isolation feature. As mentioned earlier, in this evaluation I have considered three FP variable parameters including length, dielectric permittivity and thickness. In order to minimize the number of simulations, where the basis of optimization is provided in the rest of the discussion, I have first optimized the thickness and permittivity of the dielectric material which is used under the field-plate. Accordingly, I have assessed the effect of L_{FP} on BV_{off} while the optimized values of t_{FP} and ε_r are selected.

3.5.2.1 Effect of t_{FP} on BV_{off}

As shown in Figure 3. 8, BV_{off} of the wide fin HFET with FP I (in which L_{FP}, t_{FP} and ε_r are respectively, 0.5 μm, 0.1 μm and 4) is 190 V, which is a 265% improvement in BV_{off} compared to

the same device with no FP (Figure 3. 7). This indicates that while BV_{off} is 48% increased by just shrinking of the isolation feature width from 200 nm to 50 nm, FP implementation can enhance BV_{off} more effectively.

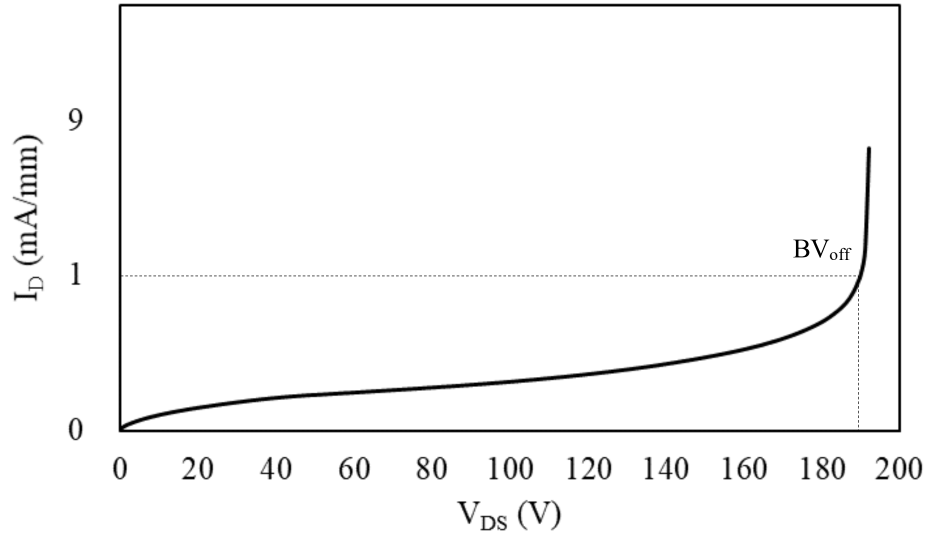

Figure 3. 8 Log-scale I_D-V_{DS} at $V_{GS\text{-}Eff}$=-0.5 V of the wide fin HFET with FP I.

In order to investigate the effect of t_{FP} on BV_{off} I have evaluated the off-state I_D-V_{DS} characteristics of three HFETs with identical L_{FP} and ε_r (i.e. 0.5 µm and 4) but different dielectric material layer thicknesses. As shown in Figure 3. 9 and Figure 3. 10, BV_{off} is 21% and 53% reduced when t_{FP} is reduced from 0.1 µm to 0.05 µm and increased from 0.1 µm to 0.2 µm, respectively. These results indicate that there is an optimum value for the t_{FP} at which the maximum value of the BV_{off} can be achieved. In order to identify the origin of this behavior, I have investigated the profile of the longitudinal electric field (E_x) along the channel which is responsible for the impact ionization and channel breakdown.

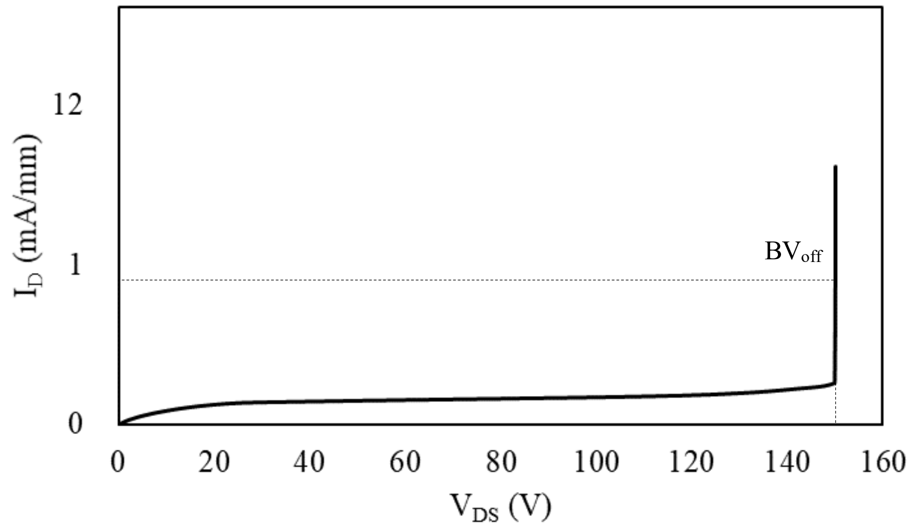

Figure 3. 9 Log-scale I_D-V_{DS} at $V_{GS\text{-}Eff}$=-0.5 V of the wide fin HFET with FP II.

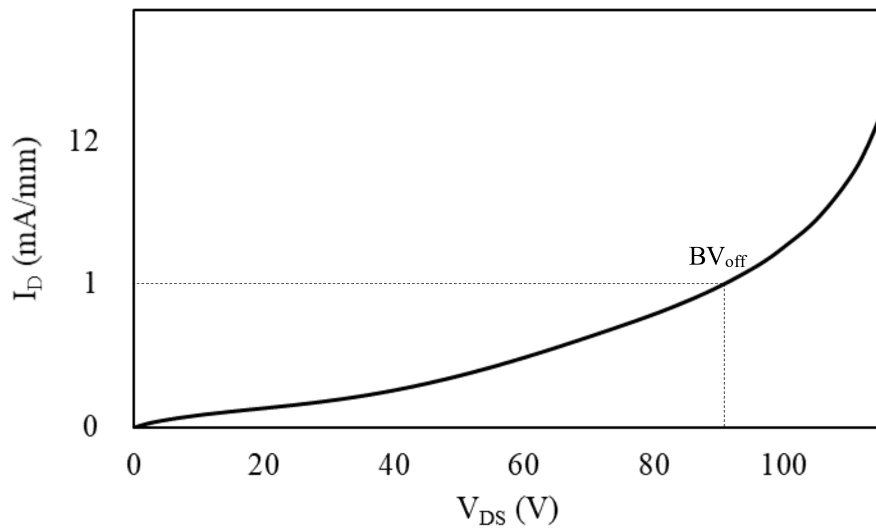

Figure 3. 10 Log-scale I_D-V_{DS} at $V_{GS\text{-}Eff}$=-0.5 V of the wide fin HFET with FP III.

When a FP is connected to the gate, by increasing the value of V_{DS} in addition to the drain-edge of the gate, an electric field peak forms at the drain-edge of the field-plate. As shown in Figure 3. 11-Figure 3. 13 the drain-source voltage at which the second peak (i.e. the one at the

drain-edge of the FP) forms depends on the specifications of the FP. For instance, for a specific value of L_{FP} and ε_r the resistivity of the channel under the FP is not the same for different values of t_{FP} thus, in the HFET whose t_{FP} is larger (i.e. HFET with FP III) due to its smaller channel resistivity the second peak of the electric field occurs at a larger value of V_{DS} compared to the HFET whose t_{FP} is smaller (i.e. HFET with FP I and II). Therefore, the electric field peak reaches the critical value at the drain-edge of the gate before the second peak becomes large enough to provide a high BV_{off}. On the other hand, in the case of HFET with FP II, which has the smallest t_{FP} among the explored HFETs, due to the large resistivity of the channel under the FP, the second peak forms at a smaller value of V_{DS}. Since, upon formation of the second peak, the rate of increase in the electric field versus V_{DS} is higher in the second peak compared to the first one, the breakdown occurs when the second peak reaches the critical value and while the first peak is still far away from this critical value. Therefore, the optimum value of the t_{FP} that can provide the maximum BV_{off} is when both peaks approach the critical value, which among the explored HFETs is the case for the HFET with FP I (Figure 3. 11).

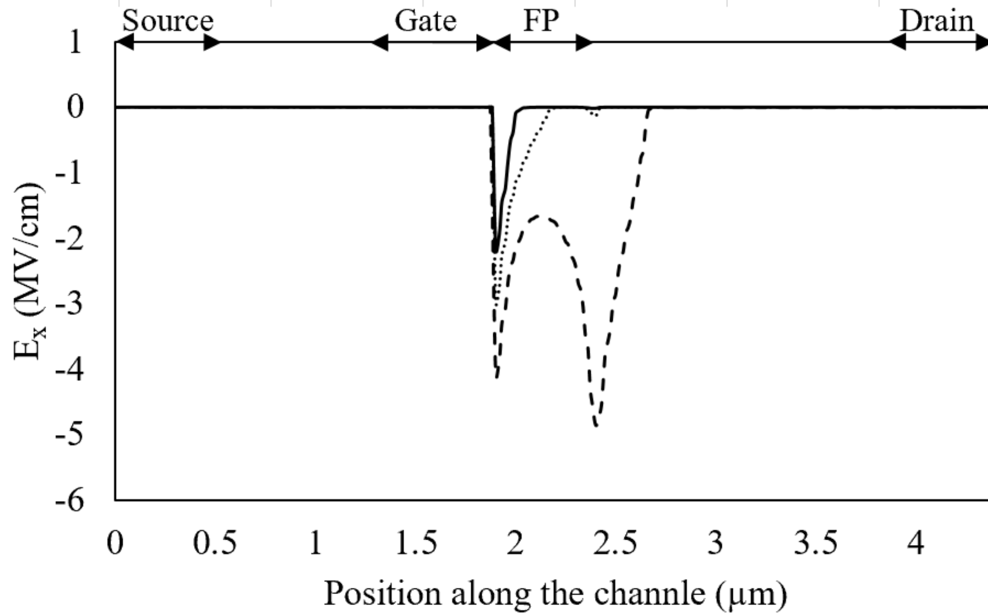

Figure 3. 11 Electric field profile along the channel (E_x) of the wide fin HFET with FP I at V_{DS} = 15, 35 and 190 V (solid, dotted, and dashed curve, respectively).

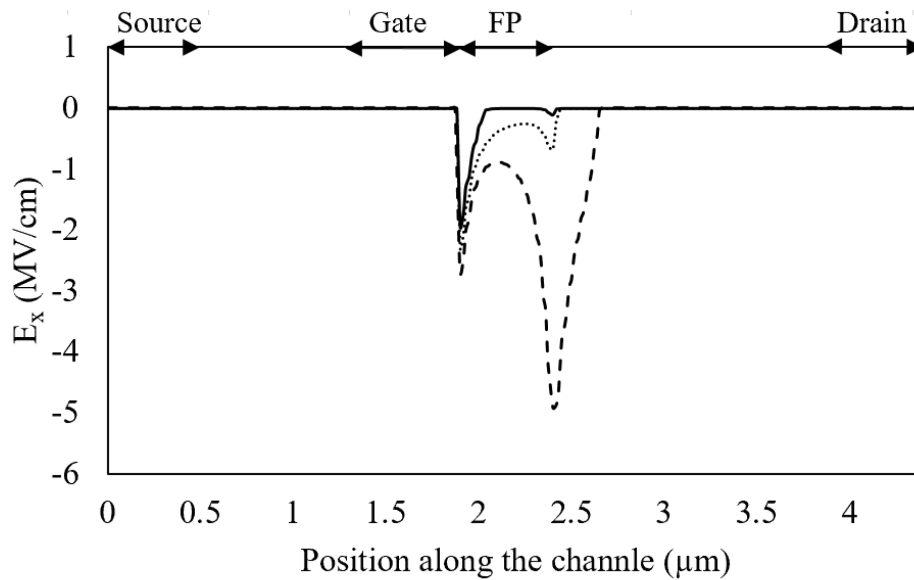

Figure 3. 12 Electric field profile along the channel (E_x) of the wide fin HFET with FP II at V_{DS} = 15, 35 and 150 V (solid, dotted, and dashed curve, respectively).

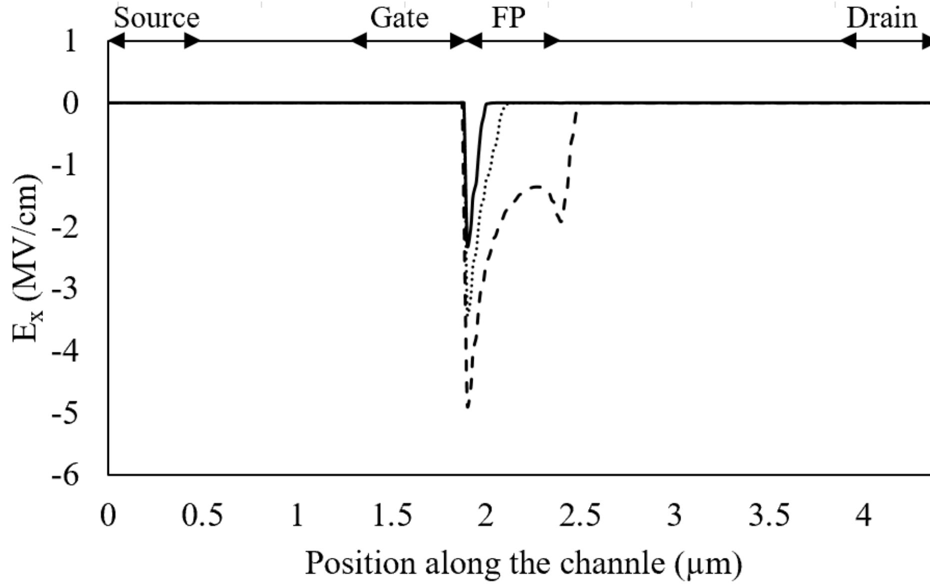

Figure 3. 13 Electric field profile along the channel (E_x) of the wide fin HFET with FP III at V_{DS} = 15, 35 and 120 V (solid, dotted, and dashed curve, respectively).

3.5.2.2 Effect of ε_r on BV_{off}

Since among the explored values of t_{FP} the value of 0.1 μm maximizes BV_{off}, I have adopted that value to investigate the effect of permittivity on BV_{off}. Figure 3. 14 demonstrates that the BV_{off} of the wide fin HFET with FP IV is 150 V. While in the wide fin HFET with FP IV ε_r is two times bigger than that of the wide fin HFET with FP I, its BV_{off} is 21% smaller. This result shows that increasing the permittivity by a factor of two reduces BV_{off} to the same extent as reducing t_{FP} by a factor of two. Therefore, compared to SiO_2 ($\varepsilon_r \cong 4$), implementing higher permittivity dielectric materials such as SiN ($\varepsilon_r \cong 8$) is not necessarily effective in improving the BV_{off}.

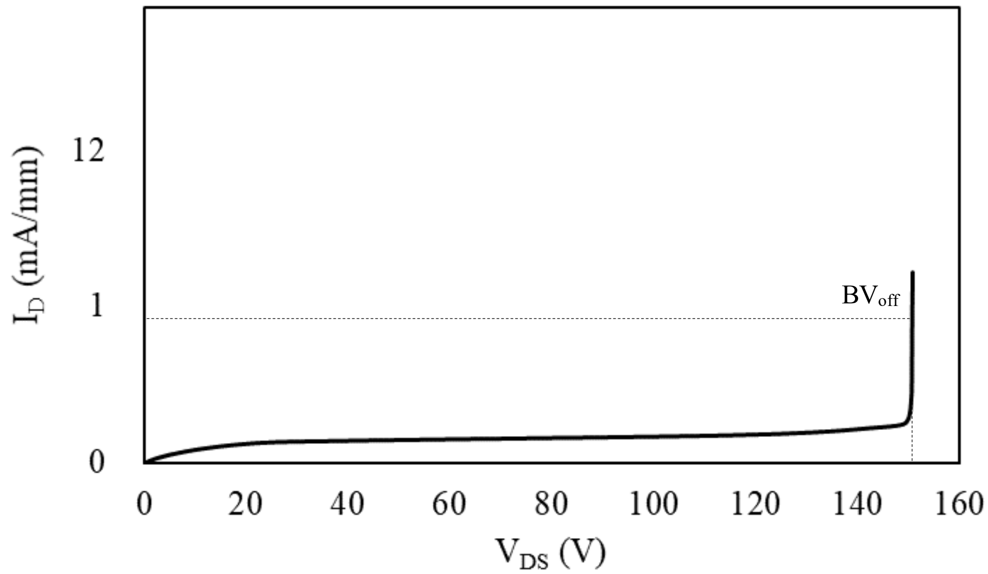

Figure 3. 14 Log-scale I_D-V_{DS} at $V_{GS\text{-}Eff}$=-0.5 V of the wide fin HFET with FP IV.

3.5.2.3 Effect of L_{FP} on BV_{off}

In this section, I have evaluated the effect of FP length on the off-state breakdown voltage of the wide fin HFET with the optimized t_{FP} and ε_r values (i.e. 0.1 μm and 4). As demonstrated in Figure 3. 15 and Figure 3. 16 by increasing the L_{FP} from 0.5 μm (i.e. the wide fin HFET with FP I shown in Figure 3. 8) to 1 μm and 1.5 μm, BV_{off} respectively increases by 5.2% and 5.7%, which infers that for these specific values of L_{GD}, t_{FP} and ε_r (i.e 2 μm, 0.1 μm and 4) further increase in the L_{FP} from 1 μm does substantially improve the BV_{off}.

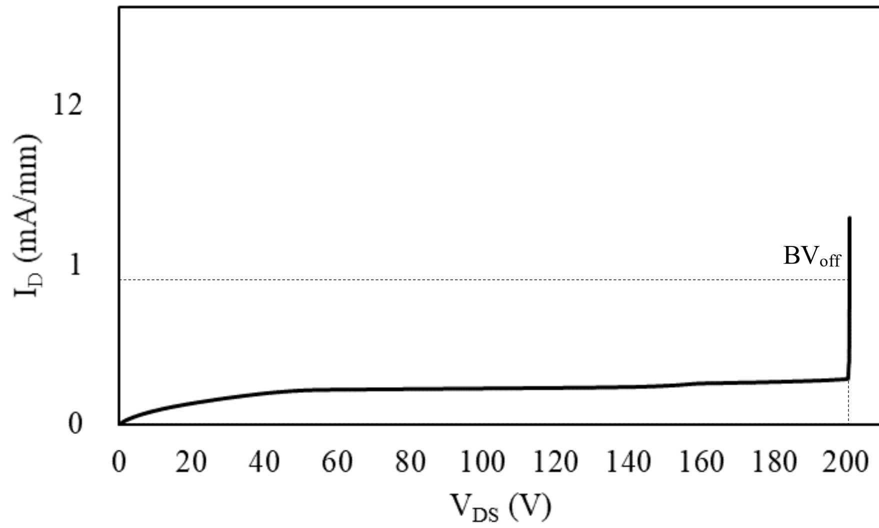

Figure 3. 15 Log-scale I_D-V_{DS} at $V_{GS\text{-}Eff}$=-0.5 V of the 200nm-wide fin HFET with FP V.

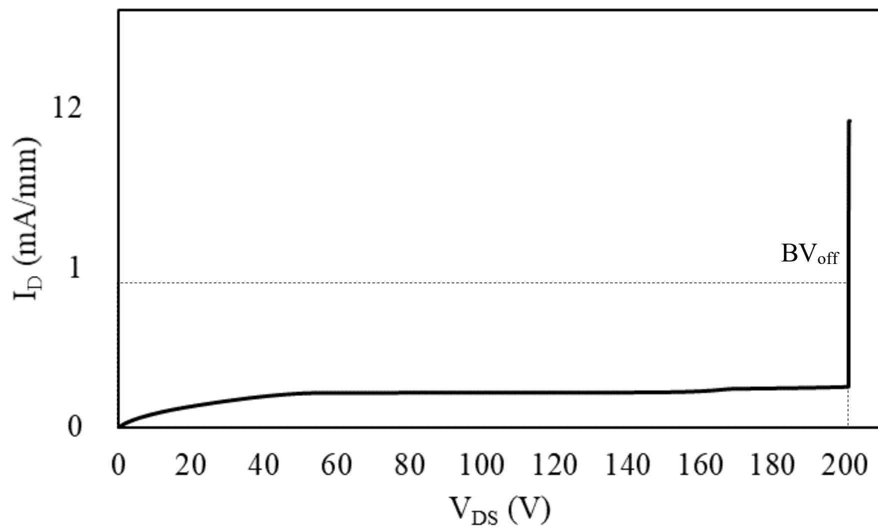

Figure 3. 16 Log-scale I_D-V_{DS} at $V_{GS\text{-}Eff}$=-0.5 V of the 200nm-wide fin HFET with FP VI.

3.6 Capacitance-voltage characteristics

It has been shown so far that a FP can improve BV_{off} more effectively than just reducing the isolation feature width. However, it is worth mentioning that employing a FP adds to the gate capacitance, which in turn deteriorates the high-frequency characteristics of the HFET. In order to

quantitatively investigate the effect of isolation feature geometry and FP on the total gate capacitance (C_g=C_{gd}+C_{gs}), as demonstrated in Figure 3. 17-Figure 3. 22, I have simulated the C-V characteristics of theses HFETs at 1 MHz and V_{DS}= 10 V. In these figures where I have distinguished the contribution of the FP from the gate capacitance (denoted by FP capacitance in the caption of the Figure 3. 18-Figure 3. 22), it is shown that among other FP specifications (i.e. L_{FP}, t_{FP} and ε_r) FP length has the most impact on the gate capacitance. For instance, while compared to the HFET with FP I, ε_r and L_{FP} are respectively doubled in the HFETs with FP IV and V, their capacitance is not increased to the same extent. This is because, altering t_{FP} and ε_r impacts the insulator capacitance while varying the L_{FP} also impacts the 2DEG capacitance in series with the insulator capacitance.

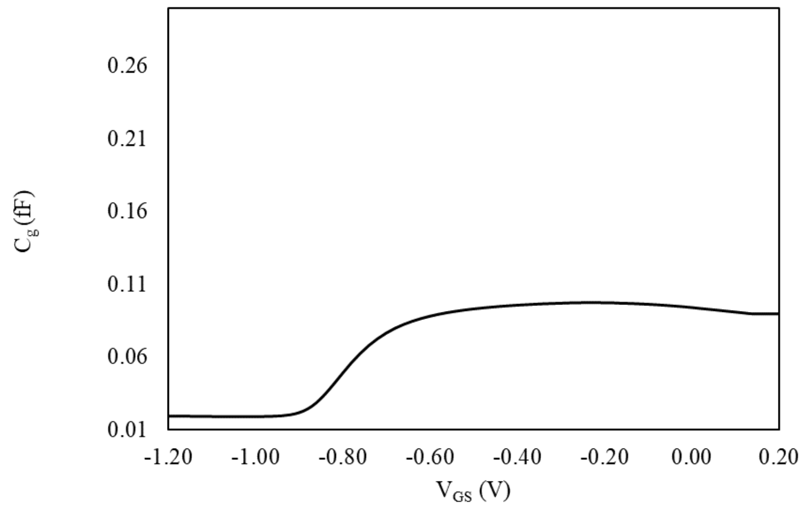

Figure 3. 17 Gate capacitance versus V_{GS} of the narrow fin HFET at V_{DS}= 10 V.

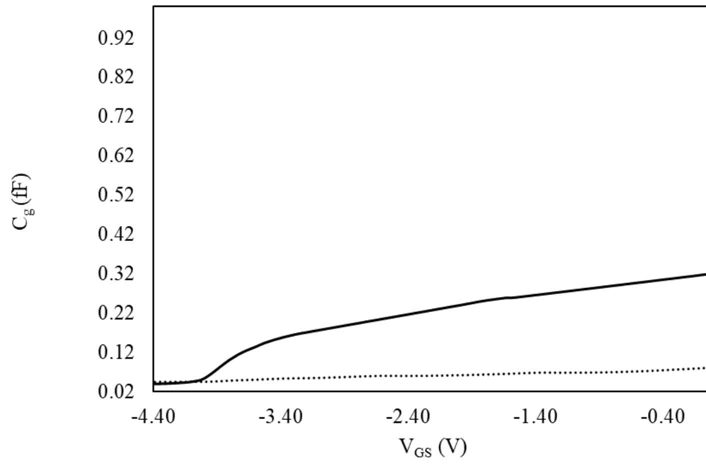

Figure 3. 18 Gate and FP components of the total gate capacitance versus V_{GS} of the wide fin HFET with FP I at V_{DS}= 10 V (solid curve: gate capacitance, dotted curve: FP capacitance).

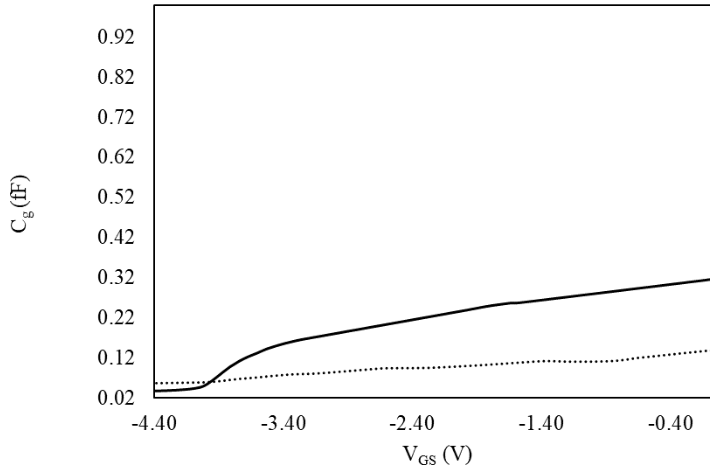

Figure 3. 19 Total gate capacitance versus V_{GS} of the wide fin HFET with FP II and HFET with FP IV at V_{DS}= 10 V (solid curve: gate capacitance, dotted curve: FP capacitance).

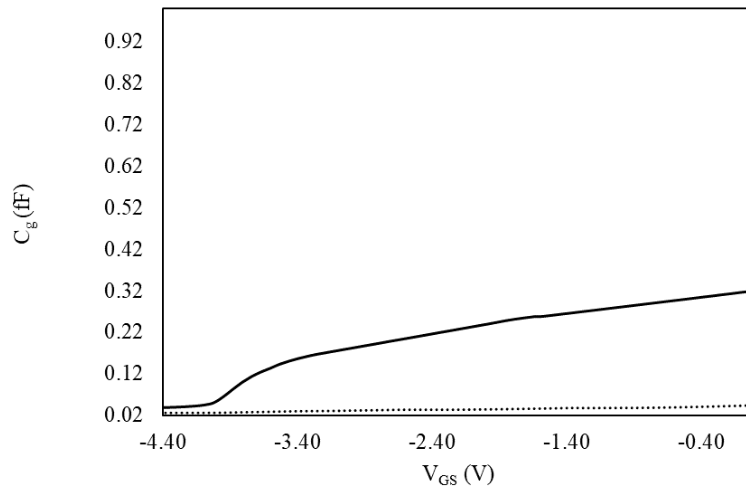

Figure 3. 20 Total gate capacitance versus V_{GS} of the wide fin HFET with FP III at V_{DS}= 10 V (solid curve: gate capacitance, dotted curve: FP capacitance).

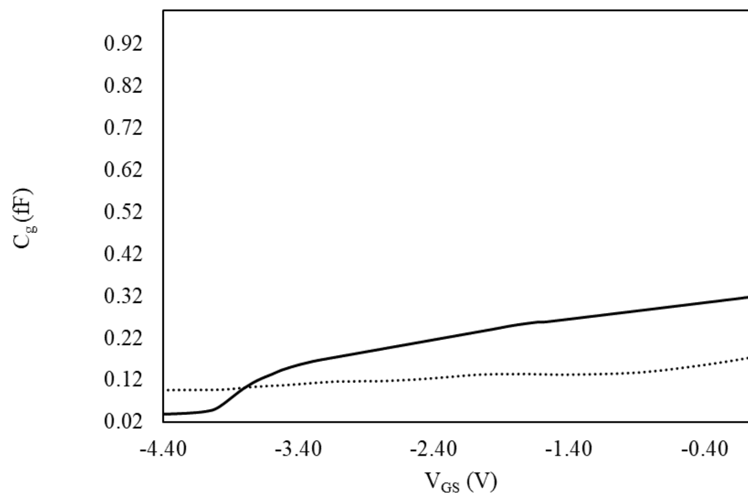

Figure 3. 21 Total gate capacitance versus V_{GS} of the wide fin HFET with FP V at V_{DS}= 10 V (solid curve: gate capacitance, dotted curve: FP capacitance).

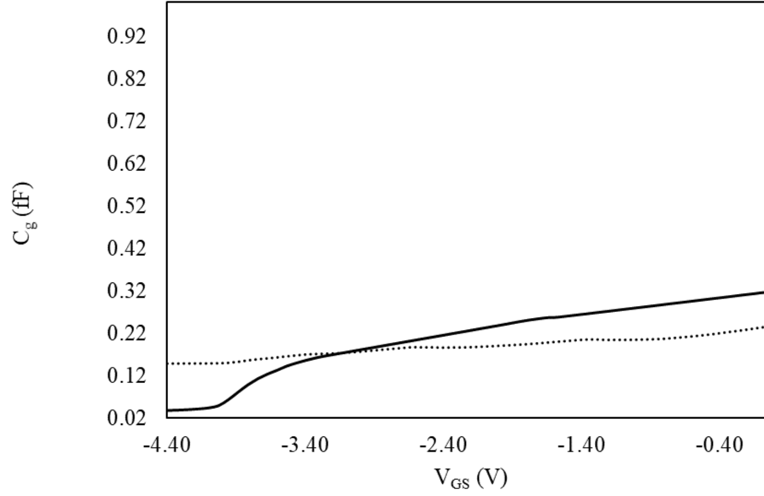

Figure 3. 22 Total gate capacitance versus V_{GS} of the wide fin HFET with FP VI at V_{DS}= 10 V (solid curve: gate capacitance, dotted curve: FP capacitance).

3.7 Johnson's Figure-of-Merit

In order to investigate the effect of FP specifications on the high-frequency characteristics of these HFETs, I have calculated the value of f_T versus V_{GS} using Eq. (3.1)

$$f_T = G_m/2\pi C_g, \tag{3.1}$$

where C_g and G_m are respectively extracted from Figure 3. 2 and Figure 3. 17-Figure 3. 22. As demonstrated in Figure 3. 24, the maximum f_T occurs at V_{GS}= -2.3 V which is the gate voltage at which G_m shows a peak. Based on Figure 3. 24 and the data presented Table 3. 3, while the wide fin HFET with a 1.5 µm long FP has the highest BV_{off}, it has the smallest f_T among all the explored HFETs. In addition, the wide fin HFET that has no FP demonstrates the maximum f_T while it delivers the minimum BV_{off}. Due to the observed trade-off between the f_T and BV_{off}, I have calculated JFOM, which is a metric to quantitatively assess the suitability of these HFETs for high-power microwave applications. According to the results presented in Table 3. 3, the wide fin HFET

with respective L_{FP}, t_{FP} and ε_r of 0.5 μm 0.1 μm and 4 (i.e. HFET with FP I) has the highest JFOM among all the explored HFETs here.

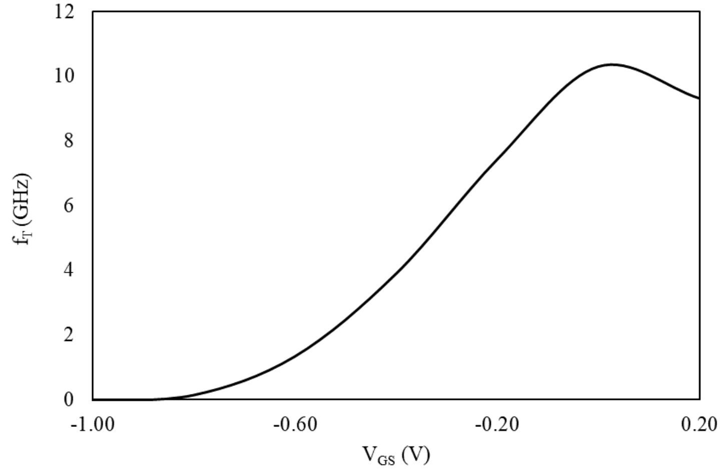

Figure 3. 23 f_T versus V_{GS} of the narrow fin HFET at V_{DS}=10 V.

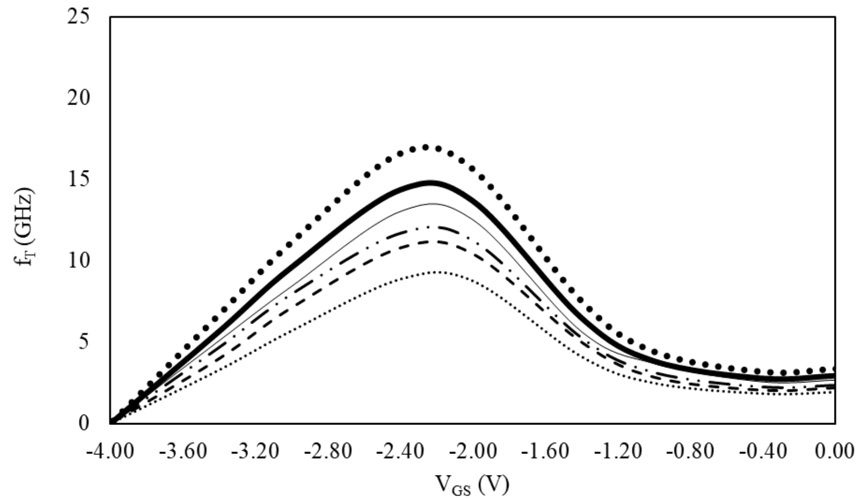

Figure 3. 24 f_T versus V_{GS} of the wide fin HFET with FP I (thin solid curve), FP II (dotted dashed curve), FP III (thick solid curve), FP IV (dotted-dashed curve), FP V (dashed curve), FP VI (thin dotted curve) and without FP (thick dotted curve) at V_{DS}=10 V.

Table 3. 3 Calculated values of G_m, C_g, f_T, BV_{off} and JFOM of the explored AlGaN/GaN HFETs.

Type of device	G_m(S) peak	C_g (fF) at G_m peak	f_T (GHz) at G_m peak	BV_{off}(V) at $V_{GS\text{-}Eff}$=-0.5	JFOM (THz.V)
Non-slanted fin	6.5×10^{-6}	0.09	11.5	101	1.16
Slanted fin I	6.5×10^{-6}	0.09	11.5	69	0.8
Slanted fin II	6.5×10^{-6}	0.09	11.5	100	1.15
Slanted fin III	6.5×10^{-6}	0.09	11.5	100	1.15
Wide fin without FP	2.4×10^{-5}	0.21	16.6	52	0.88
Wide fin with FP I	2.4×10^{-5}	0.27	13	190	2.47
Wide fin with FP II	2.4×10^{-5}	0.30	11.7	150	1.76
Wide fin with FP III	2.4×10^{-5}	0.25	14.3	88	1.26
Wide fin with FP IV	2.4×10^{-5}	0.30	11.7	150	1.76
Wide fin with FP V	2.4×10^{-5}	0.33	10.8	201	2.17
Wide fin with FP VI	2.4×10^{-5}	0.40	8.9	202	1.8

Table 3. 4 f_T, BV_{off} and JFOM of GaN HFETs reported in the literature (measurement data) and presented in this work (simulation).

L_G (μm)	L_{GD} (μm)	f_T (GHz)	VB_{off} (V)	JFOM (THz.V)	Ref
1.00	4.5, no FP	10	90	0.9	[2]
1.00	4.5, with FP	7	160	1.12	[2]
1.00	2.5, with FP	7.8	160	1.2	[79]
1.00	2.5, no FP	9.8	50	0.5	[79]
0.50	not determined, with FP	13.9	250	3.48	[80]
0.30	not determined, with FP	25	70	1.75	[81]
0.15	0.65, T-gate	60	55	3.3	[82]
0.6	2.0, narrow fin, no FP	11.5	101	1.16	This work
0.6	2.0, wide fin, no FP	16.6	52	0.88	This work
0.6	2.0, wide fin, with FP	13	190	2.47	This work

As a comparison between the measurement data and simulation results of this work, Table 3. 4 presents some of the JFOM data of GaN HFETs obtained from the literature and this work.

According to this table, BV_{off} of a conventional HFET with no FP and L_{GD} of 2.5 μm is 50 V [79], which is very close to the 52 V breakdown voltage of the wide fin HFET without FP simulated in this work. However, the value of f_T is 40% smaller in the HFET explored in [79], which can be due to its larger L_G compared to the simulated HFET. In addition, based on the data presented in Table 3. 4, the calculated value of JFOM of the HFET with FP I (i.e. 2.47 THz.V) is within the range of the experimentally reported data of GaN HFETs with FP (i.e. 1.12-3.48 THz.V).

3.8 Conclusion

In this chapter the effects of field-plate and isolation feature geometry on the off-state breakdown voltage and high frequency characteristics of AlGaN/GaN HFETs are investiagted. It is demonstarted that mere shrinking the isolation fetaure width by 75 % improves the BV_{off} by a factor of two. This results in 32% improvement in JFOM by just shrinkng the width of the isolation fetaure geometry from 200 nm to 50 nm and without employing any field-plate.

In addition, I evaluated the effect of FP parameters including its length and the thickness and permittivity of the dielectric material used under the FP to formulate a guideline for FP parameter defenition to achive as high as possile of JFOM for the wide fin HFETs explored in this work.

Results show that there is an optimum value for t_{FP} ($t_{FP,opt}$) where the maximum BV_{off} is achieved. This is because further increse in the thickness of the dielectric material layer from $t_{FP,opt}$ reduces the effect of FP in tailoring the electric field profile and BV_{off} improvement while further reduction of t_{FP} from $t_{FP,opt}$ results a large electric field peak at the darin adge of the FP resembeling an HFET with an extension to the gate by the FP lenght. Furthermore, it is demonstrated that in addition to t_{FP}, maximum BV_{off} can be obtained for an optimum value of ε_r. Furthermore, BV_{off} does not increase for increase in L_{FP} beyond a certain point. According to these results, the maximum BV_{off} can be achieved for the wide fin HFET with FP VI which is 3 times improvement

in BV_{off} compared to the wide fin HFET without FP. Nevertheless, the value of f_T of this HFET is 46 % smaller than that of the wide fin HFET without FP. Results from calculating the JFOM of the explored HFETs with various FP specifications show that the maximum JFOM can be obtained from the HFET with FP I. Finally, it is worth emphasizing that as mentioned before in chapter 2, the surface charge density that I have assumaed on the fin sidewalls of the simulated HFETs is almost one order of magnitude smaller than the concentration of surface states reported in the literature. Thus, it is speculated that if the realistic value of the nagative charge density was assumed on the sidewalls of the simulated AlGaN/GaN HFETs fins, the breakdown voltage and consequently JFOM of the same 50 nm-wide fin HFET could be substantially higher.

Chapter 4

The isolation feature geometry dependence of reverse gate-leakage current of AlGaN/GaN HFETs

4.1 Introduction

Although AlGaN/GaN HFETs have been widely used over the past two decades in power electronics and RF applications there are still issues with their full-scale commercialization due to problems such as excessive reverse gate leakage [83],[84],[85]. In order to understand the origin of the reverse gate leakage in these HFETs, several mechanisms have been investigated so far [22],[83],[86],[87], which depending on the bias and temperature conditions, the pertinence of these mechanisms in describing the leakage behavior might differ. For instance, in polar III-nitride HFETs for large negative values of gate-source bias, due to the presence of a strong electric field across the barrier, Fowler-Nordheim (FN) has been demonstrated to be the dominant leakage mechanism [86], [88]–[90]. This is while thermionic field emission (TFE) is expected to take over when the electron temperature is also sufficiently elevated [91], [92]. When the electric field across the barrier and temperature are not sufficient for FN or TFE, other mechanisms such as Poole-Frenkel (PF) emission or trap-assisted tunneling (TAT) that rely on the existence of traps are observed to be dominant in the evaluation of the reverse gate leakage [83], [92]–[94]. Surface leakage which is associated with the surface traps is another leakage mechanism that becomes

significant for large V_{DS} and V_{GS} values [95].

In addition to the leakage through the AlGaN barrier, leakage between the gated sidewalls of the isolation features and the 2-D electron gas (2DEG) has been also demonstrated to be worthy of consideration [86], [87], [96], [97], [98]. For instance, in evaluating the reverse gate leakage of AlGaN/GaN HFETs Rahbardar *et al.* have observed that at less negative values of V_{GS}, gate leakage is smaller in conventional mesa HFETs compared to devices with the same overall gate width but comprising of fin-type isolation features. They have justified this observation by substantiating the dominance of leakage at the gate-covered isolation feature sidewalls over the leakage through the AlGaN barrier at less negative values of V_{GS} [86], [87]. They have also attributed the lack of substantial difference between the values of I_G for more negative values of V_{GS} among these devices to the significance of leakage through the equally wide barrier of the explored devices over the sidewall leakage for this later range of V_{GS} [86].

In this chapter, the relevance of isolation feature geometry to the reverse gate leakage is investigated over AlGaN/GaN HFETs realized not only on the conventional mesa configuration but also on the fin-type isolation features which are more than one order of magnitude narrower than those studied in [86]. I demonstrate that when the dimensions are shrunk to the sub-micrometer range, in addition to gate voltages greater than the threshold voltage, gate current is dominated by the leakage through the gated sidewalls for $V_{GS}<V_{th}$. Accordingly, by investigating the effect of isolation feature geometry on the profile of the electric fields responsible for the leakage through sidewall and top surface gate, I present mechanisms that explain the room temperature leakage characteristics of HFETs realized on micron and sub-micron size isolation features at V_{DS}=0 V.

4.2 Device Fabrication and Specifications

The epitaxial layer structure used in this work is a Ga-face Wurtzite $Al_{0.25}Ga_{0.75}N$/GaN heterostructure composed of a 25 nm thick unintentionally doped (UID) barrier, a 250 nm thick GaN channel and a 1.45 µm thick Fe-doped GaN buffer layer grown on a 4-inch 4-H SiC substrate. The device processing at McGill University's Nanotool Microfabrication facilities, for realization of the transistors depicted in Figure 4. 1, started with coating the sample with ma-N 2403 negative resist followed by electron beam lithography (EBL) with a beam energy of 20 keV to define the mesa and the fins. After developing the sample in ma-D 525, magnetically-enhanced reactive ion etching (MERIE) using Cl_2/Ar plasma in an Applied-Materials P5000 MERIE system was employed to etch mesas and fins to depth of 200 nm. After removing the resist, the sample was coated with MMA(8.5)MAA-EL11/PMMA-A2 co-polymer positive resist for the 2nd EBL step of registration of the Ohmic contacts with the same beam energy as step one. Following this step, after developing the photoresist in MIBK/IPA 1/3 the sample was immersed in HCl solution to remove the native oxide followed by Ohmic metallization using NEXDEP e-beam evaporation and lift-off in acetone. After that, the metal stack of Ti/Al/Ni/Au (20 nm/140 nm/55 nm/45 nm) underwent rapid thermal annealing (RTA) at 830°C for 30 s using JetFirst 200 to form the alloyed Ohmic contact to the 2DEG. Demonstrating the good quality of the fabricated Ohmic contacts, the contact resistance (R_c) and sheet resistance (R_{sh}) extracted through transfer length measurement (TLM) are consistently about 0.78 Ω.mm and 400 Ω/□, respectively. The 3rd EBL step with the same conditions as the previous EBL step was performed to define the gate contacts. DisCharge H_2OX2 anti-charging agent was used during the 2nd and 3rd EBL steps to eliminate the e-beam divergence, which otherwise occurs due to accumulation of electrons caused by the presence of the insulating SiC substrate. Subsequently, Ni/Au (20 nm/20 nm) metal stack was e-beam

evaporated and lifted-off to form the Schottky gate electrode. In the reported process, no surface passivation has been carried out.

Following deposition of contact pads, SÜSS MicroTec PM5 probing station and Keithley 4200-SCS semiconductor characterization system were used for on-chip room-temperature characterization of the fabricated AlGaN/GaN HFETs.

In order to investigate the effect of isolation feature geometry on the reverse gate leakage of AlGaN/GaN HFETs, I have fabricated HFETs realized on two different isolation features including conventional mesa and fin structures (Figure 4. 1) in which cases the channel width is 44 µm and 0.4 µm, respectively. The HFETs of the fin-type consist of three fins that are 0.4 µm wide, therefore the overall gate width in the fin category is 1.2 µm. All of the fabricated devices have L_G of 0.6 µm, L_{GS} of 2.4 µm, and L_{GD} of 3 µm.

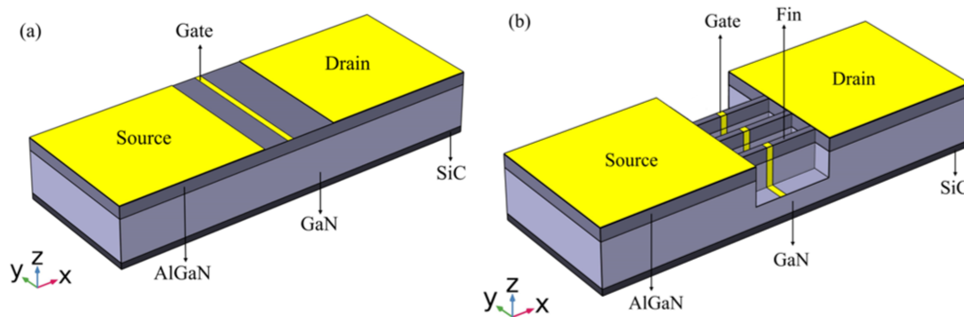

Figure 4. 1 Schematic illustration of the transistors built on (a) conventional mesa and (b) fin isolation features.

As demonstrated in Figure 4. 2 the threshold voltage is -3.3 V and -1.9 V for the conventional mesa and fin-type HFETs, respectively. The less negative threshold voltage of the fin-type HFET compared to the conventional mesa device determines that a better electrostatic control is offered over the intrinsic gated channel of HFETs realized on narrower isolation feature which is mainly due to the triple-gate effect [57], peel force development (hence, strain minimization) [62], and the

presence of surface states at the sidewall facets, which is believed to be the dominant mechanism for this positive shifting [39]. The more negative V_{th} of the conventional mesa HFET explored in this chapter compared to the one presented in chapter 2 could be due to its smaller gate length and relatively being more exposed to DIBL.

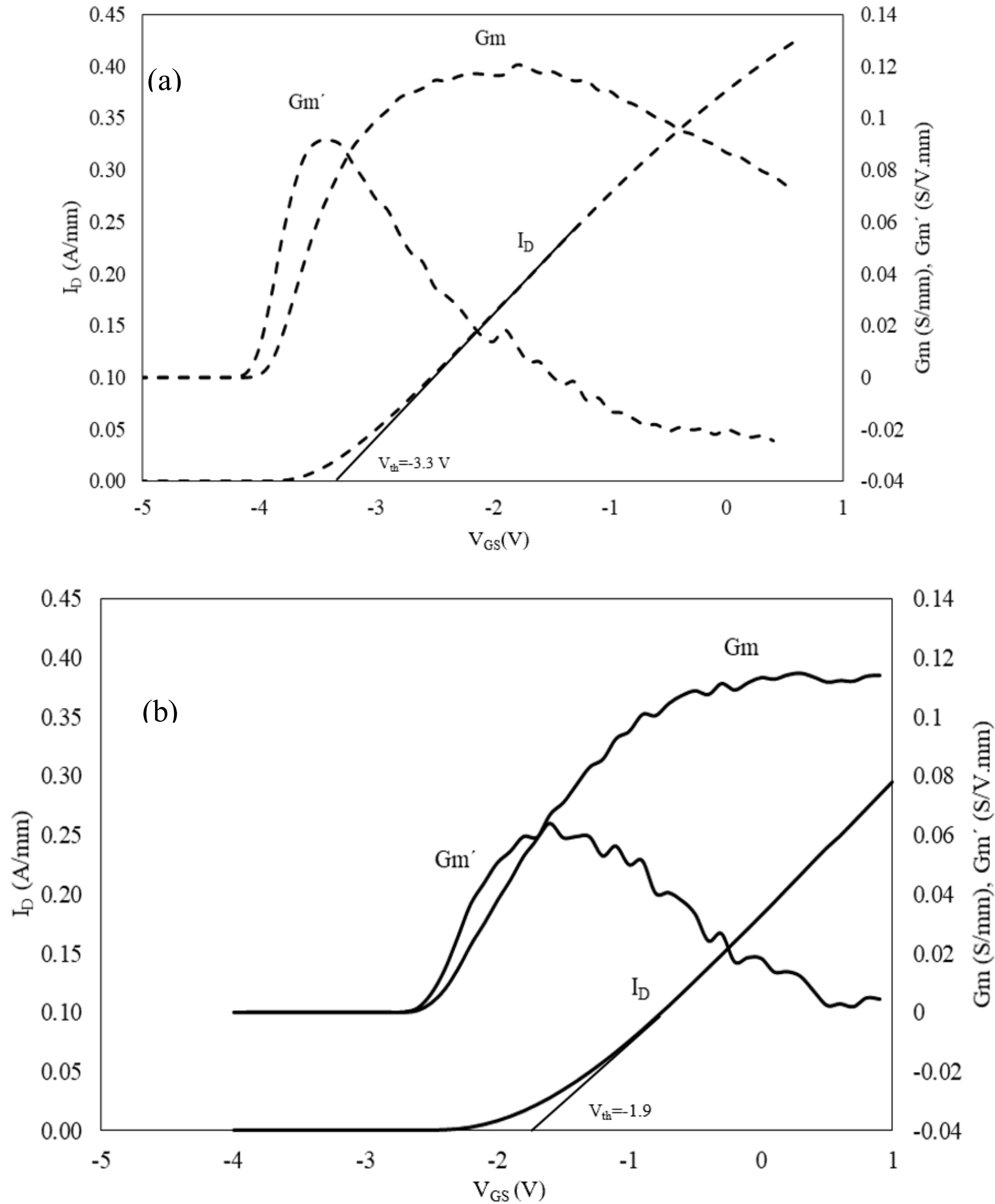

Figure 4. 2 Normalized transfer characteristics and variation of gate transconductance (G_m) and its first derivative versus V_{GS} of the conventional mesa (a) and fin (b) type HFETs at V_{DS}= 10 V.

4.3 Results and discussion

Since the overall gate width is not identical among the two device categories, to perform a fair assessment of the gate leakage I have calculated the scaled-up gate current of a fin-type HFET consisting of 110 fins, yielding the same width as the fabricated conventional mesa HFET. While in the explored fin-type HFETs I_{on}/I_{off} ratio is as high as 2×10^7 (Figure 4. 3), as shown in Figure 4. 4, at all values of V_{GS} the gate current of the fin-type HFET with the same overall gate width as the conventional mesa is more than one order of magnitude higher than that of the mesa counterpart.

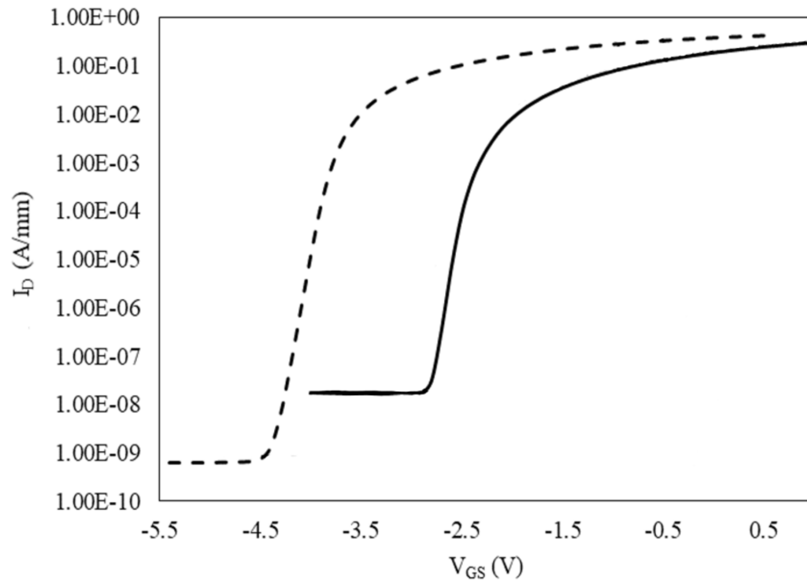

Figure 4. 3 Log-scale normalized drain current versus gate-source of the conventional mesa (dashed curve) and fin (solid curve) HFETs at V_{DS}=10 V

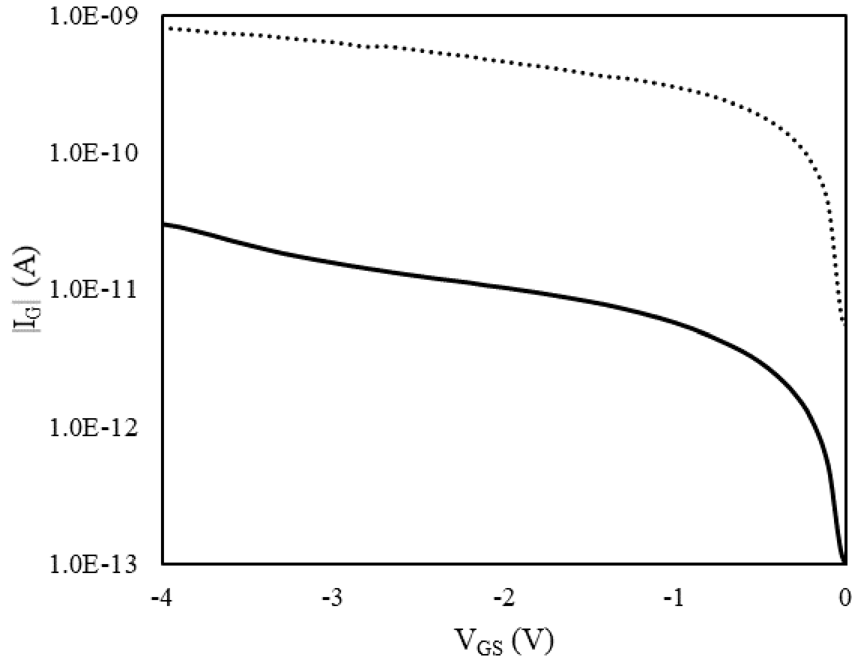

Figure 4. 4 Log-scale room-temperature measured gate current (I_G) of a 44 µm-wide conventional mesa HFET (solid curve) and an HFET with 110 fins of 400 nm width (dotted curve) at V_{DS}=0 V.

This observation suggests that compared to the mesa-type HFET, sidewall leakage becomes more prominent in determining the gate leakage even at V_{GS} values below the threshold voltage in devices comprising of much smaller fin widths, and consequently larger number of sidewalls to yield the same overall gate width as a single mesa.

In order to substantiate this speculation, the amount of leakage due to each of the assumed individual leakage components (i.e. leakage to the 2DEG through the gated sidewalls and through the top surface gate) should be separately identified. Relying on the prior evidence [87], [90], [92] to this end, I have modeled the gate leakage speculating FN as the mechanism responsible for the leakage through the top-surface gate for more negative values of V_{GS}. Accordingly, the current associated with the FN process is calculated by [91] ,

$$I_{FN} = S_{FN} \frac{q^2(m_e/m^*_{n,AlGaN})(\gamma E)^2}{8\pi h \varphi_b} \exp(\frac{-B}{\gamma E}) \quad (4.1)$$

in which q is fundamental electronic charge, h is the Planck's constant, m_e is the free electron mass, $m^*_{n,AlGaN}$ is the conduction band effective electron mass in the barrier layer, $q\varphi_b$ is the Schottky barrier height considering the Schottky barrier lowering and

$$B = 8\pi \frac{\sqrt{2m^*_{n,AlGaN}(q\varphi_b)^3}}{3qh}. \quad (4.2)$$

As per [86], based on the information on the presence of inhomogeneity of the vertical electric field across the barrier of III-nitrides [86], [89], [99], [100], the current due to the FN leakage mechanism is position-dependent. Therefore, the FN-related current which leaks through a part of the barrier that boasts a higher electric field dominates the total leakage current through the barrier. This small portion of the barrier through which FN tunneling predominantly takes place is called the "FN leakage zone (S_{FN})" and the magnification of the electric field across this zone is defined by the γ factor.

In our analysis in assessing the current associated with the FN process (I_{FN}) in terms of (4.1), E which is the electric field half way through the barrier under the gate is calculated employing COMSOL Multiphysics [65]. The accuracy of the calculated electric field using COMSOL is confirmed by its similar value calculated by (4.3) [92]

$$E = \frac{\varphi_b - V_{GS} - \Delta\varphi_C + \varphi_F}{d_{barrier}} \qquad \text{for } V_{GS} > V_{th} \qquad (4.3)$$

in which $q\Delta\phi_c$ is the conduction-band discontinuity at the barrier/channel hetero-interface, $q\varphi_F$ is the difference between fermi energy level and conduction-band edge at the GaN side and $d_{barrier}$ is the barrier thickness. Device parameters used in COMSOL simulations have been already summarized in Table 2. 2

Figure 4. 5 demonstrates the profile of the vertical electric field in the middle of the barrier along the channel of AlGaN/GaN HFETs of two different isolation feature geometries having similar electrical characteristics such as V_{th} with the fabricated HFETs. As demonstrated in this figure, the strength of the vertical electric field is almost constant under the gate for V_{GS} values above the threshold voltage, while it is larger at the gate edges for V_{GS} values below the threshold voltage. Therefore, for calculating I_{FN} I have integrated the current due to the FN process at each mesh point in COMSOL simulations over the length of the gate. As an example, based on Figure 4. 6, the vertical electric field almost saturates at V_{GS} values below the threshold voltage, which is due to the partial depletion of the 2DEG for this bias range. Due to the less negative threshold voltage of the HFET comprising of narrower fins, the saturation of the electric field occurs at a less negative V_{GS} compared to the HFET of wider isolation feature. This is why below V_{GS} of -1.9 V (i.e. the threshold voltage of the narrower fin HFET) the amount of the vertical electric field is larger in the HFET of wider isolation feature.

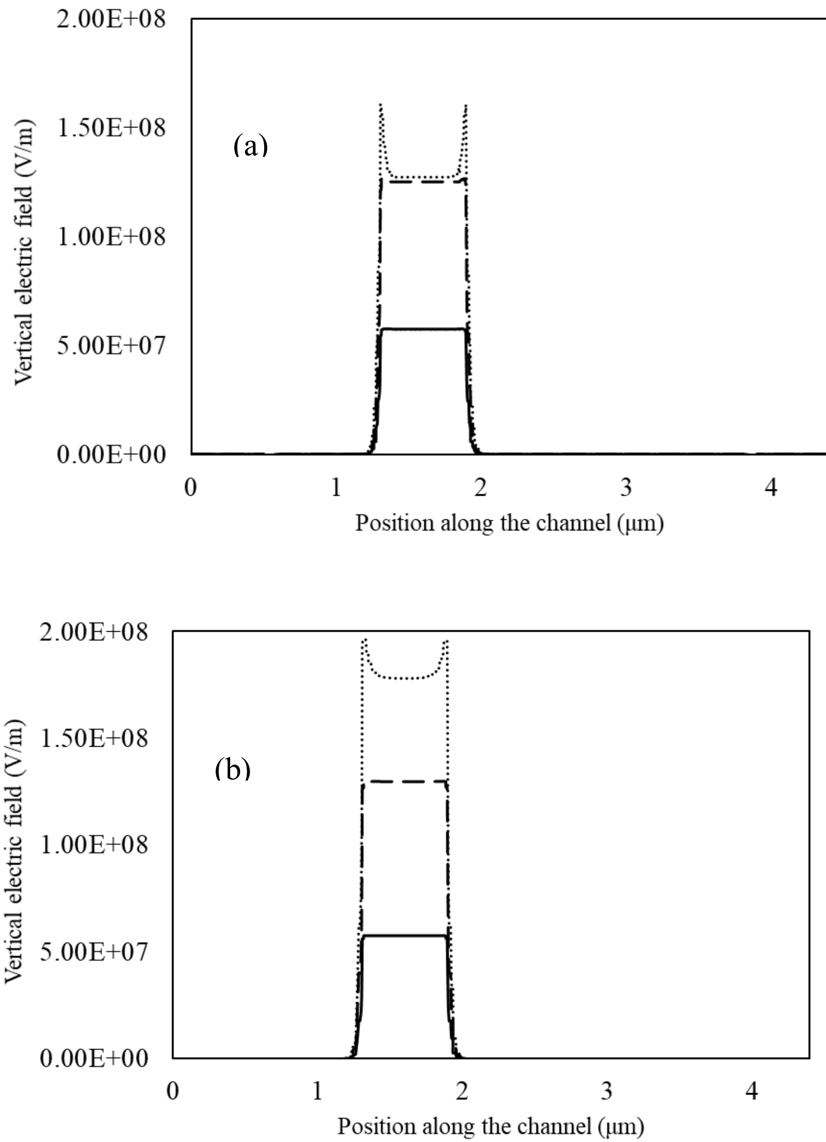

Figure 4. 5 Profile of the vertical to the channel electric field halfway through the barrier versus position along the channel length at V_{GS}= 0, -2, and -4 V and V_{DS}=0 V, for (a) narrower channel HFET with V_{th} of -1.9 V and (b) wider channel HFET with V_{th} of -3.3 V.

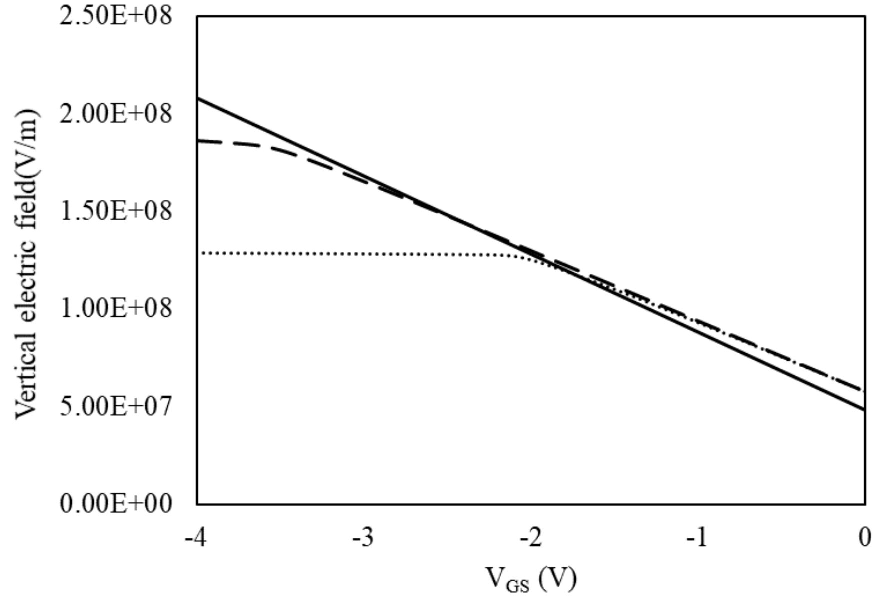

Figure 4. 6 Vertical to the channel electric field halfway through the barrier under the drain-edge of gate versus V_{GS} at V_{DS}=0 V, for wider channel HFET with V_{th} of -3.3 V (dashed curve) and the narrower channel HFET with V_{th} of -1.9 V (dotted curve). The solid curve represents the same electric field component calculated by (4.3).

Based on (4.1) the V_{GS} range across which I_{FN} takes the dominant role, is where a linear dependence of $\mathrm{Ln}(I_G/(\gamma E)^2)$ versus $1/\gamma E$ is observed. In establishing this trend, the value of γ was initially adopted from [86], and was gradually increased until the slope of $\mathrm{Ln}(I_G/(\gamma E)^2)$ versus $1/\gamma E$ is proportional to $\sqrt{m_n^* \varphi_b{}^3}$. Accordingly, as shown in Figure 4. 7 the intercept of $\mathrm{Ln}(I_G/(\gamma E)^2)$ versus $1/\gamma E$ curve with the vertical axis determines the value of S_{FN}. Further below, it is shown that the calculated values of S_{FN} and γ provide the best match between the measured gate current and modeled I_{FN} at more negative values of V_{GS} in the mesa isolated HFET.

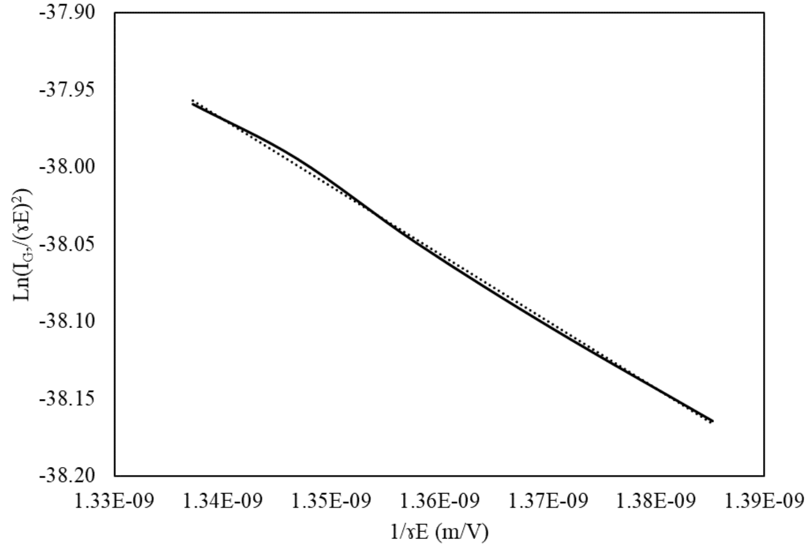

Figure 4. 7 Ln($I_G/(\gamma E)^2$) versus $1/\gamma E$ for the mesa-type HFET. Dotted curve is based on the measured I_G and calculated values of γ and E and the solid line is the linear interpolation among these data points.

It is worth mentioning that the absence of such a linear relationship in the Ln($I_G/(\gamma E)^2$) versus $1/\gamma E$ characteristics of the fin-isolated HFETs indicates the lack of the dominance of FN for any value of V_{GS} in this device type. Furthermore, I have assessed the suitability of other vertical leakage mechanisms such as PF, TAT and phonon-assisted tunneling (PhAT) [101] in predicting the observed leakage trend in the fin-type HFETs. However, these trap-related mechanisms also fall short of acceptable modeling of the gate leakage in these HFETs. Based on this observation and our earlier speculation on the dominance of leakage through the gated sidewalls in HFETs realized on fins across the whole range of the explored V_{GS}, I have investigated the applicability of TAT, PF and PhAT to this leakage path. However due to the depletion of the 2DEG below the threshold voltage PF is incompetent in predicting the gate leakage for this bias range. PhAT also is more dominant at higher temperatures and V_{DS} values [102]. This is while the TAT mechanism taking place between the gated sidewalls and the 2DEG of the explored fin-type HFETs provides

sufficient evidence on the dominance of this mechanism not only for $V_{GS}>V_{th}$ but also for $V_{GS}<V_{th}$. Accordingly, sidewall leakage due to TAT is calculated using (4) [92]

$$I_{TAT} = 2S_{Sidewall} \frac{q}{E_{Sidewall}} \int_0^{\varphi^{t-2}} \left(\frac{1}{C_1 f_{FD} N_1 P_1^0} + \frac{1}{C_2 N_2 P_2^0} \right)^{-1} d\varphi \tag{4.4}$$

$$P_{1,2}^0 = P_{1,2} | \psi = 0 \tag{4.5}$$

$$P_1 = exp\{- \frac{\alpha}{E_{Sidewall}} \left[\varphi^{3/2} - (\varphi_1 - \psi)^{3/2} \right] \} \tag{4.6}$$

$$P_2 = ex\,p \left[- \frac{\alpha}{E_{Sidewall}} (\varphi_2 + \psi)^{3/2} \right] \tag{4.7}$$

$$\alpha = 8\pi \frac{\sqrt{2m_{n,GaN}^* q}}{3h} \tag{4.8}$$

$$C_{1,2} = \frac{16\pi q E_1^{3/2}}{3h\sqrt{\varphi_{1,2} - E_1}} \tag{4.9}$$

$$f_{FD} = \frac{1}{1 + exp[(\varphi_b - \varphi)/V_t]} \tag{4.10}$$

$$N_{1,2} = \frac{N_t}{\phi_1 - \phi_2} \left(\int_0^{\varphi_1 - \varphi_2} P_{1,2} d\psi / P_{1,2}^0 \right) \tag{4.11}$$

in which $S_{Sidewall}$ is the area of the gated sidewall through which leakage occurs, $E_{Sidewall}$ is the electric field defined in terms of the potential difference between the gate and the 2DEG calculated employing COMSOL (Figure 4. 8), and P_1 and P_2 represent probability of the tunneling process from metal to the lower edge of the localized trap band and from the higher edge of the trap band to 2-DEG, respectively and N_t is the trap concentration.

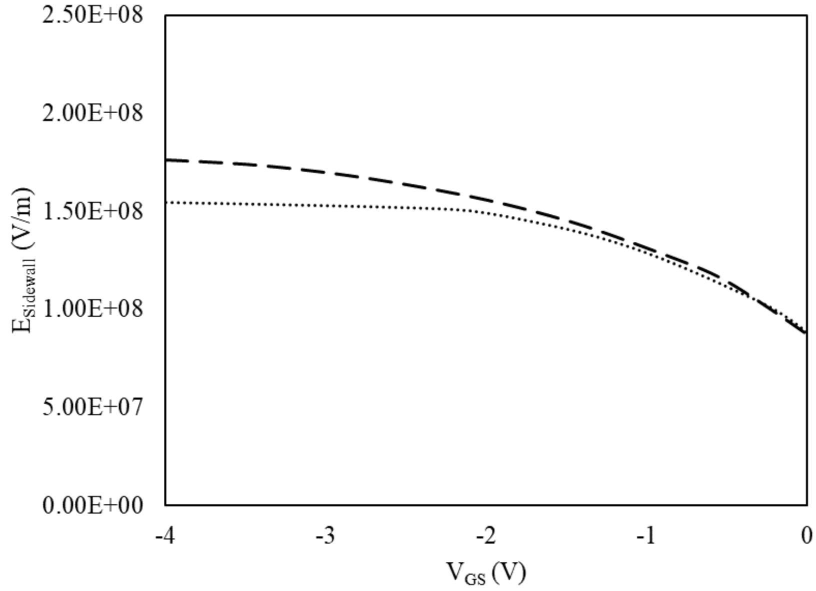

Figure 4. 8 Normal to the sidewall electric field at the sidewall drain-edge of gate 5nm below the heterointerface versus V_{GS} at V_{DS}=0 V, for wider channel HFET with V_{th} of -3.3 V (dashed curve) and the narrower channel HFET with V_{th} of -1.9 V (dotted curve).

Table 4. 1 represents the values of the parameters used in calculation of the currents associated with each leakage mechanism.

Table 4. 1 Values of the parameters used in (4.1)-(4.11)

Parameter	Value	Unit	Ref.
$m_{n,AlGaN}^*$	$0.4 \times 9.11 \times 10^{-31}$	Kg	[103]
$m_{n,GaN}^*$	$0.2 \times 9.11 \times 10^{-31}$	Kg	[55]
$\varphi_{b0,GaN}$	0.84	V	[55]
$\varphi_{b0,AlGaN}$	1.16	V	[55]
φ_b	$\varphi_{b0} - 4.7 \times 10^{-6}\sqrt{E}$	V	[87]
$\Delta\varphi_C$	0.3	V	[55]
φ_F	0.2	V	[86]
φ_1	1.1	V	[92]
φ_2	0.45	V	[92]
E_1	0.2	V	[92]
N_t	10^{17}	m^3	Fitted
γ	4	-	Extracted
S_{FN}	10^{-20}	m^2	Extracted
$S_{sidewall}$	3×10^{-16}	m^2	Calculated

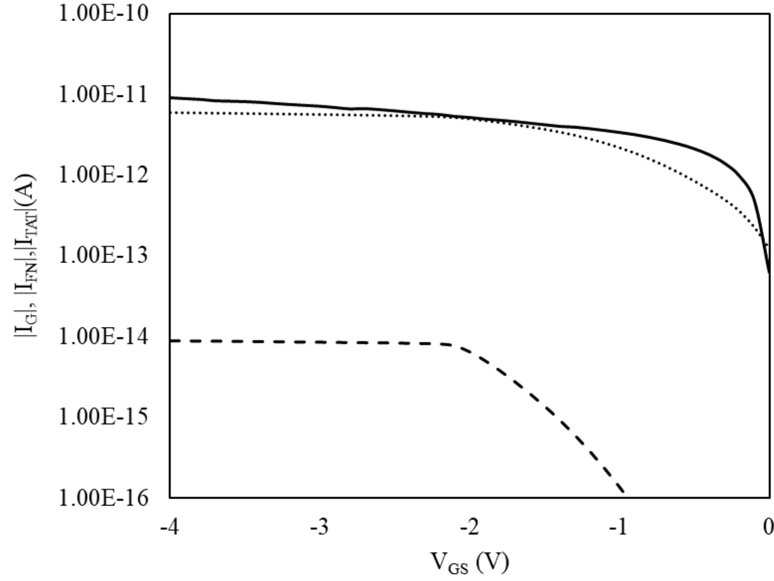

Figure 4. 9 Log-scale gate current components of an HFET with a 400 nm-wide fin, the dotted curve is the leakage due to the TAT process through the gated sidewalls, the dashed curve is the leakage current due to the FN process through the top surface gate and the solid curve is the experimentally measured leakage current of this HFET.

Using (4.1) and (4.4) as shown in Figure 4. 9, within the range of 0 V to -4 V of the V_{GS} in the fin-type HFET the dominant leakage mechanism is TAT through the gated sidewalls. However, as demonstrated in Figure 4. 10, in the mesa HFET FN process through the top surface gate is the dominant leakage mechanism for gate voltages below -3 V and TAT through the gated sidewalls is dominant for V_{GS}>-3 V. It is worth mentioning that V_{GS} of -3 V is the same voltage where a kink in the measured gate current versus V_{GS} curve is observed in mesa-type HFET (solid curve in Figure 4. 10). In other words, the sudden increase in the saturated gate current at V_{GS}=-3 V is because at this point vertical leakage due to the FN process which exponentially increases with the electric field prevails the sidewall leakage due to TAT. This is while in the fin-type HFETs the dominant leakage path is through the gated sidewalls at all values of V_{GS}. This dissimilarity in the dominance of the gate leakage mechanism at V_{GS}<V_{th} among the explored mesa and fin-type

HFETs is attributed to the difference in the profile of the electric field among these device categories for large negative values of V_{GS}. In broad terms, the vertical electric field, which exponentially impacts the vertical leakage due to FN process almost saturates for $V_{GS}<V_{th}$, therefore compared to the conventional mesa, the fin-type HFET due to whose geometry has a more positive value of V_{th}, retains a weaker electric field at any value of V_{GS} below its threshold voltage. Consequently, for V_{GS} values below the threshold voltage of the fin-type HFET, leakage due to the FN process is larger in the mesa HFET.

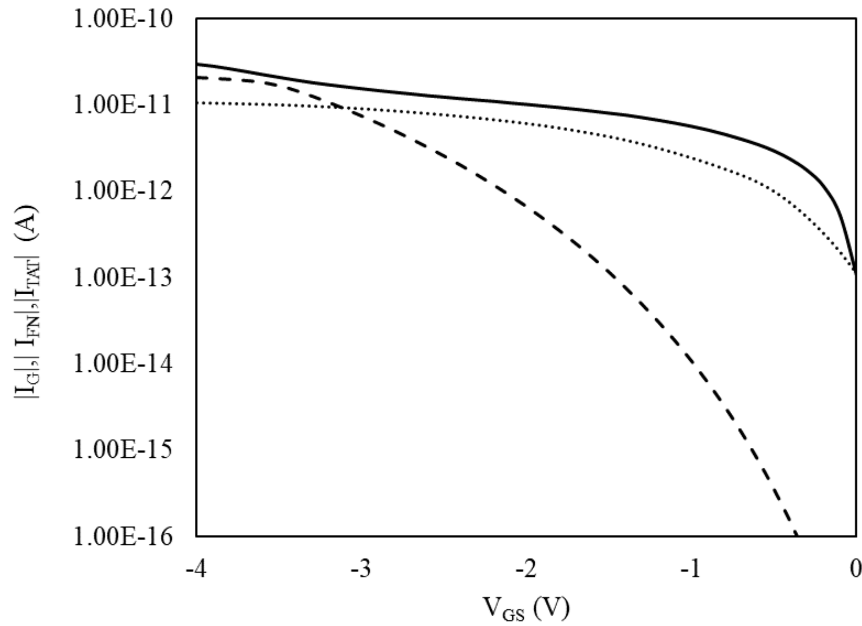

Figure 4. 10 Log-scale gate current components of an HFET realized on a 44 µm-wide mesa, dotted curve is the leakage due to the TAT process, the dashed curve is the leakage current due to the FN process and the solid curve is the experimentally measured leakage current of this HFET.

4.4 Conclusion

Reverse gate leakage at V_{DS}=0 V is investigated over HFETs realized on fins and mesa-isolated features and it is shown that two main leakage mechanisms that contribute to the total gate leakage

at room temperature are FN and TAT. It is demonstrated that due to the positive shift of threshold voltage in devices realized on fins of smaller widths compared to the wider mesas, the saturation of their electric field across the barrier happens at a more positive value of V_{GS}. Accordingly, at any value of V_{GS} below the threshold voltage of the fin-isolated HFET, the electric field across the barrier of the mesa HFET is stronger, which results in its exponentially larger value of the FN-related leakage component compared to the fin counterpart. While it is demonstrated that in the leakage characteristics of the mesa HFET there is a turning point below which FN process takes the dominant role, in the fin-type HFET, even at the extreme negative end of the explored gate voltages, sidewall leakage due to TAT is superior to the vertical leakage due to the FN process. Although leakage due to the FN process is substantially larger in the mesa HFET, the total amount of gate leakage is higher in the fin type HFET consisting 110 fins to yield the same overall gate width as the conventional mesa which indicates the importance of sidewall leakage in devices comprising a large number of fins of sub micrometer size gate width. Finally, devices made on narrow fins while offer a luring avenue for V_{th} tuning and realization of enhancement-mode devices, need to pay an excessive price in terms of reverse gate leakage current unless suitable solutions such as properly isolating the sidewalls are considered.

Chapter 5

Conclusions and future work suggestions

5.1 Concluding remarks

In chapter 1, I presented the excellent electronic properties of GaN which have made it a suitable candidate as the semiconducting channel in transistors of high-power/ high-frequency amplifiers and RF switches, in addition to switches of power electronic circuitry. Since in all these applications the ability to operate at high voltages is crucial, understanding the mechanisms that limit the breakdown voltage of these HFETs is of substantial importance. To this end, I first presented the underlying physics and mechanisms of the breakdown and according to the existing body of literature, identified field-plate as the mainstream technique for improving the off-state breakdown voltage in AlGaN/GaN HFETs. In this chapter, some of the main field-plate configurations that have been explored so far are explained and a brief description about their fabrication process is presented to highlight the difficulty and challenges associated with FP implementation.

In chapter 2, I explored the correlation between the isolation feature geometry and BV_{off} of AlGaN/GaN HFETs. Accordingly, I presented the fin technology as a novel approach in BV_{off} improvement. Employing COMSOL Multiphysics, I showed that in this approach by reducing the isolation feature width, the depleting effect of sidewall surface states becomes more pronounced

thus, a more resistive path is imposed on the drain access region of these HFETs. By exploring the profile of the longitudinal electric field along the channel I observed that at a given drain-source voltage, a smaller electric field peak forms at the drain edge of the gate in devices of narrower isolation feature widths which explains their higher BV_{off}. Due to the simultaneous importance of superior output current in addition to the off-state breakdown voltage in power electronic applications, I presented a slanted-fin configuration that due to its geometry can maintain a better trade-off between I_{on} and BV_{off}, which is substantiated by its highest BFOM among the explored HFETs with a slanted and non-slanted isolation feature geometries. Finally, I substantiated the suitability of isolation feature geometry in improving the off-state breakdown voltage by fabricating and characterizing real HFETs of submicrometer-wide fins in addition to the conventional mesa isolation feature geometry.

In chapter 3 employing COMSOL Multiphysics, I explored the effect of variation in the tapering position of the slanted fins on BV_{off} of the AlGaN/GaN HFETs. It is shown that while shifting the tapering position from the drain edge of the gate toward the drain enhances BV_{off}, there is a point beyond which BV_{off} does not increase any further. In addition, I explored the effect of FP on BV_{off} of devices of larger isolation feature widths where the depleting effect of sidewall surface states is not as pronounced as the narrower counterparts. In these HFETs I evaluated the effect of various FP parameters including FP length and the thickness as well as permittivity of the dielectric material under the FP, to formulate a guideline for FP parameter definition to achieve as high as possible of the BV_{off}. According to this assessment there is an optimum value for each of the explored FP parameters that maximize the breakdown voltage. As mentioned in chapter 1, one of the disadvantages of field-plate implementation is the augmented gate capacitance that limits the high frequency FOMs of the transistors. Hence, I calculated this parasitic gate capacitance to

identify the impact of FP with different configurations on the f_T. Results demonstrate that the HFET with the highest BV_{off} has the minimum f_T while the HFET with the highest f_T has the minimum BV_{off}. Since there is a trade-off between f_T and BV_{off}, by calculating the JFOM of theses HFETs, I identified the FP configuration that suits the millimeter-wave applications best.

In chapter 4, I explored the effect of isolation feature geometry on the reverse gate leakage of AlGaN/GaN HFETs. While based on the literature, FN is deemed as the main leakage mechanism specially at large negative values of V_{GS}, in this chapter I showed that in HFETs realized on fins of sub-micrometer width due to their more positive value of V_{th}, the saturation of the electric field occurs earlier compared to a conventional mesa HFET. Therefore, unlike conventional mesa HFETs FN mechanism does not have the dominant role even at V_{GS} values well below the threshold voltage. I also proved that apart from the leakage from the top-surface gate, there is a leakage path between the gated sidewalls and the 2DEG channel which becomes worthy of consideration when an HFET consists of a large number of isolation features and consequently larger number of the gated sidewalls.

5.2 Future work suggestions

While in this thesis I have assessed the suitability of sidewall surface states on improving BV_{off} in devices of sub-micrometer isolation feature width, exploring this effect in devices of nanometer isolation feature width seems to be worthy of consideration. In addition, exploring the efficiency of isolation feature engineering on BV_{off} improvement is suggested to be assessed in devices of different gate-drain spacings. In this work, I was not able to perform this assessment, since our measurement capacity was limited and this effect could not be identified.

Furthermore, exploring other annealing techniques such as laser annealing is suggested as a future work, since specially when the lateral dimension are shrunk the quality of the ohmic contact becomes crucial.

In this thesis I only simulated the high frequency characteristics of AlGaN/GaN HFETs with/without FP however, fabricating devices with FP and performing actual measurement of their high frequency characteristic to compare with those of non-FP devises is recommended.

In addition, I suggest exploring the off-state breakdown voltage, high frequency figures of merit and gate leakage of AlGaN/GaN HFETs with a wide isolation feature geometry from source to drain edge of the gate and fin-type isolation features in the drain access region.

Finally, I would suggest investigating the effect of isolation feature geometry on the reverse gate leakage of AlGaN/GaN HFETs at V_{DS} values above zero volt to identify the dominant leakage mechanisms of submicron/nanometer fin-isolated HFETs at V_{DS} values other than zero.

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Appendix I: Process flow

❖ Steps toward mesa/fin lithography and etching

1. Cleaning

- Acetone [5 min]
- Isopropyl alcohol [1 min]
- Deionized water [2 min]
- Nitrogen gun
- Dehydrate on hotplate at 150 °C [2 min]

2. Spin coating

▪ Coat sample with ma-N 2403 resist

- Spread at 500 rpm for 5sec
- Spin with 3000 rpm for 30 sec
- Deceleration 5sec

3. Soft bake

▪ 90 °C hotplate for 60 sec

4. E-beam lithography

- Exposures dose: 100 μC/cm^2 (mesa) and 200 μC/cm^2 (fin)
- Line spacing and center to center distance: 10 nm
- Working distance: 4.6 mm
- Spot size: 2.9 nm
- Absorption current 37 pA

5. Develop

- ma-D 525 for 3 min
- DI water
- Nitrogen gun

6. Hard bake

▪ 100 °C for 60 sec

7. **Etch**

- Use MERIE P5000

• Cl_2: 20	Ar: 10	70 G	0 W	100 mtorr	10 s
• Cl_2: 20	Ar: 10	70 G	170 W	100 mtorr	110 s
• Cl_2: 0	Ar: 60	0 G	50 W	0 mtorr	10 s

8. **Resist removal**

   - Acetone
   - IPA
   - DI water
   - Nitrogen gun

❖ Steps toward fabrication of Ohmic contacts

1. **Cleaning**

   - Acetone [5 min]
   - Isopropyl alcohol [1 min]
   - Deionized water [2 min]
   - Nitrogen gun
   - Dehydrate on hotplate at 150 °C [2 min]

2. **Spin coating**

- Spin coat MMA(8.5)MAA-EL11 resist
  - Spread at 500 rpm for 5sec
  - Spin with 4000 rpm for 45 sec
  - Deceleration 5sec

- Bake sample on hotplate at 150°C for 90s
- Cool down the sample

- Spin coat PMMA-A2
  - Spread at 500 rpm for 5 sec
  - Spin with 4000 rpm for 45 sec
  - Deceleration 5sec

3. **Soft bake**

- Bake sample on hotplate at 180°C for 90 s

4. E-beam lithography

- Exposures dose: 100 µC/cm^2
- Line spacing and center to center distance: 20 nm
- Working distance: 3.2 mm
- Spot size: 2.6 nm
- Absorption current 39 pA

5. Develop

- Develop in MIBK/IPA 1/3 for 30 sec
    - Stop develop in DI water
    - Post-bake at 100°C for 60 sec
    - Oxide removal in $HCl:H_2O$ (1:4) solution for 2 minutes
    - Rinse in DI water
    - Drying with nitrogen gun (hot plate was not used to prevent oxide re-growth)

6. Metallization

- Ti 200 Å / Al 1400 Å / Ni 550 Å/ Au 450 Å

7. Liftoff

- Liftoff in acetone and ultrasound bath

8. RTA

- 830°C for 30 s

❖ Steps toward fabrication of gate metal

1.Cleaning

- Acetone [5 min]
- Isopropyl alcohol [1 min]
- Deionized water [2 min]
- Nitrogen gun
- Dehydrate on hotplate at 150 °C [2 min]

2.Spin coating

- Spin coat MMA(8.5)MAA-EL11 resist
    - Spread at 500 rpm for 5sec
    - Spin with 4000 rpm for 45 sec

- Deceleration 5sec

- Bake sample on hotplate at 150°C for 90s
- Cool down the sample
- Spin coat PMMA-A2
    - Spread at 500 rpm for 5 sec
    - Spin with 4000 rpm for 45 sec
    - Deceleration 5sec
- Bake sample on hotplate at 180°C for 90 s
- Spin coat H_2OX2 anti-charge agent
    - Spread at 500 rpm for 5 sec
    - Spin with 4000 rpm for 45 sec
    - Deceleration 5sec

3.E-beam lithography

- Exposures dose: 100 μC/cm^2 (gate pad) and 200 μC/cm^2 (gate finger)
- Line spacing and center to center distance: 20 nm
- Working distance: 3.2 mm
- Spot size: 2.6 nm
- Absorption current: 39 pA

5.Develop

- Develop in MIBK/IPA 1/3 for 30 sec
    - Stop develop in DI water
    - post-bake at 100°C for 60 sec

6.Metallization

- Ni 200 Å/ Au 500 Å

7.Liftoff

- Liftoff in acetone and ultrasound bath

❖ Steps toward pad deposition

1.Spin coating

- Spin coat with AZ5214 photoresist
    - Spread at 500 rpm for 5sec
    - Spin with 3000 rpm for 30 sec
    - Deceleration 5sec
- Bake sample on hotplate at 90°C for 55 s

2.Photolithography

- Exposure with 25 mJ/cm^2
- Post-bake at 105°C for 120 sec
- Flood Exposure with 250 mJ/cm^2 for 0.6 s

3.Develop

- AZ726 developer for 30 s
- Stop develop in DI water
- Post-bake at 100°C for 60 sec

4.Metallization

- Ni 200 Å/ Au 200 Å

5.Liftoff

- Liftoff in acetone and ultrasound bath
- Sample cleaning with acetone, IPA, and DI water

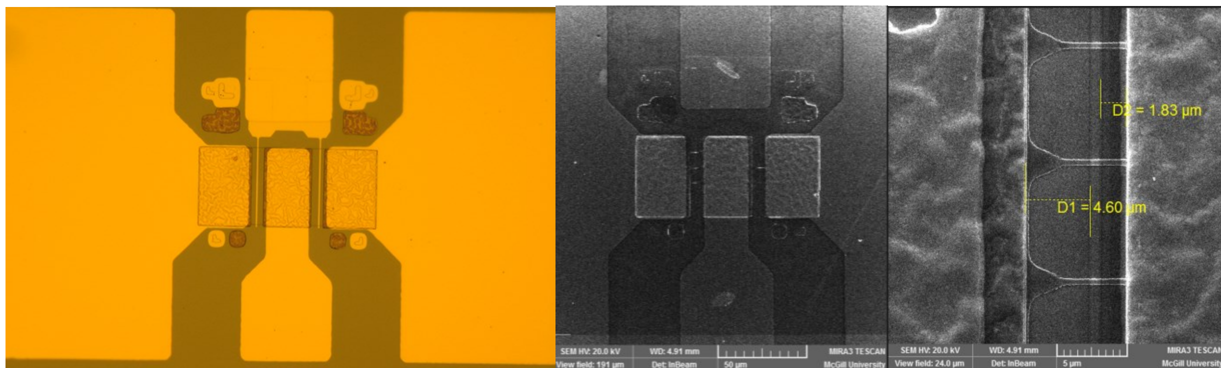

Figure I. 1 Micrograph and SEM images of the fabricated conventional mesa and slanted-fin HFETs.