Design of Reconfigurable Interfaces for Energy Efficient Nanophotonic Interconnects

Shayan Zohrei

A Thesis

in

The Department

of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements

for the Degree of

Master of Applied Science (Electrical and Computer Engineering) at

Concordia University

Montréal, Québec, Canada

December 2023

CONCORDIA UNIVERSITY

School of Graduate Studies

This is to certify that the thesis prepared

By: **Shayan Zohrei**

Entitled: **Design of Reconfigurable Interfaces for Energy Efficient Nanophotonic Interconnects**

and submitted in partial fulfillment of the requirements for the degree of

Master of Applied Science (Electrical and Computer Engineering)

complies with the regulations of this University and meets the accepted standards with respect to originality and quality.

Signed by the Final Examining Committee:

_____ Chair
Dr. Otmane Ait Mohamed

_____ External Examiner
Dr. Mohsen Ghafouri

_____ Examiner
Dr.

_____ Supervisor
Dr. Sébastien Le Beux

Approved by _____
Dr. Yousef Shayan, Chair
Department of Electrical and Computer Engineering

_____ 2023

_____
Dr. Mourad Debbabi, Dean
Faculty of Engineering and Computer Science

Abstract

Design of Reconfigurable Interfaces for Energy Efficient Nanophotonic Interconnects

Shayan Zohrei

Many core architectures have become instrumental in addressing the ever-increasing demand for computational power in modern computing systems. As these architectures scale to accommodate an ever-growing number of processing cores on a single chip, the need for efficient data movement within and between these cores has become a crucial concern. As chip designs become more complex, traditional electrical interconnects face limitations due to increasing power dissipation, signal integrity issues, and bandwidth constraints. Short-reach nanophotonic interconnects offer a promising alternative to overcome these challenges. Photonic Networks on Chips (PNoCs) have been demonstrated to provide high bandwidth with low latencies and low data-dependent power. However, large-scale adoption of PNoC is hampered by laser power overheads, thermal tuning, and electrical-optical conversion. To meet the target bit error rate (BER), the laser source must output enough optical power to overcome the optical channel loss and limited receiver sensitivity for the silicon photonic links. In addition, several parallel applications, such as multimedia processing, have built-in tolerances for inaccuracies that allow soft errors on a chip, such as bit flips. However, there is no method to design energy efficient optical links. This thesis investigates the design of reconfigurable nanophotonic interconnects and provides a reduction method to reduce the control complexity of the receivers and transmitters.

Acknowledgments

Thanks to my supervisor, Professor Sébastien Le Beux who helped me in each step and I learned a lot from him.

Thanks to my family who were supportive of me the whole time.

Thanks to Mehrshad, Ashkan, Mohsen and Khadijeh for their kindness and friendship.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

This chapter presents the context and motivation of this thesis, followed by the problem statement and proposed methodology. We conclude the chapter by outlining the thesis organization.

1.1 Context

The demand for faster data transmission, lower power consumption, and increased data capacity has become a paramount concern in the rapidly evolving landscape of modern computing and information technology. As electronic devices continue to shrink in size and increase in complexity, traditional metal-based interconnects, which are essential components for transmitting data within and between integrated circuits, are encountering severe limitations [11]. These limitations stem from various factors, including high signal propagation delays, power dissipation, and crosstalk issues, which are particularly pronounced in short-distance communication links within microchips and data centers.

Nanophotonics has emerged as a promising solution to address these challenges and pave the way for the next generation of high-performance computing systems. Nanophotonics leverages the properties of light at the nanoscale, offering the potential to overcome

the limitations of traditional metallic interconnects. This thesis is motivated by the need to explore the potential of nanophotonics in the context of short-reach interconnects within the domain of electrical engineering [12].

1.2 Motivation

The motivation for this thesis lies in the need to revolutionize how short-reach interconnects operate. As computing systems and data transmission requirements advance remarkably, there is a pressing demand for interconnect solutions to keep pace with these evolving challenges. Short-reach interconnects, used in microchips, data centers, and high-speed communication systems, are central to the efficient functioning of circuits. However, they are facing various challenges that necessitate innovative solutions.

Traditional metal-based interconnects face scaling limitations as semiconductor technology progresses. As devices become smaller and more densely packed, signal propagation delays, cross-talk, and heat dissipation become increasingly problematic. Nanophotonic interconnects provide a promising alternative by leveraging the advantages of photonics at the nanoscale. Furthermore, recent advancements in silicon photonics have enabled the integration of photonics with existing CMOS technology, facilitating the development of on-chip nanophotonic interconnects. These innovations open the door to cost-effective and scalable solutions for short-reach interconnects. The impact of efficient short-reach interconnects extends beyond academia and research. It has significant economic and industrial relevance, as companies and organizations seek solutions that can enhance the performance and sustainability of their products and services.

One of the difficult challenges to implementing nanophotonic interconnects is the high power consumption of lasers due to their low efficiency. High insertion loss of optical devices such as microrings and waveguides increases the required optical power for the receivers. Furthermore, high insertion loss leads to different received optical power for each

receiver that can be utilized. High bandwidth nanophotonic interconnects are limited to high power consumption, and their full potential can only be achieved with innovative architectures and algorithms. Utilizing multiple receivers with multiple wavelengths requires complex controllers that use many control bits and limit the stability of nanophotonic interconnects.

1.3 Problem Statement

Silicon photonics offers high bandwidth and low latency optical connections, making it ideal for high-speed data transfer and processing in data centers. However, there are some limitations that need to be overcome. This thesis aims to answer the following key questions.

- How can we minimize the data transfer energy per bit, considering optical losses, lasing efficiency, and BER requirements, while keeping the control complexity of the interface acceptable?
- Can we design a ubiquitous transmitter and receiver that could be used for all nodes of a Photonic Network on Chips (PNoC)? Due to the high number of receivers and transmitters in optical links, employing similar circuits can help the scalability of the design.
- What are the key design considerations when developing reconfigurable circuits for PNoC, and how can these circuits adapt to varying communication requirements?

This thesis tries to answer these problems by utilizing reconfigurable circuits that reduce power consumption and a proposed reduction method to reduce the control complexity of the circuits. By addressing these questions, the thesis aims to comprehensively understand the practical implications and innovative solutions surrounding short-reach nanophotonic

interconnects, ultimately contributing to advancing energy-efficient, high-performance many-core architectures.

1.4 Proposed Methodology

In this thesis, first, we propose reconfigurable receivers for Single Writer Multiple Reader (SWMR) optical links. By tuning the gain of the receivers based on their optical requirements, each receiver can be fine-tuned to amplify the signal to reach its required Bit Error Rate (BER). A reconfigurable optical link can reduce power consumption by controlling each receiver with a current steering Digital to Analog Converter (DAC).

Next, reconfigurable transmitter circuits are proposed, further reducing power consumption. Then, in order to reduce the design complexity, the number of control bits is reduced using the proposed method. As a result, a design flow and reduction method is proposed to tune each receiver based on its distance from the transmitter, number of receivers, number of active wavelengths, and the required BER. Figure 1.1 depicts the proposed design method in which, based on the provided electrical and optical libraries, the circuit is designed. Furthermore, the optical link is simulated in a system-level simulator, and its results are used to design it. By utilizing the circuit and system simulations on the reduction method, an optical link with reduced DAC can be achieved that provides low power consumption with minimum required control bits. The design flow can be used for other receiver and transmitter architectures to improve the overall design.

This thesis aims to investigate and contribute to the field of short-reach nanophotonic interconnects by exploring their potential to address these challenges. By employing reconfigurable circuits and proposed methods, we aim to improve state-of-the-art designs and proliferate the usage of applications of nanophotonic interconnects. Through this research, we seek to offer ideas that can propel the field of photonic interconnects toward more efficient and high-performance technologies, aligning with the growing demands of

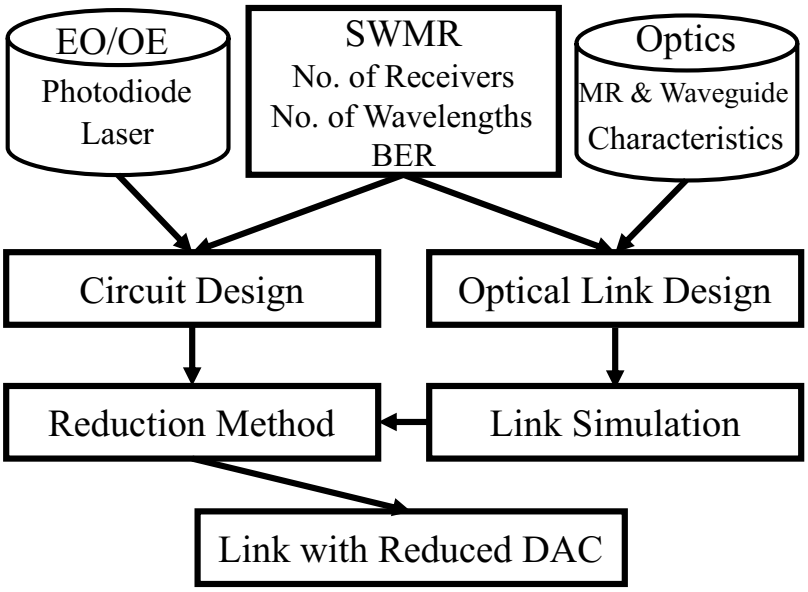


Figure 1.1: Design flow of an optical link.

the digital era.

1.5 Thesis Organization

The rest of this thesis is organized as follows: in Chapter 2, a literature review of optical devices and circuits is presented. Subsequently, to present the three state-of-the-art algorithms and architectures, three papers are reviewed and discussed in detail.

In Chapter 3, we propose a receiver reconfigurable optical link. The proposed circuits are explained, and an analytical model to configure the receivers is proposed. Circuit and system simulations are presented and discussed at the end.

Chapter 4 presents a method to reduce the design complexity of optical links, which are transmitter and receiver reconfigurable. A design flow and reduction method is used to improve the design of such links. Lastly, Chapter 5 summarizes the thesis and outlines potential future research directions.

Chapter 2

Silicon Photonic Interconnects

In this chapter, first, the silicon photonics devices are introduced. Then, optical links, receiver, and transmitter circuits are presented. At last, state-of-the-art architectures and algorithms are discussed.

2.1 Silicon Photonics

Among technology candidates to replace electrical interconnects, silicon photonics has developed thanks to compatibility with the CMOS manufacturing process. Recent prototypes demonstrate promising results in bandwidth and cost-effectiveness [13]. With recent advancements in Silicon photonics, the optical I/O technology shown in Figure 2.1 (a) has evolved from conventional pluggable to optics co-packaged with high-performance SoCs. As the optics move closer to the SoCs, the electrical I/Os get denser and more energy efficient. Optical links are well suited to realize the in-package optical/electrical (O/E) chiplets, as shown in Fig. 2.1 (b). Short-distance optical I/O channels are typically fiber-based waveguides. These optical channels offer Much lower path loss and crosstalk, are less frequency dependent, and are relatively smaller than the electrical traces.

At the fabrication level, significant research efforts have been conducted to improve

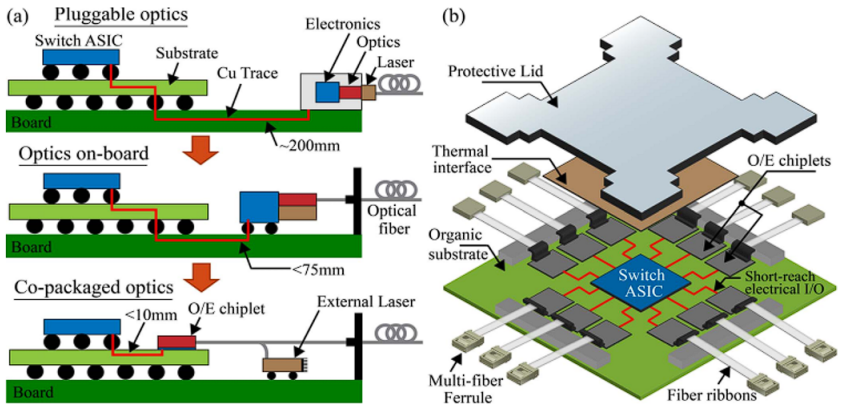


Figure 2.1: (a) Evolution of optical I/O technology (b) Switch ASIC copackaged with optical I/O chiplets [1].

the efficiency of key optical devices such as lasers, microring resonators, and photodetectors. For instance, bandgap materials have been used to improve the efficiency of on-chip lasers [14]. Reduction of waveguide propagation losses [15], [16], and microrings resonator losses were obtained by optimizing the shape and size of deposited material and by adding steps in the fabrication process. Finally, using different materials in multiple layers during fabrication allowed significant improvement of the photodiode's responsivity and capacitance [17].

A waveguide is a physical structure that confines and guides electromagnetic waves, such as light, along a particular path within it. Optical waveguides are specifically designed to confine and guide light, allowing it to propagate while minimizing losses. As shown in Fig. 2.2(a) [2]. Planar Waveguides are the most common waveguides used in integrated photonics. Planar waveguides consist of thin, flat layers of dielectric materials, often silicon or silicon dioxide, with lower refractive indices cladded by materials with higher refractive indices. Light is confined and guided within the planar layers. Waveguides can introduce optical losses due to absorption and scattering, which should be minimized for efficient light transmission.

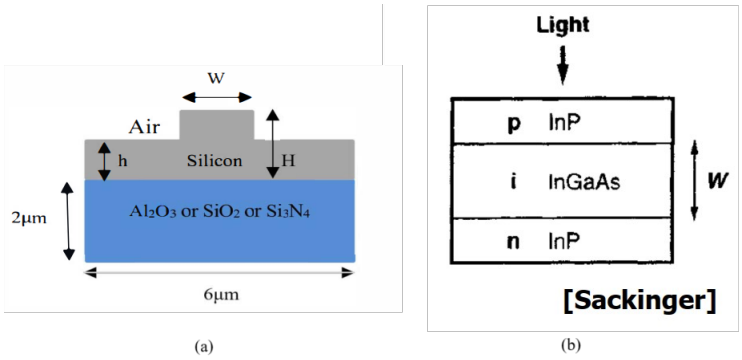


Figure 2.2: (a) Rib waveguide [2] (b) Diode structure [3].

A photodetector is an optoelectronic device that converts incident light into current and is depicted in Fig 2.2(b). Responsivity is the ratio of the generated output current to the input optical power. Maximizing responsivity is a primary goal when designing high-performance photodetectors around 1 A/W Bandwidth, which is limited by photodetector intrinsic capacitance. There is a trade-off between efficiency and speed set by the intrinsic layer width W. A wider W allows for higher optical efficiency but results in longer carrier transit times, reducing the detector bandwidth [3].

$$I_{PIN} = \eta \times \frac{\lambda q}{hc} \times P = \ R \times P \tag{2.1}$$

Micro Ring Resonators (MRRs) are an essential component in the field of integrated photonics and optical communication. They are small, circular waveguides that are used to filter and manipulate specific wavelengths of light utilizing voltage and temperature. Light is coupled into and out of the MRR through straight waveguides that connect to the ring. When the optical path length around the ring is an integer multiple of the wavelength of light, constructive interference occurs, and light of that particular wavelength resonates within the ring. Fig. 2.3(a) shows periodic wavelengths that transmit through the MRR [4]. All other wavelengths are largely canceled out by destructive interference. Fig. 2.3(b)

depicts the effect of temperature to adjust the transmitted wavelength [5].

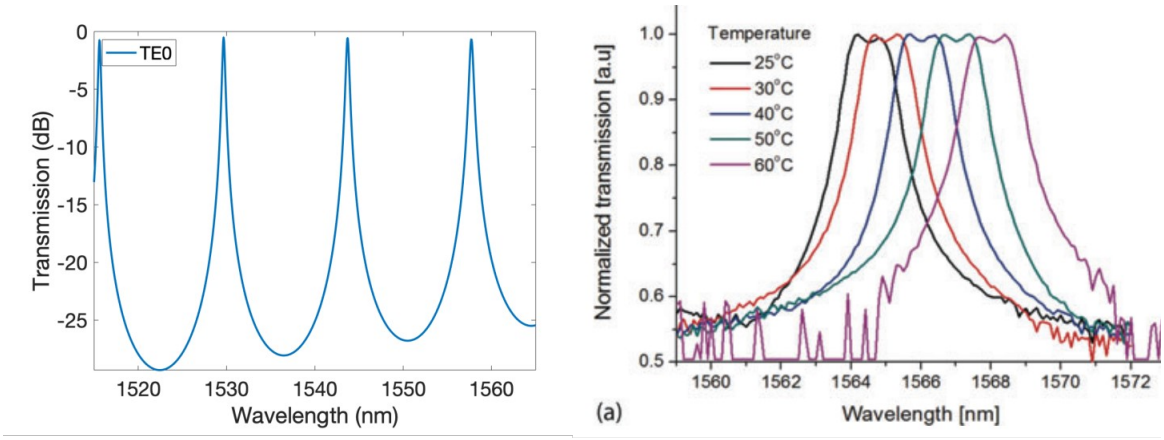


Figure 2.3: (a) Microring transmission for multiple wavelengths [4] (b) Tuning the transmission wavelength by adjusting the temperature [5].

Fig. 2.4 shows a conventional silicon photonic link. Due to its narrow frequency (wavelength) spectrum, a single longitudinal mode (SLM) laser source generates a continuous optical wave directed to a waveguide through a grating coupler. Microring resonators (MRR), which can be used as modulators and filters, are implemented on both the transmitter and receiver sides. Driver circuits control the MRRs to modulate the input data into the optical signals by employing, for instance, on-off keying (OOK) modulation. The following sections elaborate on the modulation methods and MRRs in more detail. Modulated optical signals propagate until they reach their destination. MRR filters are tuned to the wavelength of the optical signal, opt for the signal, and transmit it to a photodiode. The photodiode generates a photocurrent, which is steered into a transimpedance amplifier (TIA) to be amplified and converted to a voltage. After sufficient amplification, a comparator decodes the signal, and data is extracted [18].

One way to increase the bandwidth density is to multiplex multiple wavelengths to transmit independent information, as shown in Fig. 1.4. This is called wavelength-division multiplexing (WDM), which allows efficient use of the several THz bandwidths of the

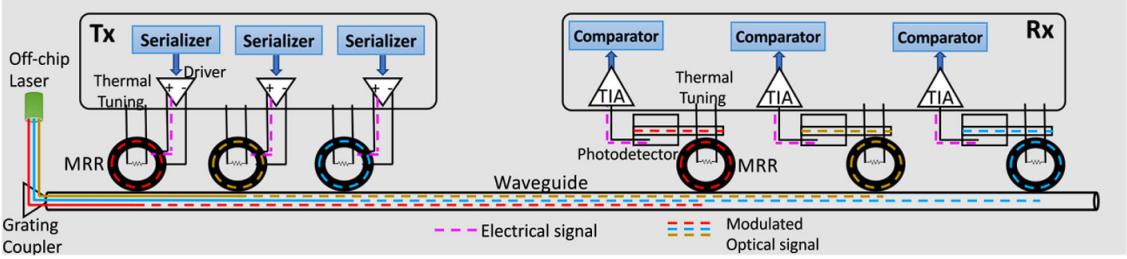


Figure 2.4: An example of silicon-photonic link [6]

optical fiber with many wavelengths independently modulated at 10s of Gbps.

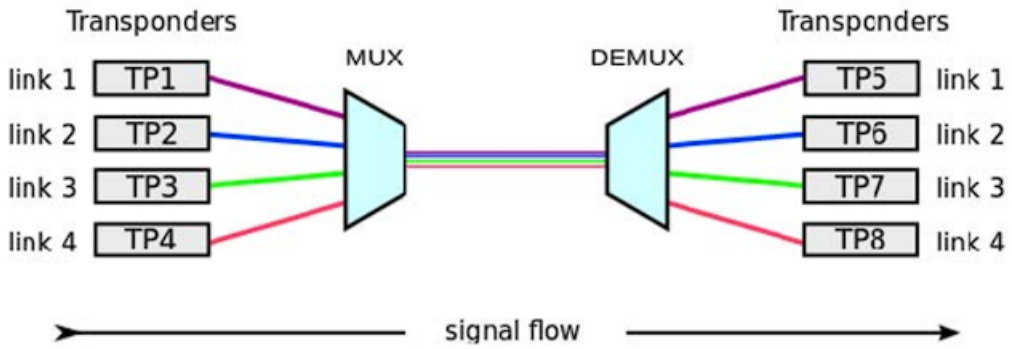


Figure 2.5: WDM concept [7]

Various solutions at the circuit and system are proposed to improve the efficiencies of nanophotonic interconnects. At the circuit level, low input-referred noise circuits utilizing the BiCMOS process [19] are proposed to increase the sensitivity of the receivers. In [20], a laser driver with RC load is designed to reduce power consumption and mitigate package parasitic. This design has led to a 13% increase in the eye diagram amplitude. In [21], a trade-off between the receiver's gain and the receiver's power consumption is utilized to decrease the optical link power consumption by up to 10%. High-power integrated lasers are fabricated in [22], achieving low power consumption and efficiency up to 20% for low temperatures.

At the fabrication level, significant research efforts have been conducted to improve

the efficiency of key optical devices such as lasers, microring resonators, and photodetectors. For instance, bandgap materials have been used to improve the efficiency of on-chip lasers and [23]. The reduction of waveguide propagation losses [24], [9] and microrings resonators losses [25] were obtained by optimizing the shape and size of deposited material and by adding steps in the fabrication process. Finally, using different materials in the multiple layers fabrication process allowed significant improvement of the photodiode's responsivity and capacitance [26]. The reconfigurability feature of the proposed receiver ideally complements device-level progress since it allows adapting to the evolution of silicon photonic platforms.

2.2 Network on Chip (NoC) and Approximate Communications

Based on the explained concepts, optical Network-on-Chip (NoC), a chip composed of tens of cores communicating with optical links, appears as an efficient multicore architecture. Since electrical NoCs suffer from scalability in terms of latency and energy due to a considerable increase in hops between cores. Optical NoC is a promising solution to overcome bandwidth and latency issues, as optical signals propagate near speed-of-light in waveguides. However, their implementations remain challenging due to the low efficiency of the lasers, which are key devices in such interconnects. Many new data-intensive applications, including machine learning (ML), pattern recognition, image processing, and big data analytics, can tolerate errors with acceptable accuracy. Approximate computing has emerged as an appealing technique for extracting the benefits of these applications' error-resilient nature by trading off calculation precision for performance and energy efficiency gains. We may use the same approximate computing notion in communication by estimating the communication data needed for computation between compute nodes. For example,

by increasing the BER of the communication link, the power consumption of transferring data can be reduced without degrading the performance. There are various approximate computing implementations, such as reducing the power levels on the transmitter or receiver sides for error-tolerable portions of data [27].

At the system level, wavelength selection based on the application required bandwidth has been exploited with minimal performance loss. In [28], phase change materials (PCMs) are deployed as switching elements on the runtime traffic photonic inter-chiplets to improve the overall network congestion. With 2.5D chiplet technology, up to 25% power reduction and 35% lower latency were achieved. In [29], a distance-aware optical link is proposed, which utilizes the laser optical power based on the receiver's distance from the transmitter and required BER, to reduce the link power consumption. Compared to [30], this thesis analyses both the receiver and transmitter configurations and calculates the optimum one for each receiver. In [6], the bandwidth needed to execute an application is utilized to activate and deactivate lasers dynamically. It involves a policy to select minimum laser wavelength, which requires forecasting bandwidth needs. The authors in [29] proposed to tune the laser power according to the communication distance and the required data precision. For long-range communication, the losses experienced by the optical signals are compensated with a higher laser output power. Compared to this approach, we aim to reduce power consumption by focusing on the receiver and transmitter. The proposed circuits allow configuring the gain according to the received optical power, thus reducing the power consumption while reaching the required BER. Our approach is complementary to existing solutions aiming at overcoming the thermal sensitivity of optical devices, such as the approach proposed in [31] to distribute data traffic. With the growing bandwidth needs, equalization circuits can be accompanied by low bandwidth TIAs to achieve high speeds without decreasing the noise performance. Techniques such as duobinary sampling [32] that employs multiple comparators and double sampling [33], which compares consecutive

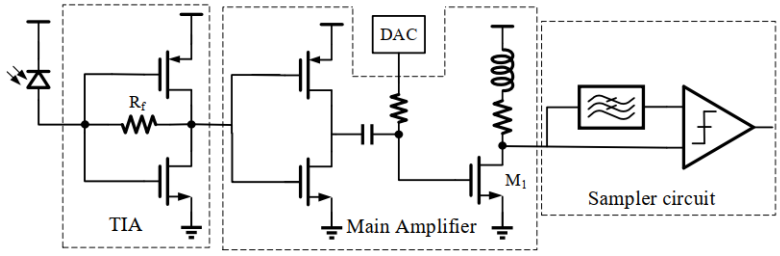


Figure 2.6: Conventional receiver circuit

samples to resolve the data, improve the power efficiency of the receivers.

2.3 Transmitter and Receiver Circuits

A conventional receiver circuit is depicted in Fig. 2.6. It is composed of a high bandwidth Trans Impedance Amplifier (TIA), the Main Amplifier (MA), a digital to analog converter (DAC), and a sampler circuit.

The TIA is composed of an inverter with resistive feedback, which is known to be scalable and low-power [34]. The photocurrent generated by the photodiode is linearly proportional to the optical power and is steered into the TIA for amplification and conversion into voltage. After the second stage of amplification by the main amplifier, a decision circuit compares the signal with a DC voltage obtained from a low pass filter to determine if the received signal is 0 or 1 [16]. The main amplifier consists of inverter-based and common source (CS) stages. An inductor in series with a resistor is used for the load of the CS amplifier to enhance the high-frequency gain and extend the bandwidth. The inductor has low quality factor to spread its effect through the bandwidth of the receiver [35]. The TIA and the first stage of the main amplifier are self-biased; thus, their power consumption and gain are constant. However, the bias voltage of the CS stage is controlled by a DAC, and therefore, the power consumption of this stage changes depending on the bias voltage. By adjusting the bias voltage of M_1, a trade-off between the total gain of the receiver and its

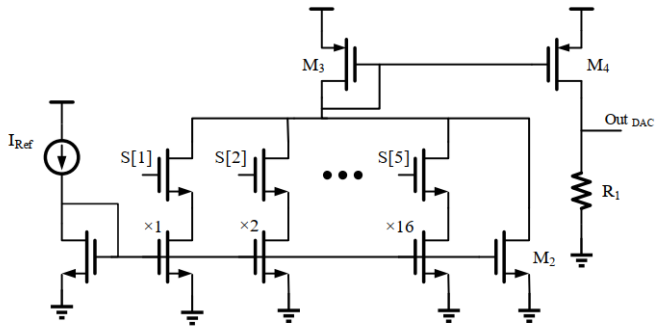


Figure 2.7: DAC circuit.

consumption power is established.

As illustrated in Fig. 2.7, the DAC is based on a current steering architecture [34] controlled by a number of input bits. Transistor M_2 generates a current that ensures the minimum bias voltage. The N bits generate 2^n voltage levels that control the M_1 transistor. Each bit controls a transistor and hence the current contribution from the weighted current mirrors. The accumulated currents of M_2 and other branches are mirrored through M_3 and M_4, and by passing through R_1, they generate the desired bias voltage to control M_1. For all control bits set to 0 (i.e., configuration '00000'), the DAC output voltage is the lowest, which leads to the least gain but also the least power consumption. The gain is the highest when all bits are set to 1 (i.e., configuration '11111'), resulting in the highest power consumption. The receiver circuit is designed to reach the targeted BER on the last reader for configuration '11111'. Indeed, the last receiver requires the highest gain since it receives the lowest optical power.

2.4 Laser-Forwarded Coherent Transceiver

2.4.1 Transceiver Architecture

This section presents a Binary Phase Shift Keying (BPSK) modulation integrated into the optical links. At first, the shortcomings of the Intensity Modulation/Direct Detection (IMDD) links are explored. As shown in Fig.2.8, for a receiver with a sensitivity of 75 µA and responsivity of 0.5 A/W, the laser power should be at least 7.5 mW, which is 50 times the required receiver power. This leads to the high power consumption of the laser, which is power inefficient. Therefore, novel architectures are required to reduce the power consumption of the laser or avoid path loss of the links.

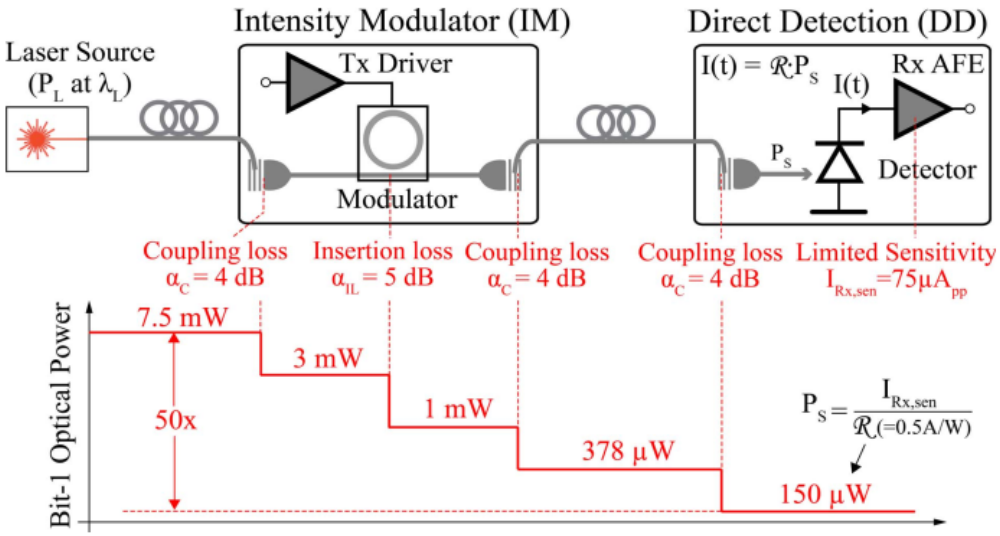


Figure 2.8: Conventional IMDD link with optical path loss [1].

This section introduces a laser-forwarded (LF) coherent link architecture, depicted in Fig. 2.9. The laser power is split into two paths, each containing half of the laser power. The signal path is modulated by phase and experiences a significant power loss by passing through three couplers and one modulator. However, the LO path has lower path loss and can transfer more laser power to the receiver's end, increasing the SNR of the signal. A

3-dB coupler is utilized at the receiver side, which combines the P_S and P_{LO} and splits them into P_1 and P_2. Then, two Photodetectors are used to convert the optical powers into the currents. Next, the difference current between I_1 and I_2 flows to the receiver's analog front end (AFE) to be amplified and decoded to retain the data. Each part of the architecture will be explained and discussed in the upcoming sections.

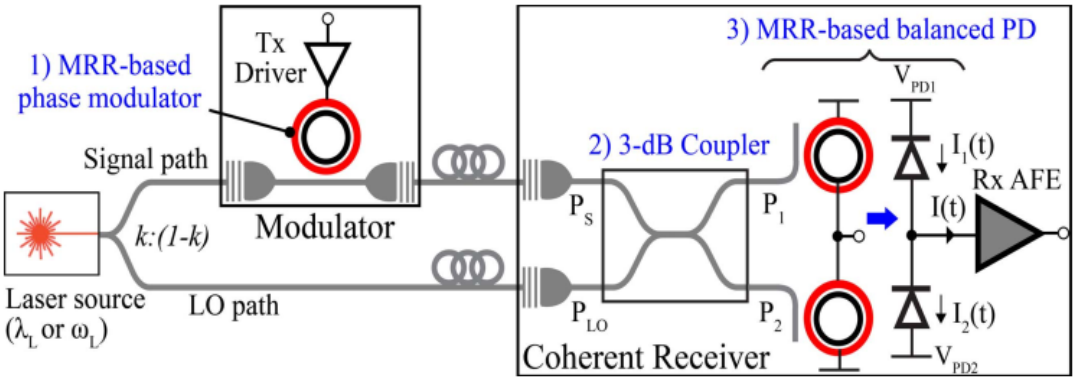


Figure 2.9: MRR-based LF coherent link concept [1].

By employing one photodetector, as shown in Fig. 2.10 (a) receiver can only detect the amplitude of the illuminated light, which is in the form of (2.2), and information encoded in phase is lost. A 3-dB coupler in conjunction with a balanced PD can solve this problem, and data can be extracted.

As seen in Fig. 2.10(b), S presents the signal, and LO, which is in the form of equation (2.3), presents the unmodulated signal light emitted from the laser source. A 3-dB coupler combines S and LO and outputs P_1 and P_2, which have a 180^o phase difference between them. The optical power of P_1 and P_2 are shown in equation (2.4). The differential current between the two generated currents is calculated in equation (2.5). Compared to a conventional solution (Fig 2.10(a)) for the same link components, this solution has a current gain of 9. This rises from the fact that the optical power of both paths contributes equally to the generated current, and the LO path experiences much lower path loss and can transfer

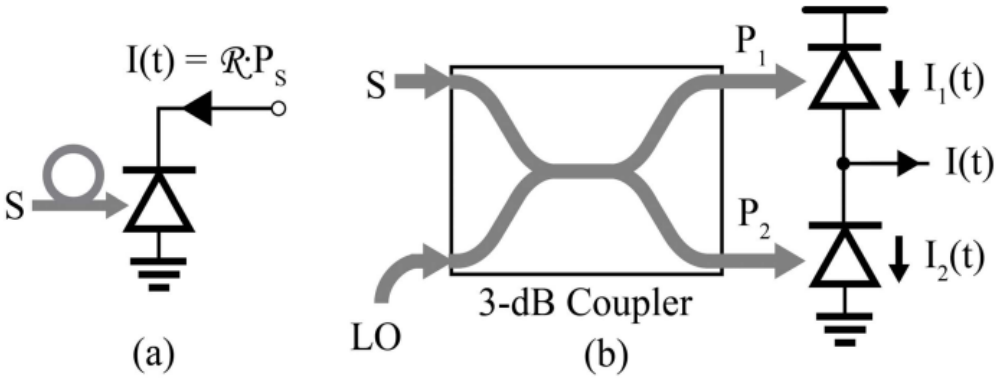


Figure 2.10: (a) Direct detection. (b) Coherent balanced detection [1].

more optical power to the receiver side. The created gain improves the SNR, and thus for the same receiver sensitivity reduces the laser power and the optical link.

$$S = \sqrt{P_S} e^{j(w_L t + \emptyset_{in}(t))} \tag{2.2}$$

$$LO = \sqrt{P_{LO}} e^{j w_L t} \tag{2.3}$$

$$P_1 = \frac{(S + LO)^2}{2} \quad and \quad P_2 = \frac{(S - LO)^2}{2} \tag{2.4}$$

$$I\left(t\right) = I_1\left(t\right) I_2\left(t\right) = 2R\sqrt{P_S P_{LO}} \tag{2.5}$$

Fig. 2.11 (a) shows a setup that compares photocurrent generated in an IMDD and an LF coherent link. The peak current of the IMDD link is 18 μA which is less than the LF link, which can generate up to 45 μA current. Due to the laser's accumulated phase noise, fluctuations in the balanced PD photocurrent can be seen. The phase shift limits the discussed gain from 9 to 5. Due to the path-length mismatch, the phase noise affects

the BER in time. Therefore, the BER is measured in time intervals. The best achieved BER is 10-9, which requires path length compensation; otherwise, the link has a low BER reaching zero at times, which makes the link unusable. Fig. 2.11 (b) breaks down the energy consumption of the LF link in which the DPLL consumes the most power as it is designed to support higher data rates. The link operates with 4 dBm laser power, and the receiver's sensitivity is -15.6 dBm.

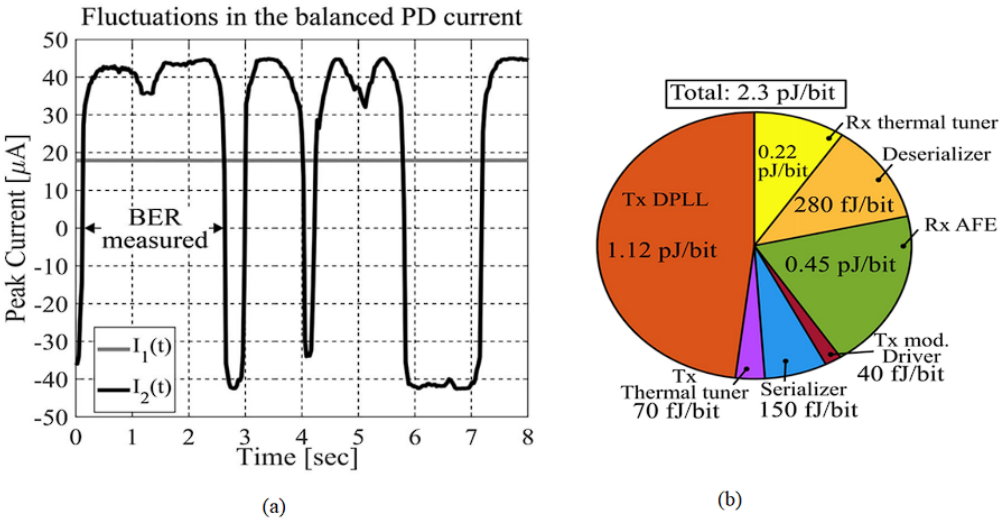


Figure 2.11: (a) Comparison of generated current under no modulation (b) Electrical energy efficiency breakdown [1].

Overall, this architecture requires the two paths to be at the same length to cancel the phase noise of the laser, which limits the layout design and implementation. Multiple waveguides are required to scale and expand this work from point to point to SWMR. Because each receiver has a different distance from the transmitter, and equal path lengths are required for correct transmission. Furthermore, in practice, the two photodiodes do not have the same characteristics, which can induce noise to the differential current and degrade the SNR of the link.

In summary, the feasibility of phase modulation can lead to the combination of amplitude and phase modulation, which can increase the speed of the link. This goal requires

modifications and innovations in optical link architectures to be achievable. Various noise sources and path length mismatches can reduce the BER and quality of the link and make it impractical. The section presents a compact form of the transceiver in which the MRRs are controlled at each side without performance degradation and adding noticeable power consumption.

2.4.2 Phase Modulator and Coherent Balanced Detector

By interleaving p-n junction phase shifters along the circular MRR cavity and driving each segment independently, an MRR based O-DAC can be formed, which is depicted in Fig. 2.12 (a). This modulator is controlled by 16 drivers, which can tune the transmission wavelength. As shown in Fig. 2.12 (b), control codes 2 and 15 have the same transmission amplitude but differ in phase by 180°. The characteristics of these two codes enable us to modulate the signal only in phase without affecting the amplitude.

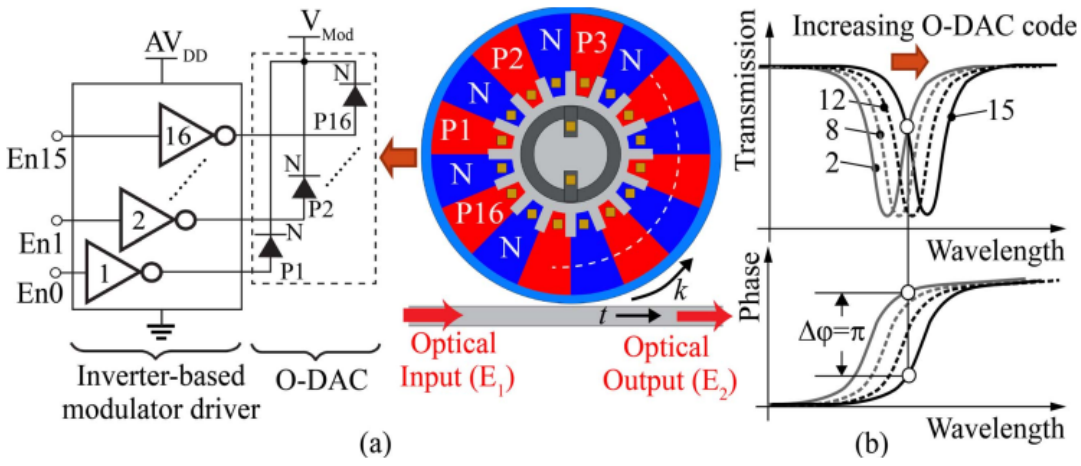


Figure 2.12: (a) MRR-based O-DAC. (b) Phase shift with O-DAC code [1].

2.5 Wavelength Selection for Photonic NoCs

This section focuses on the laser sources and by predicting the needed bandwidth for each application, selectively deactivates laser wavelengths. Utilizing lower bandwidth demand can alleviate high PNoC power consumption. ARIMA, an autoregressive model is used to predict the average latency of transferred packets.

2.5.1 Network On Chip Architecture

As shown in Fig. 2.13, the narrowband wavelength of an MRR can be used for the modulation and filtering of optical signals. An MRR utilizes a constructive interference phenomenon to resonate with the laser wavelength. The parameters used to characterize an MMR are the free-spectral range (FSR), full width at half maximum (FWHM), and the peak transmissions at resonance.

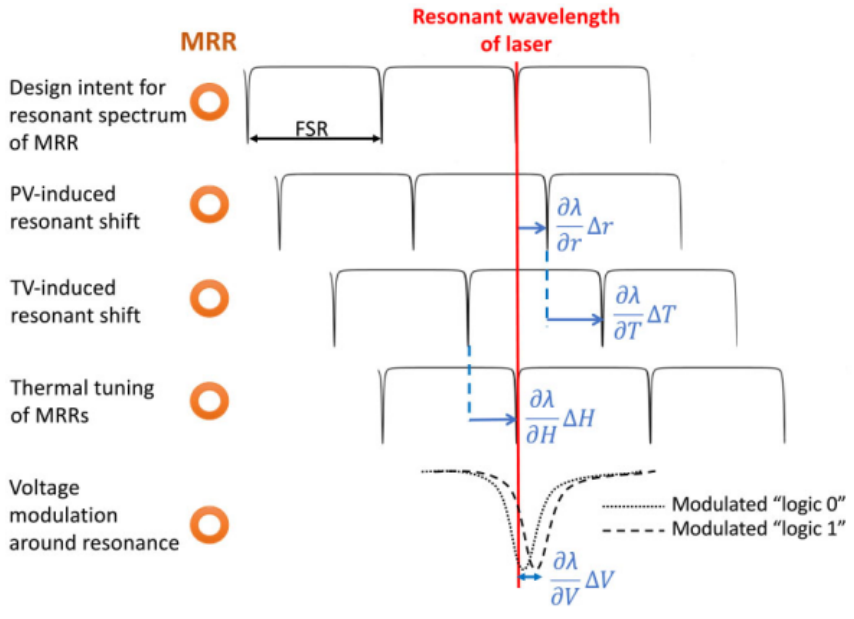


Figure 2.13: Designing MRRs to work at wavelength of the laser [6].

The nonidealities associated with the CMOS fabrication process introduce variations in

the thickness and width of the MRRs, leading to shifts in the MRR resonant wavelengths. Furthermore, the high thermo-optic coefficient of Si makes the MRRs sensitive to temperature. These TVs are not only temporal but also spatial. Therefore, MRRs on the interposer can experience TV-induced resonance shifts between a completely cold state and peak activity, and distant MRRs can shift very differently depending on local activity. The MRRs can be thermally tuned by controlled local heat injection to compensate for the PV and TV-induced resonant shifts. Thermal tuning is conventionally done via the Joule effect using resistive heaters. It is possible to reduce the wavelength shift required for an MRR using WDM. The maximum resonance shift required for any MRR to tune to the nearest laser wavelength is FSR/n if N laser sources are used with resonant wavelengths evenly distributed within the FSR of an MRR.

As shown in Fig. 2.14 (a), a 2.5-D system is targeted to implement the architecture due to its cost reduction and higher yield. The system consists of 96 cores Within six compute chiplets and eight (C = 8) TxRx chiplets integrated on a photonic interposer. The chiplets can communicate with each other and IOs through TxRx chiplets. For each Tx MRR, there is a serializer and a modulation driver. Additionally, for each Rx MRR, there is a filter bias, a TIA, and a comparator.

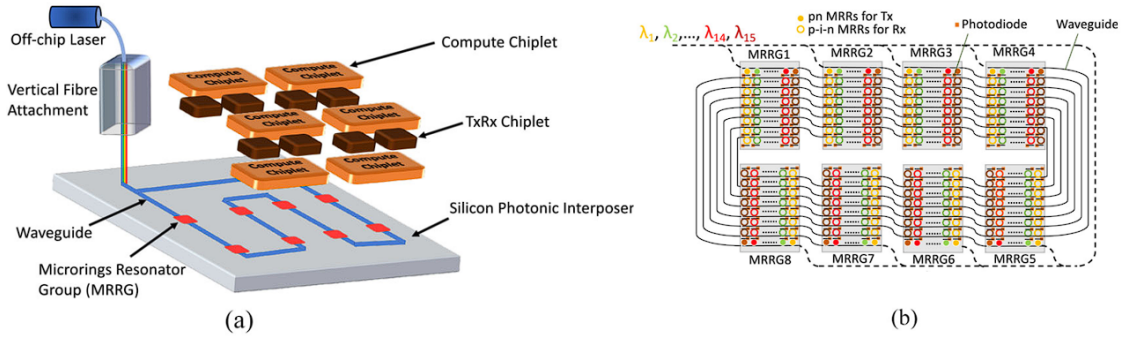


Figure 2.14: 2.5-D manycore system (b) PNoC topology and MRRG assignment [6].

The system utilizes 16 laser wavelengths (λ_{tot}) and activates them based on the required

bandwidth. Each optical link connects a chiplet wavelength to 7 other chiplets. This results in an aggregate of 16 Tx MRRs and (7×16) 112 Rx MRRs in each chiplet. Equation (2.6) calculates the overall wavelength shift ($\Delta\lambda_{\text{shift}}$) for an MRR, where T is the difference between the MRRG temperature and the ambient temperature,($\Delta\lambda_{\text{shift}}$) and shift, PV is the PV-induced wavelength shift. The power of drivers and serializers (in two states: active and idle) are included in the transmitter power. The receiver's power consists of the power of TIA and comparator (active and idle) power. The arbitration and flow control block also consumes power in active and idle modes. Hence, the overall electrical to power to electrical (EOE) power consumption can be computed as equation (2.7).

$$\Delta\lambda_{shift} = \frac{d\lambda}{dT} .\Delta\mathrm{T} + \Delta\lambda_{shift,PV} \tag{2.6}$$

$$P_{EOE} = C.\left(P_{Tx} + P_{Rx} + P_{arb}\right) \tag{2.7}$$

The total required heating power, P_{heat}, in equation (2.9), can be calculated by aggregating the heating power of the active MRRs over all chiplets, where $\Delta\lambda_{\text{heat}}$ in equation (2.8) is the required wavelength shift to the nearest laser wavelength for an MRR.

$$\Delta\lambda_{heat} = \frac{FSR}{\lambda_{tot}} - \left(\Delta\lambda_{shift}\ mod\ \frac{FSR}{\lambda_{tot}}\right) \tag{2.8}$$

$$P_{heat} = \sum_{i=1}^{C} \sum_{r=1}^{C.\lambda_{act}} \frac{\Delta\lambda_{heat_{ir}}}{\frac{d\lambda}{dH}} \tag{2.9}$$

2.5.2 Simulation Framework

As shown in Fig. 2.15, the targeted applications are simulated in the Sniper simulator [36] for a region of interest (ROI) of 10 billion instructions. The performance traces, such

as the number of packets transferred in the PNoC, and total queue delay, were collected in intervals of 100 million instructions. These performance statistics are fed to McPAT [33] to estimate the average power consumption of the processors. Using the logic power and TxRx power as an input of HotSpot 3D [34], the MRRs temperature is estimated, and thermal tuning power is extracted.

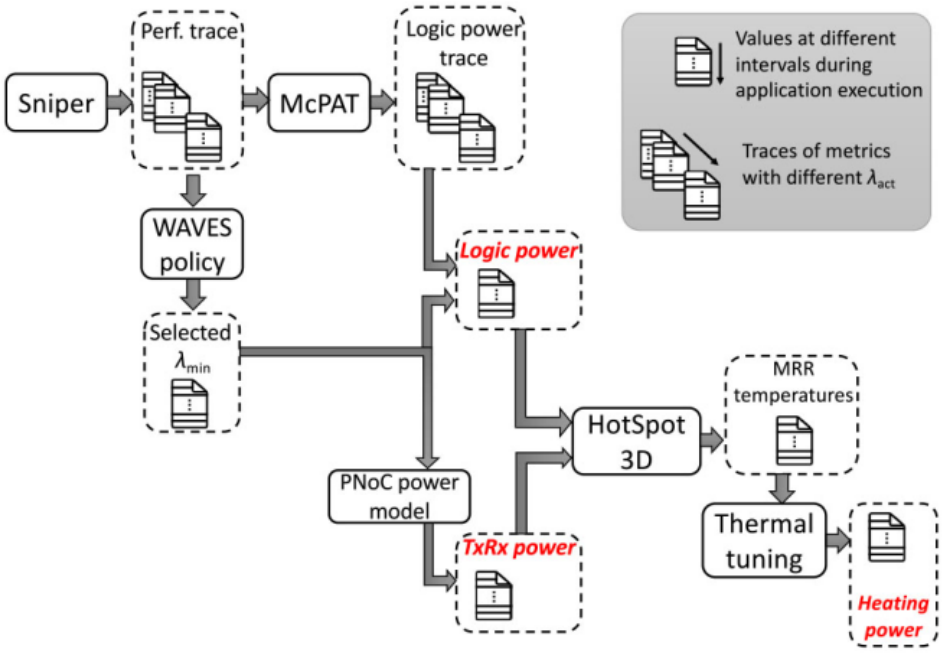


Figure 2.15: Simulation framework for modeling performance, power, and temperature, and performing wavelength selection [6].

An indicator called average packet latency (Lat_{avg}) is used to activate the minimum number of laser wavelengths. Lat_{avg} is the aggregate queue latency of all packets divided by the total number of interchiplet transferred packets computed for each interval. A time series predictor called ARIMA is used to forecast the Lat_{avg} and select minimum laser wavelengths (λ_{min}) based on that. ARIMA consists of two parts, an autoregression model (AR) forecasting the variable using a linear combination of past values of the variable and a moving average model (MA), which uses past forecast errors in a regression-like

model. As shown in Fig. 2.16, after 30 intervals, an ARIMA model is built, which predicts the Lat_{avg}. Then, in each interval, the real and predicted Lat_{avg} are compared with Kolmogorov–Smirnov (K–S) [35] test. If the test fails, the current ARIMA model is not suitable for time-series forecasting, and a new one should be built.

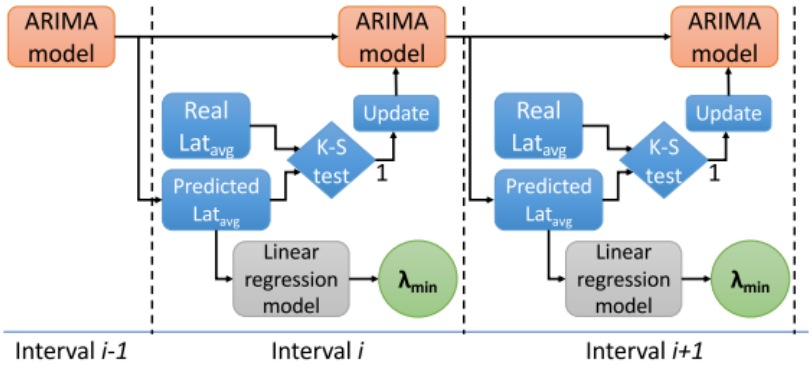


Figure 2.16: Flow of PROWAVES [6].

Fig. 2.17 shows the different components contributing to the latency overhead of wavelength selection. When λ_{min} is increased, the latency comprises of the laser power-on latency and the thermal remapping of the new WDM group of MRRs to the activated laser wavelengths. When λ_{min} is decreased, the next application interval requires the deactivation of certain laser sources without thermal remapping of the MRRs.

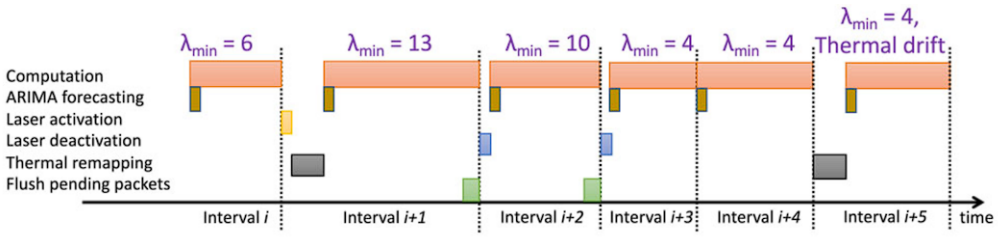


Figure 2.17: Latency overhead of PROWAVES [6].

Since laser sources are power inefficient, optimizing their activation time can reduce the overall power consumption. This goal was achieved by predicting the average latency

of transferred packets and controlling the laser sources based on that. This work can be expanded for other applications, and other time-series predictors can be implemented to improve the results.

As discussed, this section introduces overhead time and increases the execution time of the applications. Furthermore, the reduction of PNoC power is minimal for some applications. Hence, the saved energy consumption per bit can be minimal compared to the baseline system. The section focuses on specific applications with a constant trend for Lat_{avg}. This approach limits the paper's scope to specific applications with static average bandwidth needs. Applications with user inputs have unpredictable bandwidth requirements, so this method is not helpful in reducing power consumption. Lastly, the proposed method does not improve the PNoC power consumption for some specified applications, which calls for other time-series predictors or indicators.

2.6 Low-power Approximate Network on Chips

This section presents an approximate dual-voltage router for Network on Chips (NoCs) called AxNoC. Perfect data transfer is secured by employing a high voltage to transmit critical data such as header flits. For other error-tolerant flits, a lower voltage is utilized, leading to the reduction of power consumption. On the other hand, a higher BER for these flits is inevitable, making this approach application-specific. It is calculated that reducing the voltage by 0.1V increases the BER by 100×. Hence, the high and low voltages are 1.1 and 0.7 V, respectively, which leads to BERs of 10^{-12} and 10^{-5}.

2.6.1 AxNoC Router

Fig. 2.17 depicts the proposed architecture of AxNoC. Compared to a conventional router, Voltage Switches (VS) and Level Shifters (LS) are added to implement the dual

voltage. Also, a look ahead per flit method is needed to control the data path voltage and prevent performance degradation. Voltage selection for each of the five physical channels is independent of the others, called the Fine-Grained Variable Vdd (FG-VV) method [8]. Additionally, the crossbar in this router is merged with each output channel to simplify the voltage control signals. A power controller to manipulate the added circuits is required as well.

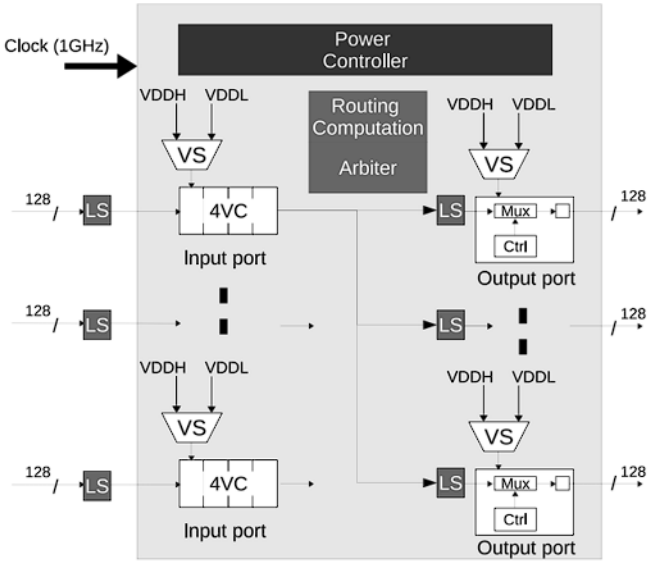


Figure 2.18: AxNoC router architecture [8].

Switching the supply voltage creates an inevitable delay, which at least would take one cycle. To reduce the performance overhead, a look-ahead wake-up method is implemented [37]. As depicted in Fig. 2.19, a packet with a critical head flit followed by three error-tolerable data flits is sent from router A to router C. The head flit, which is transferred through three cycles, consists of Next Route Computation (NRC) and Virtual channel / Switch Allocation (VSA), Switch Traversal (ST), and Link Traversal (LT). When the receiver router receives the NRC/VSA flit, it decodes the flit and specifies the number of approximate incoming flits. According to that, the voltage of the router is configured, and no performance degradation occurs. The high-to-low voltage transition in an upstream node

must be conducted at the same time as the low-to-high voltage change in the corresponding downstream node because the voltage transition is initiated by the upstream router one cycle before the HEAD flit arrives at the downstream router. . As shown in Fig. 2.20(a), as

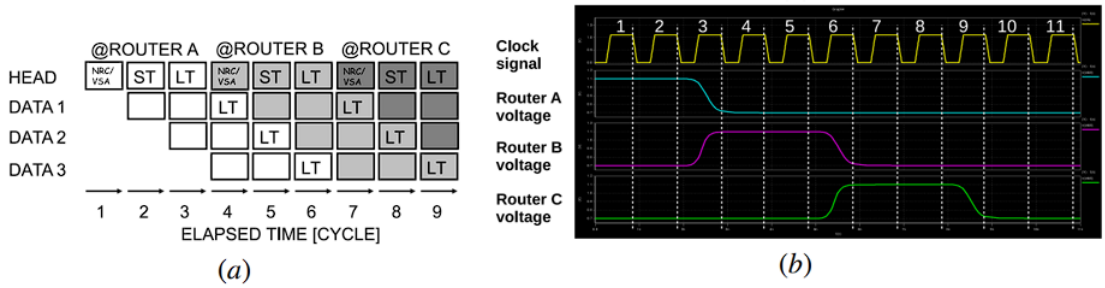
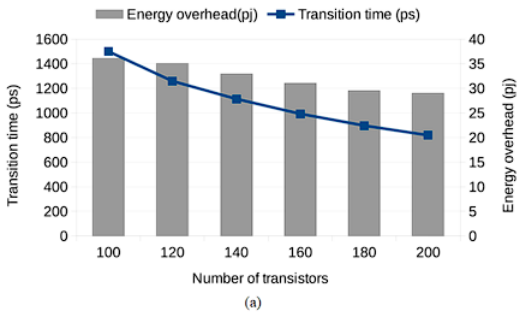


Figure 2.19: Look-ahead voltage transition: (a) timing diagram (b) waveform snapshot [8].

the number of transistors for a low to high-voltage circuit increases, the transition time and energy consumption decrease. Since the working frequency used is 1 GHz, 160 transistors are utilized, which adds up to the 10 transistors used for a high to low-voltage circuit. The total area of each block is shown in Fig. 2.20 (b), in which the added blocks add 6% to the overall area.



	Router	Level shifter	Voltage Sw.	Total
Baseline	852846	0	0	852846
AxNoC	906249	1948.44	534.06	908740.5

(b)

Figure 2.20: (a) Low-to-high voltage transition latency and energy overhead for a single input-port (b) Total area of transistors [µm2] [8].

The energy overhead for a pair voltage transition for an input and output channel is 36.8 pJ. A Break-Even Time (BET) is the minimum time that the router should remain in the low voltage to compensate for the transition energy overhead. The calculated BET

for this router is evaluated to be 23 cycles. However, in rare situations, such as when two critical flits arrive at a router within the BET period of 23 cycles, the power transition would diminish the benefits. Compared to the baseline router, the proposed one only incurs 6.15% additional area overhead. Fig. 2.21 (a) shows the power breakdown and amount of approximation technique that applications utilize. The amount of power consumed by approximate communication varies from one application to another. This variation is highly dependent on the percentage of approximate data, which is represented by the blue line in Fig.2.21. Power saving obtained with AxNoC is around 1% for Canneal and can reach up to 43% with Sobel.

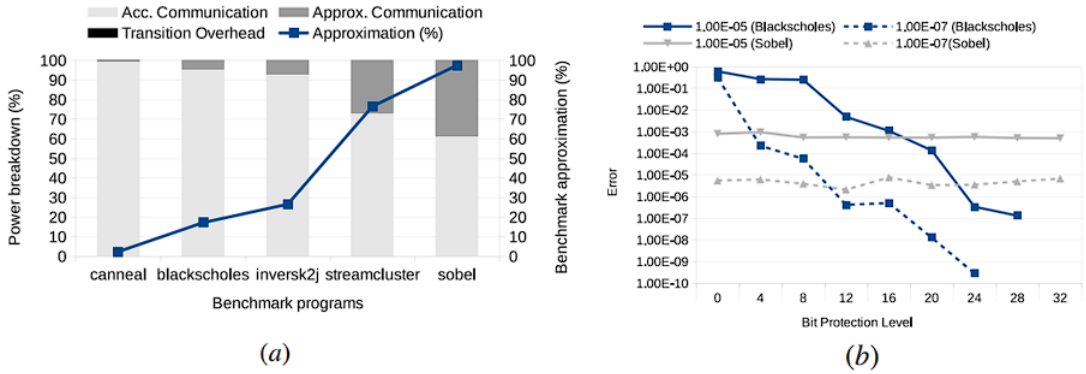


Figure 2.21: (a) AxNoC power consumption breakdown for different programs (b) generated errors vs bit protection level [8].

Fig. 2.21 (b) depicts the resulting errors based on bit protection levels for 10^{-5} and 10^{-7} BERs. The number of bits that are approximated can affect the quality of results of applications such as Blackscholes. But for applications like Sobel, the number of bits that can be approximated can be increased without degrading the performance.

In summary, this paper explores approximate computing ideas and presents a dual-voltage network on a chip. Power consumption can be reduced by transferring error-tolerant data with lower voltage without noticeable performance loss. This idea can be expanded into optical NoCs in different ways. The approximate technique can be applied

at the transmitter, receiver, or both sides, which is an interesting path to explore.

2.7 Summary

In this chapter, silicon photonic devices are explained individually. Then, applications of optical links, such as NOCs and Approximate communication, are explored. Next, associated optical links are explained. Three papers, each covering one area of nanophotonic interconnects, are explained and discussed. The first paper presents the Laser forwarded coherent transceiver architecture. The second paper focuses on wavelength selection methods, and the last paper studies the utilization of approximate communication in NoCs.

Chapter 3

Design of Reconfigurable Circuits for Nanophotonic Interconnects

In this chapter, first, the Proposed Receiver Reconfigurable Optical Link is presented. Then, the proposed reconfigurable circuits are explained. After the analytical model is elaborated, the simulation results are discussed.

3.1 Introduction

Nanophotonic interconnects typically consist of lasers emitting continuous optical signals at given wavelengths. As signals propagate through a waveguide, they are modulated by microring resonators using, for instance, on-off keying (OOK) modulation [38]. Modulated signals propagate until they reach their destination, where photocurrent conversion is carried out by a photodiode. At the system level, Single Writer Multiple Reader (SWMR) is one of the most popular on-chip optical communication links [32], which is a practical solution for the processor to memory communications. However, the number of readers required and the non-ideal characteristics of optical devices involve significant waveguide propagation losses and microring coupling losses [38]. Depending on the interconnect

length and the receiver's position in the link, signals can experience up to 16 dB losses [24], which calls for a transimpedance amplification to reach the targeted BER. Depending on the applications, BER can range from 10^{-12} for data centers to 10^{-3} for approximate computing [29]. For cost-effectiveness and regularity purposes, the same receiver circuit is used to design all receivers on a chip. Receivers are thus designed based on the worst-case scenario, which implies amplifying the signal experiencing the highest losses while targeting the lowest BER required. As a result, receivers account for up to 27% of optical link energy consumption [15]. The need for energy-efficient on-chip communication thus calls for disruptive solutions to adapt and reduce receiver power consumption according to the interconnect length and characteristics.

In this chapter, we propose a digitally reconfigurable receiver and transmitter for nanophotonic interconnects. The receivers closer to the transmitter take advantage of the high received optical power to decrease their gain while reaching the targeted BER. We also propose a method allowing us to configure the receivers according to their position on the link, thus minimizing the average power consumption of the receivers. Results show that the proposed reconfigurable receiver leads to up to 25% power saving on a single wavelength SWMR link.

The chapter is organized as follows. Section 3.2 presents the overview of the proposed optical link. Section 3.3 presents an interconnect based on the proposed reconfigurable receiver. The circuit and design method to configure the receivers are then explained. section 3.4 elaborates the analytical power model. We present our results in Section 3.4, and Section 3.6 concludes this chapter. 3.4

3.2 Proposed Receiver Reconfigurable Optical Link

We assume a SWMR optical link that enables communication between a writing core and N reader cores. As described in [38], such a link involves the continuous emission

of optical signals utilizing the WDM (wavelength division multiplexing) technique by using microring modulators. Each reader is composed of multiple microring filters, which correspond to the number of wavelengths. The filters resonance wavelengths are aligned with the signal's wavelengths. The signals are then transmitted toward photodetectors for photocurrent conversions. After transimpedance amplification, the signal is sampled to recover the data. Without lack of generality, we illustrate the considered optical link in Fig.

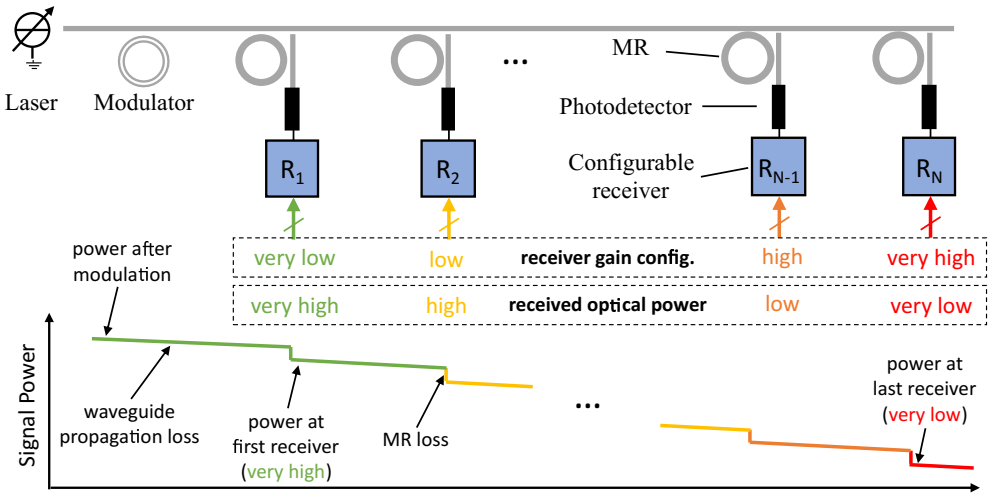


Figure 3.1: Proposed optical link utilizing a reconfigurable receiver.

3.1 for a single wavelength scenario. Typically, the laser output power is defined based on the targeted BER and the worst-case optical losses, which correspond to communication with the last receiver. Due to the waveguide propagation and microrings through and drop losses, the received optical power changes from one receiver to another. The further the destination, the lower the received optical power. Hence, compared to a receiver close to the transmitter, receivers toward the end of the link require a larger gain to reach the same BER.

To improve nanophotonic interconnect energy efficiency, we propose to adapt the receiver amplification according to the received optical power. We aim to design a reconfigurable receiver circuit for regularity and cost-efficiency purposes, which is reusable for

all the readers in the SWMR link. The gain is digitally controlled to allow reaching the targeted BER, thus reducing power consumption for the readers receiving higher optical power (i.e., readers closer to the writer).

3.3 Proposed Reconfigurable Circuits

As shown in Fig. 3.2 (a), a current steering DAC is proposed in which I_{ref} is multiplied into other branches based on the width of the corresponding transistor. The $S_{[i]}$ inputs are connected to the controller, switching the branches' current and accumulating them into M_2. The resulting current passes through the current mirror and generates the output voltage. Furthermore, an additional transistor (M_1) is added to generate the baseline voltage. A DAC with M control bits results in 2M control levels. A trade-off between the circuits' power consumption and gain of the receiver and output optical power of the transmitter is established by controlling the bias voltage. Then, as discussed in Section 3.4, the proposed method eliminates the unrequired voltage levels, reduces the number of control bits, and optimizes the DAC. This will reduce the control complexity, area, and consumption power overhead resulting from the DAC [39].

Fig. 3.2 (b) depicts the laser driver adapted from [20] in which I_{th} generates the threshold current of the laser to turn it on. The M_4 transistor, based on the input, controls the steering of current into the laser. Transistor M_3, controlled with a DAC, determines the amount of current and, hence, the optical power configuration. Because of the high voltage requirement for turning on the laser, the anode side of the laser is connected to a high positive voltage. The maximum bias voltage is selected based on the linear region of the laser [40]. This proposed reconfigurable transmitter is used in the next chapter.

Fig. 3.2 (c) shows the proposed reconfigurable receiver circuit, which consists of a high bandwidth TIA, a Main Amplifier, and a DAC that connects to a comparator circuit. The photodiode converts the received light into current and steers it into the TIA. Passing

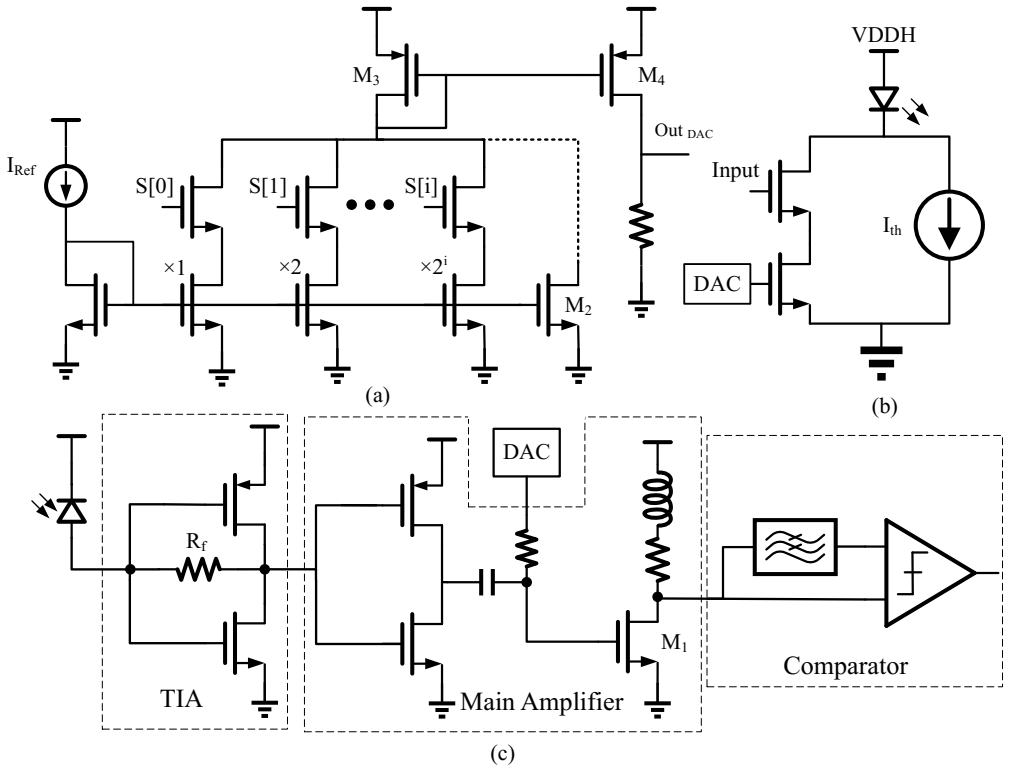


Figure 3.2: (a) DAC circuit (b) Laser driver (c) Receiver circuit.

through R_f, the signal current is amplified and converted to a voltage. The main amplifier further amplifies the signal, and implementing an inductor in its common source stage improves the circuit's bandwidth. The bias voltage of M_5 is connected to the DAC, controlling the gain and power consumption of the circuit. The minimum and maximum bias voltages are defined such that the CS stage does not attenuate the signal or enter the triode region. The DAC is implemented in the last stage of the amplifiers to have the minimum effect on the circuit noise performance [41].

Figure 3.3 depicts the comparator circuit used to determine the digital value of the signal. With the negative level of the clock, the intermediate nodes are charged through the PMOS transistors connected to the clock. There are two inverters at the top, which are connected through positive feedback. Positive feedback means that when the circuit is active, the outputs (OutP and OutN) diverge from each other to 0 or 1. When the clock goes

1st Stage	2nd Stage	Ind. Stage	Comparator	
NMOS: 25/0.18	NMOS: 40/0.18	NMOS: 45/0.18	InN: 5/0.18	OutN: 4/0.18
PMOS: 30/0.18	PMOS: 35/0.18	Inductor: 6.3nH	CLKP: 2/0.18	OutP: 6/0.18
Rf: 550 ohm		RL: 75 ohm	CLKN: 80/0.18	Vconst: 1.3 V

Table 3.1: Parameters of the receiver circuit

low, the differential outputs settle quickly based on the differential inputs (InP and InN). Because our proposed circuit is single-ended, one of the inputs is connected to a specific voltage so the circuit can work properly. A first-order RC filter implements the low pass filter, which is used to extract the DC voltage of the signal. Changing the bias voltage of M_1 leads to changes in drain DC voltage. The output voltage of the filter follows the DC voltage of the signals and ensures the correctness of the comparison. Table 3.3 shows the parameters of the receiver circuit. The sizes of transistors are shown in micrometers.

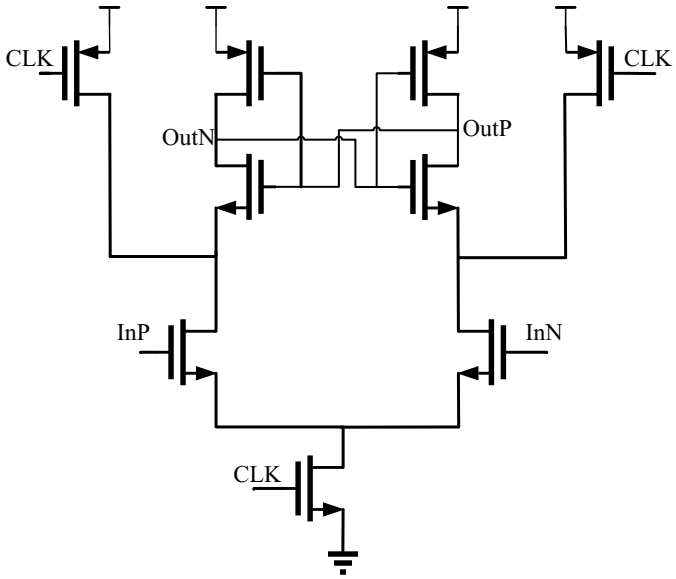


Figure 3.3: comparator circuit

Device	Parameter	Value
Laser	Efficiency	10 %
Waveguide	Insertion Loss	0.1 dB/cm
MR modulator	Through IL	3 dB
MR filter	Drop IL	2 dB
	Through IL	0.7 dB
Photodiode	Responsivity	1 A/W
	Capacitance	90 fF

Table 3.2: Optical device parameters [9], [10].

3.4 Analytical Power Model

The optical power received by a photodiode, PPD, is given by Eq. (3.1).

$$P_{PD} = P_{Laser} - (IL_{wg} \times L \times K) - (IL_{MR} \times (K-1)) - IL_{Mod} - IL_{MRsel} \quad (3.1)$$

where P_{Laser} is the optical power injected by the laser, IL_{wg} and IL_{Mod} are the insertion losses introduced by the waveguide and the modulator, IL_{MR} is the MR through loss and IL_{MRsel} is the MR drop loss. The distance between the receivers is L and K is the number of receivers. The device parameters we use in the experiments are summarized in Table 3.4.

The design method is defined as follows. First, we define a BER to be reached. Then, the sensitivity for the last receiver is determined according to the highest gain achievable by the circuit. This means that the last receiver configuration is set to '11111'. Then, for given L and K, we calculate P_{Laser} to reach the sensitivity required for the last receiver. From P_{Laser}, we estimate the received optical power for each intermediate receiver, from which individual configuration is deduced.

3.5 Results

3.5.1 Circuit Design and Analysis

The receiver has been designed and simulated using Cadence Virtuoso with 0.18 um TSMC technology. It is designed to reach a 10 Gbps data rate with a 1.8 V supply voltage. We assume a photodiode with a responsivity of 1 A/W and 90 fF input capacitance [14] and a 7 dB extinction ratio was considered for the modulator. By taking into account the input capacitance and the targeted bandwidth of 60% of the data rate (6 GHz), we set R_f to 550 ohm. Fig. 3.4 depicts the transimpedance gain of the receiver for three DAC configurations. Due to the 6.3 nH inductor used in the CS stage, we obtain a maximum gain at 2.8 GHz, which allows us to increase the bandwidth. The achieved 3 dB bandwidth is 6.2 GHz, ensuring no inter-symbol interference (ISI) occurs [16]. At 2.8 GHz, the gain ranges from 70.8 dB (config. '00000') to 78.4 dB (for '11111'), thus leading to a 7.6 dB difference.

The 32 bias voltages range from 550 mV (for config. '00000') to 750 mV (config. '11111'). Below 550 mV, transistor M_1 does not amplify the signal, and above 750 mV, the gain-bias voltage relation becomes nonlinear, and amplification above this point is not power efficient. The range of configurations leads to 6 mV bias differences between consecutive DAC configurations, which enables fine-grain tuning of the gain. Because of the components, such as microrings, which are thermally tuned, the accuracy of the bias voltage reduces the temperature variation effect on the circuit performance. Table 3.3 depicts the comparison between similar optical receivers that are designed in 180 nm technology.

	[42]	[43]	[40]	This Work
Transimpedance (dB)	54	69	78	70-78
Bandwidth (GHz)	9.5	7.5	7	6.3
Power (mW)	10.6	11.2	8.9	7.4-10.9

Table 3.3: Receiver circuits Comparison

The laser is assumed to be linear up to 9 dBm and is modeled with a 100-ohm resistor

and 150 pF capacitor [44] while connected to a 2.5-V high voltage supply. Three control bits generating 8 optical power levels are used for the laser DAC, leading to a voltage bias range of 630 to 750 mV, and consuming 2 mW to produce the highest voltage.

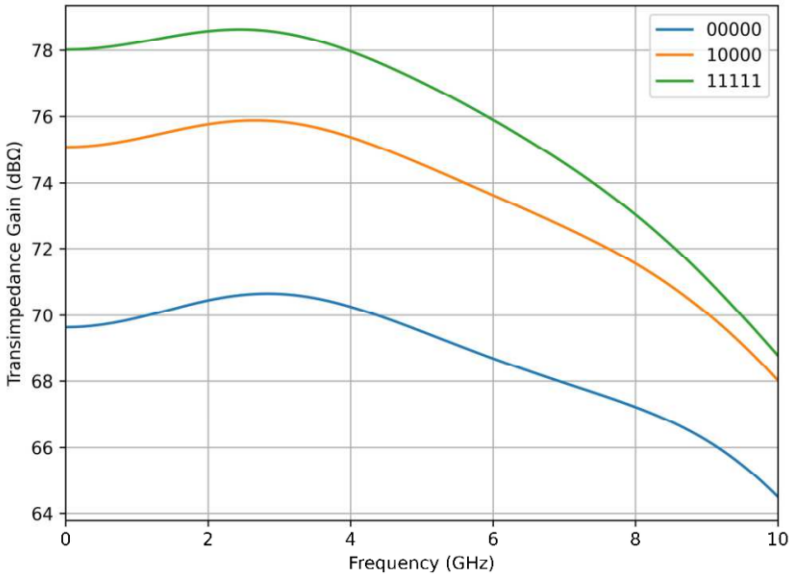


Figure 3.4: Receiver gain according to the frequency and for various DAC configurations.

Fig. 3.5 reports the receiver power consumption and the achieved BER for all configurations. The receiver is designed to reach 10^{-12} BER for configuration '11111' and -17 dBm input optical power. This configuration corresponds to a gain of 78 dB and is obtained with a 750 mV bias voltage previously mentioned. As seen in the figure, it leads to a power consumption of 8.6 mW for the receiver. Configuration '00000' (i.e., 550 mV bias voltage) leads to 5.4 mW power consumption for a 10^{-3} BER. For comparison purposes, we also designed a conventional, i.e., non-configurable receiver, using the same technology node and parameters. We obtained a power consumption of 8 mW for the conventional receiver. However, as discussed in the next chapter, significant power reduction is obtained when considering the links.

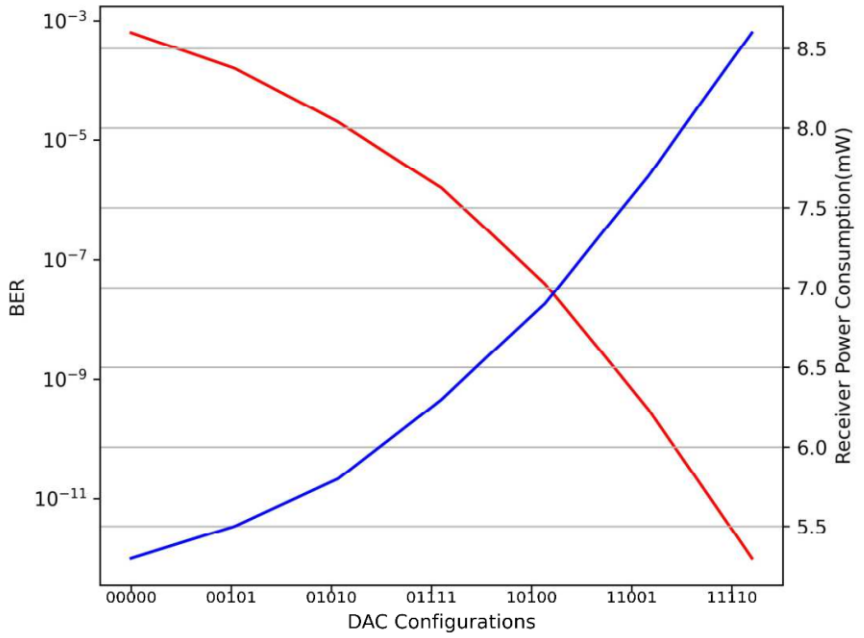


Figure 3.5: BER and power consumption according to the DAC configurations.

3.5.2 System Level Analysis

In this section, we use the design method to design a link with 8 receivers and one wavelength. We assumed an optical link with 8 receivers and a 1 cm distance between them. Required laser power for assumed BER of 10^{-12} is -6.3 dBm. The laser power is used in equation (3.1) to calculate the received optical power and DAC configuration for each receiver. Fig. 3.6 shows the DAC configuration of each receiver for 10^{-12}, 10^{-9}, and 10^{-6} BERs. For 10^{-12} BER, configuration '01001' is chosen for the first receiver with an estimated received optical power of -11.4 dBm. For BER of 10^{-9} and 10^{-6} the DAC configurations are '00011' and '00000', respectively. By targeting 10^{-9} BER instead of 10^{-12}, the receivers can be reconfigured to lower their power consumption. Since the SNR is not linearly proportional to the BER [36], targeting 10^{-6} instead of 10^{-9} is more beneficial than targeting 10^{-9} instead of 10^{-12} which will allow us to investigate, in our future work, the design of approximate nanophotonic interconnects with reconfigurable receivers. The first

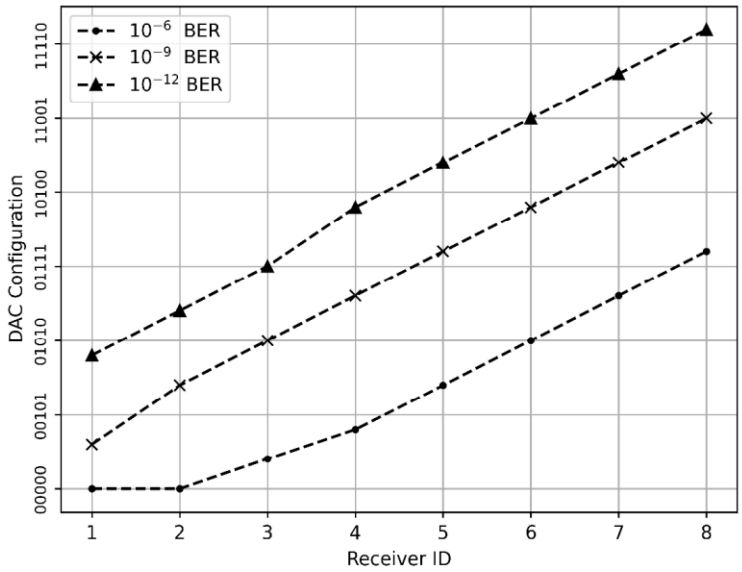


Figure 3.6: DAC configuration of a link with 8 receivers for 3 different BERs.

two receivers in the 10-6 scenario are configured with '00000' due to the limited range of the DAC to fully take advantage of the optical power overhead available in the waveguide. To overcome this limitation, we plan to extend the proposed link with reconfigurable transmitters to increase the modulation speed for short-range communications benefiting from the optical power overhead.

Fig. 3.7 depicts the power consumption breakdown of each receiver for 10^{-12} BER. The TIA and the first stage of MA consume 4.9 mW. The CS stage consumes from 1.2 mW for the first receiver to 3.1 mW for the last receiver. Similarly, the DAC power consumption ranges from 0.2 mW to 0.6 mW, which corresponds to up to 6% of the total power consumption. Compared to a link involving conventional receivers, we obtain a total of 9% power reduction. Indeed, although the last reconfigurable receivers lead to power overhead due to the DAC, the receivers closer to the transmitter experience significant power reduction due to the higher optical power in the waveguide.

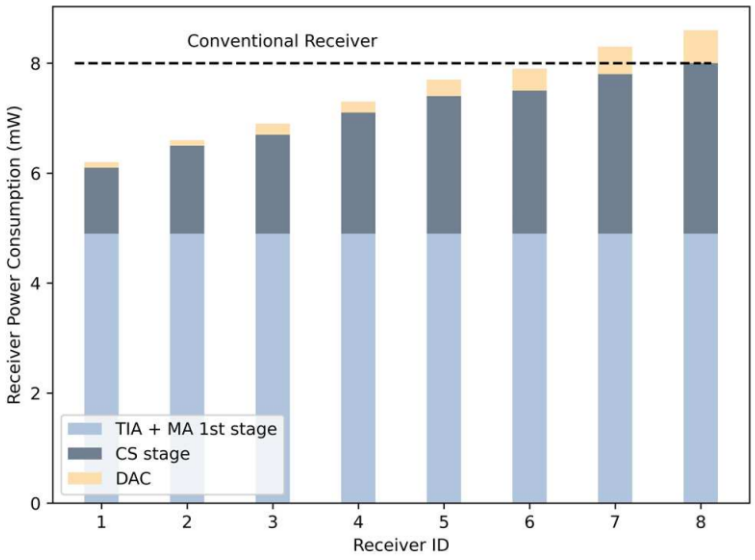


Figure 3.7: Power breakdown for each receiver.

3.6 Conclusion

In this chapter, we proposed a reconfigurable receiver for nanophotonic interconnects. The proposed circuit allows adapting the signal gain according to received optical power. The receiver is digitally controlled using five bits, thus enabling its deployment in various optical interconnects such as SWMR. When used to design eight receivers with a single wavelength, the proposed receiver leads to a 9% power consumption saving on average and up to 25% power reduction for receivers close to the transmitter. We also show that the receivers can be configured according to the targeted BER, allowing us to envision approximate nanophotonic interconnects in which receivers are configured according to data precision requirements.

Chapter 4

A Method to Reduce the Design Complexity of Nanophotonic Interconnects

In this chapter, first, the Proposed transmitter and Receiver Reconfigurable Optical Link is presented. Then, the design flow and reduction method are explained. The simulation results are discussed at the end.

4.1 Introduction

This chapter proposes a reconfigurable laser driver on top of reconfigurable receivers for nanophotonics interconnects. A digital current DAC is proposed to control the receiver's gain and the transmitter's optical power. Then, we present a design flow in which laser optical power and receiver gain design space are analyzed to find the optimum configurations and achieve the lowest power consumption for each receiver communication. A reduction method is designed for this purpose to detect unused configurations. The results are used to optimize the DACs to reduce control complexity and power consumption. Up to 20%

power reduction is achieved for a link with 4 receivers.

The rest of the chapter is organized as follows. Section 4.2 presents the reconfigurable photonic circuits, while Section 4.3 discusses the design flow of the optical links. Results are presented in Section 3.5.

4.2 Reconfigurable Silicon Photonics Interconnects

As shown in Fig. 4.1 (a), we illustrate a Single Writer Multiple Readers (SWMR) link in which a transmitting core communicates with N similar readers utilizing one wavelength. The transmitter modulates the laser's light amplitude by implementing the OOK modulation, which propagates through the waveguide. The microring of the intended receiver is tuned to match its wavelength resonance with the optical signal. The signal is converted to current by a photodiode and amplified by a transimpedance amplifier (TIA). Then, a comparator determines the value of the received signal [45]. This communication is extended to utilize WDM to increase the link's bandwidth. Due to the insertion losses of waveguides and microrings, the optical signal is attenuated as it propagates through the waveguide to reach its destination. Therefore, the received optical power differs based on the receiver's location. The least amount of optical power reaches the last receiver, which means higher gain or laser optical power is needed to achieve the required BER. This means the highest power consumption of the link is required. On the other hand, the first receiver receives more optical signal due to the short propagating distance and benefits from lower receiver gain and laser optical power [46].

In this chapter, we propose an optical link in which the laser optical power and receiver gain are reconfigurable and are used to satisfy the required BER. For this purpose, a DAC is implemented at the transmitter and receiver to change the optical laser power and receiver gain, respectively. The DACs are designed with high voltage resolution to find the

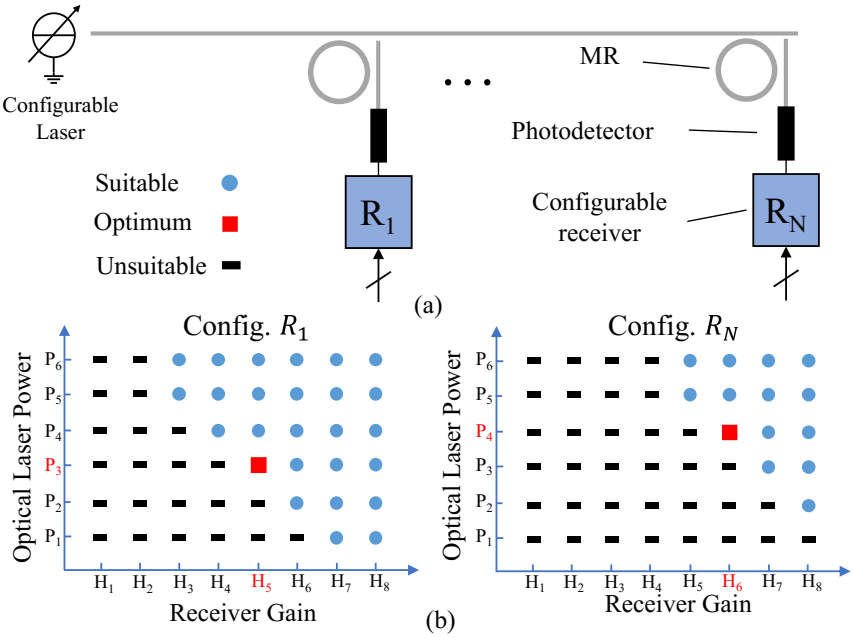


Figure 4.1: (a) Proposed reconfigurable optical link (b) Possible configurations for communication with the first and last receiver.

optimum power configuration. Therefore, a 2D design space consisting of these two parameters is explored to find the configuration that leads to the least power consumption for each receiver communication. By determining the optimum configurations, the DACs are optimized to only correspond to the specified configurations.

Fig. 4.1 (b) depicts a case study of possible communication configurations with the optical link's first and last receiver. Six optical laser power levels [$P_1 \ldots P_6$] and eight receiver gain levels [$H_1 \ldots H_8$] are assumed. Based on the receivers' location, unsuitable configurations that do not satisfy the needed BER are specified in black. The remaining configurations are suitable for communication and are shown in blue, and the lowest power consumption configuration is shown in red. For the first and last receiver, configurations (P_3, H_5) and (P_4, H_6) give the lowest power consumption while satisfying the BER. Then, the DACs are optimized to only correspond to (P_3, P_4) and (H_5, H_6); hence other configurations are removed.

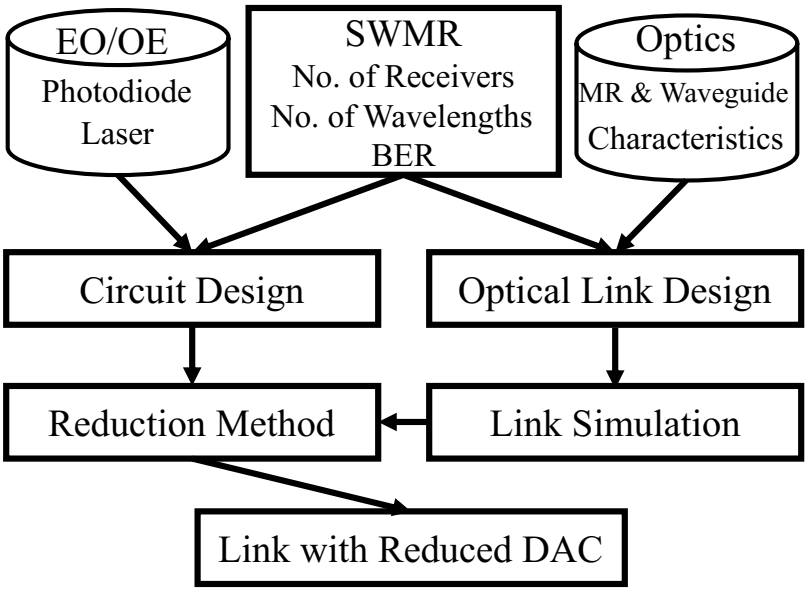


Figure 4.2: Proposed design flow of an optical link.

4.3 Design Flow and Reduction Method

In this section, we first present an overview of the design method. Then, the reduction method is explained.

4.3.1 Overview

Fig. 4.2 depicts the overall design flow. The number of receivers, wavelength, and needed BER are design inputs. A library of optical device parameters is used in the calculations [45]. Based on the waveguide losses and microring resonators' characteristics, the length of the rings and corresponding wavelengths of the link are designed [5], and the results are used in a system-level optical simulator.

Based on the laser and photodiode characteristics, a reconfigurable receiver from last chapter and laser driver circuits are designed to satisfy the required BER. Furthermore, the input current noise of the receiver is minimized to achieve high sensitivity. The required number of DAC control bits is defined depending on the required optical power and

range of the receiver gain. The simulation results, such as laser optical power vs. power consumption and receiver gain vs. power consumption, are used in the reduction method.

The reduction method calculates the possible configurations based on the optical link and circuit characteristics. Then, optimum power configurations are determined for each communication. After validating the optimum configurations in the optical simulator, the DAC circuits are optimized to remove unused configurations. This is achieved by modifying the transistors' weights of the DACs' branches or eliminating the whole branch if possible.

In the end, the design flow determines the optimum optical laser power and receiver gain for each transmitter-receiver communication and the characteristics of the modified DAC. This method can be used with various sets of optical parameters by redesigning the optical link.

4.3.2 Reduction Method

The BER of a communication signal is determined by calculating the Q parameter [44] for a signal after the amplification and before the comparator stage, which is given in equation (4.1):

$$Q = \frac{V_S^{PP} - V_{MN}}{2V_n^{rms}} \tag{4.1}$$

$$V_S^{PP} = H_R.I_{in} = H_R\left(P_L - IL_{tot}\right)R_{PD} \tag{4.2}$$

$$V_n^{rms} = H_R * \sqrt{BW\left(I_{n,PD}^2 + I_{n,Amp}^2\right)} \tag{4.3}$$

$$IL_{tot} = (IL_{wg} \times L \times K) - (IL_{MR} \times (K-1)) - IL_{MRsel} \tag{4.4}$$

In which V_S^{PP} is the peak-to-peak voltage of the signal and V_{MN} is the minimum voltage that the comparator requires to evaluate the digital value of the signal. The topology of the comparator and technology of the transistors determine V_{MN}. V_n^{rms} is the total rms noise of the signal. Eq. (4.2) calculates V_S^{PP} in which H_R is the gain of the receiver and I_{in} is the generated photodiode current. $H_{R,Min}$ and $H_{R,Max}$ are defined as the minimum and maximum gains of the receiver circuit. P_L is the laser optical power, IL_{tot} is the total insertion loss that optical signal experiences and R_{PD} is the responsivity of the photodiode. V_n^{rms} consists of the uncorrelated photodetector $(I_{n,PD})$ and amplifier $(I_{n,Amp})$ noise and it is calculated by equation. (4.3). BW represents the 3-dB bandwidth of the receiver. The photodetector noise is correlated to the received optical power. Hence, the generated noise of detecting 1 is more than detecting 0. However, for simplicity and noise margin, the upper limit of noise, which is detecting 1, is considered in this study. Furthermore, the DAC circuit implemented in the later stages of the receiver has minimal effect on the amplifier noise; thus, it is assumed to be constant. IL_{tot} is computed by Eq. (4.4) in which IL_{wg} and IL_{MR} represent the insertion loss of the waveguide and through insertion loss of the microring filter. L and K are the distance of the receivers from each other and the number of receivers, respectively. IL_{MRsel} is the drop insertion loss of the receiver's microring filter. Table 4.3.2 summarizes the device parameters that are used in the equations.

Device	Parameter	Value
Laser	Efficiency	15 %
Waveguide	Insertion Loss	0.8 dB/cm
MR filter	Drop IL	2 dB
	Through IL	0.3 dB
Photodiode	Responsivity	0.9 A/W
	Capacitance	100 fF

Table 4.1: Device parameters [9].

After determining the $H_{R,Max}$ and $H_{R,Min}$ from the receiver circuit simulations, equation. (4.1) is iterated to calculate the required input current for each case. Then, by calculating the IL_{tot} for each receiver, the required P_L is computed. In this study, $I_{n,PD}$ is relatively small compared to $I_{n,Amp}$. Therefore, for each receiver, the relation between the gain and laser optical power is modeled linearly. The maximum $(P_{L,Max})$ and minimum $(P_{L,Min})$ optical laser powers are calculated by determining the intersection of $H_{R,Max}$ and $H_{R,Min}$ with the last and first receiver, respectively. Based on the number of optical laser power and receiver gain levels determined by the DACs control bits, possible configurations, and their consumption power are defined. Then, for each receiver, the optimum configuration is determined. Finally, the DACs are optimized to only correspond to the optimum configurations, and unused ones are eliminated.

4.4 Results

4.4.1 System Level Analysis

Synopsys OptSim is used for the system-level simulator. The targeted BER for the optical link is 10^{-12}, and the distance between the receivers is 1 cm.

For the case of an optical link with 4 receivers utilizing 4 wavelengths, 1.8 dB insertion loss between the receivers has resulted from OptSim. Fig. 4.3 depicts the possible laser power versus receiver gain configurations assuming 3-bit DAC control for both the transmitter and the receiver, resulting in eight levels for each. For each receiver, the best configuration is specified with the color of that receiver, and the corresponding consumption power is shown. As the receivers take distance from the transmitter, the receiver gains, and laser power increases to compensate for the insertion loss of the link, leading to higher power consumption. R_2 and R_4 use the 74 dB receiver gain, which reduces the used receiver gain levels and control bits of the receiver DAC decreases to two. For the baseline

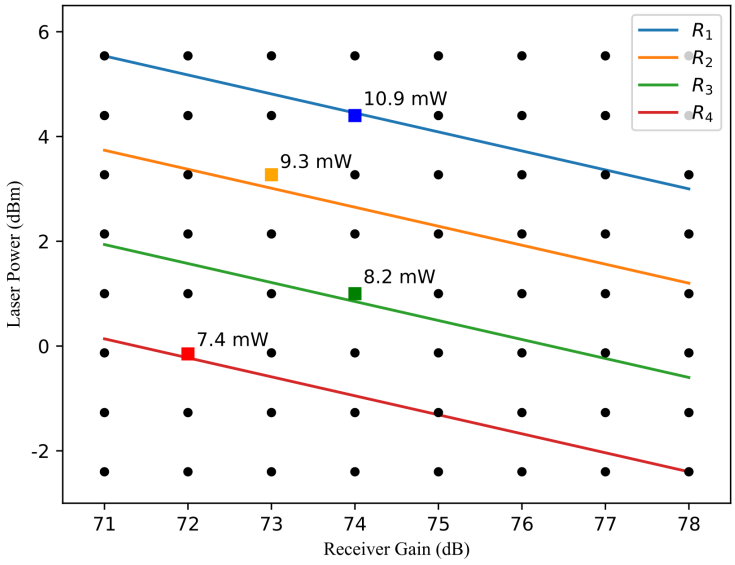


Figure 4.3: Possible configuration for 4 receivers.

optical link, which utilizes one receiver gain and laser optical power, the configuration of R_4 is used for all the receivers. By accounting for the DACs power overhead, this design reduces the optical link power consumption by 19%.

Silicon Photonics waveguides are fabricated mainly with silicon, silicon nitride, and compound platforms. Table 4.2 summarizes the critical parameters of these technologies. Since the fabrication processes are not mature enough, the insertion losses vary between the platforms. The design can expand for different platforms and a high number of receivers. However, the limitation is the maximum optical power that the lasers can provide. As it is summarized in [11], III–V Silicon lasers support output power of around 50 mW [47] [48].

	SiON [49]	Si_3N_4 [50]	Silica [51]	Silicon [52]
Insertion Loss (dB)	2.5	0.5	4.5-5	1-1.5
Central Wavelength (nm)	880	900	750	1550
Footprint (um^2)	340	100	150	110

Table 4.2: Comparison of waveguide fabrication platforms

4.4.2 Control Complexity and Scalibilty

Fig. 4.4 (a) shows the power consumption of an optical link based on the number of control bits, assuming 4 receivers and 4 wavelengths. The transmitter is configured to communicate with each receiver equally. The control bits are divided into varied cases between the receiver and transmitter. For each side, M control bits result in 2M levels. (R, L) defines the number of Receiver gain and optical laser levels accordingly. Compared to the baseline optical link, our design reduces the link power consumption from 43.3mW to 35.5mW, translating to 18% consumption power reduction. The blue line highlights the best power reduction configuration for each case. Further increasing the control bits does not improve the power consumption, since the selected configurations are close enough to the general optimum configurations. In this case, more control bits for the receiver DAC are more favorable for reducing power consumption. By increasing the distance between the receivers, the laser consumes more power, and a greater number of laser control bits is more effective in improving the power consumption.

Fig. 4.4 (b) illustrates the link's average power saving compared to the baseline optical link according to the number of receivers. Three control bits are assumed for each laser and receiver DAC circuit. The design saves the most power for the case of 4 to 6 receivers, accounting for up to 20%. With fewer receivers, the DAC power consumption would be considerable, reducing the power saving. Since the receiver's gain range is fixed, a high number of receivers increases the optical laser power and power consumption. This means that the laser consumes a lot more than the receiver, and the design flow cannot properly utilize the configurations, reducing the power-saving efficiency. To optimize the design for a high number of receivers, the design method should start with the laser optical power and then design the circuit based on the required gain.

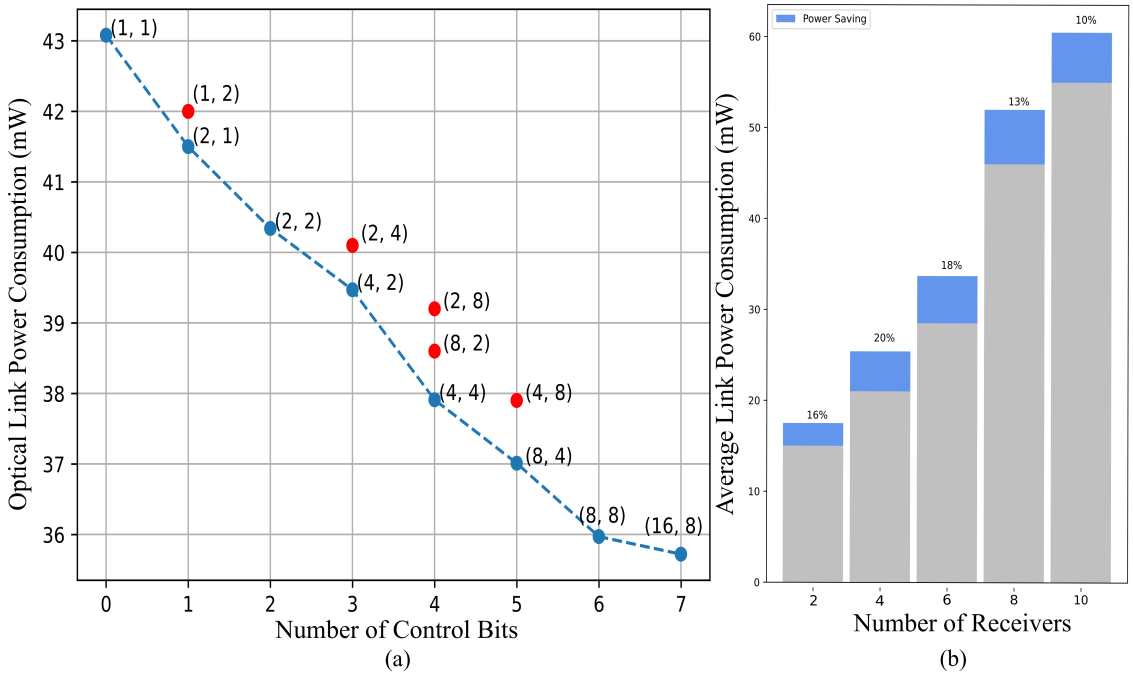


Figure 4.4: (a) Optical link power consumption versus number of control bits (b) Average power consumption based on the number of receivers.

4.5 Conclusion

This chapter proposes a reconfigurable transmitter and receiver for nanophotonic optical interconnects. A design flow to determine the optimum power configuration for each receiver communication is presented based on the optical link parameters. The reduction method utilizes circuits and optical characteristics to optimize the DACs, which control the laser optical power and receiver gain to correspond only to the specified configurations. This design decreases the power consumption of the SWMR optical links by up to 20%. By utilizing multiple BERs, approximate nanophotonic interconnects can be envisioned.

Chapter 5

Conclusion and Future Works

5.1 Conclusion

In this thesis, reconfigurable receivers for optical links are proposed first. It allows us to tune the receivers based on the BER and power consumption trade-off. We show that it is possible to reduce the power consumption of optical links based on the existing optical device parameters and communication requirements. An optical link with only reconfigurable receivers can reduce power consumption by 9% on average. Using the reduction method with an added reconfigurable transmitter can further reduce the power consumption to 15% and up to 20% in some cases.

We demonstrated that ubiquitous receiver and transmitter circuits can be used for the optical link and reduce the design complexity. This has been achieved by using similar DACs for each receiver and transmitters tuning these circuits' bias voltage.

The proposed reduction method helps us to design power-efficient communication links based on the position of the receivers from the transmitter with minimal added complexity. The proposed method can be used with different optical parameters and technologies. With an increasing demand for high-performance computing and artificial intelligence, data-intensive domains, a growing need to transfer extensive data with low power consumption

and high speed emerges, and this thesis tries to utilize the proposed circuits and reduction method to improve optical links power consumption and reduce power consumption.

5.2 Future Work

Reconfigurable nanophotonic interconnects still need time to be matured, and much work is still needed. Some of the future tasks to improve the proposed methods are listed below.

- Noise calculations can be improved by using the more detailed optical devices noise models. for example photodiode noise model can be elaborated and we can replace the assumption of constant noise effect with shot and Thermal noise [53] [54].

- Approximate Computing (AC) is one of the applications that can implement the proposed circuits and method and result in reducing the power consumption even more. The proposed circuits can be tuned for different BERs, thus enabling the utilization of AC solutions. Dynamic BERs in the communication should be accounted for in the design of the optical link [55] [56].

- Develop and study of the proposed method for other optical link architectures. Multi-writer, Multiple Reader (MWMR) links are an attractive architecture that can benefit from reconfigurable circuits. Utilizing reconfigurable circuits with laser-forwarded coherent transceivers can improve the optical link energy efficiency [57] [58].

- Implementing the proposed method for different applications and finding the more suitable ones. The proposed method can be more optimized for specific tasks. AI-related applications that require the transfer of an enormous amount of data between memory and the processors are good candidates. Tuning the microrings to the required temperature takes time, and the predictability of data movements can reduce

the downtime of the optical link and improve the data throughput.

- The research on optical devices offers different fabrication processes and various models; therefore, their parameters, such as insertion loss, are different across different platforms. The compatibility and integration of these optical devices require more research. Using optical devices from one fabrication process can reduce the effectiveness of the proposed reduction method to the extent that some fabrication processes may not benefit from power consumption reduction [50] [59].

Bibliography

[1] N. Mehta, S. Lin, B. Yin, S. Moazeni, and V. Stojanović, "A laser-forwarded coherent transceiver in 45-nm soi cmos using monolithic microring resonators," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 4, pp. 1096–1107, 2020.

[2] V. Sumanth, Manish, S. A. Chanu, and R. K. Sonkar, "Silicon waveguides for mid-infrared integrated photonics," in *2020 IEEE 8th International Conference on Photonics (ICP)*, pp. 103–104, 2020.

[3] E. Säckinger, *Broadband circuits for optical fiber communication*. John Wiley & Sons, 2005.

[4] D. Gostimirovic and N. Y. Winnie, "A comparison of microresonator devices for wdm-compatible mode-division multiplexing," in *Smart Photonic and Optoelectronic Integrated Circuits XXII*, vol. 11284, pp. 80–87, SPIE, 2020.

[5] W. Bogaerts, P. De Heyn, T. Van Vaerenbergh, K. De Vos, S. Kumar Selvaraja, T. Claes, P. Dumon, P. Bienstman, D. Van Thourhout, and R. Baets, "Silicon microring resonators," *Laser & Photonics Reviews*, vol. 6, no. 1, pp. 47–73, 2012.

[6] A. Narayan, Y. Thonnart, P. Vivet, and A. K. Coskun, "Prowaves: Proactive runtime wavelength selection for energy-efficient photonic nocs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 40, no. 10, pp. 2156–2169, 2021.

[7] I. A. Young, E. Mohammed, J. T. S. Liao, A. M. Kern, S. Palermo, B. A. Block, M. R. Reshotko, and P. L. Chang, "Optical i/o technology for tera-scale computing," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 1, pp. 235–248, 2010.

[8] A. B. Ahmed, D. Fujiki, H. Matsutani, M. Koibuchi, and H. Amano, "Axnoc: Low-power approximate network-on-chips using critical-path isolation," in *2018 Twelfth IEEE/ACM International Symposium on Networks-on-Chip (NOCS)*, pp. 1–8, 2018.

[9] Q. Wilmart, C. Bellegarde, C. Petit-Etienne, L. Youssef, J.-M. Hartmann, D. Fowler, S. Brision, S. Garcia, A. Myko, K. Ribaud, P. Grosse, B. Charbonnier, S. Bernabé, C. Sciancalepore, E. Pargon, and B. Szelag, "Ultra low-loss silicon waveguides for 200 mm photonics platform," in *2019 IEEE 16th International Conference on Group IV Photonics (GFP)*, pp. 1–2, 2019.

[10] B. Szelag, B. Blampey, T. Ferrotti, V. Reboud, K. Hassan, S. Malhouitre, G. Grand, D. Fowler, S. Brision, T. Bria, *et al.*, "Multiple wavelength silicon photonic 200 mm r+ d platform for 25gb/s and above applications," in *Silicon Photonics and Photonic Integrated Circuits V*, vol. 9891, pp. 225–239, SPIE, 2016.

[11] Z. Yao, K. Wu, B. X. Tan, J. Wang, Y. Li, Y. Zhang, and A. W. Poon, "Integrated silicon photonic microresonators: Emerging technologies," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 24, no. 6, pp. 1–24, 2018.

[12] H. Xu, D. Dai, and Y. Shi, "Silicon integrated nanophotonic devices for on-chip multi-mode interconnects," *Applied Sciences*, vol. 10, no. 18, 2020.

[13] M. H. Nazari and A. Emami-Neyestanak, "A 24-gb/s double-sampling receiver for ultra-low-power optical communication," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 2, pp. 344–357, 2013.

[14] D. Kharas, J. Plant, S. Bramhavar, W. Loh, R. Swint, C. Sorace-Agaskar, C. Heidelberger, and P. Juodawlkis, "High power (¿ 300 mw) 1550 nm on-chip laser realized using passively aligned hybrid integration," in *2020 Conference on Lasers and Electro-Optics (CLEO)*, pp. 1–2, May 2020.

[15] C. Sun, D. Jeong, M. Zhang, W. Bae, C. Zhang, P. Bhargava, D. Van Orden, S. Ardalan, C. Ramamurthy, E. Anderson, A. Katzin, H. Lu, S. Buchbinder, B. Beheshtian, A. Khilo, M. Rust, C. Li, F. Sedgwick, J. Fini, R. Meade, V. Stojanović, and M. Wade, "Teraphy: An o-band wdm electro-optic platform for low power, terabit/s optical i/o," in *2020 IEEE Symposium on VLSI Technology*, pp. 1–2, 2020.

[16] Q. Wilmart, S. Brision, J.-M. Hartmann, A. Myko, K. Ribaud, C. Petit-Etienne, L. Youssef, D. Fowler, B. Charbonnier, C. Sciancalepore, E. Pargon, S. Bernabé, and B. Szelag, "A complete si photonics platform embedding ultra-low loss waveguides for o- and c-band," *Journal of Lightwave Technology*, vol. 39, no. 2, pp. 532–538, 2021.

[17] M. Wade, D. Jeong, B. Kim, M. Zhang, W. Bae, C. Zhang, P. Bhargava, D. V. Orden, S. Ardalan, C. Ramamurthy, E. Anderson, A. Katzin, H. Lu, S. Buchbinder, B. Beheshtian, A. Khilo, M. Rust, C. Li, F. Sedgwick, J. Fini, R. Meade, V. Stojanović, and C. Sun, "Monolithic microring-based wdm optical i/o for heterogeneous computing," in *2021 Symposium on VLSI Technology*, pp. 1–2, 2021.

[18] C. Koos, W. Freude, J. Leuthold, M. Kohl, L. R. Dalton, W. Bogaerts, M. Lauermann, S. Wolf, C. Weimann, A. Melikyan, N. Lindenmann, M. R. Billah, S. Muehlbrandt, S. Koeber, R. Palmer, K. Koehnle, L. Alloatti, D. L. Elder, A.-L. Giesecke, and T. Wahlbrink, "Silicon-organic hybrid (soh) integration and photonic multi-chip systems: Extending the capabilities of the silicon photonic platform," in *2015 IEEE Photonics Conference (IPC)*, pp. 480–481, 2015.

[19] I. García López, A. Awny, P. Rito, M. Ko, A. C. Ulusoy, and D. Kissinger, "100 gb/s differential linear tias with less than 10 pa/ $\sqrt{\text{hz}}$ in 130-nm sige:c bicmos," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 2, pp. 458–469, 2018.

[20] D. Zhang and G. Cowan, "A pull-up vcsel driver with a shunt rc load in 65-nm cmos," in *2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1022–1025, 2021.

[21] S. Zohrei and S. L. Beux, "Design of a reconfigurable receiver for nanophotonic interconnects," in *2022 20th IEEE Interregional NEWCAS Conference (NEWCAS)*, pp. 203–207, 2022.

[22] S. Fathololoumi, C. Malouin, D. Hui, K. Al-hemyari, K. Nguyen, P. Seddighian, Y.-J. Chen, Y. Wang, A. Yan, R. Defrees, T. Liljeberg, and L. Liao, "Highly integrated 4 tbps silicon photonic ic for compute fabric connectivity," in *2022 IEEE Symposium on High-Performance Interconnects (HOTI)*, pp. 1–4, 2022.

[23] S. Fathololoumi, K. Nguyen, H. Mahalingam, M. Sakib, Z. Li, C. Seibert, M. Montazeri, J. Chen, J. K. Doylend, H. Jayatilleka, C. Jan, J. Heck, R. Venables, H. Frish, R. A. Defrees, R. S. Appleton, S. Hollingsworth, S. McCargar, R. Jones, D. Zhu, Y. Akulova, and L. Liao, "1.6tbps silicon photonics integrated circuit for co-packaged optical-io switch applications," in *2020 Optical Fiber Communications Conference and Exhibition (OFC)*, pp. 1–3, 2020.

[24] Q. Wilmart, S. Brision, J.-M. Hartmann, A. Myko, K. Ribaud, C. Petit-Etienne, L. Youssef, D. Fowler, B. Charbonnier, C. Sciancalepore, *et al.*, "A complete si photonics platform embedding ultra-low loss waveguides for o-and c-band," *Journal of Lightwave Technology*, vol. 39, no. 2, pp. 532–538, 2021.

[25] J. Sun, R. Kumar, M. Sakib, J. B. Driscoll, H. Jayatilleka, and H. Rong, "A 128 gb/s pam4 silicon microring modulator with integrated thermo-optic resonance tuning," *Journal of Lightwave Technology*, vol. 37, no. 1, pp. 110–115, 2018.

[26] S. Saeedi, S. Menezo, G. Pares, and A. Emami, "A 25 gb/s 3d-integrated cmos/silicon-photonic receiver for low-power high-sensitivity optical communication," *Journal of Lightwave Technology*, vol. 34, no. 12, pp. 2924–2933, 2016.

[27] S. P. Crago and D. Yeung, "Reducing data movement with approximate computing techniques," in *2016 IEEE International Conference on Rebooting Computing (ICRC)*, pp. 1–4, 2016.

[28] E. Taheri, S. Pasricha, and M. Nikdast, "Resipi: A reconfigurable silicon-photonic 2.5 d chiplet network with pcms for energy-efficient interposer communication," in *Proceedings of the 41st IEEE/ACM International Conference on Computer-Aided Design*, pp. 1–9, 2022.

[29] J. Lee, C. Killian, S. Le Beux, and D. Chillet, "Distance-aware approximate nanophotonic interconnect," *ACM Trans. Des. Autom. Electron. Syst.*, vol. 27, nov 2021.

[30] H. Yu, D. Patel, W. Liu, Y. Malinge, P. Doussiere, W. Lin, S. Gupta, K. Narayanan, I. Hoshino, M. Bresnehan, S. Sunkoju, D. Mantegazza, R. Herrick, R. Venables, H. Mahalingam, P. Seddighian, A. Fuerst, J. Davis, D. Gold, X. Pan, K. Al-hemyari, A. Agrawal, Y. Li, X. Zheng, M. Geethachar, M. Favaro, D. Zhu, A. Liu, and Y. Akulova, "800 gbps fully integrated silicon photonics transmitter for data center applications," in *2022 Optical Fiber Communications Conference and Exhibition (OFC)*, pp. 1–3, 2022.

[31] Y. Ye, W. Zhang, and W. Liu, "Thermal-aware design and simulation approach for optical nocs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 39, no. 10, pp. 2384–2395, 2020.

[32] M. G. Ahmed, D. Kim, R. K. Nandwana, A. Elkholy, K. R. Lakshmikumar, and P. K. Hanumolu, "A 16-gb/s -11.6-dbm oma sensitivity 0.7-pj/bit optical receiver in 65-nm cmos enabled by duobinary sampling," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 9, pp. 2795–2803, 2021.

[33] S. Li, J. H. Ahn, R. D. Strong, J. B. Brockman, D. M. Tullsen, and N. P. Jouppi, "Mcpat: An integrated power, area, and timing modeling framework for multicore and manycore architectures," in *2009 42nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp. 469–480, 2009.

[34] J. Meng, K. Kawakami, and A. K. Coskun, "Optimizing energy efficiency of 3-d multicore systems with stacked dram under power and thermal constraints," in *DAC Design Automation Conference 2012*, pp. 648–655, 2012.

[35] A. Narayan, Y. Thonnart, P. Vivet, C. F. Tortolero, and A. K. Coskun, "Waves: Wavelength selection for power-efficient 2.5d-integrated photonic nocs," in *2019 Design, Automation and Test in Europe conference Exhibition (DATE)*, pp. 516–521, 2019.

[36] T. E. Carlson, W. Heirman, and L. Eeckhout, "Sniper: Exploring the level of abstraction for scalable and accurate parallel multi-core simulation," in *SC '11: Proceedings of 2011 International Conference for High Performance Computing, Networking, Storage and Analysis*, pp. 1–12, 2011.

[37] H. Matsutani, M. Koibuchi, D. Ikebuchi, K. Usami, H. Nakamura, and H. Amano, "Performance, area, and power evaluations of ultrafine-grained run-time power-gating

routers for cmps," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, no. 4, pp. 520–533, 2011.

[38] Y. Thonnart, S. Bernabé, J. Charbonnier, C. Bernard, D. Coriat, C. Fuguet, P. Tissier, B. Charbonnier, S. Malhouitre, D. Saint-Patrice, M. Assous, A. Narayan, A. Coskun, D. Dutoit, and P. Vivet, "Popstar: a robust modular optical noc architecture for chiplet-based 3d integrated systems," in *2020 Design, Automation and Test in Europe Conference Exhibition (DATE)*, pp. 1456–1461, 2020.

[39] B. Razavi, "Design techniques for high-speed wireline transmitters," *IEEE Open Journal of the Solid-State Circuits Society*, vol. 1, pp. 53–66, 2021.

[40] D. Koh, D. Jeong, J. Hwang, and D.-K. Jeong, "Optical receiver front-end for active optical cable in 180 nm cmos," in *2020 International SoC Design Conference (ISOCC)*, pp. 43–44, 2020.

[41] R. Polster, Y. Thonnart, G. Waltener, J.-L. Gonzalez, and E. Cassan, "Efficiency optimization of silicon photonic links in 65-nm cmos and 28-nm fdsoi technology nodes," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 12, pp. 3450–3459, 2016.

[42] B. Analui and A. Hajimiri, "Bandwidth enhancement for transimpedance amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 8, pp. 1263–1270, 2004.

[43] D. Li, M. Liu, and L. Geng, "A 10-gb/s optical receiver with sub-microampere input-referred noise," *IEEE Photonics Technology Letters*, vol. 29, no. 24, pp. 2268–2271, 2017.

[44] B. Razavi, *Design of Integrated Circuits for Optical Communications*. McGraw-Hill Series in Electrical and Computer Engineering, McGraw-Hill, 2003.

[45] S. Y. Siew, B. Li, F. Gao, H. Y. Zheng, W. Zhang, P. Guo, S. W. Xie, A. Song, B. Dong, L. W. Luo, C. Li, X. Luo, and G.-Q. Lo, "Review of silicon photonics technology and platform development," *Journal of Lightwave Technology*, vol. 39, no. 13, pp. 4374–4389, 2021.

[46] L. Liao, S. Fathololoumi, K. Nguyen, H. Mahalingam, D. Hui, J. Heck, H. Frish, R. Defrees, C. Malouin, P. Seddighian, M. Huang, K. Al-Hemyari, Y.-J. Chen, Y. Wang, W. Lin, D. Zhu, R. Jones, Y. Akulova, and T. Liljeberg, "Silicon photonics for next-generation optical connectivity," in *2023 Optical Fiber Communications Conference and Exhibition (OFC)*, pp. 1–3, 2023.

[47] S. Chen, J. Wu, W. Li, M. Liao, M. Tang, Q. Jiang, S. Shutts, S. Elliott, A. Sobiesierski, I. Ross, P. Smowton, A. Seeds, and H. Liu, "Electrically pumped continuous-wave iii–v quantum dot lasers monolithically grown on silicon," in *2016 International Semiconductor Laser Conference (ISLC)*, pp. 1–2, 2016.

[48] S. Keyvaninia, G. Roelkens, D. Van Thourhout, C. Jany, M. Lamponi, A. Le Liepvre, F. Lelarge, D. Make, G.-H. Duan, D. Bordel, *et al.*, "Demonstration of a heterogeneously integrated iii-v/soi single wavelength tunable laser," *Optics express*, vol. 21, no. 3, pp. 3784–3792, 2013.

[49] N. Ismail, F. Sun, G. Sengo, K. Wörhoff, A. Driessen, R. M. de Ridder, and M. Pollnau, "Improved arrayed-waveguide-grating layout avoiding systematic phase errors," *Opt. Express*, vol. 19, pp. 8781–8794, Apr 2011.

[50] A. Rahim, E. Ryckeboer, A. Z. Subramanian, S. Clemmen, B. Kuyken, A. Dhakal, A. Raza, A. Hermans, M. Muneeb, S. Dhoore, Y. Li, U. Dave, P. Bienstman, N. Le Thomas, G. Roelkens, D. Van Thourhout, P. Helin, S. Severi, X. Rottenberg, and R. Baets, "Expanding the silicon photonics portfolio with silicon nitride photonic

integrated circuits," *Journal of Lightwave Technology*, vol. 35, no. 4, pp. 639–649, 2017.

[51] S. Ashar-Ali and S. Jeen-Hong, "Compact arrayed waveguide gratings for visible wavelengths based on silicon nitride," *Ukrainian journal of physical optics*, no. 18,№ 4, pp. 239–248, 2017.

[52] D. Martens, A. Z. Subramanian, S. Pathak, M. Vanslembrouck, P. Bienstman, W. Bogaerts, and R. G. Baets, "Compact silicon nitride arrayed waveguide gratings for very near-infrared wavelengths," *IEEE Photonics Technology Letters*, vol. 27, no. 2, pp. 137–140, 2015.

[53] D. Abdelrahman and G. E. R. Cowan, "Noise analysis and design considerations for equalizer-based optical receivers," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–1, 2020.

[54] X. Zhou, L. Zhang, and W. Pang, "Performance and noise analysis of optical microresonator-based biochemical sensors using intensity detection," *Opt. Express*, vol. 24, pp. 18197–18208, Aug 2016.

[55] J. P. R and A. S. Pillai, "Enhancing energy efficiency of intensive computing applications using approximate computing," in *2022 3rd International Conference on Electronics and Sustainable Communication Systems (ICESC)*, pp. 1231–1236, 2022.

[56] Z. Wang, G. Zhang, J. Ye, J. Jiang, F. Li, and Y. Wang, "Accurate reliability analysis methods for approximate computing circuits," *Tsinghua Science and Technology*, vol. 27, no. 4, pp. 729–740, 2022.

[57] D. Abdelrahman, O. Liboiron-Ladouceur, and G. E. R. Cowan, "Cmos-driven vcsel-based photonic links: an exploration of the power-sensitivity trade-off," *IEEE Access*, vol. 10, pp. 89331–89345, 2022.

[58] S. Le Beux, J. Trajkovic, I. O'Connor, G. Nicolescu, G. Bois, and P. Paulin, "Optical ring network-on-chip (ornoc): Architecture and design methodology," in *2011 Design, Automation and Test in Europe*, pp. 1–6, 2011.

[59] P. Liao, M. Sakib, F. Lou, J. Park, M. Wlodawski, V. I. Kopp, D. Neugroschl, and O. Liboiron-Ladouceur, "Ultradense silicon photonic interface for optical interconnection," *IEEE Photonics Technology Letters*, vol. 27, no. 7, pp. 725–728, 2015.