Testing and Investigation of GaN-Based High Voltage Inverters for Electric Drives

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Abstract

Testing and Investigation of GaN-Based High Voltage Inverters for Electric Drives

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In recent times, scholarly attention on Wide-bandgap (WBG) devices, like silicon carbide (SiC) and gallium nitride (GaN) transistors, focuses on power conversion for heightened efficiency in electric vehicles. GaN HEMTs, with superior characteristics like low on-resistance and high-speed switching, enable compact power converters with increased integration and power density, crucial for EV advancement.

GaN-powered converters require accurate models for device behavior. Manufacturers use internal data and physics-based models, but these are unavailable to the public and time-consuming to develop. Accurate analytical models, mimicking transistor dynamics and predicting energy loss, offer a solution without extensive computational demands.This thesis validates superior GaN device switching model, proven via experiments and reduced parasitics confirmed with double pulse tests, affirming enhanced accuracy.

Due to the fast switching of GaN device, high voltage slew rate or dv/dt at the inverter output gives rise to switching harmonics, higher voltage stress at the motor winding, and EMI issues in the motor drive system. This thesis conducts a comprehensive review of filter design for GaN-based inverters to attenuate the harmonics and hence mitigate the high dv/dt and EMI issues. A case study is also provided for a three-phase inverter developed. Another limitation of GaN-based converter technology has resulted from the limited voltage and current capability of GaN transistors available in the market. To apply GaN transistors in high-power applications, multi-phase multi-level converter design is also investigated in this thesis. A comparative study on a new neutral pointless multi-level inverter against the traditional topologies is carried out.

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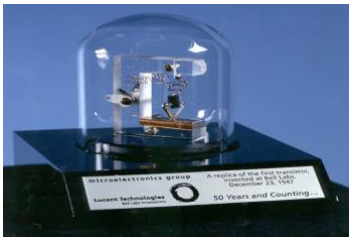
CHAPTER 1 INTRODUCTION

1.1 Historic overview of transistors

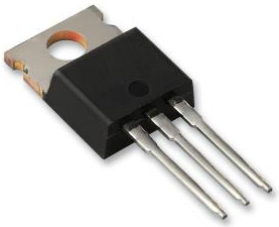
- (1950s-1960s): In the early stages, silicon-based diodes and bipolar junction transistors (BJTs) operated at lower voltage levels, typically in the range of tens to hundreds of volts. They were fundamental components in electronic circuits and early computing systems.

- 1970s-1980s: With the advent of metal-oxide-semiconductor field-effect transistors (MOSFETs), voltage levels improved. MOSFETs were capable of handling several hundred volts, aiding in the development of more efficient power switches used in various electronic applications.

- 1990s-2000s: The introduction of insulated-gate bipolar transistors (IGBTs) further increased voltage capabilities. IGBTs were engineered to handle voltage levels in the kilovolt (kV) range, supporting high-power applications like industrial drives and traction systems in transportation.

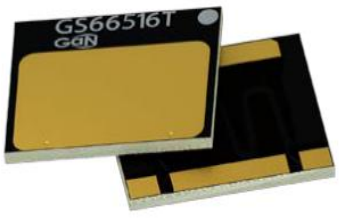


(a) Stylized replica of first transistor



(b) MOSFETs from the 1970s-1980s

(c) IGBT module from the 1990s



(d) Gallium Nitride (GaN) switch from modern era

Figure 1. 1 Historic overview of transistors

- 2010s-Present: Gallium Nitride (GaN) technology marked a shift in voltage capabilities. GaN-based switches have achieved voltage levels surpassing 1 kV and even up to several kilovolts. These switches exhibit remarkable efficiency and power-handling capabilities, particularly in high-frequency and high-power applications such as automotive, telecommunications, and renewable energy systems.

1.2 Background review

The progression of power electronics is deeply entwined with the evolution of semiconductor materials, and the emergence of wide bandgap semiconductors marks a pivotal milestone in this journey. Conventional silicon-based devices have long served as the bedrock of power electronic systems, yet their inherent limitations in terms of efficiency, size reduction, and overall performance have fueled a quest for alternatives. This quest has led to the exploration and utilization of wide bandgap materials, with Gallium Nitride (GaN) positioned at the forefront of this transformative revolution. Semiconductor materials are the linchpin of modern power electronic devices, facilitating the control and manipulation of electrical energy across various applications. Silicon, owing to its abundance and well-established manufacturing processes, has dominated the industry for decades. However, escalating demands for higher efficiency, increased power densities, and faster switching speeds, particularly in industries like automotive, renewable energy, and consumer electronics, exposed the intrinsic limitations of silicon-based devices. Silicon devices, while reliable and versatile, grapple with inherent drawbacks. The material's modest bandgap, approximately 1.1 electron volts (eV), constrains its operational capabilities, particularly in efficiently handling high voltages and frequencies. Silicon's electron mobility, a pivotal factor determining a semiconductor's switching speed, is relatively modest when compared to wide bandgap materials like GaN. This inherent need for alternatives led to the exploration of wide bandgap materials characterized by larger bandgaps than silicon. The study [1], focuses on the development of a high-efficiency single-phase transformerless photovoltaic (PV) inverter. The key components in the inverter design include Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) and Silicon Metal-Oxide-Semiconductor Field-Effect Transistors (Si MOSFETs). The research emphasizes the mitigation of switching losses, improvement of efficiency, and reduction of reactive power in the context of PV inverters. The incorporation of

GaN HEMTs and Si MOSFETs, along with the use of the HERIC (Highly Efficient and Reliable Inverter Concept) topology, aims to enhance the overall performance of the PV inverter. GaN, a binary III-V semiconductor compound, boasts a wide bandgap of approximately 3.4 eV, significantly exceeding silicon's bandgap. This unique property empowers GaN devices to operate at higher breakdown voltages and frequencies while maintaining lower conduction and switching losses.

GaN's significance is further underscored by its exceptional physical properties. The wider bandgap, measuring around 3.4 electron volts (eV) compared to silicon's 1.1 eV, enables GaN devices to operate at significantly higher temperatures without compromising performance. This, in turn, contributes to higher breakdown voltages and efficient electron transport, resulting in reduced on-state resistance and lower switching losses. Through experimental evaluations, the study [2] aims to provide insights into the comparative characteristics of these semiconductor technologies, considering factors such as switching speed, power efficiency, and device reliability. The superiority of GaN devices is succinctly captured by the summarized properties in Table 1.1, showcasing a comprehensive comparison between Silicon and GaN [2], [3].

Table 1. 1 GaN vs Silicon

Parameter	**Silicon**	**GaN**
Band gap E_g (eV)	1.12	3.39
Critical Field E_{Crit} (MV/cm)	0.23	3.3
Electron Mobility μ_n ($cm^2/V \cdot s$)	1400	1500
Permittivity ε_r	11.8	9
Thermal Conductivity λ (W/cm·K)	1.5	1.3
Saturated electron velocity (10^7cm/s)	1.0	2.8

The integration of GaN devices represents a significant advancement in power electronics, offering myriad advantages that reshape the landscape of energy conversion and control systems. GaN devices revolutionize efficiency in power electronics, minimizing conduction and switching losses in high-frequency operations. A research study [4] investigated and compared Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) and Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) in the context of high-efficiency, high-power-density electric vehicle (EV) battery chargers.

In [5], the research conducted a comparative analysis of the driving and switching characteristics between Gallium Nitride Field-Effect Transistors (GaN-FET) and Silicon Carbide Metal-Oxide-Semiconductor Field-Effect Transistors (SiC-MOSFET) in a transient high-voltage pulse discharge circuit. The study focused on investigating the performance of these two wide-band gap semiconductor devices in the context of high-voltage nanosecond pulse applications. Specifically, the research delved into aspects such as drive regulation and transient analysis to gain insights into their suitability for high-voltage pulse discharge circuits. The comparison aimed to provide valuable information for researchers and practitioners seeking to understand and optimize the performance of GaN-FETs and SiC-MOSFETs in applications involving transient high-voltage pulses. The experimental validations corroborate the superior efficiency of GaN devices compared to silicon counterparts, with efficiency improvements ranging from 5% to 10% in various applications. This gain translates into substantial energy savings, especially in systems requiring high power density and continuous operation, such as data centers, electric vehicles, and renewable energy systems. One hallmark advantage of GaN devices lies in their capacity to enable miniaturization while simultaneously enhancing power density in electronic systems. GaN's high electron mobility and superior thermal conductivity facilitate the design of power electronic circuits operating at higher frequencies within compact form factors. This potential for miniaturization finds application in consumer electronics, aerospace, and various industries where space constraints are critical. For instance, GaN-based power adapters and chargers in consumer electronics exhibit reduced size and weight compared to traditional silicon-based counterparts. In portable devices like laptops and smartphones, GaN chargers provide increased power delivery while occupying significantly smaller footprints, enhancing user convenience without compromising performance.

[6] focused on the implementation and comparative analysis of Silicon Carbide (SiC) and Gallium Nitride (GaN) switches in Electric Vehicle (EV) fast recharging systems. The investigation involved a comprehensive evaluation of performance aspects, including voltage measurement, harmonic analysis, electromagnetic compatibility (EMC), and the dynamics of the DC-DC converter. The study aimed to provide insights into the technical nuances and comparative performance of SiC and GaN switches in the context of isolated converters for EV fast recharging. Gan’s ability to operate at higher frequencies finds application in renewable energy systems like solar inverters, optimizing power conversion efficiency and reducing the overall system's footprint.

The study [7] introduces a novel hybrid configuration for electric vehicle traction

inverters. The proposed configuration combines Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) with Silicon (Si) components in a T-Type Three-Level topology. The study explores the use of GaN HEMTs alongside traditional Si components, such as Insulated Gate Bipolar Transistors (IGBTs) and Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), to achieve an innovative three-level inverter design suitable for electric vehicle traction applications. This hybrid approach aims to leverage the high-performance characteristics of GaN devices while maintaining compatibility with existing Si-based technologies in the context of traction inverters for electric vehicles. The advent of GaN technology in electric drives marks a transformative milestone, impacting diverse applications ranging from electric vehicles (EVs) to industrial motor drives and renewable energy systems. In EVs, GaN-based inverters contribute to improved driving ranges and faster charging capabilities. The efficiency gains realized by GaN devices enable more effective power conversion, enhancing the overall performance of EV power trains.

The study [8] addresses the crucial aspect of gate driver circuit design for Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) in the context of electric vehicles. The research focuses on the multi-objective optimization of the gate driver circuit, considering factors such as efficiency, reliability, and performance in power-switching converters specific to electric vehicles. The study emphasizes the importance of tailoring the gate driver design for GaN HEMTs to enhance the overall efficiency and effectiveness of power conversion in electric vehicles. The validity of the proposed design approach has been proved through a simulation study in which the optimized gate driver circuit and a classical symmetrical gate driver circuit have been implemented on a leg inverter for comparison purposes. Simulation results highlighted the effectiveness of the proposed design approach, as both higher efficiency and lower EMI levels have been successfully achieved.

In the continued literature review, the study [9] explores the efficiency and performance of Gallium Nitride (GaN) transistors in power conversion applications. The study emphasizes several key considerations in the design process, including gate drive strategies, EMI (Electromagnetic Interference) mitigation techniques, overcurrent protection mechanisms, and the implementation of a Miller clamping circuit. Furthermore, the researchers address challenges related to cooling and capacitance in high-power GaN inverters, aiming to enhance reliability and overall performance. Ongoing research endeavours aim to optimize GaN-based inverters by addressing challenges related to manufacturing scalability, cost-effectiveness, and reliability, emphasizing advancements in packaging technologies, material quality, and system integration methodologies as key areas of focus to unlock GaN's full potential [10]. The

integration of GaN devices in multi-level inverters is also discussed, showcasing their role in high-voltage and high-power applications with reduced harmonic distortions. GaN's incorporation amplifies the efficiency, reliability, and performance of multi-level inverters, ushering in a new era in power conversion technology [11]-[12]. In [11], the research specifically explores the use of Flying Capacitor Multi-Level Converter Stages in a 1500 V GaN-based solar inverter. Key components such as capacitors, inductors, switches, and stress factors are thoroughly considered in the design optimization process. In [12], the research delves into the intricacies of the inverter's architecture, featuring a flying capacitor multilevel converter (FCML) utilizing GaN technology. Key elements such as capacitors, switches, and the application of phase-shifted PWM (PSPWM) are explored in the design and control strategy. The study emphasizes the use of ceramic capacitors and the overall high-density nature of the inverter, showcasing its potential in DC-AC power conversion applications. The specific power density and advanced features of the proposed inverter topology contribute to the broader understanding of GaN-based multilevel converters for enhanced power electronics applications. Continued research in GaN technology [13] focuses on improving efficiency in power conversion systems, particularly in the context of renewable energy sources. The inverter design leverages the benefits of Wide Band Gap (WBG) devices, combining GaN and Si technologies. A noteworthy aspect of the study is the introduction of a Pulse Width Modulation (PWM) scheme tailored for this hybrid inverter architecture. The proposed scheme aims to mitigate switching losses and enhance the overall efficiency of the system. The paper contributes to the field by addressing the challenges associated with cost, voltage, and switching losses in multilevel converters, providing insights into the potential of integrating GaN and Si technologies for improved energy conversion.

In the study [14], a three-phase motor drive system was introduced, utilizing lateral enhancement-mode GaN devices with a vertical power loop structure. The system incorporated a unique feature for controlling common mode noise current propagation. Experimental validations demonstrated the system's stable operation at a notable switching frequency of 100 kHz over extended durations. However, a notable limitation was identified in the system's lack of compactness, attributed to the presence of only one power bridge with corresponding gate circuits on each PCB. The need for three separate bridges to form a three-phase inverter resulted in a less compact overall system configuration, indicating a potential area for improvement in terms of system miniaturization and integration efficiency.

In [14], a novel approach to three-phase inverter design is introduced. The key innovation lies in the utilization of Printed Circuit Board (PCB) embedded Gallium Nitride (GaN) Field-

Effect Transistors (FETs). The researchers address the challenges associated with parasitic inductance by incorporating GaN FETs directly into the PCB layout. This integration aims to minimize parasitic inductance, enhancing the overall performance and efficiency of the inverter. [15] introduces a novel 650V inverter leg with double-side cooling, employing ceramic substrates and bare GaN on silicon transistors. The design prioritizes compatibility with high operating temperatures and has been meticulously developed, manufactured, and tested. The inverter leg showcases a low parasitic inductance of 3 nH at 100 MHz. The paper commences with a comprehensive overview of strategies for reducing parasitic elements in power modules. Subsequently, it delves into intricate details encompassing the technology, design optimization, original test methodology, manufacturing procedures, and thorough examination of electrical results.

Challenges and future perspectives of GaN in Power Electronics

In the current landscape of Gallium Nitride (GaN) integration, several challenges impede its widespread adoption, presenting hurdles that researchers and industry stakeholders actively work to overcome. Foremost among these challenges is the consideration of costs associated with GaN technology. While the performance benefits are evident, the manufacturing expenses, including material costs and fabrication processes, are currently higher compared to traditional silicon devices. Addressing this hurdle requires strategic cost-reduction measures to enhance the economic feasibility and accessibility of GaN technology, making it more viable for broad implementation. Another critical challenge revolves around ensuring the reliability and consistent performance of GaN devices. Variations in material quality and fabrication processes can impact yield and reliability, necessitating efforts to enhance manufacturing techniques and mitigate defects to achieve higher yields and long-term reliability [16]. Simultaneously, achieving scalability in manufacturing is imperative for GaN technology's evolution. This entails endeavours to achieve larger wafer sizes and optimize manufacturing scalability, which is vital for reducing costs and meeting the growing demand for GaN devices. The advancement of epitaxial growth techniques and substrate technology is instrumental in enabling larger, higher-quality wafers at competitive costs [17]. Moreover, effective thermal management solutions are essential due to the high-power densities and heat dissipation exhibited by GaN devices. Overcoming these thermal challenges is crucial for maximizing GaN device performance and ensuring long-term reliability. Looking ahead, the future of GaN integration involves addressing these challenges through innovative approaches, paving the way for

transformative advancements in the realm of power electronics.

The future perspectives and research directions for GaN technology encompass a multifaceted approach that spans material innovations, packaging and thermal solutions, standardization, design optimization, and holistic system-level approaches. Ongoing research endeavours to explore new materials and crystal growth techniques to enhance GaN material quality and device performance. Innovations in device packaging and thermal management, including advanced packaging techniques and thermal interface materials, are critical to address heat dissipation challenges. The establishment of industry standards and optimized design methodologies for GaN-based systems plays a pivotal role in streamlining manufacturing processes and ensuring compatibility among different components. Moreover, holistic system-level approaches, integrating GaN devices, control algorithms, and circuit designs, aim to maximize the benefits of GaN technology. These collective efforts signify the collaborative synergy between academia and industry, supported by research consortia, industry partnerships, and government initiatives, all contributing to the advancement and successful integration of GaN technology. The transition to GaN aligns with global initiatives for energy efficiency and sustainability, representing a significant stride towards a more efficient and environmentally conscious future.

1.3 Research objectives and publications

The objective of this thesis is to employ the GaN-based inverter technology in motor drive applications. As a continuation of the previous work, this thesis tests and validates an improved design of GaN-based three-phase inverter/motor drive, which achieves better performance and system compactness. To successfully build an inverter requires an overall understanding of not only the characteristics of power switches but also the gate circuit considerations, components selections, associated switching transients, switching frequencies and so on. This thesis goes through design, device selection, PCB manufacture concerns and related design issues. A comprehensive literature review on filter design for GaN-based inverters is also conducted to address the practical engineering issues including the harmonics and EMI resulting from the fast switching of GaN devices. Lastly, investigations on a new multi-level GaN-based inverter topology are performed to allow the use of GaN transistors in high power motor drive applications. To achieve such research objectives, this thesis contributes to:

1. Validating the prototype of a improved GaN-based three-phase inverter and conducting comprehensive experiments to analyze the inverter design and performance. The improved design is based on minimization of parasitic parameters in the PCB traces.
2. Comprehensive simulation-based comparison of new Neutral Point Less topology of six-phase multi-level inverters with the traditional 2-level and 3-level six-phase inverter topologies.
3. Literature review of electric drive filters including both active and passive components to ensure reliable electric vehicle motor drive operation by suppressing dv/dt, current ripple, and EMI levels due to WBG devices. Recommendations on filter design for GaN based motor drives are provided.

Contributions in the form of publications contain:

S. Jaglan, D. L. M. Nzongo and C. Lai, "Investigations on An Advanced Six-Phase Neutral Point Less Multi-Level Inverter," *2023 12th International Conference on Renewable Energy Research and Applications (ICRERA)*, Oshawa, ON, Canada, 2023, pp. 1-6, doi: 10.1109/ICRERA59003.2023.10269440.

1.4 Thesis outline

The rest of this thesis is divided into 4 chapters as described below:

Chapter 2: Design, Testing, and Validation of a 3-Phase GaN Inverter with an Improved Switching Transition Model

In chapter 2, the operating principles, and characterizations of GaN HEMTs are demonstrated first. Additionally, this chapter will offer an in-depth exploration of the practical implementation of GaN technology. Specifically, it will detail the design, rigorous testing procedures, and validation process of a 3-phase GaN inverter. Emphasis will be placed on analyzing and optimizing the parasitics in PCB design, crucial for understanding and improving the inverter's operational efficiency and stability.

Chapter 3: Filter Design for improved GaN-based motor drive performance

Subsequently, this chapter will undertake a comprehensive exploration of electric drive filters. Focusing on mitigating high dv/dt, current ripple, and electromagnetic interference (EMI) in motor drives, this section will delve into filter designs including active and passive

components. For the case study, a filter is designed for the GaN inverter developed in Chapter 2. The emphasis will be on the better performance of GaN inverter which will be demonstrated through simulations. Additionally, the research also aims to identify solutions that not only suppress EMI effectively but also ensure the robust performance of motor drives across diverse operating conditions.

Chapter 4: Review and Comparison of an Advanced Six-Phase Neutral Point Less Multi-Level Inverter Topology

The final chapter will delve into an exhaustive review and comprehensive comparison of an advanced six-phase neutral point-less multi-level inverter. Leveraging insights from the published research paper titled "Investigations on an Advanced Six-Phase Neutral Point Less Multi-Level Inverter," this section will not only dissect the new topology's attributes but also compare it with existing multi-level six-phase inverter topologies such as dual-T-type topology. The aim is to evaluate performance metrics, efficiency gains, and applicability in various power electronic applications.

These forthcoming chapters collectively aim to deepen the understanding of GaN technology's applications, practical implementations, and advancements within power electronics. They represent a focused exploration of critical areas in GaN-based power electronics, striving to address challenges and explore innovative solutions in this dynamic field.

The last chapter is the conclusion and future work.

CHAPTER 2 THREE PHASE GAN INVERTER DESIGN AND TESTING

This chapter delves into the design and testing of a three-phase GaN inverter, beginning with a preliminary study on GaN inverter design. It explores the fundamentals of GaN transistors and discusses the motivation behind utilizing GaN technology for the inverter design. A review of GaN power transistors and packaging technologies sets the stage for component selection. The chapter then presents the results of single-phase R-load tests and double-pulse test experiments, highlighting the experimental setup and discussing the obtained results. Additionally, it addresses parasitic component issues in GaN inverters, followed by verification and extraction methodologies. Experimental verification of parasitics is conducted, and the results are discussed, leading to conclusions regarding the GaN inverter design and testing process.

2.1 Preliminary study on GaN inverter design

2.1.1 Introduction to GaN transistors

Gallium Nitride (GaN) transistors have emerged as promising alternatives to traditional silicon-based transistors in power electronic applications due to their superior electrical properties. GaN transistors offer higher electron mobility, faster switching speeds, and better thermal conductivity compared to silicon devices. Understanding the operating principle of GaN transistors is essential for leveraging their advantages in various power electronics applications.

Semiconductor structure of GaN transistors

GaN transistors are typically fabricated on a GaN epitaxial layer grown on a substrate material such as silicon carbide (SiC) or silicon (Si). The semiconductor structure of a GaN transistor consists of several layers:

- Substrate: Provides mechanical support and thermal management for the device.
- Buffer layer: Reduces defects and strain between the substrate and the epitaxial layer.

- Epitaxial layer: Consists of a GaN layer doped with specific impurities to form the transistor's source, drain, and gate regions.
- Source and Drain contacts: Metal contacts are deposited on the epitaxial layer to form the source and drain terminals of the transistor.
- Gate electrode: Controls the flow of current between the source and drain terminals by modulating the conductivity of the epitaxial layer.

Operation Modes of GaN Transistors

GaN transistors operate in two primary modes: enhancement mode (E-mode) and depletion mode (D-mode). These modes determine how the transistor behaves under different biasing conditions:

- Depletion Mode (D-mode):

D-mode GaN transistors have a conductive channel that exists at zero gate-source voltage. Applying a negative voltage to the gate terminal depletes the channel, reducing the conductivity between the source and drain terminals as shown in Figure 2.1. D-mode GaN transistors behave like normally-on devices and require a negative bias to turn off, making them less commonly used in practical applications compared to E-mode devices.

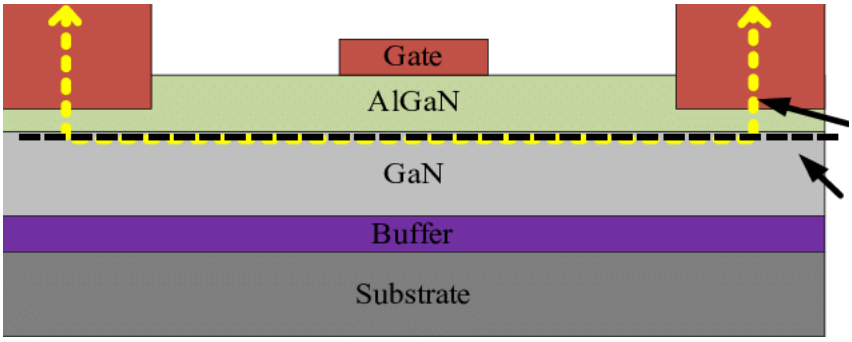


Figure 2. 1 D-mode GaN high electron mobility transistors (HEMT). (Chao-Tsung & Gu et al. 2021)

- Enhancement Mode (E-mode):

In E-mode GaN transistors, the channel is normally off (non-conductive) at zero gate-source voltage. Applying a positive voltage to the gate terminal induces an electron-rich channel in the epitaxial layer, allowing current flow between the source and drain terminals. E-mode GaN transistors behave like normally-off devices, offering inherent safety and ease of control in power electronics applications [18].

Operating principle of E-mode GaN transistors

The operating principle of E-mode GaN transistors involves controlling the conductivity of the epitaxial layer through the application of gate-source voltage. The following steps outline the operation of an E-mode GaN transistor:

- Off State (Gate Voltage = 0 V):

  With zero gate-source voltage, the channel in the epitaxial layer remains depleted, and the transistor is in the off state. Minimal current flows between the source and drain terminals due to the absence of an electron-rich channel.

- Turn-On (Positive Gate Voltage):

  Applying a positive voltage to the gate terminal induces an electron-rich channel in the epitaxial layer beneath the gate electrode. The electric field generated by the gate-source voltage attracts electrons, creating a conductive path between the source and drain terminals. The transistor enters the on state, allowing a significant current to flow through the channel.

- Operation (Conducting State):

  Once turned on, the GaN transistor remains conducting as long as the gate-source voltage is maintained above the threshold voltage. The transistor exhibits low on-resistance ($R_{DS\,(on)}$) and can efficiently conduct large currents with minimal losses.

- Turn-Off (Zero or Negative Gate Voltage):

  Removing or reducing the gate-source voltage depletes the electron-rich channel in the epitaxial layer, effectively turning off the transistor. The absence of a conductive channel interrupts current flow between the source and drain terminals, returning the transistor to the off state.

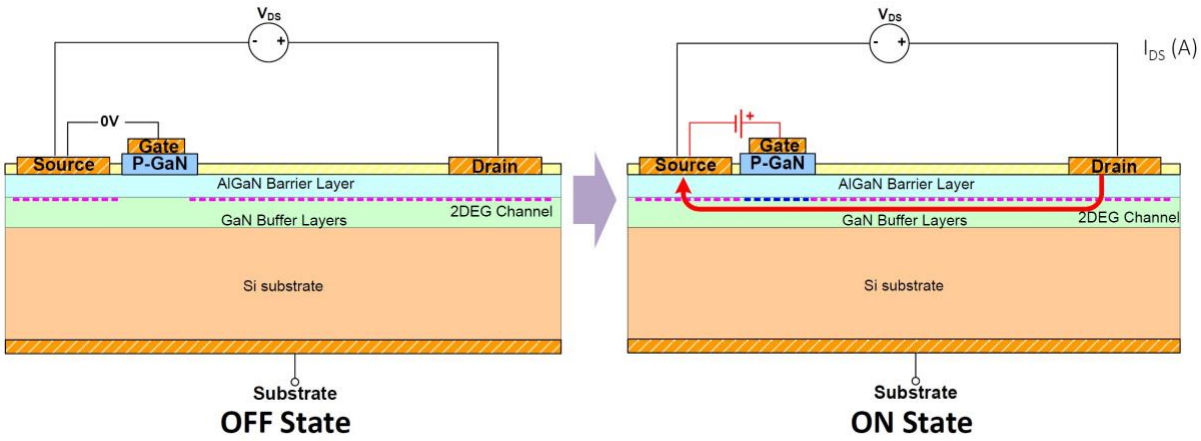


Figure 2. 2 Simplified structure of e-GaN HEMT showing the Vth modulation layer below the gate. [19]

Advantages of GaN transistors

- The operating principle of GaN transistors provides several advantages over traditional silicon-based devices:
- High Electron Mobility: GaN transistors offer higher electron mobility, enabling faster switching speeds and reduced switching losses.
- Wide Bandgap: The wide bandgap of GaN allows for higher breakdown voltages and operation at elevated temperatures, improving device reliability.
- Low On-Resistance: E-mode GaN transistors exhibit low on-resistance, leading to lower conduction losses and higher efficiency in power electronic circuits.
- Miniaturization: GaN devices can be scaled to smaller sizes without sacrificing performance, enabling compact and lightweight power electronics systems.

Applications of GaN transistors

The operating principle and advantages of GaN transistors make them well-suited for various power electronics applications, including:

- Switched-Mode Power Supplies (SMPS): GaN transistors are used in high-frequency SMPS designs for improved efficiency and power density.
- Electric Vehicle (EV) Powertrains: GaN transistors contribute to the efficiency and performance of EV powertrain systems, enabling faster charging and longer driving ranges.

- Renewable Energy Systems: GaN transistors play a crucial role in grid-tied inverters and solar photovoltaic (PV) systems, enhancing energy conversion efficiency.
- Wireless Power Transfer: GaN transistors facilitate high-frequency resonant converters in wireless charging applications for smartphones, wearables, and electric vehicles [20].

2.1.2 Motivation of GaN inverter design

The motivation for GaN inverter design stems from the transformative capabilities of Gallium Nitride (GaN) transistors within the power electronics landscape. After years of development, GaN transistors have gained widespread acceptance in the market, emerging as a promising contender alongside traditional silicon (Si) and silicon carbide (SiC) semiconductors. This recognition has catalyzed advancements in various industries and research domains [2]-[6]. GaN's inherent properties, derived from its wide band-gap (WBG) nature, present a host of advantages over conventional semiconductor materials. With a band gap exceeding 3.4 eV, GaN exhibits a superior critical breakdown electric field, enhanced radiation resistance, and elevated electronic saturation velocity [21]-[25]. These attributes make GaN transistors well-suited for demanding applications, particularly in motor drive systems.

In motor drive applications, where efficiency and compactness are paramount, GaN technology shines. The quest for low losses and high switching frequencies is pivotal in increasing power density and system compactness [26]. Elevated pulse-width modulation (PWM) switching frequencies, facilitated by GaN transistors, yield multiple benefits. They reduce motor current ripple, diminish noise, and curtail losses in alternating current (AC) motors. Moreover, higher switching frequencies enable the downsizing of passive components such as LC filters, thereby fostering the generation of ideal sinusoidal output waveforms and overall system efficiency enhancements [27]-[28].

However, achieving the full potential of GaN-based inverters necessitates robust gate drive circuitry. GaN transistors impose stringent requirements on gate voltage management, demanding sophisticated gate drive designs. In the realm of three-phase inverters, intricate gate drive circuits have been traditionally employed, often laden with excess components. This approach, while effective, can inadvertently amplify gate loop parasitic inductance, attributable to the presence of equivalent series inductance (ESL) within the system [29]-[30]. In contrast, the half-bridge topology, a fundamental structure prevalent in various power converters including inverters, offers a simpler, cost-effective solution. Bootstrapping circuits, commonly integrated into half-bridge configurations, efficiently supply the voltage necessary for high-

side transistor operation. This streamlined approach mitigates complexity and cost while maintaining performance integrity [29]-[30].

Furthermore, efforts from industry players like EPC, Navitas, and Power Integrations have focused on the monolithic integration of GaN High Electron Mobility Transistors (HEMTs), gate drivers, and logic circuits. While promising, such integrated solutions face challenges regarding cost, complexity, and design flexibility, potentially limiting their widespread adoption [29]-[30].

2.1.3 Review of GaN power transistors and packaging technologies

GaN Power Transistors:

- Device Structures: GaN power transistors typically come in two main configurations: Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) and High Electron Mobility Transistors (HEMTs). HEMTs, in particular, are widely used due to their high electron mobility and low on-resistance.
- Manufacturing Processes: GaN transistors are typically fabricated using epitaxial growth techniques such as Metal Organic Chemical Vapor Deposition (MOCVD) or Molecular Beam Epitaxy (MBE), followed by advanced lithography and etching processes.

Packaging technologies:

- Chip-scale Packaging: Chip-scale packaging (CSP) techniques aim to minimize the size and weight of the package while maximizing thermal performance. This includes direct attach methods where the GaN die is mounted directly onto a substrate, such as copper or ceramic, to enhance heat dissipation.
- Enhanced Thermal Management: Advanced packaging technologies incorporate features like thermal vias, heat spreaders, and solder-based interfaces to improve thermal conductivity and heat dissipation. Additionally, techniques such as flip-chip bonding and embedded cooling structures help to mitigate thermal issues.
- Integration with Gate Drivers: Packaging solutions often integrate gate driver circuits and control electronics alongside the GaN power transistors to enhance system-level performance and reliability.
- Hermetic vs. Non-Hermetic: Depending on the application requirements, GaN transistors may be packaged in hermetic or non-hermetic packages. Hermetic

packages provide superior protection against environmental factors such as moisture and contaminants but are often more expensive.

Challenges and future directions:

- Reliability and Yield: Despite their numerous advantages, GaN power transistors face challenges related to reliability and manufacturing yield. Issues such as defects in the epitaxial layers, gate oxide reliability, and gate oxide charging can impact device performance and longevity.
- Cost Reduction: The high cost of GaN substrates and manufacturing processes presents a barrier to widespread adoption. Research efforts are focused on developing cost-effective production techniques and improving wafer yield to drive down costs.
- Standardization and Scalability: Establishing industry-wide standards for GaN device packaging and interconnect technologies is crucial for scalability and interoperability across different applications and manufacturers.
- Integration with System-Level Design: Future advancements will likely focus on tighter integration between GaN power transistors and system-level design considerations, including gate drive circuitry, thermal management, and control algorithms, to optimize overall performance and efficiency.

EPC and Panasonic utilize a similar approach involving a p-doped layer of Gallium Nitride (GaN) beneath the gate of their GaN transistors. This layer introduces a diode-like characteristic to the gate, which raises the threshold voltage by an amount equivalent to the diode's voltage drop. However, there are differences in their implementations. EPC's device exhibits a diode knee at around 5 volts, while Panasonic's occurs at approximately 3 volts. Consequently, EPC's transistors [31] are typically driven just below the diode knee, around 4.5 to 5 volts, while Panasonic's are driven above it, resulting in steady-state current flow into the gate. This deliberate injection of minority carriers enhances the conductivity of the two-dimensional electron gas (2DEG) and lowers the ON resistance, but it adds complexity to the gate drive design. HRL initially utilized plasma treatment to introduce fluorine ions beneath the gate, depleting the 2DEG until it's re-enhanced by a positive gate voltage. Later, they transitioned to a recessed gate structure, where the AlGaN beneath the gate is etched to a precise depth and replaced with an insulating material like Aluminum Nitride (AlN). This recessed gate technique is also adopted by other manufacturers like Exagan and NEC, sometimes alongside additional modifications to further increase the threshold voltage. Sanken has developed devices with a non-insulated recessed gate, but details regarding its current implementation are not publicly available. Another approach is the hybrid Metal-Insulator-Semiconductor Heterostructure Field-Effect Transistor (MIS-HFET), where the AlGaN layer

beneath the gate is etched away, removing the 2DEG. In this structure, the 2DEG on the drain and source sides of the channel must be connected by a Metal-Insulator-Semiconductor Field-Effect Transistor (MISFET) inversion layer beneath the gate to enable device operation. Additionally, Powdec has introduced an e-mode structure similar to a cascode, where the lower voltage device is fabricated on the top surface of the GaN device next to the HFET gate. While GaN Systems' [32] gate structure details are not publicly disclosed, their devices appear to feature an insulated gate similar to those seen in other manufacturers' implementations.

Table 2. 1 Commercial E-mode devices [36]

Manufacturer	Voltage Rating(V)	Current Rating(A)	$R_{ds,on}$(m Ohm)	Q_g (nC)	Package	Availability
EPC	30	60	1.3	20	Near Chipscale, LGA	Online Ordering
	40		1.5	19		
	60		2.2	16		
	80		2.5	15		
	100		3.2	13		
	200	9	43	1.8		
GaN Systems	650	7	220	1.5	Near-Chipscale	Online Ordering
		15	110	3.0		
		22	73	4.6		
		30	55	5.8		
		60	27	12		
	100	90	7.4	12		
		45	15	6.6		
Panasonic	600	15	65	11	TO220-DFN	Online Ordering
		10	155	--	DFN	
HRL	1200	10	500	--	--	Samples
	600	10	350	--	--	
Navitas	650	--	169	2.5	PQFN	Sample
Exagan	600	100	--	--	--	Unknown
	1200	100	--	--	--	

Powdec	1200	16	--	--	--	Unknown
Sanken	600	10	100	24	PQFN	Unknown
		20	50	30		

The survey indicates that GaN Systems' GS66516 series device stands out as the most suitable discrete device for high-power, high-density inverters among various alternatives. GaN Systems' die fabrication technology enables significant scalability in the GaN High Electron Mobility Transistor (HEMT) die area, distinguishing it as the first company to offer a 650V discrete GaN device with a remarkable 60A current rating. This scalability not only enhances versatility but also positions GaN Systems as a leader in pushing the boundaries of device performance. Moreover, GaN Systems [32] employs a laminated Surface Mount Device (SMD) package for their GS66516 series, a design feature that delivers exceptional benefits. This package design achieves ultra-low package inductance while facilitating top-side cooling simultaneously. By integrating these features, GaN Systems eliminates the need to parallel multiple GaN devices to achieve high current ratings. As a result, the GS66516 series enables direct high current ratings, enhancing both the power density and reliability of the inverter system. In summary, GaN Systems' GS66516 series offers a compelling solution for high-power, high-density inverters, leveraging cutting-edge die fabrication technology and innovative package design to deliver exceptional performance, scalability, and reliability.

2.2 Component selection for the design

In designing a three-phase inverter system, we focus on three main components: the three-phase inverter itself, the gate drive circuit, and the power supplies.

Three-phase inverter

The key components of the inverter section are the power transistors and the DC-link capacitor. Based on our research highlighted in the previous section, we have specifically chosen the GaN HEMT GS66516 series manufactured by GaN Systems for this design.

a) Power transistors

Commercially available GaN HEMTs come in different configurations for heat dissipation: top-side cooling, bottom-side cooling, and double-sided cooling. Top-side cooling transistors have their thermal pads on the top side, allowing direct attachment to an external

heatsink. However, it's important to use interface material with High Voltage (HV) insulation between the thermal pad and heatsink to enhance heat transfer and prevent short circuits. On the other hand, bottom-side cooled transistors have their substrate at the bottom, requiring heat dissipation through the FR4 PCB board using thermal vias. However, this can create a conflict between heat dissipation and current flow path, limiting overall electrical performance. Double-sided cooling packages offer superior thermal resistance compared to single-sided cooling but pose challenges in balancing cooling design complexity with system requirements. Considering heat dissipation and performance, we've chosen the GS66516T from GaN Systems. This selection is based on GaN Systems' GaNPX® packaging technology [33], which ensures low inductance (less than 1nH) and low junction-to-case thermal resistance (0.2°C/W) in a compact package. This makes the GS66516T the first 650V discrete GaN device with a high current rating of 60A. By avoiding the need to parallel multiple devices to achieve high current ratings [34] - [35], the GS66516T allows for efficient operation, with at least 30A AC operation capability.

b) DC link capacitor:

In a three-phase inverter system, the DC-link capacitor plays a crucial role in providing a stable DC voltage to the main power bridges while driving an AC motor as in Figure 2.3. It ensures smooth operation by addressing two key functions:

Absorbing high-frequency currents: as the frequency increases, the inductive parasitic impedance in the power supply and cables also increases. However, the impedance of the DC link capacitor decreases, allowing it to absorb high-frequency components of AC (ripple current). This helps maintain a low impedance path for high-frequency currents, ensuring smooth operation of the system.

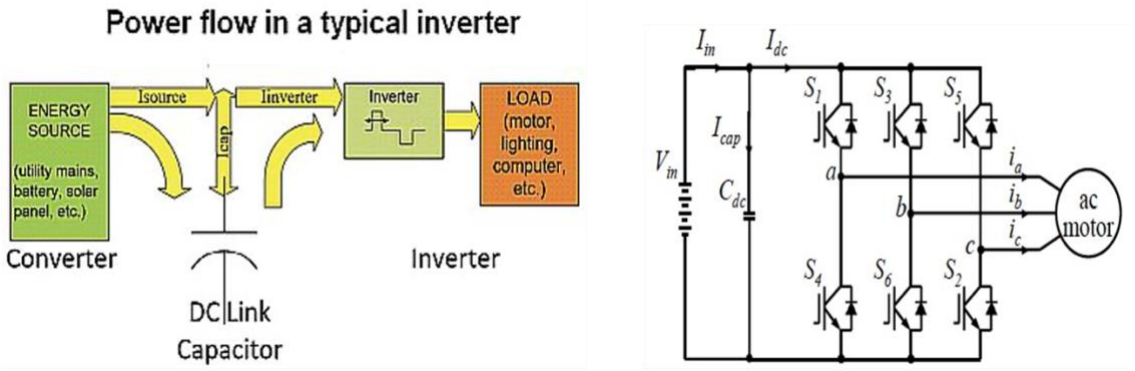


Figure 2. 3 Power Flow Diagram in a VSI and a simplified circuit diagram of VSI. [37]

Stabilizing the DC Bus: stray inductance in the DC voltage source can cause voltage fluctuations on the DC bus, leading to a ripple in the output current. The DC-link capacitor helps stiffen the DC bus by removing the effects of stray inductance, ensuring a stable DC voltage supply to the main power bridges.

$$C = \frac{I_{rip}}{\Delta\frac{V_{rip}}{T}} \tag{2-1}$$

$$I_{rip} = \frac{(I_{load,max} \times D)}{f_{sw}} \tag{2-2}$$

$$\Delta V_{rip} = \frac{(I_{load,max} \times ESR)}{C \times f_{sw}} \tag{2-3}$$

The root mean square (RMS) value of the input current in an inverter can be separated into two components: a direct current (dc) component and an alternating current (ac) component. The AC component, which represents the fluctuating part of the current, is absorbed by the DC-link capacitor. Consequently, the rms value of the capacitor current can be calculated based on this absorbed AC component. The ESR of the capacitor affects the voltage ripple and power losses. It should be kept low to minimize losses.

$$I^2{}_{rms} = I^2{}_{ac,rms} + I^2{}_{dc} \tag{2-4}$$

$$Irms = \frac{I_m}{\sqrt{2}} \times \sqrt{\frac{2\sqrt{3}}{\pi} \times M\left(\frac{1}{4} + \cos^2\varphi\right)} \tag{2-5}$$

$$I_{dc} = \frac{3}{4} M I_m \cos\varphi \tag{2-6}$$

References [38] and [39] provide detailed analyses and derivations for determining the rms and average value currents in the inverter. These calculations involve the modulation index (M), the peak value of the phase current (I,), power factor (cosφ), and the angle between the current and voltage vectors (φ).

$$I_{c,rms} = I_{n,rms}\sqrt{2M\left[\frac{\sqrt{3}}{4\pi} + \cos^2\varphi\left(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M\right)\right]} \tag{2-7}$$

Substituting the derived expressions for rms and average currents into the equation for the capacitor current, we obtain a formula for the rms value of the capacitor current. This formula accounts for factors such as modulation index, power factor, and peak phase current, enabling the calculation of the rms capacitor current. The modulation index (M) is a critical parameter that influences the capacitor current. For most Permanent Magnet (PM) motors, which typically have power factors between 0.70 and 0.95, the maximum capacitor current occurs when M is

in the range of 0.6-0.75. During this range, the capacitor current is approximately 0.55-0.65 times the phase current.

$$C_{dc_{min}} = \frac{I_{c,rms}}{\Delta V \times 2\pi f_{sw}} \quad (2\text{-}8)$$

When selecting the type of capacitor, film capacitors are preferred over electrolytic capacitors due to their high ripple current rating, low equivalent series resistance (ESR), and low equivalent series inductance (ESL). While electrolytic capacitors have a higher capacitance-to-volume ratio, they suffer from higher ESR and ESL, requiring multiple capacitors to be connected in parallel to reduce parasitic parameters. However, this increases the size of the inverter and reduces its power density, negating the advantages of GaN-based systems. Film capacitors offer higher volumetric efficiency and a longer working lifetime compared to electrolytics, making them the preferred choice.Therefore, the DC-link capacitor can be sized based on the rms capacitor current, considering the allowable ripple voltage (ΔV) [40]. In this design, a capacitor with a voltage rating of 700V and a capacitance of 160μF is selected to meet the system requirements. For this design, three DC link capacitors (MKP1848650094Y5) rated at 50uF, and 900V are used for the better PCB layout.

c) Gate drive circuit:

Bootstrap topology:

In gate driver design for inverters, the bootstrap topology plays a pivotal role in efficiently driving high-side power MOSFETs or IGBTs. Its primary function is to ensure proper gate voltage levels for these high-side switches, especially when they are floating with respect to the ground reference. This topology employs key components such as a bootstrap capacitor, bootstrap diode, and optionally, a bootstrap resistor. During the low side switch's ON period, the bootstrap capacitor is charged to a voltage higher than the supply voltage through the bootstrap diode as shown in Figure 2.4. This capacitor stores the necessary charge to provide an elevated gate voltage for the high-side switch during its turn-on period [41]. When the low side switch turns off, and the high side switch needs to turn on, the gate driver utilizes the charge stored in the bootstrap capacitor to elevate the gate voltage of the high-side switch facilitating its turn-on. This cyclic process ensures proper switching of both low and high side

switches in the inverter, enabling efficient operation of the power conversion system. To ensure effective implementation of the bootstrap topology, several considerations must be considered.

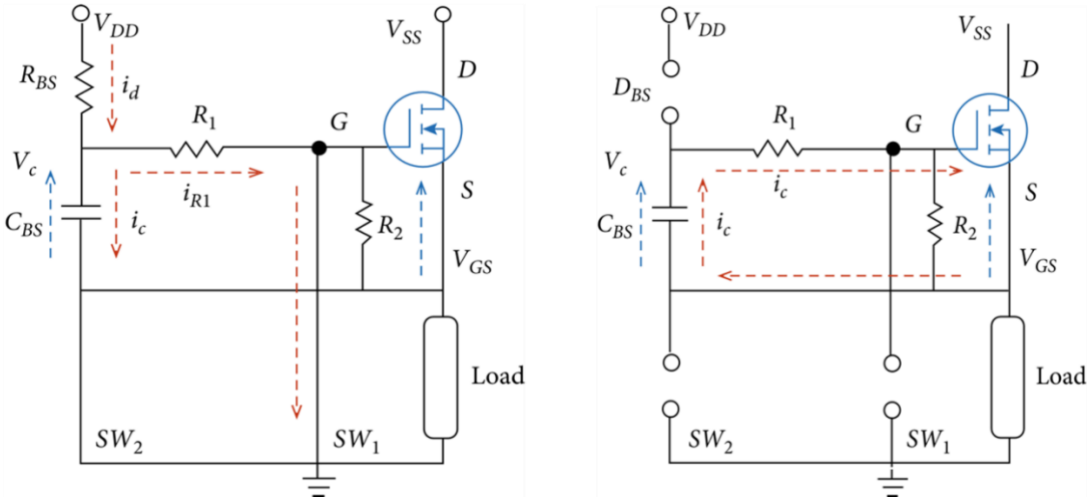


Figure 2. 4 Charging and discharging modes of the bootstrap circuit. [39]

Proper sizing of the bootstrap capacitor is crucial to maintain the required gate voltage for the high side switch during its ON period. Additionally, careful selection of the bootstrap diode is essential, as it must possess fast switching characteristics and low forward voltage drop to minimize losses and the variation of the bootstrap capacitor is shown in Figure 2.5. The inclusion of a bootstrap resistor, while optional, can help limit the charging current to prevent excessive stress on the gate driver and power supply. However, it's important to note that the bootstrap topology adds complexity to the gate driver circuit compared to direct gate drive configurations and is sensitive to layout and parasitic capacitances, which can affect its performance. Nevertheless, despite these challenges, the bootstrap topology remains a widely used and effective solution for driving high-side switches in floating configurations, offering simplicity and efficiency in gate driver design for inverters.

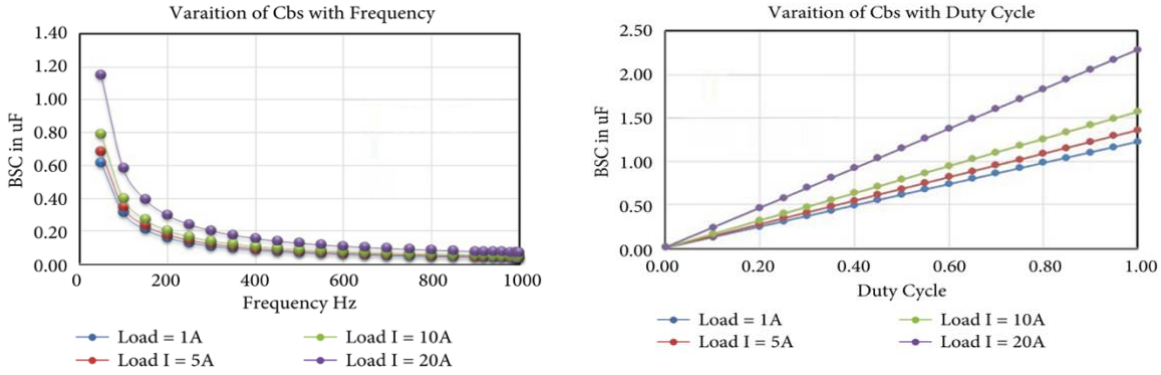


Figure 2. 5 Bootstrap capacitor variation with frequency and duty cycle [39]

- **Design of bootstrap capacitance:**

For the design of a Bootstrap capacitor, the Texas Instruments Handbook [42] of designing a bootstrap circuit is considered. Generally, the size of the capacitor is considered to be big enough to drive the High side GaN HEMT without depleting by more than 10%. So, the ratio of bootstrap cap and gate capacitance should be at least 10:1. The gate capacitance is calculated as follows: -

$$C_g = \frac{Q_g}{V_{q1_g}}. \tag{2-9}$$

$$V_{q1_g} = V_{DD} - V_{BootDiode} \tag{2-10}$$

Where Q_g is gate charge, $V_{BootDiode}$ is the forward voltage drop across the boot diode.

Now from this, the value of bootstrap can be calculated: -

$$C_{boot} \geq 10 \times C_g \tag{2-11}$$

Now, the peak current is also related to the bootstrap cap in the following way: -

$$I_{peak} = C_{boot} \times \frac{dv}{dt} \tag{2-12}$$

- **Design of bootstrap resistor:**

The bootstrap resistor serves a crucial role in the bootstrap circuit by controlling the peak currents flowing through the bootstrap diode during startup. Its selection is vital as it interacts with the bootstrap capacitor to establish a time constant, as described in the following equation

$$\tau = \frac{(R_{boot} \times C_{boot})}{\text{Duty Cycle}} \quad (2\text{-}13)$$

This time constant, occurring primarily during the high-side switch's off time, is influenced by the duty cycle. Essentially, the duty cycle represents the ratio of time the high-side switch is on versus off. When this duty cycle remains constant, changes in the bootstrap resistor and capacitor values affect the startup time. Increasing the value of the bootstrap resistor extends the time constant, resulting in a slower startup time. In other words, a higher resistance value slows down the rate at which the bootstrap capacitor charges and discharges. Consequently, tuning the bootstrap resistor and capacitor appropriately is essential to achieve the desired startup time for the high-side switch, ensuring optimal performance and efficiency in the power electronics system.

- **Gate resistors:**

Selecting gate resistors in gate driver design involves balancing several factors to optimize the performance and reliability of power electronic systems. Gate resistors control the switching speed of MOSFETs or IGBTs by influencing the rate of voltage change at the gate terminal. Higher resistor values slow down switching transitions, while lower values speed them up. Additionally, gate resistors dampen ringing and oscillations in the gate drive circuit, mitigating voltage spikes and EMI issues. They also contribute to gate drive losses, with higher resistor values increasing losses but providing overcurrent protection to the gate driver circuit. Thermal considerations are crucial, as gate resistors dissipate power and self-heat during operation, necessitating careful selection to ensure compatibility with expected operating conditions. By carefully evaluating these factors, engineers can choose gate resistors that strike an optimal balance between switching speed, ringing suppression, gate drive losses, overcurrent protection, and thermal considerations, thus enhancing the overall performance and reliability of the power electronic system.

From the second order system step response graph under different damping conditions, it becomes evident that a damping ratio of $\zeta = 0.8$ is a suitable choice to ensure a rapid rise time while effectively limiting oscillations in V_{gs}. Considering the capacitance of C_{gs} and assuming that the gate inductance is primarily influenced by the ferrite bead, an external gate resistor of

10 Ohms is opted for the turn-on process, following consideration of the internal parasitic gate resistance as outlined in reference [43]. This selection aims to strike a balance between achieving fast switching times and minimizing potential oscillations, thereby enhancing the overall performance and reliability of the GaN HEMT device. According to the Gate drive design application from GaN systems, the ratio of the gate off resistor to the gate on resistor should be 5 to 10 times greater. Therefore, given the inherent parasitic resistance within the gate electrode of the GaN HEMT, a gate-off resistor of 1 Ohm is chosen for the turn-off process. While this selection may result in a minor negative overshoot during turn-off, it is deemed acceptable considering that the negative gate-to-source voltage is rated at -10V, as specified in reference [44]. Hence, any slight spike observed during the turn-off transient is not expected to present a significant risk or pose a threat to the device's operation or reliability.

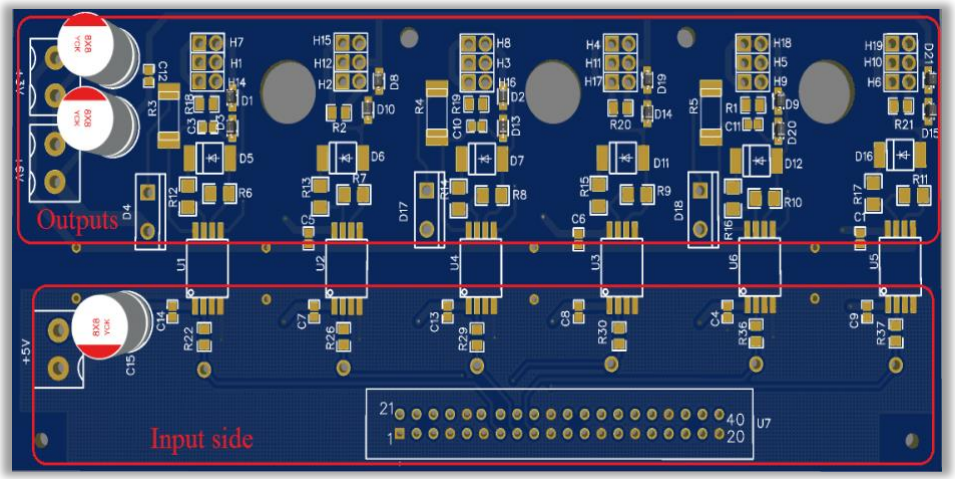


Figure 2. 6 Gate driver board layout with isolation in the input and output side [101]

d) Power supplies

The power supplies integrated into the GaN inverter system consist of one Sorenson DLM600-6.6E power supply (Figure 2.7) and two RIGOL DP832 (Figure 2.8) units. One RIGOL DP832 model serves the gate driver circuitry by delivering both 6V and 3V outputs, catering to the varied voltage requirements of the gate driver components as shown in the layout in Figure 2.6. This power supply is responsible for the output side of the Gate driver. Additionally, the second RIGOL DP832 unit provides an isolated 5V output specifically dedicated to the gate driver, enhancing safety and stability by minimizing interference. This DC supply is responsible for the input side of the Gate Driver. That's the reason these supplies are kept isolated from each other. Meanwhile, the Sorenson DLM600-6.6E (Figure 2.7) power supply is employed to power the DC link of the GaN inverter board, ensuring reliable and

appropriately regulated power delivery to the main power stage of the inverter. Through the combination of these power supply units, the GaN inverter system benefits from precise voltage control, stability, and efficiency across its various operational components.

Figure 2. 7 Power supply for DC link

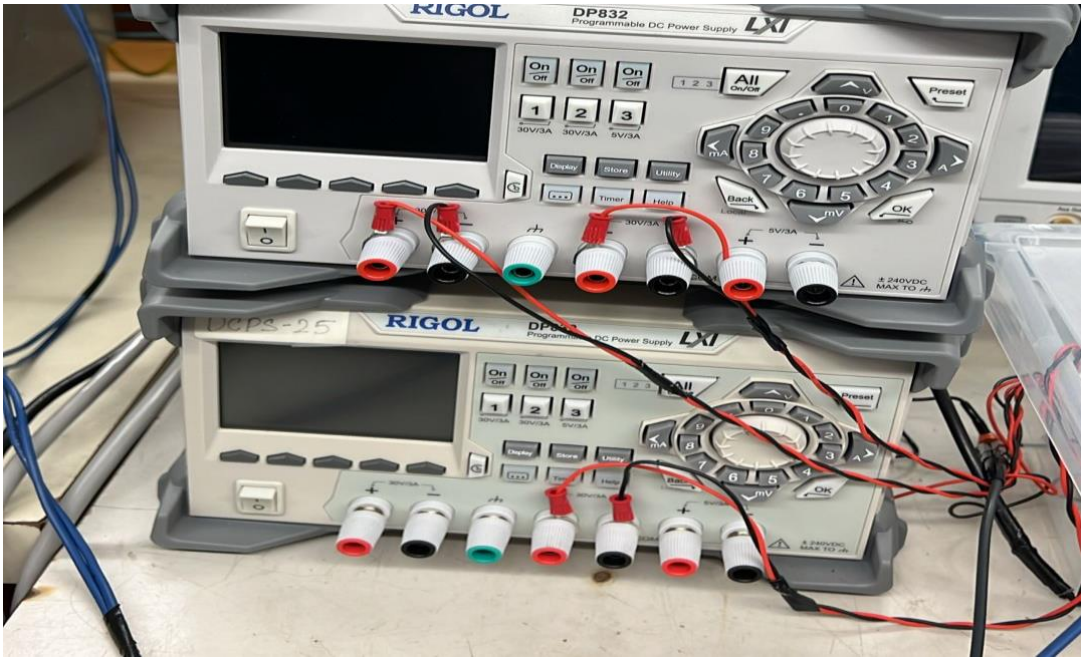


Figure 2. 8 Two isolated RIGOL DC power supplies for input/output side of the gate driver board

2.3 Single-phase R-load test

The single-phase R-load test conducted on the GaN inverter system involved a comprehensive evaluation of various components and functionalities to ensure proper operation and performance. Initially, meticulous attention was given to checking all signals within the gate driver board. Two isolated power supplies were employed to provide the necessary voltages, with one supplying +6V and 3V, and the other delivering +5V. This setup ensured precise voltage control and minimized interference, essential for reliable gate driver operation. The gate driver board was then subjected to rigorous testing by supplying PWM signals from a C2000 TI microcontroller, specifically the TI F28069 Piccolo. Each gate driver was meticulously tested by supplying PWM high and low signals to ascertain proper functionality and response.

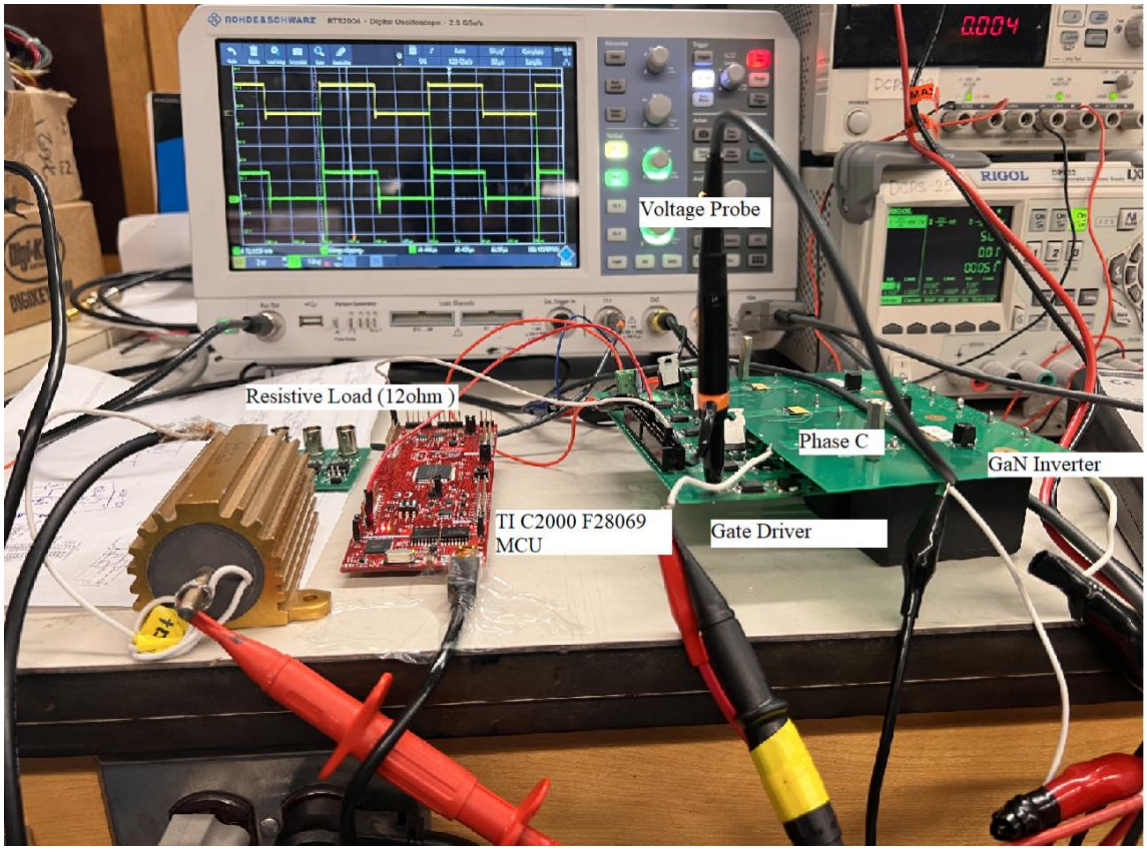


Figure 2. 9 Single phase R-load test setup

Subsequently, the focus shifted to testing the GaN inverter board to verify if the GaN switches were receiving the gating signals as intended. This step is crucial in ensuring that the gate driver signals are effectively transmitted to the power stage of the inverter. Following successful verification of the gating signals, the next phase of the test involved assessing the

GaN output for just one phase using a small 12.7-ohm resistive load as shown in Figure 2.9. This test served to validate the switching operation of the GaN inverter as shown in Figure 2.10 and under load conditions mentioned in Table 2.2.

Table 2.2 Experimental Specification

Parameter	Value
Amplitude Modulation Ratio (m_a)	0.9
Fundamental Frequency (Hz)	60
Switching Frequency (KHz)	10
V_{bus} (V)	30
Resistive Load (ohm)	12.7

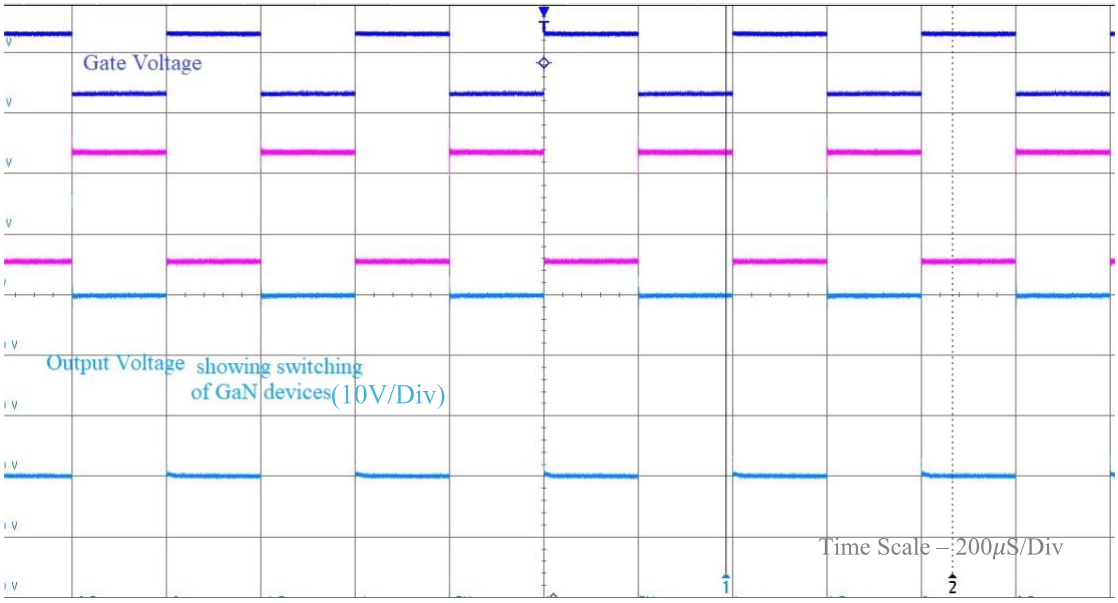


Figure 2.10 Verification of gating signals receiving from the gate driver to the inverter board

It's important to note that during the test, the DC link voltage was not maintained at a high level, and the inverter was not tested in a continuous current state due to the absence of a heat sink design for the inverter at that stage. Without proper thermal management, continuous current operation could lead to excessive heat buildup within the inverter components, potentially causing damage or degradation of the board's performance and reliability. Heat dissipation is crucial in power electronic systems, especially during continuous operation, to ensure that components operate within safe temperature limits. By opting for a single-phase R load test instead, the risk of overheating and potential damage to the board is minimized, allowing for a safer and controlled evaluation of the system's functionality. Additionally,

focusing on a single-phase test provides an initial assessment of the inverter's performance, paving the way for further testing and optimization with proper thermal management measures in place. However, simulations were conducted in LTSpice, where a 400V three-phase inverter was designed, and waveform analysis as shown in Figure 2.11 was performed to simulate the expected behaviour of the inverter under a continuously loaded operating conditions.

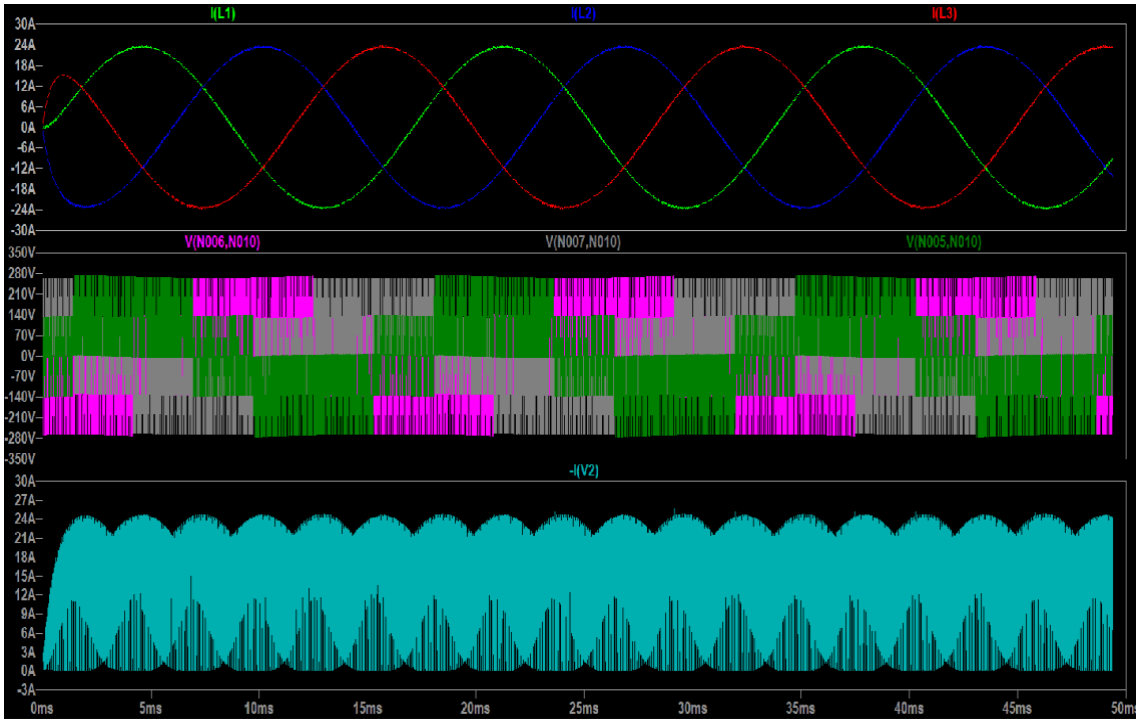


Figure 2. 11 Simulation waveforms in LT-Spice for 3-phase output

Overall, the single-phase R-load test provided valuable insights into the performance and functionality of the GaN inverter system. By meticulously examining various signals, testing the gate driver board, verifying gating signals to the GaN switches, and conducting switching tests under load conditions, the test served to validate the design and functionality of the GaN inverter system, laying the groundwork for further optimization and development.

2.4 Double pulse test experiment

The double pulse test (DPT) is a crucial experimental technique employed in the field of power electronics for characterizing the switching behaviour of semiconductor devices, such as transistors and diodes. It offers a comprehensive means of analyzing the transient response

during turn-on and turn-off events, providing valuable insights into device performance and efficiency. Below is a detailed overview of the key aspects of the DPT:

Purpose:

The primary purpose of the double pulse test is to evaluate the switching characteristics of semiconductor devices under realistic operating conditions. By subjecting the device to two consecutive gate pulses, the DPT allows researchers to capture and analyze the transient waveforms of voltage and current during both turn-on and turn-off transitions. The turn-on pulse duration can be calculated using the following equation:

$$V_{\text{load}} = \frac{\text{Ldi}_{\text{load}}}{\text{dt}} \tag{2-14}$$

with the initial condition $V_{\text{load}} = V_{\text{DC}}$. After integrating the above equation, substituting i_{load} with the desired test current I_{Test} ($i_{\text{load}} = I_{\text{Test}}$) leads to the pulse duration (τ_1) for the first pulse (the parasitic series resistance RS is neglected):

$$\tau_1 = \text{L}_{\text{load}} \times \frac{\text{I}_{\text{test}}}{\text{V}_{\text{dc}}} \tag{2-15}$$

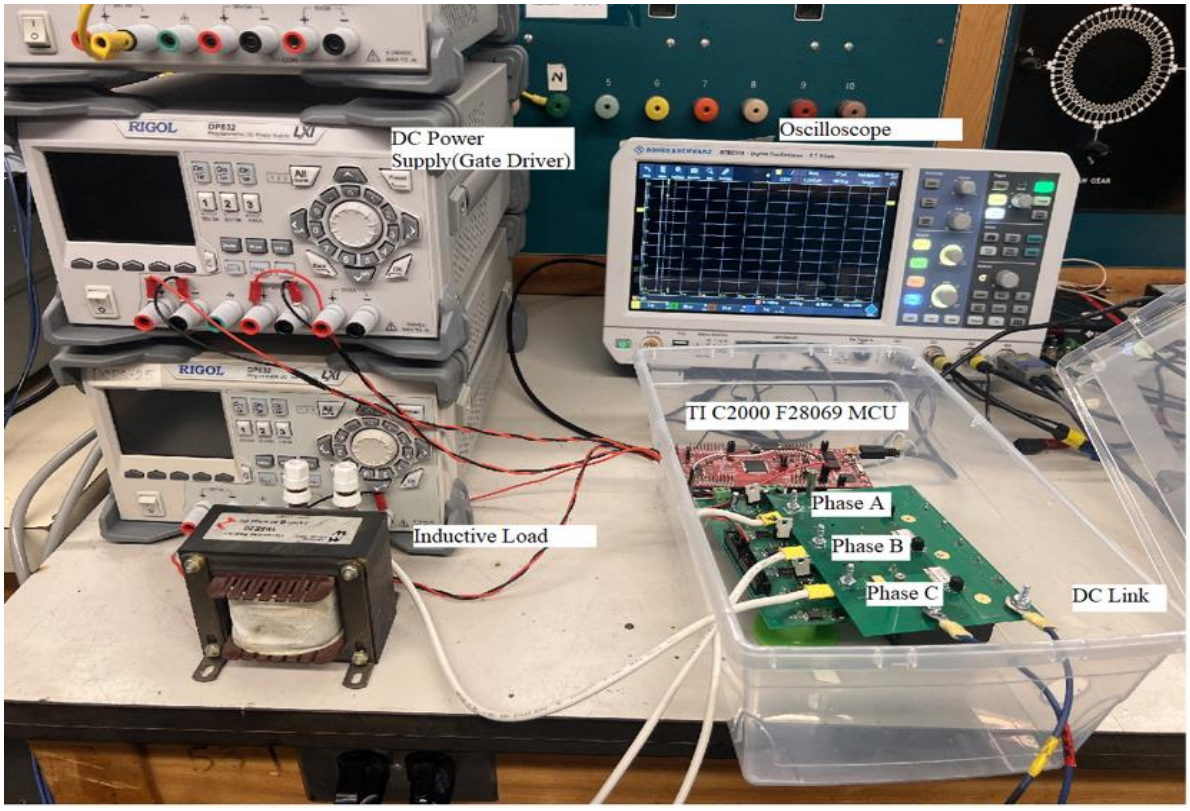


Figure 2. 12 DPT hardware setup

2.4.1 Experimental setup

In the first test of the double pulse experiment (Figure 2.12), the focus lies on the switching-on transient process during the second gate-on pulse, with the first pulse dedicated to charging the inductor current to 5A. This ensures that the measured switching-on loss during the first gating-on interval does not include the energy contributed by the load current. When the gate-off signal is applied to the DUT (Device Under Test), specifically the high-side switch, a brief dead time of 30 ns occurs before the low-side switch is activated. During this interval, the energy stored in the inductor from the previous stage is released, causing the current to circulate through the low-side switch and the load. Consequently, the current in the up-side switch decreases to zero. Subsequently, the second gate-on pulse is generated to re-enable the DUT under the switching condition of V_{DS}=100/200/400 V, while the I_{DS} remains at 5 A due to the insignificant reduction in the inductor current. Throughout this period, voltage and current waveforms are recorded to illustrate the transient process as shown in Figure 2.13. The absence of a heat sink in the design leads to increased switching losses.

The experimental waveforms depicted in Figure 2.13 reveal a noticeable ringing in the current at the initial stage of turning on, attributed to parasitic stray inductance in the DC bus and the half-bridge module. This ringing results in higher losses compared to ideal conditions. However, the primary spike in rising current contributes the most to these losses, including additional loss induced by displacement current, as discussed previously. Following the initial overshoot of current, although ringing persists, the voltage across the GaN device decreases to nearly zero. As a result, subsequent losses stemming from the remaining current ringing have a negligible impact on the estimation of switching-on losses. These observations align with the turn-on transient model proposed in [100], validating its consistency with the experimental waveform tendencies.

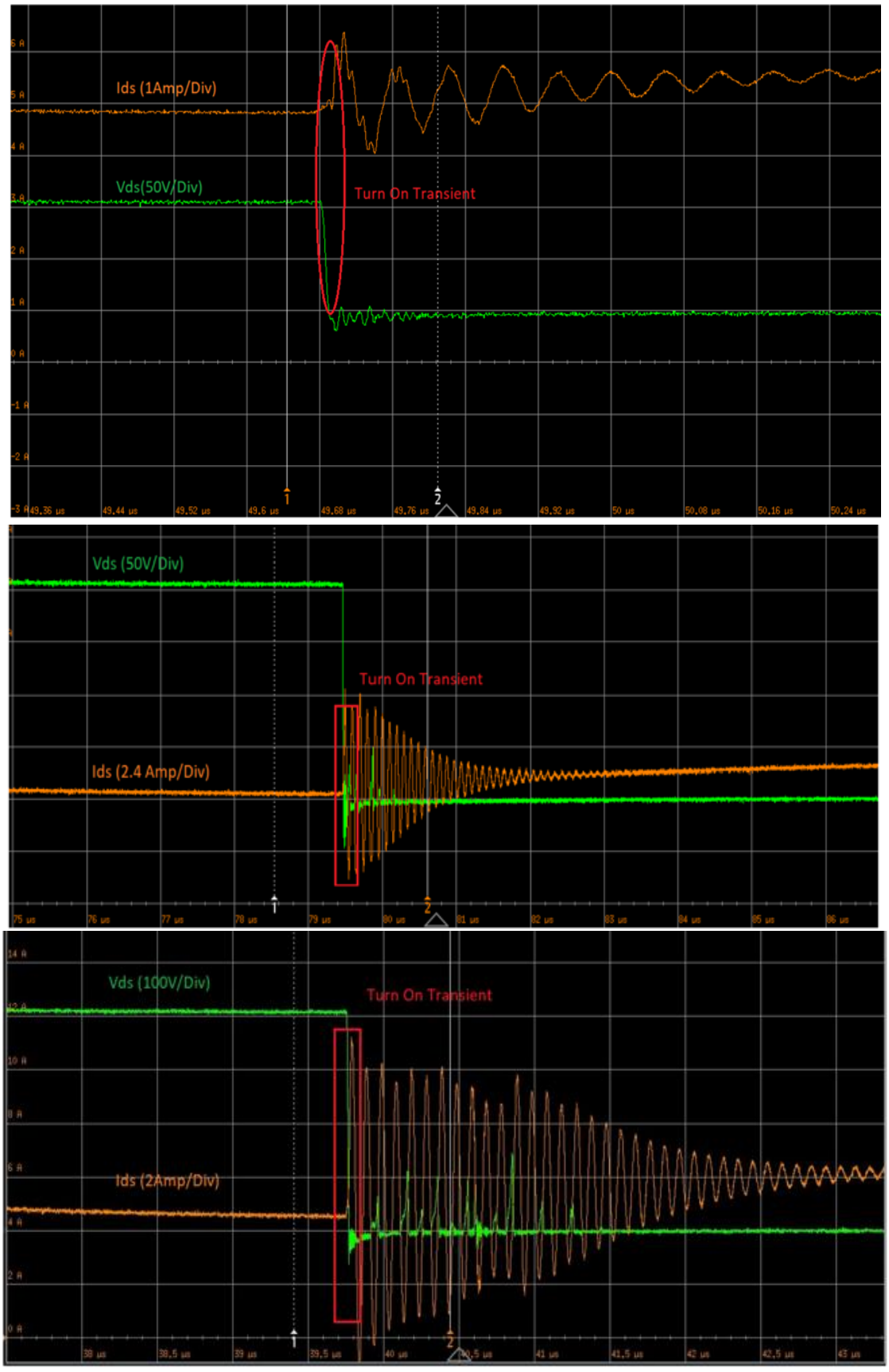


Figure 2. 13 Turn on transients at 100/200/400V and I_{ds}=5Amps

In the turn-off transient, the DUT transitions from the on-state to the off-state when the gate pulse is removed. Similar to the turn-on transient, the turn-off process is characterized by rapid changes in voltage and current. Analysis of the turn-off waveforms provides insights into parameters such as turn-off time and reverse recovery behaviour in diode-based devices. From the experimental data, it can be proved that the loading conditions affect the switching speed of GaN devices. For the data, two different loading conditions of 1mH and 2.5mH are introduced to calculate the turn-off time of the GaN device. The turn-off voltage transients are shown in the Figure (2.14).

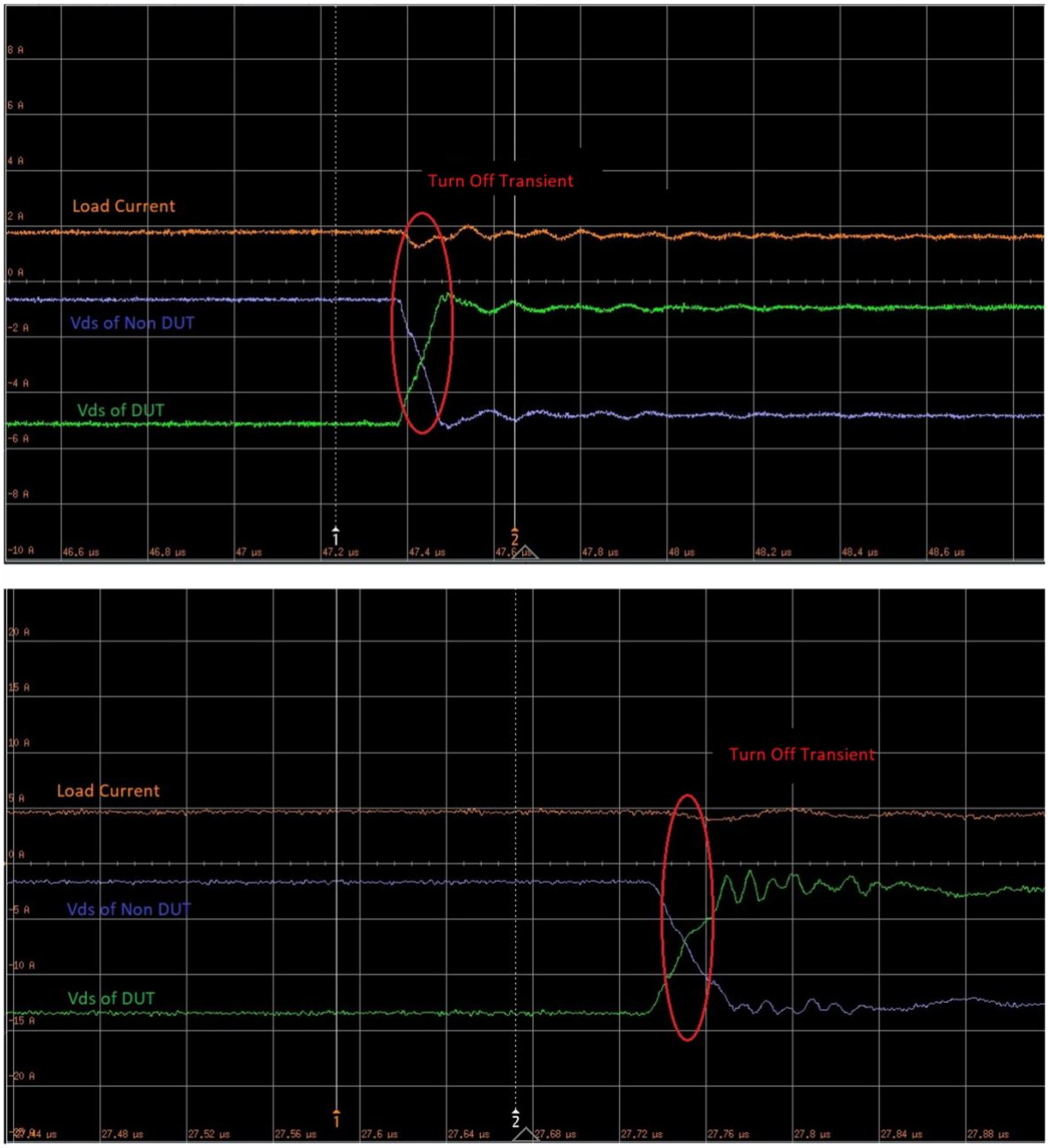


Figure 2. 14 First, turn off ringing oscillations at V_{ds}=100V and I_{ds}=2/5Amps

2.4.2 Results and discussion

The results of this design of a three-phase inverter are compared with a previous version of GaN inverter design that did not consider optimizations of the layout and parasitic components. In Table 2.2, the comparison of turn-off time was made between the previous version and the improved design. It is obvious from the results that the turn-off time is decreased and the GaN device is switching at a faster speed and the results are closer to the turn-off time estimated from the analytical model. Since the stray inductances are not taken into consideration, the experimental results are different than the simulation and theoretical calculations. In the new design, the parasitics are improved in the board layout, and less time was needed by the switches to achieve a fully off state as compared to the previous version.

Table 2. 2 Turn-off time estimation comparison.

100V	Proposed Method (nS)	Previous Design(nS)	New Design(nS)
5A	29	32	29.4
2A	72.4	80	75.2

Table 2. 3 Turn on Loss Estimation Comparison

5 A	Proposed Method(μJ)	Previous Design(μJ)	New Design(μJ)
200V	14.019	19.921	24.67
400V	19.921	44.037	48.63

In Table 2.3, the turn-on loss estimation is compared, and it was found that the losses in the new design are increased because of the absence of a heat sink. However, as a rough estimate, a well-designed heat sink can typically reduce the temperature of the semiconductor device by 20% to 50% or more compared to operating without a heat sink. Then in a similar percentage, the switching and conduction losses can be decreased as well. Therefore, with the proper heat sink design, it can be clearly said that the turn-on losses in the new design is going to be less than the previous design. So, this means that the proper heat sink design and layout of the power loop should be considered by designers to develop the GaN HEMT potential of high switching speed.

2.5 Parasitic component issues in GaN inverters

Background review: Gallium Nitride (GaN) technology has emerged as a promising candidate for power electronics applications due to its high electron mobility, fast switching speed, and excellent thermal conductivity [45]. However, the presence of parasitic components such as inductances, capacitances, and resistances poses significant challenges in the design and operation of GaN-based inverters.

Parasitic inductances, originating from bond wires, interconnections, and package leads, can lead to voltage overshoots, ringing, and voltage spikes during switching transitions [46]. Techniques such as layout optimization and advanced packaging technologies have been proposed to mitigate these effects [47]. Additionally, embedded GaN technologies have been investigated to reduce loop area and minimize parasitic inductances effectively [48].

Parasitic capacitances between different components within the inverter, including power devices, PCB traces, and gate drivers, can result in crosstalk, electromagnetic interference (EMI), and voltage/current overshoots [49]. Proper PCB layout and decoupling capacitor placement are crucial to minimizing these effects [50]. Advanced simulation tools and techniques are employed to accurately model and analyze parasitic capacitances for optimizing system performance [51].

Parasitic resistances, including the on-state resistance of GaN devices and resistance in conducting paths, contribute to power losses and efficiency degradation [52]. While GaN devices inherently offer lower on-state resistances compared to silicon-based devices, ongoing research focuses on further minimizing these resistances through device optimization and advanced packaging materials. Integrated approaches that encompass device design, packaging, and system-level optimization have emerged as promising solutions to address parasitic component issues comprehensively [53] [54] [55]. These integrated solutions aim to maximize the performance, efficiency, and reliability of GaN-based inverters by minimizing parasitic components and optimizing thermal and electrical characteristics. Reliability and robustness considerations are paramount in ensuring the long-term operation and durability of GaN inverters in practical applications [56]. Continued research and development efforts are essential to overcome these challenges and unlock the full potential of GaN technology in powering diverse industrial, automotive, and renewable energy systems.

2.6 Parasitic verification and extraction

A double pulse test is done to verify the parasitics in the power loop. Two pulses of the same width are injected into the Gate driver board to obtain the load current, DC waveforms with the switching behavior of GaN switches.

In this version of the design, instead of using a single lumped capacitor as the DC-link capacitor, distributed capacitors are utilized, with one capacitor for each phase. This configuration ensures that the length of every power loop is equal, as the DC capacitor effectively acts as the power supply as shown in Figure 2.15. By having equal loop lengths, the parasitic inductance of the PCB traces becomes more balanced, as the parasitic inductance is mostly dependent on the loop length when other parameters remain constant.

Moreover, the arrangement of the DC flowing out of the DC+ and flowing into DC- brings the benefit of magnetic flux cancellation as shown in Figure 2.16. This cancellation occurs due to the folding of the current path through the devices, increasing the mutual coupling between the current through the two devices. Additionally, mounting the DC-link capacitor near the devices minimizes the total parasitic inductance of the current commutation loop by promoting self-cancellation, compared to the previous design.

The side view of the layout further illustrates how the current through the top layer and the bottom layer are folded in opposite directions, enhancing magnetic field cancellation to reduce the parasitic inductance in the loop.

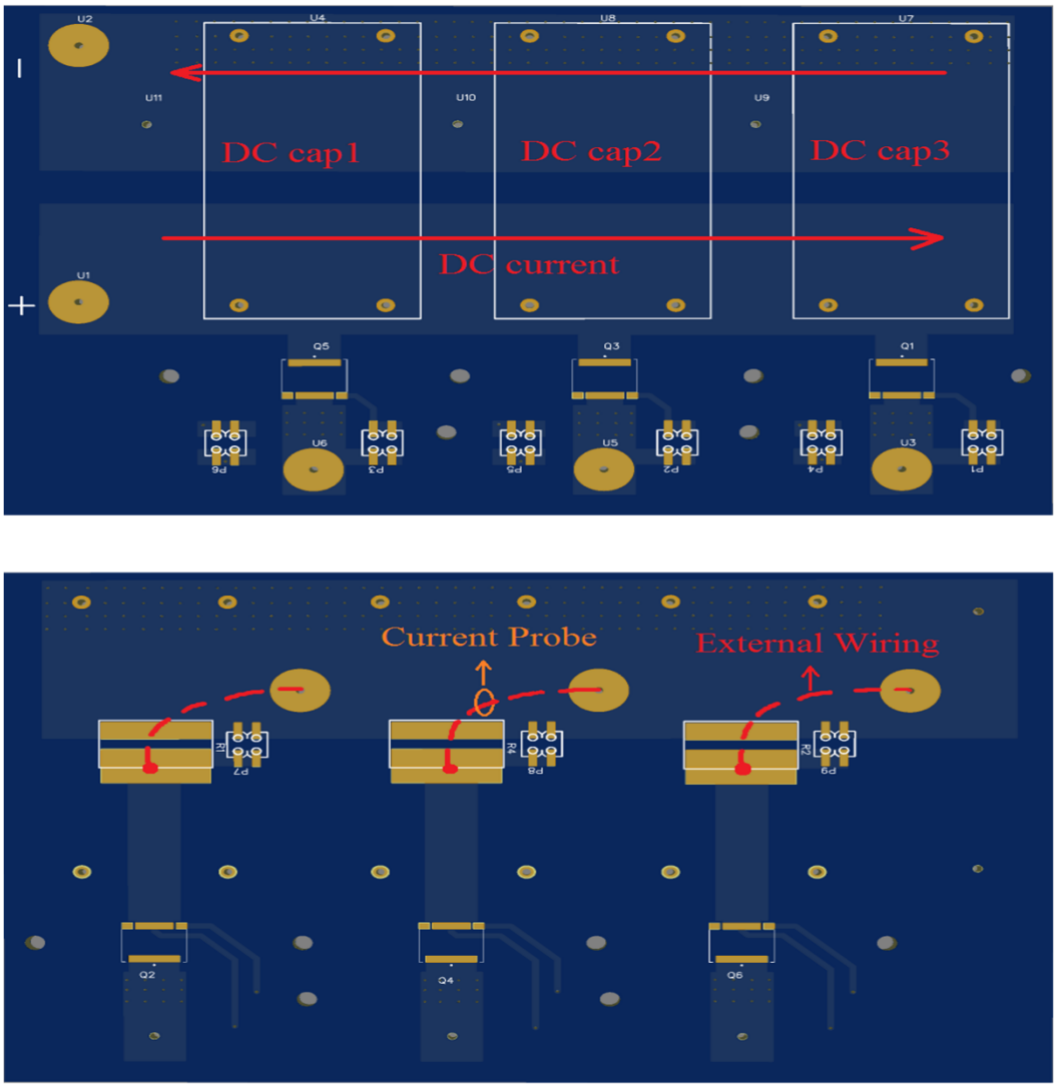


Figure 2.15 The top side and bottom side of the GaN inverter board designed for lower parasitics [101]

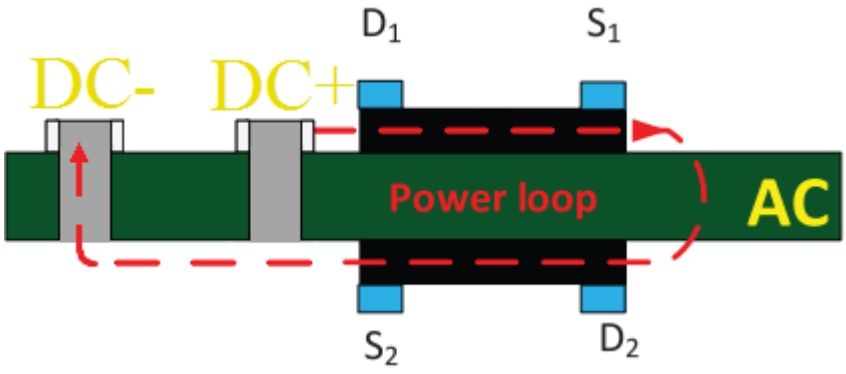
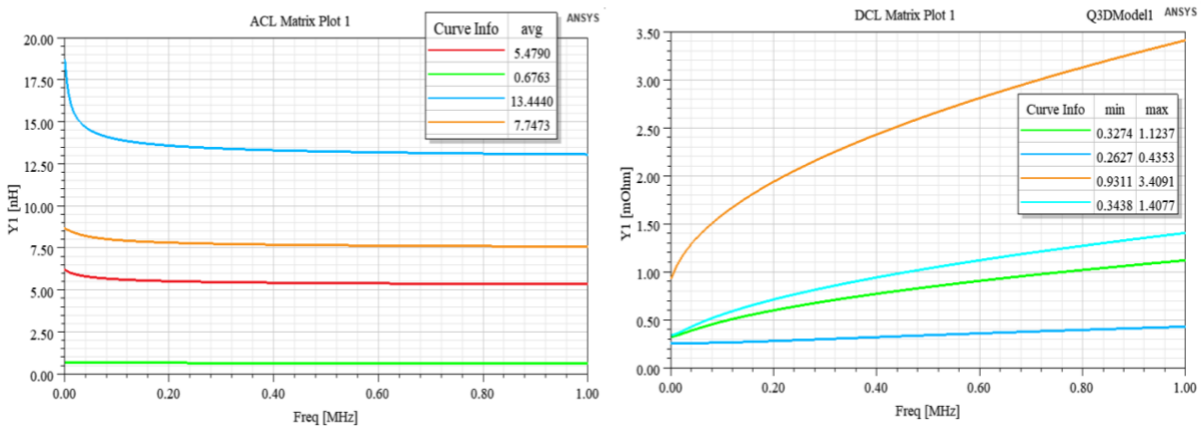


Figure 2. 16 Power loop for parasitic calculation [101]

The parasitics traces are extracted in Ansys Q3D simulation software as done in [57]. Q3D simulation results confirm that this version of the layout significantly reduces the total loop inductance for each bridge by approximately 60% compared to the previous version. In Figure 2.17, the traces are divided into the segmentation as shown in [57]. The results of parasitics from the simulations are summarized in Table 2.4.



(a) (b)

Figure 2. 17 Q3D simulation Result. (a) Parasitic inductance (b) Parasitic resistance.

Table 2. 4 Parasitic components extracted from Q3D simulation

Parameter	Value
Parasitic Inductance (L_{loop})	27.35 nH
Parasitic Resistance (R_{loop})	6.3758 mΩ

2.6.1 Experimental verification of parasitics

The experimental setup (Figure 2.12) for the double pulse test involves several components arranged systematically to evaluate the performance of the GaN-based inverter board.

- Gate Driver Board and Inverter Board: The gate driver board is positioned above the GaN-based inverter board using male/female pins on the gate and source electrodes. This setup allows for precise control over the switching behaviour of the GaN devices.

- GaN Devices: The inverter utilizes 650 V GS66516T GaN E-HEMTs from GaN Systems. These devices are responsible for the power conversion process in the inverter circuit.
- Control Signals: Control signals necessary for the operation of the inverter are generated by a TI C2000 MCU. These signals are transmitted to the gate driver board to control the switching of the GaN devices.
- Power Supply PCB: Functions as the various power supplies, providing the required voltages to the gate driver board and the DC link.
- Load Inductor: This represents the inductive load used in the double pulse test. This component is essential for simulating real-world operating conditions and evaluating the performance of the inverter under varying load conditions.

During the double pulse test, specific attention is given to the switching-off moment after the first pulse and the switching-on transient process during the second gate-on pulse. The test conditions and equipment used are summarized in Table 2.5.

Table 2. 5 Experimental specifications

Parameter	Specifications
Temperature	25°C(room temperature)
Switching Frequency (kHz)	10
V_{Bus} (V)	100
I_L (A)	5/2
$Rg_{(on)}/Rg_{(off)}$ (ohm)	10/1
Current Proble	Yokogawa 701933 50 MHz/30 Arms
Voltage Probe	Yokogawa 700924 Differential Probe/ 100MHz
Oscilloscope	Rhode & Schwarz RTB2004 2.5 GSa/s
DC Power Supply	Sorensen DLM600-6.6E

2.6.2 Results and discussions

The experiment was done at 100V DC supply, and the load current was kept around 5 amperes during the transition. The duty cycle was kept being 50% and the pulse width was calculated in the same way as done previously in the DPT. The output waveforms are captured in the Oscilloscope. Figure 2.18 represents the output load current waveforms. From the load current waveform obtained during the double pulse test (DPT), several conclusions can be drawn regarding its relationship with parasitic components in the power electronic circuit. Firstly, the oscillations or ringing in the load current waveform during the transients indicate the presence of parasitic inductances in the circuit—high-frequency components of the load current generally couple with parasitic capacitances, resulting in voltage transients and overshoots.

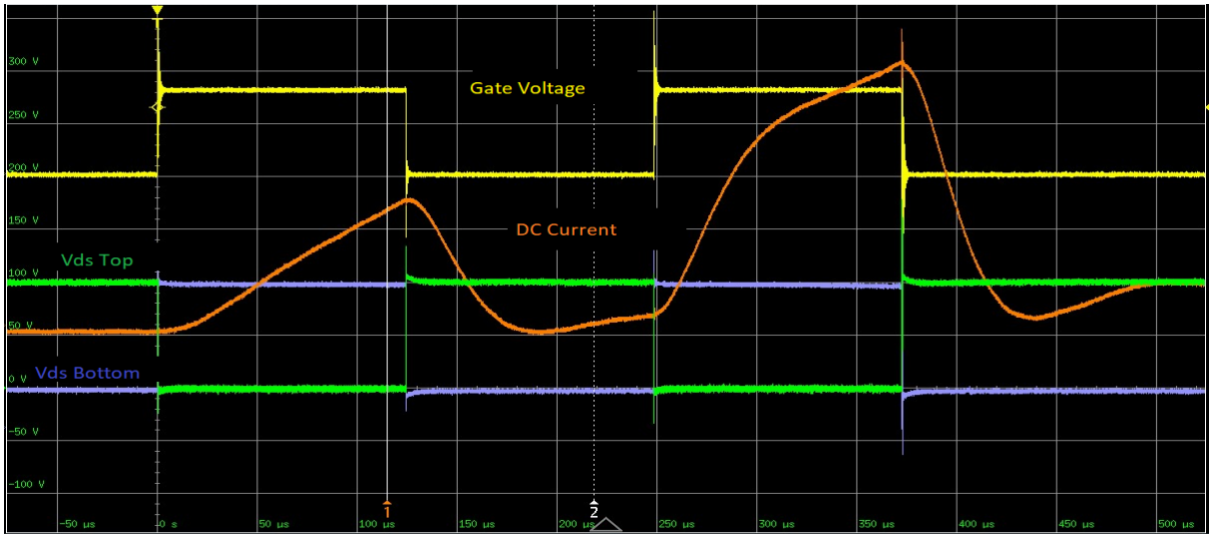


Figure 2. 18 Switching behaviour vs output load current

Figure 2.19 represents the DC bus current waveforms. From the waveform, it can be observed that there is no or negligible ringing in the DC bus current waveform during the transition. It implies that the parasitic inductance in the DC path of the circuit is likely low. The absence of ringing suggests minimal parasitic inductance affecting the DC path, which can be attributed to factors like a low loop area achieved through careful layout design, utilization of components with low parasitic inductances, and effective grounding technique.

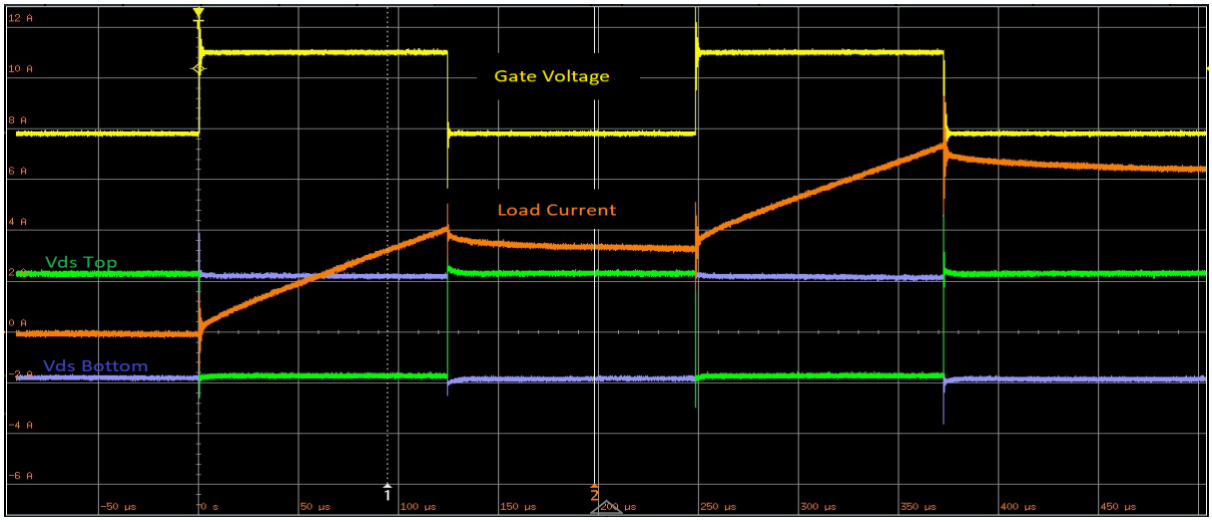


Figure 2. 19 Switching behavior vs DC behavior

From the experimental results of a turn-off oscillation, the turn-off ringing was calculated from the oscilloscope as shown in the waveforms in Figure 2.20. The parasitic inductances within the power loop can be evaluated by analyzing the oscillations in the turn-off transient.

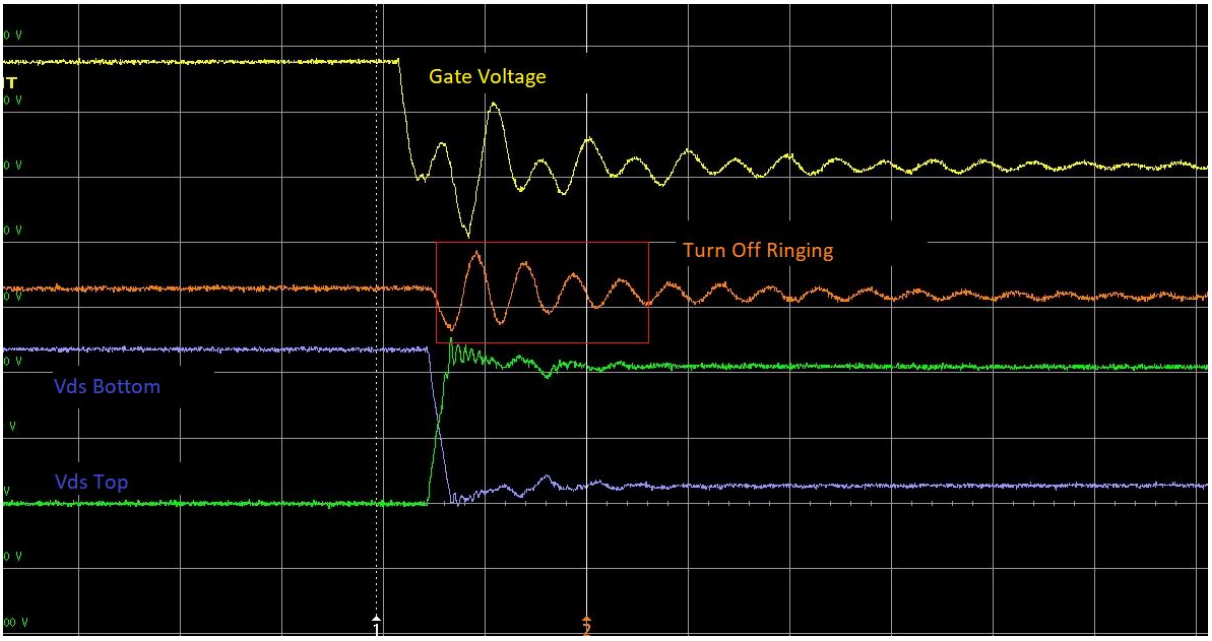


Figure 2. 20 Turn off ringing oscillator to calculate parasitic inductance.

This analysis considers one device in reverse conducting mode, with the turn-off device represented by three capacitors in a simplified circuit as shown in Figure 2.21(a) This circuit is further simplified into an equivalent RLC circuit as in Figure 2.21(b), where the resonance frequency of the turn-off waveform matches the oscillation frequency of the RLC loop [58]

[59]. By applying an approximation formula, the resonance frequency is calculated based on the capacitance extracted from the characteristic curve.

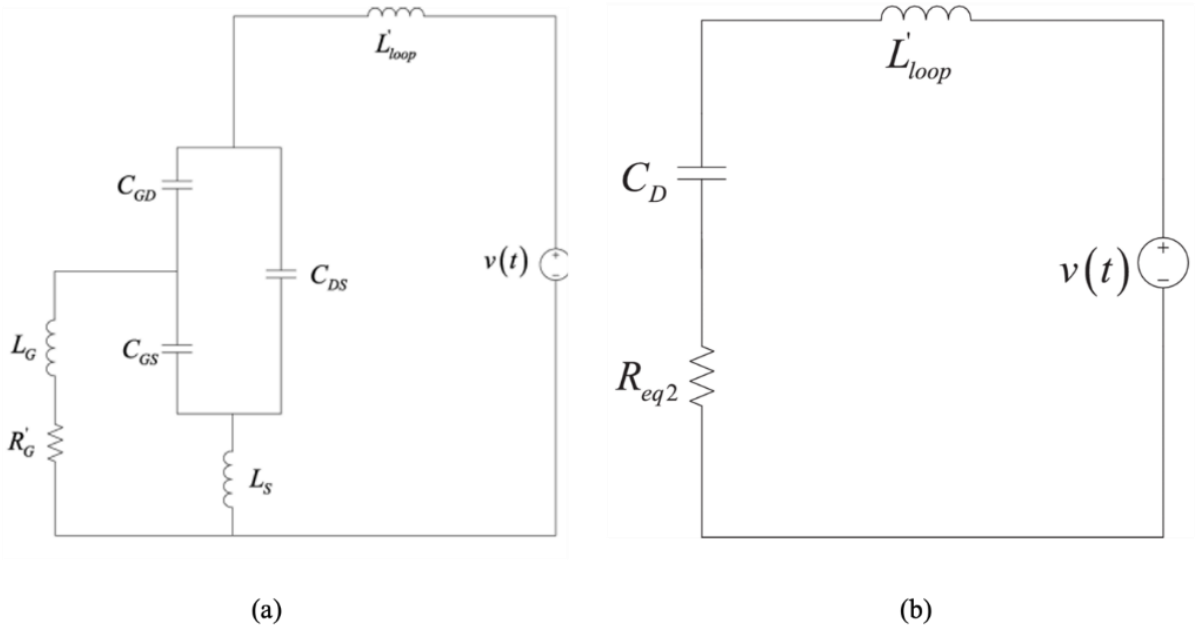


Figure 2. 21 (a) Simplified circuit for analysis of Turn off switching parasitics (b) simplified RLC circuit [58]-[59]

$$X_{C_D} = \frac{\left(X_{C_{DS}} \times X_{C_{GD}}\right)}{X_{C_{GS}} + X_{C_{DS}} + X_{C_{GD}}} \tag{2-13}$$

$$2 \times \pi \times f_{off} = \frac{1}{\sqrt{L_{loop} \times C_D}} \tag{2-14}$$

In this specific case, the capacitance (C_D) is determined to be approximately 370 pF, and the turn-off ringing from the waveform is observed to be around 46.27MHz, leading to the calculation of the loop inductance as 32.26nH. These results are consistent with those obtained from Ansys Q3D simulations, which show around 28 nH. Although there's a slight discrepancy between the simulation and calculation results because of the absence of a heat sink in the design, however still the results fall within an acceptable range. Consequently, the simulation results serve as validation for the analytical calculation method.

2.7 Conclusion

This chapter explains the design, simulation and experimental verification of a 3-phase GaN inverter, with enhancements to the design layout aimed at minimizing parasitic effects. Through experimental testing, the reduction fo the parasitic elements in the new layout is

verified. In addition, it brings extra benefits in reducing the turn-on energy losses and improving turn-off switching times.

Two double pulse tests were carried out to evaluate the performance enhancements achieved in the new design. In the first test, improvements in turn-on energy losses and switching times were observed, indicating the effectiveness of the design modifications.

Furthermore, the second double pulse test focused on verifying parasitic effects identified through Ansys simulation results. The analysis revealed enhancements in the power loop and DC loop parasitics, contributing to improved overall performance and efficiency.

Due to the high switching frequency inherent in Gallium Nitride (GaN) inverters and the presence of nonlinearities in their operation, the output current waveform of these inverters often exhibits significant harmonic distortion across a wide frequency spectrum. This distortion includes both low-frequency harmonics, stemming from the fundamental switching frequency and its multiples, as well as high-frequency harmonics resulting from rapid switching transitions and transient behaviours within the inverter circuitry. The presence of such harmonic distortions can have detrimental effects on the performance and efficiency of the overall system. Low-frequency harmonics can lead to voltage waveform distortion, increased losses in connected loads, and potentially violate regulatory standards for harmonic content in power systems. On the other hand, high-frequency harmonics can introduce additional electromagnetic interference (EMI), increase switching losses, and degrade the performance of sensitive electronic equipment connected to the inverter output.

To address these challenges, it becomes imperative to design a filter capable of effectively attenuating both low-frequency and high-frequency harmonics present in the inverter output current waveform. The filter must be designed to offer selective attenuation across the entire frequency spectrum of interest, ensuring compliance with harmonic distortion standards while minimizing losses and maintaining system efficiency

Overall, the results of the simulation studies and double pulse tests underscore the success of the design improvements implemented in the 3-phase GaN inverter. The enhanced layout not only mitigated parasitic effects but also improved energy efficiency and switching characteristics, making it a viable solution for high-voltage applications.

CHAPTER 3- FILTER DESIGN FOR IMPROVED GAN-BASED MOTOR DRIVE PERFORMANCE

This chapter focuses on enhancing the performance of GaN-based motor drives through effective filter design. It begins with a literature review on various filter topologies aimed at suppressing dv/dt, current ripple, and electromagnetic interference (EMI) in electric vehicle (EV) motor drives. This includes an exploration of passive filters, active filters, and hybrid filter designs. A case study is presented, detailing the design of a filter specifically tailored for the three-phase inverter developed in the previous chapter. Finally, the key findings and implications of the filter design for enhancing GaN-based motor drive performance are summarized.

3.1 Literature review on filter topology for suppressing dv/dt, current ripple, and EMI in EV motor drives

3.1.1 Introduction

Importance of filters in EV motor drives

Electric vehicle (EV) motor drives heavily rely on power electronic converters to efficiently control the flow of energy between the battery and the electric motor [60]. However, the operation of these converters often introduces undesirable effects such as voltage stress (dv/dt), current ripple, and electromagnetic interference (EMI) [61]. Left unaddressed, these effects can degrade the performance, reliability, and safety of the EV system [62].

Challenges with conventional filter designs

Traditional approaches to mitigating dv/dt, current ripple, and EMI in EV motor drives have primarily involved the use of either passive or active filters [63]. While passive filters are effective at attenuating high-frequency noise, they tend to be bulky, heavy, and unable to address a wide frequency range efficiently [64]-[66]. On the other hand, active filters offer flexibility and can handle low-frequency disturbances, but they often come with increased complexity, cost, and losses [67]-[70].

Research gap and need for hybrid filter designs

Despite the advancements in passive and active filter technologies, there remains a

significant research gap in achieving optimal noise suppression in EV motor drives while minimizing size, weight, cost, and losses. To address this gap, there is a pressing need for the development of hybrid filter designs that leverage the strengths of both passive and active elements [71] [72]. By combining passive filtering for high-frequency noise attenuation with active filtering for low-frequency disturbances, hybrid filters offer the potential to achieve superior performance and efficiency in EV applications [73]-[74].

The objective of the literature review

This literature review aims to provide a comprehensive overview of existing research and advancements in hybrid filter designs for EV motor drives, specifically focusing on suppressing dv/dt, current ripple, and EMI levels. By examining the latest developments in passive and active filter technologies, as well as emerging trends in hybrid filter design methodologies and control techniques, this review seeks to identify opportunities for further research and innovation in the field. Ultimately, the goal is to contribute to the advancement of EV technology by enhancing the reliability, efficiency, and performance of motor drive systems through optimized filter design.

3.1.2. Passive filters for EV motor drives

Overview of passive filter designs

Passive filters are essential components in EV motor drives to mitigate high-frequency noise and harmonics generated by power electronic converters. These filters typically consist of inductors, capacitors, and resistors arranged in various configurations such as L-C, LCL, or LC traps [65].

Case Study: LCL filter design for EV traction motor

In the study [75] A.K. Panda et al., a new type of high-performance permanent magnet synchronous motor (PMSM) drive is proposed for applications requiring high-speed operation. The drive utilizes an LCL filter and operates at a fundamental frequency of 916 Hz. It employs synchronous sine-triangle (SST) pulse-width modulation (PWM) with a limited switching frequency of 8 kHz. To mitigate resonance effects, active damping is incorporated into the system. Simulation results demonstrate that the proposed LCL-based PMSM drive, using SST PWM, outperforms an asynchronous sine-triangle (AST) PWM system with f_{sw} of 8 kHz in terms of line current total harmonic distortion (ITHD) and peak-peak torque ripple (τ_e) for

fundamental frequencies ranging from 0 to 500 Hz and from 700 Hz onwards. Additionally, a low-order current harmonic compensation (LHC) technique is introduced to further enhance THD and τ_e across the entire range of fundamental frequencies for the LCL-based PMSM drive.

The simulation outcomes are based on a three-phase, 50 kW PMSM drive with a voltage rating of 244 V operating at a frequency of 916 Hz. The study concludes that the proposed LCL filter based PMSM drive, when combined with SST PWM, active damping, and LHC, exhibits superior performance compared to conventional PMSM drives using AST and SST PWM techniques. This enhanced performance is evident in terms of device junction temperature, I_{THD}, and peak to peak torque ripple cross the entire frequency range of operation.

Case Study: LC double trap filter optimization

In the study [76] by J. Cheng et al., a novel high-order parallel-double-trap LCL filter (PDTLCL) designed specifically for high-speed permanent magnet synchronous motor (HS-PMSM) applications. This filter features two notch branches strategically set at specific frequencies to effectively attenuate current harmonics near the switching frequency and its multiples while maintaining a steep attenuation rate in the high-frequency range. Two parameter design methods for the PDTLCL filter topology are presented, with Design Scheme I offering improved attenuation of switching-frequency current harmonics compared to traditional filters, and Design Scheme II ensuring robustness against parameter variations. The paper investigates parameter selection criteria and optimization methods, considering the HS-PMSM load. Additionally, it analyzes the parameters of PI controllers and the active damping control method for the PDTLCL filter. In conclusion, it presents a performance comparison analysis between the PDTLCL filter and similar topology filters, supported by simulation and experimental results demonstrating the feasibility and validity of the proposed theory. The PDTLCL filter maintains a steep attenuation rate at high frequencies and effectively suppresses dominant switching harmonic currents compared to other LCL topology families as shown in Table 4.1. The parameter design methods avoid the trial-and-error approach of traditional methods, and the capacitor-current-feedback active damping control strategy ensures stable operation across all frequency bands, reducing damping losses. Simulation results confirm the feasibility and effectiveness of the proposed PDTLCL topology.

Table 3. 1 Performance comparison with LCL filtering topology.

Filter	LCL	PDTLCL(Scheme I)
THD	5.41	4.22
Harmonics around f_s	1.72	0.10
Harmonics around $2f_s$	0.65	0.05

Limitations of passive filters

Despite their effectiveness, passive filters have inherent limitations, including their large size, weight, and limited bandwidth [76]. These factors can pose challenges in integrating passive filters into compact EV systems, especially for high-power applications.

Emerging trends: Integrated passive filters

An emerging trend in passive filter design is the integration of passive components directly onto the power module or substrate as shown in Figure 3.1 In the study [77] by J.Zhang et al., the paper introduces a novel passive common-mode voltage (CMV) filter for motor, which utilizes partial motor windings (L) and an additional branch of passive elements (RC) to achieve higher power density. Simulation results demonstrate that the integrated filter effectively reduces CMV, particularly when the cut-off frequency is low (6000 Hz or below). The reduction in CMV is evident in terms of peak-to-peak value, RMS value, and harmonic components, with reductions of up to 10% for peak-to-peak and RMS values, and up to 98% for harmonic components at 10 kHz.

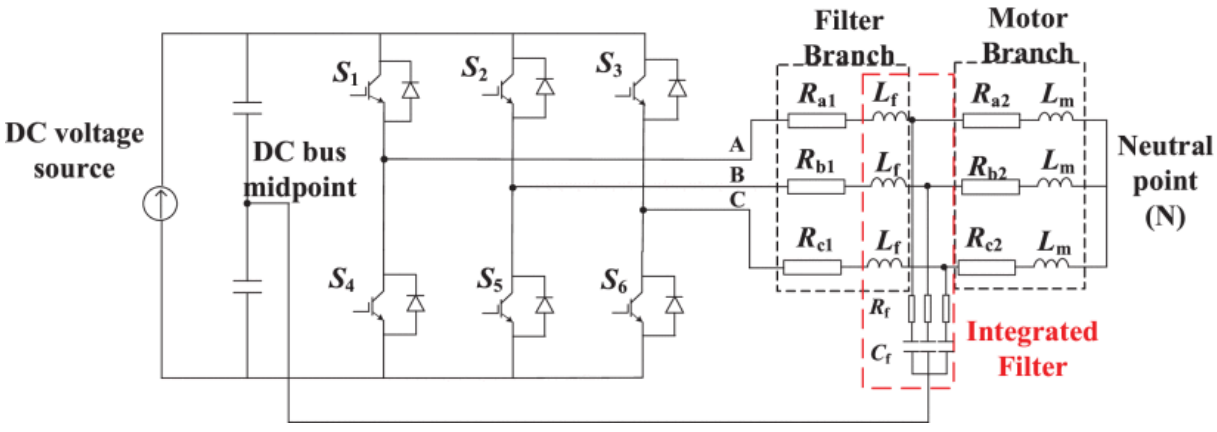


Figure 3. 1 Schematics of the motor drive system with integrated passive filter. [77]

However, when the integrated filter has a high cut-off frequency (8000 Hz and 10000 Hz), it fails to reduce CMV and instead worsens performance. This is attributed to the increased passage of harmonics and the occurrence of resonance, resulting in noise amplification rather

than elimination.

Despite the additional passive components leading to increased losses and torque ripple, careful selection of passive components can minimize these negative effects. Results indicate that integrated filters with lower cut-off frequencies experience less energy loss and torque ripple increment. For frequencies between 2000 Hz and 6000 Hz, torque ripple remains comparable to the original motor with minor fluctuations, whereas noticeable increments are observed for cut-off frequencies exceeding 8000 Hz, particularly at low resistance.

In summary, for comprehensive motor drive system considerations, it is advisable to set the cut-off frequency (determined by the value of passive elements) equal to or less than 6000 Hz. Lower cut-off frequencies offer superior performance in CMV reduction.

Conclusion

Passive filters play a critical role in suppressing high-frequency noise and harmonics in EV motor drives. While traditional passive filter designs have been effective, they face challenges related to size, weight, and bandwidth. However, recent advancements in passive filter technology, including optimized LCL and LC trap filters, as well as innovative multilayered inductor designs and integrated solutions, offer promising opportunities to overcome these challenges and improve the performance and efficiency of EV motor drive systems.

3.1.3 Active filters for EV motor drives

Overview of active filter technologies

Active filters offer an alternative approach to mitigating power quality issues in motor drives compared to passive filters. Unlike passive filters, which rely on passive components such as inductors and capacitors, active filters employ active electronic components such as transistors and operational amplifiers to actively control and adjust the harmonic content of the electrical waveform [78].

Case study: Active filter implementation for EV motor drive

In the study [79] by P. Paipodamonchai et al., it investigates the efficacy of an active EMI filter installed in a drive system comprising a PWM inverter (with a rectifier) and an induction

motor as shown in Figure 3.2. System specifications include a 2.2-kW inverter with 3-phase input/output rated between 360–450 V, 50/60 Hz, and an induction motor rated at 230/400 V, 50 Hz, with 4.65/2.65 A, and 1410 rpm. Operating at a fundamental frequency of 50 Hz, 3 kHz switching frequency, and no-load motor condition, the active EMI filter is evaluated in two conditions: without any filter and with the proposed active filter. Experimental results demonstrate significant attenuation of high-frequency leakage current through the AC supply with the active filter, reducing it from approximately 1.5 A_{peak} to 0.2 A_{peak}. Spectrum analysis reveals the effectiveness of the active filter in attenuating leakage current throughout the frequency range of 1 kHz to 5 MHz, with a reduction of at least 5 dB observed from 1–800 kHz. However, limitations related to amplifier gain and resonance issues are also identified, indicating areas for further improvement.

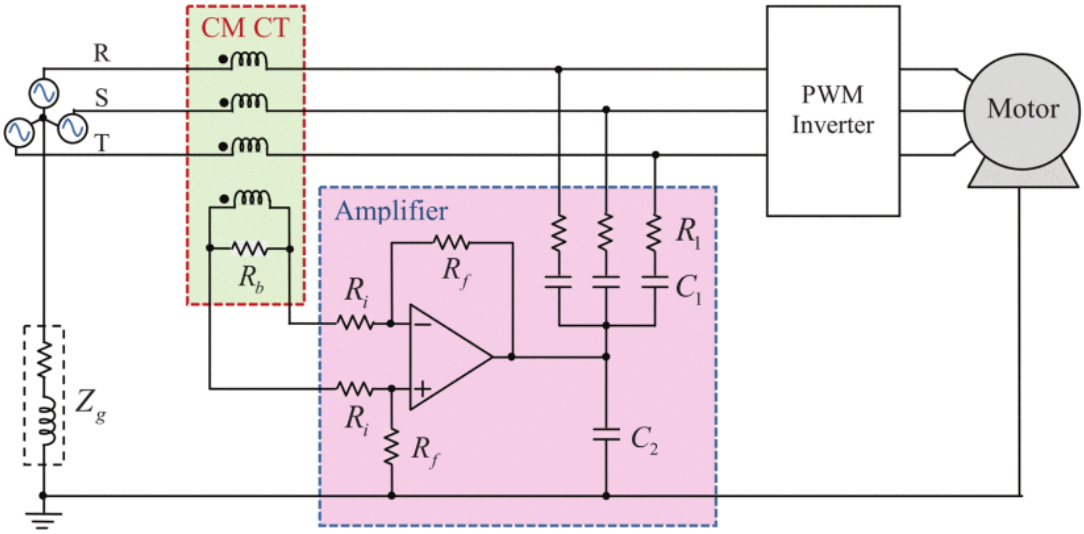


Figure 3. 2 PWM inverter-fed AC motor drive system and leakage current flow. [79]

Hence, the study explores the mitigation of EMI issues in motor drive systems through the implementation of an active EMI filter with a simple structure. The proposed filter as shown in figure 4.4, comprising a common-mode current transformer and an amplifier circuit, effectively reduces high-frequency leakage current, thereby addressing EMI concerns. Experimental findings validate the filter's performance, demonstrating significant attenuation of leakage current across a broad frequency range. While the active filter proves advantageous, limitations related to amplifier gain and resonance underscore the need for further optimization and refinement. Nonetheless, the study presents a promising solution for mitigating EMI problems in industrial motor drive systems.

Advantages of active filters

Active filters offer several advantages over passive filters in EV motor drives. Firstly, they provide greater flexibility and control over the harmonic content of the electrical waveform, allowing for precise tuning and optimization [80]. Secondly, active filters can compensate for dynamic changes in load and system parameters, ensuring consistent performance under varying operating conditions [81]. Additionally, active filters are typically more compact and lightweight compared to passive filters, making them suitable for space-constrained EV applications [82].

Challenges and considerations

Despite their benefits, active filters also pose certain challenges and considerations. One challenge is the complexity and cost associated with the implementation of active filter circuits, which may outweigh the benefits for some applications [83]. Moreover, active filters require careful design and tuning to ensure stability and reliability, as improper operation can lead to system instability and potential damage to sensitive components.

Future directions and research opportunities

Future research in active filter technologies for motor drives may focus on addressing the aforementioned challenges and exploring novel architectures and control strategies. Additionally, advancements in semiconductor technology and power electronics packaging techniques may enable the development of more efficient and cost-effective active filter solutions.

3.1.4 Hybrid filter designs for EV motor drives

Introduction

Hybrid filter designs for Electric Vehicle (EV) motor drives represent a synergistic approach that combines the advantages of both passive and active filtering techniques [84]. By integrating passive elements such as inductors and capacitors with active components like transistors and operational amplifiers, hybrid filters aim to achieve optimal noise suppression and power quality enhancement [85]. This section provides an overview of hybrid filter concepts and recent developments in their design methodologies for EV motor drives. In Figure 3.3, the working of active and passive filters in hybrid filter topology can be seen using

insertion loss in the frequency domain.

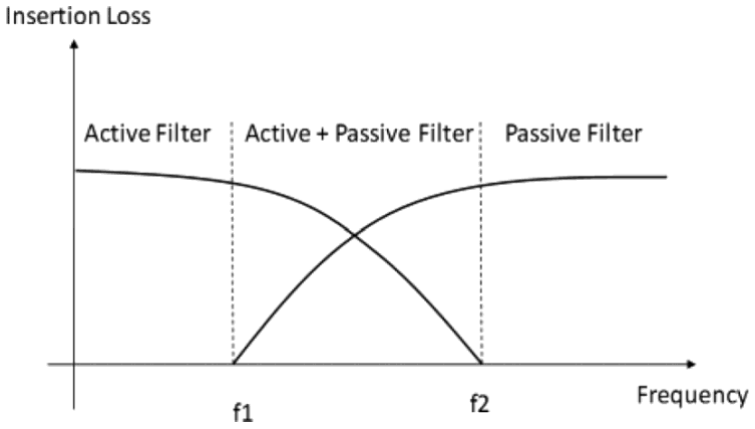


Figure 3. 3 Insertion loss of active and passive filters in hybrid EMI filter [S.Wang et al. 2010]

Review of recent developments

Recent advancements in hybrid filter design methodologies have focused on improving filter performance while addressing the constraints of EV applications [86]. Researchers have explored novel topologies and optimization techniques to achieve enhanced noise suppression and harmonic mitigation. These developments encompass various aspects such as filter configuration, component selection, and control algorithms, aimed at optimizing filter efficiency and reliability in EV motor drive systems.

Benefits of hybrid filters

Hybrid filters offer several advantages over traditional passive or active filters, making them increasingly attractive for EV motor drives. One of the key benefits is size reduction, as hybrid filters can achieve comparable or even superior performance to conventional filters while occupying less physical space [85]. Additionally, hybrid filters contribute to weight savings, a critical consideration in EV applications where minimizing vehicle weight is essential for improving energy efficiency and driving range. Furthermore, hybrid filters are often more cost-effective than purely active solutions, as they leverage the inherent benefits of passive components while incorporating active control for improved performance [84]. Overall, hybrid filters offer a holistic approach to power quality improvement, combining the advantages of passive and active filtering techniques to meet the stringent requirements of EV motor drives.

Case study

In the study [87] by F. Luo et al., paper systematically explores the design and implementation of hybrid EMI filters for motor drive systems, focusing on mitigating common-mode (CM) noise as shown in Figure 3.4. It begins with a thorough investigation of transmission-line busbar filter concepts and their historical context, followed by an analysis of the impedance requirements for effective hybrid filter designs. The study emphasizes the importance of using passive filters before active filters to reduce CM noise amplitude, enabling active filters to function optimally. Through Fourier analysis and insertion loss characterization in the frequency domain, the paper demonstrates that passive filters excel at attenuating high-frequency (HF) noise, while active filters effectively handle low-frequency (LF) noise.

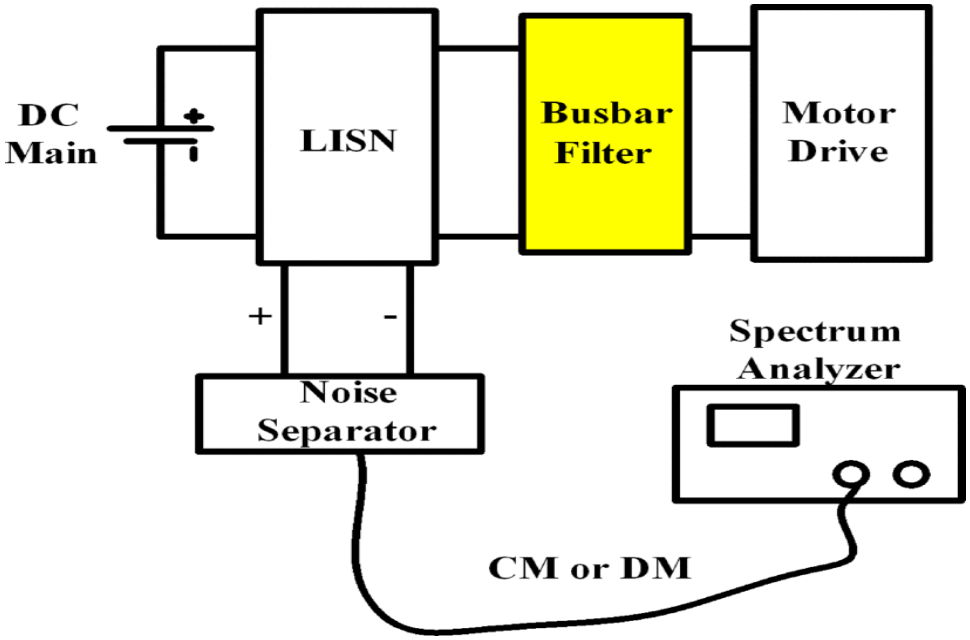


Figure 3. 4 Motor Drive System in EMI test designed in [87]

Various hybrid filter configurations are proposed and analyzed, considering impedance relationships and voltage or current cancellation techniques. Experimental validation of the proposed hybrid filters in a motor drive system confirms their effectiveness in noise attenuation across a wide frequency range. The study also investigates the impact of magnetic materials on filter performance, highlighting the trade-offs between different core materials. Additionally, the paper presents experimental results demonstrating significant CM noise reduction achieved by the hybrid filter prototypes as shown in Figure 3.4, showcasing their potential for practical applications in motor drive systems. Overall, the analysis and design methodologies presented in this paper offer valuable insights and practical solutions for improving EMI mitigation in

motor drive applications, paving the way for more compact and efficient hybrid filter designs in the future.

3.2 Case Study: A filter design for the proposed three-phase inverter

3.2.1 Need for attenuating switching frequency harmonics in GaN-based motor drives

In GaN (Gallium Nitride) based motor drives, similar to other types of motor drives, there is a need to attenuate switching harmonics rather than low order harmonics due to several reasons, some of which are specific to GaN technology:

- Fast switching: GaN devices offer fast switching capabilities, often a rising time in the ns range. As a result, the output voltage slew rate of GaN-based inverters is high, which gives rise to high voltage stress at the motor windings. Applying such a voltage to the motor can cause accelerated insulation degradation with high voltage stress. Filtering the pulse voltage output from GaN inverter is crucial to ensure safe motor operation and a long life span of the motor drive system.

- Efficiency and performance: GaN devices are known for their high efficiency and fast switching speeds, which are advantageous for motor drive applications. However, the fast-switching transitions can lead to the generation of high-frequency harmonics in the motor that can affect motor performance and efficiency if not properly attenuated. Filtering these harmonics helps to maintain system efficiency and performance.

- Minimization of EMI: GaN-based motor drives can generate significant electromagnetic interference (EMI) due to their high-speed switching characteristics. Attenuating switching harmonics helps reduce EMI emissions, ensuring compliance with electromagnetic compatibility (EMC) standards and minimizing interference with other electronic devices in the vicinity.

Overall, while low-order harmonics are still important to be considered in GaN-based

motor drives for power quality reasons, the primary focus is often on attenuating switching harmonics due to their significant impact on motor operation, system efficiency, EMI emissions, and overall system performance and safety.

In the literature review, it is evident that passive filters are commonly preferred for motor drive applications due to their simplicity, cost-effectiveness, and reliability. While active filters offer advantages such as dynamic response and flexibility in compensation, their implementation on the power line of a PWM inverter can be challenging. Active filters typically require complex control algorithms and additional power electronic components, increasing system complexity and cost. Moreover, active filters may introduce potential reliability issues and electromagnetic interference (EMI) concerns. Therefore, for the suppression of high switching frequency harmonics in a GaN-based three-phase inverter, passive filters emerge as a favourable choice. The subsequent section will delve into the design process of a passive filter tailored to address the specific requirements of the case study, aiming to enhance the performance and efficiency of the motor drive system.

3.2.2 Design of passive filter

Step 1: Determine requirements

Frequency Range: Since the inverter is operating at 20 kHz, the cut-off frequency of the LC filter should be chosen to target the higher harmonics generated by the switching frequency.

Attenuation Requirements: Determine the level of attenuation required for each harmonic frequency. This will depend on your specific application and the allowable harmonic distortion.

Step 2: Calculate Inductance (L) Value

Determine Cut-off Frequency: Choose a cut-off frequency based on the harmonics you want to attenuate. For example, you might target the switching harmonics so, the cut-off frequency should be taken slightly less than switching frequency

Select Capacitance (C): Choose a standard capacitor value based on the cut-off frequency and your desired filter characteristics.

Calculate Inductance (L): Use the formula: $L = \frac{1}{(2\pi f_c)^2 C}$

Step 3: Check Resonance Frequency

Check for Resonance: Ensure that the resonant frequency of the LC circuit is well

above the cut-off frequency to avoid resonance issues. Calculate the resonance frequency using: $f_r = \frac{1}{2\pi\sqrt{LC}}$

Step 4: Design the LC Filter Circuit

Choose Component Values: Select standard component values for the LC filter based on the calculated inductance and your chosen capacitor value.

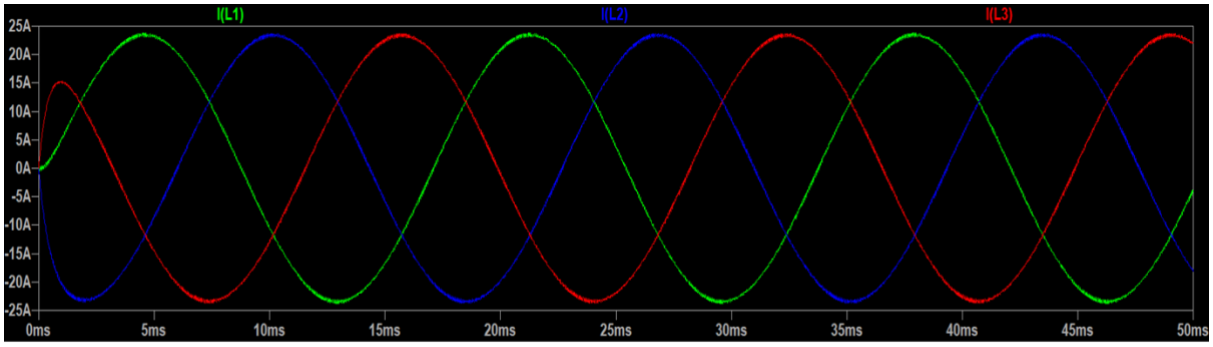
Connection: Connect the capacitor and inductor in series to form the LC filter circuit.

Step 5: Simulation and Testing:

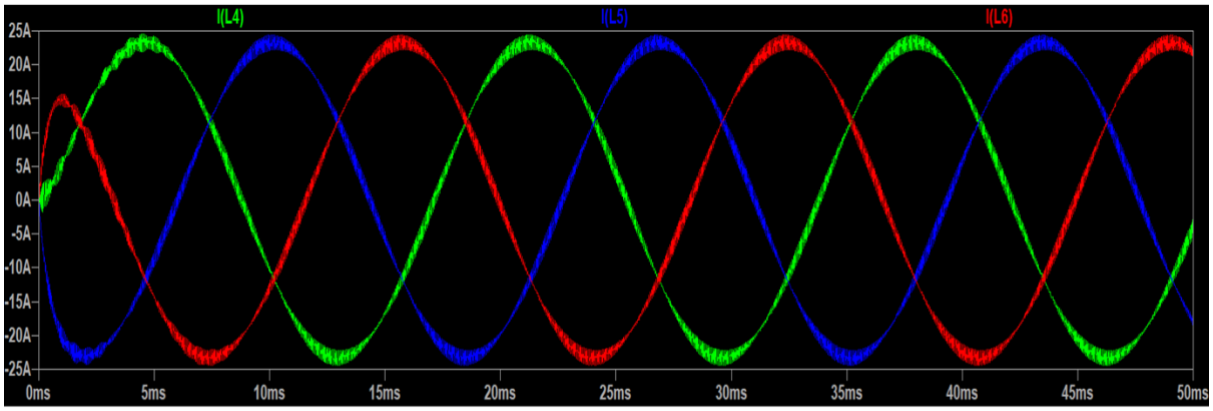
Now, from the above formulas, the values of cut-off frequency, Filter Inductance and Filter Capacitance have been determined i.e. f_c=18 kHz, C=1μF and L=0.078 mH and the inverter is simulated using LTSPICE. Now in Figure 3.5, the output current harmonics are compared with filter and without filter. From the results, it can be seen that the high frequency harmonics i.e. greater than 20kHz have been attenuated using a sine wave passive filter.

Discussions

The output current frequency response analysis following the implementation of a passive filter in the GaN-based three-phase inverter system reveals a remarkable attenuation of high-frequency harmonics, particularly those exceeding 20 kHz. This outcome underscores the effectiveness of the passive filter in achieving a cleaner and smoother output current waveform, thereby enhancing system stability, improving motor performance by reducing torque ripple, mitigating electromagnetic interference (EMI), and ensuring compliance with relevant standards and regulations for electromagnetic compatibility (EMC). The successful suppression of high-frequency harmonics signifies the crucial role of passive filters in optimizing the performance, reliability, and compliance of the inverter system in motor drive applications.



(a)



(b)

Figure 3. 5 Simulation results of output current waveforms (a) with LC filter and (b) without LC filter

3.3 Conclusion

In this chapter, a filter was designed for a three-phase inverter system by leveraging insights gained from a comprehensive literature review on existing active, passive, and hybrid filters in the market. An LC output filter is designed to attenuate the higher switching frequencies.

Through extensive simulation studies, it was observed that the LC filter provided significant attenuation for higher-order harmonics beyond the switching frequency. These simulation results validated the effectiveness of the filter in achieving the desired harmonic suppression objectives.

Although simulation studies provided valuable insights, experimental validation remains a crucial step for real-world implementation. Future endeavours could focus on conducting experimental tests to validate the performance of the filter under practical operating conditions. Additionally, further research into filter sizing and constraints, such as cost, size, and power handling capability, could enhance the applicability and effectiveness of the filter in diverse industrial applications. Overall, this study represents a significant contribution to the field of power electronics and harmonic mitigation techniques.

CHAPTER 4: REVIEW AND COMPARISON OF AN ADVANCED SIX-PHASE NEUTRAL POINT LESS MULTI-LEVEL INVERTER TOPOLOGY

This chapter presents an in-depth examination of an advanced six-phase neutral point less multi-level inverter topology, starting with an introduction and comprehensive literature review. The methodology employed in the comparative study is outlined, followed by an analysis of conventional topologies to provide context. Simulation results are then presented and discussed, offering insights into the performance of the advanced topology. The chapter concludes with a summary of findings, highlighting the strengths and limitations of the proposed topology, and outlines prospects for further research and development in this area.

4.1 Introduction and literature review

Evolution of multiphase electric motors

The evolution of multiphase electric motors has been a focal point of research, marked by significant strides and contributions [88] - [91]. The inherent advantages of multiphase drives, including enhanced fault tolerance and the ability to distribute motor power across multiple phases, have been instrumental in their sustained development. Early works in this area laid the foundation for the exploration of multiphase drives, emphasizing benefits such as increased power levels, improved efficiency, and robust fault tolerance [92], [93]. These advantages extend to practical features like high torque density and reduced torque ripple, making multiphase drives indispensable in various applications, especially those demanding high-performance electric propulsion systems.

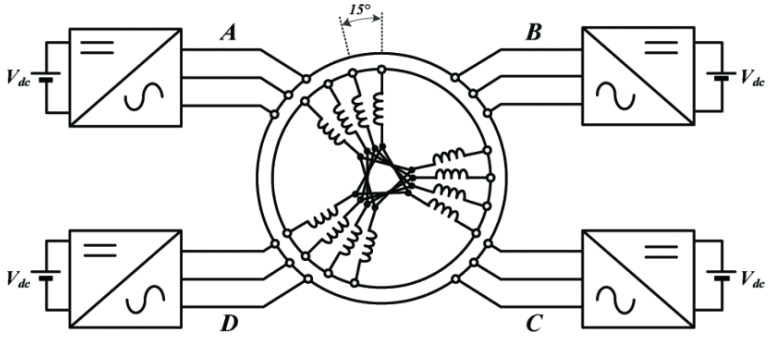


Figure 4. 1 The multi-phase electric drive system as shown in [90]

Role of multi-level inverters:

Multi-Level Inverters (MLIs) have emerged as indispensable components in high-power electrical propulsion systems, notably finding applications in electric aircraft, trains, and heavy-duty electric vehicles. This widespread adoption stems from the unique advantages that MLIs offer over traditional 2-level inverters, particularly in the context of high-power systems operating with DC bus voltages exceeding 400V. The capability to operate at higher DC bus voltages becomes critical in high-power applications, enabling a reduction in current and, consequently, mitigating conduction losses. This inherent characteristic contributes significantly to enhancing the overall power density of these systems.

The key advantages of MLIs are multifaceted. Firstly, they exhibit lower switching losses compared to their 2-level counterparts, a crucial attribute for high-power applications where minimizing losses is pivotal for achieving optimal efficiency and reliability. The distributed nature of the voltage stress across multiple levels in the multi-level structure results in reduced stress on individual components, leading to prolonged device lifespan and heightened overall reliability. Additionally, MLIs inherently generate lower harmonics in the output waveform, a crucial aspect for applications that demand high power quality and necessitate a reduction in electromagnetic interference (EMI). The comparatively lower rate of change of voltage (dv/dt) in the output of MLIs contributes to improved performance in terms of motor insulation and electromagnetic compatibility. Furthermore, MLIs demonstrate superior electromagnetic compatibility by producing minimal voltage distortion at the output, a critical factor for applications requiring minimal interference with other electronic systems.

Despite the numerous advantages, multiphase and multi-level electric motors introduce specific challenges. These challenges include increased complexity in both control algorithms and hardware implementation, potential compatibility issues with existing infrastructure, an elevated component count that can impact system reliability, increased complexity in gate driver design, capacitor voltage imbalance issues, modulation complexity, and concerns related to scalability. Addressing these challenges requires ongoing innovation in multiphase and multi-level topologies.

In this context, the proposed research on a Neutral Point Less (NPL) Multilevel Inverter Topology stands out as a significant contribution to the ongoing innovation in this field. The primary focus of this research is to address the challenges associated with neutral point

connections in six-phase applications. Notably, the elimination of series-connected DC link capacitors in the proposed NPL topology represents a departure from conventional designs, promising not only a simplified design but also mitigation of challenges related to capacitor voltage imbalance and the inherent complexity in traditional multi-level topologies.

This research, situated within the broader landscape of advancements in power electronics, showcases a dedicated effort toward overcoming the challenges posed by conventional multiphase and multi-level inverter designs. The implications of such innovations extend beyond theoretical contributions, potentially impacting the practical implementation of high-power electrical propulsion systems. As the research unfolds, it holds the promise of not only enhancing the understanding of these advanced inverter topologies but also contributing tangible solutions to make them more viable for real-world applications.

Advancements in multiphase drives and MLIs

Recent works in the field of multiphase drives and MLIs have demonstrated a commitment to overcoming these challenges. E. Levi's comprehensive review [88] outlines advances in converter control and the innovative exploitation of additional degrees of freedom for multiphase machines. The technology status review by Levi et al. [93] and Lipinskis et al. [99] further enriches our understanding of multiphase induction motor drives. Specific applications, such as electric ship propulsion [88] and diagnostics for asymmetrical twelve-phase induction motor drives [89], showcase the diversity of research efforts aimed at improving the efficiency and reliability of multiphase systems. Additionally, Salem and Narimani's review [91] provides valuable insights into multiphase drives for automotive traction applications, highlighting the role of multiphase systems in advancing transportation electrification.

DC-link voltage balancing strategies

Balancing strategies for DC-link voltage in three-level neutral point-clamped (NPC) inverters have been the subject of recent investigation [94]. Kumar and Jiji's work emphasizes the importance of comparing different strategies to achieve optimal voltage balancing. Moreover, Rasoanarivo, Martin, and Pierfederici [96] focus on improving the electromagnetic interference (EMI) behaviour of NPC multilevel inverters without relying on the balancing of voltage boundaries in DC bank capacitors.

Recent Trends: Neutral Point-Less (NPL) Multilevel Inverter Topology

Recent trends have seen a shift towards addressing challenges posed by neutral point connections. Benson et al.'s work on a Neutral-Point-Less (NPL) Multilevel Inverter Topology [98] introduces a promising solution. Their H-type inverter configuration with a single DC-link capacitor demonstrates a departure from traditional approaches, eliminating the need for series-connected DC-link capacitors to achieve the neutral point connection. The application of this innovative topology in three-phase inverters has already yielded favourable results, prompting further exploration in the context of six-phase applications.

Problem statement

While multiphase electric motors and multi-level inverters (MLIs) have witnessed substantial advancements, a critical gap exists in addressing challenges associated with neutral point connections in six-phase applications. Conventional multi-phase, multi-level inverter topologies, such as neutral point-clamped, flying capacitor, and cascaded H-bridge MLIs, encounter significant hurdles related to neutral point connections and capacitor voltage imbalances [94][97]. The current solutions, relying on the connection of a neutral point between stacked DC-link capacitors, lead to unbalanced capacitor voltages due to high neutral currents at three times the fundamental frequency. This phenomenon results in undesirable fluctuations in capacitor voltage, causing damage to switching devices, distortion in output voltage and current, and imposing significant voltage stress on capacitors [96].

Motivation for the proposal

The motivation for this research stems from the increasing demand for high-power applications, such as heavy-duty electric vehicles, electric aircraft, and electric marine ships. As these applications necessitate high DC bus voltage levels exceeding 400V, the challenges posed by conventional multi-phase inverters become more pronounced. The limitations of existing solutions, including neutral point connections and capacitor voltage imbalances, underscore the need for innovative approaches.

The proposed research seeks to address these challenges through the investigation of a Neutral Point Less (NPL) Multilevel Inverter Topology specifically designed for six-phase applications. This topology, derived from the modification of a traditional 3-level active neutral point converter (ANPC), eliminates the need for series-connected DC link capacitors required for obtaining the neutral point connection in the traditional 3-level topology. The root causes of DC link capacitor ripple and imbalanced voltages are targeted by introducing an H-type switch configuration to eliminate the neutral point connection effectively.

The significance of this proposed research lies in its potential to revolutionize the design and performance of six-phase inverters, particularly in high-power applications. By addressing the challenges associated with neutral point connections, the NPL Multilevel Inverter Topology is anticipated to offer a more efficient and reliable solution. The elimination of series-connected DC link capacitors not only simplifies the design but also contributes to a reduction in size, cost, and overall system complexity. Moreover, the extension of the comparative analysis from three-phase to six-phase inverters provides valuable insights into the scalability and adaptability of the proposed topology.

Expected contributions

The research anticipates several contributions to the field:

Innovative Topology Design: The introduction of the NPL Multilevel Inverter Topology for six-phase applications represents an innovative solution to the challenges associated with neutral point connections.

Improved System Reliability: By reducing DC link capacitor ripple and imbalanced voltages, the proposed topology is expected to enhance the reliability and lifespan of six-phase inverters.

Increased Power Density: The elimination of series-connected DC link capacitors contributes to a reduction in size, ultimately increasing the overall power density of the system.

Scalability Insights: Extending the comparative analysis to six-phase inverters provides insights into the scalability and adaptability of the proposed topology across different phases.

4.2 Methodology

The proposed H-type inverter as shown in Figure 4.2, a key element in this investigation, represents a paradigm shift in the design and operation of multi-level inverters (MLIs). This section delves into the fundamental principles of the Neutral Point Less (NPL) topology, elucidating the intricate details of the H-type inverter's architecture and its operating principle.

Operating principle of the H-Type Inverter

Implementation and configuration

At the core of the H-type inverter lie six active switching devices meticulously crafted

with two half-bridge (HB) modules and one bidirectional (BD) MOSFET module. Notably, a common-drain BD switch configuration has been judiciously chosen to streamline the design. This configuration strategically positions the source of the BD module at the center point of each HB module, fostering a dynamic flow path for the two equal and opposite phase currents. This ingenious arrangement serves a dual purpose - reducing the complexity of the topology and eliminating the need for a middle-point connection to the center of the DC-link capacitors.

Gate driver circuits and power supplies

A hallmark of the H-type inverter's simplicity lies in its reduced demand for isolated power supplies. With two gate driver circuits per leg, summing up to six gate driver signals in total, and three isolated power supplies for the complete configuration, this topology minimizes complexity compared to other multi-phase MLI configurations. This strategic design choice not only enhances the robustness of the system but also contributes to ease of implementation.

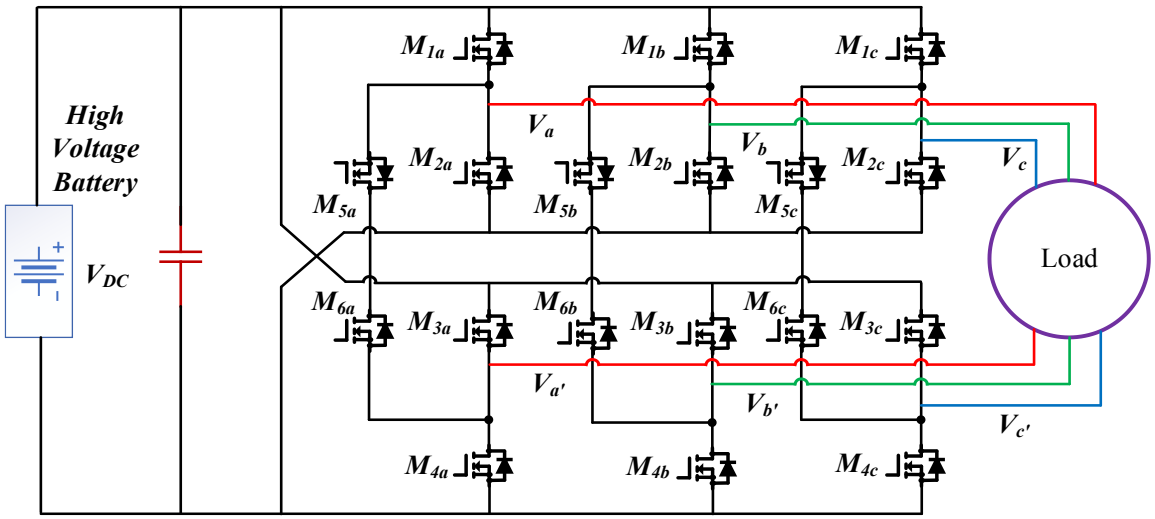


Figure 4. 2 The circuit diagram of the NPL-MLI for investigation.

Minimizing switch count for multilevel operation

The elegance of the H-type inverter extends to its minimalistic approach to achieving multilevel operation. Remarkably, a single H-type inverter module, comprising six active switches, generates two equal and opposite output voltage channels. This unique characteristic translates to unparalleled efficiency, as the topology demands only three active switches for each three-level output voltage. Such frugality in switch count represents the absolute minimum number of switches required for multilevel operation within the current landscape of inverter designs.

Three-Level output voltage generation

The crux of the H-type inverter's functionality lies in its ability to generate three-level output voltages with a single DC-link capacitor. Delving into the switching states and commutation of the H-type inverter reveals a meticulous orchestration. For both positive and negative output states ('A' and 'B'), the voltage levels at each output equate to half the DC-link voltage ($V_{DC}/2$). Notably, Vout1 signifies the positive output voltages (V_a, V_b, or V_c) through the upper half of the inverter leg, while V_{out2} denotes the inverting voltages ($V_{a'}$, $V_{b'}$, or $V_{c'}$) of the same leg. The nuanced control achieved through selective activation of switches M_1, M_2, M_3, M_4, M_5, and M_6 orchestrates the intricate dance of voltage states, demonstrating the versatility and precision of the H-type inverter.

Three-level pulse width modulation (PWM) generation using sine wave modulation

Introduction

The generation of three-level PWM signals is a critical aspect of the H-type inverter's operation, determining its ability to control the output voltages effectively. The sine wave PWM modulation technique is employed to achieve this, leveraging mathematical principles to create precise and controlled electrical transitions. In this section, we delve into the detailed mechanics of the sine wave PWM generation method.

Sine wave PWM modulation technique

The sine wave PWM modulation technique relies on a sinusoidal reference voltage to produce three-level PWM signals. The process involves comparing the sinusoidal reference voltage with a high-frequency triangular carrier wave as shown in Figure 4.3, creating a PWM pattern that dictates the inverter's output. A crucial aspect of this technique is the introduction of a phase shift of 120° among the modulating signals between each inverter leg.

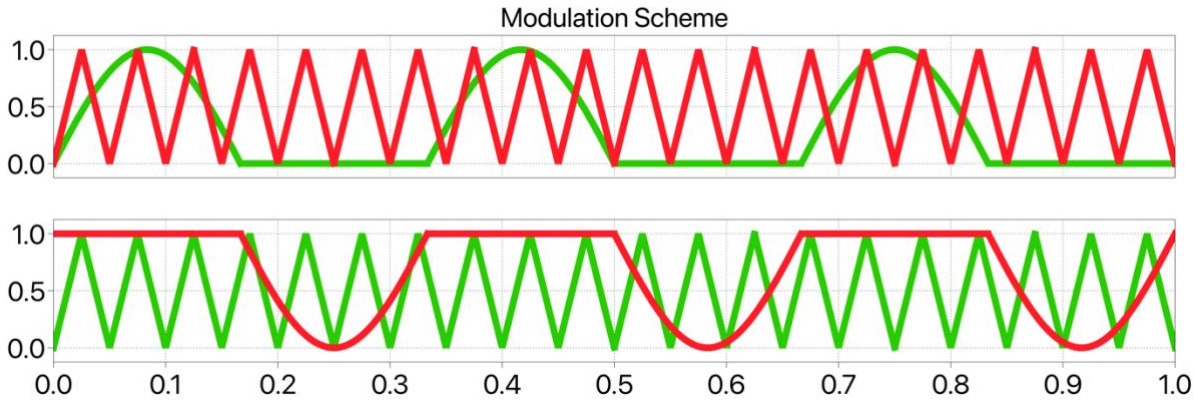


Figure 4. 3 Modulation scheme for the sine wave PWM generation

Mathematical representation

The mathematical representation of the sine wave PWM modulation technique is rooted in sinusoidal functions. Let V_{ref} represent the overall voltage reference, V_{aref} denote the reference voltage for the first half cycle and $V_{a'ref}$ for the other half cycle. The mathematical expressions are as follows:

$$V_{ref}=A\sin(2\pi ft+\alpha) \quad (4\text{-}1)$$

$$V_{aref}=A_1\sin(2\pi f't+\alpha_1) \quad (4\text{-}2)$$

$$V_{a'ref}=A_2\sin(2\pi f't+\alpha_2) \quad (4\text{-}3)$$

- A, A_1, A_2 are the amplitudes.
- f, f' are the frequencies.
- α, α_1, α_2 are the phase angles of the reference voltages.

Operation of the H-Type Inverter with Sine Wave PWM

The H-type inverter operates with a single-carrier sine PWM (SPWM) technique. This involves the generation of a half-sine wave and its comparison with a high-frequency triangular carrier waveform. Simultaneously, an inverted half-sine wave is created for the alternating cycle from the first carrier wave. The modulation index (m) is a crucial parameter defined as the ratio of the reference voltage to half of the DC-link voltage:

$$m = \frac{v^{ref}}{v_{dc/2}} \tag{4-4}$$

This modulation approach, facilitated by synchronized PWM signals for specific switches, allows the H-type inverter to achieve a three-level PWM output efficiently.

Implications on Output Characteristics

The frequency of the output voltage is dictated by the frequency of the carrier signals, offering control over the temporal characteristics of the inverter's output. Additionally, the modulation signal's frequency influences the amplitude of the output voltage, providing a means to regulate the magnitude of the electrical transitions.

In summary, the detailed mathematical foundations of the sine wave PWM modulation technique in the H-type inverter underscore its versatility and precision in generating three-level PWM signals. This method, coupled with synchronized PWM signals and complementary configurations, forms the basis for controlling the inverter's output, ensuring efficient energy conversion and precise operational control in the realm of six-phase multi-level inverter applications.

Zero states and commutation logic

Furthermore, the zero states, a critical aspect of the H-type inverter's operation, are achieved under specific conditions. The careful activation of switches M5 or M6 underpins these zero states, presenting a comprehensive commutation logic elucidated in Table 4.1. This section's detailed exploration lays the foundation for a profound understanding of the H-type inverter's operational dynamics, setting the stage for a deeper analysis in subsequent sections.

Table 4. 1 Commutation logic of NPL MLI

State	V_{Out1}	$-V_{Out2}$	M_1	M_2	M_3	M_4	M_5	M_6
A	$V_{DC}/2$	$-V_{DC}/2$	✓	**x**	**x**	✓	**x**	**x**
Zero($+i_{ph}$)	0	0	**x**	**x**	**x**	**x**	✓	**x**
Zero($-i_{ph}$)	0	0	**x**	**x**	**x**	**x**	**x**	✓
B	$-V_{DC}/2$	$V_{DC}/2$	**x**	✓	✓	**x**	**x**	**x**

The switching states and commutation logic play a crucial role in determining the output voltages of the H-type inverter. This intricate process orchestrates a series of electrical transitions within the inverter. The details provided in the table serve as a fundamental guide, outlining how the inverter operates. This meticulous orchestration is the foundation of the inverter's functionality, ensuring accurate control and efficient energy conversion.

State A:

Positive Output: $+V_{DC}/2$ Negative Output: $-V_{DC}/2$

Switch Configuration: M_1 and M_4 in ON state

Commutation Logic: In this state, Vout1 represents the positive output voltages (V_a, V_b, or V_c) through the upper half of the inverter leg, while Vout2 denotes the inverting voltages (V_a', V_b', or V_c') of the same leg. Positive $V_{DC}/2$ is achieved when switches M_1 and M_4 are in the ON state.

Zero States ($+i_{ph}$ and $-i_{ph}$): Output: 0

Switch Configuration: M_5 in ON state for the positive zero state, M6 in ON state for the negative zero state

Commutation Logic: Both zero states are characterized by the absence of voltage output. Positive and negative zero states are achieved when either M_5 or M_6 is turned ON, creating a balanced current path.

State B:

Positive Output: $-V_{DC}/2$ Negative Output: $+V_{DC}/2$

Switch Configuration: M_2 and M_3 in ON state

Commutation Logic: State B represents a transition to the negative output, with Vout1 being $-V_{DC}/2$ and V_{out2} being $+V_{DC}/2$. This state is achieved when switches M_2 and M_3 are in the ON state.

4.3 Comparative study of the conventional topologies:

Dual T-type six-phase inverter topology:

The six-phase dual T-type inverter, an advanced adaptation of the T-type Inverter for six-

phase applications, employs a sophisticated design involving the replication of the fundamental T-type leg to create one leg for each phase, resulting in a total of six legs. The operational intricacies of the T-type leg are preserved, involving semiconductor devices like IGBTs or MOSFETs. This innovative configuration facilitates the generation of a three-level voltage waveform in each T-type leg, ensuring a balance between positive, negative, and zero voltage states.

The operation of the six-phase T-type inverter hinges on the coordinated switching states of its multiple legs as shown in Figure 4.4. Each T-type leg contributes to the overall six-phase output, with precise control over the switching states determining the quality and characteristics of the generated voltages. Each T-Type leg operates by toggling between positive, negative, and zero voltage states. This toggling is orchestrated through the controlled switching of semiconductor devices, typically insulated gate bipolar transistors (IGBTs) or metal-oxide-semiconductor field-effect transistors (MOSFETs).

Positive Voltage State: In this state, the upper switch (M_{1a}) is turned on, connecting the positive DC bus voltage to the load. The lower switch (M_{2a}) remains off.

Negative Voltage State: Here, the lower switch (M_{2a}) is turned on, connecting the negative DC bus voltage to the load. The upper switch (M_{1a}) is turned off.

Zero Voltage State: Both switches (M_{1a} and M_{2a}) are turned off, resulting in a state where the voltage across the load is zero.

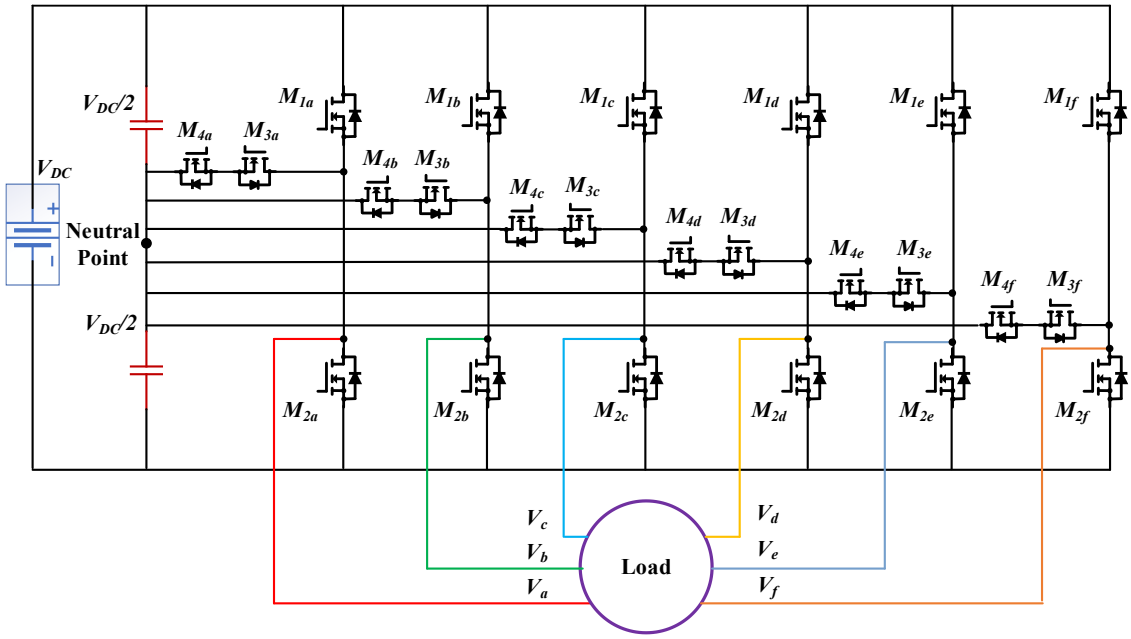


Figure 4. 4 Dual T-type six phase 3-level topology

2-Level six-phase inverter topology:

The 2-level Six-Phase Inverter is a simpler configuration compared to multi-level inverters. It operates with two voltage levels, typically positive and negative, and is designed for six-phase applications. This topology employs a total of 12 switching devices (MOSFETs or IGBTs) as shown in Figure 4.5. The switches are arranged in a way that allows for toggling between positive and negative voltage states. It utilizes a single DC link capacitor (C). The capacitor stores energy and helps in achieving the desired voltage levels. The operating principle involves turning on and off specific switches to create positive and negative voltage states. So, only two states are utilized for each phase: positive and negative. It achieves voltage switching by manipulating the states of the switches. Switching logic ensures that the transition between positive and negative voltage levels is smooth. Commutation involves managing the state changes to avoid sudden voltage spikes or disruptions. The advantages of 2-Level topology include the less complexity in design as compared to multi-level inverters with fewer switches and a single DC link capacitor. Also, the reduced number of components contributes to lower costs. Now, on the other hand, the challenges include the limitation of two voltage levels (positive and negative), which may affect the quality of the output waveform. In addition to this, the simplicity of the topology may lead to a higher total harmonic distortion (THD) in the output.

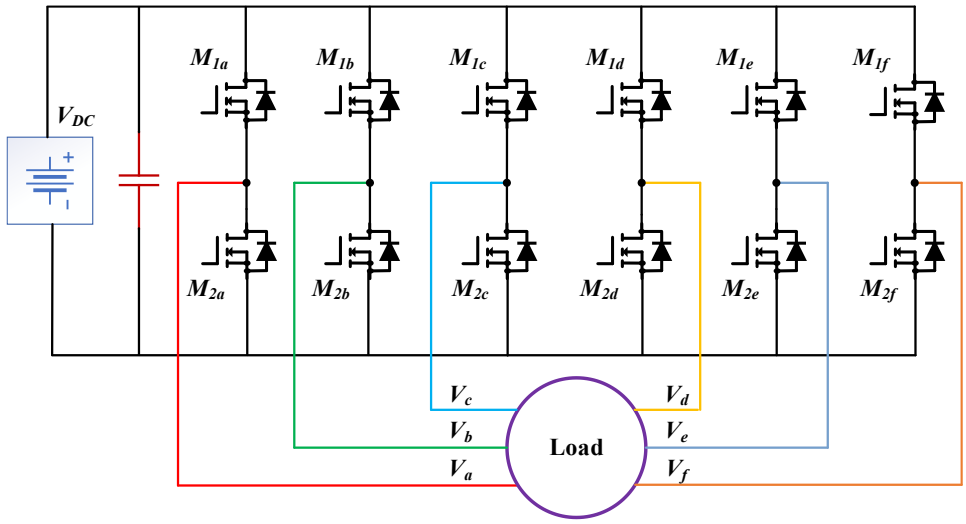


Figure 4. 5 2-Level six-phase inverter topology

In this research, a detailed comparative analysis is conducted among three distinct six-phase inverter topologies: Neutral Point Less Multi-Level Inverter (NPL-MLI), Dual T-Type, and 2-Level Six Phase. The investigation focuses on key parameters critical to the performance and efficiency of these topologies. Firstly, the number of switches employed in each configuration is scrutinized, revealing that the NPL-MLI utilizes 18 switches, the Dual T-Type requires 24 switches, and the 2-Level Six Phase employs 12 switches. The impact of DC link capacitance is assessed, with the NPL-MLI utilizing a single capacitor 'C,' the Dual T-Type requiring twice the capacitance labelled as '2C', and the 2-Level Six Phase employing a single capacitor 'C.' Further, the complexity of Pulse Width Modulation (PWM) is addressed, highlighting that the NPL-MLI involves 6 gate driver signals, the Dual T-Type demands 12 gate driver signals, and the 2-Level Six Phase requires 6 gate driver signals for PWM. Additionally, the DC-Link Rating is explored, indicating that the NPL-MLI operates with all switches at the same DC link voltage (VDC), the Dual T-Type has middle switches at VDC/2 and others at VDC, while the 2-Level Six Phase operates with all switches at the same VDC. Lastly, the phase shift parameter is considered, with the NPL-MLI operating at a 60-degree phase shift, the Dual T-Type at either 30 or 60 degrees, and the 2-Level Six Phase at either 30 or 60 degrees. This comprehensive comparative analysis forms a foundation for evaluating the strengths and weaknesses of each topology, aiding in the determination of the most suitable configuration for specific applications. Please refer to the table below for all the comparison parameters.

Table 4. 2 Comparison parameters of three topologies

Topology	NPL-MLI	Dual T-Type	2-Level Six Phase
No. of Switches Used	18	24	12
DC Link Capacitance	C	2C	C
PWM Complexity	6 Gate Driver Signals	12 Gate Driver Signals	6 Gate Driver Signals
DC-Link Rating	V_{DC} for all the switches	$V_{DC}/2$ for the middle switches and V_{DC} for all other switches	V_{DC} for all the switches
Phase Shift	60 °	30 ° or 60 °	30 ° or 60 °

4.4 Simulation and results

In the presented study, the performance of the Neutral Pointless Multi-Level Inverter (NPL-MLI) is rigorously evaluated and compared against traditional two-level and dual T-type three-level inverters through detailed simulations conducted in PLECS. The simulations are conducted with an 800V DC input, resistive load (R-load), a modulation index set to 1, and a switching frequency of 50 kHz. To ensure a fair comparison, an LC output filter is incorporated with 1 mH inductance and 1μF capacitance in all three topologies. The schematics drawn in PLECS software for the simulation of NPL-MLI topology are shown in Figure 4.6.

Table 4. 3 Simulation parameters

Parameter	Value
V_{BUS}(V)	800V
F_{sw}	50 KHz
L (inductance)	1 mH
C (capacitance)	1 uF
m (Modulation Index)	1
Phase Shift	120° (NPL-MLI)

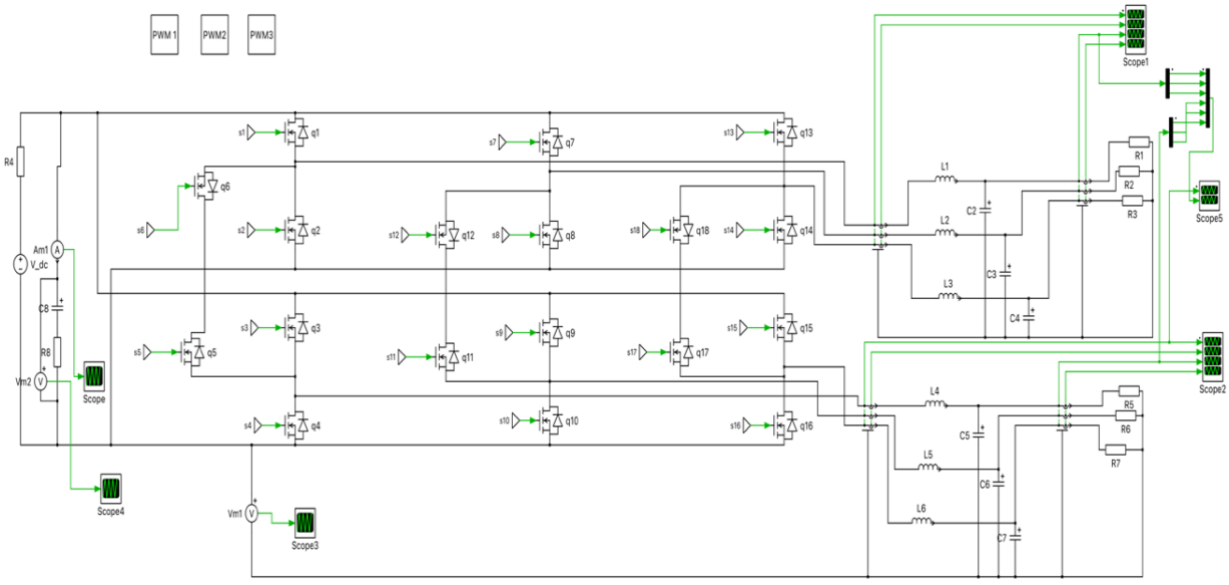


Figure 4. 6 Schematics of NPL-MLI simulation.

Voltage waveforms:

The line-neutral three-level voltage waveforms depicted in Figure 4.7 (a), (b) and (c) offer a visual representation of the output voltages produced by the proposed Neutral Pointless

Multi-Level Inverter (NPL-MLI) and the Dual T-Type topology. These waveforms are crucial for understanding the quality and characteristics of the output voltage, which directly impacts the performance of the inverter in driving motor loads or other applications.

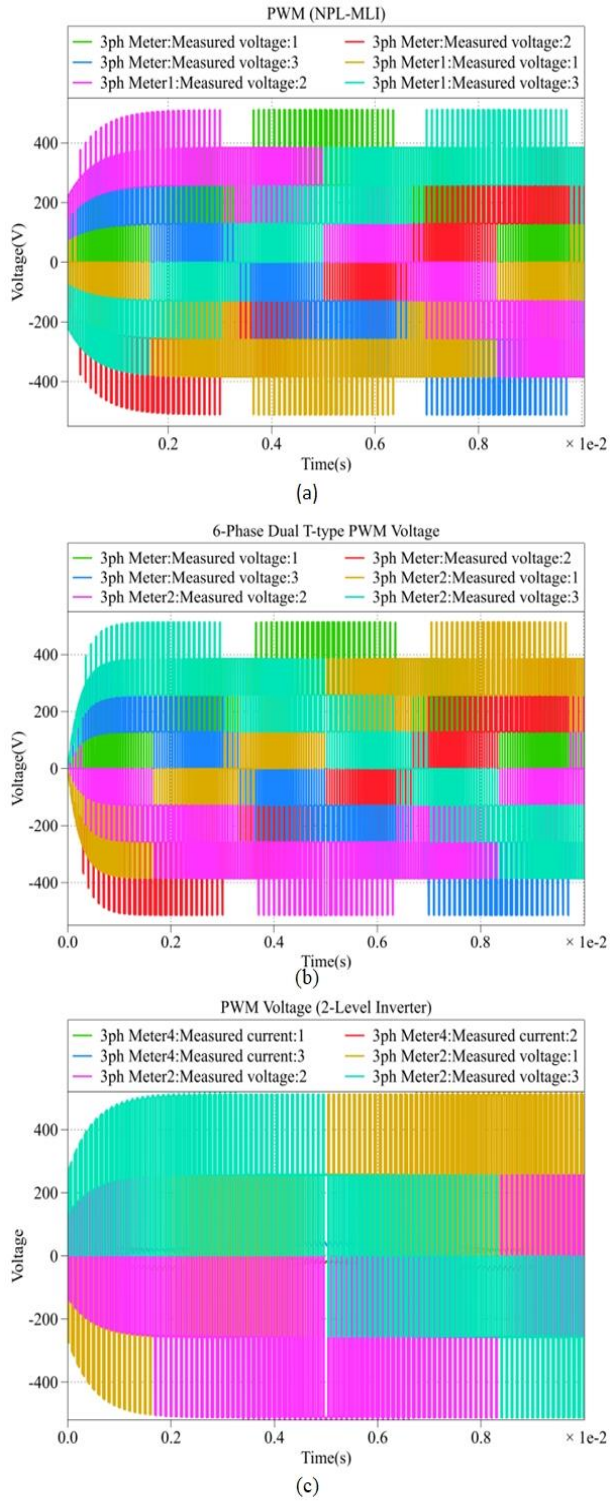


Figure 4. 7 Output PWM voltage waveforms

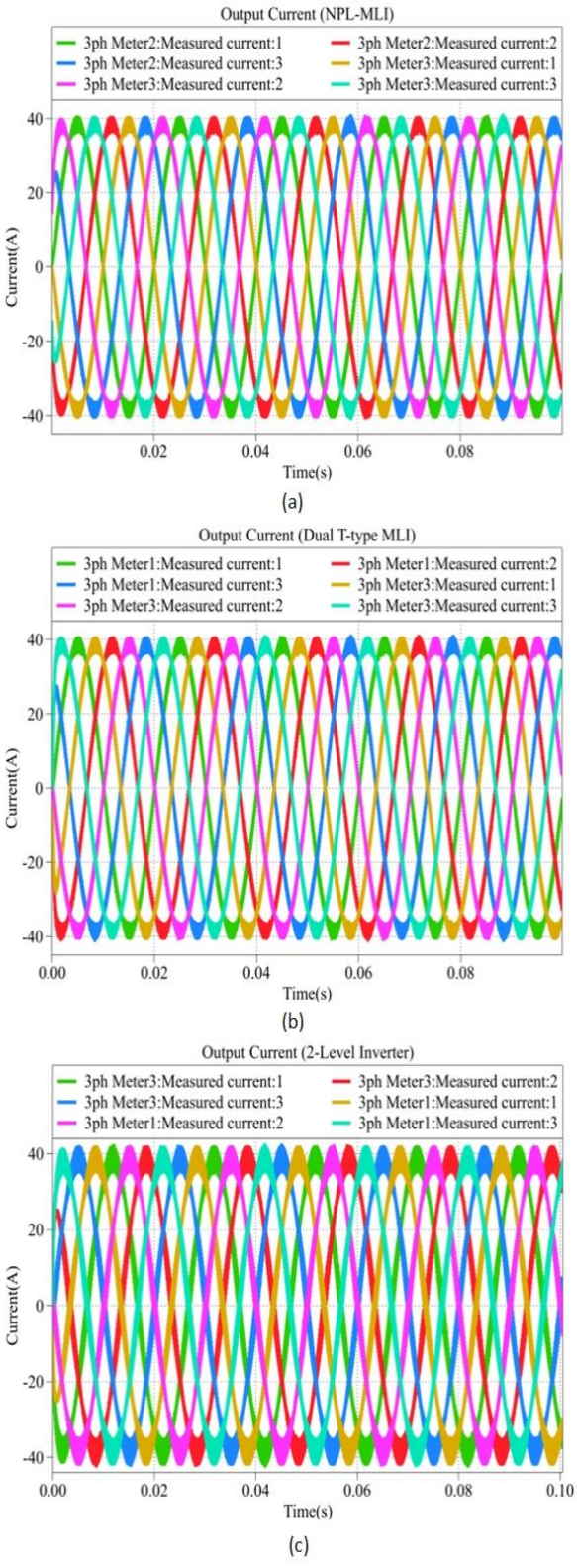


Figure 4. 8 Output current waveforms

Current waveforms:

Figure 4.8 (a), (b), and (c) showcase the output current waveforms of the proposed NPL-MLI and conventional topologies. The current waveforms are instrumental in analyzing the impact on motor performance, efficiency, and potential issues such as torque ripple, noise, and losses. Understanding the shape and magnitude of these waveforms is essential for evaluating the inverter's operational dynamics.

Total Harmonic Distortion (THD):

THD is a measure of the distortion present in the output current waveform. The equation below calculates THD by considering the squared magnitudes of harmonic components. The lower the THD, the closer the current waveform is to a pure sinusoidal waveform. In the context of this study, the THD values (2.8% for NPL-MLI, 3% for Dual T-Type, and 6.3% for the traditional two-level six-phase topology) quantify the quality of the output current and its deviation from an ideal sinusoid as shown in Figure 4.9. Reduced THD is desirable as it indicates less distortion and improved power quality.

$$\mathrm{THD} = \sqrt{\frac{\sum_{i=2}^{n} X_{i2}}{X_1^2}}$$

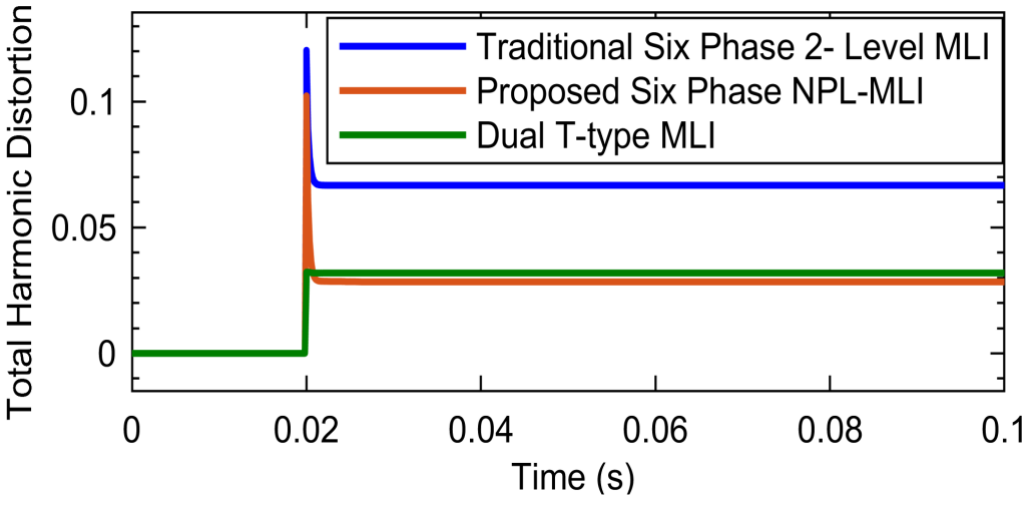


Figure 4. 9 Comparison of THD in the output current of six-phase inverters.

DC link capacitance size:

The DC link capacitance is a critical component in the inverter's energy storage and voltage stabilization. The proposed NPL-MLI demonstrates a 50% reduction in DC link capacitance compared to the Dual T-Type topology. This reduction has significant implications for the size and cost of the overall system. A smaller DC link capacitance can lead to cost savings and a more compact system, contributing to higher power density.

Current ripple performance:

Figure 4.10 illustrates the capacitor current ripple performance among the three topologies. Current ripple refers to the variation in the DC link current over time. A lower current ripple is advantageous as it reduces stress on components, minimizes losses, and enhances system reliability. The proposed NPL-MLI, with a 40% reduction in current ripple compared to the traditional six-phase two-level inverter and a 67% improvement compared to the Dual T-type inverter, demonstrates superior performance in this regard.

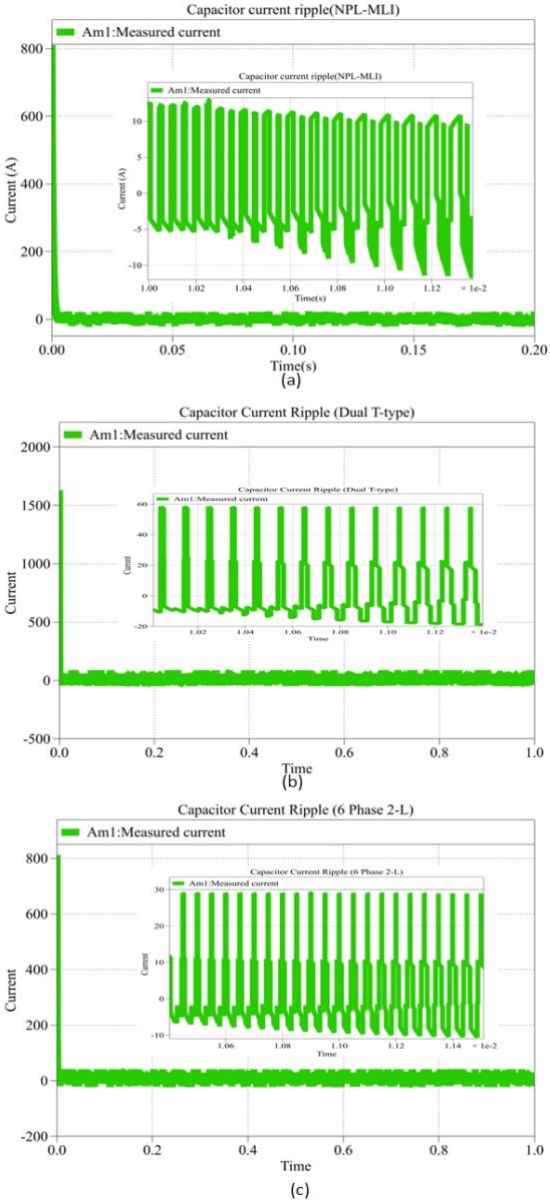


Figure 4. 10 Capacitor current ripple

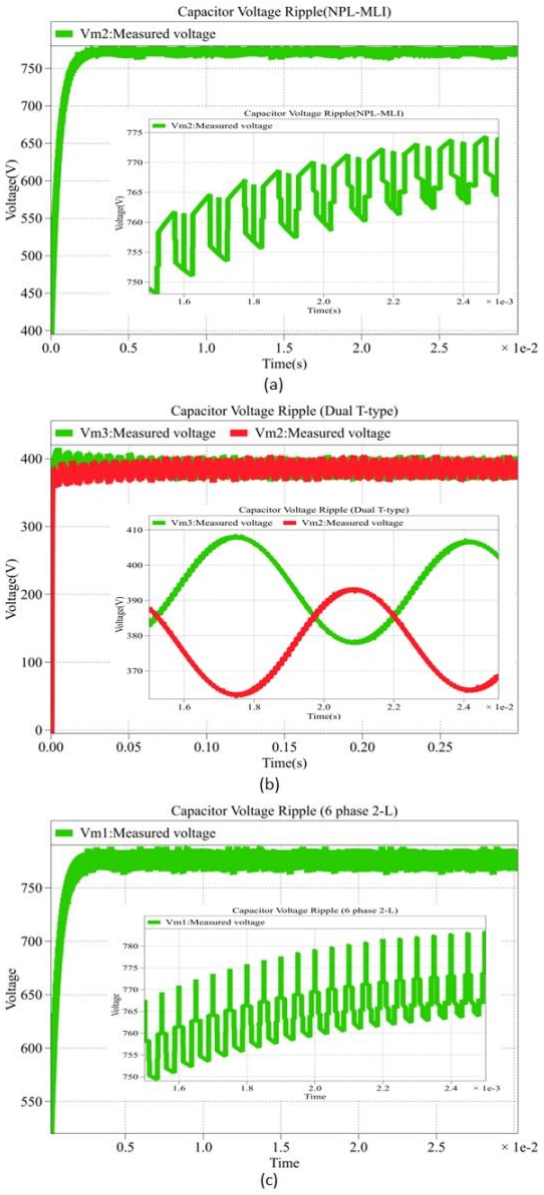


Figure 4. 11 Capacitor voltage ripple

Capacitor voltage ripple:

Figure 4.11 analyzes the capacitor voltage ripple, representing the variation in the DC link voltage over time. Voltage ripple affects the overall performance and reliability of the inverter. The proposed NPL-MLI exhibits a 50% reduction in voltage ripple compared to the Dual T-Type topology and a 33% reduction compared to the traditional two-level six-phase inverter. Controlling voltage ripple is crucial for ensuring stable operation and minimizing stress on the inverter components.

Effect of capacitor size on voltage ripple:

The study emphasizes the trade-off associated with increasing capacitor size. While larger capacitors can reduce DC link voltage ripple, they also contribute to a larger overall system. Balancing the benefits of reduced ripple with the drawbacks of increased system size is a critical consideration in designing an efficient and compact inverter system. The findings highlight the importance of optimizing capacitor size to achieve the desired balance between voltage ripple, system reliability, and power density.

In summary, each parameter provides valuable insights into different aspects of inverter performance, including waveform quality, distortion, component size, and ripple characteristics. Analyzing these parameters collectively allows for a comprehensive evaluation of the proposed NPL-MLI against traditional topologies, emphasizing its potential advantages in multi-phase inverter applications.

Thermal loss analysis

Thermal losses in power electronic systems, particularly in inverters, play a critical role in determining the overall efficiency, reliability, and lifespan of the system. These losses primarily result from two sources: switching losses and conduction losses. Switching losses occur during the transition of a switch from an ON state to an OFF state and vice versa. The frequency at which these switches toggle directly influences the magnitude of switching losses. On the other hand, conduction losses arise from the resistance of the switches and the associated current flowing through them during the ON state. Thermal losses, resulting from switching and conduction losses, significantly impact the overall efficiency, reliability, and lifespan of an inverter.

In the context of the simulated thermal losses, the SiC switches C3M0065100K, as per the datasheet in [100] have been employed. The comparison is performed under varying switching frequencies and modulation indices. It's important to note that the chosen SiC switches are known for their high-temperature tolerance and fast switching capabilities, making them suitable for high-frequency applications.

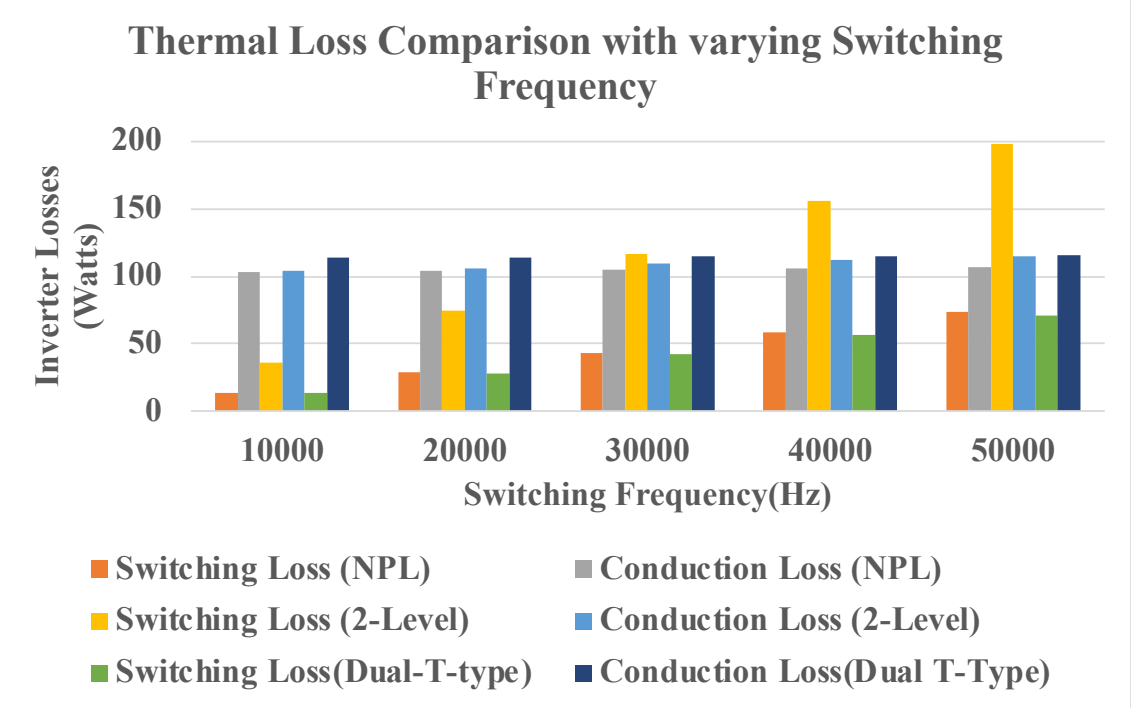


Figure 4. 12 Comparison of inverter losses for the NPL-MLI, dual T-type, and the 2-Level inverter topologies under different switching frequencies.

Figure 4.12 and Figure 4.13 in the thesis illustrate the thermal losses comparison under different conditions. Figure 4.12 delves into the impact of switching frequency on inverter losses, demonstrating that as the switching frequency increases, the total losses also rise. This is a common phenomenon, as more frequent switching results in heightened switching losses. Notably, the Neutral Pointless Multi-Level Inverter (NPL-MLI) exhibits the lowest total losses at each frequency. This can be attributed to the inherent advantages of the multi-level structure, which mitigates voltage stress on individual switches, coupled with the advantage of employing fewer switches compared to the Dual T-type topology.

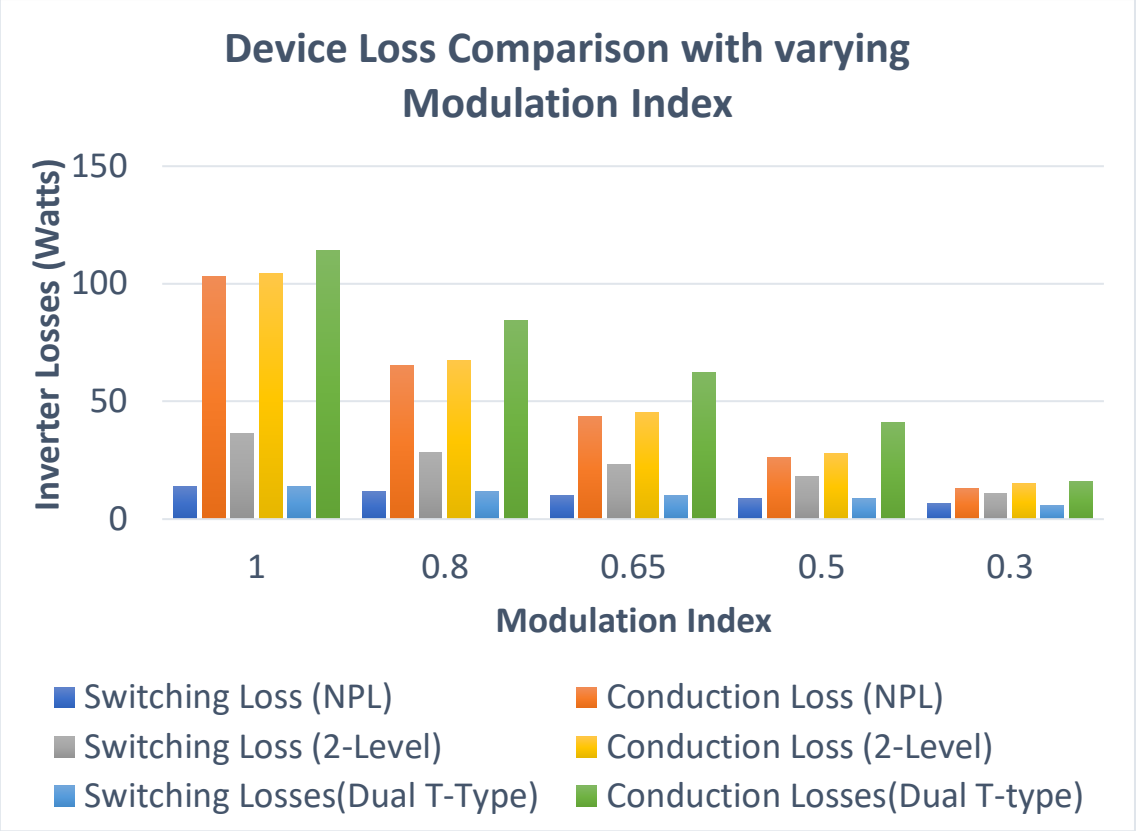


Figure 4. 13 Comparison of inverter losses for the NPL-MLI, dual T-type, and the 2-Level inverter topologies with different modulation indexes.

Figure 4.13 explores the effects of modulation index variation on inverter losses. The results indicate that as the modulation index decreases, overall inverter losses decrease due to reduced voltage and current magnitudes, leading to a significant reduction in conduction loss. Once again, the NPL-MLI demonstrates superior performance in terms of conduction loss at each modulation index. However, it's noteworthy that the Dual T-type topology performs best in terms of switching losses compared to the other two topologies.

4.5 Conclusion

The investigation into the Neutral Point-Less Multi-Level Inverter (NPL-MLI) has unveiled its substantial potential for enhancing the landscape of multi-phase inverter systems. This research meticulously explored the operating principles, switching states, and

commutation logic of the proposed H-type inverter, which forms the core of the NPL-MLI. The simplicity of the topology, achieved through the innovative common-drain BD switch configuration, promises reduced complexity compared to existing multi-phase configurations.

The 3-level PWM generation methodology, employing a single carrier sine-PWM technique, was presented along with detailed explanations and mathematical formulations. This approach not only ensures efficient multilevel voltage generation but also lays the groundwork for achieving a balanced six-phase output.

Results from extensive simulations using PLECS software provided a comprehensive performance evaluation of the NPL-MLI in comparison to conventional multi-phase alternatives, namely the Dual T-Type and 2-Level Six Phase topologies. The NPL-MLI exhibited superior outcomes in various critical aspects. It displayed lower Total Harmonic Distortion (THD) in phase current, reduced DC-link voltage and current ripples, and minimized switching and conduction losses. The advantages were particularly pronounced at a modulation index of 0.65, showcasing the robustness of the NPL-MLI under varying operating conditions. Furthermore, thermal analysis emphasized the NPL-MLI's enhanced efficiency, with lower losses contributing to reduced thermal stress on components. This is pivotal for achieving prolonged system reliability and longevity. The comparison table highlighted the NPL-MLI's advantages, requiring fewer switches, reduced DC-link capacitance, and simpler PWM complexity, all leading to potential cost savings and improved overall system efficiency.

In conclusion, the Neutral Point-Less Multi-Level Inverter emerges as a promising and efficient solution for multi-phase applications, demonstrating superior performance metrics in terms of output quality, efficiency, and thermal management. The insights gained from this study open avenues for further exploration and practical implementation of the NPL-MLI in diverse high-power, high-voltage variable-frequency drive applications.

4.6 Future prospects

Optimization of Phase Shift:

The current design of the Neutral Point-Less Multi-Level Inverter (NPL-MLI) operates with a 120-degree phase shift between each leg, deviating from the conventional 60-degree

phase shift commonly used in six-phase applications. A future avenue for research and improvement involves optimizing the phase shift to align with the standard 60 degrees. This adjustment could potentially enhance the compatibility of the NPL-MLI with existing six-phase systems and improve its integration into diverse applications. An in-depth investigation into the impact of different phase shifts on the overall performance, efficiency, and harmonics of the inverter is crucial for optimizing its design.

Advanced Control Strategies:

Future research can explore advanced control strategies to further enhance the performance of the NPL-MLI. Implementing sophisticated control algorithms, such as predictive control, model predictive control (MPC), or artificial intelligence-based control, could offer improved precision in regulating the output voltage and current waveforms. These advanced control techniques may contribute to the better dynamic response, faster transient behaviour, and increased adaptability to varying load conditions. Investigating the feasibility and effectiveness of such advanced control strategies in the NPL-MLI context could be a valuable area for future exploration.

Integration with Renewable Energy Systems:

The increasing prominence of renewable energy sources calls for the development of power electronic systems that can efficiently interface with these sources. Prospects for the NPL-MLI involve exploring its integration with renewable energy systems, such as solar or wind power. Investigating how the NPL-MLI can contribute to improved energy harvesting, grid-tied applications, or standalone renewable energy systems is a promising avenue. This includes adapting the inverter for grid synchronization, exploring energy storage solutions, and assessing its performance in microgrid applications. The NPL-MLI's potential role in advancing the integration of renewable energy into power systems represents an exciting and socially impactful direction for future research.

CHAPTER 5: CONCLUSION AND FUTURE WORK

5.1 Conclusion

This thesis presented a comprehensive investigation into the design, simulation, and performance evaluation of advanced inverter systems, focusing on three key areas: the testing of an optimally designed GaN inverter, the design of an LC filter for harmonic mitigation, and the exploration of a novel Neutral Point-Less Multi-Level Inverter (NPL-MLI) topology.

In Chapter 2, the design, experimental and simulation verification of a 3-phase GaN inverter were discussed. The main contribution lies in the integration of hardware experiments alongside simulation studies for a 3-phase GaN inverter. Building upon the design scheme of a previous student, hardware experiments were conducted to compare the double pulse test results and parasitic components. The new layout prioritized minimizing parasitic effects to improve the GaN inverter performance in terms of energy efficiency and switching characteristics. Double pulse test experiments validated the effectiveness of the design modifications, demonstrating improvements in turn-on energy losses and switching times. These enhancements underscored the success of the design improvements implemented in the GaN inverter, making it a viable solution for motor drive applications.

Chapter 3 focused on the design of an LC filter for a three-phase inverter system. Leveraging insights from a comprehensive literature review, the passive filter is integrated into the inverter output to target different harmonic frequencies. Simulation studies validated the effectiveness of the hybrid filter in achieving harmonic suppression objectives, with the LC filter attenuating higher-order harmonics. Experimental validation and further research into filter sizing and constraints were recommended for future endeavours.

In Chapter 4, the investigation into the Neutral Point-Less Multi-Level Inverter (NPL-MLI) highlighted its substantial potential for enhancing multi-phase high-voltage inverter systems. The innovative common-drain BD switch configuration promised reduced complexity compared to existing multi-phase configurations. Results from extensive simulations using PLECS software demonstrated superior performance metrics of the NPL-MLI compared to conventional multi-phase alternatives, including lower Total Harmonic Distortion (THD) and

reduced switching and conduction losses. Thermal analysis emphasized the NPL-MLI's enhanced efficiency and reduced thermal stress on components, contributing to prolonged system reliability and longevity.

In conclusion, the research presented in this thesis contributes to the advancement of power electronics and inverter technology. The improved GaN inverter design, passive filter, and NPL-MLI represent promising solutions for high-voltage motor drive applications, offering improved performance, efficiency, and reliability. The insights gained from this study open avenues for further exploration and practical implementation of advanced inverter systems in diverse high-power, high-voltage variable-frequency drive applications.

5.2 Future work

Moving forward, there are several promising avenues for further exploration and development based on the findings and contributions of the thesis. In the second chapter, while the design and simulation of the GaN inverter have been addressed comprehensively, there remains potential for enhancing its practical implementation. One key aspect is the design and integration of a heat sink to improve thermal management and ensure long-term reliability, particularly under high-power operating conditions. Additionally, conducting a proper 3-phase RL load test would provide valuable insights into the inverter's performance in real-world scenarios, allowing for validation and refinement of the design. Furthermore, analyzing the inverter's behaviour in continuous current mode would enable a deeper understanding of its capabilities and suitability for various load conditions and applications.

In the third chapter, although the design and simulation of the passive filter have been presented, there is scope for further refinement through hardware implementation and experimentation. Utilizing proper motor load specifications identified from the literature review, a practical passive filter could be designed and implemented to validate its performance in harmonic mitigation. Real-world experiments using actual motor loads would provide crucial validation of the filter's effectiveness and pave the way for its practical application in industrial settings.

Moving to the fourth chapter, the investigation into the Neutral Point-Less Multi-Level Inverter

(NPL-MLI) has revealed significant potential for enhancing multi-phase inverter systems with GaN transistors. One avenue for future research involves optimizing the phase shift between each leg of the NPL-MLI. Currently operating with a 60-degree phase shift, deviating from the conventional 30-degree phase shift used in many six-phase motor drive applications, optimizing this parameter could enhance compatibility and integration with existing systems. Furthermore, exploring advanced control strategies, such as predictive control or artificial intelligence-based control, could further enhance the performance and efficiency of the NPL-MLI. Implementing sophisticated control algorithms to improve precision in regulating output voltage and current waveforms would lead to better dynamic response and adaptability to varying load conditions.

In summary, the prospects for the thesis encompass a range of opportunities for further exploration and development, spanning from practical implementation and experimentation to optimization and integration with emerging technologies such as renewable energy systems. By pursuing these avenues, the research has the potential to make significant contributions to the field of power electronics and advance the state-of-the-art in GaN-based inverter technology and renewable energy integration.

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