Comparative Study of the Effects of Device Geometry on the DC Characteristics, Linearity and Low-Frequency Noise Performance of Lattice-matched InAlN/GaN HFETs

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ABSTRACT

Comparative Study of the Effects of Device Geometry on the DC Characteristics, Linearity and Low-Frequency Noise Performance of Lattice-matched InAlN/GaN HFETs

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The novel lattice-matched HFETs realized on an epilayer consisting of a thin $In_{0.17}Al_{0.83}N$ barrier layer grown on top of an undoped GaN channel have been demonstrated over the past decade to enjoy improved stable high-frequency power characteristics compared to their famous AlGaN/GaN counterparts. This is specially thanks to employing a lattice-matched barrier enjoying substantial spontaneous polarization-induced sheet charge density.

An extensive body of research implies a significant correlation exists between electronic device technology, the level of 1/f noise, and the manifestation of generation–recombination (G-R) bulge signatures. This correlation has been shown to offer a highly sensitive foundation for reliability and further performance optimization of electronic devices. A decrease in low frequency noise (LFN) has a significant impact on oscillator phase noise and the performance of intermediate frequency (IF) amplifiers and mixers Thus, in this thesis, the low frequency drain noise-current characteristics of metallic-face InAlN/AlN/GaN heterostructure field effect transistors (HFETs) having fin structures only under the gate, while maintaining a planar structure in the access regions, are compared to those of the HFETs having fin structures stretched from source to drain. This work aims to address the possible difficulties in the performance of these devices. Evidence indicates that both device types follow the trends of carrier number fluctuation (CNF) with correlated mobility fluctuation (CMF) model of 1/f noise. Devices having fin structures just under the gate are exhibiting improved 1/f noise performance with lower drain noise-current spectral density.

Since a good gate-transconductance (G_m) linearity, specially at high gate over-drives, is essential to linear high-frequency amplifiers intended for use in modern telecommunication system (such as 6G networks), enhancing the linearity of the deeply scaled HFETs implemented on such epilayers is very much in demand. Moreover, the investigation of the on-state breakdown mechanism is beneficial for the definition and design of the safe operation area (SOA) in GaN-based high power amplifiers and switches. In this thesis, I have investigated the impact of the scaling of the gate-source length (L_{GS}) and gate length (L_G) on the DC characterises and gate-transconductance (G_m) linearity of metallic-face InAlN/AlN/GaN heterostructure field effect transistors (HFETs) having fin structures only under the gate and those having them stretched from source to drain. Evidence for both device types suggests that the downscaling of L_{GS} and L_G augments the electron velocity in the source-access region, as a result of which the higher carrier density under the gated-channel improves the maximum drain-current density but not necessarily the G_m linearity of the device. It is shown that the devices having a planar and longer source access region are exhibiting relatively improved gate-transconductance linearity. In addition, the downscaling of the L_G is observed to have a positive influence on device linearity. However, the negative impact of the downscaling of the L_{GS} and L_G on the on-state breakdown voltage has been observed.

In addition, in this thesis I have investigated the effect of partially etching of the gated barrier on the G_m linearity of lattice-matched InAlN/GaN HFETs. Simulation results show an improvement in linearity observed through broadening the gate transconductance characteristics of V_{th}-modulated HFETs over the non-recessed and an alternative recessed HFET, for which gated barrier was uniformly recessed.

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Finally, I would like to dedicate this thesis to my dearest mother, Hina Patel. Without her endless love, patience, sacrifice, and encouragement I would never have been able to complete my graduate studies.

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List of Abbreviations

Abbreviation	Description
2DEG	Two-dimensional electron gas
HFET	Heterostructure field effect transistor
LFN	Low frequency noise
G-R	Generation-recombination
PSD	Power spectral density
CNF	Carrier number fluctuation
CMF	Correlated mobility fluctuation
GVS	Gate voltage swing
UID	Unintentionally doped
DIBL	Drain induced barrier lowering
EBL	Electron beam lithography
NPGS	Nanometer pattern generation system
SEM	Scanning electron microscope
TLM	Transfer length measurement
UV	Ultraviolet
IPA	Isopropyl alcohol
DI water	Deionized water
MERIE	Magnetically-enhanced reactive ion etching
PECVD	Plasma enhanced chemical vapor deposition
RTA	Rapid thermal annealing

Chapter 1

Introduction

1.1 Overview of III-nitride technology

GaN has excellent electronic properties such as wide bandgap (E_g=3.4 eV) [1], high two-dimensional electron gas (2DEG) room temperature low-field mobility (1500 $cm^2/V \cdot s$) [1], high electron saturation velocity ($v_{sat} = 2.5 \times 10^7 \frac{cm}{s}$) [2], and high critical electric field ($E_{critical} > 3 \frac{MV}{cm}$) [3]. As a result of these properties, GaN-channel heterostructure field-effect transistors (HFETs) have been deemed suitable for high power (> 100 W), high voltage ($\geq 600\ V$), high temperature ($> 300\ °C$) [4], and high frequency (f_T/f_{MAX} of 454/444 GHz) [5] operation.

Caused by reliability concerns linked to substantial lattice mismatch between AlGaN and GaN, lattice-matched $In_{0.17}Al_{0.83}N$ barrier has been promoted to replace the AlGaN barrier layer [6]. In spite of the rightly-expected absence of piezoelectric polarization, the high Al content of such a barrier (i.e. compared to the traditional AlGaN barriers) over-compensates the absence of piezo-delivered 2DEG (2-D electron gas) through its spontaneously-polarized contribution [7], [8]. In InAlN/GaN HFETs, just like their AlGaN/GaN counterparts, the 1nm thick AlN spacer often present between the InAlN barrier layer and the GaN channel screens the 2DEG from the alloy scattering of the barrier and partially increases the electron mobility of the HFETs [9], [10].

1.2 Different contributing mechanisms to transconductance (G_m) nonlinearity

In addition to the high operation frequency and the output power of $In_{0.17}Al_{0.83}N$/GaN HFETs, linearity performance of these devices is an important factor for radio frequency applications. Next generation telecommunication systems (such as 6G networks) are extensively adopting techniques like MIMO (multiple input multiple output), in which high linearity amplifiers and switches are needed. To alleviate the problem of non-linearity, and to avoid the resulting signal distortion, it is very important to suppress the gate-transconductance (G_m) drop observed at higher gate voltages.

Several theories have been put forward to elucidate the causes for the nonlinearity of G_m at high voltages. Liu *et al.* claimed that interface and alloy scattering of two dimensional electron gas (2DEG) is the main cause of the nonlinear behavior [11]. Accordingly, in top-gated HFETs, the strength of the vertically induced electric field on the channel increases with gate bias leading to accumulation of electrons closer to the interface of channel and the barrier. This in turn increases interface and remote alloy scattering and as a result causes the maximum drain current and electron mobility to decrease. Kuzmik *et al.* claimed that self-heating at high bias values is the reason behind the nonlinear behavior [12]. As the drain current increases, power dissipation becomes more severe and as result of which channel temperature increases significantly. Thus, velocity and mobility of electrons decrease, which leads to G_m and unity gain cut-off frequency (f_T) drop. Whereas, Palacios *et al.* alluded that dynamic increase of the differential source access resistance with drain current directly affects the high-energy transport properties of electrons and the G_m linearity [13]. According to [13], this is due to the quasi-saturation of electron velocity for electric-fields higher than 10 kV/cm, which directly translates into an increase in the differential source

access resistance. The supporting data for this is shown in Figure 1.1. In this work, they reason that the quasi-saturation in the electron velocity profile can be due to the high optical phonon energy [14] and/or hot phonon scattering [15].

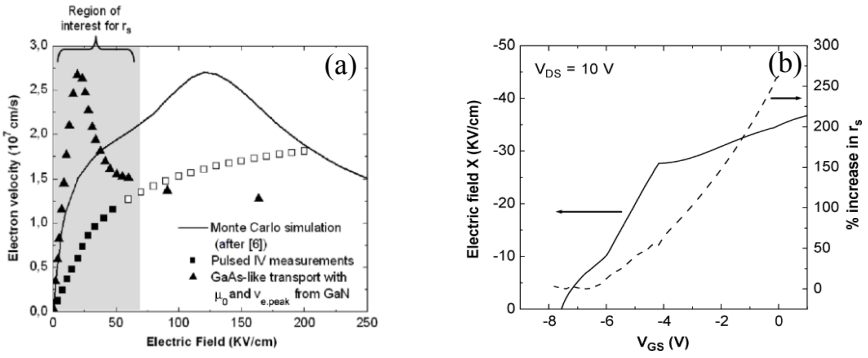


Figure 1.1 (a) Electron velocity vs electric field profile in AlGaN/GaN structures for different transport models (b) longitudinal electric field in the source access region and source access resistance increase at higher bias-voltages [13].

1.3 Literature review of the explored avenues for achieving high linearity III-Nitride HFETs

1.3.1 Self-aligned HFETs

Deeply-scaled self-aligned HFETs with highly-doped source/drain regions have been observed to significantly enhance device linearity performance by boosting electron supply in the source [16]. Shinohara *et al.* fabricated a self-aligned GaN HFET (depicted in Fig. 1.2) having very small access regions with regrown n^+-GaN ohmic contacts to 2DEG in the GaN channel, which shows reduction to the parasitic access resistances at high voltages and as a result dramatical improvement to device linearity.

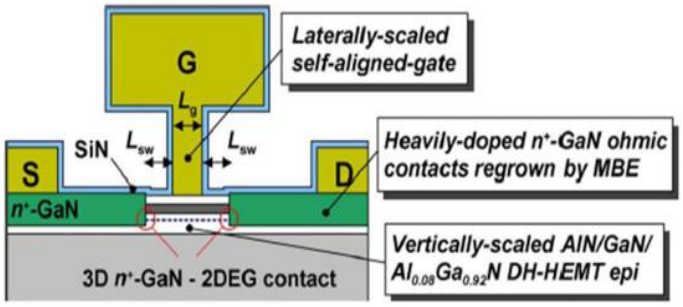


Figure 1.2 Device structure of the deeply-scaled self-aligned-gate double-heterojunction (DH) HFET with heavily-doped regrown n^+-GaN ohmic contacts to the 2DEG on the GaN channel [16].

Figure 1.3 shows that the self-aligned GaN HFET can sustain flat G_m-V_{GS} characteristics even at high gate biases, because of the sufficient electron supply from the n^+-GaN source to the 2DEG channel. Self-aligned GaN HFETs have a relatively small drain-access region leading to poor breakdown characteristics. As a result, they have limited application in high power RF amplifiers.

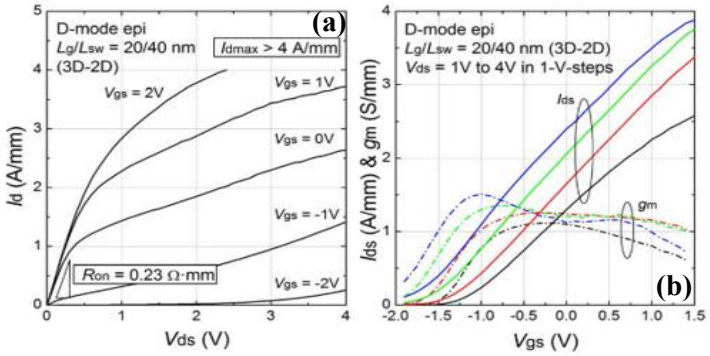


Figure 1.3 (a) Output and (b) transfer characteristics of a depletion-mode self-aligned HFET [16].

1.3.2 Double-channel HFETs

Palacios. *et al.* have designed a double-channel HFET structure (shown in Figure 1.4)

demonstrating a good linearity performance by tailoring the potential difference between the two channels, which in turn decreases the differential source-access resistance [17]. In this structure, after a 1.7-μm thick GaN buffer, a 15-nm thick $Al_{0.32}Ga_{0.68}N$ barrier was grown to supply the electrons. The AlGaN was graded back to GaN during the next 10 nm growth and doped n-type in order to overcome the polarization induced electric field and reduce the barrier height between the two channels. The barrier between the two channels was further reduced by inserting a Si delta doping between the two. Then, an 8-nm-thick GaN top channel layer was grown and capped by the AlN spacer layer to improve the carrier mobility. Finally, a 20-nm $Al_{0.32}Ga_{0.68}N$ barrier layer was grown to provide the electrons for the top channel.

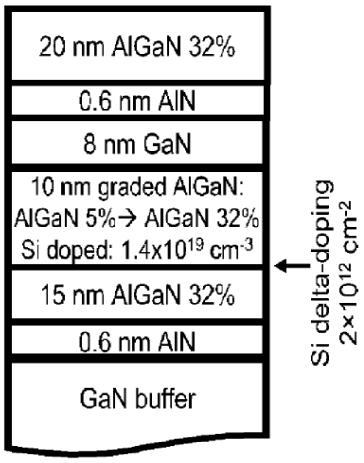


Figure 1.4 Structure of the double-channel HFET [17].

At high current levels, electrons in the top channel have enough energy to overcome the potential barrier between the top- and the bottom-channel and they partially transport to the bottom channel, as illustrated in Figure 1.5 (b). Since both channels are conducting at high I_{DS}, the suppression of dynamically increasing source-access resistance is possible and a very good linearity performance (shown in Figure 1.6) can be realized at high gate overdrives.

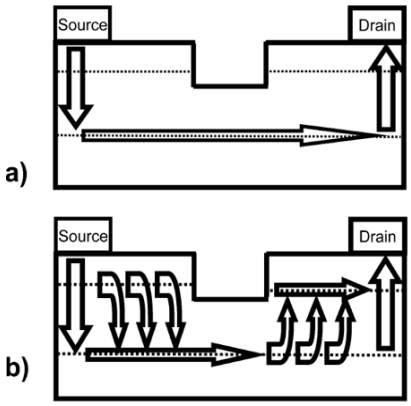


Figure 1.5 Schematic of the current flow in the double-channel device. (a) When current density is low. (b) When the current density is high. [17].

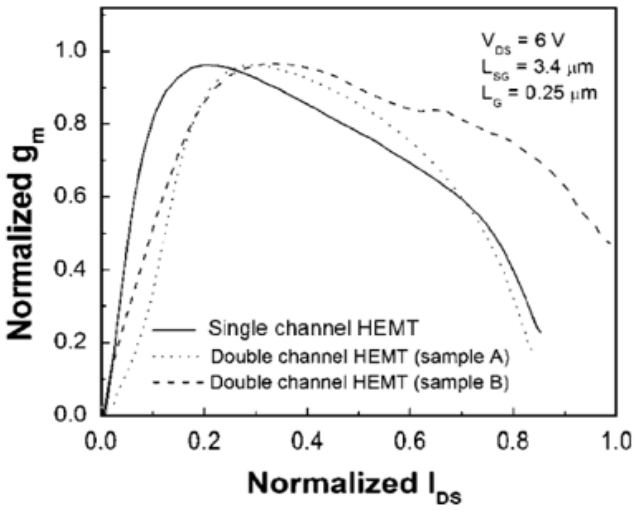


Figure 1.6 Extrinsic transconductance of single channel (solid line) and double channel HFET (dashed and dotted lines) [17].

Downfall of the double-channel HFET is the low output power compared to the single channel device, because of the excessive gate leakage at high drain voltages. This is due to the touching of the gate metal to the sidewall of the recessed region (which prevents the conductivity of the top channel) [18]. Reliability presents the other problem with this device concept, as due to the two conducting channels if proper heat dissipation mechanism is not incorporated in these kinds of HFETs self-heating becomes the reason for device failure.

1.3.3 Fin-like nanowire HFETs

Lee *et al.* reported a nanowire channel GaN HFET with an improved G_m linearity by partially etching InAlN barrier and GaN channel layer just under the gate region (shown in Figure 1.7) [19].

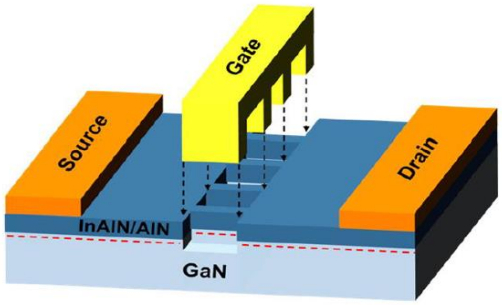


Figure 1.7 Device structure of etched nanowire channel HFET [19].

In the conventional HFETs, differential source-access resistance (R_s) increases at high I_D as the gate bias increase which limits an effective gate overdrive ($V_{OV.eff} = V_{GS} - V_{th} - I_D \times R_S$). Hence the channel-charge density can not rise linearly with an extrinsic gate bias. Fin-like nanowire channel device has much improved G_m linearity because of the suppression of the adverse effect of the dynamic increase of the source-access resistance at high drain current levels. This suppression is due to a small voltage drop in the source-access region thanks to the reduced electric field in this region at high voltages. By keeping the width of the source-access region greater than the channel width, source-access region carries higher current capability than the channel and it acts as a more ideal source. The current drive of source-access region is improved by keeping this region planar and at the same time reducing the effective channel width, as illustrated in Figure 1.8.

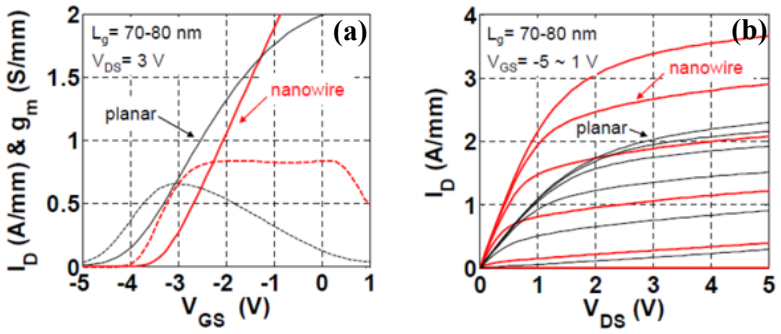


Figure 1.8 Comparison of (a) transfer and (b) output characteristics of fin-like nanowire channel device with planar GaN HFET [19].

This device concept is showing high breakdown characteristic compared to the self-aligned HFETs as the linear source-access resistance has been achieved without eliminating the drain-access region. Accordingly, scaling of the length of drain access region is possible for achieving the targeted breakdown voltage value. However, large parasitic capacitance is introduced to these devices because of the partial etching of the channel region and wrapping of the gate metal around the channel. The two major sources of the additional gate-capacitance are: capacitance between the 2DEG and gate metal and capacitance between additional access region and gate metal. In addition, plasma etching used to fabricate nanowires introduces damage to the nanowire sidewalls and etched surfaces, which lead to a significant f_T drop [19].

1.3.4 Transitional recessed gate HFETs

Wu. *et al.* fabricated transitional recessed gate (TRG) along the gate width by gradually changing the recess depth of a barrier layer through transitional dosed photoetching, which is shown in Figure 1.9 [20]. Low selectivity etching process of the 20 nm thick barrier layer has been used to realize linear inverted triangular shaped recessed gate along the gate width direction having the transitional recess depths ranging from 0 to 16nm. During the device fabrication process

a 120 nm SiN_x passivation layer has been deposited through plasma-enhanced chemical vapor deposition (PECVD) on top of the $Al_{0.25}Ga_{0.75}N$/GaN sample. For TRG, a single layer of the positive photoresist was spin coated and then exposed in the gate foot region by electron beam lithography (EBL) with a series of not-full doses, shifting along the gate width. Then through CF_4/O_2 plasma etching the exposed resist has been removed and as a result the shape was printed into the SiN_x layer. Finally, BCl_3-based slow etching has been used to transfer this shape onto the AlGaN barrier layer.

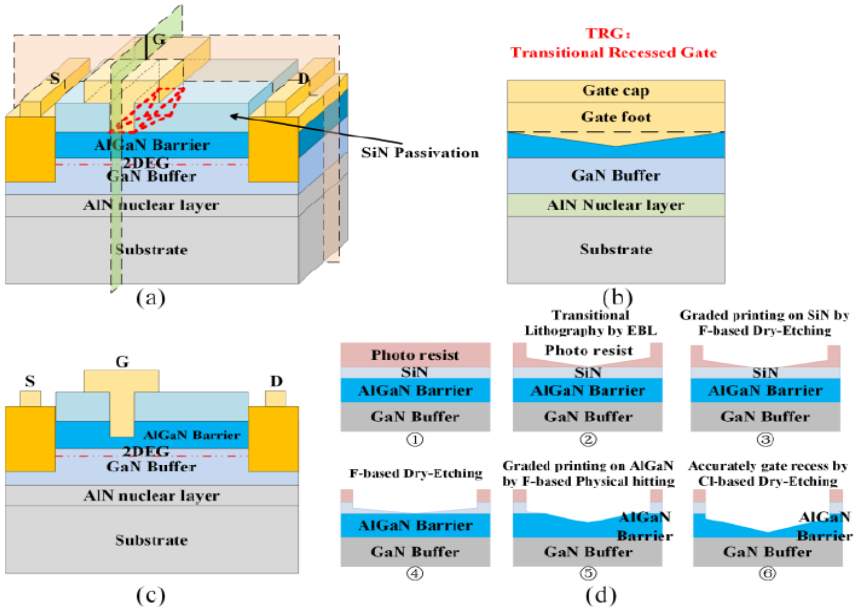


Figure 1.9 (a) The TRG-HFET structure diagram (b) cross-sectional view of TRG-HFET along the gate width (c) cross section view of the TRG-HFET (d) TRG technology processing [20].

The resulting device can be seen as parallel combination of FETs having different threshold voltages. Accordingly, for this device concept there is always an alternative local device to turn-on in order to compensate the transconductance drop of another. The realized TRG-HFET has an excellent transconductance linearity, as shown in Figure 1.10.

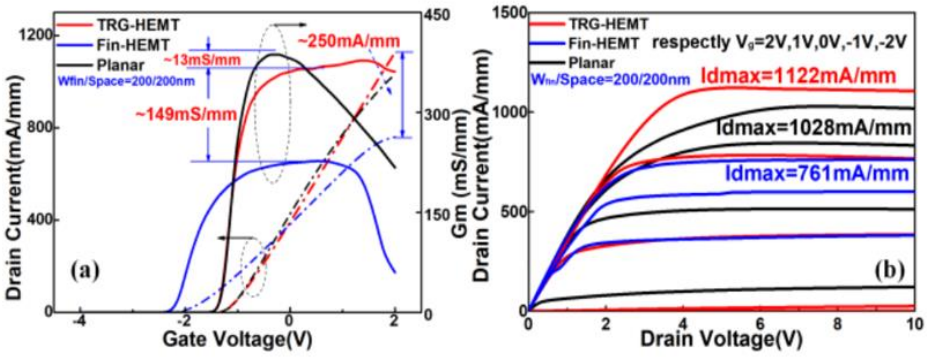


Figure 1.10 Comparison of (a) transfer and (b) output characteristics among planar, Fin-like nanowire and TRG HFETs [20].

Drawbacks of TRG technology are the need for extremely precise electron beam lithography (EBL) process and controlled etching of the barrier layer. Particularly in $In_{0.17}Al_{0.83}N$/GaN HFET where thickness of the barrier is just shy of 10 nm (for high-frequency application as L_g scaling has dictated small barrier thickness and also for the realization of E-mode HFET) this process is overly complicated. In these cases, aluminum has a very high concentration (i.e. 83%), causing the dry etching of the barrier layer to happen so quickly that it is nearly impossible to achieve precise transitional gate structure.

1.4 Low-frequency noise in semiconductor devices

The presence of a large number of noise sources limits the performance of semiconductor devices to different degrees. These noise sources are categorized in terms of their temporal behavior into a number of groups, including thermal noise, shot noise, and Generation-Recombination (G-R) and 1/f (flicker) noise:

1. Thermal noise (Johnson-Nyquist noise):

The average voltage across a conductive element, such as a finite resistor with resistance

R, is zero if all its external sources are disconnected. A more precise observation of the root mean square (RMS) value of the voltage across this resistor at temperatures higher than 0 K, demonstrates a specific power spectral density which stems from the random thermal motion of the charge carriers in the conductive element. The voltage or current power spectral density (PSD) of thermal noise is given with a white spectrum (K_B is the Boltzmann constant):

$$S_V = 4 \cdot K_B T R \tag{1.1}$$

$$S_I = \frac{4 \cdot K_B T}{R} \ . \tag{1.2}$$

2. Shot noise:

Each carrier generates a small pulse of current as it carries a single discrete charge while passing through a potential barrier in a semiconductor. This random generation leads to the current fluctuation around the average current I with a white spectrum:

$$S_I = 2 \cdot q \cdot I \ . \tag{1.3}$$

3. Generation-Recombination (G-R) noise:

The fluctuation of the number of electrons (N) in the conduction band because of the trapping/de-trapping from and to the trap centers is the reason for Generation-Recombination noise in the semiconductor. This kind of fluctuation causes fluctuation in resistance R and conductance G and the noise power spectral density of G-R noise can be calculated through:

$$\frac{S_R}{R^2} = \frac{S_G}{G^2} = \frac{S_I(f)}{I^2} = \frac{S_N(f)}{N^2} = \frac{\overline{(\Delta N^2)}}{N^2} \frac{4\tau}{1+4\pi^2 f^2 \tau^2} \tag{1.4}$$

where ΔN^2 is the variance of the number of the trapped carriers, τ is the relaxation time constant of the trap level, and f is the frequency. The power spectral density of the G-R noise (illustrated in Fig. 1.11) caused by a single trap level possesses a plateau at lower frequencies and follows $1/f^2$ spectrum at frequencies higher than a corner frequency (f_c) determined by the relaxation time

constant and its variation with temperature. Dependence of the trap relaxation time constant on temperature (T) and trap activation energy (E_A) follows the below Arrhenius characteristics (τ_0 is a proportionality constant):

$$\tau = \frac{\tau_0}{T^2} exp\left(-\frac{E_A}{K_B T}\right). \quad (1.5)$$

Trap activation energy can be evaluated through multi-temperature measurement of G-R noise.

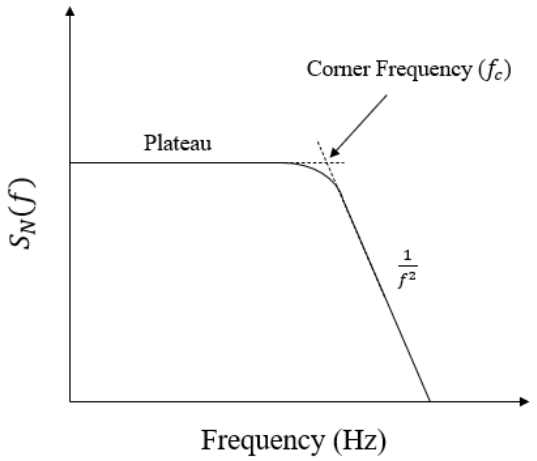


Figure 1.11 G-R Lorentzian power spectral density with the indication of corner frequency (f_c).

4. 1/f noise:

The 1/f noise is a fluctuation in the conductance of a semiconductor stemming from the fluctuation of either number or mobility of the carriers. The noise has a spectral density proportional to $f^{-\gamma}$, where γ is referred to as frequency exponent. It should be noted that a power spectral density would yield an infinite value of energy if the frequency exponent were exactly equal to one from f = 0 to f = ∞, which is theoretically unacceptable. The value of the frequency exponent must be greater than one at the higher frequency end, while a low-frequency plateau is theoretically anticipated.

Low frequency noise is a complicated issue and still theories are being developed to

describe the origin of it in electronic devices. The most acknowledged 1/f noise theories named "carrier-number fluctuation" [21], "mobility fluctuation" [22], and a certain variation of these two old theories referred to as "carrier-number fluctuations with correlated mobility fluctuation" [23] proposed by McWhorter, Hooge, and Ghibaudo, respectively, strive to explain the origin of 1/f noise. Carrier-number fluctuation theory is based on the fluctuation of the number of charge carriers in the channel, trap sites and along the interface. Accordingly, in presence of a sufficient range of energy levels associated with these traps, the integral effect of the Lorentzian spectral densities defined by the generation-recombination of the carriers through these traps, offers a 1/f spectrum (as shown in Fig. 1.12).

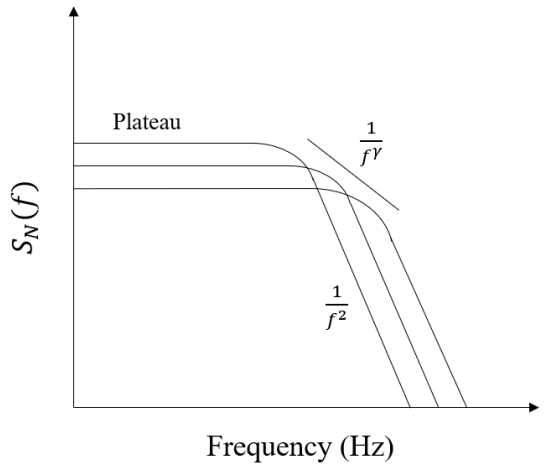


Figure 1.12 1/f noise as a result of the accumulative effect of the carrier Generation-Recombination Lorentzian profiles with a fairly dense distribution of fluctuation time constants.

Where sufficient range of traps are deemed absent, representation of the mobility fluctuation noise theory is provided in terms of an empirical relationship, in which the normalized drain-noise power is evaluated according to [22],

$$\frac{S_{I_D}}{{I_D}^2} = \frac{\alpha_H}{f \cdot N} \tag{1.6}$$

where N is the total number of carriers in the transport channel and α_H is the dimensionless constant referred as Hooge's parameter. The theoretical idea behind the aforementioned relationship is to assert that, when the electrons produce 1/f noise, regardless of the physical mechanism the electrons are involved in, they do it autonomously. It has been observed α_H varies with crystalline quality of the semiconductor and factors affecting the electron mobility [24]. The latter has mainly been related to the mobility fluctuation of the charge carriers due to the fluctuations in their scattering rate [25]. The "carrier number fluctuation with correlated mobility fluctuation" theory considers both the fluctuation of the number of carriers as a result of their trapping/de-trapping and the correlated mobility fluctuation of the charge carriers.

An extensive body of research implies a significant correlation to exist between electronic device technology, the level of 1/f noise, and the manifestation of generation–recombination (G-R) bulge signatures [26], [27], [28], [29]. In addition to suitability of 1/f noise in reliability and material studies, for the special case of HFETs, despite their exceptional high frequency noise performance, in many nonlinear applications such as mixers and oscillators, low frequency noise acts as a limiting factor [24]. A decrease in LFN has a significant impact on oscillator phase noise and the performance of intermediate frequency (IF) amplifiers and mixers [30].

1.5 Research objectives

The objectives of this PhD research can be divided into three major directions. Low-frequency noise (LFN) has been proven to be a suitable method for evaluating the performance of electronic devices. Various low-frequency noise signatures, which can be up-converted to high frequencies, is considered as a figure of merit at the circuit level in electronic and communication systems including both linear (e.g., LNA) and non-linear (e.g., VCO) circuits. Thus, the first

objective was the study of the LFN characteristics of lattice-matched InAlN/GaN HFETs having fin structures only under the gate and those having fin structures stretched from source to drain.

For high-linearity RF power amplifiers, three things are very important: 1. linearity performance 2. output power and 3. operating frequency. The widely adopted method to increase the device linearity performance at a device design level is the realization of the wider source access region connected to the gated-channel. Meanwhile the scaling of the gate-source length (L_{GS}) is having a direct impact on the source access resistance ($R_s = R_c + R_{sheet} \times \frac{L_{GS}}{W_{GS}}$, where R_{sheet} is the sheet resistance, R_c is the ohmic contact resistance and W_{GS} is the width of the gate-source access region) which affects the extrinsic gate transconductance ($G_{m\_ext} = \frac{G_{m\_int}}{(1+G_{m\_int} \times R_s)}$) and scaling of the gate length (L_G) directly affects the device f_T/f_{MAX} performance and RF gain. Thus, the second objective was to evaluate the correlation between the scaling of L_{GS} and L_G and variation of the source access resistance and its impact on the DC performance, transconductance linearity, and on-state breakdown voltage of InAlN/GaN HFETs having fin structures only under the gate and those having fin structures stretched from source to drain.

Devices having higher linearity are required due to complex modulation techniques utilized by 6G networks where amplitude and phase modulations are applied simultaneously in order to transmit as much as data possible for a given bandwidth. Since non-linearity causes signal distortion by saturating the maximum amplitude of the output signal, the last objective was to assess the suitability of multilevel recessing of the gated barrier to improve device linearity performance.

Chapter 2

A comparative study on the effects of planarity of access region on the low-frequency noise performance of InAlN/GaN HFETs

The contributions of this chapter have already been published and most of the materials are taken from [31].

2.1 Introduction

As alluded earlier, GaN-channel heterostructure field-effect transistors (HFETs) are considered to be excellent candidates for high voltage, high power, high temperature, and high frequency applications [32-38] due to the excellent electronic properties of GaN in heterostructures, such as wide bandgap, high electron saturation velocity, high critical electric field, and large two-dimensional electron gas (2DEG) concentration [39].

The GaN-channel HFETs experience sever nonlinearities that cause significant sidebands, gain compression, and signal distortion in the power amplifiers. The premature roll-off of gate-

transconductance (G_m) is responsible for the nonlinearities which is mainly attributed to the dynamic increase of the source-access resistance at high drain currents [13]. Accordingly, Lee et al. reported a fin-like nanowire channel InAlN/GaN HFETs having a wider source access region connected to the gated-channel to suppress the dynamically increasing source-access resistance [19]. This has been reported to facilitate improved device linearity, higher drain current density, and gate transconductance.

Several studies conducted on different devices, including GaN-based HFETs, have demonstrated that 1/f noise is an extremely sensitive characteristic of solid-state devices, which can be effectively utilized as a spectroscopy tool to examine the quality of materials. The correlation between electronic device technology, the level of 1/f noise, and the manifestation of generation–recombination (G-R) bulge signatures has been shown to offer a highly sensitive foundation for reliability and further performance optimization of electronic devices [40].

In light of the importance of these characteristics, in this study, we present a thorough analysis of the LFN characteristics of lattice-matched InAlN/GaN HFETs having fin structures only under the gate (Type-I) and those having fin structures stretched from source to drain (Type-II). Figure 2.1 illustrates the schematics of these two device types.

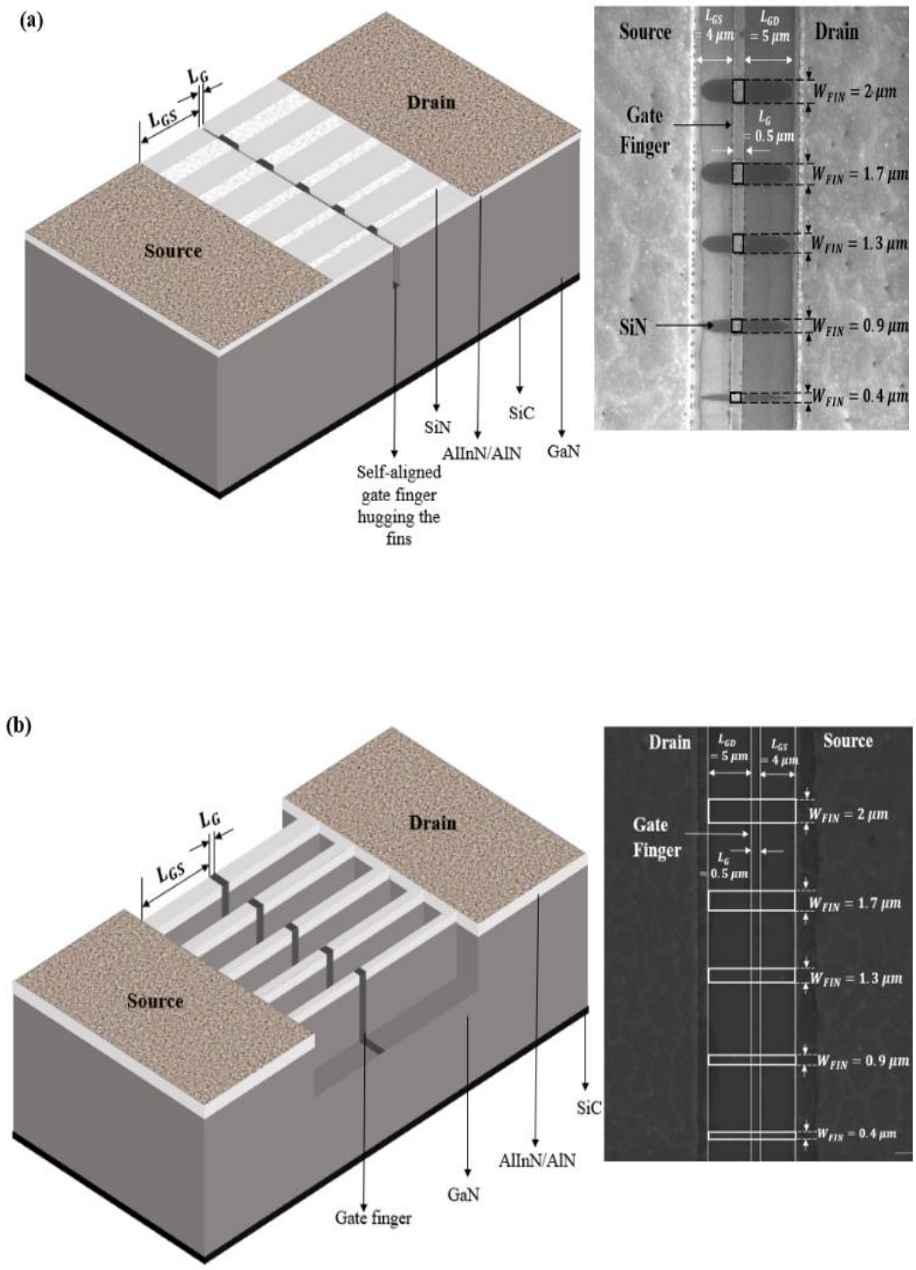


Figure 2.1 3D schematic illustration of the (a) Type-I and (b) Type-II HFET. Inset: Top view SEM images of the fabricated devices.

2.2 Device fabrication and specifications

I used the McGill's nano-tools micro-fabrication facilities (MNM) to fabricate the studied $In_{0.17}Al_{0.83}N$/GaN HFETs. In order to realize sub-micron gate III-nitride HFETs at MNM, I adopted e-beam as the mode of lithography. I have optimized the present process recipe developed by previous members of the group as I am the first one dealing with InAlN/GaN layer structure. Following steps were required to be taken in modifying the existing fabrication process into a process recipe for realization of $In_{0.17}Al_{0.83}N$/GaN HFETs having fins just under the gate while maintaining planar access regions:

- Designing pattern layouts compatible with electron beam lithography (EBL) (i.e. complying with the specifications of the e-beam resists and the writing machine).
- Choosing an appropriate negative resist and modification in the writing parameters in correlation with the specifications of the writing machine (i.e. beam intensity, spot size, accelerating voltage and working distance), which is required to satisfy the need of accurate feature sizes.
- Improving source and drain Ohmic contacts by engineering the metal stack (i.e. type of metal and thickness of each layer).
- Revising rapid thermal annealing (RTA) conditions to get a very small contact resistance so that maximum drain current can be achieved from the fabricated device.
- Optimization of the parameters required for the deposition and etching of the SiN_X passivation layer.

Accurate alignment is the most challenging part of EBL. In order to achieve precise alignment between two masking layers we have to alleviate the deflection of the electron beam from its designated path caused by the accumulation of electrons at the surface of the sample,

which is often the case when a nonconductive substrate is present. Remedies such as implementation of smaller registration marks, minimization of the exposure time by reducing the scanning electron microscopy (SEM) resolution during the alignment process and smaller gate pad surface area to rule out this problem have already been explored by the previous group members. Although they were not successful in achieving an accurate alignment due to the issue of charge accumulation, I have explored and implemented the usage of an anti-charging agent DisCharge H_2OX_2 to dissipate charge from the insulating top layer and prevent dielectric breakdown of the resist. This solution ruled out the latter problem at a great extent.

The studied devices were fabricated on a Ga-face Wurtzite $In_{0.17}Al_{0.83}N$/AlN/GaN heterostructure composed of 9 nm unintentionally doped (UID) barrier, a 1 nm thick spacer layer, a 1.7 μm thick GaN channel, and a 1.45 μm Fe-doped GaN buffer layer grown on a 4-in 4-H-SiC substrate. The fabrication process includes the following major steps: mesa etching, metallization and rapid thermal annealing (RTA) of ohmic contacts (source and drain), deposition and etching of the surface-passivation layer, deposition of schottky gate, and the contact pad deposition.

After generating the pattern through DesignCAD Express, the patterns are exported to the NPGS to specify the beam maneuver during the EBL process. In this process, we have to define writing parameters for the NPGS which includes factors such as exposure area dose, exposure time, electron beam current and line-to-line and center-to-center spacing. All these factors are related through the following formula:

$$D = \frac{I_B \times D_{well}}{cc \times L_S} \tag{2.1}$$

in which, D is the exposure area dose (C/cm^2), I_B is the electron beam current (A), D_{well} is the exposure time for each point being exposed (s), cc is the center-to-center spacing of two adjacent exposure points, and L_S is the line-spacing between the exposure lines. The beam current can be

manually adjusted by the SEM control panel. *cc*, L_S, and *D* are the input parameters of the writing. These three parameters can be set in an NPGS run file. D_{well} is automatically calculated by NPGS through Eq. (2.1).

2.2.1 Mesa isolation and printing the registration marks

The fabrication of the device starts with registration of the mesa and L-shaped alignment marks by using EBL process on the sample covered by the negative photoresist, ma-N 2403. Negative resist has been used because in this step the entire surface area of the sample, except a small portion (i.e., the mesa and alignment marks) should be etched. The aforementioned negative photoresist generates a 0.3 μm thick layer using the normal coating process proposed by the manufacturer (which is coating at 3000 rpm for 30 s). It should be noted that in this process since the large thickness of ma-N resist is comparable to some small feature sizes in the pattern, realizing these small features becomes challenging. This is because of the lack of focus at the resist/sample interface. To solve this issue, values of L_S and *cc* are chosen such that the distance between the exposed dots is small and upon development the realization of the small features can be possible due to the proper exposing of the resist. After the exposure with the 20 KeV e-beam, the sample is developed in Ma-D 525 to remove the resist from the unexposed area. Development time was increased up to 2 times the suggested value of the manufacturer, and vibration in an ultrasonic bath was added to the development process. The writing parameters used for the EBL in this step are summarized in Table 2.1.

The magnetically-enhanced reactive ion etching (MERIE) by using Cl_2/Ar plasma in an Applied-Materials P5000 MERIE system is used for etching. Table 2.2 summarizes the adopted parameters optimized by me for etching.

Table 2.1 Writing parameters used for the EBL of mesa using ma-N 2403.

Parameter	Value
Exposure area dose	235 μC/cm^2
Center to center spacing	10 nm
Line spacing	10 nm
SEM working distance	3 mm
Absorption current on the sample	34 pA
High voltage accelerating the electrons	20 kV

Table 2.2 MERIE recipe steps.

Step	Cl_2 flow (sccm)	Ar flow (sccm)	Magnetic Field (Gauss)	Power (W)	Pressure (mTorr)	Time (s)
1) Stabilize	20	10	0	0	90	30
2) Etch	20	10	70	170	90	60
3) Ramp down	0	60	0	50	0	10

Measurement of the height of the mesa was done by using atomic force microscopy (AFM). Measured mesa height is approximately 100 nm, which can be seen in Figure 2.2.

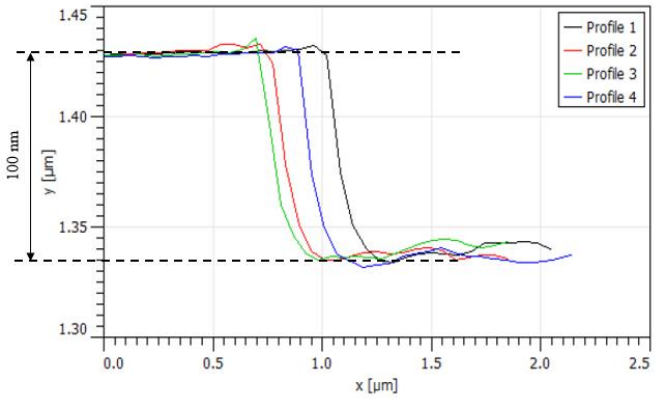


Figure 2.2 Mesa height profile.

2.2.2 Ohmic contacts and SiN_X deposition

It is important to realize very low resistance source and drain Ohmic contacts to the 2DEG

in order to get full advantages of the properties of InAlN/GaN heterostructures. For that I have adopted a new metal stack and corresponding RTA conditions. The process started with coating of the sample with MMA(8.5)MAA-EL11/PMMA-A4 co-polymer positive resist. Anti-charging agent DisCharge H_2OX_2 has been deposited after spin coating of the co-polymer. The writing parameters used for the EBL are summarized in Table 2.3.

Table 2.3 Writing parameters used for the EBL of ohmic contacts using MMA(8.5)MAA-EL11/PMMA-A4.

Parameter	**Value**
Exposure area dose	200 μC/cm^2
Center to center spacing	20 nm
Line spacing	20 nm
SEM working distance	3 mm
Absorption current on the sample	28 pA
High voltage accelerating the electron	20 kV

After EBL, the sample is developed in MIBK/IPA 1/3 for 60 s to remove the resist from the exposed area and then immersed in DI water to stop the development process. A post-bake at 100°C for 60 s is applied to remove the residual developer and moisture from the resist. Prior to the Ohmic contact deposition, the native oxide was removed by keeping the sample in HCl:H_2O (1:4) solution for 2 minutes, then rinsed in DI water and dried out by using nitrogen gun. This step is performed because even a very thin layer of native oxide can drastically increase the ohmic contacts resistance, which in turn decreases the current drive and the output power of fabricated HFET. The NEXDEP electron-beam evaporator was used for metal deposition. The metal stack of Ti/Al/Ni/Au (200Å/1200Å/400Å/500Å) is deposited under the base pressure of 9×10^{-6} Torr. This step is followed by the liftoff in the acetone using ultrasonic bath. Finally, rapid thermal annealing (RTA) process at 765°C for 60 sec using Qualiflow Therm-JetFirst 200 has been used to make an alloyed ohmic contact to the 2DEG channel. Through optimizing the thickness of the metal layers

and annealing conditions (i.e. maximum anneal temperature and duration of the exposure to this temperature), the contact resistance (R_c) and sheet resistance (R_{sh}) extracted through transfer length measurement (shown in Figure 2.3) are consistently about 0.67 Ω·mm and 243 Ω/□, respectively. Table 2.4 presents an overview of published results of contact resistances and sheet resistances for $In_{0.17}Al_{0.83}N$/GaN heterostructure. Where multiple values for a particular metallization scheme and RTA condition are given, the minimum value is presented in the table.

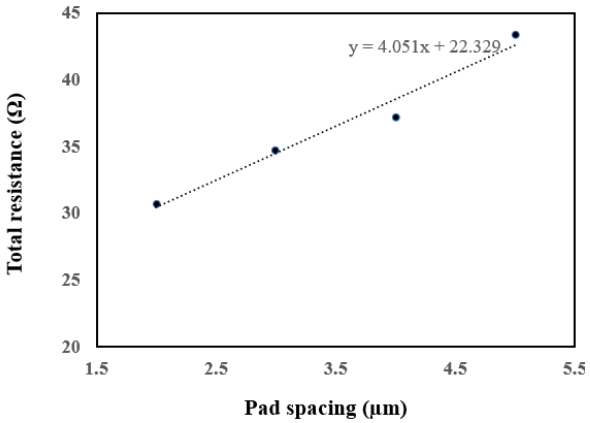


Figure 2.3 Total resistance vs. pad spacing for the adopted Ti/Al/Ni/Au Ohmic metal stack annealed at 765°C for 60 sec. Trend line equation is indicated at the top right.

Table 2.4 Summary of Ohmic contact quality to $In_{0.17}Al_{0.83}N$/GaN.

Metal stack	Thickness	RTA condition	R_C (Ω·mm)	R_{sh} (Ω/□)	Ref.
Ti/Al/Ni/Au	20/120/40/50	850 °C for 30 sec	0.35	241	[41]
	20/120/40/50	725 °C for 30 sec	0.2	270	[42]
	20/120/40/50	725 °C for 30 sec	0.2	-	[43]
	-	830 °C for 30 sec	0.4	-	[44]
	-	850 °C for 40 sec	0.3	-	[45]
	20/120/30/50	780 °C for 60 sec	0.25	214	[46]
	20/120/40/50	775 °C for 60 sec	0.16	466	[47]

For devices having fins just under the gate, after the realization of the ohmic contacts, a

120 nm thick SiN_X was deposited by plasma-enhanced chemical vapor deposition (PECVD). Table 2.5 summarizes the adopted parameters optimized by me to realize 120 nm thick SiN_X.

Table 2.5 PECVD recipe steps.

Step	SiH_4 flow (sccm)	N_2 flow (sccm)	NH_3 flow (sccm)	Power (W)	Pressure (Torr)	Time (s)
1) Soak	0	0	0	0	0	30
2) Pre-deposition	180	2000	0	350	4.5	5
3) Deposition	180	2000	75	350	4.5	13
4) Purge	0	2000	75	0	4.5	60

2.2.3 Fin structures and gate contacts

A third EBL has been performed using negative photoresist, ma-N 2403 to form fin structures of different widths along the gate width in SiN_X. Subsequently dry etching of SiN_X in CF_4/O_2 plasma has been done using MERIE where fin-like structures are protected by negative resist (shown in Figure 2.4). Table 2.6 summarizes the adopted parameters optimized to etch 120 nm thick SiN_X.

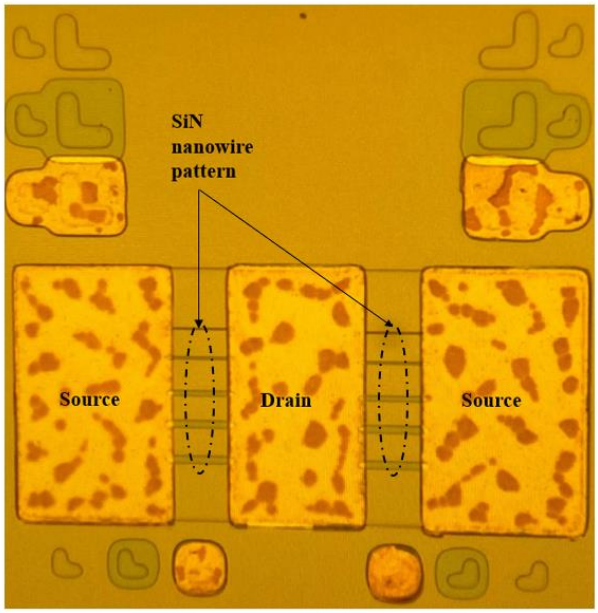


Figure 2.4 Micrograph after deposition of SiN_X and nanowire patterning with e-beam lithography and selective dry etching of SiN_X with CF_4/O_2 plasma.

Table 2.6 MERIE recipe to etch SiN_X.

Step	CF_4 flow (sccm)	O_2 flow (sccm)	Magnetic Field (Gauss)	Power (W)	Pressure (mTorr)	Time (s)
1) Stabilize	40	4	0	0	100	15
2) Etch	40	4	70	100	100	90
3) Ramp down	0	20	0	25	0	15

Then fouth EBL has been conducted to define the gate electrode. The sample has been coated with MMA(8.5)MAA-EL11/PMMA-A4 co-polymer/positive resist to register gate contacts. Anti-charging agent DisCharge H_2OX_2 has been deposited after spin coating of the co-polymer. For the EBL, exposure dose is 200 $\mu C/cm^2$. Other EBL parameters are similar to the ones indicated in Table 2.3. Development in MIBK/IPA 1/3 for 30 sec and a post-bake at 100°C for 150 sec are followed by the dry etching of the top InAlN barrier and AlN spacer layers, as well as about 90 nanometers of the GaN channel layer was done in Cl_2/Ar plasma using the MERIE. During the etching process SiN_X served as the hard mask and protected fins areas. Succeeding this step, SiN_X was dry etched to expose channel area whereas the protected SiN_X by the co-polymer positive resist in the access regions serves the purpose of surface passivation (as shown in Fig. 2.5). This way fin-like structures were formed in the gate opening region without conducting an additional EBL step and as a result of this, the nanowire features have the same length as the gate electrode.

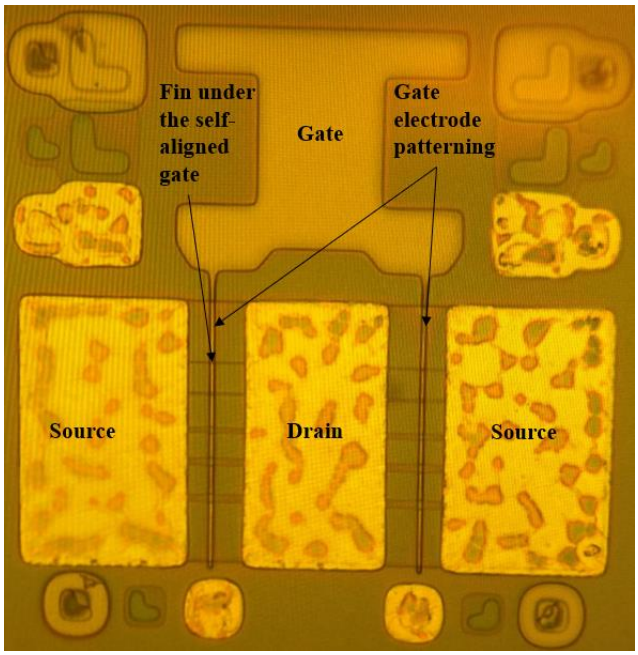


Figure 2.5 Micrograph after gate electrode patterning and dry etching of the barrier and GaN channel layer followed by dry etching of the SiN_X layer to expose the channel area.

Finally, Ni/Au 200Å/200Å gate metal stack using the NEXDEP electron-beam evaporator has been deposited and then the standard lift-off process in acetone using ultrasonic bath is performed to define self-aligned gate (shown in Figure 2.6). The I_G-V_{GS} data showing Schottky behavior of the gate is provided in Chapter 3.

Evidently, the remaining SiN_X in the access regions only provides surface passivation to the parts of the access region aligned with the gated fins of the devices having fins just under the gate. Such a manner of implementation allows a simpler way of implementing the needed small fins.

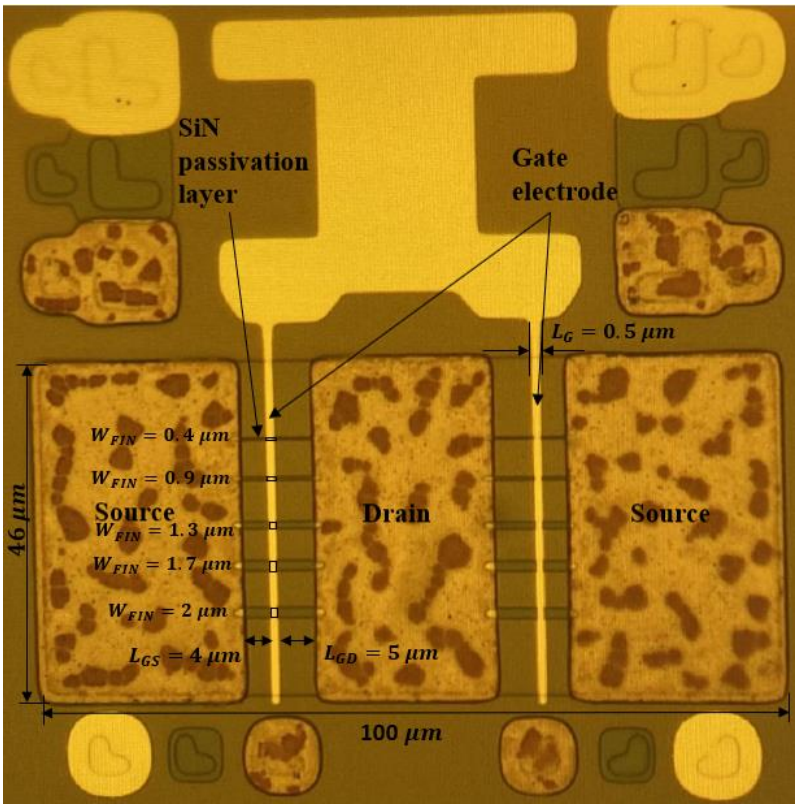


Figure 2.6 Micrograph after gate metal deposition and lift-off.

2.2.4 Pad deposition

Since the dimensions of pads are larger than the maximum writing field of SEM, an optical lithography is used for the definition of this feature. EVG620 mask aligner is used to align the optical mask of the pads with the previously generated patterns. Image reversal lithography using AZ5214 (and developer AZ726) is used in this step. The metal stack of Ni/Au 200Å/500Å is used for the pads deposited by using NEXDEP e-beam evaporator. Figure 2.7 illustrates the micrograph of the fabricated transistor.

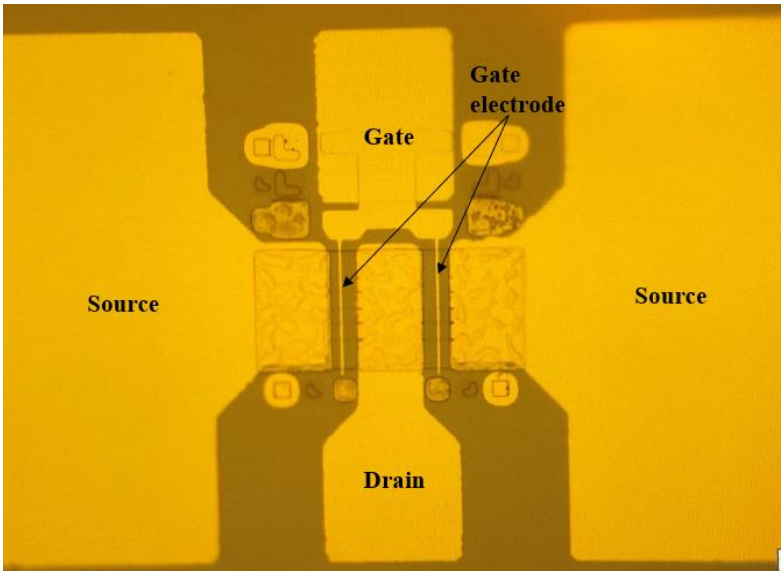


Figure 2.7 Micrograph of a fabricated transistor after deposition of pads.

Following the deposition of contact pads, Keithley 4200-SCS semiconductor characterization system was used for room-temperature on-chip characterization of the fabricated HFETs.

Both device types are consisting of five fin structures of 400, 900, 1300, 1700, and 2000 nm width along the gate width direction. The broad range of threshold voltage (V_{th}) from – 4 V for 2 µm wide fin to – 1 V for 0.4 µm wide fin gives privilege to realize a linear multichannel device, comprised of sets of individual channels each possessing a specific V_{th}. These sets of individual channels turn on sequentially and the sum of the transconductances attributed to the parallel channels can effectively reduce the drop in the G_m at high gate-source over-drives (V_{GS}), essentially yielding a broader G_m-V_{GS} characteristics [48]. This way the choice of the fin structures was made with improvement of linearity in mind. According to the given dimensions, the fabricated devices have overall gate width of 6.3 µm with unless reported otherwise gate length (L_G) of 0.5 µm, gate-source spacing (L_{GS}) of 4 µm, and gate-drain spacing (L_{GD}) of 5 µm.

Tested among a large number of devices, consistently the threshold voltage of the Type-I HFETs is around – 4 V, while that of Type-II is about – 3.7 V. Since the two device types have been realized on pieces cut from different positions on the surface of the wafer, the relatively minor difference between the threshold voltage values defined ideally by the fin of the largest width is deemed acceptable. Nonetheless, for the sake of accuracy, effective gate-source voltage ($V_{GS,Eff}$) defined as the difference between the applied extrinsic gate-source voltage and the threshold-voltage of each device has been employed in our analysis.

Maximum drain-current density of the Type-I HFETs at $V_{GS,Eff} = 4$ V is about 1307 mA/mm and this value is about 1185 mA/mm for the Type-II HFETs, whereas the peak transconductance values of Type-I and Type-II HFET at drain-source voltage (V_{DS}) of 4 V are about 318 mS/mm and 240 mS/mm, respectively. The figure of merit of gate voltage swing (GVS) can be used to quantitively assess the linearity performance of various types of devices. GVS is defined as the gate voltage range across which the value of the transconductance remains at least 80% of its peak value. The GVS of the Type-I HFETs at the said V_{DS} is 4.5 V, while this metric equals 2.8 V for Type-II devices. As anticipated [19], it is very evident that by keeping the width of the access-region greater than the width of the gated channel, channel-charge density can rise closer to an ideal linear characteristic with an extrinsic gate bias (i.e. through maintaining the source-access region resistance well below that of the gated channel resistance).

2.3 Experimental setup

On-wafer LFN characterization was conducted utilizing a measurement setup developed in-house (Figure 2.8) [49]. In order to eradicate the effect of undesired noise sources, batteries and wire-wound resistors were used as part of the bias circuit. Moreover, coaxial cables were used in order to prevent interfering noise sources. All capacitors in this setup are of the order of 1 mF. The deployment of capacitors C_1 and C_2 prevents the noise components caused by batteries and potentiometers from mixing with the internal noise of the devices. Capacitors C_3 and C_4 are used for AC coupling. The use of resistors in this setup is to convert current noise of the device to voltage noise by acting as load resistors. A low-noise amplifier with a voltage gain of 60 dB was used to amplify the noise spectral density. The amplified noise power spectral density was acquired by the dynamic signal analyzer HP35670A (using the Hanning window and 30 averages for the frequency range of 1–10 Hz and 50 averages for the frequency decades from 10 Hz to 10 kHz). The dynamic signal analyzer was calibrated by measuring the thermal noise of wire-wound resistors. The data points with unreasonable overshoot were rejected by the signal analyzer. The drain noise-current was measured, while the gate terminal was AC grounded.

Noise measurements at room temperature were conducted in the linear and early saturation regime to prevent any uncertainties caused by factors arising in the saturation mode of device operation, such as pinch off, carrier velocity saturation, and self-heating which might make the noise analysis gratuitously complex and unreliable [49].

In this work, at least four devices of each type were selected for characterization on each die. A total of two dies were utilized for this evaluation. The DC characteristics of the devices of each type at room temperature were identical (with a variation of less than two percent). The noise

data presented reflects the observed trends among these devices.

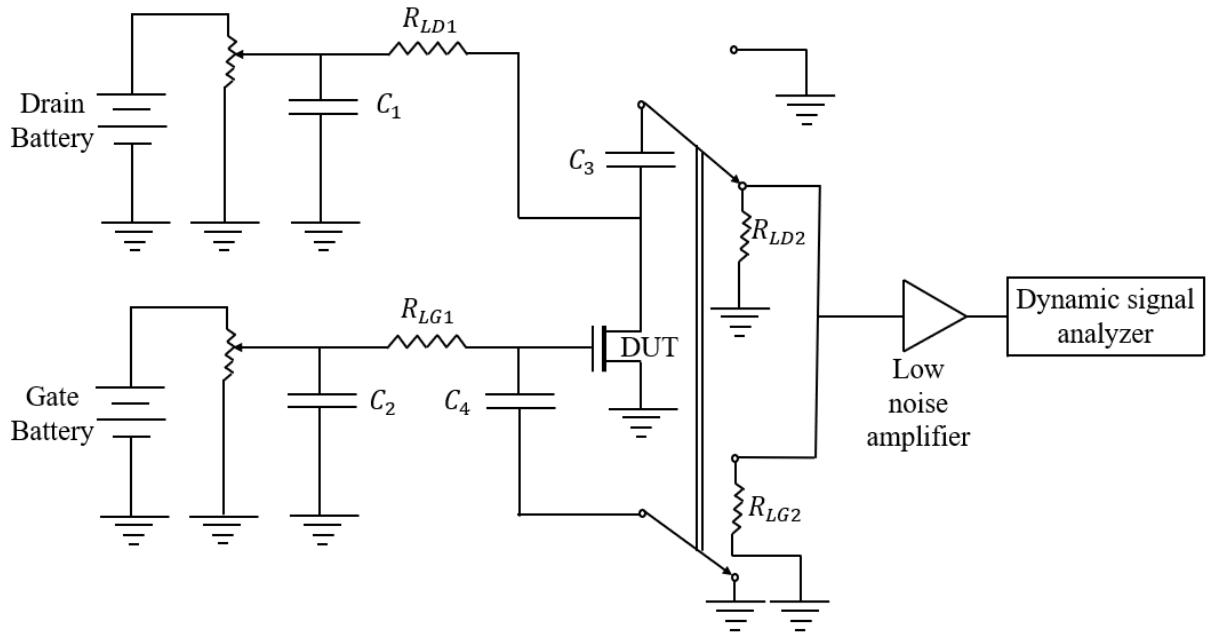


Figure 2.8 Standard low frequency noise measurement setup.

2.4 Experimental results and analysis

Fig. 2.9 shows the comparison of drain noise-current spectral density for the devices studied in this chapter biased in the early linear regime (V_{DS} = 0.25, 0.5, and 0.75 V). As shown here, in the frequency range of 1 Hz to 10 KHz a $1/f^{\gamma}$ characteristics, with a frequency exponent (i.e., γ) varying within the range of 0.98-1.11, is observed on the drain noise-current of both device types. Type-II devices consistently show higher levels of drain noise-current density than Type-I devices at the same effective gate-source voltage and applied drain voltage.

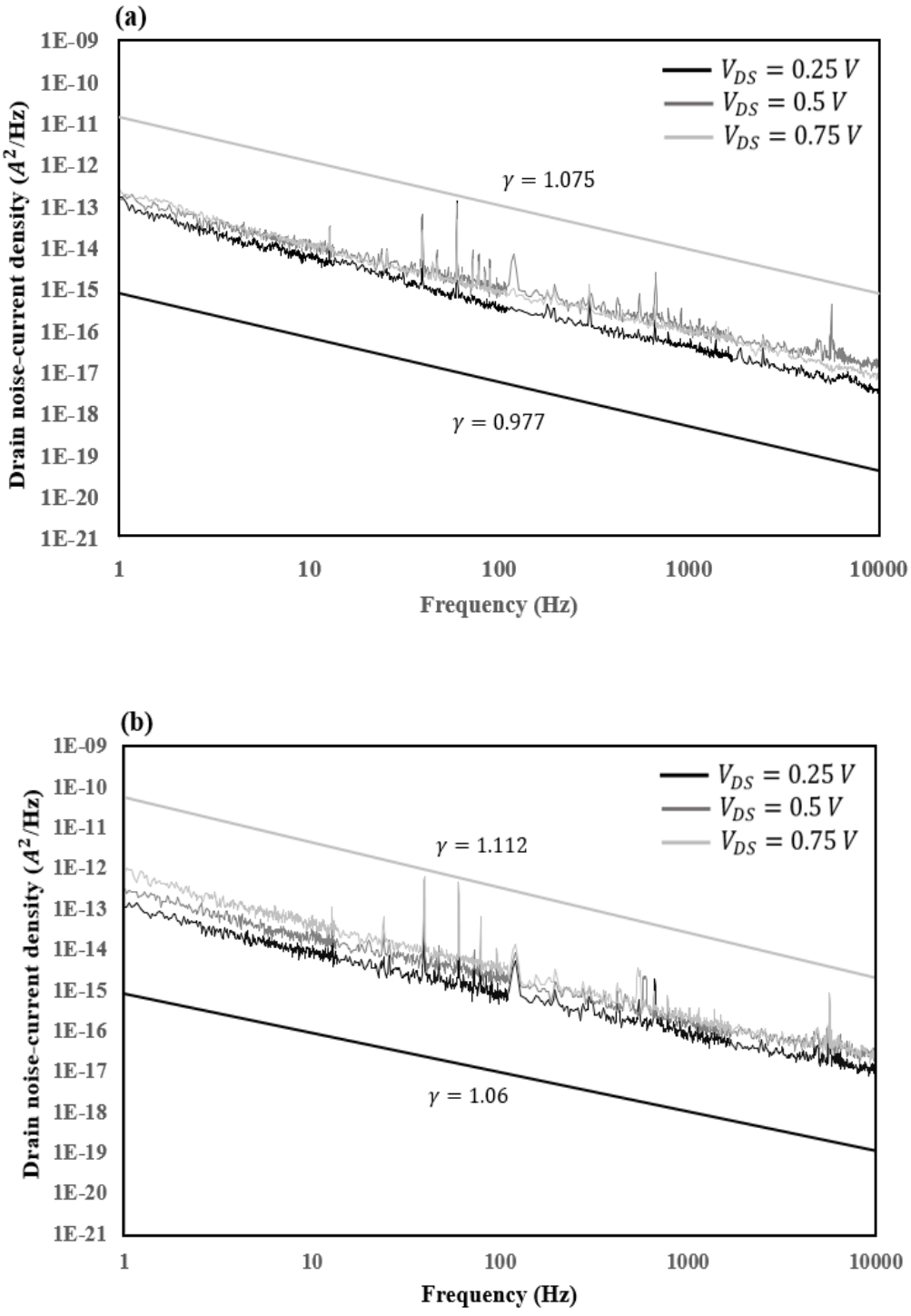


Figure 2.9 A comparison of room temperature drain noise-current spectral density as a function of frequency of (a) Type-I and (b) Type-II devices at $V_{GS,Eff}$ = 3 V and V_{DS} = 0.25, 0.5, and 0.75 V.

In this study, in order to determine the dominant noise source, the models proposed by Peransin et al. [50] and Kammeugne et al. [51] have been explored. For a long time Hooge's empirical formulation has been used based on which Peransin et al. [50] by studying the gate-bias dependence of the normalized drain noise-current (i.e., per-carrier drain noise-current level) formulated a strategy to find out where in the channel the noise is dominant. The latter model disagreeing with this strategy suggests that in order to discriminate between the LFN from the access regions and the gated-channel, the impact of access resistance on the recorded LFN must be studied by varying the gate length [51].

2.4.1 Carrier mobility fluctuation-based model for the determination of the dominant noise source

As summarized in Table 2.7, variation of the normalized 1/f noise level with the normalized effective gate-source voltage (defined as $(V_{GS}-V_T)/|V_T|$), has been suggested to have the possibility of identifying the dominant noise source and resistance along the channel [50]. In this framework, S_{Access} represents the noise spectral density of the access-resistance, while S_{Ch} represents the noise spectral density of the gated-channel. Furthermore, R_{Access} denotes the resistance of the access-channel, and R_{Ch} denotes the resistance of the gated-channel.

Table 2.7 Summary of the criteria developed in [50] for the determination of the dominant noise and resistance along the channel.

		Dominant Noise Source	Dominant Resistance
$\frac{S_I}{I^2}\alpha$	$(V_{GS}-V_T)^{-3}$	S_{Ch}	R_{Access}
	$(V_{GS}-V_T)^{-1}$	S_{Ch}	R_{Ch}
	$(V_{GS}-V_T)^{0}$	S_{Access}	R_{Access}
	$(V_{GS}-V_T)^{2}$	S_{Access}	R_{Ch}

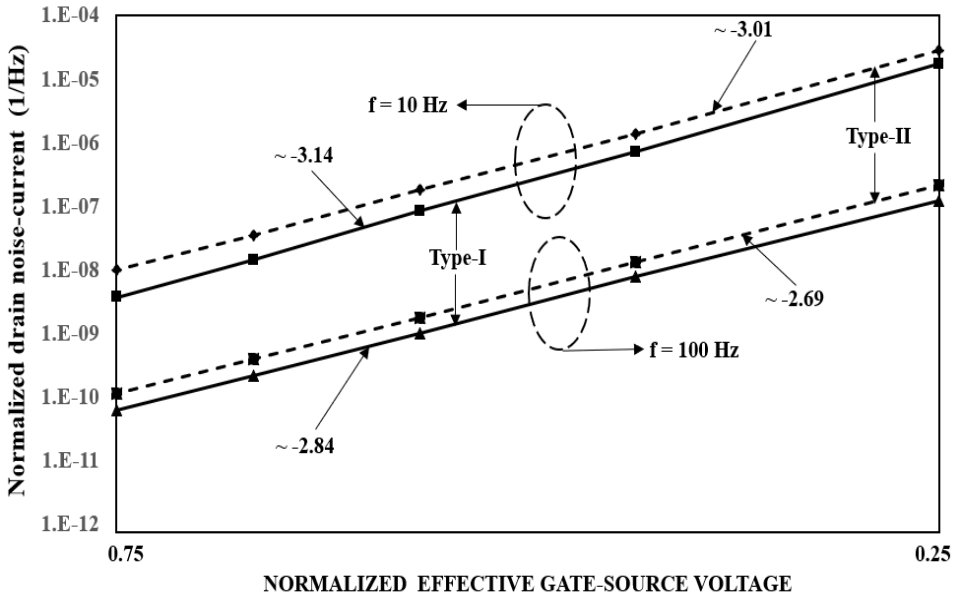


Figure 2.10 Variation of the normalized drain noise-current level at 10 and 100 Hz vs. effective gate-source voltage at room temperature, for $V_{GS,Eff}$ = 1, 1.5, 2, 2.5, and 3 V and V_{DS} = 0.25 V. The presented number on each linear section indicate the slope of the characteristics.

At room temperature, the normalized drain noise-current vs the normalized effective gate-source voltage of both types of devices is demonstrating the existence of an exponential dependence with an exponent of about -3 (as shown in Figure 2.10). This observation suggests that, at room temperature, and in the studied range of bias, for both types of devices if the carrier mobility fluctuation theory prevails [50], the dominant resistance is the access-resistance and the dominant noise source is that of the gated channel.

2.4.2 Carrier number fluctuation with correlated mobility fluctuation-based model for the determination of the dominant noise source

The gate length has been varied for Type-I and Type-II devices, while maintaining the L_{GS} and L_{GD} the same, to see the impact of access resistance on LFN analysis. As alluded in [51], this

is supposed to be more evident for devices having shorter L_G. Among these devices, Fig. 2.11 presents the drain noise-current density as a function of frequency while Fig. 2.12 illustrates the variation of the normalized drain noise-current as a function of drain current for the Type-I and Type-II devices having L_G = 300, 500, and 700 nm and in the early linear regime of operation (V_{DS} = 0.25). The impact of series resistance on LFN can simply be obtained by adding to the channel drain noise-current the contribution of the excess noise stemming from the access region. For instance, in the linear region, the total drain noise-current becomes [52]:

$$\frac{S_{I_D}}{I_D{}^2} = \left(\frac{S_{I_D}}{I_D{}^2}\right)_{channel} + \left(\frac{I_D}{V_D}\right)^2 \times S_{RD} \tag{2.2}$$

where $S_{RD} = R_{ON}{}^2 \times \frac{S_{I_D}}{I_D{}^2}$ is the spectral density of source-drain series resistance and R_{ON} is the ON resistance.

From Eq. 2.2 I can say that if the normalized drain noise-current tends to increase at high drain currents, this is indicative of an enhanced LFN contribution of the access resistance [51]. Based on Fig. 2.12, since there is a drop in the normalized drain noise-current at the higher drain currents (i.e. even for devices having shorter L_G), data suggests that the LFN from access regions is negligible and the dominant noise source is more likely to be the gated channel for all of the studied devices.

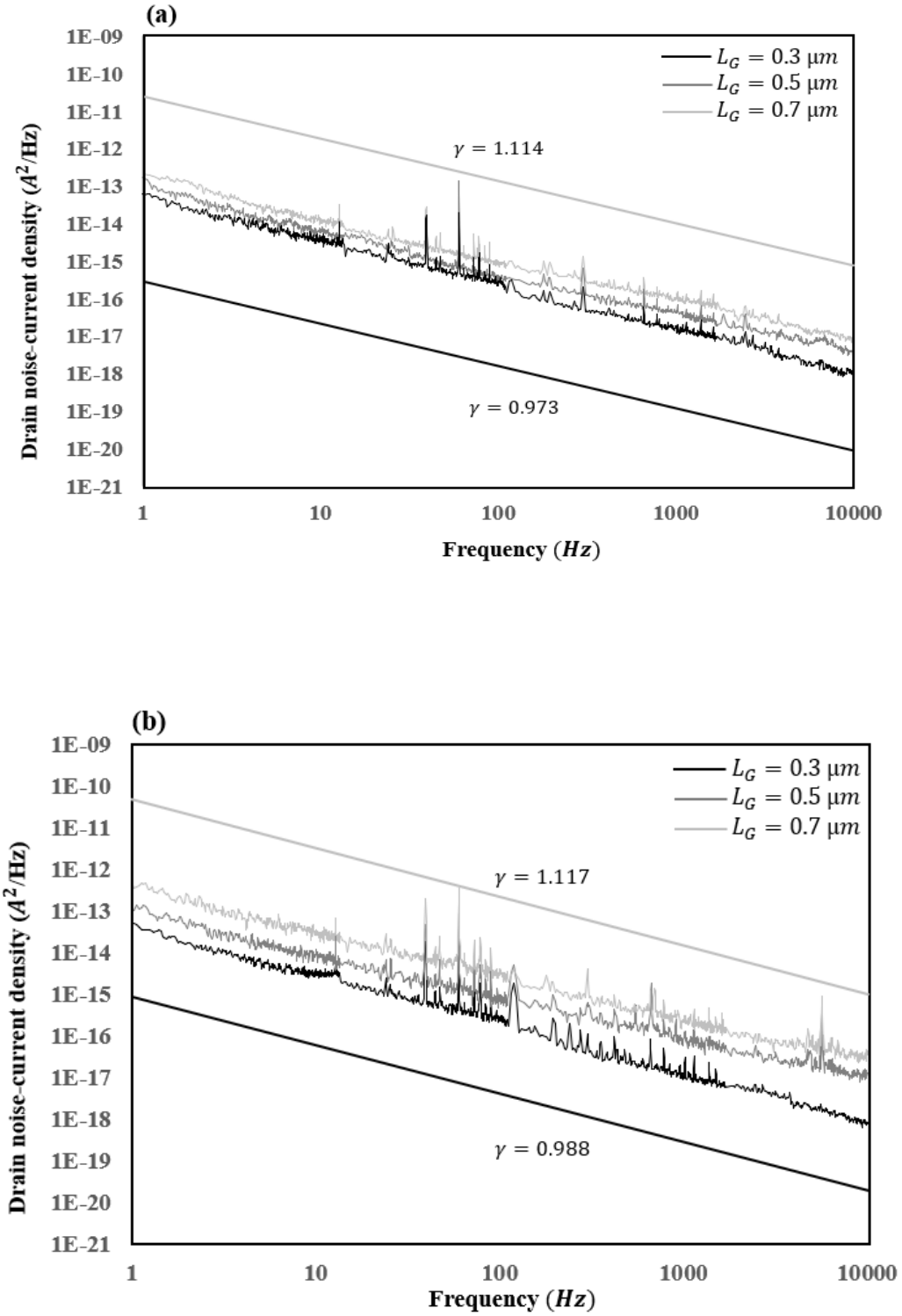


Figure 2.11 Comparison of room temperature drain noise-current spectral density as a function of frequency of (a) Type-I and (b) Type-II devices having L_G of 300, 500, and 700 nm at $V_{GS,Eff}$ = 3 V and V_{DS} = 0.25.

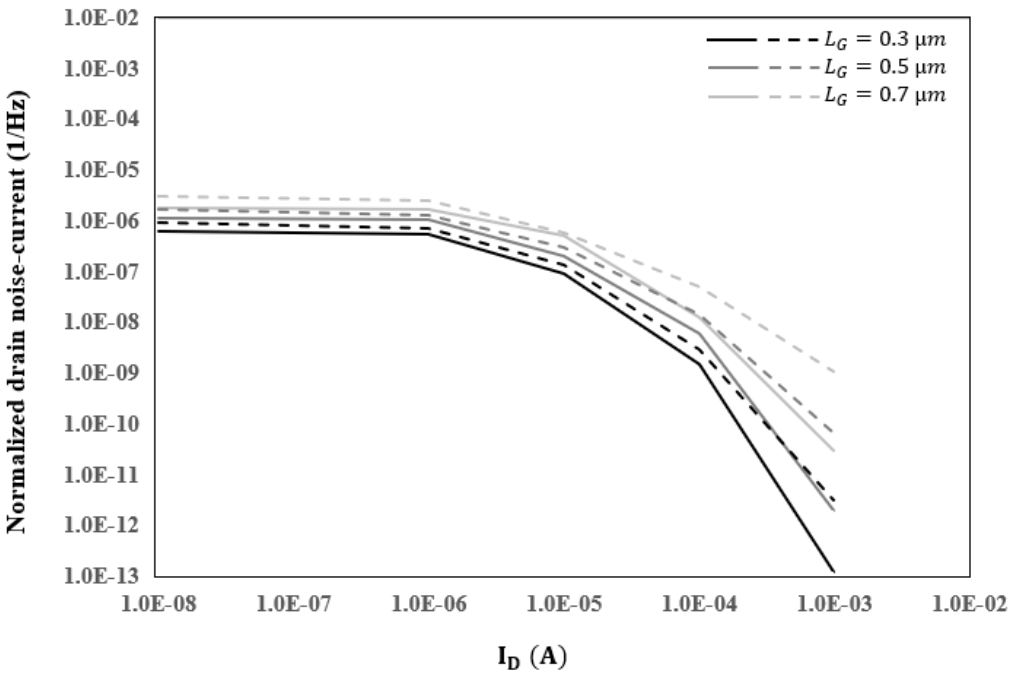


Figure 2.12 Normalized drain noise-current spectral density as a function of I_D of Type-I (solid line) and Type-II (dashed line) HFETs at V_{DS} = 0.25 and f = 10 Hz.

The study of the variation of $\frac{S_{I_D}}{I_D{}^2}$ and $\left(\frac{G_m}{I_D}\right)^2$ with the drain current has been conducted to determine the applicability of the appropriate noise theory for the studied devices in this chapter. As can be seen in Fig. 2.13, $\frac{S_{I_D}}{I_D{}^2}$ and $\left(\frac{G_m}{I_D}\right)^2$ both tend to saturate to a plateau at low drain currents. Additionally, they both exhibit a reduction with increasing the drain current. As suggested in [23], these results satisfy the carrier number fluctuations (CNF) with correlated mobility fluctuations (CNF/CMF) theory, which considers both the change of the flat-band voltage (V_{FB}) following the trapping/de-trapping of carriers and the mobility fluctuation of the charge carriers:

$$\frac{S_{I_D}}{I_D{}^2} = \left(1 + \Omega \frac{I_D}{G_m}\right)^2 \left(\frac{G_m}{I_D}\right)^2 S_{V_{FB}} \tag{2.3}$$

where $S_{V_{FB}}$ is the flat-band voltage power spectral density, which depends on the volume trap density, the effective channel area, the frequency and the tunneling constant between channel and traps and Ω is the CMF coefficient given by:

$$\Omega = \alpha_{sc}\mu_{eff} \tag{2.4}$$

where μ_{eff} is the effective mobility and α_{sc} is the Coulomb scattering coefficient.

At low drain currents, where $\frac{S_{I_D}}{I_D{}^2}$ and $\left(\frac{G_m}{I_D}\right)^2$ are varying similarly with I_D, and where there is no significant difference in noise performance between the two studied device types, the model presented in [23] suggests that the dominant noise source is the CNF. At higher drain currents, where there is a substantial difference between $\frac{S_{I_D}}{I_D{}^2}$ and $\left(\frac{G_m}{I_D}\right)^2$, and where Type-II HFETs are showing higher normalized drain noise-current than Type-I HFETs, the model presented in [23] suggests the dominant noise source to be the CMF.

Considering the applicability of the CNF/CMF theory for a wide range of I_D, the model proposed by Kammeugne et al. [51] has been determined more convincingly adoptable for the determination of the dominant noise source among the reported devices.

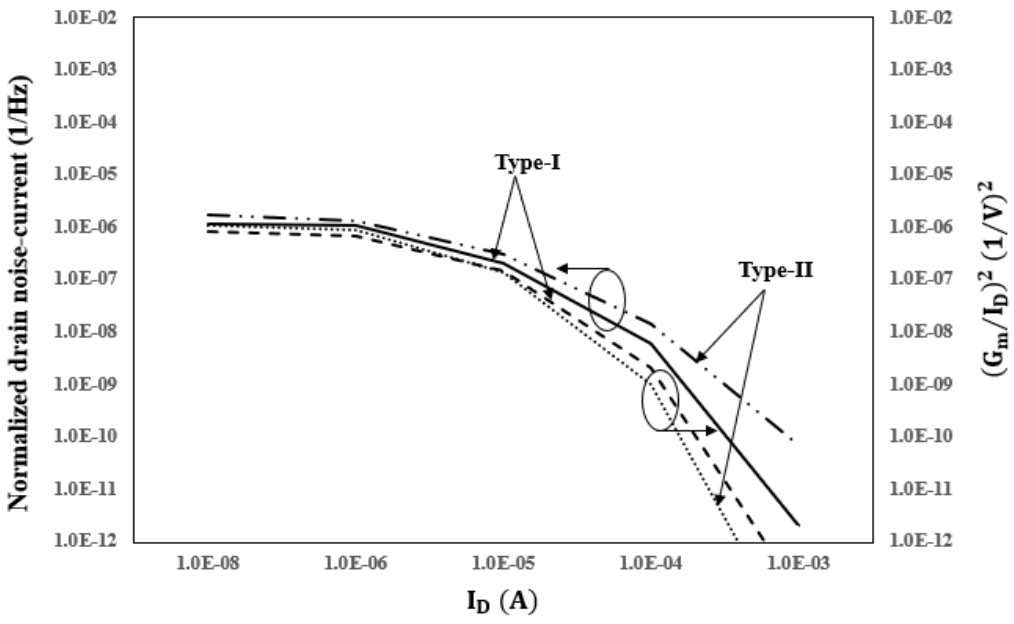


Figure 2.13 Comparison of normalized drain noise-current spectral density and $(G_m/I_D)^2$ versus I_D at V_{DS} = 0.25 and f = 10 Hz.

Having made the observation of the dominance of the noise of the gated channel, studying the variation of the normalized drain noise-current versus the drain current has been observed to provide an interesting link between the LFN performance of the two device types and their earlier-mentioned differences in terms of dynamic variation of source access region resistance [19]. According to what has been reported in the work of Lee et al. [19], dynamically increasing source-access resistance of Type-II devices decreases the effective drive between gate electrode and the gated channel at higher drain currents, whereas due to the wider source-access region of Type-I HFETs, the source access resistance stays well below that of the gated channel for this latter group of devices. As a result, for this device type a large supply of the carriers from the source-access region to the gated-channel takes place. Considering the noted significance of mobility-fluctuations at high drain currents, the resulting presence of higher sheet carrier density under the

gated channel for the Type-I HFETs at relatively higher values of I_D likely results in screening of the Coulomb interactions between channel carriers and scattering centers present in the channel or in the barrier layer [53]. Owing to this screening effect, both the mean value of the Coulomb scattering rate and the mobility fluctuations are expected to reduce, resulting in a reduced noise level of Type-I devices in comparison to Type-II HFETs. Also, the presence of relatively higher carrier density in Type-I HFETs at high drain currents overshadows the fluctuation of the number of charge carrier under the gated-channel, resulting in lower value of CNF term $S_{V_{FB}}$ compared to that of the Type-II HFETs for which the impact of CNF contribution is more evident. However, close to the threshold voltage the current supply from the source-access region to the gated channel stays at the same level. As a result of which, there can not be any substantial difference in the screening effect and/or carrier number fluctuation due to trapping/de-trapping of the carriers among the two device types, yielding the noise level to remain the same at relatively low drain currents.

2.5 Conclusion

The InAlN/GaN HFETs having fin structures present only in the gated channel exhibited not only the expected much better direct current (DC) performance, but at the same token a better 1/f LFN performance compared to the device having fins stretched from source to drain. These improvements are believed to have originated from the wider source-access region of the HFETs having fin structures present only under the gate which facilitates in maintaining the source access resistance well below of the gated channel. LFN in both types of HFETs is representable by the carrier number fluctuations with correlated mobility fluctuation, whereas the noise of the gated

channel has been deemed likely to be the dominant noise source. The presence of higher sheet charge density under the gated channel for devices having fins only under the gate can be explained by reducing the chances of mobility fluctuation owing to the carrier screening effect and the overshadowing of the carrier number fluctuation which is the result of trapping/de-trapping and/or tunneling of the carriers.

Chapter 3

Investigation of the DC performance, linearity and on-state breakdown voltage of InAlN/GaN HFETs via studying the impact of the scaling of L_{GS} and L_G on the source access resistance

The contributions of this chapter have already been published and most of the materials are taken from [54], [55].

3.1 Introduction

Over the past two decades, the GaN-channel heterostructure field-effect transistors (HFETs) have been extensively studied due to the excellent electronic properties of GaN in heterostructures, such as high electron saturation velocity, high critical electric field, and large two-dimensional electron gas (2DEG) concentration [39]. As a result of these properties, GaN-channel HFETs are arguably the front runner candidates for high power, high voltage, and high frequency operation [32-38].

In addition to the high operation frequency and the output power of GaN-channel HFETs, linearity performance of these devices is an important factor for radio frequency applications. Next

generation telecommunication systems (such as 6G networks) are extensively adopting techniques like MIMO (multiple input multiple output), in which high linearity amplifiers and switches are needed. To alleviate the problem of non-linearity, and to avoid the resulting signal distortion, it is very important to suppress the gate-transconductance (G_m) drop observed at higher gate voltages.

Several hypotheses including mobility degradation due to interface roughness [11], self-heating effects [12], and emission of optical phonons [15] have been put forward to elucidate the causes for the nonlinearity of G_m at high bias values. Palacios et al. claimed that the key reason behind the nonlinear behavior of GaN HFETs is the dynamic increase of the differential source access resistance with drain currents, which directly affects the high-energy transport properties of electrons [13]. Accordingly, Lee et al. reported a fin-like nanowire channel InAlN/GaN HFETs having a wider source access region connected to the gated-channel to suppress the dynamically increasing source access resistance [19]. The mechanism behind the off-state breakdown (BV_{off}) characteristics that dictate the power range of GaN-based power devices has been the subject of intense research [56-58]. However, only a limited number of works have been reported on the investigation of the on-state breakdown mechanism in GaN-channel HFETs, although the high-power state of high current and high voltage is typically an intermediate state for both RF power amplifiers in large-signal operation and power switches in the switching process of turn-on and turn-off [59-62]. The investigation of the on-state breakdown mechanism is beneficial for the definition and design of the safe operation area (SOA) in GaN-based high power amplifiers and switches [63], [64].

In light of the importance of the scaling of device geometric parameters and their impact on the source access resistance, in this chapter, I present a thorough analysis of the DC performance, linearity, and on-state breakdown voltage of the lattice-matched InAlN/GaN HFETs

having fin structures only under the gate (Type-I) and those having fin structures stretched from source to drain (Type-II) with varying L_{GS} (for fixed L_G and L_{GD}) and varying L_G (for fixed L_{GS} and L_{GD}). Figure 3.1 illustrates the schematics of these two device types.

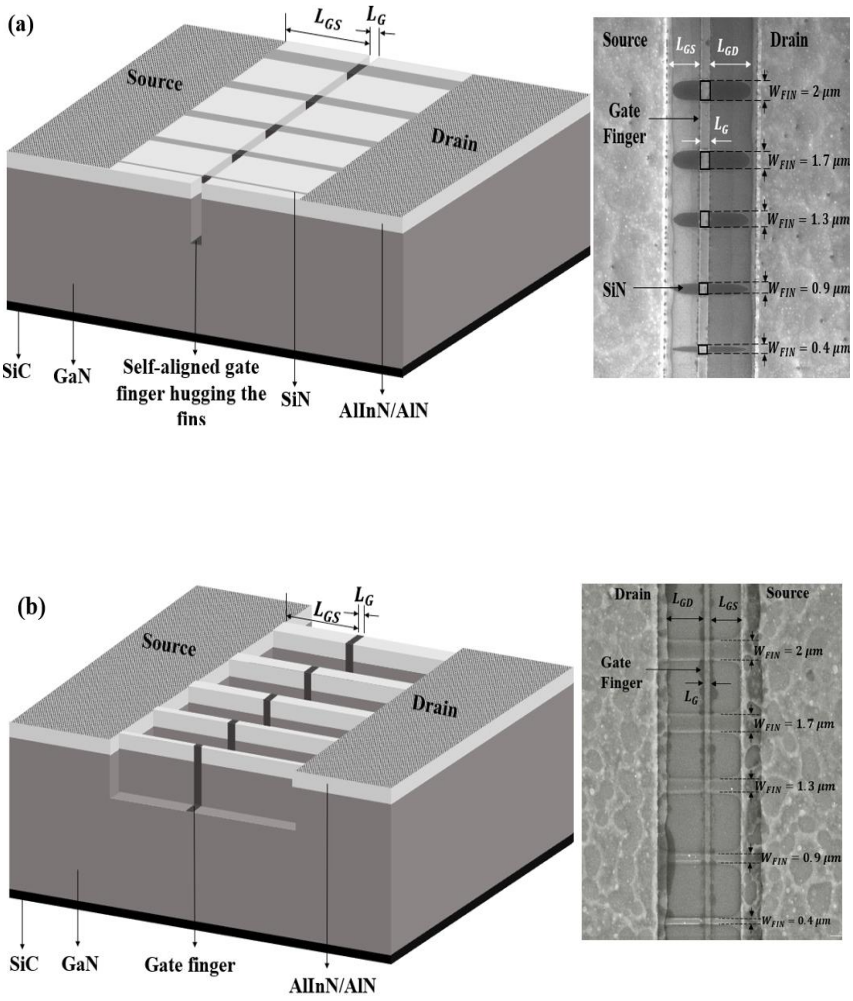


Figure 3.1 3D schematic illustration of the (a) Type-I and (b) Type-II HFET. Inset: Top view SEM images of the fabricated devices.

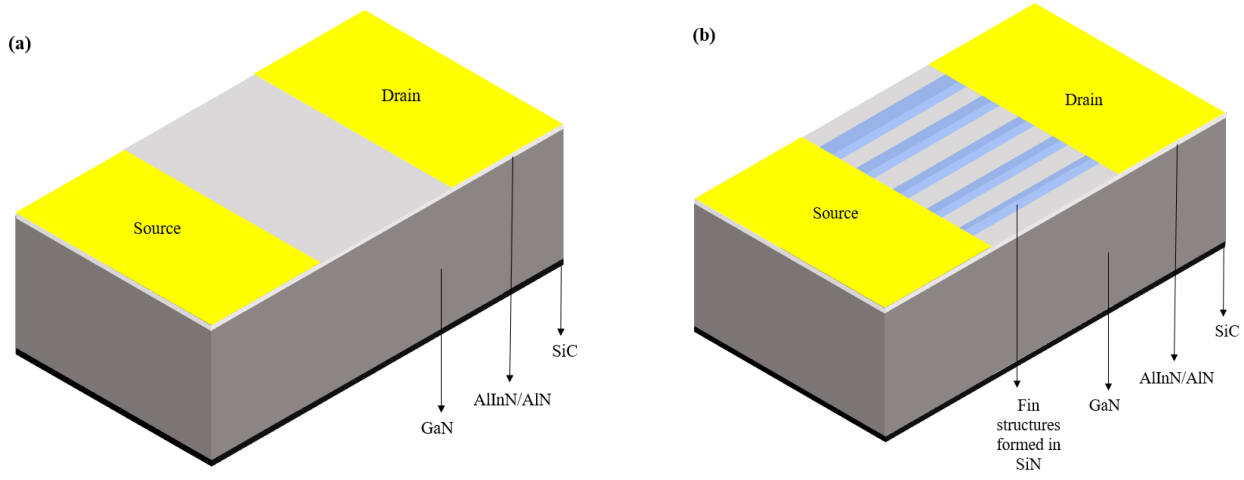
3.2 Device fabrication

The devices studied in this study were fabricated on a Ga-face Wurtzite $In_{0.17}Al_{0.83}N$/AlN/GaN heterostructure composed of 9 nm unintentionally doped (UID) barrier, a 1 nm thick AlN spacer layer, a 1700 nm thick GaN channel, and a 1.45 μm Fe-doped GaN buffer layer grown on a 4-in 4-H-SiC substrate.

The device fabrication process started with spin coating of the sample with ma-N 2403 negative resist to define the isolation features using electron beam lithography (EBL) of beam energy 20 keV. Mesa isolation to 100-nm depth was performed post developing the sample in ma-D 525, employing magnetically enhanced reactive ion etching (MERIE) using Cl_2/Ar plasma. Then, followed the second EBL conducted with the same beam energy as step one, after the sample was coated with MMA(8.5)MAA-EL11/PMMA-A4 co-polymer positive resist for the registration of the Ohmic contacts. After developing the co-polymer photoresist in MIBK/IPA 1/3 solution for 1 min, the sample underwent immersion in HCl solution to eradicate the native oxide layer. Subsequently, Ohmic metallization was carried out using NEXDEP e-beam evaporation, followed by lift-off in acetone using ultrasonication. After depositing Ti/Al/Ni/Au (20/120/40/50 nm) ohmic metal stack, the sample underwent rapid thermal annealing (RTA) at 765 °C for 60 s in nitrogen ambient to form the alloyed Ohmic contact to the 2DEG. The fabricated Ohmic contacts exhibit high quality, as evidenced by the consistently low values of contact resistance (R_c) and sheet resistance (R_{sh}) obtained through transfer length measurement (TLM), which are approximately 0.67 Ω·mm and 243 Ω/□, respectively. The third EBL step was performed for the realization of the gate contacts for Type-II devices. For Type-I devices, after the realization of the ohmic contacts, a 120 nm thick SiN_X was deposited by plasma-enhanced chemical vapor deposition and

fin structures were formed in SiN_X through the EBL with ma-N 2403 negative resist and subsequent dry etching of SiN_X in CF_4/O_2 plasma. By using MMA(8.5)MAA-EL11/PMMA-A4 co-polymer positive resist as a mask following the pattern of the gate finger, the dry etching of the top InAlN barrier and AlN spacer layers, as well as about 90 nanometers of the GaN channel layer was done in Cl_2/Ar plasma using the MERIE. During the etching process SiN_X served as the hard mask and protected fin areas. Succeeding this step, SiN_X was dry etched to expose channel area whereas the protected SiN_X by the co-polymer positive resist in the access regions serves the purpose of surface passivation. This way fin-like structures were formed in the gate opening region without conducting an additional EBL step and as a result of this, the fins have the same length as the gate electrode. DisCharge H_2OX_2 anti-charging agent was employed to eliminate electron beam divergence from its designated path caused by the accumulation of electrons at the surface of the sample due to the existence of the insulating SiC substrate. Finally, Schottky gate-stack of Ni/Au (20/20 nm) was evaporated followed by the standard lift-off process in acetone using ultrasonic bath.

The process flow for the fabrication of Type-I HFETs is illustrated in Fig. 3.2 and Type-II HFETs is illustrated in Fig. 3.3.



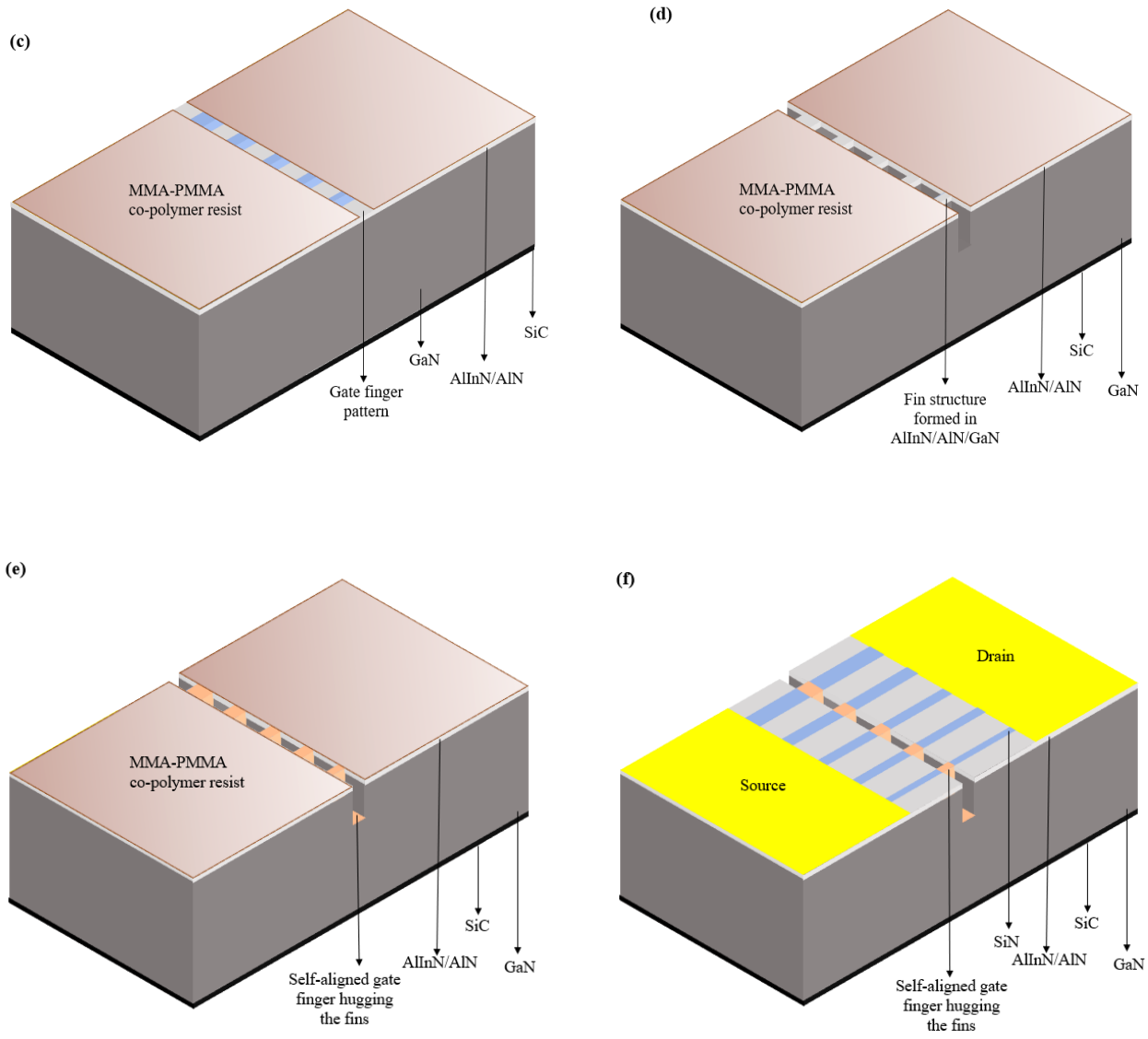


Figure 3.2 Fabrication process of the Type-I HFETs. (a) Mesa isolation and ohmic contact formation, (b) SiN deposition and fin structures pattering in SiN with EBL and dry etching using CF_4/O_2 plasma, (c) gate finger pattering using MMA-PMMA co-polymer photoresist, (d) barrier layer and GaN channel layer dry etching in Cl_2/Ar plasma following etching of SiN, (e) gate metal deposition, (f) final device structure post lift-off of the co-polymer resist.

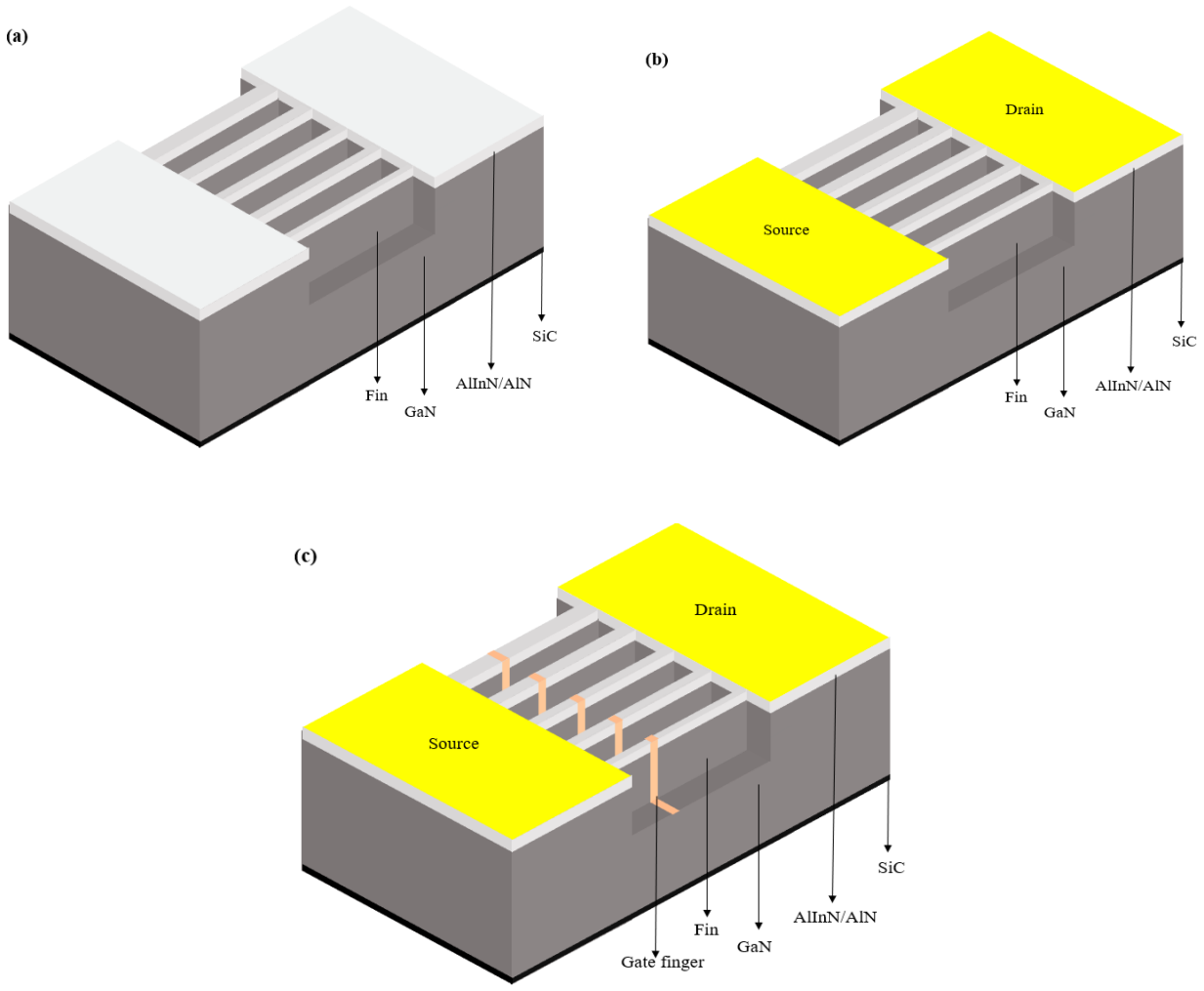


Figure 3.3 Fabrication process of the Type-II HFETs. (a) Mesa isolation, (b) Ohmic contact formation, and (c) final device structure.

Evidently, the remaining SiN_X in the access regions only provides surface passivation to the parts of the access region aligned with the gated fins of the Type-I devices. Such a manner of implementation allows a simpler way of implementing the needed small fins.

The devices studied in this chapter are composed of five fin structures with widths of 400, 900, 1300, 1700, and 2000 nm, along the gate width direction, in order to operate the fins

sequentially for achieving a more linear and broader G_m-V_{GS} characteristics [48]. According to the given dimensions, the fabricated devices have overall gate width of 6.3 µm with unless reported otherwise.

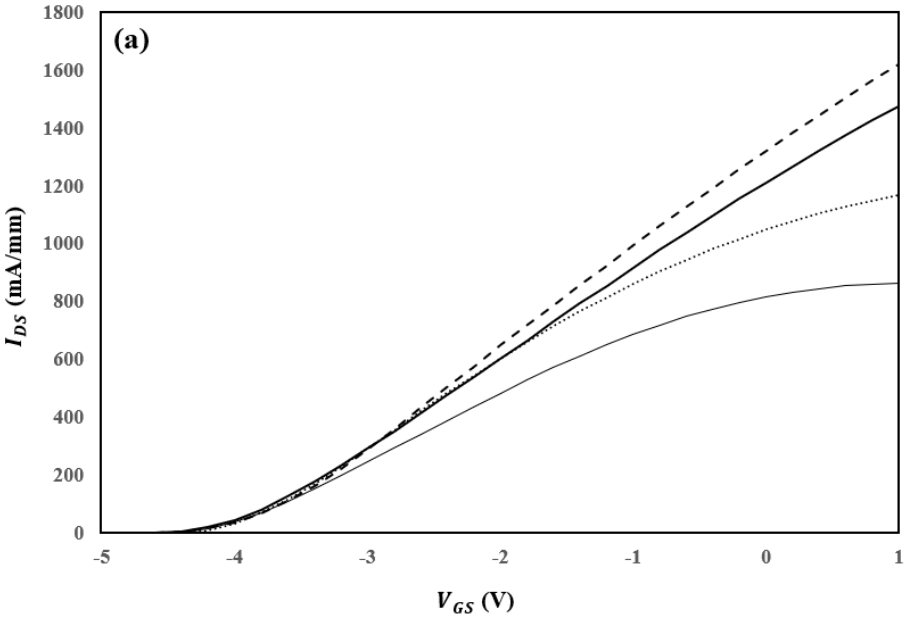
Following the deposition of contact pads, Keithley 4200-SCS semiconductor characterization system was used for room-temperature on-chip characterization of the fabricated HFETs.

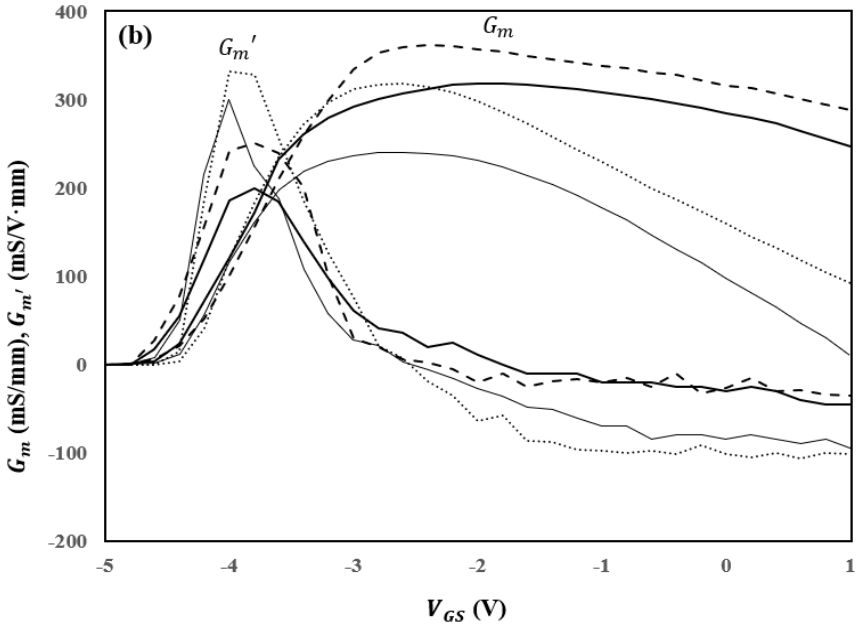
3.3 Results and discussion

3.3.1 Experimental results

3.3.1.1 Influence of L_{GS} scaling

Fig. 3.4 shows the comparison of the normalized transfer characteristics, gate-transconductance, and output characteristics for the HFETs depicted in Fig. 3.1 having L_{GS} of 1.5 µm and 3 µm, while retaining the same L_G = 0.5 µm, L_{GD} = 5µm, and gate width (W_G) = 6.3 µm.


(a)
1800
1600
1400
1200
1000
800
600
400
200
0
-5
-4
-3
-2
-1
0
1
I_{DS} (mA/mm)
V_{GS} (V)


(b)
G_m
G_m'
400
300
200
100
0
-100
-200
-5
-4
-3
-2
-1
0
1
G_m (mS/mm), G_m' (mS/V·mm)
V_{GS} (V)

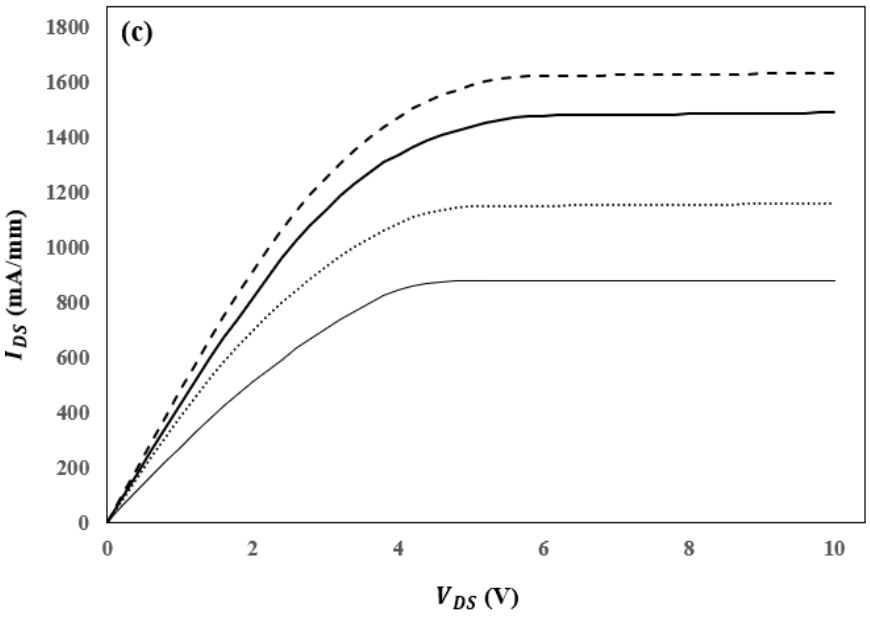


Figure 3.4 (a) Normalized transfer characteristics, (b) gate-transconductance (G_m) and its first derivatives (G_m') at V_{DS} = 6 V, and (c) output characteristics at V_{GS} = 1 V of the fabricated Type-I HFETs having L_{GS} = 1.5 μm (dashed line) and L_{GS} = 3 μm (thick solid line) and Type-II HFETs having L_{GS} = 1.5 μm (dotted line) and L_{GS} = 3 μm (thin solid line) for fixed L_G = 0.5 μm, W_G = 6.3 μm, and L_{GD} = 5 μm.

Tested among a large number of devices, consistently the threshold voltage of all the devices with the aforementioned L_{GS} is around – 4 V. By downscaling the L_{GS} from 3 μm to 1.5 μm, for the devices represented in Fig. 3.4, the values of maximum drain-current density and gate-transconductance are observed to increase from 1490 mA/mm and 319 mS/mm to 1632 mA/mm and 362 mS/mm, respectively for Type-I HFETs and 880 mA/mm and 241 mS/mm to 1159 mA/mm and 318 mS/mm, respectively for Type-II HFETs.

As shown in Figure 3.5, while all devices demonstrating a low level of gate leakage, the gate leakage is slightly higher in the Type-I devices in comparison with the Type-II devices. This might be a result of the damage induced by the plasma etching employed to etch SiN_X to expose channel area prior to the deposition of gate metal stack. Meanwhile, almost similar gate-leakage

current is observed among HFETs having different L_{GS}.

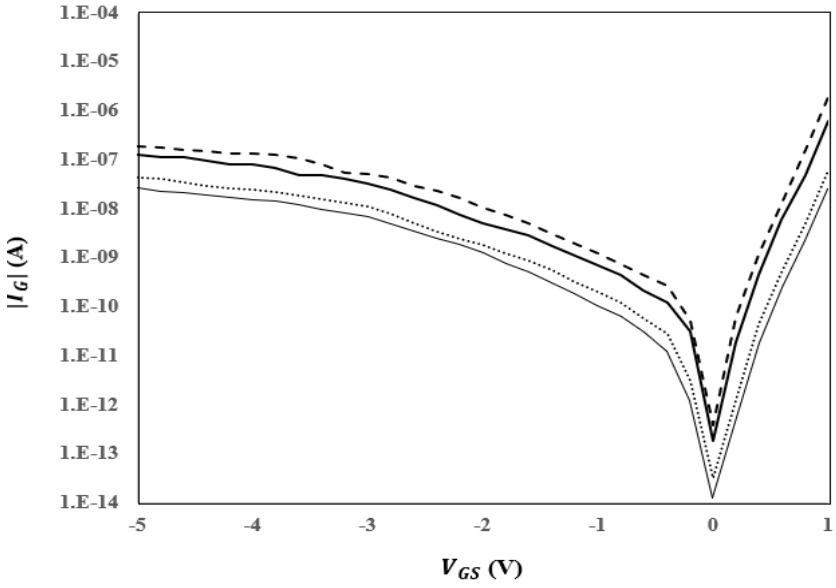


Figure 3.5 Log-scale gate current vs gate-source voltage of the fabricated Type-I HFETs having L_{GS} = 1.5 μm (dashed line) and L_{GS} = 3 μm (thick solid line) and Type-II HFETs having L_{GS} = 1.5 μm (dotted line) and L_{GS} = 3 μm (thin solid line) for fixed L_G = 0.5 μm, W_G = 6.3 μm, and L_{GD} = 5 μm at V_{DS} = 0 V.

The figure of merit of gate voltage swing (GVS) can be used to quantitively assess the linearity performance of various types of devices. The reported values of GVS are not limited by the applied gate bias unless reported otherwise. The GVS of the Type-I HFETs is observed to vary from 4 V (for L_{GS} = 1.5 μm) to 4.5 V (for L_{GS} = 3 μm), and from 2 V (for L_{GS} = 1.5 μm) to 2.4 V (for L_{GS} = 3 μm) for the Type-II HFETs. Whereas, resistance of the gate-source access region serving as a negative feedback loop is expected to have a positive impact on the device linearity in common source measurement configuration, if not of a constant value its dynamic variation affects the overall linearity of the device negatively [65].

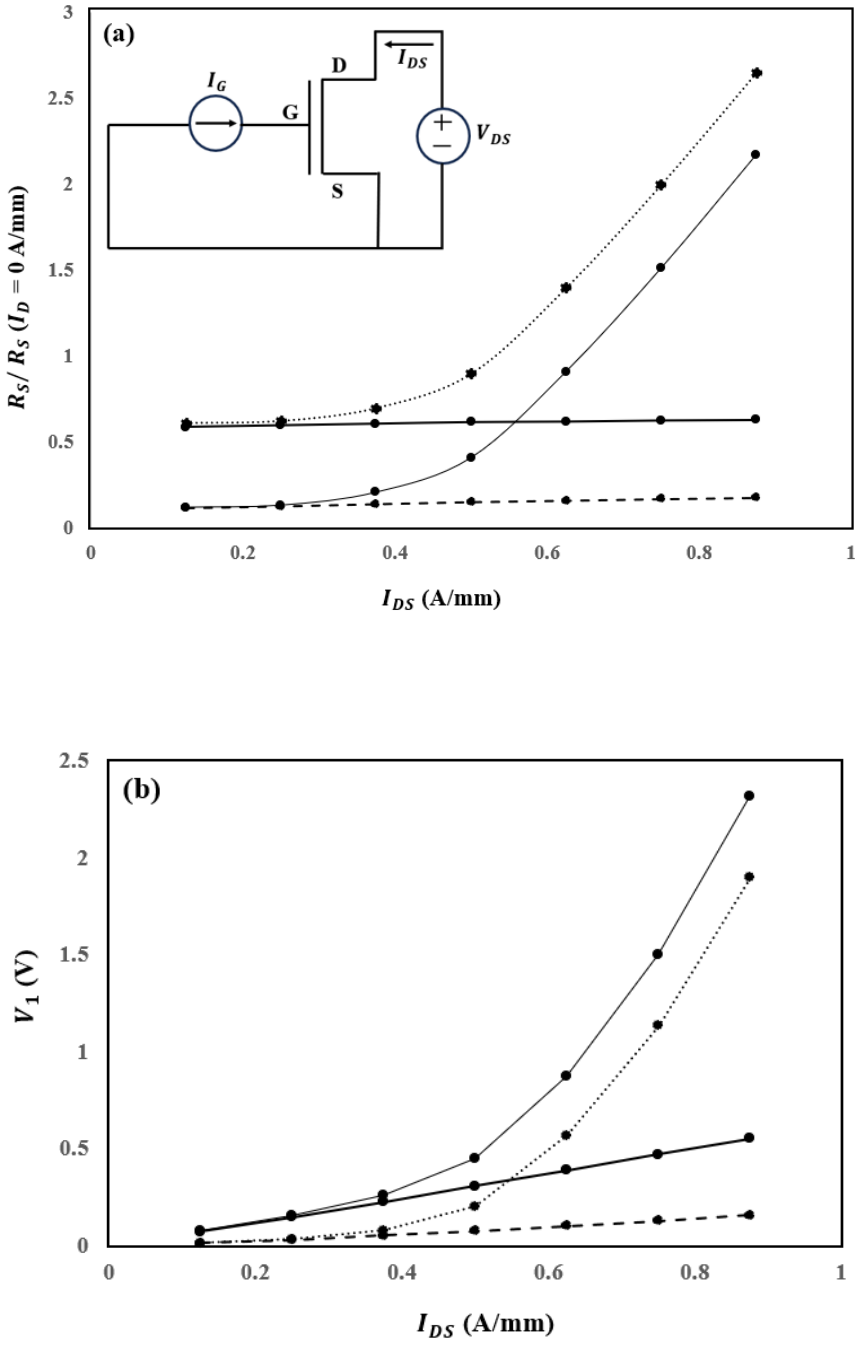


Figure 3.6 (a) Source access resistance and (b) potential drop in the source access region as a function of drain current density in the fabricated Type-I HFETs having L_{GS} = 1.5 µm (dashed line) and L_{GS} = 3 µm (thick solid line) and Type-II HFETs having L_{GS} = 1.5 µm (dotted line) and L_{GS} = 3 µm (thin solid line) for fixed L_G = 0.5 µm, W_G = 6.3 µm, and L_{GD} = 5 µm. Inset of part (a): Measurement setup.

The dynamic source access resistance (R_S) has been measured employing gate current injection method in which the gate electrode was subjected to a constant current supply and the gate voltage was measured with an increment of the drain current (I_{DS}) [66]:

$$R_S = \frac{\partial V_G}{\partial I_{DS}}. \tag{3.1}$$

As shown in Fig. 3.6 (a), the source access resistance is almost constant in the devices having fins just under the gate, while it is increasing rapidly with the increase of the drain current density in the devices having fins stretched from source to drain. For the intrinsic device under the gate electrode, the electric field towards the drain end is high enough for the electron velocity to reach its saturation value at relatively higher drain voltages [13]. However, it is not the same situation for the source-access region because the electric field in the source-access region is not high enough and limits the electron to be in the "quasi-saturation" regime (10 kV/cm < E ≪ 100 kV/cm) [66]. This way, in GaN HFETs the nonlinear relation between electric field and electron velocity in the quasi-saturation limits the current supply to the intrinsic device, hence, the source access resistance dynamically increases with the increase of the drain current density.

As shown in Fig. 3.6 (b), potential drop across the source access region ($V_1 = R_S \times I_{DS}$) is comparatively lower even at high drain currents in Type-I HFETs, facilitating higher gate overdrive ($V_{OV} = V_{GS} – V_T – V_1$) compared to Type-II devices. Hence the channel charge density in Type-I HFETs, unlike the Type-II, can respond more strongly to an extrinsic gate bias. As a result of which, these devices are showing higher drain current density and gate-transconductance values compared to Type-II HFETs. The broader extrinsic gate-transconductance profiles and their smaller first derivatives (i.e., $G_m{}'$) for Type-I HFETs are indications of the improved device linearity performance compared to Type-II HFETs. This is because the planar source access region is offering larger current drive, as a result of which the suppression of a dynamic increase of the

source-access resistance is attainable.

In order to assess the impact of L_{GS} scaling on the on-state breakdown voltage, drain current-voltage (I_{DS}-V_{DS}) characteristics of the studied devices are explored at V_{GS} = -1 V (as shown in Fig. 3.7). In this study, on-state breakdown voltage (BV_{on}) refers to the drain voltage at which the drain current increases exponentially. The on-state breakdown voltage of the Type-I HFETs is observed to vary from 74 V to 60 V and from 115 V to 99 V for the Type-II HFETs by scaling down the L_{GS} from 3 μm to 1.5 μm. No exponential increase in the gate-current (as shown in Fig. 3.7) or physical damage to the gate electrode was observed during the measurement, which provided evidence of channel and not barrier breakdown. In these measurements, if the studied devices are experiencing breakdown, then the peak of the electric field at the drain edge of the gate and present concentration of the electrons in this high-field region are the two main controlling factors. Since the peak of the electric field at the drain edge of the gate is not expected to have been substantially affected by the scaling of the gate-source spacing, we speculate that the reason behind the lower breakdown voltage of the devices having shorter L_{GS} is the presence of the higher carrier density in the proximity of the high-field velocity saturation region (i.e., drain edge of the gate).

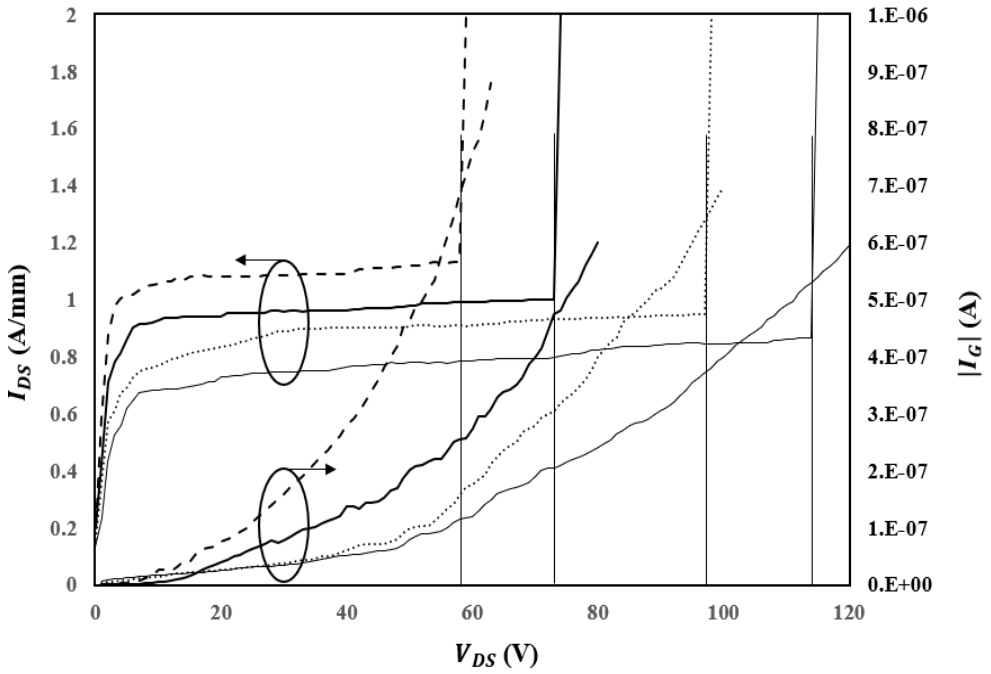


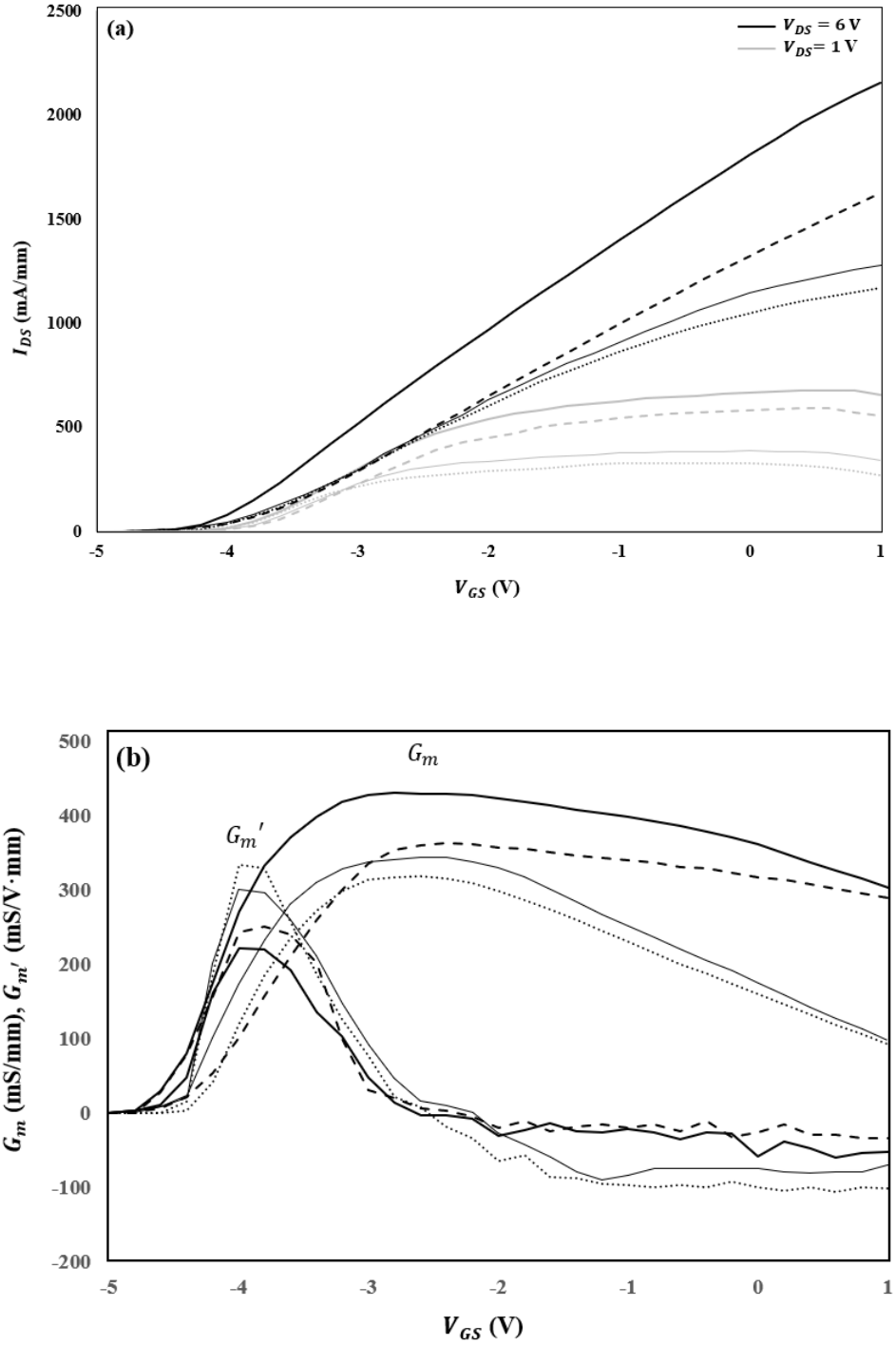
Figure 3.7 I_{DS}-V_{DS} and I_G-V_{DS} at V_{GS} = -1 V of the fabricated Type-I HFETs having L_{GS} = 1.5 µm (dashed line) and L_{GS} = 3 µm (thick solid line) and Type-II HFETs having L_{GS} = 1.5 µm (dotted line) and L_{GS} = 3 µm (thin solid line) for fixed L_G = 0.5 µm, W_G = 6.3 µm, and L_{GD} = 5 µm.

Following an earlier work of the group [67], we speculate that the enhancement of the on-state breakdown voltages of Type-II HFETs is a result of the higher resistance inflicted on the drain access region due to its smaller width compared to the much wider drain access region of Type-I HFETs. The higher drain access resistance redistributes the drain-induced electric field along the gated-channel in a way that the peak of the electric field at the drain edge of the gate is significantly reduced and as result of which the channel breakdown is triggered at higher V_{DS}.

3.3.1.2 Influence of L_G scaling

Fig. 3.8 shows the comparison of the normalized transfer characteristics, gate

transconductance, and output characteristics for HFETs depicted in Fig. 3.1 having L_G of 0.25 µm and 0.5 µm, while retaining the fixed L_{GS} of 1.5 µm and L_{GD} of 5 µm, and W_G of 6.3 µm.



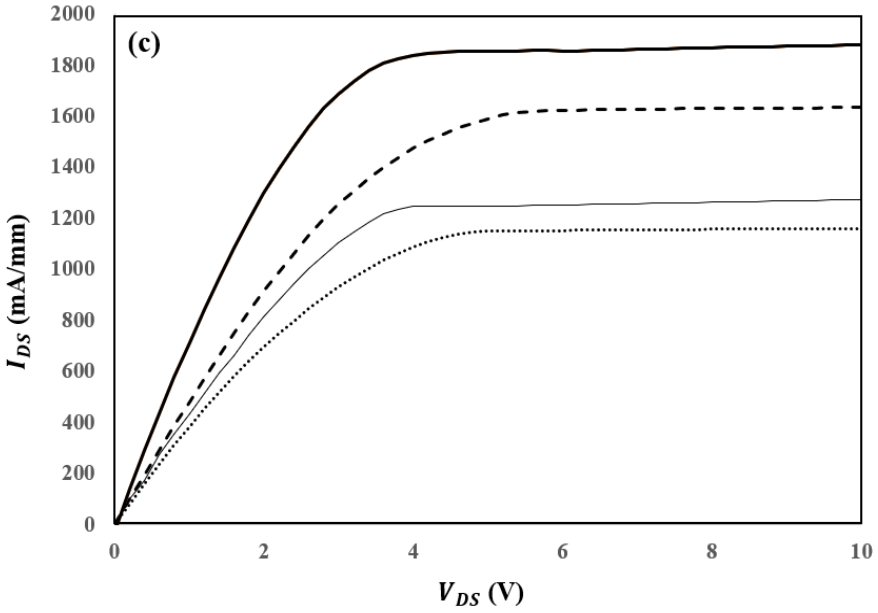


Figure 3.8 (a) Normalized transfer characteristics, (b) gate-transconductance (G_m) and its first derivatives (G_m') at V_{DS} = 6 V, and (c) output characteristics at $V_{GS,Eff}$ = 5 V of the fabricated Type-I HFETs having L_G = 0.25 μm (thick solid line) and 0.5 μm (dashed line) and Type-II HFETs having L_G = 0.25 μm (thin solid line) and 0.5 μm (dotted line) for fixed W_G = 6.3 μm, L_{GS} = 1.5 μm, and L_{GD} = 5 μm.

Tested among a large number of devices, consistently the threshold voltage of HFETs having L_G of 0.25 μm is around – 4.2 V and – 4 V for those having L_G of 0.5 μm. Appreciating the difference among the threshold voltages of the aforementioned devices, effective gate-source voltage ($V_{GS,Eff}$) defined as the difference between the applied extrinsic gate-source voltage and the threshold-voltage of each device has been employed in our analysis. Among the presented devices of Fig. 3.8, the value of maximum drain-current density at $V_{GS,Eff}$ = 5 V improves from 1632 mA/mm to 1890 mA/mm for Type-I HFETs and 1159 mA/mm to 1272 mA/mm for Type-II HFETs by downscaling the L_G from 0.5 μm to 0.25 μm. In Fig. 3.8 (b), the gate-transconductance and GVS of the Type-I HFETs are observed to increase from 362 mS/mm and 4 V to 430 mS/mm and 4.15 V, respectively and from 318 mS/mm and 2 V to 345 mS/mm and 2.1 V, respectively for

the Type-II HFETs by the same token of L_G scaling.

Yang et al. claimed that the combination of the Polar optical phonon (POP) scattering and polarization Coulomb field (PCF) scattering of the electrons in the source access region is the key reason behind the variation of R_S [68]. Accordingly, with increase of drain current, the temperatures of electrons and POP scattering start to increase, including an increase in R_S and a decrease in G_m. Meanwhile the PCF scattering becomes weaker with the increase of drain current, leading to decrease in R_S and an increase in G_m. As a result, both together determine the variation of G_m.

PCF scattering originates from the non-uniform distribution of the polarization charges at the AlGaN/GaN interface stemming from the converse piezoelectric effect in the gate region [69]. The strain variation of the AlGaN barrier layer causes the variation of the polarization charges [70]. The difference between the non-uniform and uniform distributed polarization charges is defined as the additional polarization charges ($\Delta\sigma$). The more the $\Delta\sigma$ is the stronger the PCF scattering is. The decrease of PCF scattering at higher gate voltages due to lesser additional polarization charges under the gate region can partly offset the increase of POP scattering and decease the variation of R_S and G_m [68], [70].

When the L_G is increased, the increase of the gate area makes the total number of the additional polarization charges under the gate region increased and the influence of PCF scattering on R_S will be enhanced. Based on the scattering mechanism calculation and analysis, Cui et al. reported that increasing the L_G can decrease the R_S variation due to enhanced PCF scattering, facilitating improved device linearity [71],[72].

The absence of the piezoelectric polarization in the lattice-matched HFETs realized on an epilayer consisting of a thin $In_{0.17}Al_{0.83}N$ barrier layer grown on top of an undoped GaN channel

makes this theory unapplicable to the studied device types in this chapter.

We speculate that the reason behind the broader extrinsic gate-transconductance profile and its smaller first derivatives of devices having shorter L_G is their larger exposure to the drain-induced barrier lowering (DIBL).

The DIBL effect can be measured by the lateral shift of the transfer curves in the subthreshold regime (ΔV_T) divided by the drain voltage difference (ΔV_{DS}) of the two curves. Though all studied devices are experiencing some DIBL at larger V_{DS}, its value for Type-I HFETs is varying from 38 mV/V to 60 mV/V and from 18 mV/V to 30 mV/V for Type-II HFETs by downscaling the L_G from 0.5 μm to 0.25 μm. We speculate that the presence of higher electron concentration in the gate-source access region of Type-I HFETs make them more exposed to DIBL. Also, we believe that for Type-II HFETs, granted by the reduced 2DEG concentration caused by the sidewall depletion [73] and the drop in the drain induced channel potential as a result of the higher resistance inflicted on the drain access region, they are less exposed to DIBL. Nevertheless, for the devices having shorter L_G, the chance of lowering the barrier between the source-access region and the gated-channel is much higher compared to the devices having longer L_G. This aids with a noticeable supply of the carriers from the source-access region to the gated-channel and as a result the suppression of the increasing source-access resistance at higher drain currents (as shown in Fig. 3.9) offers the improved linearity performance of the devices having shorter L_G.

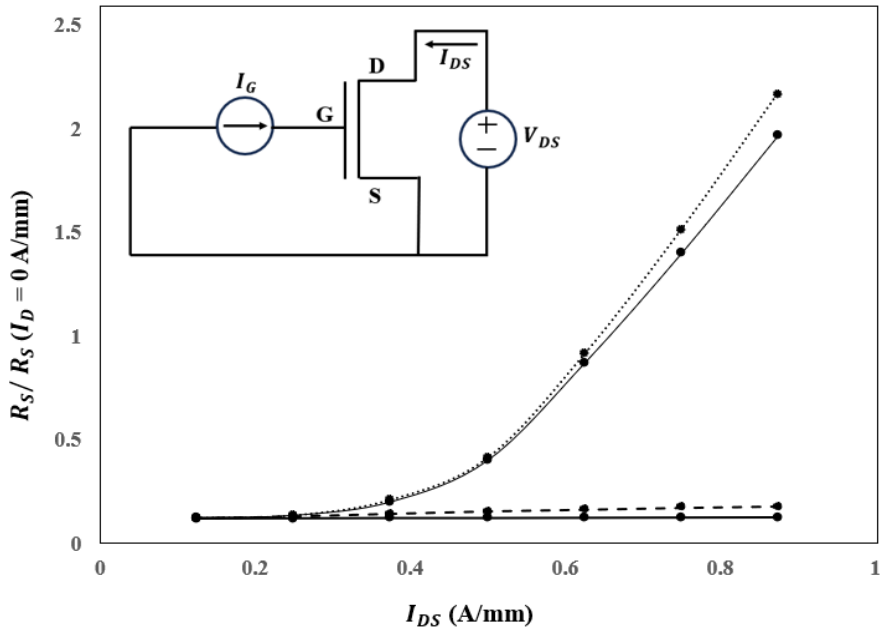


Figure 3.9 Source access resistance as a function of drain current density in the fabricated Type-I HFETs having L_G = 0.25 μm (thick solid line) and L_G = 0.5 μm (dashed line) and Type-II HFETs having L_G = 0.25 μm (thin solid line) and L_G = 0.5 μm (dotted line) for fixed W_G = 6.3 μm, L_{GS} = 1.5 μm, and L_{GD} = 5 μm. Inset: Measurement setup.

As shown in Fig. 3.10, the gate-leakage current increases as the gate length increases. When evaluating the gate-leakage of III-N HFETs, different leakage paths should be taken into account. The gate-leakage current is summation of the Trap-Assisted Tunneling (I_{TAT}), Poole-Frenkel (I_{PF}) and Fowler-Nordheim (I_{FN}) components [74-78]. The length of the gate can affect I_{TAT} and I_{PF}, but I_{FN} remains unaffected because it is concentrated near the gate edges [79].

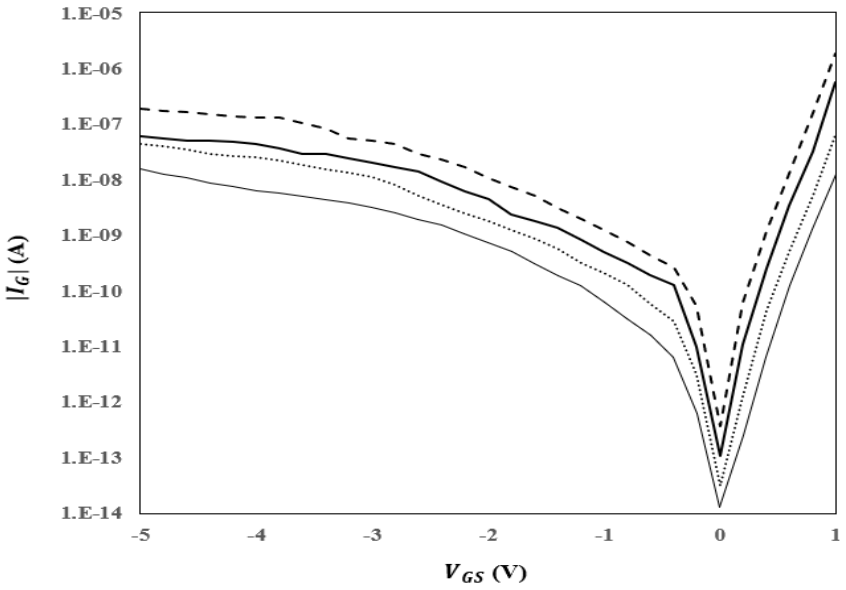


Figure 3.10 Log-scale gate current vs gate-source voltage of the fabricated Type-I HFETs having L_G = 0.25 μm (thick solid line) and 0.5 μm (dashed line) and Type-II HFETs having L_G = 0.25 μm (thin solid line) and 0.5 μm (dotted line) for fixed W_G = 6.3 μm, L_{GS} = 1.5 μm, and L_{GD} = 5 μm at V_{DS} = 0 V.

In order to assess the impact of the scaling of L_G on the device on-state breakdown characteristics, drain current-voltage (I_{DS} -V_{DS}) characteristics of the studied devices are explored at $V_{GS,Eff}$ = 3 V (as shown in Fig. 3.11). The on-state breakdown voltage of the Type-I HFETs is observed to vary from 38 V (for L_G = 0.25 μm) to 60 V (for L_G = 0.5 μm) and from 85 V (for L_G = 0.25 μm) to 99 V (for L_G = 0.5 μm) for Type-II HFETs. No exponential increase in the gate-current (as shown in Fig. 3.11) or physical damage to the gate electrode was observed during the measurement, which provided evidence of channel and not barrier breakdown.

We speculate that the reason behind the lower BV_{on} of devices having shorter L_G is their larger exposure to the drain-induced barrier lowering (DIBL) in addition to a larger peak electric field at the drain edge of the gate. The DIBL effect can be measured by the lateral shift of the transfer curves in the subthreshold regime (ΔV_T) divided by the drain voltage difference (ΔV_{DS}) of

the two curves. Though all studied devices are experiencing some DIBL at larger V_{DS}, its value for Type-I HFETs is varying from 38 mV/V to 60 mV/V and from 18 mV/V to 30 mV/V for Type-II HFETs by downscaling the L_G from 0.5 µm to 0.25 µm.

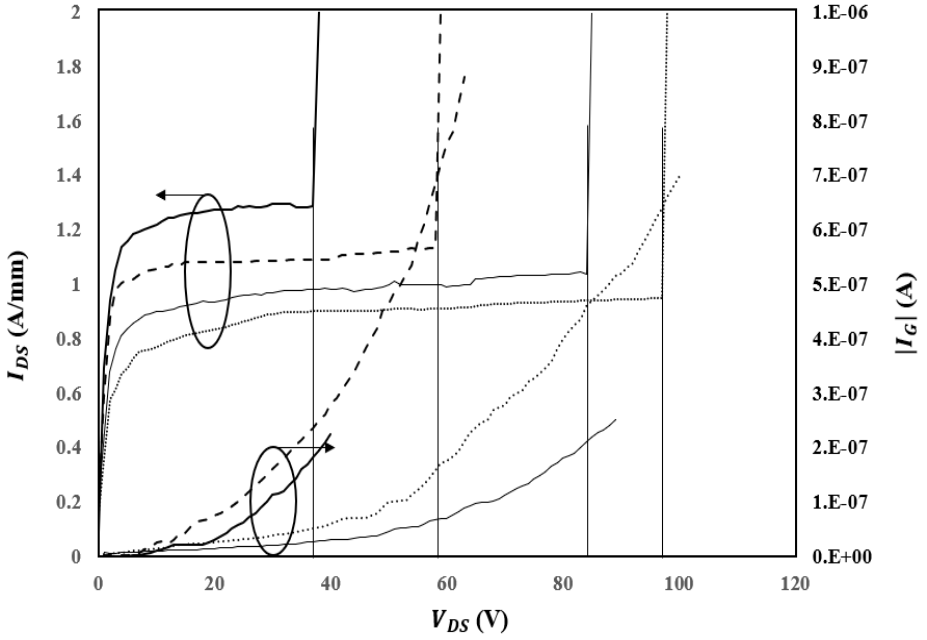


Fig. 3.11 I_{DS}-V_{DS} and I_G-V_{DS} at $V_{GS,Eff}$ = 3 V of the fabricated Type-I HFETs having L_G of 0.25 µm (thick solid line) and 0.5 µm (dashed line) and Type-II HFETs having L_G = 0.25 µm (thin solid line) and 0.5 µm (dotted line) for fixed W_G = 6.3 µm, L_{GS} = 1.5 µm, and L_{GD} = 5 µm.

For the devices having shorter L_G, a noticeable supply of the charge carriers from the source-access region to the gated-channel takes place due to the higher probability of lowering the barrier between the source-access region and the gated-channel. In addition to the stronger peak electric-field at the drain edge of the gate, the presence of higher concentration of electrons in the proximity of the high-field region for devices having shorter L_G inflicts the breakdown at relatively lower drain-source voltages.

3.3.2 Simulation results

3.3.2.1 Influence of L_{GS} and L_G scaling on DC characteristics

To comprehend the reasons behind the observed increment of the maximum drain-current density and peak gate-transconductance values with the downscaling of the L_{GS} and L_G, device simulations using COMSOL Multiphysics [80] were conducted to estimate longitudinal electric field profile and electron velocity along the channel. The 9 nm thick $In_{0.17}Al_{0.83}N$ barrier layer and 1.7 µm thick GaN channel layer were considered UID to the level of 1×10^{14} cm^{-3}. Source and drain contacts were assumed as ideally Ohmic, whereas the gate was defined as Schottky contact with metal work function of 5.2 eV. The sheet charge density of 0.035 C/m^2 (for In mole fraction equal to 0.17 in the $In_xAl_{1-x}N$ barrier) has been added to induce polar-induced 2DEG concentration of 2.1×10^{13} cm^{-2} at the InAlN/GaN interface. The simulated planar devices are having varying L_{GS} (for fixed L_G of 0.5 µm and L_{GD} of 5 µm) and L_G (for fixed L_{GS} of 1.5 µm and L_{GD} of 5 µm).

Reference lattice temperature (T_0) has been set to 300 K for all three simulations. Electrons and holes drift/diffusion current densities and electrical potential have been calculated using the following equations:

$$J_n = qn\mu_n\nabla E_c + \mu_n K_B T\nabla n + qnD_{n,th}\nabla\ln(T) \quad (3.2)$$

$$J_p = qp\mu_p\nabla E_v - \mu_p K_B T\nabla p - qpD_{p,th}\nabla\ln(T) \quad (3.3)$$

$$E_c = -(qV + \chi_0) \quad (3.4)$$

$$E_v = -(qV + q\chi_0 + E_g) \quad (3.5)$$

$$\rho = q\left(p - n + N_d{}^+ - N_a{}^-\right) \quad (3.6)$$

The material properties of $In_{0.17}Al_{0.83}N$ and GaN used in simulations are presented in Table 3.1 [39], where we have adopted the field-dependent mobility [$\mu_n(E)$] using the Caughey and

Thomas model [81] represented by,

$$\mu_n(E) = \frac{\mu_{n,low}}{\left(1+\frac{\mu_{n,low}\times|E_x|}{v_{n,sat}}\right)} \quad . \tag{3.7}$$

where $\mu_{n,low}$ is the low-field electron mobility, E_x is the longitudinal electric field, and $v_{n,sat}$ is the electron saturation velocity.

To study the on-state breakdown behavior, we have incorporated the effect of impact ionization using the following equations:

$$\alpha = 4.48 \times 10^8 \, exp\left(-\frac{3.39 \times 10^7}{|E_x|}\right) \tag{3.8}$$

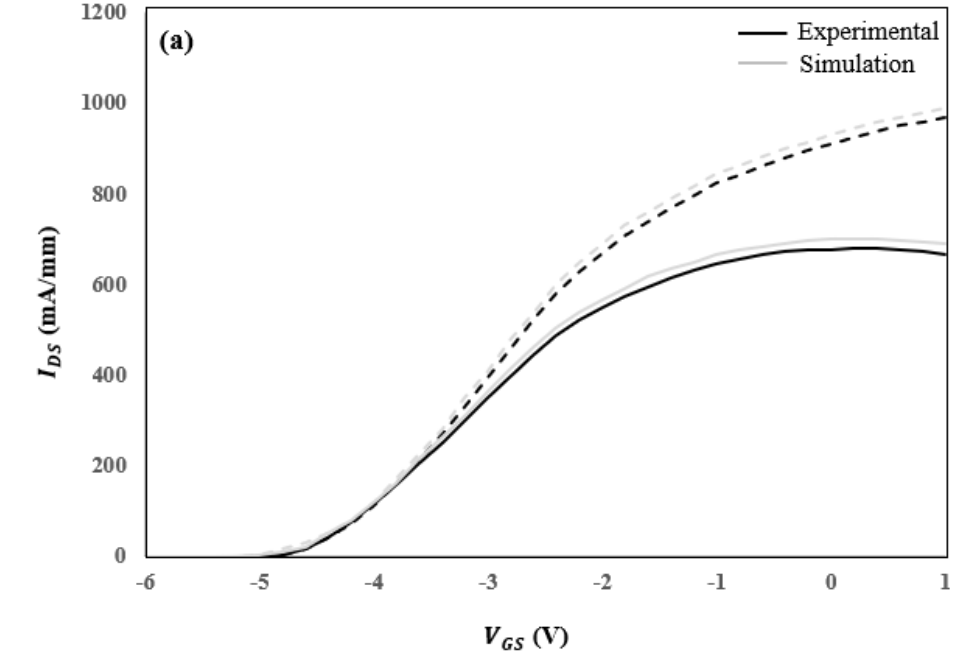
$$\beta = 7.13 \times 10^6 \, exp\left(-\frac{1.46 \times 10^7}{|E_x|}\right) \tag{3.9}$$

in which α represents the electron and β represents the hole ionization rates [82].

Table 3.1 Material properties of $In_{0.17}Al_{0.83}N$ and GaN used in the simulation.

Parameter	Value ($In_{0.17}Al_{0.83}N$)	Value (GaN)
Static relative permittivity (ϵ_r)	6.16	8.9
Bandgap (E_g)	4.62 (eV)	3.39 (eV)
Electron affinity (χ_0)	1.484 (eV)	4.1 (eV)
Effective density of states, valance band (N_{vo})	2.23×10^{19} cm^{-3}	4.6×10^{18} cm^{-3}
Effective density of states, conduction band (N_{co})	4.6×10^{18} cm^{-3}	2.3×10^{18} cm^{-3}
Low-field electron mobility (μ_n)	800 ($cm^2/V{\cdot}s$)	1000 ($cm^2/V{\cdot}s$)
Low-field hole mobility (μ_p)	82 ($cm^2/V{\cdot}s$)	200 ($cm^2/V{\cdot}s$)
Electron saturation velocity ($v_{n,sat}$)	1.1×10^{17} (cm/s)	1.5×10^{17} (cm/s)

It is observed that the obtained output characteristics are closely following the experimental data, which validates the performed simulations (as shown in Fig. 3.12 and 3.13).



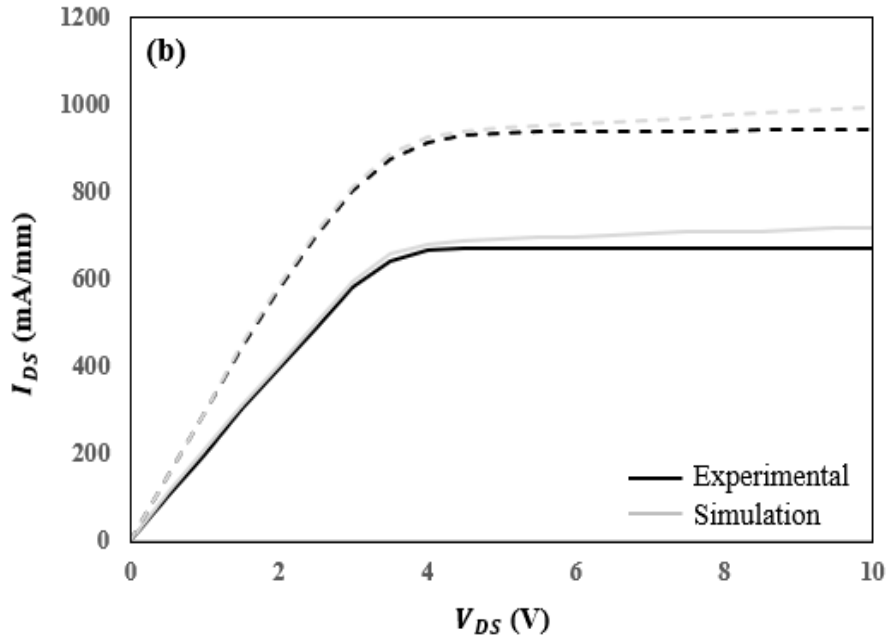


Figure 3.12 (a) Normalized transfer characteristics at V_{DS} = 6 V and (b) output characteristics at V_{GS} = 1 V of the planar devices having L_{GS} = 1.5 μm (dashed line) and L_{GS} = 3 μm (solid line) for fixed L_G = 0.5 μm and L_{GD} = 5 μm.

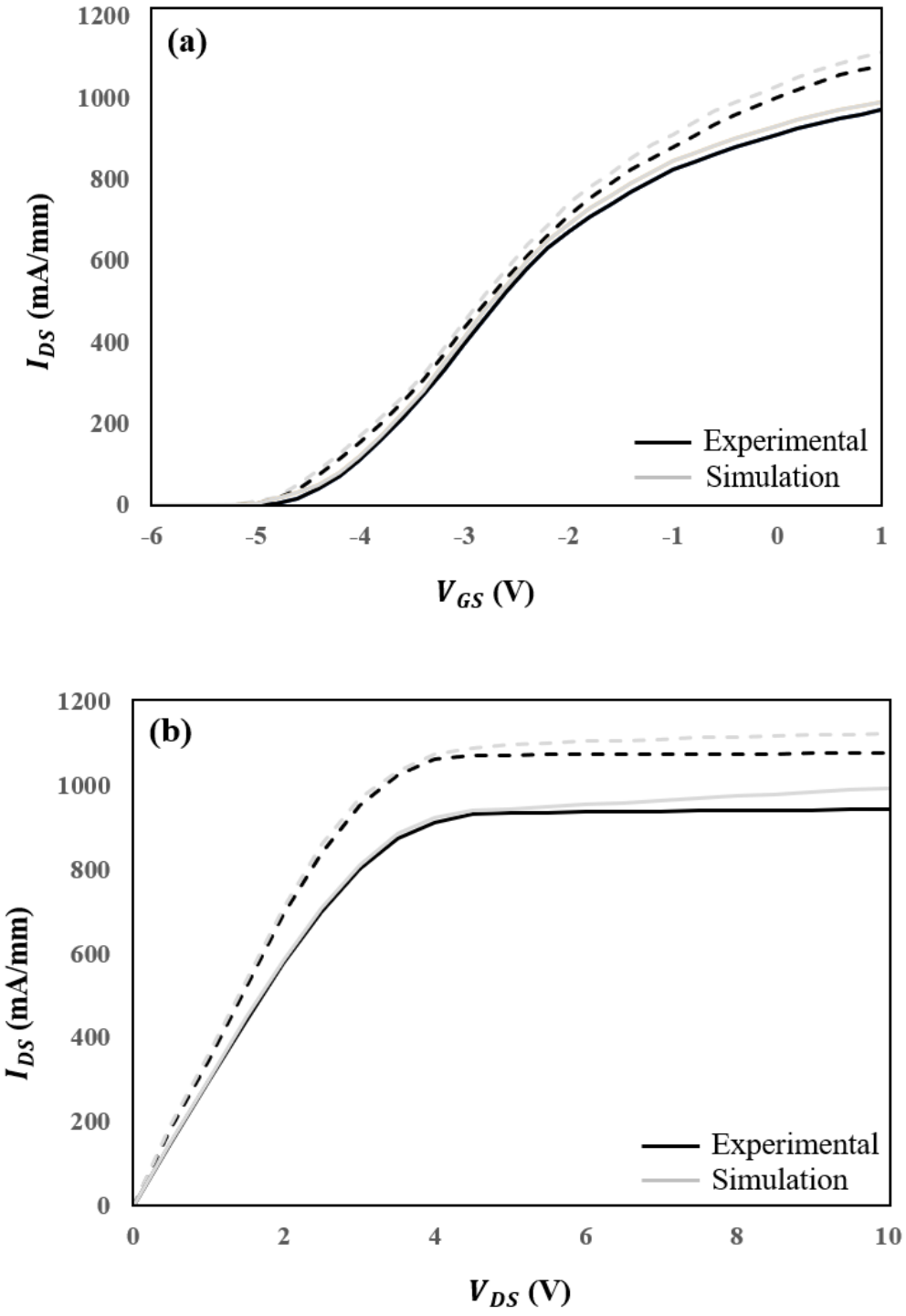
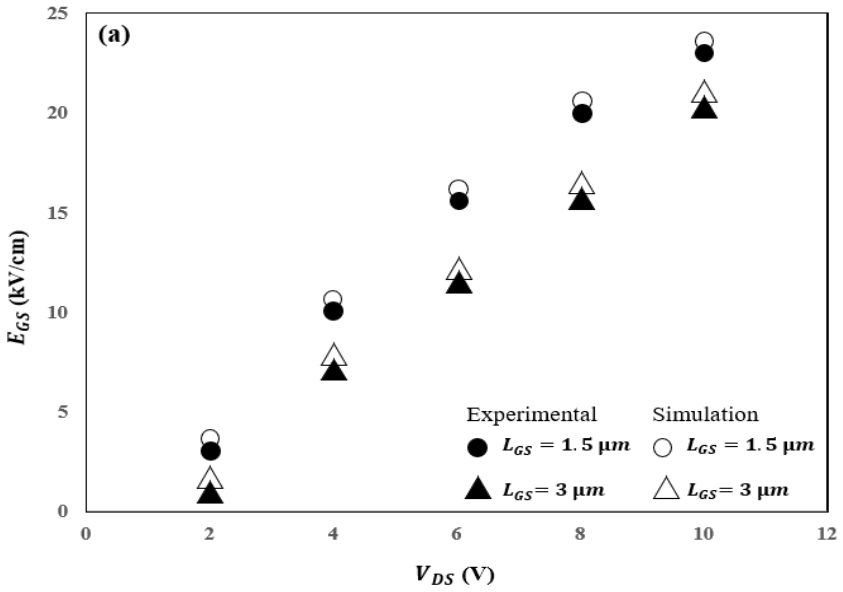


Figure 3.13 (a) Normalized transfer characteristics at V_{DS} = 6 V and (b) output characteristics at $V_{GS,Eff}$ = 5 V of the planar devices having L_G = 0.25 µm (dashed line) and L_G = 0.5 µm (solid line) for fixed L_{GS} = 1.5 µm and L_{GD} = 5 µm.

Electric-field along the source-access region (E_{GS}) is given by,

$$E_{GS} = \frac{V_1}{L_{GS}} . \tag{3.3}$$

The potential drop across the source-access region has been calculated from the measured source access resistance values for the fabricated planar HFETs having varying L_{GS} and L_G employing gate current injection method. Fig. 3.14 shows the comparison of simulated E_{GS} alongside experimental E_{GS} for all the variation of L_{GS} and L_G. It is observed that the simulated values follow the experimental values very closely. This validation is taken as a reassurance for the accuracy of the calculated electric field profile across the channel.



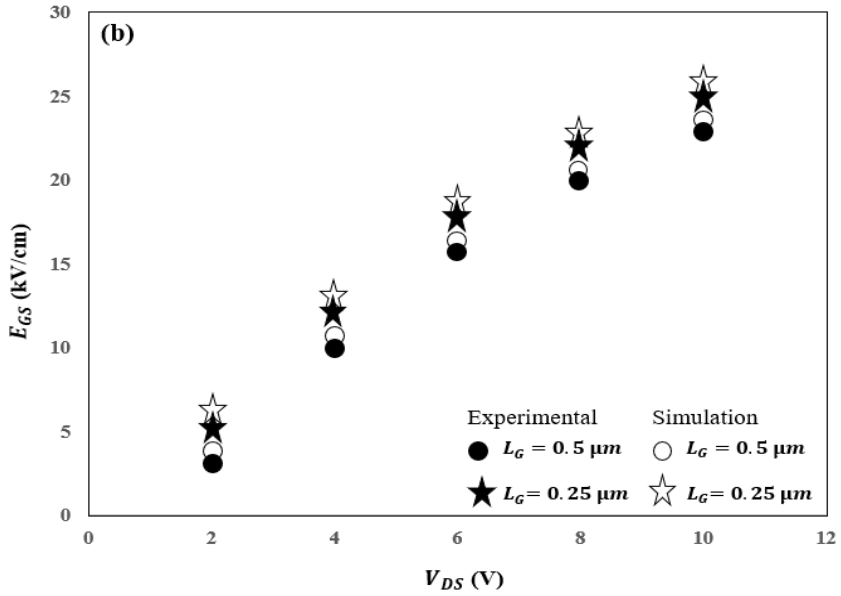


Figure 3.14 The magnitude of electric-field along the source-access region for planar devices having (a) L_{GS} of 1.5 µm and 3 µm for fixed L_G of 0.5 µm and L_{GD} of 5 µm at V_{GS} = 1 V and (b) L_G of 0.25 µm and 0.5 µm for fixed L_{GS} of 1.5 µm and L_{GD} of 5 µm at $V_{GS,Eff}$ = 5 V.

As shown in Fig. 3.15 at V_{GS} = 1 V and V_{DS} = 6 V, the magnitude of electric-field along the source-access region is observed to increase from 12 kV/cm to 16 kV/cm with the downscaling of L_{GS} from 3 µm to 1.5 µm, which in turn increase the carrier velocity in the aforementioned region. There are two possible reasons for the observed field reversal at the source-edge of the gate: (1) large charge gradient and (2) large change in the potential [83]. Due to current conservation, the higher carrier velocity in the gate-source region for the device having a shorter L_{GS} induces a higher electron density under the gated-channel (as seen in Fig. 3.16) and as a result the maximum drain-current density increase. This way downscaling of the L_{GS} has a strong positive impact on the device DC performance.

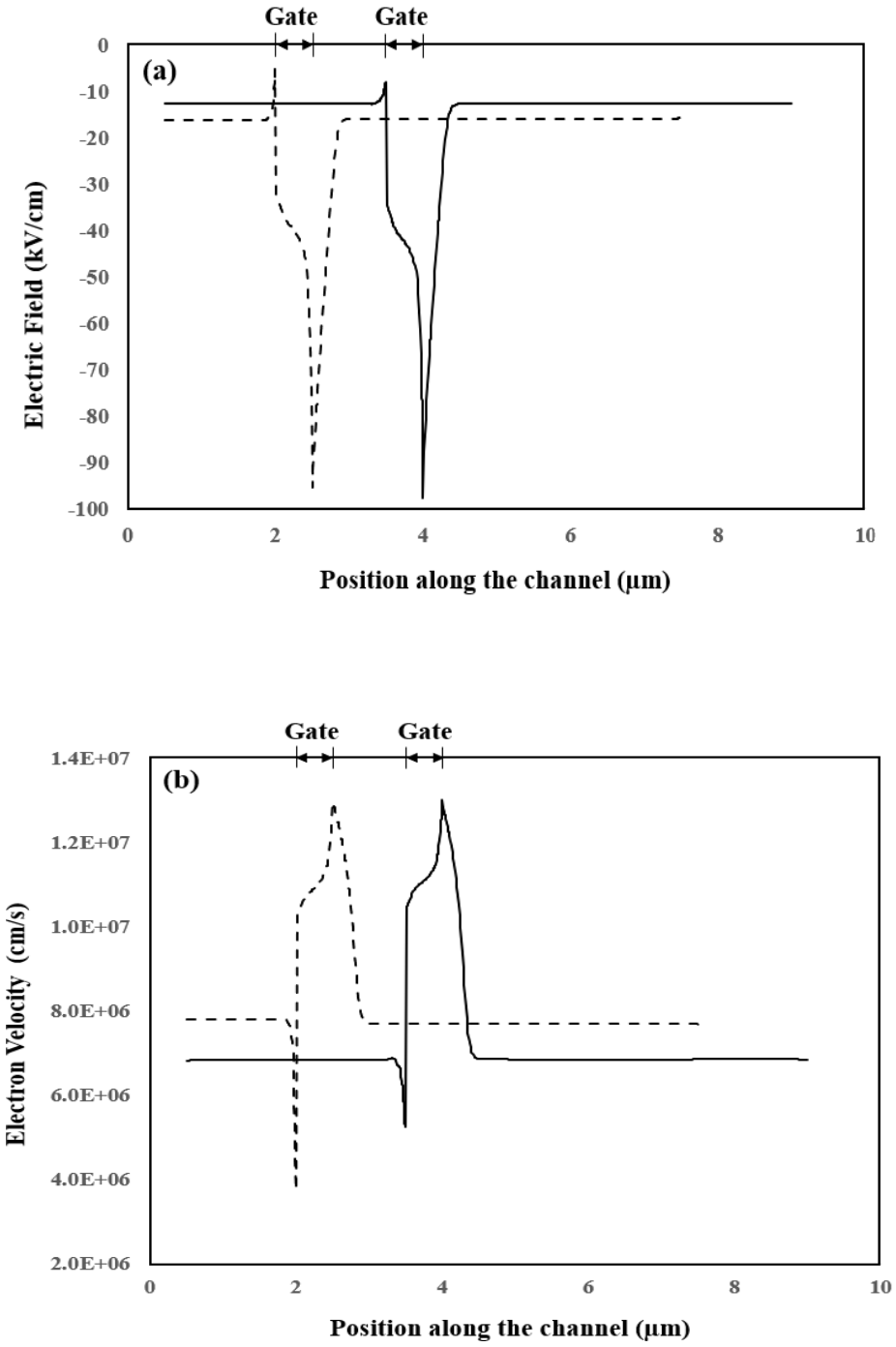


Figure 3.15 (a) Longitudinal electric field profile and (b) electron velocity along the channel and 1 nm below the heterointerface of devices having L_{GS} = 1.5 µm (dashed line) and L_{GS} = 3 µm (solid line) for fixed L_G of 0.5 µm and L_{GD} of 5 µm at V_{GS} = 1 V and V_{DS} = 6 V.

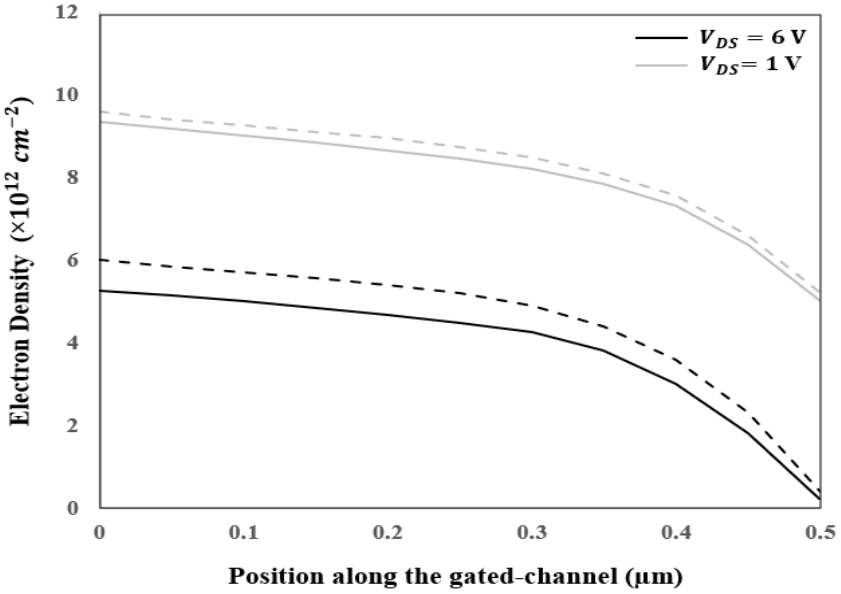
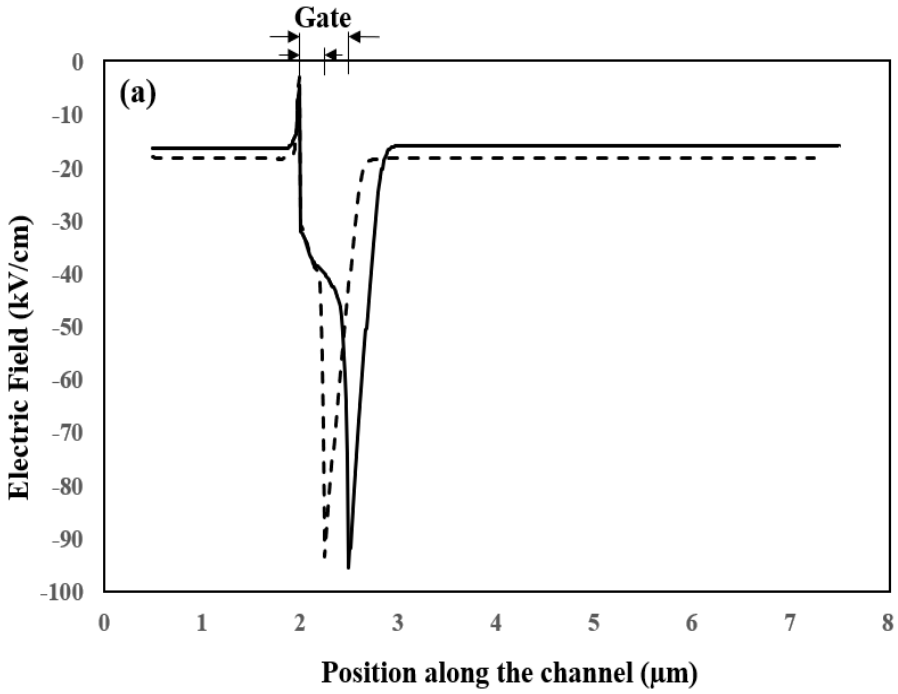


Figure 3.16 Electron density under the gated-channel and 1 nm below the heterointerface of devices having L_{GS} = 1.5 µm (dashed line) and L_{GS} = 3 µm (solid line) for fixed L_G of 0.5 µm and L_{GD} of 5 µm at V_{GS} = 1 V.

From results shown in Fig. 3.17, it can be deduced that with the downscaling of L_G from 0.5 µm to 0.25 µm, the average electric field along the gate-source access region is increasing from 16 kV/cm to 18kV/cm. In turn, this increases the electron velocity of the charge carriers in the aforementioned region and as a result the electron density under the gated-channel (as seen in Fig. 3.18). The presence of higher 2DEG concentration under the gated-channel, facilitating the enhancement of the maximum drain-current density.

The value of DIBL is varying from 30 mV/V to 50 mV/V (as seen in Fig. 3.19) by downscaling of the L_G from 0.5 µm to 0.25 µm, which substantiate the speculation presented earlier in the section about the devices having shorter L_G and their larger exposure to the DIBL.



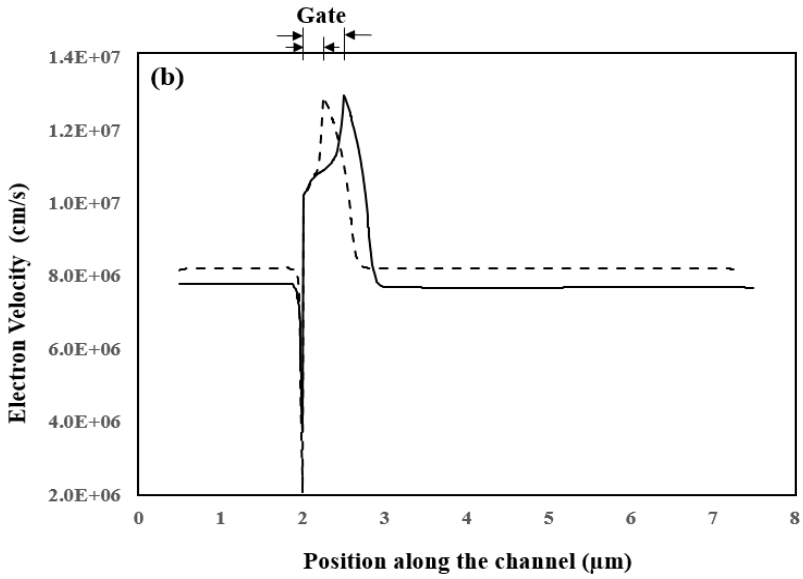


Figure 3.17 (a) Longitudinal electric field profile and (b) electron velocity along the channel and 1 nm below the heterointerface for devices with L_G = 0.25 µm (dashed line) and 0.5 µm (solid line) for fixed L_{GS} of 1.5 µm and L_{GD} of 5 µm at $V_{GS,Eff}$ = 5 V and V_{DS} = 6 V.

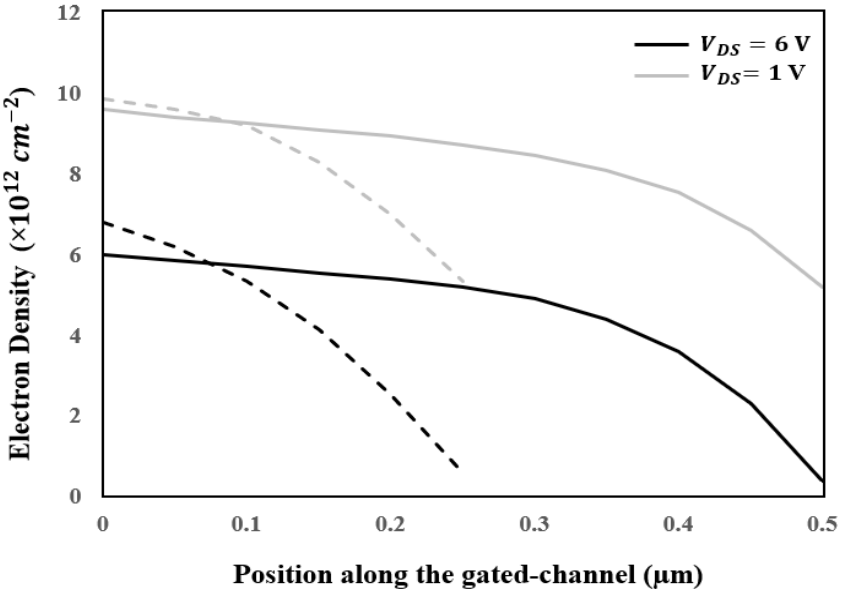


Figure 3.18 Electron density under the gated-channel and 1 nm below the heterointerface of devices having L_G = 0.25 μm (dashed line) and L_G = 0.5 μm (solid line) for fixed L_{GS} of 1.5 μm and L_{GD} of 5 μm at $V_{GS,Eff}$ = 5 V.

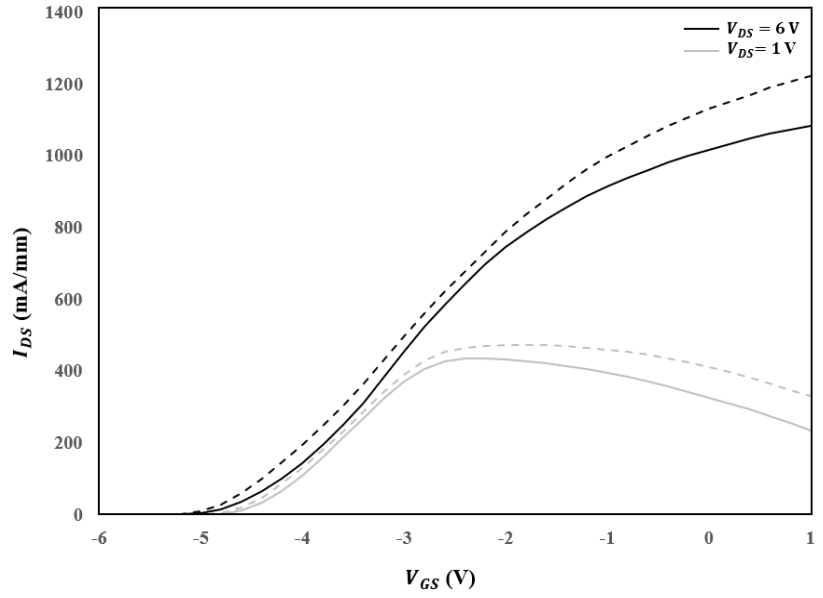
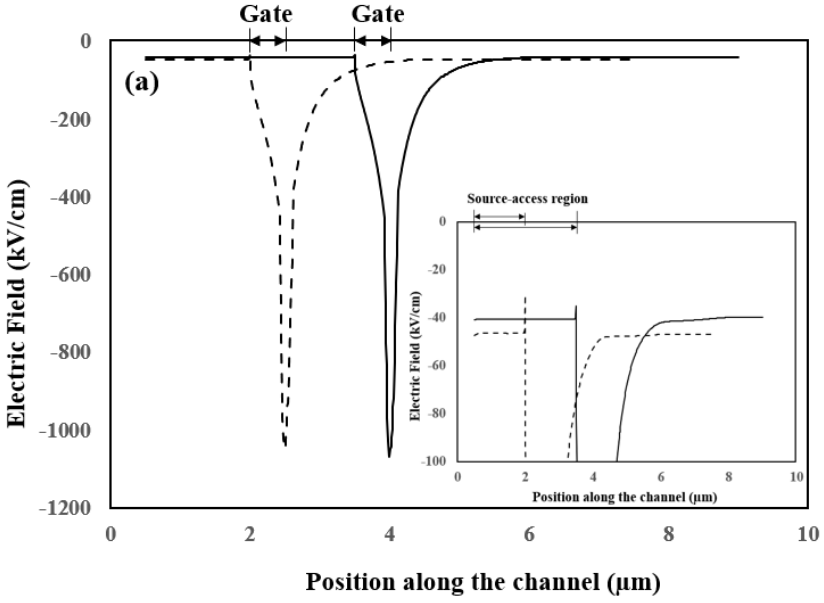


Figure 3.19 Normalized transfer characteristics of the simulated HFETs having L_G = 0.25 μm (dashed line) and 0.5 μm (solid line) for fixed L_{GS} = 1.5 μm and L_{GD} = 5 μm.

3.3.2.2 Influence of L_{GS} and L_G scaling on the on-state breakdown voltage

To comprehend the reasons behind the observed diminution of on-state breakdown voltage with the downscaling of the L_{GS} and L_G, device simulations using COMSOL Multiphysics [80] were conducted to estimate longitudinal electric field profile and electron velocity along the channel.

As shown in Fig. 3.20 at V_{GS} = -1 V and V_{DS} = 60 V, the magnitude of electric-field along the source-access region is observed to increase from 40 kV/cm to 46 kV/cm with the downscaling of L_{GS} from 3 µm to 1.5 µm, which although a small difference in turn increases the carrier velocity in the aforementioned region. There are two possible reasons for the observed field reversal at the source-edge of the gate: (1) large charge gradient and (2) large change in the potential [83]. Due to current conservation, the higher carrier velocity in the gate-source region for the device having a shorter L_{GS} induces a higher electron density in the proximity of the high-field region (as seen in Fig. 3.21) and as a result the avalanche breakdown process initiates at lower V_{DS}.



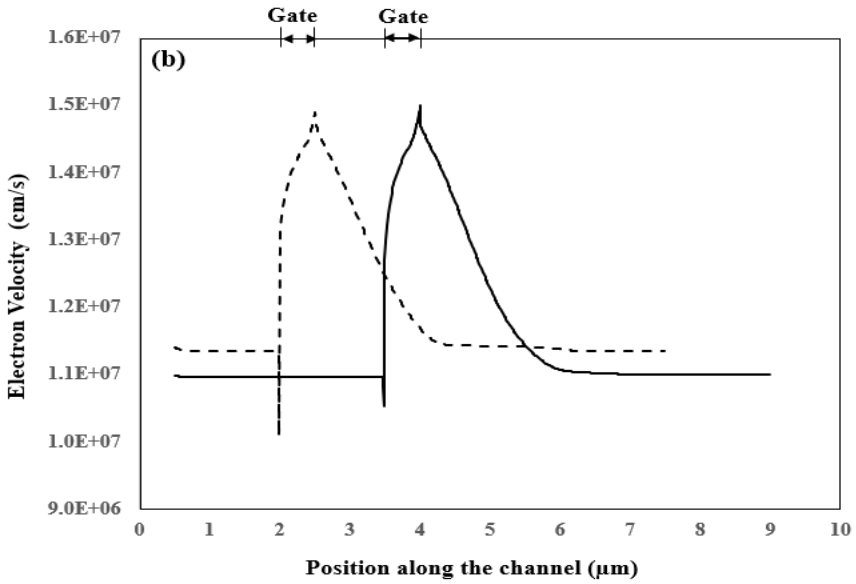


Figure 3.20 (a) Longitudinal electric field profile and (b) electron velocity along the channel and 1 nm below the heterointerface of devices having L_{GS} = 1.5 µm (dashed line) and L_{GS} = 3 µm (solid line) for fixed L_G of 0.5 µm and L_{GD} of 5 µm at V_{GS} = - 1 V and V_{DS} = 60 V. Inset of part (a): close-up of the electric field profile across the source-access region.

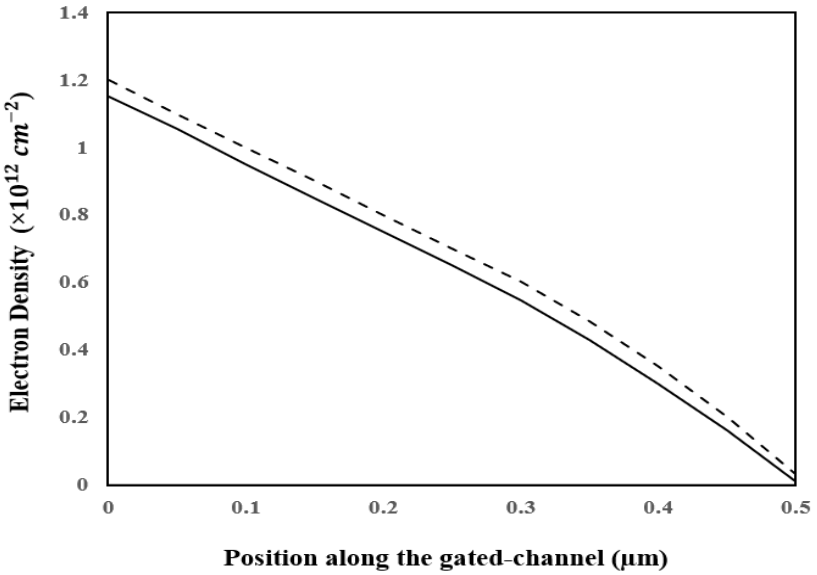


Figure 3.21 Electron density under the gated-channel and 1 nm below the heterointerface of devices having L_{GS} = 1.5 µm (dashed line) and L_{GS} = 3 µm (solid line) for fixed L_G of 0.5 µm and L_{GD} of 5 µm at V_{GS} = - 1 V and V_{DS} = 60 V.

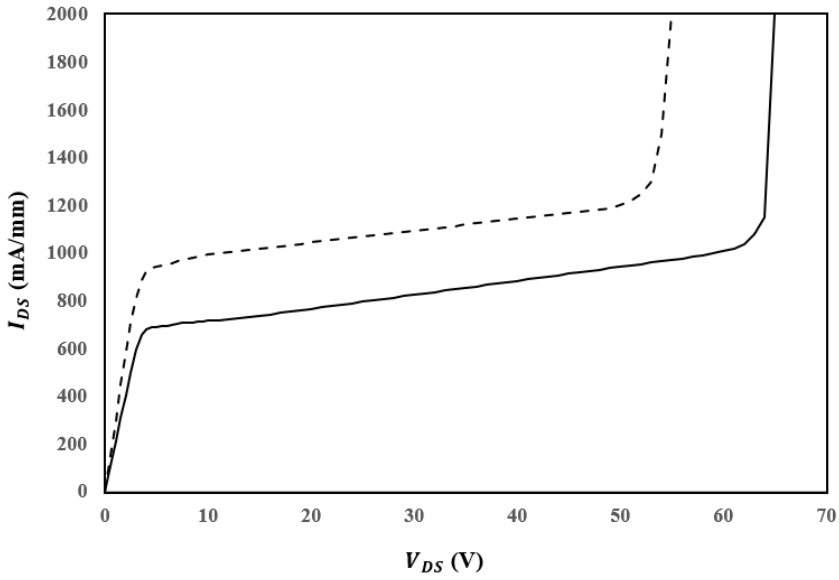


Figure 3.22 I_{DS} -V_{DS} at V_{GS} = -1 V of the simulated devices having L_{GS} = 1.5 µm (dashed line) and L_{GS} = 3 µm (solid line) for fixed L_G = 0.5 µm and L_{GD} = 5 µm.

As shown in Fig. 3.22, the on-state breakdown voltage is observed to vary from 65 V to 55 V by scaling down the L_{GS} from 3 µm to 1.5 µm.

From results shown in Fig. 3.23, it can be deduced that with the downscaling of L_G from 0.5 µm to 0.25 µm, the average electric field along the gate-source access region is increasing from 22 kV/cm to 25 kV/cm. In turn, while a small difference, this increases the electron velocity of the charge carriers in the aforementioned region and as a result the electron density in the proximity of the high-field region (as seen in Fig. 3.24). The presence of higher 2DEG concentration in the proximity of the high-field region, initiates the avalanche breakdown at lower V_{DS}.

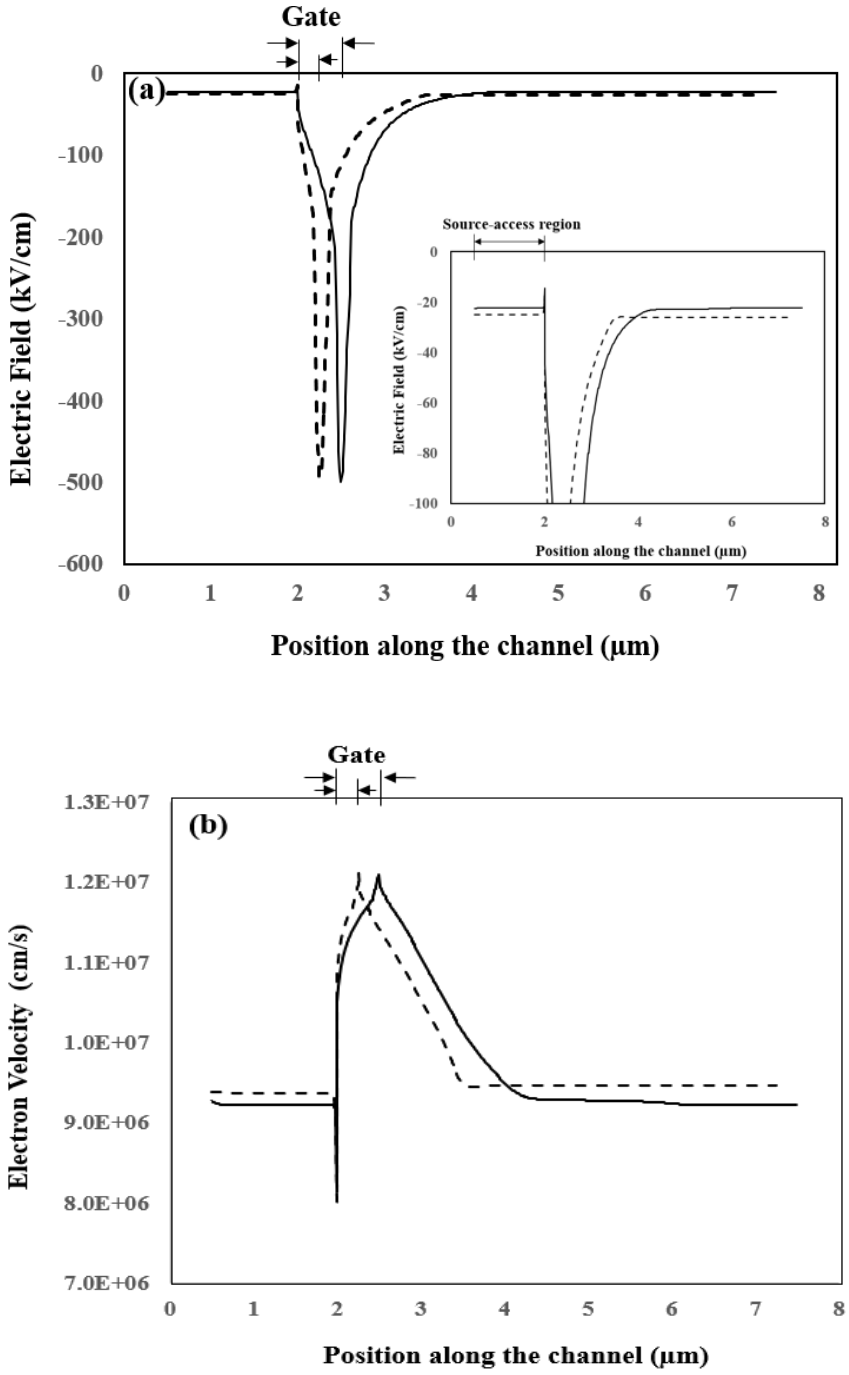


Figure 3.23 (a) Longitudinal electric field profile and (b) electron velocity along the channel and 1 nm below the heterointerface for devices with L_G = 0.25 μm (dashed line) and 0.5 μm (solid line) for fixed L_{GS} of 1.5 μm and L_{GD} of 5 μm at $V_{GS,Eff}$ = 3 V and V_{DS} = 38 V. Inset of part (a): close-up of the electric field profile across the source-access region.

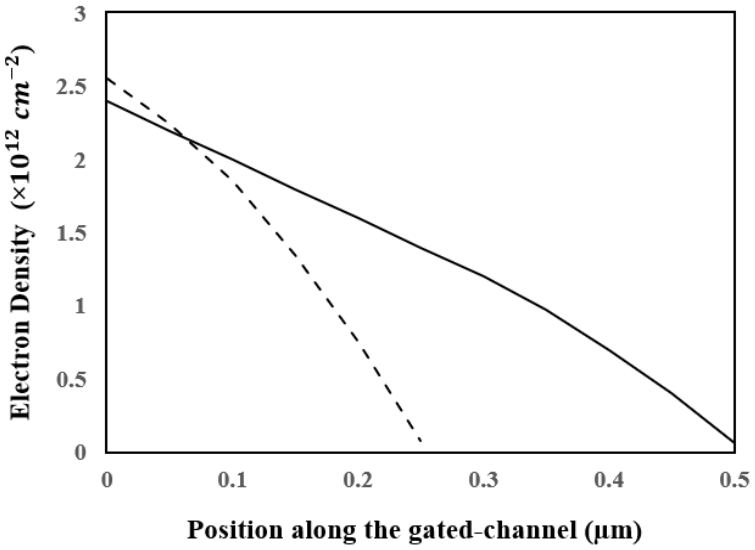


Figure 3.24 Electron density under the gated-channel and 1 nm below the heterointerface of devices having L_G = 0.25 µm (dashed line) and L_G = 0.5 µm (solid line) for fixed L_{GS} of 1.5 µm and L_{GD} of 5 µm at $V_{GS,Eff}$ = 3 V and V_{DS} = 38 V.

As shown in Fig. 3.25, the on-state breakdown voltage is observed to vary from 55 V to 30 V by scaling down the L_G from 0.5 µm to 0.25 µm.

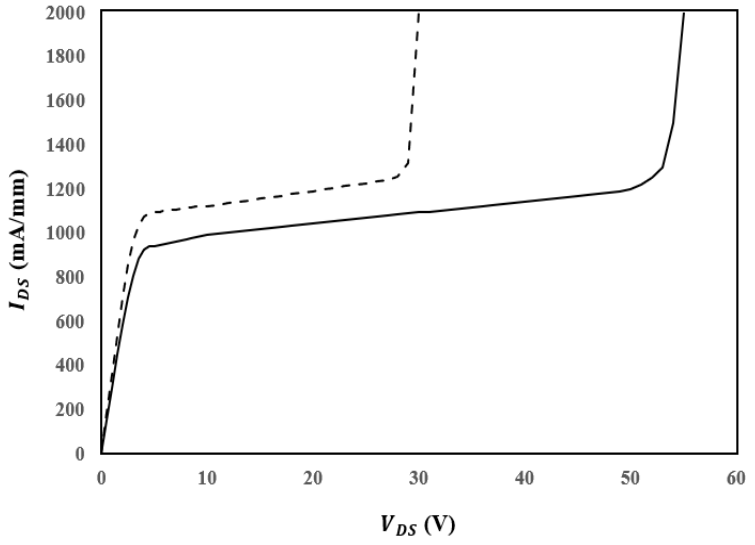


Figure 3.25 I_{DS}-V_{DS} at $V_{GS,Eff}$ = 3 V of the simulated devices having L_G = 0.25 µm (dashed line) and L_G = 0.5 µm (solid line) for fixed L_{GS} = 1.5 µm and L_{GD} = 5 µm.

3.4 Conclusion

In this chapter, I have performed an extensive analysis to understand the correlation between the scaling of L_{GS} and L_G and their impact on the source access resistance and the performance of InAlN/GaN HFETs. In the presence of the source access region, two potential solutions have been explored to increase the current supply from the aforementioned region: 1. increase of the electron velocity of the gate-source access region by the downscaling of L_{GS} and L_G and 2. increase of the electron concentration in the gate-source access region which is realizable with a wider source-access region connected to the intrinsic gated channel. The downscaling of L_{GS} and L_G will enhance the electron velocity in the source access region and as a result the presence of higher sheet charge density under the gated channel facilitates the enhancement of the maximum drain-current density. Whereas the improvement of the device linearity performance is attainable through a longer and planar source-access region and shorter gate length. However, downscaling of the L_{GS} and L_G is limited by the breakdown effects due to the presence of higher charge density in the vicinity of the high electric field region initiating breakdown at lower drain voltages.

Chapter 4

Multilevel recessing of the gated barrier for improving device linearity performance of InAlN/GaN HFETs

4.1 Introduction

Enhanced optical phonon scattering [15], alloy and interface scattering [67] and dynamically increasing gate-to-source access resistances at high channel currents cause non-linearity among GaN-channel HFETs [68]. Device concepts like self-aligned HFETs [16], double channel heterostructures [17], nanowire-channel GaN HFETs [19], and transitional recessed gate HFETs [20] have been studied to reduce the device nonlinearity. However, these approaches often contribute to extra parasitic capacitances, poor gate controllability and poor breakdown voltage, which in turn degrade the device performance. In response, in this chapter, I present a novel "V_{th}-modulated HFET" to achieve a broad G_m curve exemplifying transistor linearity.

Recessing of the barrier layer to different depths changes the device's threshold-voltage (V_{th}). Increased electrotactic static control of the gate over the channel and decreased polarization charge density as a result of the recessing of the barrier layer shifts the threshold voltage of the recessed HFET towards a less negative value. Considering the aforementioned physics, "V_{th}-modulated HFET" can be seen as a system of transistors comprised of a number of parallelly

connected HFETs of different V_{th}, in which upon proper design the HFETs having less negative threshold voltage get to compensate the gate transconductance drop of HFETs of relatively more negative threshold voltage at a given gate overdrive coinciding with the trailing end of the transconductance characteristics. Mi *et al.* reported the InAlN/GaN HFET consisting of non-recessed and recessed gated barrier along the gate width [86]. When the applied gate voltage is close to V_{th} of a non-recessed HFET (i.e., an HFET of relatively more negative V_{th}), the channel of non-recessed part turns on, and when the gate voltage increases and reaches to the value close to V_{th} of recessed HFET for which the gated barrier is uniformly recessed along the gate width, the channel of recessed part turns on [86]. This way, gate transconductance profiles of the non-recessed and recessed HFET are superimposed on each other and a broad gate transconductance profile has been realized with an evident double peak feature, which screams the need for a proper design as high linearity requires a single broad peak profile. The issue of signal distortion in power amplifiers is mainly due to the gate transconductance fluctuation and improvement of the same is a necessity for modern wireless communication technologies where high data transfer rates and spectrum efficiency are the basic needs [87].

4.2 Device schematics and material properties

Using COMSOL Multiphysics three different $In_{0.17}Al_{0.83}N$/GaN HFETs have been simulated to observe the effect of multilevel recessing of the barrier layer at gate, source, and drain along the gate width: the non-recessed HFET (shown in Figure 4.1 (a)), recessed HFET (shown in Figure 4.1 (b)), and V_{th}-modulated HFET (shown in Figure 4.1 (c)). The layer structure for non-recessed and recessed HFET consists of 9 nm and 4 nm thick $In_{0.17}Al_{0.83}N$ barrier layer, respectively on top of 1.7 μm thick GaN channel layer. Both layers were considered UID to the

level of 1×10^{14} cm^{-3}. For the V_{th}- modulated HFET, height of the barrier layer is changing from 4 nm to 9 nm in step of 1nm where the width of each region is 0.1 μm (i.e., from total gate width of 0.6 μm). Source and drain contacts were assumed as ideally Ohmic whereas the gate defined as Schottky contact with metal work function of 5.2 eV. In all three structures the gate-source length (L_{GS}), gate-drain length (L_{GD}) and gate length (L_G) are 0.5 μm, 1.5 μm, and 0.1 μm, respectively.

The material properties of $In_{0.17}Al_{0.83}N$ and GaN used in simulations are presented in Table 4.1 [39], where we have adopted the field-dependent mobility [$\mu_n(E)$] using the Caughey and Thomas model [81] represented by,

$$\mu_n(E) = \frac{\mu_{n,low}}{\left(1+\frac{\mu_{n,low} \times |E_x|}{v_{n,sat}}\right)}. \quad (4.1)$$

where $\mu_{n,low}$ is the low-field electron mobility, E_x is the longitudinal electric field, and $v_{n,sat}$ is the electron saturation velocity.

Table 4.1 Material properties of $In_{0.17}Al_{0.83}N$ and GaN used in the simulation.

Parameter	Value ($In_{0.17}Al_{0.83}N$)	Value (GaN)
Static relative permittivity (ϵ_r)	6.16	8.9
Bandgap (E_g)	4.62 (eV)	3.39 (eV)
Electron affinity (χ_0)	1.484 (eV)	4.1 (eV)
Effective density of states, valance band (N_{vo})	2.23×10^{19} cm^{-3}	4.6×10^{18} cm^{-3}
Effective density of states, conduction band (N_{co})	4.6×10^{18} cm^{-3}	2.3×10^{18} cm^{-3}
Low-field electron mobility (μ_n)	800 (cm^2/V·s)	1000 (cm^2/V·s)
Low-field hole mobility (μ_p)	82 (cm^2/V·s)	200 (cm^2/V·s)
Electron saturation velocity ($v_{n,sat}$)	1.1×10^{17} (cm/s)	1.5×10^{17} (cm/s)

Devising a mesh for numerical simulation is one of the most important tasks in simulating the devices in COMSOL simulation tool and its proper optimization has been done to ensure that the results are not changing drastically when the mesh is refined.

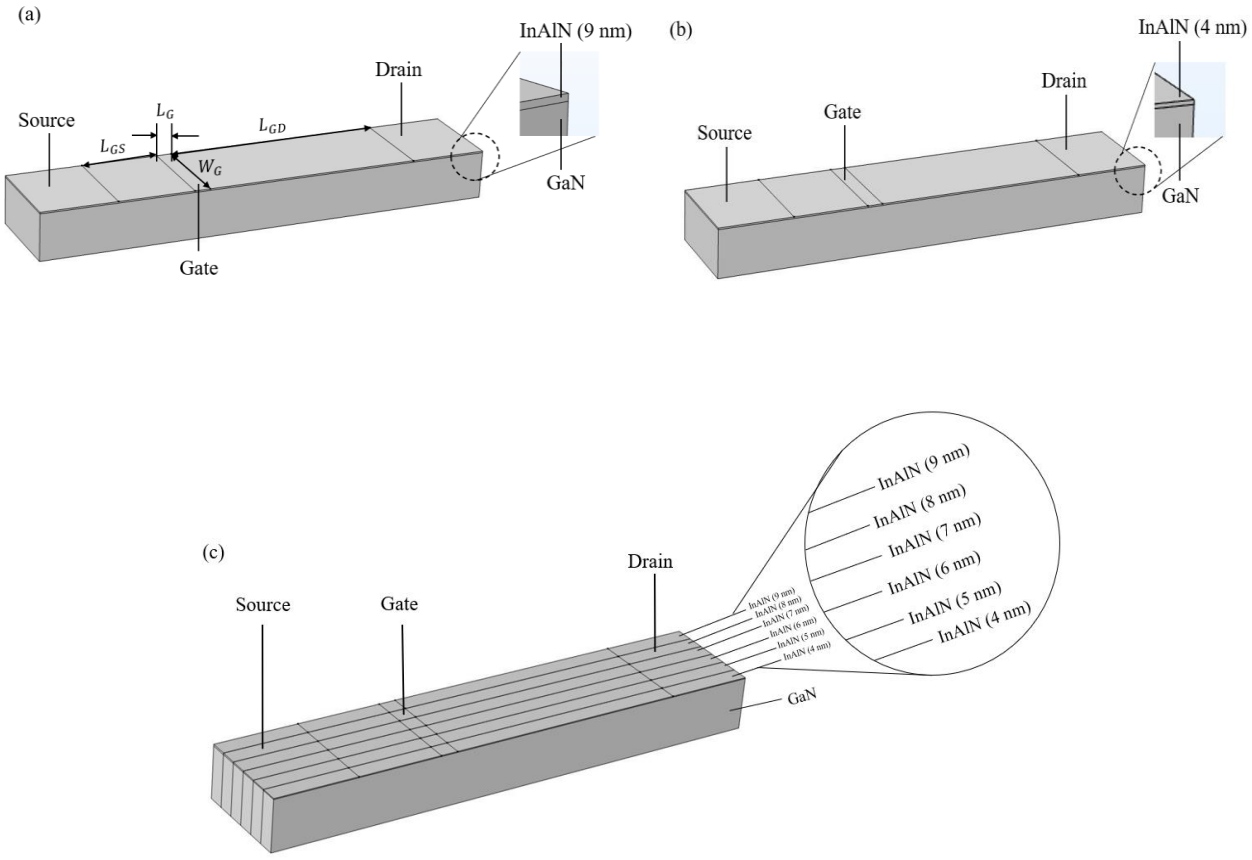


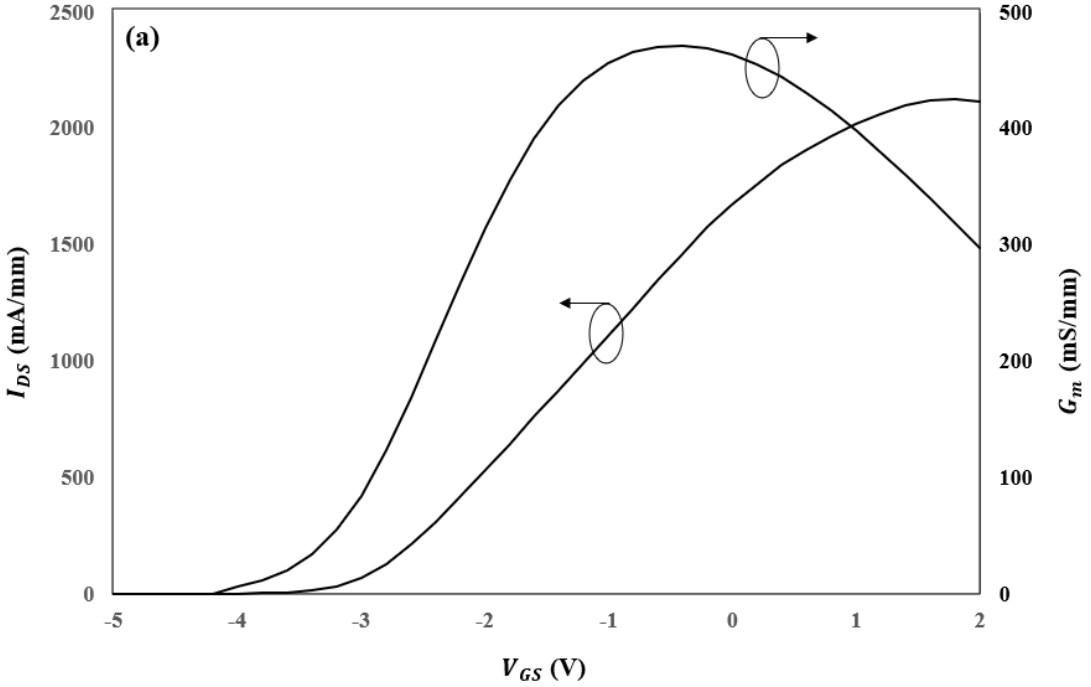
Figure 4.1 Schematic diagram of the: (a) non-recessed HFET, (b) recessed HFET, and (c) V_{th}-modulated HFET.

4.3 Results and discussion

The normalized transfer characteristics and gate transconductance profiles of non-recessed, recessed and V_{th}-modulated HFETs at V_{DS} = 6 V are shown in Figure 4.2. In the performed

simulations, we have not taken into consideration the gate leakage current which is more evident at relatively positive $V_{GS.}$ A straightforward solution is to add a gate dielectric layer between the gate and barrier layer to reduce the gate leakage current. The threshold voltage for the recessed HFET has been shifted from –3 V, which is the threshold voltage of non-recessed HFET to 0.1 V. This is due to the enhanced gate electrostatic control over the channel benefiting from the recessing of the barrier layer. Whereas its value is around -2.5 V for the V_{th}-modulated HFET.

The peak G_m values for non-recessed, recessed, and V_{th}-modulated HFETs are 472 mS/mm, 867 mS/mm, and 868 mS/mm, respectively. In this study, the figure of merit GVS is defined as the gate voltage range across which the value of the gate transconductance remains at least 80% of its peak value and $|\Delta G_m|$ (where $|\Delta G_m| = |G_{m1} – G_{m2}|$; as depicted in Figure 4.2 (c)) is signifying the difference between the highest and lowest peaks of the G_m profile of the V_{th}-modulated HFET indicating partial improvement in the flatness of the transconductance curve. To achieve a flat G_m curve the value of $|\Delta G_m|$ should be zero. The GVS of non-recessed and recessed HFET are 2.6 V and 2 V, respectively. The V_{th}- modulated HFET shows the highest GVS of 4.5 V among all three devices and $|\Delta G_m|$ of 43 mS/mm, indicating a scope for the improvement of the flatness of the transconductance profile.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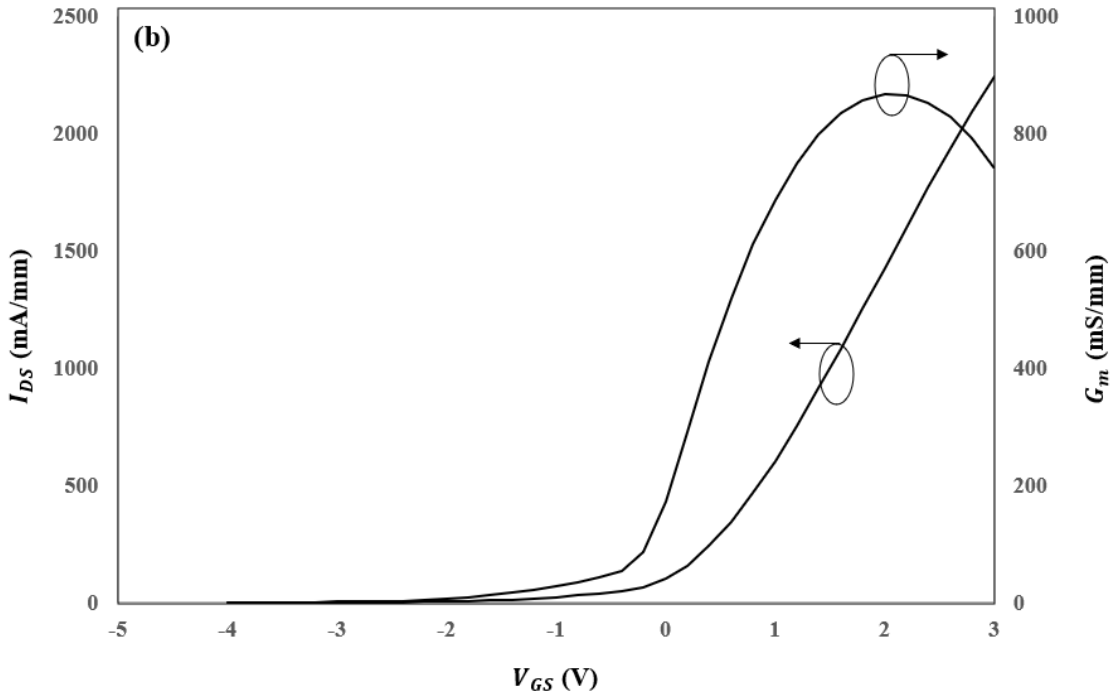
I_{DS} (mA/mm)
G_m (mS/mm)
V_{GS} (V)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I_{DS} (mA/mm)
G_m (mS/mm)
V_{GS} (V)

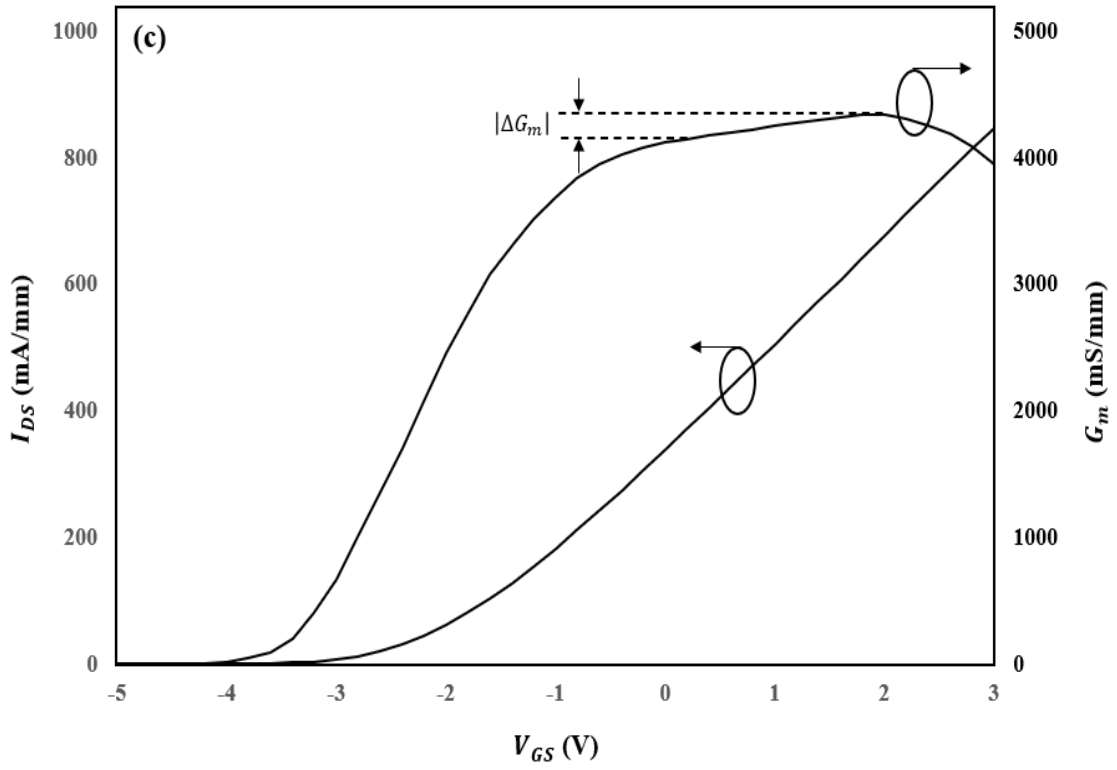
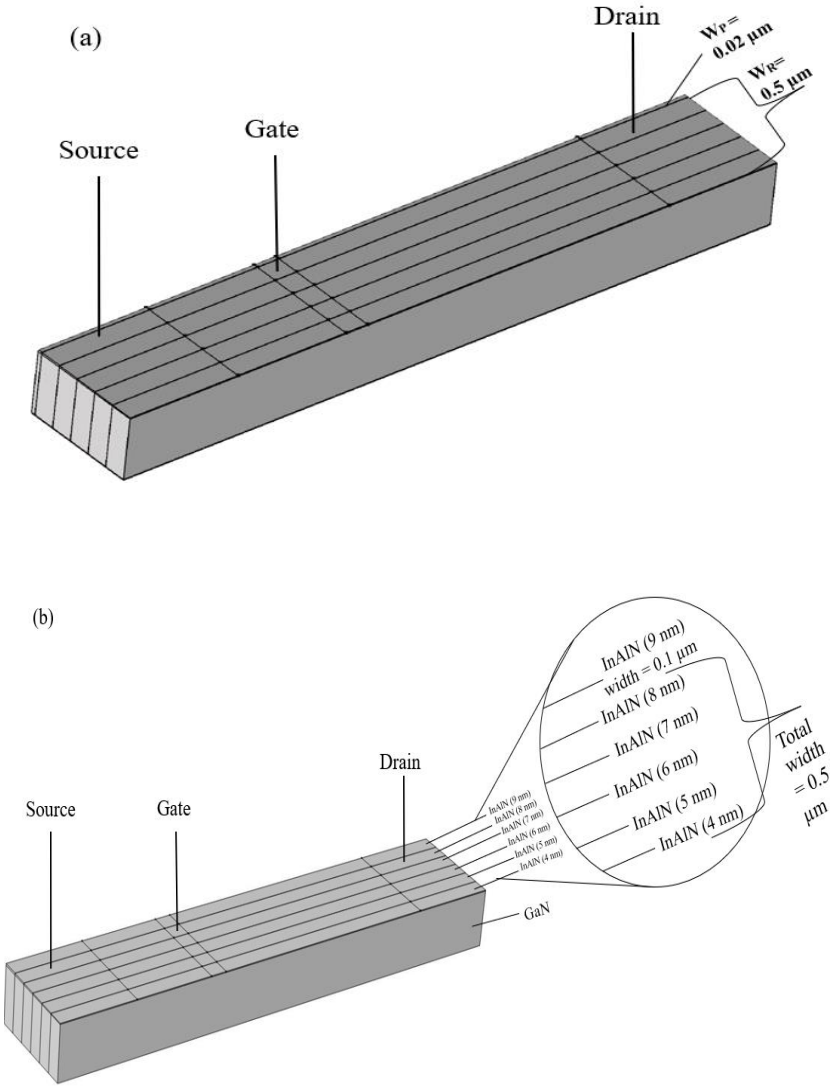


Figure 4.2 Normalized transfer characteristics and variation of gate transconductance vs V_{GS} at V_{DS} = 6 V for: (a) non-recessed, (b) recessed, and (c) V_{th}-modulated HFET.

Zhao *et al.* reported the improvement in terms of the flatness of the gate transconductance curve of HEFT having no-recessed and recessed regions connected parallelly along the gate width by having a wider non-recess region compared to recess region [88]. By taking the same concept, I have analyzed the influence of the width of the non-recessed region (W_N) on the flatness of the transconductance profile of the V_{th}-modulated HFET providing the total width of the recessed regions (W_R) remains same. Using COMSOL Multiphysics, four different V_{th}-modulated $In_{0.17}Al_{0.83}N$/GaN HFETs, having a significant difference in terms of the width of the non-recessed (W_N) region amongst them, have been simulated. These structures are illustrated in Figure 4.3. In all four structures the gate-source spacing, drain-gate spacing, and gate length are 0.5 µm, 1.5 µm, and 0.1 µm, respectively. The layer structure consists of $In_{0.17}Al_{0.83}N$ barrier layer on top of 1.3

μm thick GaN channel layer with UID donor concentration of 1 $\times 10^{14}$ cm^{-3}. Height of the barrier layer is changing from 4 nm to 9 nm in step of 1nm, where the width of each recessed region is 0.1 μm occupying in total 0.5 μm from the total gate width and W_N is varying from 0.02 μm (type-I) to 0.1 μm (type-II) to 0.5 μm (type-III) to 2.5 μm (type-IV).



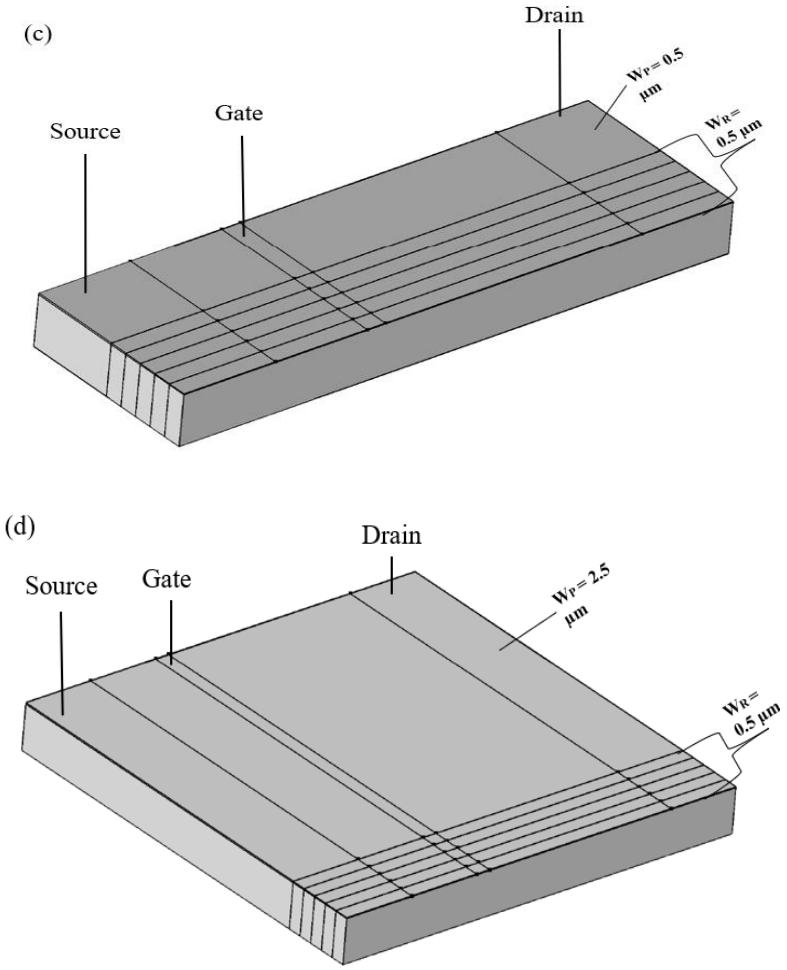


Figure 4.3 Schematic diagrams of the: (a) Type-I, (b) Type-II, (c) Type-III, and (d) Type-IV V_{th}-modulated HFETs.

The linear transfer characteristics and gate transconductance vs. V_{GS} profiles of all four types of V_{th}-modulated HFETs are shown in Figure 4.4. Threshold voltages of the devices are consistently observed to be around −2.5 V, while maximum drain current density of type-I, II, III, and IV at V_{GS} = 0 V and V_{DS} = 6 V are 1672 mA/mm, 1690 mA/mm, 1705 mA/mm, and 1722 mA/mm, respectively. The peak G_m values for type-I, II, III, and IV V_{th}-modulated HFETs at V_{DS} = 6 V are 864 mS/mm, 868 mS/mm, 874 mS/mm, and 878 mS/mm, respectively. GVS of all four types of V_{th}-modulated HFETs is around 4.5 V but $|\Delta G_m|$ values for type-I, II, III, and IV devices are 50 mS/mm, 43 mS/mm, 35 mS/mm, and 17 mS/mm, respectively.

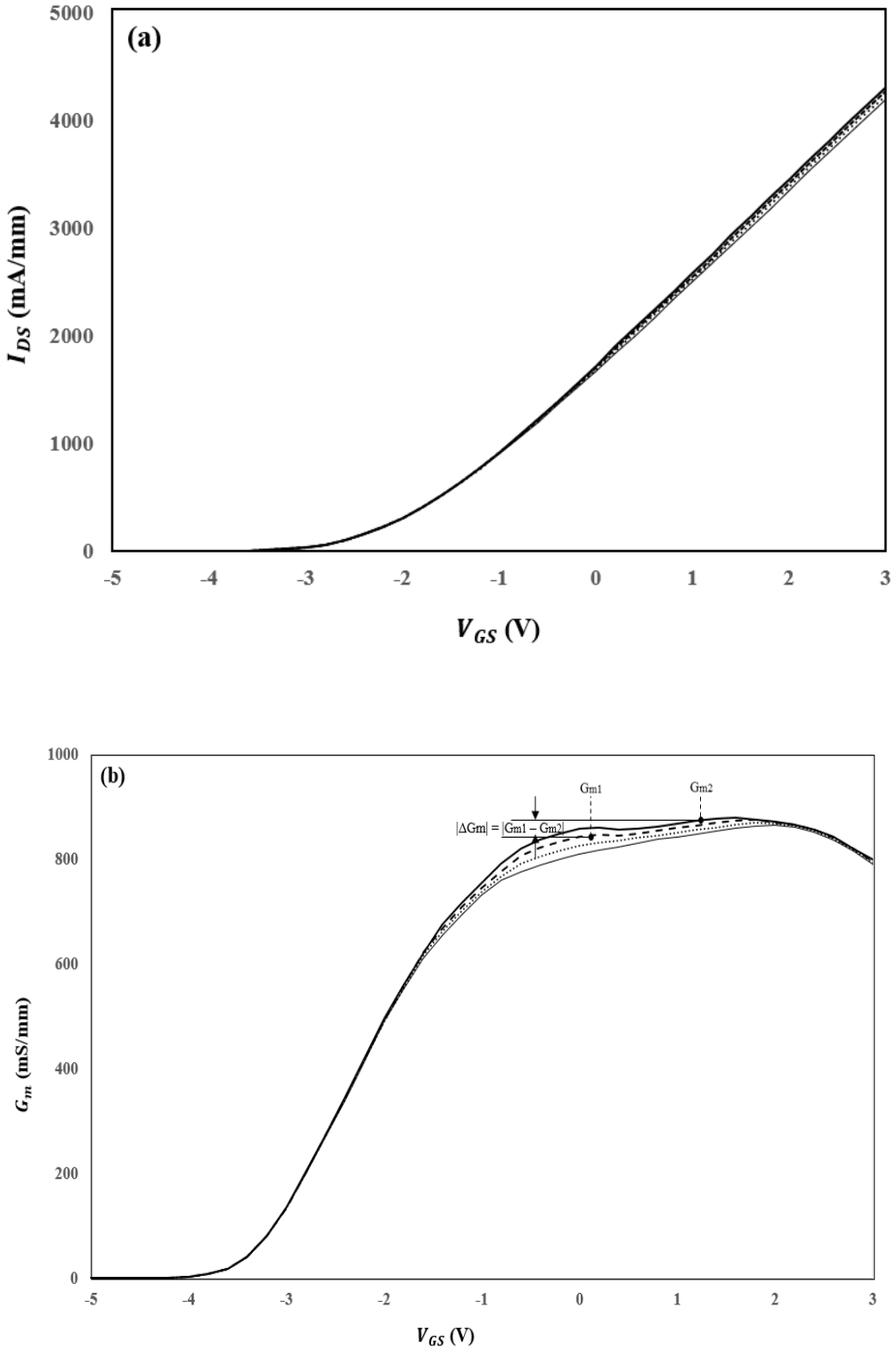


Figure 4.4 (a) Normalized transfer characteristics and (b) gate transconductance profiles vs. V_{GS} of type-I (thin solid line), type-II (dotted line), type-III (dashed line), and type-IV (thick solid line) V_{th}-modulated $In_{0.17}Al_{0.83}N$/GaN HFETs at V_{DS} = 6 V.

Accordingly, among these it is observed that the flatness of a G_m profile is improving by increasing the width of the non-recessed region by keeping the total width of the recessed parts the same. To understand the improvement of the flatness with increasing the width of the non-recessed region, I have conducted device simulations employing COMSOL Multiphysics to plot the vertical electric-field profiles of all four types of HFETs along the gate width (as shown in Figure 4.5). The presence of a varying vertical electric-field along the gate width for the V_{th}-modulated devices compared to a constant electric-field for the devices of a constant barrier height along the gate width is a result of established polarization charge gradient along the gate width, which has been verified by checking the 2DEG density 1 nm below the heterointerface at V_{GS} = 0 V and V_{DS} = 6 V (from Table 4.2).

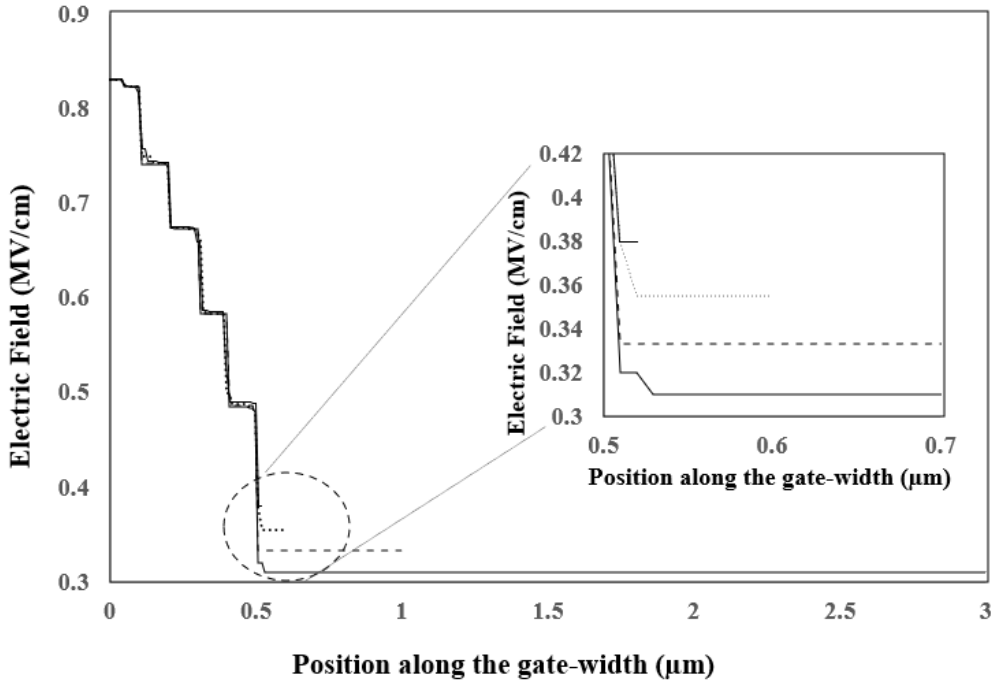


Figure 4.5 Vertical electric field profile of type-I (thin solid line), type-II (dotted line), type-III (dashed line), and type-IV (thick solid line) V_{th}-modulated $In_{0.17}Al_{0.83}N$/GaN HFETs along the gate width and in the middle of the gate and 1nm below the heterointerface at V_{GS} = 0 V and V_{DS} = 6. Inset: Close up of the vertical electric field profile along the gate width at the beginning of the non-recessed region.

Table 4.2 The electron concentrations are extracted in the middle of the gated channel and along the gate width and 1 nm below the heterointerface at V_{GS} = 0 V and V_{DS} = 6 V.

Thickness of the barrier (nm) through which 2DEG cut line is passing	**2DEG of the freestanding HFETs ($\times 10^{13}$ cm^{-2})**	**2DEG of the V_{th}-modulated HFETs ($\times 10^{13}$ cm^{-2})**			
		Type-I	**Type-II**	**Type-III**	**Type-IV**
4	0.028	0.132	0.134	0.134	0.135
5	0.236	0.303	0.309	0.316	0.318
6	0.562	0.577	0.577	0.578	0.581
7	0.862	0.854	0.855	0.857	0.857
8	1.298	1.271	1.272	1.275	1.275
9	1.806	1.544	1.602	1.688	1.752

From Table 4.2 and Figure 4.5 we can say that 2DEG density under the non-recessed region is increasing with an increment of the width of the non-recessed region. Also, from Table 4.2 it is very clear that charge carrier density below the recessed HFETs varies with the width of the non-recessed region. Thus, the interplay between the increased and redistributed 2DEG density and pronounced vertical electric-field along the gate width with an increment of the non-recessed region is contributing to the ameliorating of the flatness of a G_m profile by decreasing the difference between the two peaks (i.e., G_{m1} and G_{m2}).

Extremely precise and controlled etching of the barrier layer is indeed a crucial part for the realization of the V_{th}-modulated $In_{0.17}Al_{0.83}N$/GaN HFET having multilevel recessing along the gate width. After performing AFM measurement on the samples having mesas for which MERIE parameters used for the recessing of the barrier layer (i.e., RF power, strength of the magnetic field, pressure, and etching time) were different, I have found that entire layer of the $In_{0.17}Al_{0.83}N$ has been etched from all the mesas. Etching of the barrier layer is happening so quickly as the barrier layer is consisting of a very high concentration of the aluminum (i.e. 83%). As a result of this, I was not able to fabricate and characterize the V_{th}-modulated $In_{0.17}Al_{0.83}N$/GaN HFETs.

4.4 Conclusion

A new approach for enhancing the linearity and flatness of gate-transconductance profile of InAlN/GaN HFETs was presented. Simulation results show an improvement in linearity observed through broadening the gate transconductance characteristics of V_{th}-modulated HFETs, for which gated barrier was uniformly recessed along the gate width. In aforementioned devices, the gate transconductances attributed to the parallel channels can effectively eliminate the drop in the gate transconductance at higher gate over drives due to their sequential turn-ons, and essentially yield a sufficiently broad G_m-V_{GS} characteristics. Simultaneously, broadening the width of the non-recessed region of the V_{th}-modulated HFET can enhance the flatness of the gate-transconductance profile. This could be the result of the interplay between the increased and redistributed 2DEG density and pronounced vertical electric-field along the gate width.

Chapter 5

Conclusions and future work suggestions

5.1 Concluding remarks

In chapter 1, I presented the underlying physics and mechanisms of the premature roll-off of gate-transconductance which is responsible for nonlinearities. According to the existing body of literature, dynamic increase of the source-access resistance at higher drain currents has been identified as the main contributor of the nonlinearity in GaN-channel HFETs. In this chapter, some of the device concepts that have been explored so far to conquer the nonlinear effect are explained and a brief description about the difficulty and challenges associated with the presented device technologies.

In chapter 2, the reliability of metallic-face InAlN/GaN HFETs having fin structures only under the gate, while maintaining a planar structure in the access regions and those of the HFETs having fin structures stretched from source to drain is investigated by the means of low-frequency noise as an ultra sensitive spectroscopy tool. LFN in both types of HFETs is representable by the carrier number fluctuations with correlated mobility fluctuation, whereas the noise of the gated channel has been deemed likely to be as the dominant noise source. According to this investigation, the InAlN/GaN HFETs having fin structures present only in the gated channel exhibited not only the expected much better direct current (DC) performance, but at the same token a better 1/f LFN performance compared to the device having fins stretched from source to drain. This is a result of

the presence of the higher charge density under the gated channel in the HFETs having a wider source access region connected to the intrinsic channel overshadowing the carrier number and mobility fluctuations.

In chapter 3, I explored the correlation between the scaling of gate-source length and gate length and their impact on the source access resistance and the performance of InAlN/GaN HFETs having fin structures only under the gate and those having them stretched from source to drain. Accordingly, I presented two potential solutions to improve the device linearity performance: 1. planar and longer source access region connected to the gated-channel and 2. downscaling of the gate length. In this approach, the planar source access region is offering larger current drive, as a result of which the suppression of a dynamic increase of the source-access resistance is attainable. For devices having shorter L_G, the chance of lowering the barrier between the source-access region and the gated-channel is much higher compared to the devices having longer L_G. This aids with a noticeable supply of the carriers from the source-access region to the gated-channel and as a result the suppression of the increasing source-access resistance at higher drain currents offers the improved linearity performance of the devices having shorter L_G. Employing COMSOL Multiphysics, I showed that the downscaling of L_{GS} and L_G will enhance the electron velocity in the source access region and as a result the presence of higher sheet charge density under the gated channel facilitates the enhancement of the maximum drain-current density. However, downscaling of the L_{GS} and L_G is limited by the breakdown effects as a result of the presence of higher charge density in the high electric field region initiating avalanche breakdown at lower drain voltages.

In chapter 4 employing COMSOL Multiphysics, I assessed the suitability of multilevel recessing of the gated barrier to improve device linearity performance. Accordingly, I presented a novel threshold-voltage (V_{th})-modulated GaN channel HFET consisting of non-recessed and

recessed gated barrier along the gate width. The V_{th}-modulated HFET can be seen as parallelly connected HFETs of different V_{th}, in which the HFETs having less negative threshold voltages compensate the transconductance drop of HFETs of relatively more negative threshold voltage at a given gate overdrive. This way the summation of the transconductances attributed to the parallel channels essentially yields a sufficiently broad G_m-V_{GS} characteristics. Also, I evaluated the impact of the width of the non-recessed region on the flatness of the transconductance profile while keeping the width of the recessed regions the same. It has been observed that the interplay between the presence of a varying vertical electric-field and established polarization charge gradient along the gate width in the V_{th}-modulated devices is facilitating the improvement of the flatness of the transconductance profile.

5.2 Future work suggestions

As mentioned in section 5.1, a part of this research work was dedicated to thorough investigations of the low frequency noise characteristics of InAlN/GaN HFETs having fin structures only under the gate, while maintaining a planar structure in the access regions and those having them stretched from source to drain at room temperature (i.e., 300 K). I would suggest investigating the effects of planarity of access region on the low-frequency noise performance of InAlN/GaN HFETs at temperatures other than 300 K. According to number fluctuation theory, the spectrum of the G–R noise follows a Lorentzian profile and the corner frequency, which is identified by this relaxation time constant, is temperature-dependent. As a result, studying the temperature-dependent variation of this corner frequency can be used in evaluation of the energy level of the responsible trap site and help to address the possible difficulties in the performance of the presented devices in this research work. Also, the application of devices having fins just under the gate to microwave through design of MMICs would be tremendously interesting.

Furthermore, it has been reported that unpassivated devices endure significant changes in the output resistance and drain noise current level after DC stress while passivated devices do not show any considerable variation upon DC stress [89]. Thus, I suggest the investigation of the impact of DC stress on partially passivated devices having fins just under the gate and unpassivated devices having fins starched from source to drain by means of low frequency noise measurements.

The plasma etching employed to realize the fin structures introduces shallow and/or deep acceptor/donor type trap levels in both InAlN barrier layer and GaN-channel layer. Existence of these traps in the different regions of a HFET structure is the main reason for the parasitic effects like gate and drain lags and high gate leakage current which will lower the breakdown voltage and the power added efficiency (PAE), which ultimately limits the device high power performance. In response, I suggest the usage of high-k gate dielectric layer between the gate metal and barrier layer which in turn establishes significant large potential barrier between the gate metal and 2DEG channel to reduce the gate leakage current. Also, the implantation technology can be used instead of the etching process for isolation to decrease the damage associated with the plasma etching and the fringing capacitance through sidewall for the fin structures.

While in this thesis I have assessed the suitability of multilevel recessing of the gated-barrier on improving device linearity performance via simulation only, fabricating such devices and performing actual measurement of their high frequency characteristic to compare with those of having gate metal wrapped around the fin structures which introduces large parasitic capacitance is recommended.

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Appendix I: Process flow

❖ Steps toward mesa lithography and etching

1. **Cleaning**
    - Acetone [5 min]
    - Isopropyl alcohol [1 min]
    - Deionized water [2 min]
    - Nitrogen gun
    - Dehydrate on hotplate at 150 ℃ [2 min]
2. **Spin coating**

▪ Coat sample with ma-N 2403 resist

- Spread at 500 rpm for 5sec
- Spin with 3000 rpm for 30 sec
- Deceleration 5sec

3. **Soft bake**

▪ 90 ℃ hotplate for 60 sec

4. **E-beam lithography**
    - Exposures dose: 235 $\mu C/cm^2$
    - Line spacing and center to center distance: 10 nm
    - Working distance: 3 mm
    - Spot size: 2.9 nm
    - Absorption current 34 pA
5. **Develop**
    - ma-D 525 for 3 min (including 1 min in ultrasonication)
    - DI water

- Nitrogen gun

6. Hard bake

- 100 °C for 60 sec

7. Etch

- Use MERIE P500

• Cl_2: 20	Ar: 10	0 G	0 W	90 mtorr	30 s
• Cl_2: 20	Ar: 10	70 G	170 W	90 mtorr	60 s
• Cl_2: 0	Ar: 60	0 G	50 W	0 mtorr	10 s

8. Resist removal

- Acetone
- IPA
- DI water
- Nitrogen gun

❖ Steps toward fabrication of Ohmic contacts and deposition of SiN_X

1. Cleaning

- Acetone [5 min]
- Isopropyl alcohol [1 min]
- Deionized water [2 min]
- Nitrogen gun
- Dehydrate on hotplate at 150 °C [2 min]

2. Spin coating

- Spin coat MMA(8.5)MAA-EL11 resist
  - Spread at 500 rpm for 5 sec
  - Spin with 4000 rpm for 45 sec
  - Deceleration 5 sec

- Bake sample on hotplate at 150°C for 90 sec
- Cool down the sample

- Spin coat PMMA-A4 resist
    - Spread at 500 rpm for 5 sec
    - Spin with 4000 rpm for 45 sec
    - Deceleration 5sec

- Spin coat H_2OX_2 anti-charge agent
    - Spread at 500 rpm for 5 sec
    - Spin with 4000 rpm for 45 sec
    - Deceleration 5sec

3. Soft bake

- Bake sample on hotplate at 180°C for 90 s

4. E-beam lithography

- Exposures dose: 200 $\mu C/cm^2$
- Line spacing and center to center distance: 20 nm
- Working distance: 3 mm
- Spot size: 2.6 nm
- Absorption current 28 pA

5. Develop

- Develop in MIBK/IPA 1/3 for 60 sec
    - Stop develop in DI water
    - Post-bake at 100°C for 60 sec
    - Oxide removal in $HCl:H_2O$ (1:4) solution for 2 minutes

- Rinse in DI water
- Drying with nitrogen gun (hot plate was not used to prevent oxide re-growth)

6. Metallization

- Ti 200 Å / Al 1200 Å / Ni 400 Å/ Au 500 Å

7. Liftoff

- Liftoff in acetone and ultrasound bath

8. RTA

- 765°C for 60 sec

9. PECVD of SiN_X

- Use MERIE P500

• SiH_4: 0	N_2: 0	NH_3: 0	0 W	0 mtorr	30 s
• SiH_4: 180	N_2: 2000	NH_3: 0	350 W	4.5 mtorr	5 s
• SiH_4: 180	N_2: 2000	NH_3: 75	350 W	4.5 mtorr	13 s
• SiH_4: 0	N_2: 2000	NH_3: 75	0 W	4.5 mtorr	60 s

❖ Steps toward fabrication of fin structures and gate contacts

1. Cleaning

- Acetone [5 min]
- Isopropyl alcohol [1 min]
- Deionized water [2 min]
- Nitrogen gun
- Dehydrate on hotplate at 150 °C [2 min]

2. Spin coating

- Coat sample with ma-N 2403 resist
  - Spread at 500 rpm for 5sec
  - Spin with 3000 rpm for 30 sec

- Deceleration 5sec

3. Soft bake

- 90 ℃ hotplate for 60 sec

4. E-beam lithography

- Exposures dose: 235 μC/cm^2
- Line spacing and center to center distance: 10 nm
- Working distance: 3 mm
- Spot size: 2.9 nm
- Absorption current 34 pA

5. Develop

- ma-D 525 for 3 min (including 1 min in ultrasonication)
- DI water
- Nitrogen gun

6. Hard bake

- 100 ℃ for 60 sec

7. SiN_X Etch

- Use MERIE P500
- CF_4: 40 O_2: 4 0 G 0 W 100 mtorr 15 s
- CF_4: 40 O_2: 4 70 G 100 W 100 mtorr 90 s
- CF_4: 0 O_2: 20 0 G 25 W 0 mtorr 15 s

8. Spin coating

- Spin coat MMA(8.5)MAA-EL11 resist
  - Spread at 500 rpm for 5sec
  - Spin with 4000 rpm for 45 sec

- Deceleration 5 sec

- Bake sample on hotplate at 150°C for 90 sec
- Cool down the sample
- Spin coat PMMA-A4
    - Spread at 500 rpm for 5 sec
    - Spin with 4000 rpm for 45 sec
    - Deceleration 5 sec
- Bake sample on hotplate at 180°C for 90 sec
- Spin coat H_2OX_2 anti-charge agent
    - Spread at 500 rpm for 5 sec
    - Spin with 4000 rpm for 45 sec
    - Deceleration 5sec

9. E-beam lithography

- Exposures dose: 200 $\mu C/cm^2$
- Line spacing and center to center distance: 20 nm
- Working distance: 3 mm
- Spot size: 2.6 nm
- Absorption current: 28 pA

10. Develop

- Develop in MIBK/IPA 1/3 for 60 sec
    - Stop develop in DI water
    - post-bake at 100°C for 150 sec

11. Etch

- Use MERIE P500

• Cl_2: 20	Ar: 10	0 G	0 W	90 mtorr	30 s
• Cl_2: 20	Ar: 10	70 G	170 W	90 mtorr	60 s
• Cl_2: 0	Ar: 60	0 G	50 W	0 mtorr	11 s

12. Metallization

Ni 200 Å/ Au 500 Å

13. Liftoff

Liftoff in acetone and ultrasound bath

❖ Steps toward pad deposition

1. Spin coating

- Spin coat with AZ5214 photoresist
    - Spread at 500 rpm for 5sec
    - Spin with 3000 rpm for 30 sec
    - Deceleration 5sec
- Bake sample on hotplate at 90°C for 55 s

2. Photolithography

- Exposure with 25 mJ/cm^2
- Post-bake at 105°C for 120 sec
- Flood Exposure with 250 mJ/cm^2 for 0.6 s

3. Develop

- AZ726 developer for 30 s
- Stop develop in DI water
- Post-bake at 100°C for 60 sec

4. Metallization

- Ni 200 Å/ Au 200 Å

5. Liftoff

- Liftoff in acetone and ultrasound bath
- Sample cleaning with acetone, IPA, and DI water