Design and Demonstration of Optical Logic Gates with Electronic Interface for Optical Switching Applications

Ataollah Mahsafar

A Thesis

in

The Department

of

Electrical and Computer Engineering

Presented in Partial Fulfillment of the Requirements

for the Degree of

Master of Applied Science (Electrical Engineering) at

Concordia University

Montréal, Québec, Canada

September 2025

CONCORDIA UNIVERSITY

School of Graduate Studies

This is to certify that the thesis prepared

By: **Ataollah Mahsafar**

Entitled: **Design and Demonstration of Optical Logic Gates with Electronic Interface for Optical Switching Applications**

and submitted in partial fulfillment of the requirements for the degree of

Master of Applied Science (Electrical Engineering)

complies with the regulations of this University and meets the accepted standards with respect to originality and quality.

Signed by the Final Examining Committee:

_____ Chair
Dr. John Xiupu Zhang

_____ External Examiner
Dr. Pablo Bianucci

_____ Examiner
Dr. John Xiupu Zhang

_____ Supervisor
Dr. Glenn Cowan

Approved by _____
Dr. Wahab Hamou-Lhadj, Chair
Department of Electrical and Computer Engineering

_____ 2025

_____
Dr. Mourad Debbabi, Ph.D.,P.Eng., Dean
Faculty of Engineering and Computer Science

Abstract

Design and Demonstration of Optical Logic Gates with Electronic Interface for Optical Switching Applications

Ataollah Mahsafar

The scalability of high-capacity networks increasingly depends on advances in switching technology. Optical switching, particularly using microring-based logic, offers a path to higher bandwidth and lower signal degradation while enabling compact, cascadable architectures.

This thesis presents a microring modulator (MRM)-based 2×2 optical switch built from cascadable optical logic gates (OLGs) with electronic control circuits. An OLG is a fundamental building block of optical computing systems, performing logic operations by manipulating optical signals rather than electrical ones, thereby leveraging the inherently higher speed and lower propagation loss of light. The OLG's functionality is validated through experimental measurements of power transfer characteristics (PTC), optical noise margins (ONMs), and fan-out performance. The 2×2 switch, implemented with seven interconnected OLGs, demonstrates the scalability of this approach for more complex optical logic networks.

To enable higher-speed operation, a CMOS implementation of the electronic control circuit, for driving and processing optical-logic signals, was designed and fabricated in TSMC's 65 nm technology, occupying an active area of 1 mm × 1.25 mm. The design incorporates a peak/low detector-based offset compensation technique that ensures stable performance under unbalanced input data patterns. Post-layout simulations verify correct logic functionality, showing a simulated propagation delay of approximately 107 ps. Despite this delay, the standalone gate can process narrow pulses, corresponding to a data throughput of up to 8 Gbps.

The combined demonstration of discrete and integrated implementations highlights the potential

of microring-based optical switching as a scalable solution for future high-performance networking and computing systems.

Acknowledgments

I would like to thank my supervisor, Prof. Glenn Cowan, for his guidance and expertise, which have been invaluable in completing this work. I am also grateful for the opportunity to be part of his energetic research group at Concordia University.

Furthermore, I sincerely appreciate the contributions of my collaborators, whose expertise and input have been instrumental in advancing this research. In particular, I acknowledge David Rolston, Prof. Odile Liboiron-Ladouceur, José García-Echeverría, and Daniel Musat for their notable contributions.

I am thankful to my friend and office-mate, Sara Radfar, for her thoughtful advice and willingness to help whenever needed throughout this journey. I also extend my thanks to the other members of our research group, particularly Abdullah Ibn Abbas, Di Zhang, and Vinicius Sirtoli, for their valuable knowledge sharing and support along the way.

I gratefully acknowledge the Canadian Microelectronics Corporation (CMC) for their assistance and support.

Finally, I am profoundly grateful to my parents for their endless love, sacrifices, and belief in me. Even though I have been far from them during these years, their constant encouragement and guidance have been the foundation of everything I have accomplished. I also extend my heartfelt thanks to my brother, Ali, whose support, understanding, and inspiration have been a source of strength throughout my academic journey. This accomplishment would not have been possible without their unwavering presence in my life, despite the distance.

Contents

List of Figures **ix**

List of Tables **xv**

1 Introduction **1**

1.1 Motivation 1

1.2 Contributions and publications 3

1.3 Thesis organization 4

2 Literature Review **6**

2.1 Microring Resonators/ Modulators 6

2.2 MRM Device Used in This Work 13

2.3 Related Work on Optical Logic Gates 16

2.3.1 Optical Logic Gate Realization Using Zero-Bias Photonic Structures 16

2.3.2 Optical Logic Gate Realization Using Feedback-Controlled PN-Junction Tuning 19

2.3.3 Non-MRM-Based Structures 22

2.4 Logic control circuit components 24

2.4.1 I-V Conversion Circuits 25

2.4.2 Main Amplifiers (MAs) 31

2.4.3 DC Offset Compensation (DCOC) 34

2.5 Conclusion 37

3 Design and Realization of a 2×2 Optical Switch Using Cascadable Optical Logic Gates 38

3.1 Optical Logic Gate Design and Characterization 38

3.1.1 Cascadable Optical NOT Gate Design 39

3.1.2 Cascadable Optical NAND Gate Design 44

3.1.3 Logic Control Design 45

3.1.4 Power Transfer Characteristic, Optical Noise Margin, and Fan-out Measurements 46

3.2 2×2 Optical Switch Design and Characterization 52

3.2.1 2×2 Switch based on Optical Combinational Logic 52

3.2.2 2×2 Optical Switch Measurements 53

3.3 Conclusion 58

4 Design and Tapeout of the Proposed IC-Level Peak/Low Detector-Based Logic Control Circuit 60

4.1 Design of the Proposed Peak/Low Detector-Based Logic Control Circuit 64

4.1.1 Subtractive PD Pair Structure 66

4.1.2 TIA Design 67

4.1.3 MA Design 70

4.1.4 Proposaed DC Offset Compensation (DCOC) Design 72

4.1.5 NAND Gate and Output Inverter Design 85

4.2 Post-Layout Simulation Results 87

4.2.1 Behavior Under Input Densities of logical ‘1’s from 10% to 90% in 10% Increments 89

4.2.2 Behavior Under a Direct Transition from 10% to 90% Input Density (Worst-Case Scenario) 92

4.2.3 High-Speed Functionality Test with Balanced Input Signals at 8 Gbps . . . 96

4.2.4 PTC and ONM Simulations for an Optical NOT 99

4.3 Floor Planning 100

4.4 Measurement Setup and Fabricated Chip Integration 102

4.5 Conclusion 103

5 Conclusions and Future Work **105**

5.1 Comparision 106

5.2 Future Work 109

Appendix A KiCad Design of the Logic Control PCB **111**

Appendix B KiCad Design of the High-Speed PCB **116**

Bibliography **118**

List of Figures

Figure 1.1 (a) Conceptual schematic of a cascadable 2×2 optical multiplexer (switch). (b) Implementation using seven optical NAND gates with local regeneration. (c) Conceptual schematic of an optical NAND gate. 3

Figure 2.1 (a) Single-bus and (b) double-bus MRR configurations for optical signal routing. 7

Figure 2.2 (a) Transmission spectrum of an MRR, illustrating resonance wavelength (λ_{res}) and full width at half maximum (FWHM), and (b) Periodic resonance occurring at free spectral range (FSR) intervals. The figure also indicates the insertion loss (IL). 9

Figure 2.3 Structure of an MRM with an embedded pn-junction for electro-optic tuning [22]. 10

Figure 2.4 Differential transmission spectra of an MRM under varying reverse-bias voltages, showing the resonance shift between the unbiased and reverse-biased states. . 11

Figure 2.5 Block diagram of the thermal control unit for MRM [24]. 12

Figure 2.6 (a) Micrograph of the fabricated MRM, and (b) measured transmission spectra at V_{rb} = 0 V and V_{rb} = 5 V, highlighting the operating wavelength λ_{c} for differential logic operation. 14

Figure 2.7 (a) Differential optical transmission ($T_T - T_D$) measured for V_{rb} from 0 V to 5 V, showing resonance shift, (b) linear relationship between V_{rb} and differential optical transmission ($T_T - T_D$), (c) electro-optic tuning of the resonance wavelength versus V_{rb}. 15

Figure 2.8 Zero-bias PD stack in the optical-to-voltage converter (OVC) used to drive an MRM without external electrical power [27]. 17
Figure 2.9 Optical power-to-voltage characterization. Measured OVC output voltage as a function of input optical power (P_A or P_B) for different input logic P_{AB} configurations: 00, 01, 10, 11. 18
Figure 2.10 Operational principle of the zero-bias optical logic gate [27]. (a) OR gate implementation and (b) NOR gate implementation. 18
Figure 2.11 PN-junction feedback-based control scheme for implementing optical logic gates using MRMs [20]. (a) Circuit schematic for NOR gate. (b) Operational principle of NOR gate. 20
Figure 2.12 QDSOA–MZI based all-optical NOR gate with corresponding truth table [11]. 22
Figure 2.13 Schematic of the Kerr-effect-based photonic crystal AND gate structure [29]. 23
Figure 2.14 Overall block diagram of the logic control circuit, illustrating its key functional components 25
Figure 2.15 Resistor-based I–V conversion: (a) circuit schematic and (b) AC small-signal model. 26
Figure 2.16 Minimal OLG using PD, resistor R_C, and MRM. 27
Figure 2.17 CMOS inverter-based TIA: (a) circuit schematic and (b) small-signal model. 30
Figure 2.18 Cherry–Hooper amplifier used as a main amplifier stage: (a) circuit schematic and (b) small-signal model. 33
Figure 2.19 Inverter-based DCOC circuit with low-pass filtering and feedback loop. (a) Circuit schematic with compensation current I_{OC} used to stabilize the baseline. (b) Output voltage V_O without DCOC, showing baseline drift. (c) Output voltage V_O with DCOC, showing corrected baseline around $V_{\mathrm{DD}}/2$. 35
Figure 2.20 Pseudo-random signal between 300 mV and 700 mV with 50% logical '1'. The black dashed line shows the midpoint (0.50 V) and the red dashed line the average (0.503 V). 36

Figure 3.1 (a) Schematic of a conventional digital NOT gate, showing the VTC and noise margins; (b) conceptual schematic of an optical NOT gate, illustrating the PTC and its associated ONMs. 39
Figure 3.2 conceptual schematic of a simplified logic control circuit for a differential optical inverter 42
Figure 3.3 (a) Schematic of the designed cascadable optical NAND gate, and (b) micrograph of the fabricated PIC featuring a double-bus MRM, integrated PDs that receive optical input signals for logic control circuit, and monitoring PDs used for implementing the thermal control circuit. 45
Figure 3.4 Schematic of the electronic circuit designed to control each optical NAND gate. 46
Figure 3.5 (a) Experimental setup for measuring the PTC of the optical NOT gate, (b) measured VTC of the active electrical circuit and its slope, (c) measured PTC of the optical NOT gate and its slope, (d) system optical gain after removing the effect of the active electrical circuit. 49
Figure 3.6 (a) optical inverter PTC at a CW input power of $-6\,\mathrm{dBm}$, showing the full input range and extracted ONMs. (b) PTC of the optical inverter under different CW input powers, illustrating the decrease in output amplitude with reduced input power. And (c) corresponding slope variations of the inverter response as a function of input power, highlighting the reduction in gain at lower powers. 50
Figure 3.7 (a) Schematic of the designed combinational logic to perform a 2×2 optical switch function, and (b) micrograph of the manufactured photonic integrated circuit. 53
Figure 3.8 Experimental setup to perform the MRM, logic control and 2×2 switch measurements including a CW C-band laser, DMLs, PCs, DAQ TS 15130 to generate the optical input logic signals and monitor the logic control, the device under test (DUT) consisting of the PIC and PCB logic control, QPhotonics QPFD-200 PDs, low-speed I-V conversion resistance in PCB, and an oscilloscope. 54

Figure 3.9 Measured through powers of IN-1, IN-2, SEL, OUT-1, and OUT-2, along with their estimated drop (complementary) powers, demonstrating the bar and cross functionality of the 2×2 optical switch. 56
Figure 4.1 Schematic illustration of thermal locking behavior under unbalanced modulation. 61
Figure 4.2 Measured differential transmission ($T_T - T_D$) as a function of reverse bias voltage V_{rb} at 0 V and 1 V. The operating points corresponding to 10%, 50%, and 90% logical '1' data densities are highlighted. 61
Figure 4.3 Simulated photocurrent at the input of the logic control circuit of the cascaded OLG for densities of logical '1's ranging from 10% to 90%. 63
Figure 4.4 Block diagram of the proposed IC-level logic control circuit. 64
Figure 4.5 Subtractive PD Pair structure. 67
Figure 4.6 Schematic of the inverter-based TIA with selectable feedback resistors using a T-gate switching network. 68
Figure 4.7 Simulated small-signal on-resistance of the T-gate switch with optimized transistor sizing, showing a relatively constant resistance over the 0 – 1.2 V signal range. The x-axis represents the DC voltage applied to both terminals of the switch. 69
Figure 4.8 simulated AC response of the reconfigurable TIA for three different feedback resistance settings. 70
Figure 4.9 Schematic of the three-stage Cherry-Hooper main amplifier. 71
Figure 4.10 (a) Simulated AC response of the MA for different feedback resistance settings. (b) Combined response of the full three-stage MA with $R_{\mathrm{MA}} = 200\ \Omega$ in all stages. 72
Figure 4.11 Block diagram of the proposed logic control circuit with accurate peak/low detector-based DCOC. 73
Figure 4.12 High-level schematic of the PKD circuit. 75
Figure 4.13 Schematic of the two-stage comparator used in the peak detector. 77
Figure 4.14 DC sweep of the stand-alone comparator, showing a sharp switch near 700 mV. 79

Figure 4.15 Transient response to: (a) a 2 mV input step, (b) a 30 mV input step, (c) a 400 mV input step. (d) Overdrive recovery test. 80
Figure 4.16 Full PKD simulation with a triangular wave input: (a) tracking and hold operation; (b) decay and detection of a new peak. 82
Figure 4.17 High-level schematic of the LWD, complementary to the PKD. 83
Figure 4.18 Schematic of the comparator used in the LWD circuit. It follows the same structure as the PKD comparator but with complementary devices. 84
Figure 4.19 Proposed DCOC block. 85
Figure 4.20 Schematic of the electrical NAND gate followed by an inverter. 86
Figure 4.21 Layout of one receiver arm of the proposed circuit (e.g., Arm A), along with the NAND gate and the output inverter 88
Figure 4.22 Receiver output voltages under varying input data densities (10%–90%): (a) proposed receiver, (b) conventional receiver. 90
Figure 4.23 Eye diagrams for the (a) proposed and (b) conventional receivers under varying data densities. 91
Figure 4.24 Input photocurrent waveform showing a direct transition from 10% to 90% input density; (a) full view, (b) zoomed-in view. 92
Figure 4.25 Input bidirectional photocurrent with 10× faster transition: from 10% to 90% logic '1' density (red curve) and from 90% to 10% logic '1' density (blue curve). 93
Figure 4.26 (a) The proposed and (b) conventional receiver output during worst-case density (10% to 90% and 90% to 10%) transitions. 95
Figure 4.27 Transient simulation results under 8 Gbps balanced input conditions showing the outputs of the two receiver arms, the NAND gate output, and the final AND signal. 97
Figure 4.28 Eye diagrams under 8 Gbps balanced input signals (50% logical '1's): (a) Receiver Arm A output, (b) Receiver Arm B output, (c) NAND gate output, (d) Final AND signal. 98
Figure 4.29 Schematic diagram of the simulated optical NOT gate configuration used for PTC and ONM analysis. 99

Figure 4.30 Simulated results for the IC-level optical NOT gate: (a) PTC and (b) corresponding slope. 100
Figure 4.31 Top-level block diagram view of the floor plan. 101
Figure 4.32 Layout of the complete logic control block, including pad ring and seal ring. 102
Figure 4.33 High-speed test PCB with the wire-bonded fabricated chip mounted for electrical measurements. 103
Figure A.1 High-level schematic of the logic control board used for the experiments in Chapter III 111
Figure A.2 Detailed schematic of a single logic control board implementing one AND gate. 112
Figure A.3 PCB layout of the logic control board. 113
Figure A.4 Fabricated logic control PCB. 114
Figure A.5 Experimental setup of 2×2 optical switch 115
Figure B.1 High-speed PCB schematic. 116
Figure B.2 High-speed PCB design. 117
Figure B.3 3D rendering of the high-speed PCB design. 117

List of Tables

Table 3.1 Truth table of the 2×2 optical switch 53

Table 5.1 Comparison of optical logic gate implementations. 108

Chapter 1

Introduction

1.1 Motivation

The growing demand for faster and more scalable computing and communication systems has fueled the exploration of novel logic architectures beyond conventional electronics. In traditional CMOS technology, although transistor delays continue to shrink, interconnect delays have become a dominant performance bottleneck [1, 2]. As a result, research has increasingly turned toward complementary approaches such as optical logic gates (OLGs) and optical switches, which leverage the natural advantages of light, including high speed, parallelism, low loss interconnects, and low crosstalk, and can be integrated with electronics through CMOS-compatible platforms [3, 4, 5, 6, 7, 8]. By employing optical interconnects, different stages of a system can be physically distributed across a larger area, reducing local power density and thermal hotspots. Additionally, distributing the electronic circuitry in such hybrid systems mitigates global electromagnetic interference (EMI) issues that often arise in dense electronic circuits. This level of physical separation and signal integrity management is difficult to achieve with conventional electrical interconnects, which suffer from higher losses and tighter integration constraints.

To realize these advantages at the logic level, various platforms have been explored for optical gates, including nonlinear effects [9], interferometers [10], SOAs [11], and photonic crystals [8, 12]. Among these, silicon photonics has emerged as a leading platform due to its compatibility with standard CMOS processes [7, 13], enabling close integration with electronics. This hybrid approach

allows scalable, cost-effective systems that combine the strengths of both photonics and electronics [14].

Microring modulators (MRMs) are particularly attractive for building optical logic gates. They have a small footprint, low power dissipation, and can operate at very high speeds [15], [16], [17]. Recent advances have demonstrated MRMs achieving over 200 Gbps data rates [15], making them strong candidates for future optical computing and optical interconnects.

Although many optical logic gates have been demonstrated individually, cascading them into larger systems remains a significant challenge. Insertion loss (IL) accumulates across stages, and without local signal regeneration using a fresh optical supply, signal quality rapidly degrades. This issue also affects existing switching architectures, such as Mach-Zehnder interferometer (MZI) switches [18], which route the same optical signal through multiple stages without regeneration, limiting scalability. Overcoming this bottleneck requires architectures with local optical signal regeneration at each stage.

Fig. 1.1 illustrates the core concept of our approach, showing (a) a modular, cascadable 2×2 optical multiplexer (switch), (b) its implementation using seven optical NAND gates, and (c) a conceptual schematic of an optical NAND gate constructed with MRMs and electronic control circuits. Each gate incorporates local signal regeneration, ensuring that every stage produces a fresh optical signal. Thus, while the output logically depends on the input, its power and signal integrity are independent of the input optical power, effectively avoiding cumulative IL. Thanks to fully optical interconnections between stages, larger switching networks built from these gates can operate at the speed of a single gate without performance degradation.

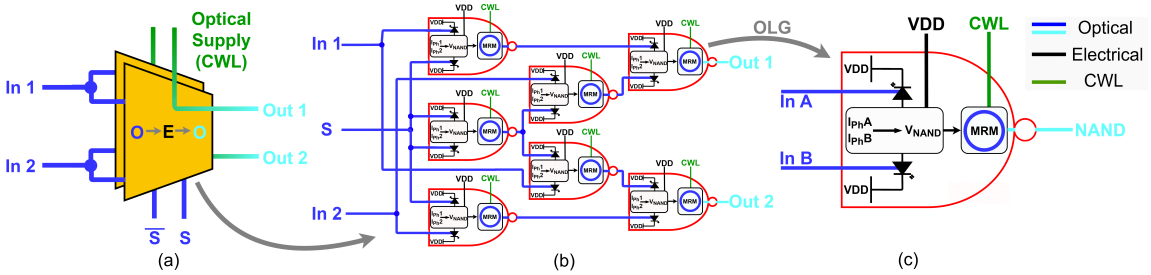

Figure 1.1: (a) Conceptual schematic of a cascadable 2×2 optical multiplexer (switch). (b) Implementation using seven optical NAND gates with local regeneration. (c) Conceptual schematic of an optical NAND gate.

1.2 Contributions and publications

In this work, we present the design, fabrication, and experimental demonstration of a multi-stage optical logic system based on cascadable MRMs, integrated with a dedicated electronic logic control circuit that processes photodetector (PD) outputs and generates drive voltages to modulate the MRMs according to the desired logic function, thereby enabling scalable optical operations. The system comprises seven interconnected gates forming a 2×2 optical switch, with regenerative behavior and logic-level performance. We experimentally verify key logic metrics for the optical system, including optical power transfer characteristics (PTC) and optical noise margins (ONM), establishing a direct analogy to conventional electronic logic gates. While previous works have explored high-speed [15], low-voltage [16], and wideband MRMs [17], and others have demonstrated or simulated optical logic gates using various platforms [19, 12, 20], they often lack cascaded architectures or logic-level analysis. A recent study demonstrates an MRM-based photonic latch [21], though the latch itself is not experimentally demonstrated. To our knowledge, this work presents the largest experimental demonstration of a cascaded MRM-based optical logic system to date.

The successful PCB implementation and testing validated the proposed approach for realizing optical logic gates using MRMs together with a logic control circuit. These results provide strong evidence supporting the feasibility of developing an integrated chip for the logic control block,

capable of operating at higher data rates and handling input data streams with unbalanced densities of 1s and 0s. As a result, a CMOS chip implementing the logic control circuit has been designed and taped out using TSMC's 65 nm CMOS technology.

A journal paper based on the research presented in this thesis is currently being finalized for submission as the primary publication arising from this work:

- **A. Mahsafar**, J. G. Echeverría, D. Musat, D. Rolston, O. Liboiron-Ladouceur, and G. Cowan, "2×2 Optical Switch Based on Combinational Logic with Microring Modulators," in preparation for submission to *Journal of Lightwave Technology*.

Additional publications (published and in preparation) and patents related to aspects of this research include:

- D. Musat, J. G. Echeverría, **A. Mahsafar**, D. Rolston, O. Liboiron-Ladouceur, and G. Cowan, "Calibration-free Stabilization Circuit for Silicon Photonics Microring Modulators," in preparation for submission to *IEEE Transactions on Circuits and Systems I: Regular Papers*.

- J. G. Echeverría, D. Musat, **A. Mahsafar**, K. R. Mojaver, D. Rolston, G. Cowan, and O. Liboiron-Ladouceur, "Self-Calibrated Microring Weight Function for Neuromorphic Optical Computing," *Journal of Lightwave Technology*, vol. 43, no. 2, pp. 602–610, Jan. 15, 2025, doi: 10.1109/JLT.2024.3462534.

- Provisional Patent Application, Serial No. 63/550,369, filed February 6, 2024.

- International PCT Application, Serial No. PCT/CA2025/050148, filed February 5, 2025.

1.3 Thesis organization

Chapter 2 introduces the fundamentals of microring resonators (MRRs) and MRMs, outlines the MRM device and thermal control method employed in this work, and reviews prior optical logic gate implementations based on these devices. It concludes with an overview of the key logic control circuit components relevant to this study. Chapter 3 describes the design of cascadable optical NOT and NAND gates, the logic control circuitry, and the 2×2 optical switch. It also presents

experimental results of individual logic gates and the full switch. Chapter 4 details the design and tape-out of a CMOS chip featuring an offset compensation technique in the logic control block, enabling reliable operation under unbalanced input data conditions at high data rates. Chapter 5 concludes the thesis by summarizing the key contributions and suggesting future research directions.

Chapter 2

Literature Review

This chapter begins by introducing the foundational concepts required to understand the operation of MRRs and MRMs, followed by a description of the specific MRM device and thermal control method employed in this work. It then reviews previous works on optical logic gates implemented using these devices, with particular emphasis on the design and structure of their logic control circuits, which process PD outputs and generate drive voltages for the modulators, as well as the associated challenges. Finally, it discusses the key components of logic control circuits commonly used in optical platforms.

2.1 Microring Resonators/ Modulators

As shown in Fig. 2.1 (a) and (b), MRRs are compact and ring-shaped waveguides that are typically implemented in either a single-bus or double-bus configuration, where light is coupled from a straight waveguide into the ring [22].

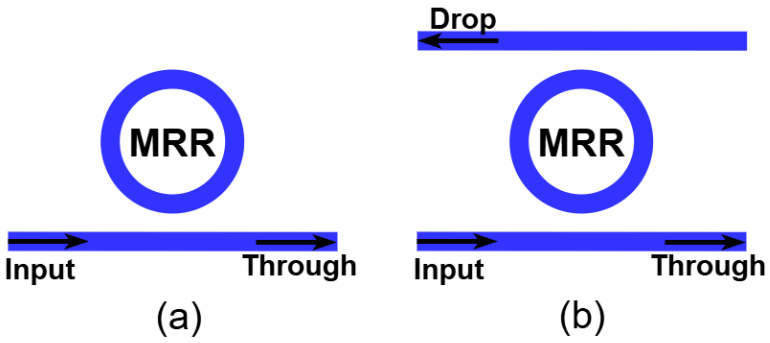

Figure 2.1: (a) Single-bus and (b) double-bus MRR configurations for optical signal routing.

In the single-bus configuration, the ring is coupled to only one straight waveguide. In the double-bus setup, an additional waveguide is placed on the opposite side of the ring, introducing a drop port alongside the through port. These configurations determine how light at different wavelengths interacts with the ring, controlling whether it continues through the bus waveguide or is coupled into the ring and redirected to the drop port.

To achieve resonance within the microring cavity, the round-trip optical path must satisfy a phase-matching condition: the total distance traveled by the light in one loop must equal an integer multiple of its wavelength. This condition is expressed as:

$$\lambda_{\text{res}} = \frac{n_{\text{eff}} L}{m} \tag{1}$$

where λ_{res} is the resonant wavelength, n_{eff} is the effective refractive index, L is the ring's optical path length (circumference), and m is a positive integer. This relationship indicates that multiple wavelengths can meet the resonance condition, each corresponding to a different resonance order defined by the integer m. The spacing between these resonances is referred to as the free spectral range (FSR), and it depends on the geometry and effective index of the ring.

Fig. 2.2 (a) shows a representative transmission spectrum of the through and drop ports in a double-bus MRR when a continuous-wave laser (CWL) is swept across the wavelength range. For the single-bus configuration, the through-port response remains similar, but no drop-port curve is present, as the drop port does not exist in that setup. As shown in this figure, in the single-bus

configuration, destructive interference occurs at resonance, resulting in a sharp notch in the transmission spectrum at the through port. Off-resonant wavelengths continue through the waveguide with minimal loss. This configuration is compact and well-suited for applications where only spectral selection is required. The double-bus configuration adds a second waveguide, forming a drop port. At resonance, a portion of the optical power goes from the input waveguide into the ring and then is transferred to the drop port. Light that does not satisfy the resonance condition remains in the through port [22].

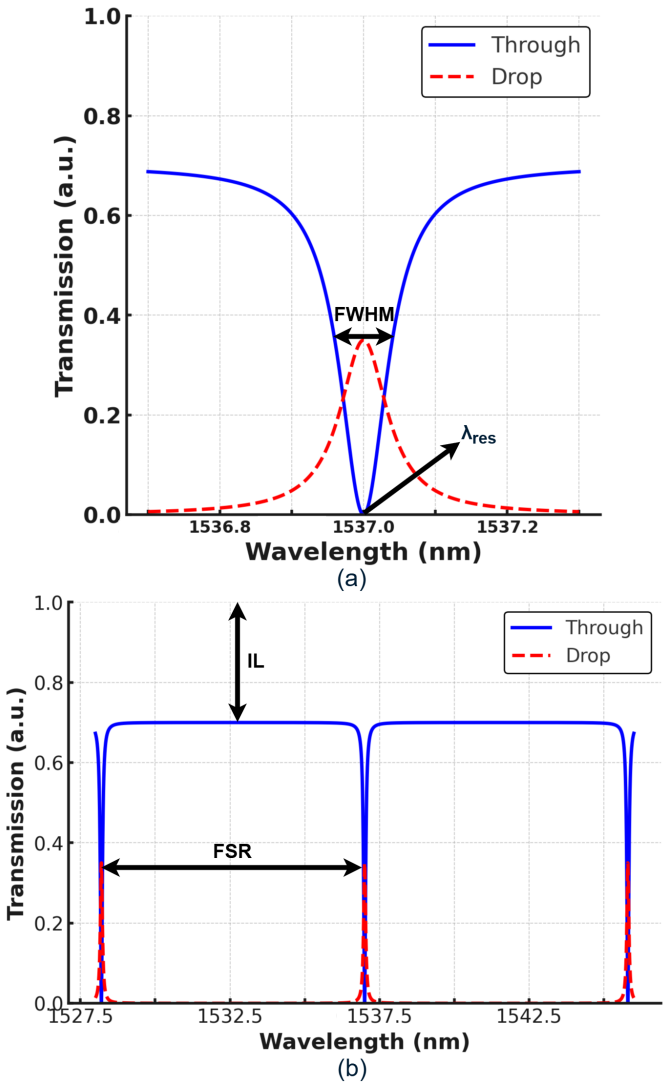

Figure 2.2: (a) Transmission spectrum of an MRR, illustrating resonance wavelength (λ_{res}) and full width at half maximum (FWHM), and (b) Periodic resonance occurring at free spectral range (FSR) intervals. The figure also indicates the insertion loss (IL).

Fig. 2.2 (a) and (b) also highlight several key parameters that influence its performance in photonic circuits. As discussed earlier, the resonant wavelength (λ_{res}) corresponds to the specific wavelength at which light interferes destructively at the through port. Another important metric is the full width at half maximum (FWHM), which defines the spectral width of the resonance notch at half its maximum depth. A smaller FWHM indicates a sharper and more selective resonance. In

addition to these parameters, the insertion loss (IL) represents the optical power lost due to absorption, scattering, or imperfect coupling in the microring structure, measured away from resonance. Also, the quality factor (Q) provides a measure of the sharpness of the resonance. A high Q factor corresponds to a narrow resonance bandwidth and is defined as follows:

$$Q = \frac{\lambda_{\text{res}}}{FWHM} \tag{2}$$

Fig. 2.3 shows the structure of a typical MRM based on a pn-junction embedded inside the ring. MRMs are derived from MRRs but are designed for active tuning of the resonance. This is typically achieved by modifying the refractive index of the ring waveguide via the carrier plasma dispersion effect under electrical bias [23].

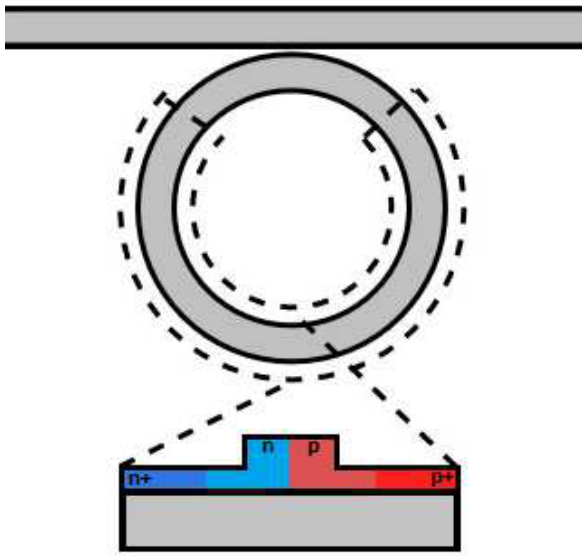

Figure 2.3: Structure of an MRM with an embedded pn-junction for electro-optic tuning [22].

Fig. 2.4 shows the through-port transmission spectrum of an MRM measured under both unbiased and reverse-biased conditions, highlighting how the curve shifts with applied voltage. As the reverse bias increases, the resonance wavelength shifts along the wavelength axis. This behavior results from changes in the carrier concentration within the ring waveguide, which alter the refractive index. Since the resonant wavelength depends on the effective refractive index, applying a reverse-bias voltage shifts the resonance condition. As a result, a given input wavelength may move from

an off-resonant to a resonant state (or vice versa), enabling modulation of the optical signal [23]. In this way, the MRM operates as an optical modulator. The effectiveness of an MRM is characterized by several key parameters. The extinction ratio (ER) refers to the ratio of transmitted optical power between the logic '1' and logic '0' levels at the through port. A higher ER indicates better contrast between logic states and thus improved signal integrity. The modulation efficiency refers to the voltage required to achieve a desired shift in resonance wavelength. More efficient MRMs require less drive voltage.

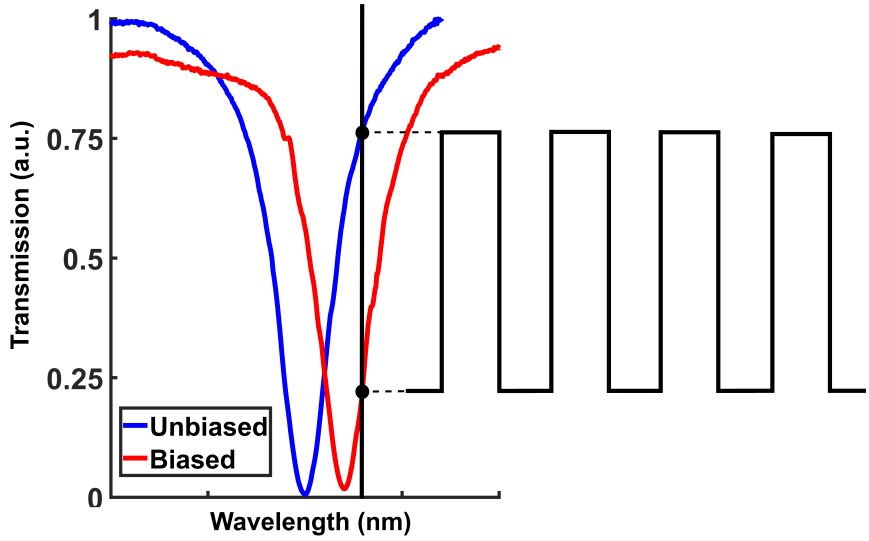

Figure 2.4: Differential transmission spectra of an MRM under varying reverse-bias voltages, showing the resonance shift between the unbiased and reverse-biased states.

MRRs and MRMs are highly sensitive to both fabrication-induced variations and changes in ambient temperature, posing a major challenge for reliable operation. To maintain the desired resonance condition despite these variations, the modulator must be equipped with an effective tuning mechanism that ensures alignment with the target wavelength.

A commonly used approach is to exploit the thermo-optic properties of silicon [23]. By placing a microheater adjacent to the ring, the local temperature can be increased to shift the resonance [24]. It should be noted that this method allows only heating; there is no active cooling mechanism. As a result, continuous heating is required to maintain resonance alignment, which can contribute to increased energy usage over time [22].

Fig. 2.5 shows the thermal feedback stabilization block diagram presented in [25]. In this approach, the optical powers at the through and drop ports of the MRM are monitored using low-speed, variable-gain transimpedance amplifiers (TIAs) connected to PDs integrated within the photonic integrated circuit (PIC). These electrical outputs (V_{Through} and V_{Drop}) are subtracted in a summer block to generate an error signal (V_{error}) that reflects the balance between the two ports. When the microring operates at the optimal locking point, the average through and drop powers are equal, yielding $V_{\text{error}} = 0$.

This error signal is fed into an analog proportional–integral–derivative (PID) controller, which regulates the voltage applied to an integrated microheater (V_{heater}). By increasing or decreasing heater power, the resonance condition is thermally tuned through the thermo-optic effect, driving the error signal toward zero and locking the microring at the desired operating point. Since this scheme derives its reference internally from the device's own optical behavior, it eliminates the need for external calibration, making it inherently robust to temperature drift, fabrication variations, and laser power fluctuations.

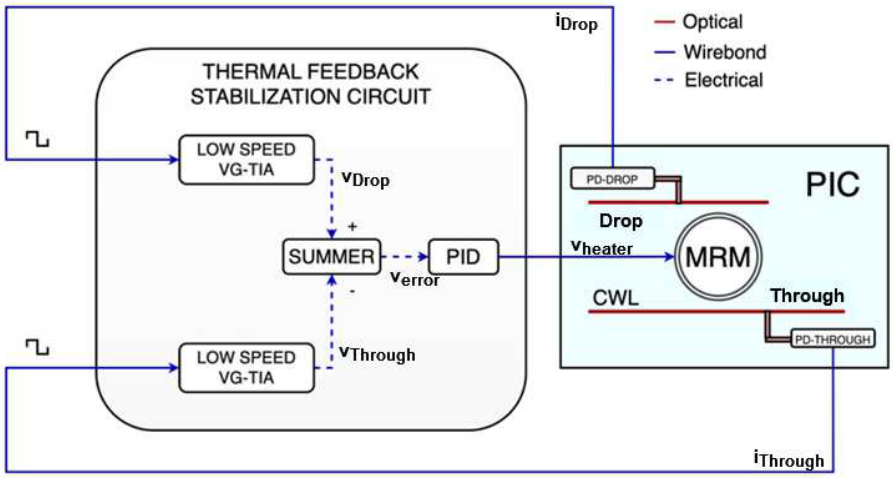

Figure 2.5: Block diagram of the thermal control unit for MRM [24].

This thermal control circuit, designed by Daniel Musat, a Ph.D. student at Concordia University, is employed in this work to maintain stable MRM operation.

2.2 MRM Device Used in This Work

The MRM used in this work is based on the design reported in [26] and was fabricated by José García Echeverría, a Ph.D. candidate at McGill University, on a silicon-on-insulator (SOI) platform using a double-bus configuration, with a measured optical insertion loss of approximately 2dB. The author contributed to the collaborative optical and electro-optic characterization of the device, the results of which are presented in this section to provide context for the implementation described in Chapter 3.

Fig. 2.6 (a) shows the micrograph of the fabricated MRM. The metal interconnect layers extend to the bondpads of the PIC, which are wirebonded to the printed circuit board (PCB) and interfaced with the MRM driver through an off-board electrical connection. In this setup, the p-type side of the pn junction was grounded, and the n-type side was biased with a positive voltage. For static (DC) biasing, this voltage is denoted as V_{rb}. Increasing V_{rb} expands the depletion region and shifts the resonance wavelength.

The OLG structure that will be introduced in Chapter 3 operates with a 0–5 V single-ended electrical drive, while the logic functionality is realized through complementary optical powers at the through and drop ports. While the detailed rationale for this architecture and drive voltage will be presented in later sections, these assumptions are stated here to establish the context for the following MRM characterization.

The differential transmission is defined as the optical power difference between the through and drop ports of the microring, evaluated at a fixed wavelength. Near resonance, this difference can be well approximated by a Lorentzian function [27]:

$$T_{\text{Out-Diff}}(\lambda) = T_T(\lambda) - T_D(\lambda) = 1 - \frac{(T+D)}{1 + 4\left(\frac{\lambda - \lambda_{\text{res}}}{\text{FWHM}}\right)^2} \tag{3}$$

where T indicates the ring's intrinsic extinction (with $T = 1$ for a critically coupled device), and D represents the coupling to the drop port. This Lorentzian approximation offers a compact and accurate description of the spectral response and will be referenced in the analysis of modulation behavior in Section 3.

While the Lorentzian model in (3) describes the differential transmission behavior, Fig. 2.6 (b)

shows the individual transmission spectra of the through and drop ports under two biasing conditions: $V_{\mathrm{rb}} = 0\,\mathrm{V}$ and $V_{\mathrm{rb}} = 5\,\mathrm{V}$. As explained, the employed thermal control circuit locks the ring at a wavelength where the average powers at the through and drop ports are equal, corresponding to identical DC power levels. Since the drop port response is the inversion of the through port, this locking condition ensures that the through and drop outputs are approximately complementary. Consequently, the MRM must operate at a wavelength that satisfies

$$T_T(0V) - T_D(0V) = T_D(-5V) - T_T(-5V) \tag{4}$$

The operating wavelength satisfying (4) is indicated in Fig. 2.6 (b) as λ_{c}.

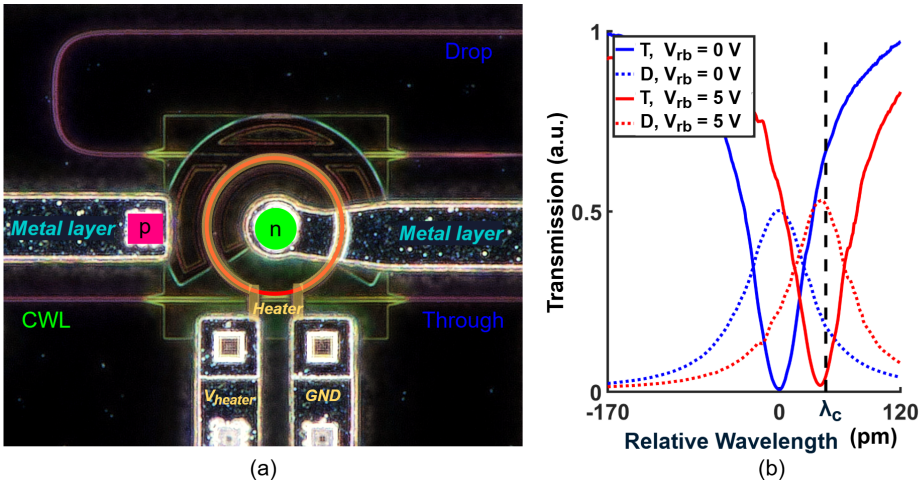

Figure 2.6: (a) Micrograph of the fabricated MRM, and (b) measured transmission spectra at V_{rb} = 0 V and V_{rb} = 5 V, highlighting the operating wavelength λ_{c} for differential logic operation.

The MRM is first characterized by measuring its optical spectrum at 19 ℃ with no applied reverse bias ($V_{\mathrm{rb}} = 0\,V$). From the through-port transmission spectrum at 0 V shown in Fig. 2.6 (b), a FWHM of 70 pm is measured, corresponding to a quality factor (Q) of 22,000. The extinction ratio (ER), measured from the same spectrum, is approximately 23 dB. The measured Q-factor translates into an optical bandwidth, f_{ph}, of approximately 8.75 GHz. As shown in Fig. 2.7 (a), the differential transmission ($T_T - T_D$) is measured for V_{rb} from 0 V to 5 V in 1 V steps. The plot illustrates the resonance shift with V_{rb} and highlights the target operating wavelength, at which the differential

transmission is extracted for each bias level. These values are then used in Fig. 2.7 (b) to analyze the relationship between V_{rb} and $T_T - T_D$, showing a slope of approximately – 0.2 a.u./V within the tested voltage range. Additionally, Fig. 2.7 (c) presents the electro-optic modulation behavior, where the resonance wavelength is tracked as a function of V_{rb}. This characterization yields a tuning slope of approximately 8 pm/V. These results establish the device operating parameters used later in Chapter 3 and 4.

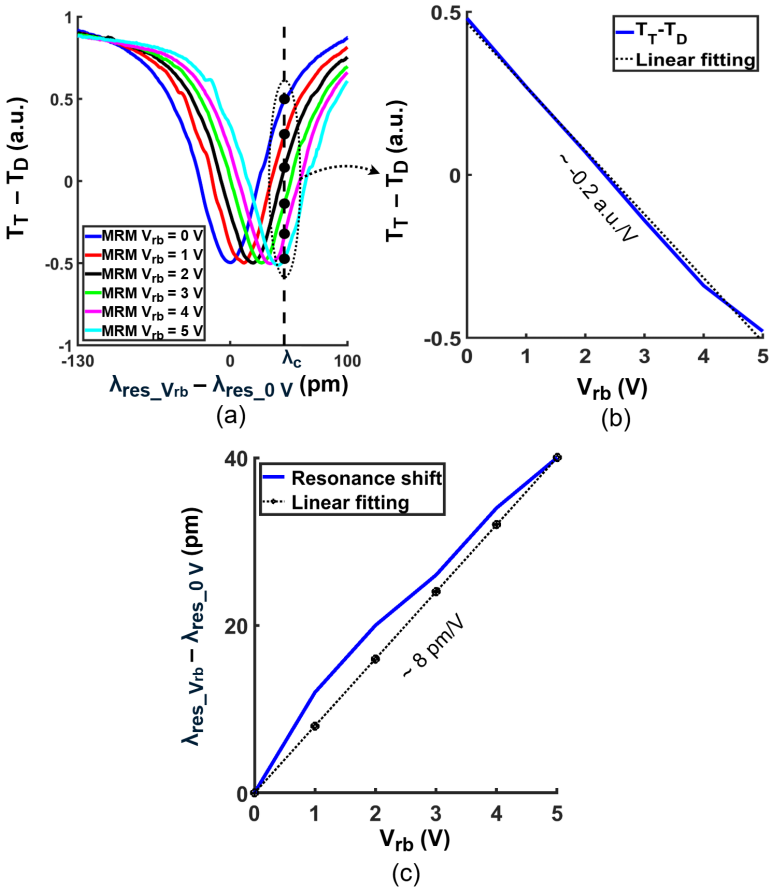

Figure 2.7: (a) Differential optical transmission ($T_T - T_D$) measured for V_{rb} from 0 V to 5 V, showing resonance shift, (b) linear relationship between V_{rb} and differential optical transmission ($T_T - T_D$), (c) electro-optic tuning of the resonance wavelength versus V_{rb}.

2.3 Related Work on Optical Logic Gates

Optical logic gates have been implemented using diverse photonic device platforms, each exploiting distinct physical mechanisms. The primary focus of this section is on MRM-based approaches, which have been studied for their compactness and CMOS compatibility. In parallel, non-MRM structures, such as SOA–MZI and photonic crystal devices, have also been reported. Together, these works illustrate both the potential and the challenges of optical logic design. The following subsections review representative examples from both categories, highlighting their operating principles, architectural assumptions, and integration challenges.

2.3.1 Optical Logic Gate Realization Using Zero-Bias Photonic Structures

As illustrated in Fig. 2.8, [28] proposed a universal all-optical logic gate capable of operating without any electrical power supply. The architecture combines the optical inputs in a multimode interference (MMI) coupler, which forms the central stage of operation. Before reaching the MMI, the signals P_A and P_B pass through thermo-optic phase shifters controlled by voltages V_{C1} and V_{C2}. To realize OR and NOR functions, these phase shifters align the two inputs so that they arrive in phase, ensuring constructive addition inside the MMI. The resulting combined optical power P_m is then delivered to the optical-to-voltage converter (OVC).

The OVC, built from a stack of 16 series-connected zero-biased photodiodes, performs a nonlinear optical-power-to-voltage conversion. The generated voltage (V_m) subsequently drives the MRM. If the ring's resonance aligns with the supply wavelength P_{sup}, the light is dropped and does not reach the output waveguide, corresponding to a logical "0." Otherwise, the light passes through to the output, representing a logical "1." By adjusting the initial resonance condition, the structure can be configured to implement OR or NOR logic, depending on the chosen biasing scheme.

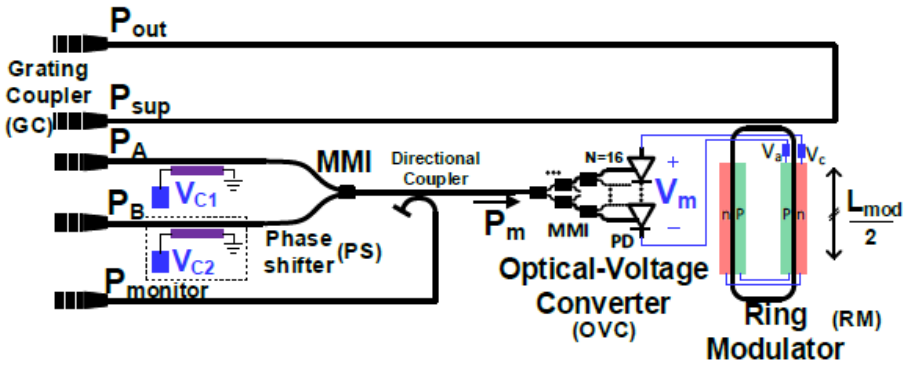

Figure 2.8: Zero-bias PD stack in the optical-to-voltage converter (OVC) used to drive an MRM without external electrical power [27].

To realize logic operations such as OR and NOR, the system exploits the nonlinear relationship between the combined input power P_m and the modulation voltage V_m, which in turn shifts the resonance of the MRM. Fig. 2.9 shows this nonlinear behavior, where the voltage response begins to saturate at higher input powers. As illustrated in Fig. 2.10 (a) and (b), different input combinations (00, 01/10, and 11) correspond to distinct OVC input powers. Based on the nonlinear transfer curve, the resonance shifts for $\lambda_{01/10}$ and λ_{11} are very close to each other, whereas both are clearly separated from λ_{00}. By appropriately choosing the initial detuning of the microring, the logic function can therefore be defined. In the OR configuration (Fig. 2.10 (a)), the ring is tuned such that $\lambda_{00} \approx \lambda_{\text{sup}}$. For the "00" input, the resonance aligns with the supply wavelength and light is dropped, yielding low output power and a logical "0." For any nonzero input (01, 10, or 11), the resonance shifts away, allowing light transmission that corresponds to a logical "1." Conversely, in the NOR configuration (Fig. 2.10 (b)), the ring is initially biased slightly off-resonance. As in the OR case, the phase shifters align the two inputs in phase so that they interfere constructively at the MMI, ensuring the correct combined power is delivered to the OVC. Under this biasing condition, the "00" input yields a logical "1," while all other input combinations shift the resonance toward λ_{sup} and suppress the output, producing a logical "0."

Additional logic functions such as XOR and XNOR can be implemented by adjusting the input phases with the phase shifters V_{C1} and V_{C2}. In this case, destructive interference is enforced at the

MMI combiner, so that the combined power P_m is nonzero only for the "01" and "10" states, while vanishing for "00" and "11." By selecting the initial biasing of the resonance appropriately, XOR or XNOR behavior can then be achieved.

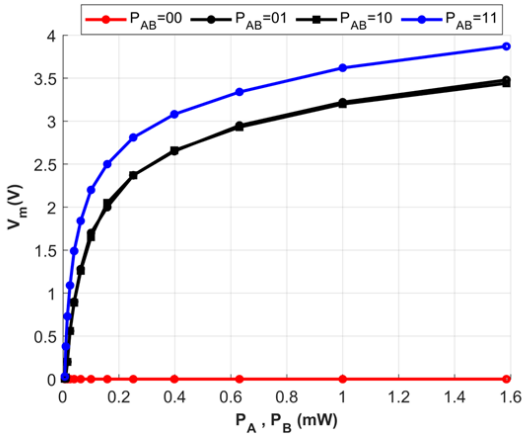

Figure 2.9: Optical power-to-voltage characterization. Measured OVC output voltage as a function of input optical power (P_A or P_B) for different input logic P_{AB} configurations: 00, 01, 10, 11.

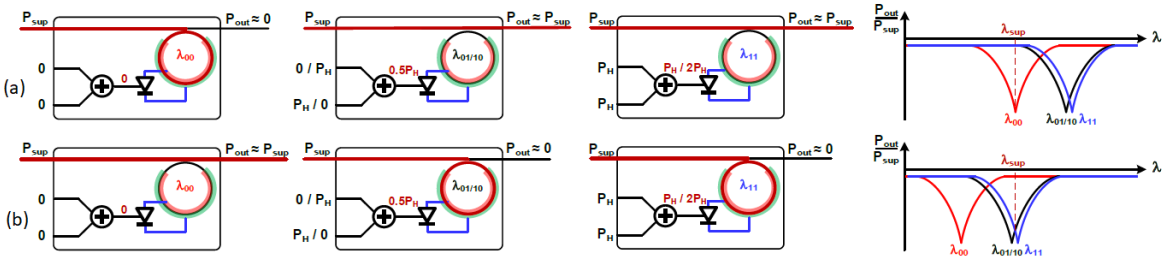

Figure 2.10: Operational principle of the zero-bias optical logic gate [27]. (a) OR gate implementation and (b) NOR gate implementation.

At a high level, the design allows an optical logic gate to operate without any electrical gain. The main practical challenge, however, lies in controlling the phase of the input signals. The thermo-optic phase shifters must be tuned with high precision to ensure that the two inputs arrive at the MMI in the desired phase relation. For OR and NOR gates, the signals must be aligned in phase so that they interfere constructively, whereas for XOR and XNOR, a 180° phase difference must

be enforced to create destructive interference. Any deviation in phase alignment directly alters the combined power at the MMI output, leading to errors in logic functionality and reduced cascadability.

Second, the demonstrated speed is restricted to 10 Mbps [28], primarily due to the slow response of the zero-bias PDs. In photovoltaic mode, the high junction resistance combined with the intrinsic capacitances of the PDs and the MRM produces a large RC time constant on the order of tens to hundreds of nanoseconds. This confines the bandwidth to only a few megahertz. In principle, the OVC could operate in reverse-biased (photoconductive) mode, which would enable drift-dominated transport, reduced resistance, and multi-gigabit per second data rates. However, doing so requires an external electrical supply and an I–V conversion stage, eliminating the self-powered feature that defines the novelty of the zero-bias architecture. Moreover, under reverse bias, the nonlinear power-to-voltage characteristic of the PD stack largely disappears, eliminating the saturating transfer curve that is central to distinguishing between input states. Thus, the speed limitation is not fundamental to photonic integration itself but rather a direct consequence of maintaining zero-bias operation, which simultaneously provides both self-powered functionality and the nonlinear P–V response used for logic realization.

2.3.2 Optical Logic Gate Realization Using Feedback-Controlled PN-Junction Tuning

Reference [21] presents a method for implementing universal optical logic gates (UOLGs) based on the electro-optic tuning of silicon MRMs using feedback from photodetected input signals. The core architecture relies on dynamic tuning of MRM resonances through PN-junction tuning. As illustrated in Fig. 2.11(a), two optical inputs, A and B, are coupled into MRMs A and B, whose resonances are initially biased symmetrically around the operating wavelength λ_0 (shown in the shaded region of Fig. 2.11(a)). A small portion of the transmitted signals is tapped and converted into photocurrents i_A and i_B. The difference current, $i_{\text{diff}} = i_A - i_B$, is amplified by a limiting amplifier (LA1), and the resulting voltage is fed back to modulate the PN junctions of MRMs A and B, dynamically shifting their resonances to enforce the correct logic state.

If $i_{\text{diff}} > 0$, meaning input A is logical “1” and input B is logical “0,” the applied feedback

shifts the resonances of MRMs A and B toward shorter wavelengths, resulting in a deeper suppression at the output of MRM A. Conversely, if $i_{\text{diff}} < 0$, corresponding to input A = "0" and input B = "1," the feedback shifts the resonances toward longer wavelengths, enhancing suppression at the output of MRM B. When the inputs are equal (00 or 11), the difference current vanishes and the resonances remain at their initial bias points. This behavior is only possible with careful initial detuning of MRMs A and B around λ_0, ensuring that the feedback response produces the intended logical outputs. As mentioned earlier, the feedback system also enhances suppression at the outputs corresponding to the logical "0" state and sharpens the transition between "0" and "1" levels, improving the overall contrast of the logical levels.

The remaining optical signals from MRMs A and B are then phase-aligned using a thermo-optic heater located next to the Y-junction combiner and subsequently combined in the Y-junction, whose output effectively performs an OR operation. This stage once again highlights the critical role of phase control. The signals must be aligned in phase so that they interfere constructively at the combiner. Any phase mismatch would degrade the interference contrast and distort the OR functionality. As with other interference-based schemes, this reliance on precise phase alignment represents a practical constraint. Thus, the overall effectiveness of the architecture depends not only on the feedback-controlled resonance tuning of the MRMs but also on maintaining stable phase alignment at the Y-junction.

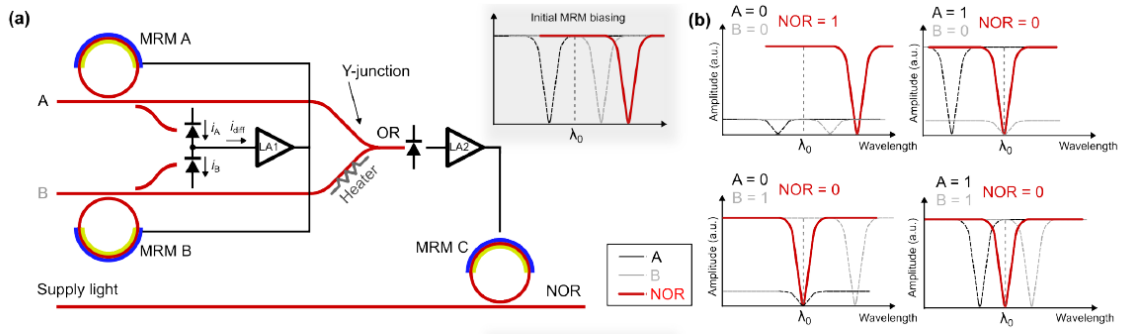

Figure 2.11: PN-junction feedback-based control scheme for implementing optical logic gates using MRMs [20]. (a) Circuit schematic for NOR gate. (b) Operational principle of NOR gate.

To complete the logic function, a third MRM (MRM C) is introduced, which is initially biased slightly off-resonance and supplied with a constant optical input. Its resonance is controlled by the output of the Y-junction after detection and amplification via LA2. When the combined output of the Y-junction corresponds to a logical "0," the resonance of MRM C remains unchanged, allowing the supply light to pass through and producing a logical "1" at the output. Conversely, when the Y-junction output is logical "1," the applied voltage shifts the resonance of MRM C toward shorter wavelengths, bringing it into alignment with the input laser. As a result, the supply light is dropped, and the output of MRM C becomes logical "0." In this way, MRM C functions as an optical inverter, and the combination of the OR output with this inversion yields the NOR function.

In addition to demonstrating NOR logic, the paper also shows that by initially biasing MRMs A and B in an alternative configuration, summing their photocurrents instead of differencing them, and adjusting the thermo-optic heater in one arm of the Y-junction, an optical AND function can be realized. Applying the same inversion stage to this output then yields a NAND gate.

In this work, no physical MRMs were fabricated; instead, a single UOLG was implemented on a programmable mesh of 2×2 Mach–Zehnder interferometers (MZIs) configured to emulate MRM behavior. The full SR latch, comprising two cross-coupled gates, was not realized experimentally but only demonstrated through software simulation on a larger photonic mesh. Another important consideration is the logic control circuitry, particularly the limiting amplifiers (LA1 and LA2) that generate the feedback signals. These amplifiers were not realized on-chip or on-board; rather, their behavior was emulated entirely in software. The paper does not provide detailed electrical specifications for these components, such as gain, bandwidth, or noise performance, making it difficult to evaluate the feasibility of a fully integrated hardware implementation.

In summary, Reference [21] presents a promising conceptual framework for scalable optical logic, supporting universal operations and enabling more complex functions such as optical latches. However, accurate phase alignment remains the critical challenge, since the heater before the Y-junction must be finely adjusted to guarantee the inputs combine in the proper phase. In addition, each gate requires three MRMs, all of which must be accurately biased, leading to increased area and higher control complexity if implemented on a photonic circuit.

2.3.3 Non-MRM-Based Structures

Beyond MRM-based implementations, several alternative device platforms have been investigated for realizing OLGs. These approaches exploit different physical mechanisms, offering distinct advantages and challenges compared to MRM-based architectures.

Quantum-Dot SOA-MZI Based Logic Gates

Reference [11] proposed an ultrafast all-optical NOR gate using a MZI with quantum-dot semiconductor optical amplifiers (QDSOAs). Compared to bulk or quantum-well SOAs, QDSOAs provide shorter carrier relaxation times, higher saturation power, lower noise figure, and improved temperature stability.

As shown in Fig. 2.12, data signals A and B are combined and injected into one QDSOA through a wavelength-selective coupler (WSC), while the clock signal (a constant stream of logical "1") is directed into the other. A CW probe is split by a 3 dB coupler and sent into both arms, with all inputs assigned distinct wavelengths. When the data or clock signals are present, they saturate the QDSOAs, changing the carrier density and refractive index, which shifts the phase of the CW probe.

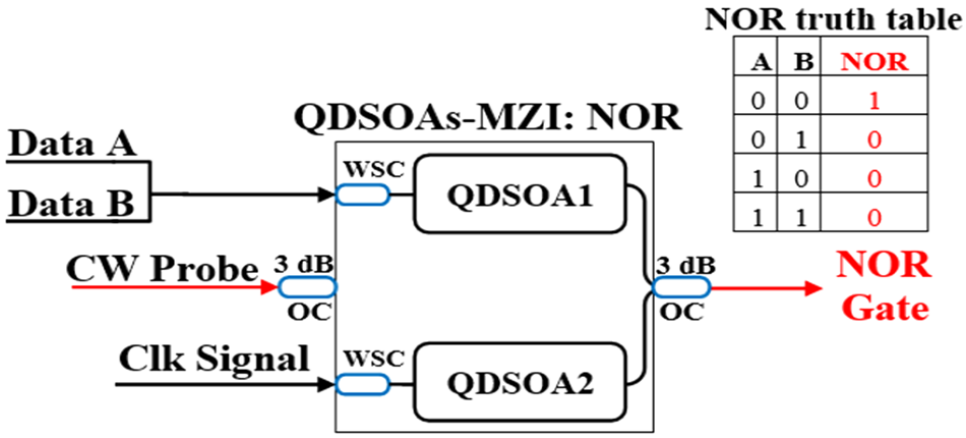

Figure 2.12: QDSOA–MZI based all-optical NOR gate with corresponding truth table [11].

The MZI is initially biased at destructive interference. For input "00," only the clock arm is saturated, producing a phase imbalance that results in constructive interference and a logical "1" at the output. For inputs "01," "10," or "11," both arms are saturated, so the probe beams remain

phase-aligned and recombine destructively, yielding logical “0.” This realizes the NOR operation.

The CW probe is distinguished from the control signals (A, B, Clk) by both power and wavelength. The control beams are launched with higher power to drive QDSOA saturation, while the probe is kept weak so that it only experiences the induced phase shift.

This work was validated through simulation. In practice, implementation would require a phase shifter to accurately bias the interferometer arms, as well as electrical biasing for the two QDSOAs used in each gate. Furthermore, the scheme depends on separate wavelengths for A, B, Clk, and the CW probe, which complicates the system. Overall, this approach demonstrates ultrafast operation and improved carrier dynamics over bulk and quantum-well SOAs, but at the expense of higher device and system complexity.

Photonic Crystal Logic Gates Based on the Kerr Effect

Reference [29] presented an all-optical AND gate based on a two-dimensional photonic crystal (PhC) ring resonator structure exploiting the nonlinear Kerr effect. The device consists of GaAs dielectric rods arranged in air, where the intensity-dependent refractive index variation enables nonlinear switching. The overall structure is shown in Fig. 2.13.

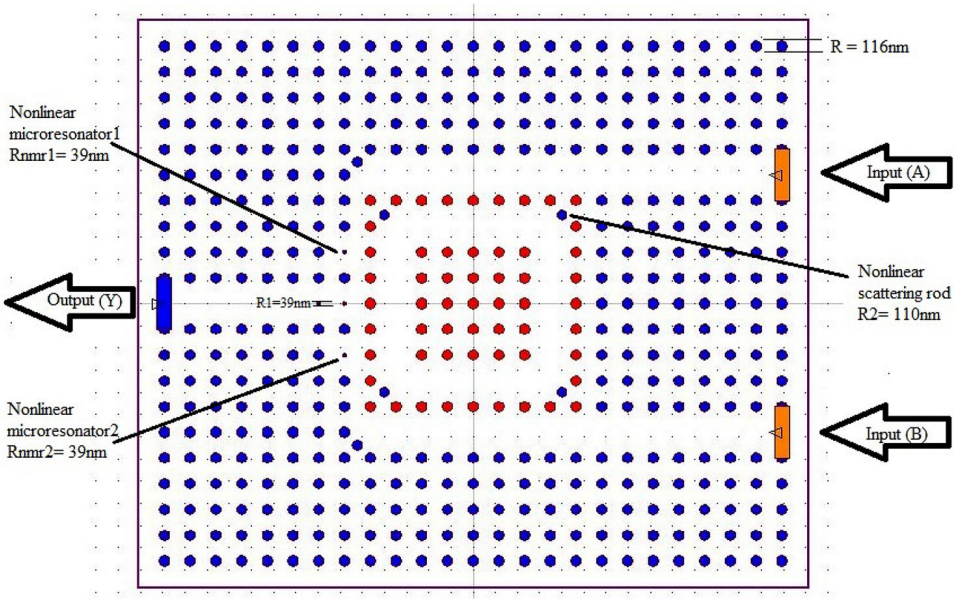

Figure 2.13: Schematic of the Kerr-effect-based photonic crystal AND gate structure [29].

The main element is the central PhC ring resonator (red rods), where the Kerr nonlinearity causes an intensity-dependent index change that shifts the resonance. Inputs A and B are injected through waveguides on the right. With only one input active, the resonance shift is too small for significant transmission, so the output remains low. When both inputs are present, the higher combined intensity produces a sufficient resonance shift, enabling strong transmission at the output port, thus realizing the AND function. Two nonlinear scattering rods (radius 110 nm), together with two auxiliary microresonators (radius 39 nm) near the output waveguide, serve as supporting features that improve coupling efficiency and enhance the output contrast ratio.

This structure achieves a compact footprint and picosecond-scale response. Its main limitations are the relatively high switching power, sensitivity to material nonlinearities, and a lack of optical signal regeneration, which limits large-scale deployment.

2.4 Logic control circuit components

While the previous section discussed two MRM-based optical logic gate implementations, both rely on simplified or emulated logic control schemes. In contrast, the present approach uses a dedicated electrical logic control circuit to interface with photodetected signals and drive the MRMs. These photocurrents are generated by PDs integrated within the PIC. This block typically performs two key functions: (1) it receives the input signals as photocurrents and processes them, acting as an optical receiver, and (2) it generates the electrical signals needed to modulate the MRMs, acting as a modulator driver.

Fig. 2.14 presents a high-level block diagram of the logic control circuit, highlighting three essential building blocks commonly used for optical-to-electrical conversion and signal control: I–V conversion stages, main amplifiers (MAs), and DC offset compensation (DCOC) circuits. To understand the functional requirements of such a circuit, it is helpful to examine these core components, which are described in the following subsections.

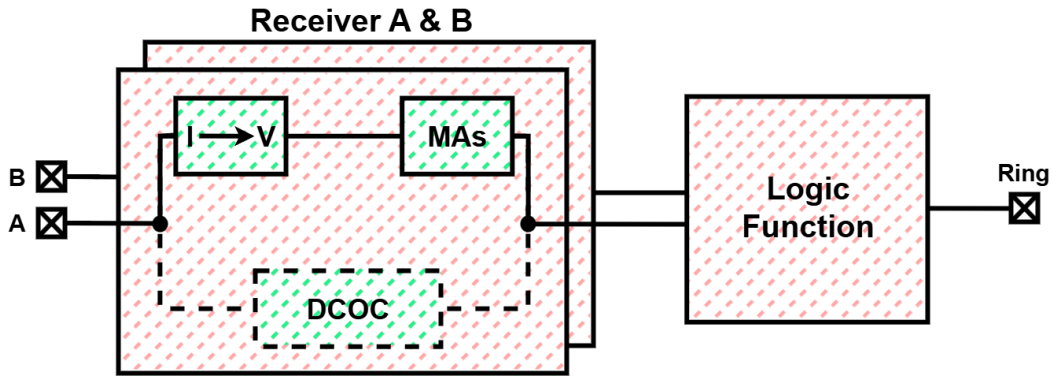

Figure 2.14: Overall block diagram of the logic control circuit, illustrating its key functional components

2.4.1 I-V Conversion Circuits

In optical logic systems, the photocurrent generated by PDs should be converted into voltage signals for further electronic processing. This conversion is typically performed by an I-V conversion circuit. This circuit is a crucial building block in any optical system. An I-V conversion circuit serves the dual purpose of converting photocurrent to voltage, and amplifying the signal to levels suitable for post-amplification or logic control.

The first and simplest approach for converting photocurrent to voltage in optical front-ends is the use of a resistor [30]. As it is illustrated in Fig. 2.15, the PD is directly connected to a load resistor R_C, and the voltage is given by:

$$V_{\text{IN}} = I_{\text{PD}} \times R_C \tag{5}$$

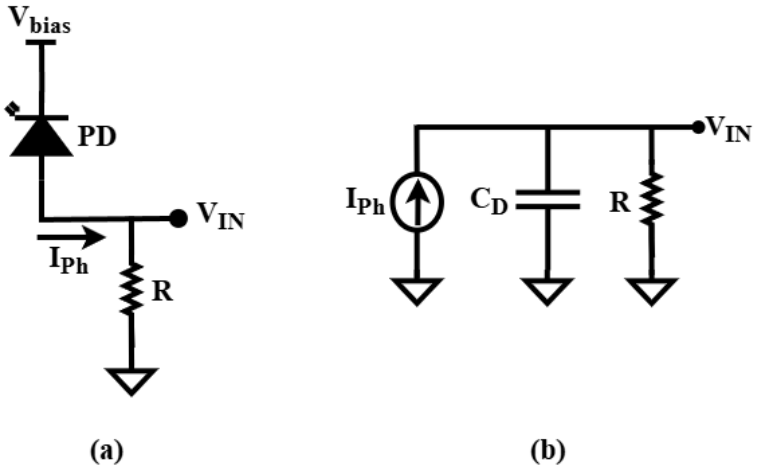

Figure 2.15: Resistor-based I–V conversion: (a) circuit schematic and (b) AC small-signal model.

While this topology offers simplicity, it suffers from a fundamental trade-off between gain and bandwidth. The load resistor, together with the total input capacitance C_D (including PD junction capacitance and pad parasitics), forms a first-order low-pass filter. The resulting 3-dB bandwidth is given by:

$$f_{3\,\mathrm{dB}} = \frac{1}{2\pi R_C C_D} \tag{6}$$

Combining the two equations shows that increasing R_C improves voltage gain but simultaneously reduces bandwidth:

$$\text{Gain} = R_C \quad \text{and} \quad \text{Bandwidth} \propto \frac{1}{R_C} \tag{7}$$

This inverse linear relationship between gain and bandwidth limits the suitability of this approach in high-speed optical systems. However, its simplicity makes it attractive in low-speed or proof-of-concept scenarios, or in cases where the total capacitance is very small—such as in monolithic integration where pad capacitance is eliminated.

A minimal optical logic gate can also be envisioned by directly connecting a PD, a load resistor, and an MRM, as illustrated in Fig. 2.16. In this system, the photocurrent generated by the PD is converted to a voltage across R_C, which directly drives the MRM and shifts its resonance. The bandwidth is limited by the RC time constant of the load resistance and the total capacitance at the

node:

$$f_{\text{3dB}} = \frac{1}{2\pi R_C \left(C_{PD} + C_{MRM} + C_{pad}\right)}. \tag{8}$$

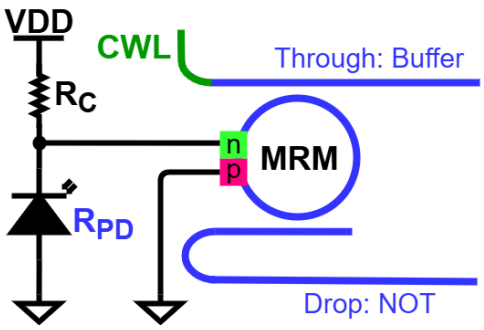

Figure 2.16: Minimal OLG using PD, resistor R_C, and MRM.

Here, both the PD junction capacitance and the intrinsic capacitance of the MRM contribute to the effective load capacitance. If the resistor is implemented on-chip inside the PIC, then the total capacitance is limited to $C_{PD} + C_{MRM}$, and the speed can be improved. However, if an off-chip resistor is used, the additional pad capacitance C_{pad} must be included in the total load, which further reduces the achievable bandwidth and makes the RC trade-off even more restrictive.

The operating voltage across the MRM depends on the input photocurrent I_{PD}. When the input optical power is high, the current is large, and the node voltage approaches

$$V_{\text{mod,L}} \approx VDD - R_C \times I_{PD,H} \tag{9}$$

while for low input optical power, the current is small and the node voltage rises toward

$$V_{\text{mod,H}} \approx VDD - R_C \times I_{PD,L} \tag{10}$$

where $I_{PD,H}$ and $I_{PD,L}$ represent the photocurrents under high and low input levels, respectively. These two levels determine the effective modulation swing applied to the MRM.

In general, the modulation voltage swing can be expressed as

$$V_{\text{mod}} = I_{\text{PD,p-p}} \times R_C \tag{11}$$

where $I_{\text{PD,p-p}}$ is the peak-to-peak photocurrent corresponding to the optical input. As shown in (9) and (10), the first inversion occurs in the I–V conversion stage, while the second inversion is introduced by the MRM itself due to the negative slope of the resonance curve when the operating point lies on the right side of the resonance (see Fig. 2.7 (b)). To ensure that the modulation swing between these levels is sufficient for proper logic operation, a relatively large R_C is required. As a result, the through port realizes a buffer function, whereas the drop port provides the complementary NOT function.

In addition, the value of R_C must also exceed a certain minimum threshold to ensure a minimum optical gain magnitude of unity, i.e., $|\text{Gain}| \geq 1$. A detailed explanation and derivation of this condition, along with numerical estimates for the fabricated device, will be presented in Section 3.1.1.

Overall, the appropriate choice of R_C depends on several design factors, including the input optical signal levels, the amplitude of the desired modulation voltage, the supply voltage VDD, the required optical gain, and the targeted speed of operation.

For example, if we assume an input optical power swing of $35\,\mu$W (with low and high levels of $5\,\mu$W and $35\,\mu$W, respectively), the corresponding photocurrent swing is $I_{\text{PD,p-p}} = 28\,\mu$A ($I_{PD,L} = 4\,\mu$A, $I_{PD,H} = 32\,\mu$A). With a supply voltage of $V_{DD} = 5\,$V, and assuming a desired modulation amplitude of approximately $4\,$V, the required resistance is $R_C = 4/(28 \times 10^{-6}) \approx 143\,\text{k}\Omega$. Under these conditions, the modulation levels are approximately $V_{\text{mod,L}} \approx 0.4\,$V and $V_{\text{mod,H}} \approx 4.4\,$V, providing the desired $4\,$V swing.

To evaluate the bandwidth, we use (8). With capacitances of $C_{MRM} = 30\,$fF and $C_{PD} = 30\,$fF, the total capacitance for the on-chip case is $C_{\text{on-chip}} = 60\,$fF, which yields a 3-dB frequency of $f_{\text{3dB,on-chip}} \approx 18.6\,$MHz. If the resistor is implemented off-chip, the additional pad capacitance of $C_{pad} \approx 150\,$fF increases the total capacitance to $C_{\text{off-chip}} \approx 210\,$fF, resulting in lower bandwidth of $f_{\text{3dB,off-chip}} \approx 5.3\,$MHz.

This PD–resistor–MRM configuration represents an extremely simple architecture, and demonstrates the feasibility of a nearly all-optical logic gate. However, the severe speed limitation due to

the RC trade-off, limited modulation swing, and strong dependence on optical input levels are the main challenges of this structure.

Returning to I–V conversion structures, the gain–bandwidth trade-off inherent in resistor-based implementations can be mitigated by employing transimpedance amplifiers (TIAs) in high-speed optical systems. One approach is to incorporate active feedback, which lowers the input impedance seen by the PD, thereby minimizing RC delay and avoiding the bandwidth limitations imposed by the PD's parasitic capacitance. This enables high transimpedance gain and wide bandwidth, making TIAs well-suited for fast and energy-efficient signal processing.

Among various TIA implementations, inverter-based architectures are particularly attractive in modern CMOS optical receivers. These designs leverage high-gain CMOS inverters, offering high transconductance, rail-to-rail output swing, and excellent compatibility with low-voltage operation in a compact form factor [30]. As a result, inverter-based shunt-feedback TIAs have become a popular choice for high-speed, low-power front-ends, providing an efficient interface between the PD and subsequent circuits in optical receivers.

The schematic of a CMOS inverter-based shunt feedback TIA is shown in Fig. 2.17 (a). When $I_{\text{in}} = 0$, the input and output voltages of the inverter are equal, i.e., $V_{\text{In}} = V_{\text{Out}}$. This defines the operating point of the TIA in an inverter-based shunt-feedback configuration. To analyze the frequency response of the TIA, its AC small-signal model, shown in Fig. 2.17 (b), is considered. This model captures the dominant parasitic capacitances and resistances, enabling analytical evaluation of the amplifier's frequency-dependent behavior. The circuit parameters are defined as follows:

$$g_m = g_{m1} + g_{m2} \tag{12}$$

$$R_0 = r_{o1} \parallel r_{o2} \tag{13}$$

$$C_I = C_{\text{gs1}} + C_{\text{gs2}} + C_{\text{D}} \tag{14}$$

$$C_O = C_{\text{db1}} + C_{\text{db2}} + C_L \tag{15}$$

$$C_F = C_{\text{gd1}} + C_{\text{gd2}} \tag{16}$$

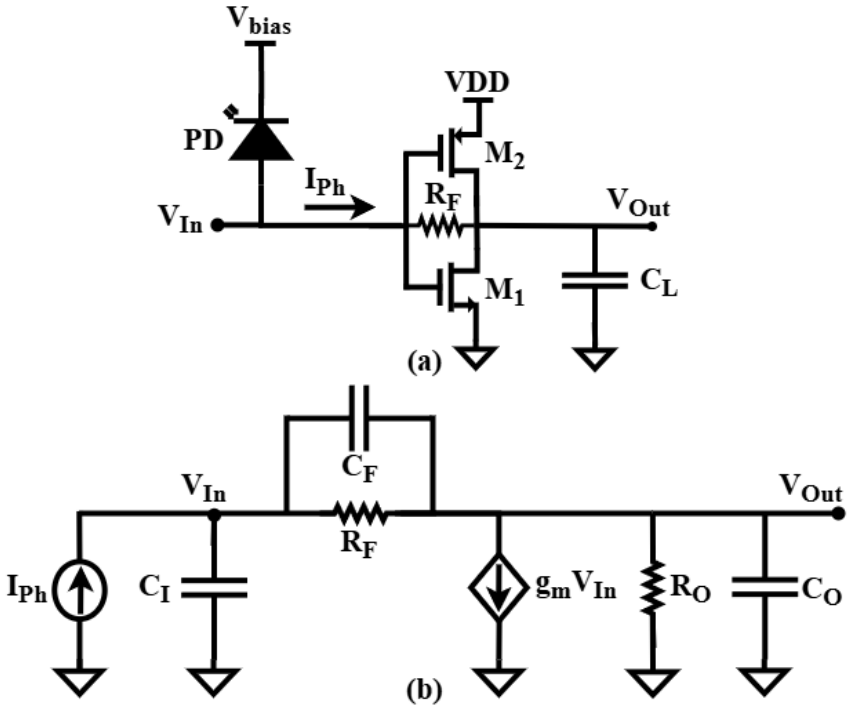

Figure 2.17: CMOS inverter-based TIA: (a) circuit schematic and (b) small-signal model.

The transfer function from the input current of the small signal I_{IN} to the output voltage V_{Out} is expressed as [31]:

$$\frac{V_o}{I_{\text{in}}} = \frac{(R_F C_F s + 1 - g_m R_F) R_O}{R_F R_O C s^2 + [R_F(1 + g_m R_O) C_F + (R_F + R_O) C_I + R_O C_O]\, s + 1 + g_m R_o} \tag{17}$$

where $C = C_I C_O + C_I C_F + C_O C_F$.

Assuming C_F is smaller than the other parasitic capacitances and contributes minimally to the frequency response, the expression simplifies to:

$$\frac{V_{Out}}{I_{\text{In}}} = \frac{(1 - g_m R_F) R_O}{R_F R_O C_I C_O s^2 + [(R_F + R_O) C_I + R_O C_O]\, s + 1 + g_m R_O} \tag{18}$$

At low frequencies, the gain can be approximated by:

$$\frac{V_{Out}}{I_{\text{In}}} = \frac{1 - g_m R_F}{1 + g_m R_O} R_O \tag{19}$$

The input resistance is given by:

$$R_{\text{in}} = \frac{R_F + R_o}{g_m R_o + 1} \approx \frac{1}{g_m} \tag{20}$$

Assuming $g_m R_F \gg 1$ and $g_m R_o \gg 1$, the transimpedance gain simplifies to:

$$\frac{V_O ut}{I_{\text{In}}} \approx -R_F \tag{21}$$

Finally, to evaluate the time-domain behavior, the natural frequency of the system is given by:

$$\omega_n = \sqrt{\frac{1 + g_m R_O}{R_F R_O C_I C_O}} \tag{22}$$

Based on the above analysis, it can be concluded that the inverter-based shunt-feedback TIA maintains a transimpedance gain approximately equal to R_F, assuming $g_m R_F \gg 1$. However, unlike the resistor-based I–V conversion where the bandwidth is directly proportional to $1/R_F$, in this active configuration the bandwidth is proportional to:

$$\text{Bandwidth} \propto \frac{1}{\sqrt{R_F}} \tag{23}$$

This indicates that in the inverter-based topology, the bandwidth decreases only slowly with increasing feedback resistance, offering a much more favorable trade-off than the linear inverse dependency of the resistor case. Nonetheless, another interpretation of this relationship is that further doubling the bandwidth would require a quadratic reduction in the gain [32]. This shows the fundamental limit on the gain for a given bandwidth.

2.4.2 Main Amplifiers (MAs)

In high-speed optical receiver systems, the TIA performs the critical task of converting photocurrent to voltage. However, due to its gain-bandwidth trade-off, the TIA alone is typically insufficient to produce voltage levels large enough to reliably drive digital logic stages or comparators. Therefore, one or more main amplifier stages are added following the TIA to further boost the signal

amplitude.

The primary objective of these main amplifiers is to significantly increase the signal amplitude while maintaining an acceptable bandwidth. However, amplifier design is also constrained by the same fundamental trade-off: as the gain of an amplifier increases, its bandwidth generally decreases. This gain-bandwidth trade-off becomes more pronounced when multiple amplifier stages are cascaded, as each stage contributes to the overall frequency response. To mitigate excessive bandwidth degradation in such cascaded configurations, careful circuit techniques, such as employing feedback mechanisms, are often necessary.

To address this, a popular approach is the inverter-based Cherry–Hooper amplifier. Like a shunt feedback inverter-based TIA, this architecture also uses CMOS inverters. As shown in Fig. 2.18 (a), the Cherry–Hooper structure consists of two stages: a transconductance stage that performs voltage-to-current conversion, followed by a transimpedance stage that converts current back to voltage. The use of local feedback in the second stage significantly lowers the impedance at both the intermediate and output nodes. As a result, the associated pole frequencies are pushed much higher compared to a conventional common-source amplifier with a load resistance equal to R_F. This makes the Cherry–Hooper structure well-suited for high-speed applications.

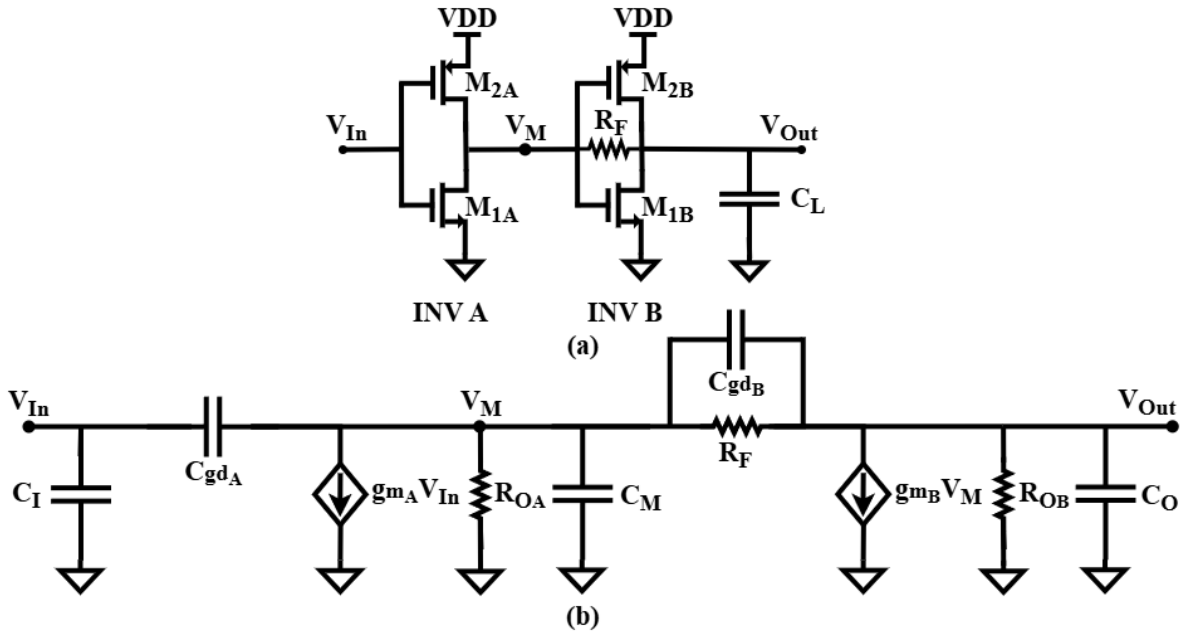

Figure 2.18: Cherry–Hooper amplifier used as a main amplifier stage: (a) circuit schematic and (b) small-signal model.

The AC small-signal equivalent model of the amplifier is shown in Fig. 2.18 (b). To simplify the analysis, the gate-to-drain capacitance (C_{gd}) of the MOSFETs is neglected, and the transistor dimensions are assumed to be equal; that is, $W/L_{(\text{M1A})} = W/L_{(\text{M1B})}$ and $W/L_{(\text{M2A})} = W/L_{(\text{M2B})}$.

The relevant circuit parameters are defined as [30]:

$$g_{mA} = g_{mB} = g_m = g_{m1} + g_{m2} \tag{24}$$

$$R_{OA} = R_{OB} = R_O = r_{o1} \parallel r_{o2} \tag{25}$$

$$C_M = C_{\text{gs1}B} + C_{\text{gs2}B} + C_{\text{db1}A} + C_{\text{db2}A} \tag{26}$$

$$C_O = C_{\text{db1}B} + C_{\text{db2}B} + C_L \tag{27}$$

The overall voltage transfer function of the amplifier is given by:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{g_m(g_m R_F - 1)R_O}{R_F R_O C_M C_O s^2 + (R_F + R_O)(C_M + C_O)s + g_m R_O + \frac{R_F}{R_O} + 2} \tag{28}$$

From this expression, the natural frequency ω_n can be derived as:

$$\omega_n = \sqrt{\frac{g_m R_O + \frac{R_F}{R_O} + 2}{R_F R_O C_M C_O}} \tag{29}$$

The low-frequency voltage gain of the amplifier is expressed as:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -g_m \cdot \frac{g_m R_F - 1}{g_m R_O + \frac{R_F}{R_O} + 2} \cdot R_O \tag{30}$$

Under the assumption that $g_m R_F \gg 1$ and $g_m R_O \gg 1$, the transimpedance gain simplifies to:

$$Z_T \approx g_m R_F \tag{31}$$

This analysis highlights the effectiveness of the Cherry–Hooper topology in providing amplification with manageable gain and bandwidth trade-offs, making it a practical choice for integration in optical systems. To achieve sufficient overall gain, post-amplifiers typically employ multiple amplification stages. However, increasing the number of stages also raises power dissipation and noise. As a practical compromise, most designs limit post-amplifiers to three or four stages [30].

2.4.3 DC Offset Compensation (DCOC)

In mixed-signal and optical front-end circuits, particularly those interfacing analog signals with digital logic or modulators, maintaining a stable DC operating point is essential. In optical receivers, the dominant source of DC offset is the average photocurrent generated by the PD. DCOC circuits are primarily used to compensate for this input DC current, ensuring that the signal remains centered around a defined level, typically near the switching threshold of the subsequent circuitry. In addition, DCOC circuits help prevent baseline drift caused by device mismatch, charge accumulation, and variations in threshold voltages. If left uncompensated, these effects can lead to signal clipping,

reduced dynamic range, or saturation in downstream stages.

Fig. 2.19 illustrates a typical inverter-based single-ended DCOC circuit used in optical front-end systems. As shown in this figure, the conventional DCOC approach uses a low-pass filter and a feedback loop to regulate the signal's DC level. The loop continuously extracts the average of the output voltage and compares it to a reference level, typically $V_{\mathrm{REF}} = V_{\mathrm{DD}}/2$, generating a correction current that gradually shifts the baseline. This approach assumes that the input data stream is statistically balanced (i.e., equal probability of logical '1's and '0's), so that the average value corresponds to the midpoint (intended baseline). Fig. 2.20 illustrates this concept using a pseudo-random signal with 50% logical '1's. The red line indicates the average of this signal, which coincides with the midpoint of the waveform (black line).

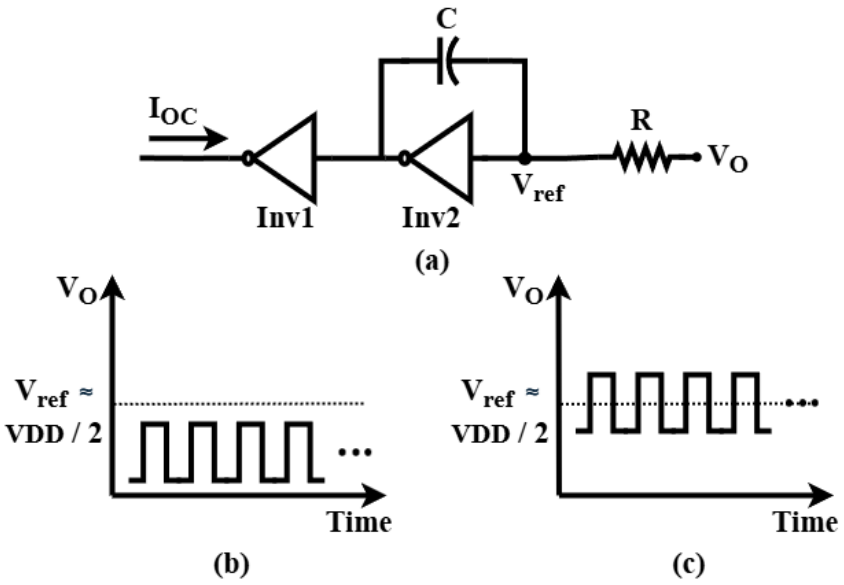

Figure 2.19: Inverter-based DCOC circuit with low-pass filtering and feedback loop. (a) Circuit schematic with compensation current I_{OC} used to stabilize the baseline. (b) Output voltage V_O without DCOC, showing baseline drift. (c) Output voltage V_O with DCOC, showing corrected baseline around $V_{\mathrm{DD}}/2$.

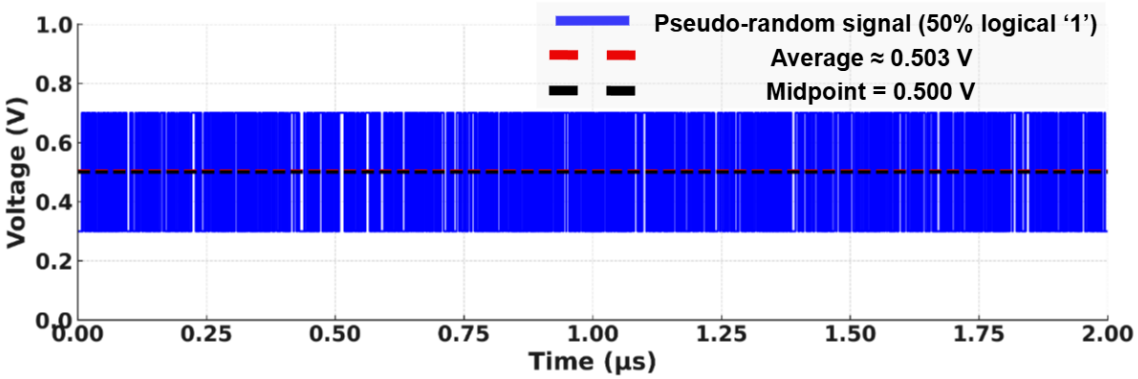

Figure 2.20: Pseudo-random signal between 300 mV and 700 mV with 50% logical '1'. The black dashed line shows the midpoint (0.50 V) and the red dashed line the average (0.503 V).

The output voltage V_O is low-pass filtered and compared to V_{REF}. The resulting error signal generates a compensation current I_{OC}, which is fed back to the input of the inverter-based TIA. This low-frequency feedback loop corrects slow drifts in the operating point without disturbing high-speed signal components [33]. The output is thus centered around V_{REF}, improving linearity and ensuring reliable logic-level detection.

Although the implementation requires relatively large resistance and capacitance values for effective low-pass filtering, these components are compatible with standard CMOS processes and support a compact, fully integrated design. The DCOC loop also enhances robustness to process variation and slow dynamic changes in the optical input signal. Fig. 2.19 (b) and (c) illustrate the impact of DCOC on the output voltage V_O of an inverter-based circuit. In Fig. 2.19 (b), without DCOC, the baseline of V_O drifts over time due to asymmetries in the signal, causing the output to deviate from the ideal midpoint $V_{\mathrm{DD}}/2$. This drift can lead to signal distortion or logic errors in downstream stages. In contrast, Fig. 2.19 (c) shows the effect of enabling DCOC, where a low-pass filtered feedback loop continuously adjusts the bias to keep the signal centered around $V_{\mathrm{DD}}/2$, thereby improving signal symmetry and reliability.

However, this method becomes ineffective when the input data is unbalanced or pattern-dependent, as is common in optical logic systems. In such cases, the average value deviates from the true baseline, leading the DCOC loop to inject an incorrect correction. This can degrade the logic signal

or shift it outside the modulator's operating range. This issue highlights the need to improve the DCOC block to ensure stable operation under data-dependent conditions.

2.5 Conclusion

This chapter established the context for optical logic gate design using MRMs by reviewing their fundamental operation and key configurations. It then examined prior work on MRM-based logic gates, highlighting common challenges in cascadability and control. The focus then shifted to the logic control block, detailing essential components such as transimpedance and main amplifiers, as well as DC offset compensation circuits. These components, commonly used in receiver front-ends, form the core of the logic control circuitry and are essential for ensuring stable and scalable logic operation.

Chapter 3

Design and Realization of a 2×2 Optical Switch Using Cascadable Optical Logic Gates

This chapter presents Phase I of the project, which focuses on the design and experimental realization of a 2×2 optical switch constructed from cascadable optical logic gates. The system comprises a PIC incorporating MRMs with PN junctions and integrated heaters, waveguides, and PDs; a thermal control circuit that stabilizes the microring resonances; and a logic control circuit that interfaces with the photonic components to perform the required logic processing. As discussed in Chapter 2, the PIC and thermal control circuit were developed by other members of the research team and are described there for context. The primary focus of this chapter is the design and implementation of the logic control circuit, along with the integration and experimental evaluation of the complete 2×2 optical switch system.

3.1 Optical Logic Gate Design and Characterization

This chapter details MRM-based OLGs, starting with a cascadable optical NOT gate and extending to a universal NAND gate.

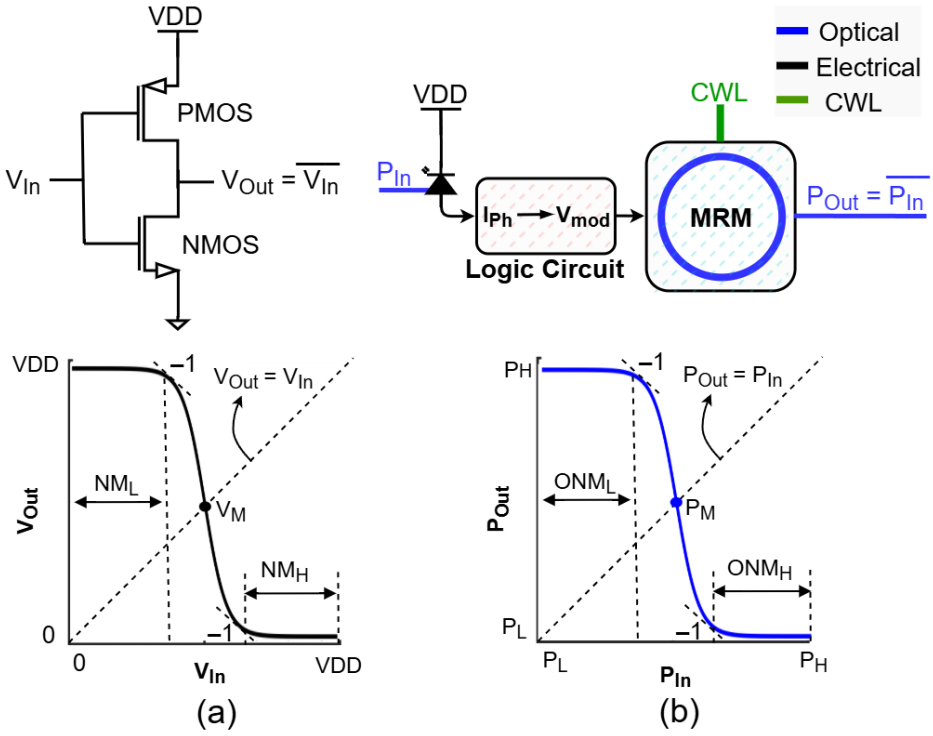

Figure 3.1: (a) Schematic of a conventional digital NOT gate, showing the VTC and noise margins; (b) conceptual schematic of an optical NOT gate, illustrating the PTC and its associated ONMs.

3.1.1 Cascadable Optical NOT Gate Design

Fig. 3.1 (a) shows a conventional CMOS inverter along with its voltage transfer characteristic (VTC) and associated noise margins [34]. The VTC defines the relationship between input and output voltages, exhibiting a steep transition region around the switching threshold. The switching threshold (V_M) is defined as the point on the VTC where the input voltage equals the output voltage. It marks the transition boundary between logic '0' and logic '1'. This steep transition region enables logic-level regeneration and noise rejection. From the VTC curve, two critical noise margins, $\mathrm{NM_L}$ and $\mathrm{NM_H}$, are extracted, representing the maximum tolerable noise for reliable logic 0 and 1 states. These margins are identified at the points where the slope of the VTC equals –1 and are used to assess logic stability in cascaded digital systems.

The regenerative property of the VTC not only ensures reliable logic restoration but also enables cascadability and scalability, as multiple inverter stages can be connected without cumulative signal degradation. This characteristic is fundamental to the widespread use of CMOS logic in large-scale

digital systems.

Building on this foundation, we introduce the structure of our optical inverter. Fig. 3.1 (b) shows the conceptual architecture, where an MRM is employed as the central element for optical signal modulation. A PD converts optical input into electrical current, which feeds into a logic control circuit that determines the modulation state of the MRM. As shown earlier in Fig. 2.7, when the operating wavelength is locked on the right side of the resonance, the transmission exhibits a negative slope with respect to the applied modulation voltage. In this regime, increasing the modulation voltage decreases the output optical power, thereby enabling inversion. In addition, the electrical logic control circuit provides the necessary gain and saturation levels. This configuration implements a NOT gate at the optical level.

The logic control circuit handles signal regeneration by interpreting the detected electrical signal and applying a reverse-bias modulation voltage (V_{mod}) to drive the MRM, regenerating a new optical output. We selected a 5 V reverse-bias modulation voltage because it provides sufficient resonance shift and optical output contrast in the MRM, as will be explained and demonstrated in the following section. Additionally, this value aligns with the 5 V supply voltage of the logic control circuit, eliminating the need for voltage-level conversion and simplifying the overall system design. This modular structure supports scalability, as larger optical networks can be built by cascading identical gates without cumulative signal degradation.

As also shown in Fig. 3.1 (b), analogous to the VTC in electronic inverters, we define the PTC for the optical inverter, which relates the optical output power to the optical input power. Unlike the VTC, which is expressed in volts, the PTC is measured in units of power (watts). This representation captures how changes in optical input signals affect the inverter's output response. As with its electronic counterpart, the slope of the PTC is used to define the ONMs, which quantify the system's tolerance to fluctuations in optical input power. This analogy enables a rigorous analysis of the optical inverter's behavior and its suitability for cascaded logic applications.

To explain the concept of the proposed OLG, we focused on a single-ended optical inverter that uses a single output port to represent logic levels. Alternatively, as explained in chapter 2, a double-bus MRM configuration, providing complementary optical power levels at the through and drop ports, can be used to implement differential OLGs; In cascaded OLG systems, this configuration

allows the downstream logic control circuit to process complementary optical inputs, where a simple subtraction effectively cancels out the common DC component. As a result, no additional baseline correction circuitry is needed, simplifying the design while ensuring proper logic interpretation in successive stages. This property is particularly beneficial when the output of one OLG directly drives the input of the next, supporting scalable and reliable optical logic systems.

To demonstrate how the MRM can be integrated into a functional optical logic gate, we now analyze a cascadable optical inverter configuration. This design incorporates the previously characterized MRM, PDs, and a simplified logic control circuit. The goal is to provide a theoretical framework that captures the key relationships between optical input signals, the resulting modulation voltage, and the differential optical output power. As illustrated in Fig. 3.2, the circuit uses resistors for current-to-voltage conversion. These are followed by a subtractor with unity gain, which processes the through and drop signals to eliminate the DC component and generate the differential signal. As shown in Fig. 3.2, the output of the control circuit drives the n-type side of the junction, consistent with the previously defined biasing convention. To maintain reverse-biased operation, the modulation signal must swing between GND and VDD and be centered around VDD/2. No active electrical amplification is considered, and the only electrical gain is provided by the resistors. The dashed area in the figure contains the unity-gain subtractor and summation blocks; the output voltage of this area is constrained to remain within the GND to VDD range. Based on these assumptions, the relationship between differential input power and modulation voltage (V_{mod}) is given by:

$$V_{\text{mod}} = \left[R_{\text{PD}} \times R_{\text{C}} \times (P_{\text{In}} - \overline{P_{\text{In}}})\right] + \frac{VDD}{2} \tag{32}$$

where P_{In} and $\overline{P_{\text{In}}}$ represent the complementary optical input signals, and R_{PD} is the PD responsivity. The I-V conversion resistance is denoted as R_{C}, which converts the photocurrents into voltage signals V_{In} and $\overline{V_{\text{In}}}$. The differential voltage $V_{\text{in-Diff}}$ is obtained by subtracting the $\overline{V_{\text{In}}}$ from the V_{In}, while VDD/2 adjusts the signal to make it suitable for reverse bias modulation of the microring. As mentioned, the output voltages from the dashed stage are inherently limited to the range between GND and VDD. Consequently, the modulation voltage is constrained by VDD and GND, limiting

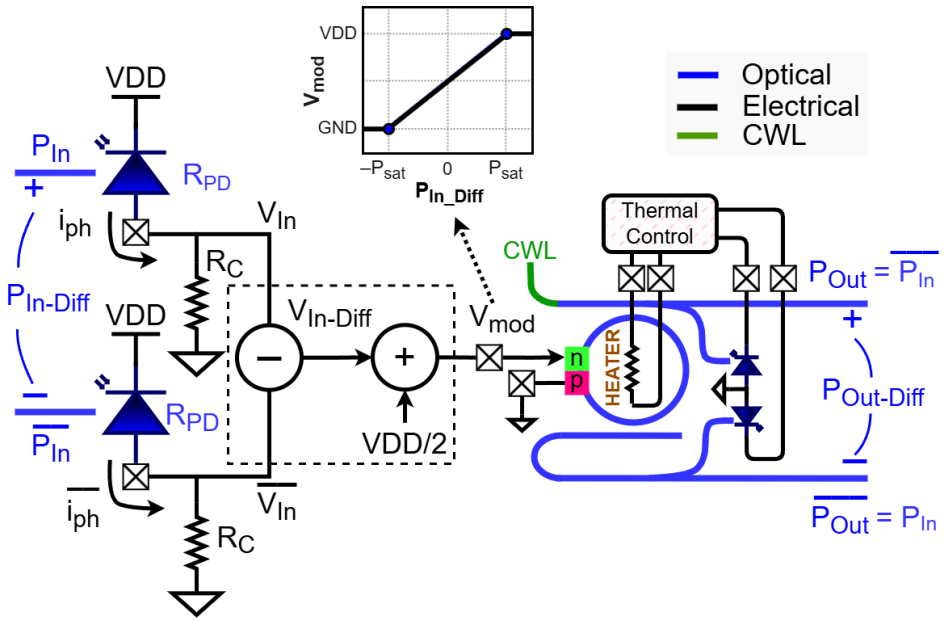

Figure 3.2: conceptual schematic of a simplified logic control circuit for a differential optical inverter

its range. As a result, the differential optical output power $P_{\text{Out-Diff}}$ depends on V_{mod}, which is subject to these saturation limits. To analytically model the differential optical output power as a function of V_{mod}, we begin with the Lorentzian approximation introduced in Chapter 2 (3), which describes the microring's transmission response near resonance. This expression is adapted under two key assumptions. First, we assume a linear relationship between the resonance wavelength and the modulation voltage, i.e., $\lambda_{\text{res}}(V_{\text{mod}}) = \lambda_{\text{res}}(0\,\text{V}) + \eta V_{\text{mod}}$, as shown in Chapter 2. This approximation was confirmed experimentally for applied voltages up to 5 V. Second, we evaluate the transmission at the fixed operating wavelength $\lambda = \lambda_{\text{c}}$, which corresponds to the complementary switching point defined in Chapter 2. Additionally, P_{CWL} denotes the continuous-wave laser input power supplied to the MRM. Substituting these into (3) yields the following expression for the differential optical output power:

$$P_{\text{Out-Diff}}(V_{\text{mod}}) = \left[1 - \frac{(T+D)}{1 + 4\left(\frac{\lambda_C - (\lambda_{\text{res}(0\,\text{V})} + \eta V_{\text{mod}})}{\text{FWHM}}\right)^2}\right] P_{CWL} \tag{33}$$

The total gain from the differential optical input power to differential optical output power is

determined by the conversion resistance (R_C), the PD responsivity (R_{PD}), and the slope of the $P_{\text{Out-Diff}}$ vs. V_{mod} response curve.

For the OLG to function as a valid logic gate, the absolute value of the gain must be at least 1. Since the I–V conversion resistance R_C is the only tunable parameter in this logic control circuit, it is useful to express the gain condition in terms of the minimum R_C required for correct operation. Therefore, the condition becomes:

$$|\text{Gain}| > 1 \Rightarrow R_{\text{C}} > \left| \frac{1}{R_{\text{PD}} \times \frac{dP_{\text{Out-Diff}}}{dV_{\text{mod}}}} \right| \tag{34}$$

This condition implies that a I-V conversion resistance of at least $1/\left|(R_{\text{PD}} \times \frac{dP_{\text{Out-Diff}}}{dV_{\text{mod}}})\right|$ is required for the OLG to operate correctly as a logic gate. For the fabricated MRM, the differential transmission slope in the 0–5 V range was measured at approximately -0.2 a.u./V. Assuming a CWL power of 250 μW, a 2 dB insertion loss, and a 3 dB loss in the splitter following the ring, the resulting slope between differential optical output power and modulation voltage is approximately –15.8 μW/V. Using a PD responsivity of $R_{\text{PD}} = 0.8$ A/W, (34) yields a minimum conversion resistance of about 79 kΩ.

Considering the calculated minimum conversion resistance, a system gain of -1, and the saturation limits defined by VDD and GND for the modulation voltage, we can determine the range of minimum differential input power required to drive the modulation voltage across its full swing. This range defines the input power interval over which V_{mod} transitions from GND to VDD. Beyond this range, the system enters saturation, and further increases in input power do not result in changes in modulation voltage or output power. The peak-to-peak amplitude of the minimum differential input power required to drive the modulation voltage from GND to VDD can be expressed as:

$$\Delta P_{\text{In, sat}} = \frac{VDD}{R_{\text{C}} \times R_{\text{PD}}} \tag{35}$$

This equation defines the transition threshold beyond which the system saturates, and additional increases in optical input power will not affect the modulation voltage or the optical output power.

It establishes an inverse relationship between the I–V conversion resistance R_C and the minimum required differential input power: a higher R_C reduces the differential input power needed to swing the modulation voltage from GND to VDD, ensuring proper logic-level operation. By substituting the device and circuit parameters (VDD = 5 V, $R_C = 79$ kΩ, and $R_{\text{PD}} = 0.8$ A/W) into (35), the minimum differential input power for |Optical Gain| $= 1$ is obtained as:

$$\Delta P_{\text{In, sat}} = \frac{5}{79 \times 10^3 \times 0.8} \approx 79\ \mu\text{W}.$$

3.1.2 Cascadable Optical NAND Gate Design

To build larger optical logic systems, a universal gate is essential. Universal gates, such as NAND and NOR gates, serve as fundamental building blocks in digital logic. In this subsection, we focus on the design of cascadable optical NAND gates, which are intended for use in more complex and scalable optical systems. Fig. 3.3 (a) illustrates the overall system architecture for the cascadable optical NAND gate. The concept behind the optical NAND gate is similar to that of the optical NOT gate, with the primary difference being the use of additional inputs and a dedicated logic control circuit.

Fig. 3.3 (b) illustrates the micrograph of the fabricated PIC, which includes a double-bus MRM, integrated PDs that receive optical input signals for logic operations, and monitoring PDs used for implementing the thermal control circuit. As shown in this figure, the optical input signals IN-A, $\overline{\text{IN-A}}$, IN-B, and $\overline{\text{IN-B}}$ are directed to corresponding PDs, which convert them into electrical signals fed into the logic control circuit. The optical output from the MRM is equally split by a 50:50 splitter, with one path directed to the monitoring PDs for thermal stabilization and the other serving as the output to subsequent OLGs. For NAND functionality, all four input signals and their corresponding PDs are used. In contrast, for the optical inverter configuration, only IN-A and $\overline{\text{IN-A}}$ are active, while IN-B and $\overline{\text{IN-B}}$ do not receive any optical input. As a result, the logic control circuit must be modified to handle all four optical input signals and generate the appropriate NAND function. The following subsection provides a detailed explanation of the logic control circuit design.

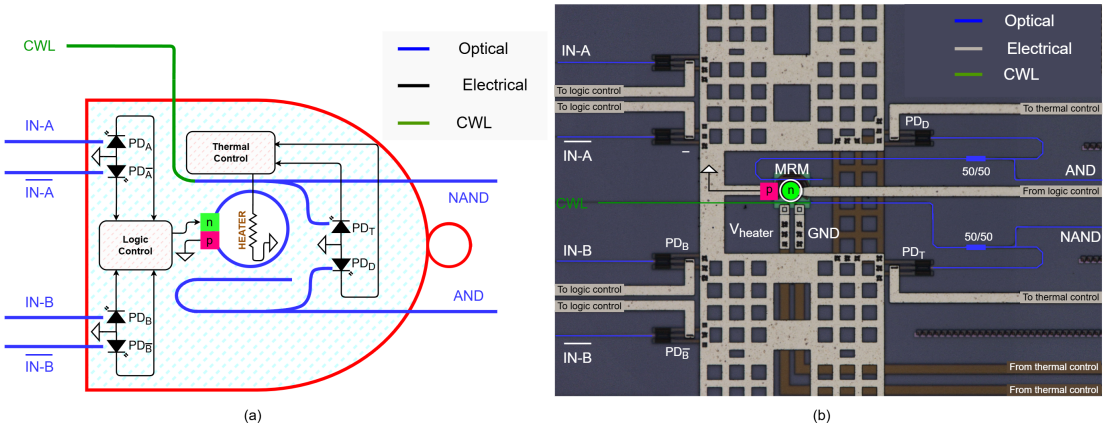

Figure 3.3: (a) Schematic of the designed cascadable optical NAND gate, and (b) micrograph of the fabricated PIC featuring a double-bus MRM, integrated PDs that receive optical input signals for logic control circuit, and monitoring PDs used for implementing the thermal control circuit.

3.1.3 Logic Control Design

The logic control circuit plays a critical role in interfacing the PIC with the electrical domain by converting photocurrents from on-chip PDs into modulation voltages that drive the MRM. This ensures accurate execution of optical logic operations. As shown in Fig. 3.3 (a) and (b), each ring includes four PDs that detect complementary optical input pairs, enhancing signal integrity and noise robustness. Upon reception, the PDs perform optical-to-electrical conversion, generating a photocurrent proportional to the incident light intensity. As illustrated in Fig. 3.4, these photocurrents then serve as inputs to the logic control circuit for further processing. To convert the photocurrent into a usable voltage signal, a simple resistor-based I-V conversion is employed. The resulting voltages, corresponding to IN-A, $\overline{\text{IN-A}}$, IN-B, and $\overline{\text{IN-B}}$, are then available for further signal manipulation.

The circuit employs a differential stage to subtract complementary voltage signals. This step improves the signal-to-noise ratio and suppresses common-mode noise. The differential stage also amplifies the resulting signal, ensuring it reaches the required voltage swing, which is needed for the following stages. At the output of the differential stages, a CMOS inverter further amplifies the signal. This inverter sharpens the transitions between logic levels and ensures the generated voltage swings meet the necessary thresholds for logic operations.

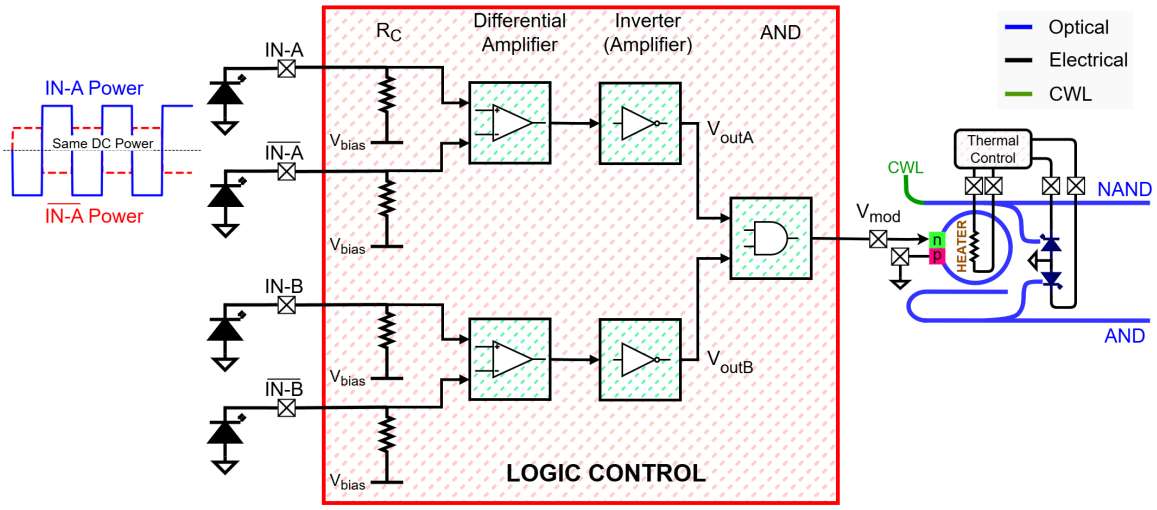

Figure 3.4: Schematic of the electronic circuit designed to control each optical NAND gate.

The amplified signals are then processed by an AND logic circuit, which executes the fundamental AND operation on the received inputs. This AND gate determines the final logic state based on the optical input signals. This logic signal directly drives the MRM with a 0–5 V modulation swing, shifting its resonant frequency and thereby controlling its transmission characteristics. Due to the inherent inversion in the relationship between output power and modulation voltage, the microring itself functions as an optical inverter, assuming the controller locks on the right side of the resonance. By combining the electrical AND gate with this optical inversion, the system successfully implements a NAND gate.

3.1.4 Power Transfer Characteristic, Optical Noise Margin, and Fan-out Measurements

The standard method for measuring the VTC of a digital NOT gate involves sweeping the input DC voltage from a low to high level while monitoring the corresponding output voltage. In the case of the optical NOT gate, the measurement focuses on the differential optical output power versus the differential optical input power. As described in previous sections, the optical NOT gate requires complementary input signals. To characterize its behavior, one input power should be swept from low to high, while the complementary signal should be swept simultaneously from high to low.

Fig. 3.5 (a) illustrates the experimental setup used to measure the PTC of the optical NOT gate. To generate the complementary optical signals, a signal generator (Keysight EDU33212A) was used to apply a slow ramp signal to the PN junction of MRM1. The optical output powers from MRM1 generate complementary through and drop signals, which are then used as inputs for MRM2 (the device under test).

The complementary through and drop powers from MRM1 are directed to the internal PDs within the PIC, and the resulting photocurrents are routed off-chip. The electrical part of the system is implemented on the board. We used $R_C = 20\,\mathrm{k}\Omega$ as I-V conversion resistance to convert the photocurrents into voltage signals. The difference between these converted voltages is represented as $V_{\text{In\_Diff}}$ in Fig. 3.5 (a). A differential amplifier, followed by an inverter, is used to convert and amplify the differential voltage into a single-ended modulation voltage (V_{mod}). Fig. 3.5 (b) shows the VTC of the active electrical circuit (differential amplifier and inverter) and its corresponding slope (V/V). The output of the electrical active circuit (V_{mod}) is constrained by VDD (5 V) and GND (0 V), with the maximum gain (slope) reaching approximately +907 V/V.

The modulation signal drives the main ring (MRM2), whose output powers are detected using QPhotonics QPFD-200 PDs. These PDs convert the optical signals into electrical signals, which are subsequently processed and monitored using conversion resistances. Fig. 3.5 (c) presents the measured PTC, showing the differential optical output power versus the differential optical input power, along with its corresponding slope (W/W). The maximum gain (slope) is approximately -171 W/W. This measurement is performed at a temperature of 20 °C, with a CWL power of -6 dBm (250 μW) and an operating wavelength of 1549.642 nm.

The conceptual circuit analyzed in the previous sections included I-V conversion resistance and a unity-gain subtractor without any active gain circuits. To compare the measurement results with the theoretical analysis, the effect of the active electrical circuit must be removed from the total system gain. This is achieved by dividing the measured optical slope by the measured slope of the active electrical circuit, yielding a system gain of approximately -0.18, as shown in Fig. 3.5 (d). This value remains stable across the transition region with a conversion resistance of 20kΩ, demonstrating the MRM's linear behavior within this range. To achieve a minimum absolute system gain greater than unity, excluding the contribution of active electrical circuits, a higher conversion

resistance is required. The necessary resistance value is $R_{\text{C, Req, Meas}} = 20\text{k}\Omega \times (1/0.18) = 111\text{k}\Omega$. This value represents the minimum required conversion resistance, extracted from measured data, needed for the system to achieve a gain magnitude greater than 1, which is the condition for valid logic-level operation without relying on additional active circuitry. This value defines the minimum acceptable gain for regeneration; however, a gain magnitude of at least five is typical in electronic logic gates. The required R_{C} was also calculated in Section 3.1.1 to be approximately 79 kΩ, based on the measured differential slope, insertion and splitter losses, and PD responsivity. As shown, the measured and analytical results follow the same trend, although the absolute values differ due to modeling approximations and experimental non-idealities.

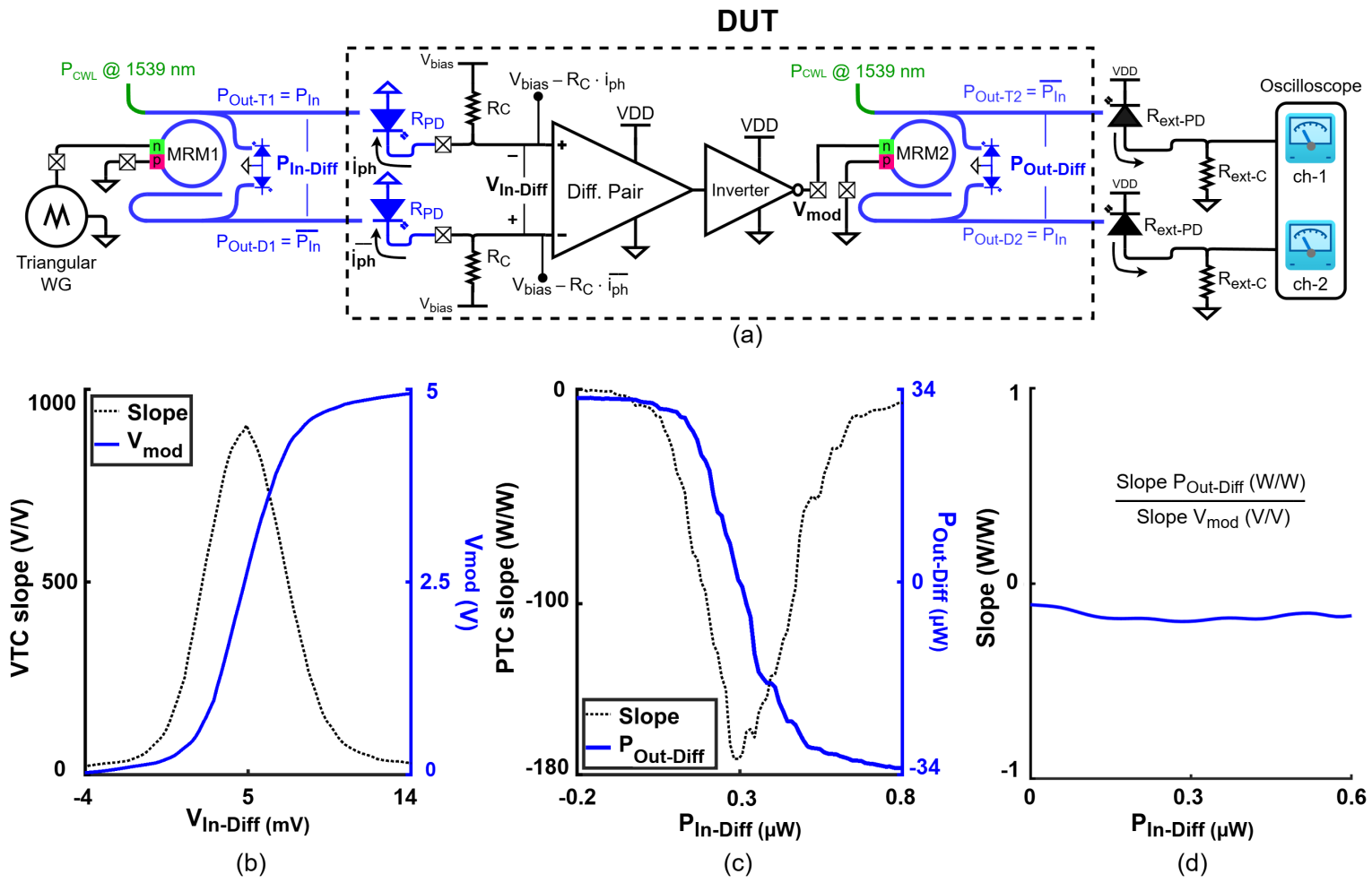

Figure 3.5: (a) Experimental setup for measuring the PTC of the optical NOT gate, (b) measured VTC of the active electrical circuit and its slope, (c) measured PTC of the optical NOT gate and its slope, (d) system optical gain after removing the effect of the active electrical circuit.

The ONM behavior of the optical NOT gate is illustrated in Fig. 3.6 (a), which shows the optical inverter's PTC with a CW input power of -6dBm (250 µW). This input power level is the maximum achievable without inducing significant self-heating effects in the device [35, 36]. The full input power range, from approximately -32 µW to 32 µW, is depicted along the x-axis. The ONMs extracted from this curve are $\mathrm{ONM}_L = 32\,\mathrm{W}$ and $\mathrm{ONM}_H = 31.4\,\mathrm{W}$.

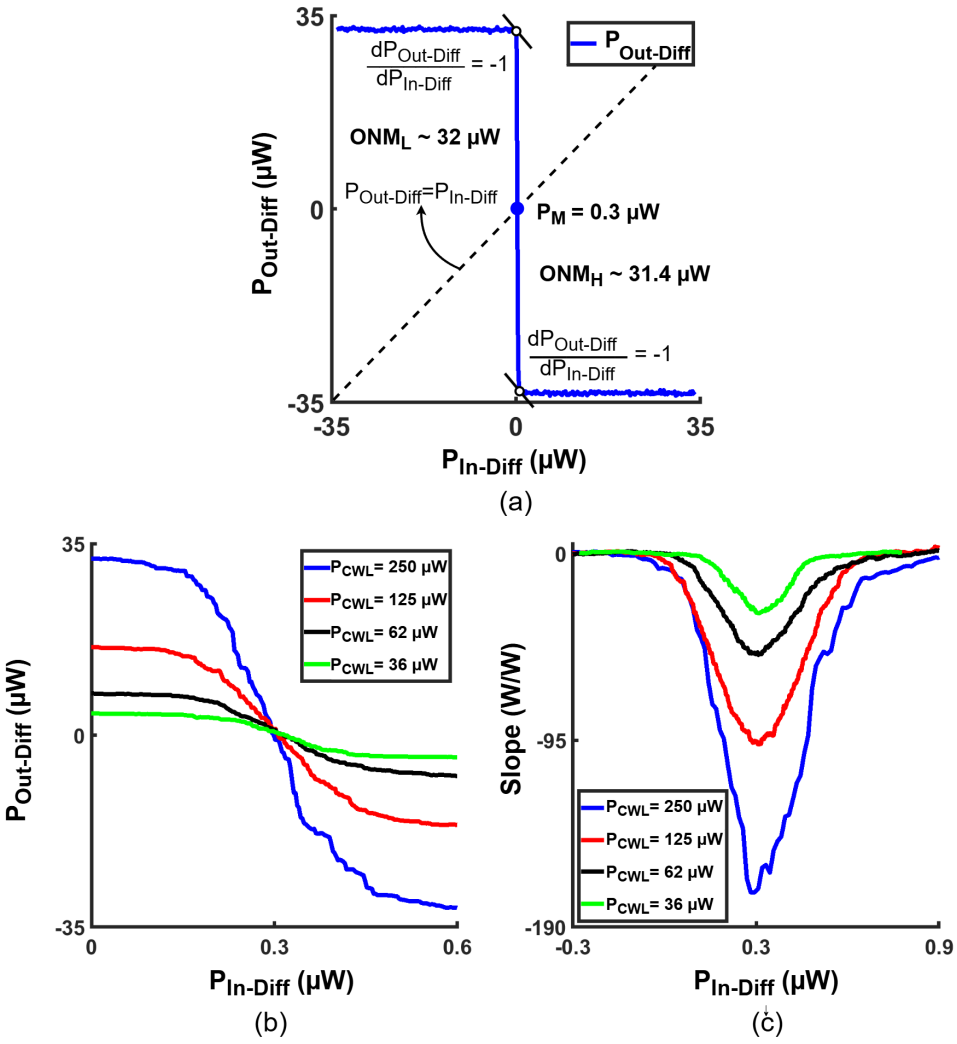

Figure 3.6: (a) optical inverter PTC at a CW input power of $-6\,\mathrm{dBm}$, showing the full input range and extracted ONMs. (b) PTC of the optical inverter under different CW input powers, illustrating the decrease in output amplitude with reduced input power. And (c) corresponding slope variations of the inverter response as a function of input power, highlighting the reduction in gain at lower powers.

Fig. 3.6 (b) and (c) present the optical inverter's PTC and corresponding slope variations under different input CW powers. As observed, reducing the CW power results in a decrease in both the amplitude of the differential output power and the overall system gain. This reduction also affects the ONMs, which scale down proportionally with the available power swing. Specifically, for an input power of -9 dBm (125 μW), the extracted ONMs are $\mathrm{ONM}_L = 16.5\,\mathrm{W}$ and $\mathrm{ONM}_H = 15.7\,\mathrm{W}$, while for -12 dBm (62 μW), the ONMs further decrease to $\mathrm{ONM}_L = 8.1\,\mathrm{W}$ and $\mathrm{ONM}_H = 7.7\,\mathrm{W}$. At an even lower input power of -15 dBm (36 μW), the ONMs drop to $\mathrm{ONM}_L = 4.0\,\mathrm{W}$ and $\mathrm{ONM}_H = 3.8\,\mathrm{W}$. Because both the slope of the transfer curve and the peak-to-peak differential output power reduce by nearly the same proportion, the ONMs decrease in magnitude but do not shift away from zero at lower CW input powers. In other words, the points where the slope is approximately -1 remain nearly aligned across different CW power levels. Although the ONMs decrease with lower input power, the gate maintains stable transitions across the tested CW input power levels, with the ONMs remaining sufficiently wide (relative to the corresponding power swing) to support reliable logic operation in each measurement.

In logic circuit design, fan-in and fan-out are key parameters that affect scalability. In the proposed OLG system, fan-in does not impose a significant limitation because multiple optical input signals can be simultaneously applied to separate on-chip PDs. Additional PDs can be integrated as needed to support more inputs, enabling scalable multi-input logic functions, such as NAND, without introducing significant optical or electrical penalties. In contrast, fan-out is more restrictive, as it depends on whether the differential optical output power from one OLG is sufficient to drive the inputs of multiple subsequent gates. Specifically, the output signal must exceed the minimum differential input power required by each receiving stage to ensure reliable logic-level transitions, defined by the ONMs. While this limits scalability, the regenerative behavior of the cascadable OLG, enabled by optical-to-electrical-to-optical (O/E/O) conversion, helps maintain signal quality across stages by re-amplifying and reshaping the output.

Experimental results show that, with a maximum CW input power of -6 dBm (250 μW), the differential optical output reaches 64 μW peak-to-peak. Additionally, the system remains operational with differential optical input power as low as 8 μW peak-to-peak, establishing a practical lower bound for logic-level recognition. This suggests that a single OLG output can drive up to

eight gates in parallel. More conservatively, considering potential variations and losses, a fan-out of four remains feasible. This estimation avoids reliance on idealized noise models and reflects real system behavior under practical conditions, indicating that the proposed OLG design can support a fan-out of 4–8, depending on system margins, and highlighting its potential for scalable optical logic networks.

It is worth noting that the electrical control circuit of the optical NAND gate shown in Fig. 3.4 shares the same foundational structure as that of the optical inverter in Fig. 3.5 (a), with the primary difference being the inclusion of an additional electrical AND gate at the output. In the optical NAND gate, when one input is held high, the expected PTC from the other input to the output closely resembles the measured PTCs of the optical inverter presented in Fig. 3.5 (f). However, due to the added electrical gain introduced by this extra stage, the optical NAND gate's PTC is expected to exhibit a sharper transition, i.e. a higher slope, compared to that of the optical inverter.

3.2 2×2 Optical Switch Design and Characterization

3.2.1 2×2 Switch based on Optical Combinational Logic

As shown in Fig. 3.7 (a), the 2×2 optical switch is designed using seven identical, cascadable optical NAND gates. It operates with two differential optical input signals (IN-1 and IN-2) and a differential optical select signal (SEL), which controls the switch's behavior, determining whether it functions in the bar state or the cross state. The PDs in the PIC convert the incoming optical signals into electrical photocurrents, which are then used by the logic control circuits. These PDs are wirebonded to the PIC's PCB and interfaced with the logic control circuit through off-board connections. In parallel, all MRMs in the system are powered by a single CW laser source, which is split into seven optical paths, each independently tuned to its operating wavelength using a dedicated thermal control circuit. Once properly tuned, the combined action of the logic control circuit and the MRM yields the intended differential optical signal for the subsequent NAND stage. Each successive NAND gate performs the same sequence: optical detection via PDs, electrical processing through the control circuit, and optical modulation via the MRM. This process repeats across the

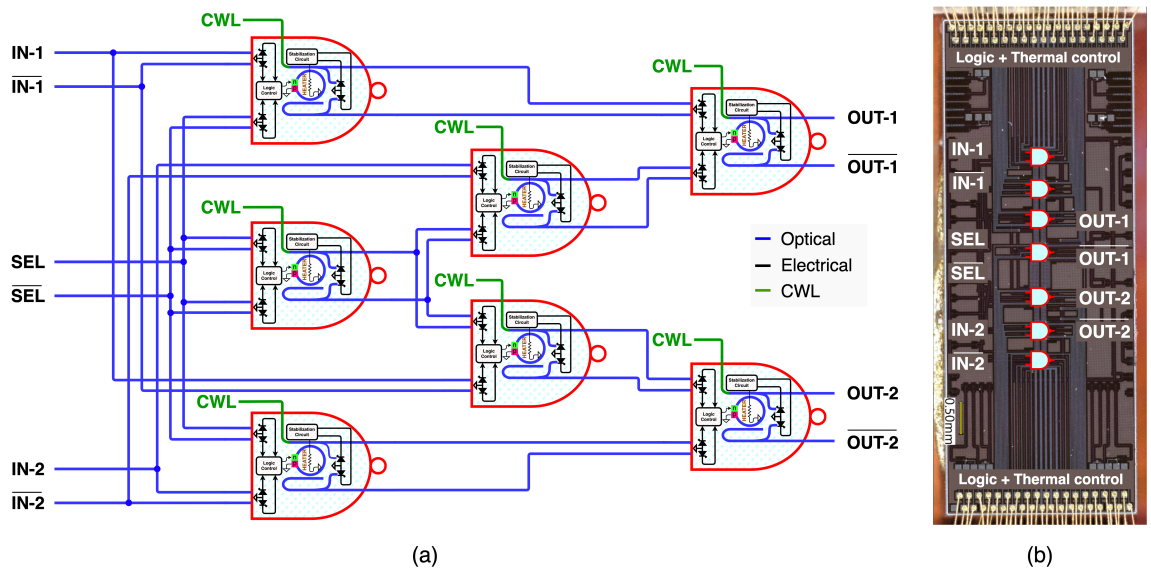

Figure 3.7: (a) Schematic of the designed combinational logic to perform a 2×2 optical switch function, and (b) micrograph of the manufactured photonic integrated circuit.

logic network until the final outputs (OUT-1, OUT-2, and their complementary signals) are generated. Fig. 3.7 (b) shows the micrograph of the manufactured PIC. The SEL optical signal plays a crucial role in determining the switch's behavior. In the bar state, where SEL=1, IN-1 is directed to OUT-1 and IN-2 to OUT-2. In the cross state, where SEL=0, IN-1 is routed to OUT-2 and IN-2 to OUT-1. The truth table summarizing the switch behaviour is reported in Table 3.1.

Table 3.1: Truth table of the 2×2 optical switch

SEL	OUT-1	OUT-2	Switch state
Low	IN-2	IN-1	Cross
High	IN-1	IN-2	Bar

3.2.2 2×2 Optical Switch Measurements

As illustrated in Fig. 3.8, the experimental setup for characterizing the 2×2 optical switch is designed to ensure precise signal generation, modulation, detection, and monitoring. The device under test (DUT) consists of a PIC, a logic control PCB, and a thermal control PCB. The PIC incorporates the photonic elements of each NAND gate, including MRMs, their heaters, waveguides, PDs, and

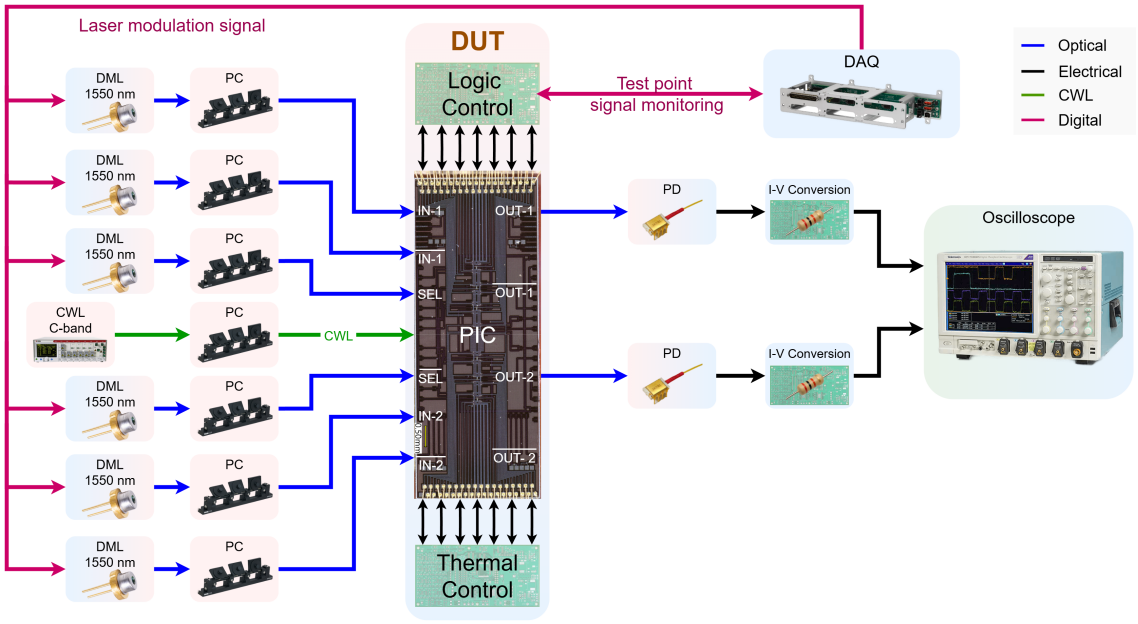

Figure 3.8: Experimental setup to perform the MRM, logic control and 2×2 switch measurements including a CW C-band laser, DMLs, PCs, DAQ TS 15130 to generate the optical input logic signals and monitor the logic control, the device under test (DUT) consisting of the PIC and PCB logic control, QPhotonics QPFD-200 PDs, low-speed I-V conversion resistance in PCB, and an oscilloscope.

grating couplers. Grating couplers on two opposing sides enable optical signal input and output. The other two sides are wirebonded to the PIC's PCB for electrical interfacing and are connected via ribbon cables to the logic and thermal control PCBs.

A CW C-band laser serves as the primary optical source, providing the necessary power to all MRMs via a 1×8 optical splitter. Additionally, directly modulated lasers (DMLs) (Modulight ML1141) generate the modulated optical input signals. These lasers are controlled by a National Instruments (NI) Data Acquisition System (DAQ) TS 15130, which generates the required modulation patterns. The modulated signals first pass through Thorlabs polarization controllers (PCs) FPC032 to ensure proper polarization alignment prior to entering the PIC. As illustrated in Fig. 3.8, once inside the PIC, the optical signals available for switching include IN-1, IN-2, SEL, and their corresponding complementary signals.

As mentioned earlier, electrical PCBs manage both logic control and thermal stabilization.

The logic control circuit generates the electrical modulation signals required to implement the desired optical logic functions within the 2×2 switch, ensuring correct operation of each MRM-based NAND gate. The thermal control circuit locks each microring at the desired wavelength by maintaining precise temperature conditions. A second DAQ system (NI DAQ TS 15100) monitors key test points on both PCBs in real time, providing comprehensive data for system evaluation.

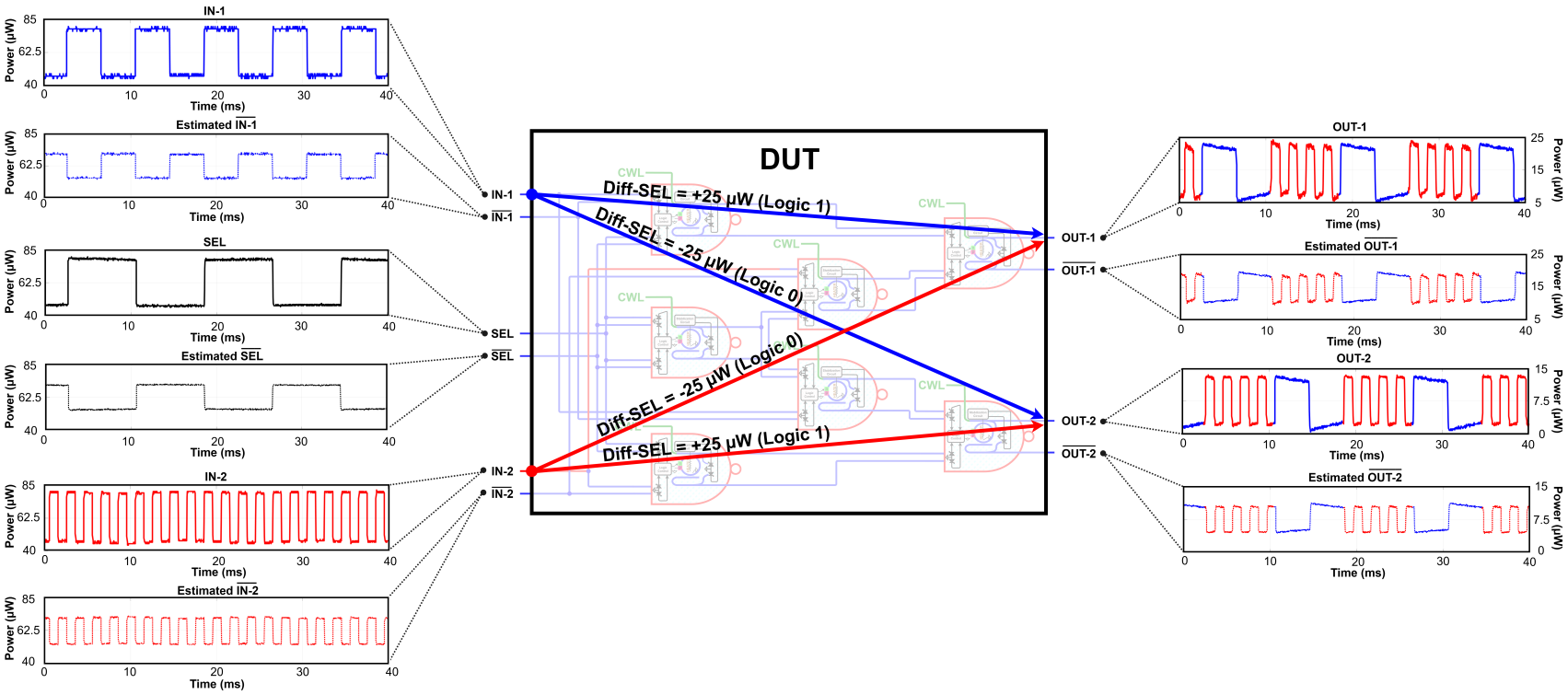

Figure 3.9: Measured through powers of IN-1, IN-2, SEL, OUT-1, and OUT-2, along with their estimated drop (complementary) powers, demonstrating the bar and cross functionality of the 2×2 optical switch.

The optical outputs, OUT-1 and OUT-2, are extracted after the modulated inputs pass through the PIC. These outputs are detected using QPhotonics QPFD-200 PDs. The detected photocurrents are then processed by I-V conversion resistances integrated into the logic control circuit. A Tektronix oscilloscope is used to analyze the output signals and verify the switching behavior. The complementary (drop) powers are estimated based on the measured through powers, the known behavior of the MRMs, and the operating wavelength specified in 4. As shown in Fig. 3.9, when SEL is low (Diff-SEL = -25 μW), IN-1 is routed to OUT-2, and IN-2 is routed to OUT-1. When SEL is high (Diff-SEL = +25 μW), the switch operates in a bar state, routing IN-1 to OUT-1 and IN-2 to OUT-2. A difference in power levels was observed between OUT-1 and OUT-2. This imbalance is primarily attributed to grating coupler misalignment and suboptimal polarization alignment, though other factors such as splitter variations, waveguide crossing losses, and general system nonidealities may also contribute. The droop observed in the blue traces of the output signals in Fig. 3.9 arises from the dynamic response of the thermal feedback control loop. In this scheme, the through and drop port powers are averaged by low-speed TIAs (in the thermal control circuit), and their difference is used to generate the error signal for the PID controller (see Chapter 2, Fig. 2.5). When the time constant of the TIAs is comparable to or shorter than the unit interval (UI) of the operating signal, the TIA output no longer represents a flat average of the through and drop port powers. Instead, it partially follows the data transitions, which distorts the error signal and introduces residual thermal drift, observed as droop in the output traces. In the 2×2 switch demonstration, a unified control setting was applied to all seven microrings, optimized for transitions at a minimum speed of approximately 1 KHz. At lower speeds, the averaging becomes less accurate, and the droop becomes more significant. While this effect could be mitigated by individually tuning each microring for slower operation, a unified configuration was chosen to streamline the testing process. Despite this, the switch behavior remains stable, and the core functionality is clearly demonstrated.

As previously described, each MRM within the 2×2 optical switch receives its optical power from the shared CW C-band laser through the 1×8 splitter, ensuring strong output signals. This architecture enables intrinsic signal regeneration, preventing degradation across multiple cascaded stages, which enhances scalability and reliability for optical computing applications.

The experimental setup shown in Fig. 3.8 effectively integrated photonic and electronic components, enabling accurate testing of the 2×2 optical switch. The DUT, consisting of the PIC, logic control PCB, and thermal control PCB, was evaluated using DML-based signal generation, polarization control, photodetection, I–V conversion, and real-time monitoring. Together, these elements ensured high-fidelity signal transmission and reliable switching by ensuring proper polarization alignment, minimizing signal degradation, and enabling accurate electrical control of the MRMs. This demonstrated the system's feasibility for advanced optical logic applications.

3.3 Conclusion

In this chapter, we have experimentally demonstrated an optical combinational logic circuit implementing a 2×2 optical switch using cascadable NAND gates based on MRMs and electronic logic control. The successful characterization and operation of this switch highlight the feasibility of integrating optical logic circuits with photonic integrated circuits to perform digital optical signal processing. Additionally, we presented characterization concepts such as the PTC and the ONM, drawing direct parallels with well-established electronic logic gate metrics. These approaches provide a deeper understanding of the optical logic gate behavior and set the foundation for systematic analysis and optimization of future optical logic circuits.

Beyond demonstrating fundamental functionality, our results show strong potential for digital optical signal processing. Furthermore, the scalability of the architecture suggests that the approach can be extended to higher-radix optical switches. The combination of design, experimental validation, and analytical methods paves the way for the development of more advanced combinational optical logic circuits and scalable, high-performance photonic switching systems, which could play a key role in the evolution of future optical computing and communication technologies.

Building on this demonstration, the next step is to implement a logic control architecture tailored for high-speed operation and robust handling of data streams with highly unbalanced logical '1'/'0' densities. While DAQ system and interconnect contribute to parasitics and delays, they are not the main performance limiter. Achieving multi-gigabit operation with preserved signal integrity will benefit from a bandwidth-optimized control circuit with enhanced regeneration capability and

tolerance to varying input statistics. The design and implementation of such a CMOS-based logic control circuit is the focus of Chapter IV.

Chapter 4

Design and Tapeout of the Proposed IC-Level Peak/Low Detector-Based Logic Control Circuit

In logic gate applications, the output of one gate drives the input of the following stage, and similarly, the input of a gate originates from the output of the preceding stage. This implies that the input considerations of a gate are directly determined by the behavior of the preceding one. Fig. 4.1 shows the schematic of a cascaded OLG in the case where the preceding gate is driven by an unbalanced data pattern, meaning that the ratio of logical '1's to '0's deviates from 50

In this situation, the thermal control circuit of the preceding MRM locks the operating wavelength at distinct points corresponding to each specific data density. As discussed in Chapter 2, the thermal control loop operates by comparing the average optical powers at the through and drop ports. With different logical '1' densities, these average signals shift: for example, when the density of logical '1's is 10%, the average signal is much closer to the low level, while at 90% density it is much closer to the high level. Consequently, the error signal, defined as the difference between the average through and average drop signals, reaches zero at slightly different wavelengths for each density.

Fig. 4.2 shows the measured differential transmission ($T_T - T_D$) at reverse bias voltages $V_{\mathrm{rb}} =$

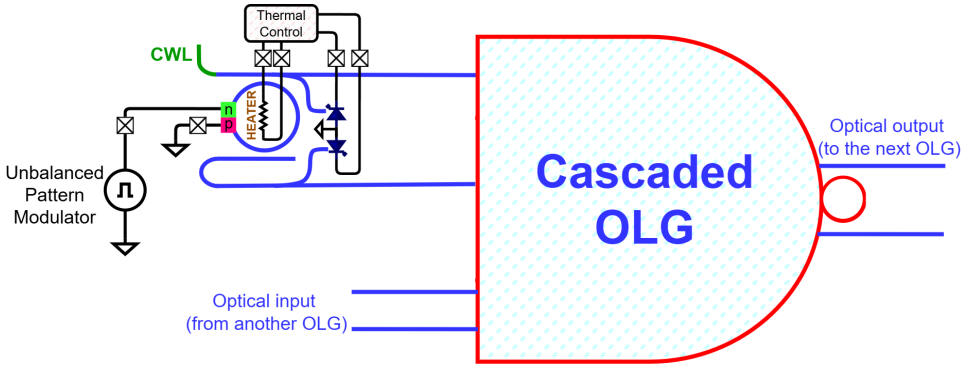

Figure 4.1: Schematic illustration of thermal locking behavior under unbalanced modulation.

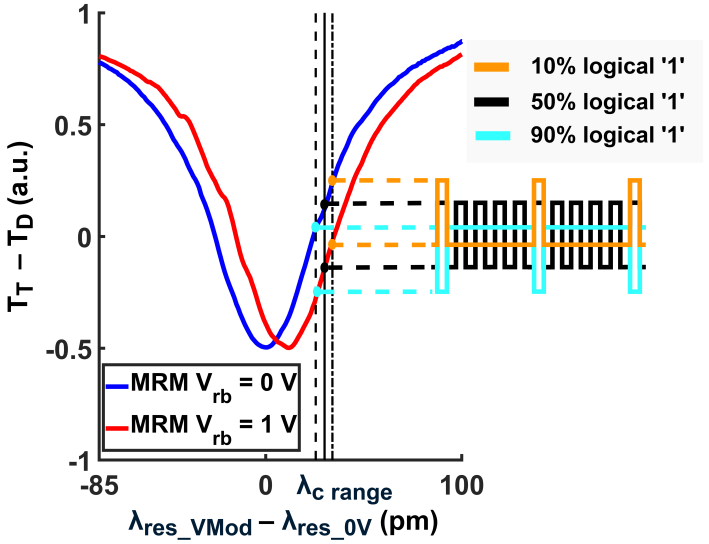

Figure 4.2: Measured differential transmission ($T_T - T_D$) as a function of reverse bias voltage V_{rb} at 0 V and 1 V. The operating points corresponding to 10%, 50%, and 90% logical '1' data densities are highlighted.

0 V and 1 V, illustrating how the locking points vary with data density and collectively form a range of stable operating wavelengths rather than a single fixed point. This behavior results in different effective input levels for the cascaded OLG depending on the statistical balance of the preceding stage's output.

Using the same MRM and thermal control system described in Chapter 2, Fig. 4.3 shows the simulated photocurrent, provided by the preceding OLG, at the input of the logic control circuit for data densities of logical '1's ranging from 10% to 90%. This photocurrent, which appears at the TIA input, is the same whether it drives the logic control block of an optical inverter or serves as one

input to the logic control block of an optical NAND gate. It is also important to note that this figure does not capture the transient behavior or the settling process when transitioning between different densities; instead, it highlights the distinct photocurrent levels associated with each input density. This simulated photocurrent is obtained by multiplying the differential optical output power of the microring (Through – Drop) by the responsivity of the PD, assuming a CWL power of -6 dBm, an insertion loss of 2 dB, along with a 90:10 splitter following the microring, a PD responsivity of 0.8 A/W, and a modulation voltage V_{mod} ranging from 0 to 1.2 V.

As explained in Chapter 2, conventional receivers typically employ DCOC circuits to compensate for the DC level of input current and align the signal level with the threshold of the logic circuit to ensure correct decision making. These circuits operate based on the average value of the input signal. This approach works well in high-speed modulators used in optical transceivers, where data streams are typically balanced (e.g., 50% logical '1's and '0's), ensuring that the average corresponds to the correct DC level. However, in optical logic gate applications, input patterns can be highly unbalanced, causing the average level to deviate significantly from the actual logic threshold. For example, a data stream with 10% logical '1's produces an average much closer to the low level, while a 90% '1' stream pushes the average near the high level. As a result, conventional DCOC mechanisms fail to provide proper compensation, leading to misaligned logic levels at the input of the stages and a degraded signal-to-noise ratio (SNR). In [25], a solution was proposed that incorporates feedback from the output voltage of the logic control circuit to dynamically regulate the thermal loop, but it adds complexity and tight coupling to the logic control circuit.

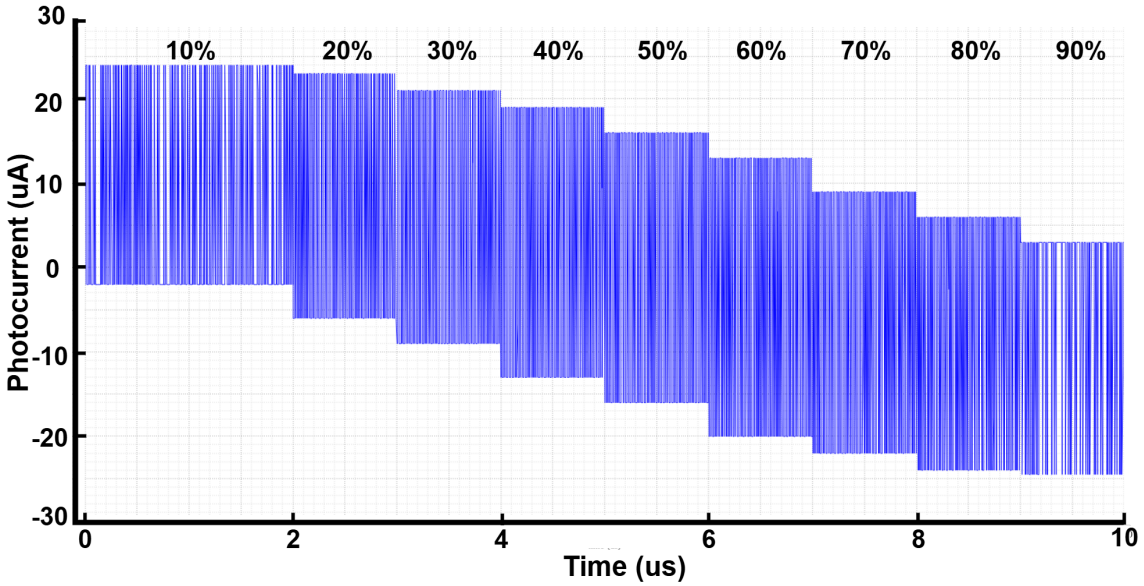

Figure 4.3: Simulated photocurrent at the input of the logic control circuit of the cascaded OLG for densities of logical '1's ranging from 10% to 90%.

This chapter introduces a logic-aware circuit that does not modify or control the thermal locking point. Instead, it enables correct logic operation by properly compensating the input DC current, even when the thermal control circuit operates within a locking range, instead of the locking point, due to unbalanced data. The proposed design is capable of handling a wide range of input data densities, from 10% to 90% logical '1's, and ensures correct functionality without requiring changes to the existing thermal controller. The overall architecture of the proposed IC-level logic control circuit is shown in Fig. 4.4, which includes the main building blocks: a TIA, MAs, a peak/low detector-based OC, and a final logic function block. In the following sections, system-level design considerations are first discussed. Then, the structure and biasing of PDs are presented, followed by a detailed description of each circuit block, including design considerations, post-layout simulations, and integration strategies to ensure correct functionality.

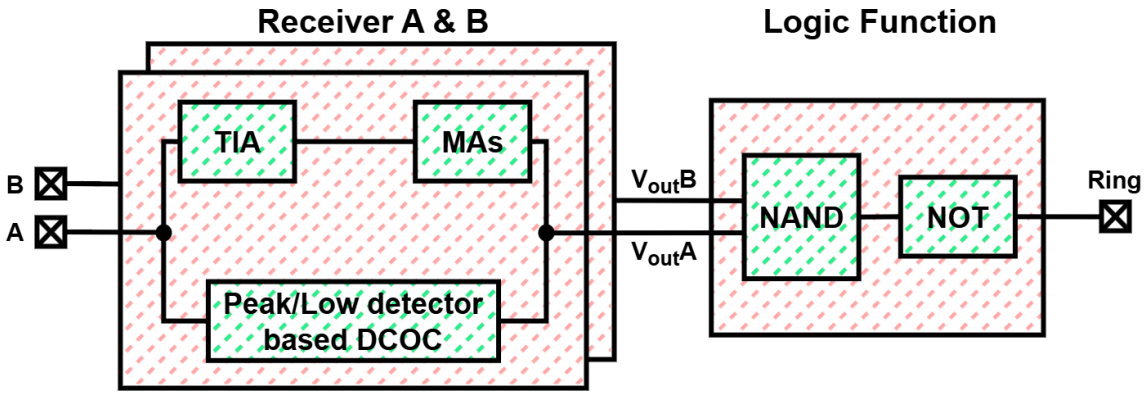

Figure 4.4: Block diagram of the proposed IC-level logic control circuit.

4.1 Design of the Proposed Peak/Low Detector-Based Logic Control Circuit

As discussed in the preceding sections, the proposed logic control circuit processes optical input signals to generate the required modulation voltages for the MRM. To ensure correct functionality, key system-level requirements, including signal level expectations, gain requirements and distribution, and the necessary bandwidth and data rate, must be clearly defined and satisfied.

Assuming a CWL input power of -6 dBm (250 μW), a 90:10 splitter following the microring, a modulation voltage range of 0 – 1.2 V, and including an additional 2 dB insertion loss in the optical path, and using the characterized differential output power versus V_{rb} relationship shown in Fig. 2.7 (b), the differential optical power received on the PDs of the following OLG is approximately 35 μW. With a PD responsivity of R = 0.8 A/W, this corresponds to a photocurrent of approximately 28 μA.

To meet the target end-to-end optical gain of 10 W/W (as defined in Chapter 3 as the ratio of differential optical output power to differential optical input power), the following relationship is used:

$$P_{\text{Out-Diff}} = P_{\text{In-Diff}} \cdot R_{\text{PD}} \cdot G_{\text{elec}} \cdot \frac{dP_{\text{Out-Diff}}}{dV_{\text{mod}}}, \tag{36}$$

G_{elec} is the electrical gain, and $\frac{dP_{\text{Out-Diff}}}{dV_{\text{mod}}}$ is the slope of the optical differential output power versus V_{mod}. Under the specified conditions, this slope is approximately -28.44 μW/V.

Solving the above equation for the desired optical gain yields an electrical gain requirement of approximately 440 kΩ for the logic control circuit.

Separately, to ensure that a voltage swing of at least 400 mV is presented at the input of the NAND gate, the analog front-end must provide a transimpedance gain of approximately 14.3 kΩ (400 mV / 28 μA). The receiver achieves the required gain through a combination of a front-end TIA and a multi-stage MA. The TIA is designed to provide a configurable transimpedance gain in the range of 100–200 Ω, depending on the selected feedback resistance. The MA stages further amplify the signal with a configurable voltage gain ranging from approximately 75 to 150.

Final logic-level restoration is performed by a NAND gate followed by an inverter, which together contribute an additional gain factor of approximately 30, resulting in a combined transimpedance gain of 400–440 kΩ at the output of the logic control circuit.

The design target was a propagation delay of approximately 100 ps for a single gate. In synchronous cascaded logic, the maximum practical clock frequency is typically several times lower than the inverse of the propagation delay, allowing margin for setup time, clock skew, and other timing uncertainties [37, 38]. Using a factor of 5-10 gives a practical synchronous range of roughly 1–2 GHz. By designing for a speed above this range, the circuit maintains robust operation across varying conditions and preserves headroom for potential higher-speed or asynchronous use. Specifically, the design goal was set to support 8–10 Gbps operation.

While this target data rate can be supported with a bandwidth of roughly 5–7 GHz, the schematic-level design included additional bandwidth margin. The TIA and MA stages were dimensioned to exceed the minimum requirement so that, after expected degradation from parasitic capacitance and resistance introduced during layout, post-layout performance would remain comfortably within the limits required for the intended operation.

In addition to high-speed operation, the circuit supports low-speed testing down to 100 Mbps, enabling functionality verification with low-cost test equipment and facilitating easier debugging and signal monitoring.

4.1.1 Subtractive PD Pair Structure

Fig. 4.5 shows the subtractive PD pair structure implemented in this work. Subtractive PDs are widely used in high-speed optical communication due to their ability to suppress common-mode signals and noise. This structure typically consists of two PDs arranged such that their photocurrents are subtracted, producing a bidirectional output current that corresponds to the optical signal difference.

In the context of the proposed logic system, the subtractive Structure serves two key purposes. First, it enables accurate detection of differential optical signals that represent logical states. Second, it improves robustness against power intensity changes by canceling the DC level of the photocurrent and producing a bidirectional signal. When the input data are balanced (e.g., 50–50), this signal is symmetric around zero. For unbalanced data, it still swings positive and negative but with a shifted baseline. While the proposed DC offset compensation circuit (detailed in the following sections) is still required, the reduced compensation range eases its design. As a result, each gate receives an input current that remains closer to the ideal centered level, which is particularly beneficial for cascaded optical logic configurations. In addition, using this configuration eliminates the need for two separate pads in both the PIC and the logic control IC, as well as the need for a dedicated electrical subtraction stage in the logic control circuitry. The resulting bidirectional current is further processed by the logic circuit described in the following subsections to generate the corresponding electrical modulation signal.

Considering a DC voltage of approximately $\mathrm{V_{DD}}/2$ at the input of the TIA, as will be discussed in the following subsection, and taking into account the need for a reverse bias of around 2 V across each PD, the subtractive PDs are connected to two bias voltages: $\mathrm{V_{bias1}} = 2.5\,\mathrm{V}$ and $\mathrm{V_{bias2}} = -1.5\,\mathrm{V}$.

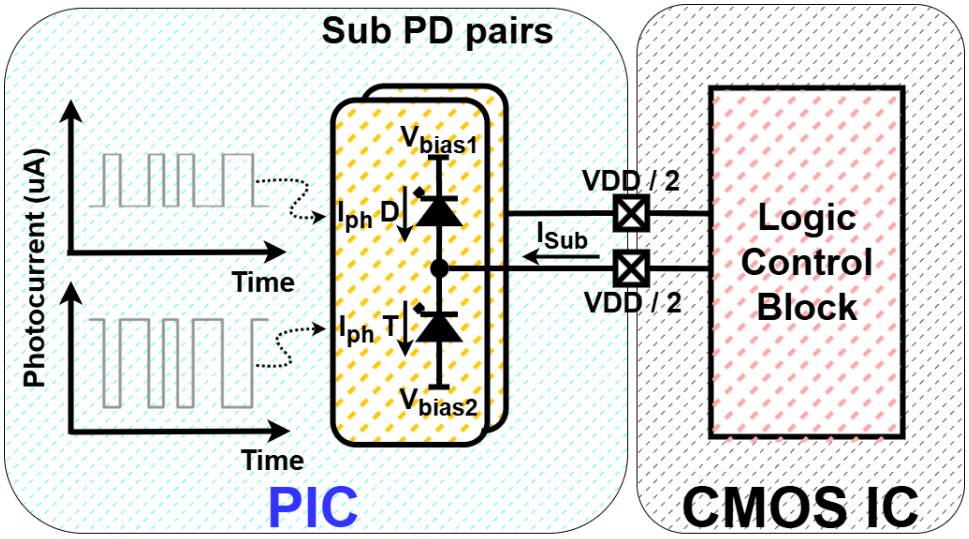

Figure 4.5: Subtractive PD Pair structure.

4.1.2 TIA Design

In the proposed logic control circuit, a conventional inverter-based TIA with shunt feedback is employed, as shown in Fig. 4.6. As mentioned in the previous section, this TIA is driven by a subtractive PD pair structure that generates a bidirectional input photocurrent $I_{\text{In-Diff}}$. The effective input capacitance, denoted C'_D, includes contributions from both PDs, the associated pad parasitic, and the electrostatic discharge (ESD) protection structures. Following the design principles outlined in [31], the sizes of the NMOS and PMOS transistors in the inverter are chosen to be equal in order to maximize the total transconductance, $g_m = g_{m1} + g_{m2}$ for a given transistor input capacitance.

Based on the equations presented in Section 2.3.1 and the parameter sweeps performed during the design process, a fundamental trade-off emerges: increasing the feedback resistor R_F enhances gain but reduces bandwidth and increases signal delay. Increasing the transistor size (W/L) moderately improves gain but also raises power dissipation and affects bandwidth in a non-monotonic way. Moderate upsizing can initially extend bandwidth through higher transconductance, but further increase in size raises input capacitance and ultimately reduces bandwidth.

Considering these trade-offs, the transistor sizes were selected as $W/L_1 = W/L_2 = 20\,\mu\text{m}/60\,\text{nm}$. To provide reconfigurability in the TIA gain, enabling adaptability for different use cases, a T-gate

switching mechanism was implemented in the feedback path. This allows the total feedback resistance to be configured as $R_F = 150\ \Omega$, $250\ \Omega$, or $350\ \Omega$, where $R_F = R_{\text{switch}} + R'_F$, and the switch resistance R_{switch} is approximately $90\ \Omega$, as will be explained in the following paragraph. The same T-gate switch structure will also be used in other parts of the circuit, such as the MAs, as described in the following sections.

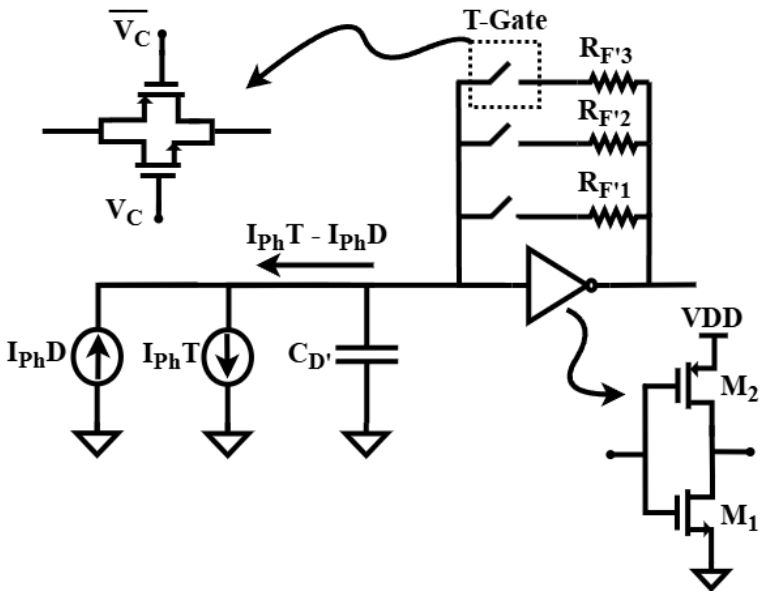

Figure 4.6: Schematic of the inverter-based TIA with selectable feedback resistors using a T-gate switching network.

Although the T-gate switch control voltages (V_C and $\overline{V_C}$) are fixed at 0 V or 1.2 V, the signals passing through the switch can vary over a wide voltage range, especially in the MAs and buffers. To ensure that the on-resistance remains relatively constant across this range, the PMOS device is sized approximately 3.5 times wider than the NMOS. This sizing ratio was determined through parameter sweeps during the design process to balance the conductance contributions of both transistors across the full signal swing. Fig. 4.7 illustrates the simulated on-resistance of the T-gate switch for $W/L_{\text{PMOS}} = 3.5 \times W/L_{\text{NMOS}} = (7 \times 2\,\mu\text{m})/60\,\text{nm}$, as a function of the signal voltage varying from 0 to 1.2 V. The previously reported switch resistance of approximately $90\,\Omega$ corresponds to this specific transistor sizing. While larger transistor sizes could further reduce the switch on-resistance,

they would also introduce greater parasitic capacitance, which in turn degrades the bandwidth of the circuit. In this design, since the switch appears in series with a physical resistor, a moderately high on-resistance is acceptable. The total resistance can be adjusted accordingly by slightly reducing the physical resistor value to maintain the desired overall resistance without compromising bandwidth.

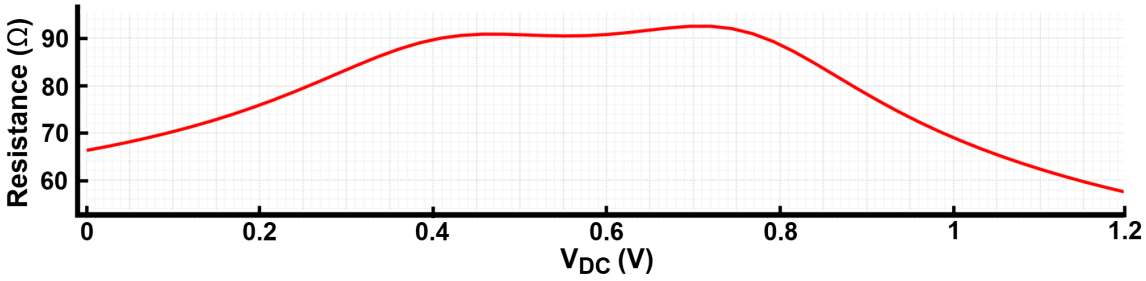

Figure 4.7: Simulated small-signal on-resistance of the T-gate switch with optimized transistor sizing, showing a relatively constant resistance over the 0 – 1.2 V signal range. The x-axis represents the DC voltage applied to both terminals of the switch.

Fig. 4.8 presents the simulated AC response for each of the three gain settings. Each case corresponds to one of the feedback switches being closed, resulting in a different total feedback resistance. The TIA configurations with feedback resistances of 150 Ω, 250 Ω, and 350 Ω exhibited transimpedance gains of 103.7 Ω, 187 Ω, and 271.1 Ω, respectively, and corresponding -3 dB bandwidths of 20.18 GHz, 15.95 GHz, and 13.08 GHz. As expected, higher gain configurations exhibit lower bandwidths, clearly demonstrating the gain–bandwidth trade-off imposed by the feedback resistance.

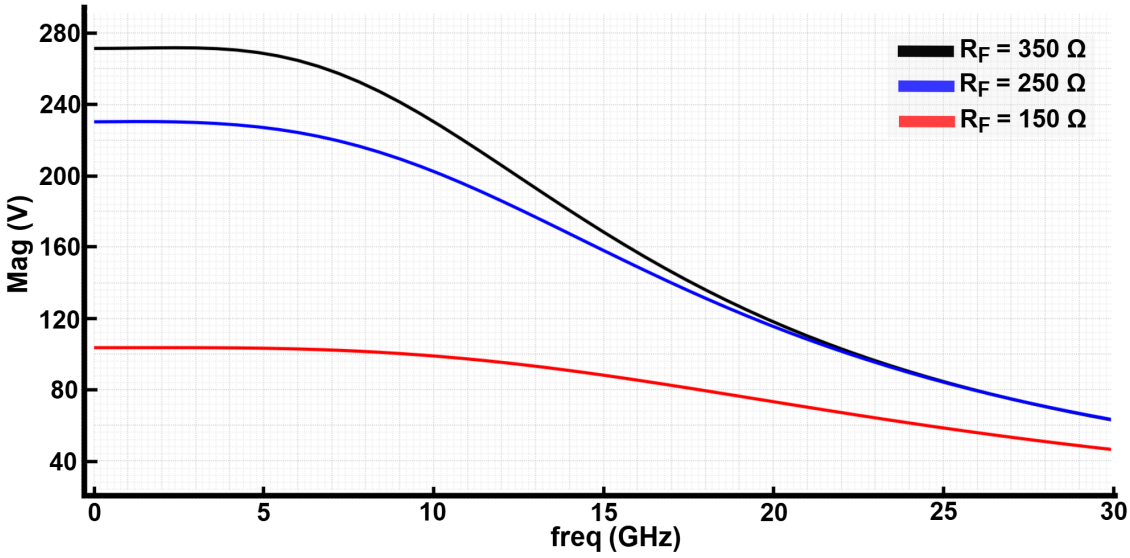

Figure 4.8: simulated AC response of the reconfigurable TIA for three different feedback resistance settings.

4.1.3 MA Design

Fig. 4.9 shows the schematic of the three-stage Cherry–Hooper MA used in the proposed system. This amplifier topology is used as the main amplification block following the TIA to increase the signal level to values detectable by subsequent logic circuitry. This circuit is chosen because its complex-conjugate pole pair produces mild gain peaking, thereby extending the –3 dB bandwidth beyond that of cascaded single-pole stages. Furthermore, the second stage of the circuit uses a shunt feedback TIA for current-to-voltage conversion while providing a lower effective output resistance compared to a purely resistive load. The resulting decrease in output RC time constant contributes to additional bandwidth improvement [31].

Similar to the TIA, the design of the MA involves key trade-offs that were explored using both analytical equations from Chapter 2 and parameter sweeps during the design process. These trade-offs include:

- Increasing the transistor size (W/L) improves gain but increases power dissipation and can reduce bandwidth.

- Increasing the feedback resistance R_{MA} improves gain but also increases delay and decreases bandwidth.

- Increasing the number of stages for fixed per-stage gain, increases the overall gain, but at the cost of higher power dissipation, increased delay, and reduced bandwidth.

To maintain compatibility with the TIA output while improving power efficiency, all transistors in the MA are sized equally for NMOS and PMOS as $W/L = 16\,\mu\mathrm{m}/60\,\mathrm{nm}$, slightly smaller than those in the TIA, primarily to achieve a modest reduction in power dissipation without compromising the gain. Furthermore, to enable configurable gain operation, the same T-gate switching mechanism is integrated into the feedback resistors of each stage, similar to the approach used in the TIA. The total feedback resistance can be configured as $R_{\mathrm{MA}} = 200\ \Omega$, $350\ \Omega$, or $450\ \Omega$, where $R_{\mathrm{MA}} = R_{\text{switch}} + R'_{\mathrm{MA}}$, and the switch resistance R_{switch} is approximately $90\ \Omega$. This flexibility allows the MA to adapt to varying signal conditions and system-level requirements.

After exploring different stage counts and their impact on performance, a three-stage Cherry-Hooper configuration was selected to achieve the necessary gain and output amplitude for generating logic-detectable signals at the next stage of the circuit.

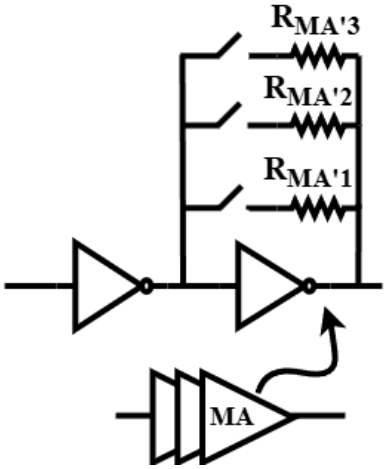

Figure 4.9: Schematic of the three-stage Cherry-Hooper main amplifier.

To assess the frequency response of the amplifier, Fig. 4.10 (a) presents the simulated AC performance for three different feedback resistance settings. For single-stage operation, the simulated

voltage gains for feedback resistances of 200 Ω, 350 Ω, and 450 Ω were 4.37, 5.74, and 6.7, respectively, with corresponding -3 dB bandwidths of 22.45 GHz, 19.2 GHz, and 17.76 GHz. In addition, as shown in Fig. 4.10 (b), when three identical MA stages were cascaded, each configured with $R_{\mathrm{MA}} = 200\ \Omega$, the overall voltage gain increased to 83, while the -3 dB bandwidth was reduced to 12.38 GHz.

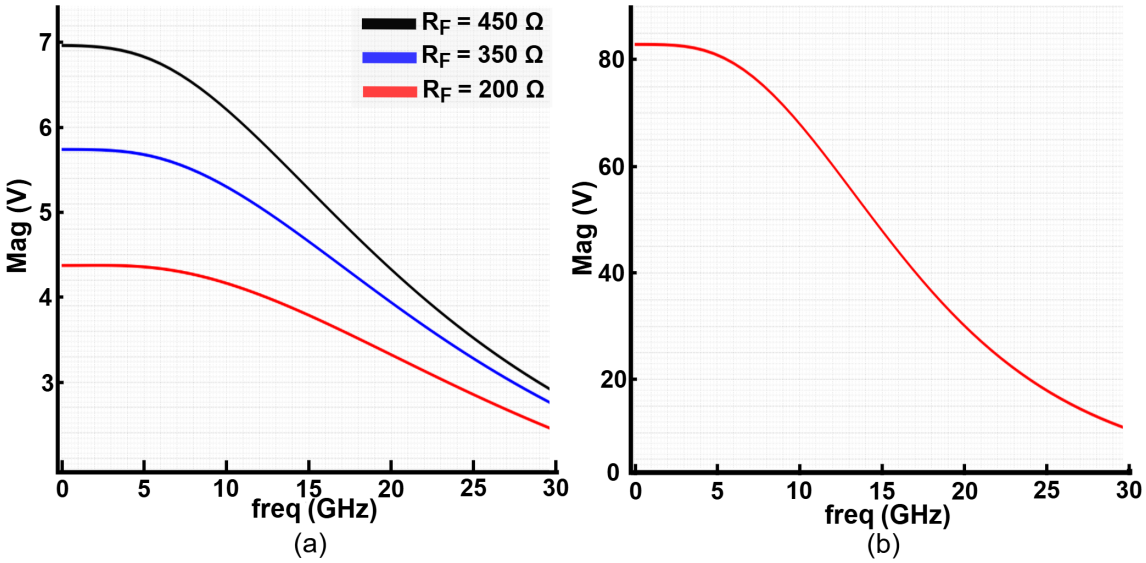

Figure 4.10: (a) Simulated AC response of the MA for different feedback resistance settings. (b) Combined response of the full three-stage MA with $R_{\mathrm{MA}} = 200\ \Omega$ in all stages.

4.1.4 Proposaed DC Offset Compensation (DCOC) Design

As discussed in Chapter 2, conventional DCOC circuits typically employ a low-pass filter to extract the average voltage at the output of the MAs. This average serves as an estimate of the signal level and is used to generate a compensation current that adjusts the input photocurrent accordingly. The objective is to shift the output signal level toward the inverter's threshold voltage, ensuring correct logic evaluation.

However, what truly matters for effective DC offset compensation is not the average voltage itself, but the voltage that lies exactly between the high and low logic levels, referred to here as the middle point. When the input data stream has a balanced 50–50 ratio of logical '1's and '0's, the

middle point coincides with the average voltage. But under unbalanced data conditions, the average deviates from the true middle point, leading to incorrect compensation if conventional methods are used. As illustrated in Fig. 4.11, the proposed compensation scheme replaces the conventional averaging-based approach with a peak/low detector-based DCOC circuit that accurately identifies both the high and low levels of the signal. A peak detector captures the maximum voltage (logic high), while a low detector tracks the minimum voltage (logic low). The middle point is defined as the average of these two voltages, not the average of the entire signal. It represents the true center between logical '1' and '0' levels, regardless of input data density, and must be aligned with the threshold of the logic circuit to ensure correct decision making.

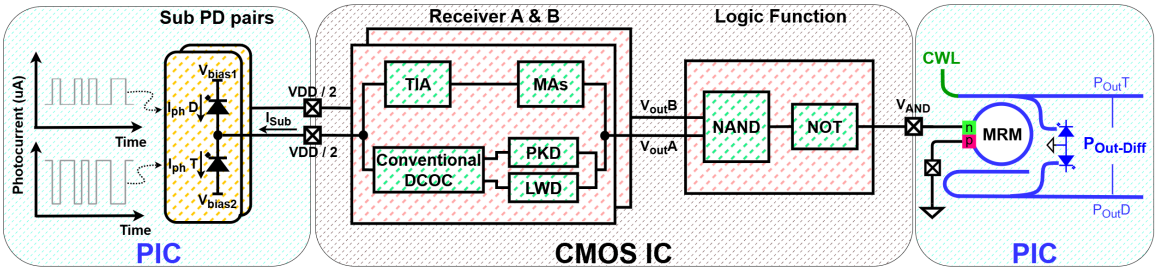

Figure 4.11: Block diagram of the proposed logic control circuit with accurate peak/low detector-based DCOC.

Using peak and low detectors to find the reference voltage is a well-known approach originally developed for burst-mode receivers, where it is typically implemented in a feed-forward path to determine a reference level for single-ended-to-differential circuits or decision circuits. This approach is also effective for compensating offset and mismatch within a single stage. However, if used across multiple stages, separate detector circuits must be employed in each stage. In burst-mode systems, the data arrives in short packets with unpredictable amplitudes and DC offset. In such scenarios, conventional averaging-based DCOC becomes ineffective due to limited observation time, so peak and low detectors offer fast reference extraction, enabling reliable detection even for short bursts [39, 40].

While the peak/low detection concept was originally developed for fast initialization in burst-mode systems, typically in a feed-forward configuration for static reference generation, we employ it

in a continuous feedback configuration, integrated with conventional DCOC, to regulate and center the output signal. Instead of directly setting the reference level for slicing or signal conversion, we use the middle point to generate a compensation current, which shifts the signal toward the inverter's threshold voltage. This approach enables effective compensation for varying densities of '1's and '0's in the input signal, static offsets in the input photocurrent, and accumulated mismatches and offsets across the TIA and all stages of the MAs. In contrast to feed-forward schemes, which would require a separate detector at each stage to remove all non-idealities, the feedback configuration provides unified compensation across the entire receiver chain.

Peak Detector (PKD) Design

This part presents the design of the PKD. The low detector (LWD) circuit follows a complementary structure and functions analogously, forming the second half of the envelope detection system used in the proposed DCOC block.

Fig. 4.12 shows the high-level schematic of the peak detector circuit. The peak detector is implemented using a comparator-based structure that continuously tracks the highest voltage reached by the input signal. The input is connected to the inverting terminal of the comparator, while the stored peak voltage, V_{peak}, is fed back to the non-inverting terminal. The comparator output drives a PMOS pass transistor. When the input signal exceeds the current V_{peak}, the comparator output goes low, turning on the PMOS and charging the capacitor to this new maximum. When the input falls below V_{peak}, the comparator turns off the PMOS, isolating the node and holding the voltage. A large capacitor at the peak node provides stable storage, while a high-value resistor in parallel introduces a slow decay mechanism to enable long-term adaptability.

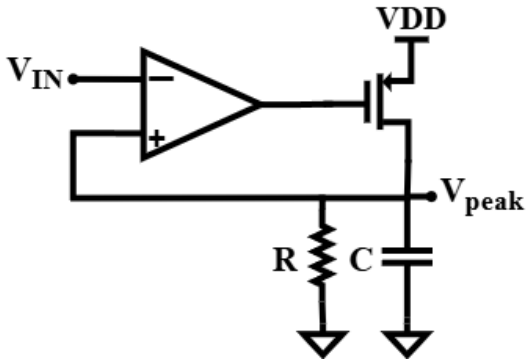

Figure 4.12: High-level schematic of the PKD circuit.

In this design, the sizing of the storage capacitor C and the parallel resistor R is critical to the overall performance of the circuit. Two key factors guide their selection: tracking speed and decay time.

Tracking speed defines how rapidly the peak detector can follow a rising input voltage. Assuming an ideal comparator with instantaneous switching, the PMOS pass transistor turns on as soon as $V_{\text{in}} > V_{\text{peak}}$. For most of this period, the PMOS operates in the triode region and can be modeled by its on-resistance R_{on}. The capacitor charging behavior is then governed by:

$$\frac{dV_{\text{peak}}}{dt} = \frac{1}{R_{\text{on}}C}\left(VDD - V_{\text{peak}}\right) - \frac{V_{\text{peak}}}{R_T C} \tag{37}$$

where R_T denotes the effective resistance formed by the parallel combination of the PKD resistance R and the DCOC resistance R_{DCOC}. The latter corresponds to the following stage in the circuit and will be explained in detail in the next section. From this relationship, it is evident that smaller values of C lead to faster tracking, which is beneficial when the input signal changes rapidly. However, this must be balanced against other factors, such as noise immunity.

The decay mechanism is controlled by the parallel resistor R, which allows V_{peak} to slowly decrease over time when no new peak is detected. In the absence of a charging current, the node discharges approximately as:

$$\frac{dV_{\text{peak}}}{dt} = -\frac{V_{\text{peak}}}{R_T C} \tag{38}$$

This exponential decay behavior is characterized by the RC time constant. While faster decay (smaller RC) may not pose a problem at high data rates, it becomes a concern during low-frequency testing scenarios. For robust and flexible testing, especially in low-speed operation, a longer decay time is preferred, which requires a larger RC time constant. During tracking, the capacitor is charged from VDD through the PMOS on-resistance R_{on}. Although the large RC discharge path to ground is still present, its much longer time constant makes its effect negligible in this phase. As a result, tracking is inherently faster than decay. Therefore, in practice, it is the decay behavior, not the tracking speed, that imposes the dominant timing constraint on the design.

As mentioned, a larger C (and R) ensures long-term peak retention and greater noise immunity. However, this comes at the cost of increased silicon area. Moreover, if the decay is too slow, the detector may fail to adapt to significant shifts in the signal envelope. The final values of R and C are selected to meet these constraints while respecting layout limitations. Based on the area budget, $C = 10\,\text{pF}$ and $R = 1\,\text{M}\Omega$ are chosen to provide adequate discharge behavior and support lower-frequency operation.

As mentioned earlier, the comparator in the peak detector is required to determine when the input signal slightly exceeds the stored peak voltage. To ensure reliable detection under small voltage differences and rapid transitions, the comparator must exhibit high gain and fast response. High gain enables accurate comparison even when the voltage difference between V_{in} and V_{peak} is small, while high speed ensures correct operation under fast-changing input conditions. Fig. 4.13 shows the schematic of the custom two-stage comparator designed to meet these requirements. The comparator operates in continuous-time and directly drives the gate of the PMOS pass transistor in the peak detector.

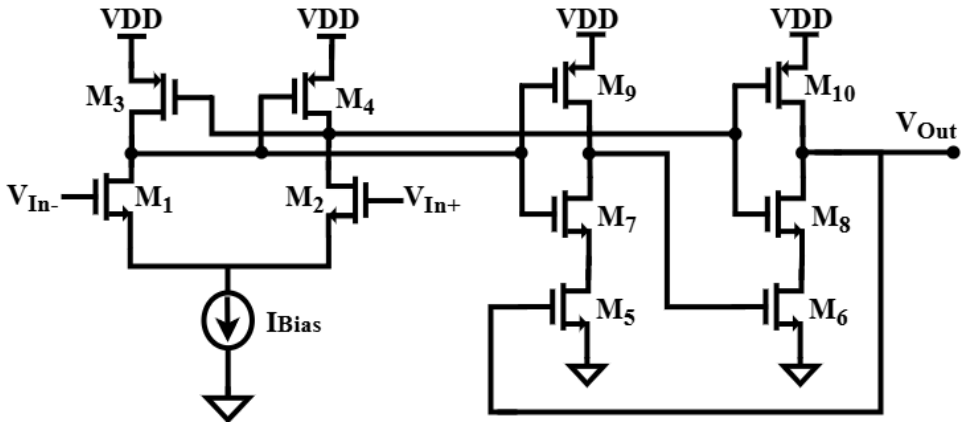

Figure 4.13: Schematic of the two-stage comparator used in the peak detector.

The first stage of the comparator is a differential amplifier with cross-coupled PMOS transistors that introduce regenerative feedback. This feedback increases the gain and sharpens the transition, improving sensitivity to small input differences. To achieve high transconductance and ensure the input pair dominates the behavior, the NMOS transistors are sized significantly larger than the PMOS devices. Specifically, the NMOS input pair uses $W/L = 4 \times 5.4\,\mu\text{m}/60\,\text{nm}$, while the cross-coupled PMOS devices are sized at $W/L = 4 \times 1\,\mu\text{m}/60\,\text{nm}$. This sizing ratio, where the PMOS width is approximately 5.4 times smaller, limits the strength of the regenerative loop (keeps the feedback moderate), ensuring continuous and stable operation. The bias current is chosen to be $850\,\mu\text{A}$ to provide sufficient transconductance for high-speed operation while maintaining a moderate power budget.

As shown on the right side of Fig. 4.13, the second stage consists of two symmetric inverters, each with an additional NMOS gating transistor inserted in series with the pull-down path. All transistors in this stage are equally sized with $W/L = 4 \times 1.8\,\mu\text{m}/60\,\text{nm}$. The differential outputs of the first stage are fed into the inputs of two inverters, whose outputs serve as the final comparator signals. A key feature of this design is the cross-gating configuration: the output of each inverter controls the gating NMOS of the opposite inverter. This cross-coupled structure introduces a regenerative feedback mechanism.

When the input of the second stage changes, one inverter, whose gating NMOS is already enabled, begins to switch; its output transitions high, which in turn enables the gating NMOS of the

opposite inverter. This activation completes the pull-down path on that side, allowing the second inverter to switch in the opposite direction. The cross-coupled feedback reinforces the transition and ensures a fast, decisive output swing. The gating NMOS devices also help prevent either inverter from responding to small or noisy differential inputs, thereby enhancing noise immunity and reducing static power dissipation.

Although this architecture introduces a slight delay, since the initial transition must partially occur before the opposite side is activated, it does not significantly impact the comparator's overall speed. Once switching begins, the regenerative mechanism rapidly drives the output to its final logic level. One minor drawback is that the low output voltage may not reach a perfect 0 V due to the series gating NMOS, especially if it is weakly driven. However, this is acceptable in the given application, as the comparator output controls a PMOS transistor in the following stage, where achieving a strong logic high is more critical for proper turn-off behavior.

A comprehensive set of simulations was conducted to validate the functionality, responsiveness, and stability of the stand-alone comparator and the complete PKD circuit. To emulate actual circuit conditions, the comparator is tested using an input configuration that reflects its role inside the PKD. Specifically, the positive input is fixed at a constant DC voltage, representing the stored peak voltage in the PKD, while the negative input is varied to simulate real-time signal conditions. For the majority of the simulations, a value of 700 mV is selected as a representative peak voltage. It should be noted that any other reasonable value consistent with expected peak levels could be used.

Fig. 4.14 shows the output of the stand-alone comparator under a fine-resolution DC sweep. As mentioned, the positive input is fixed at 700 mV, while the negative input is swept from 697 mV to 703 mV. The goal of this simulation is to evaluate the switching point, ensure the output transitions cleanly, and verify that no flat or ambiguous region exists near the threshold, conditions which could otherwise suggest metastability. As shown, the transition is sharp, continuous, and stable, confirming that the comparator responds decisively to small differential inputs, with a clean switching characteristic and no signs of instability.

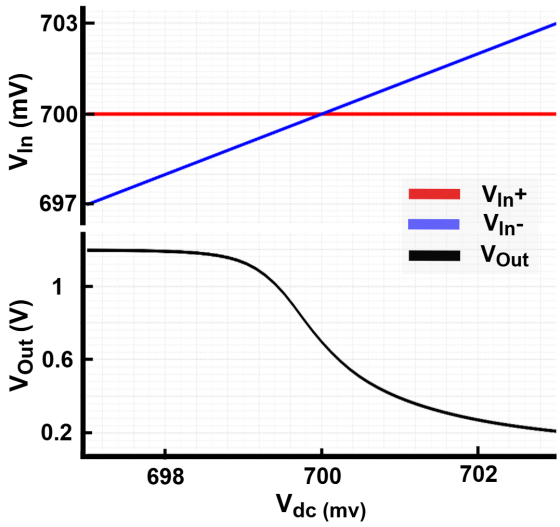

Figure 4.14: DC sweep of the stand-alone comparator, showing a sharp switch near 700 mV.

Fig. 4.15 (a), (b), and (c) show transient simulations of the comparator under various differential input step sizes, each applied with a fast 10 ps rise time. These tests evaluate dynamic behavior, regeneration speed, and overall stability across different input amplitudes.

As shown in Fig. 4.15 (a), the first case applies a differential step of 2 mV, pushing the comparator to its sensitivity limit. Despite the minimal input swing, the output transitions fully within approximately 1.5 ns, and no signs of metastability or hesitation are observed. This confirms that the comparator remains responsive and stable even under extremely small-signal conditions.

The second case uses a 30 mV step. As shown in Fig. 4.15 (b), the comparator responds within 0.8 ns, with a sharp and clean output transition. No overshoot, ringing, or output fluctuations are observed.

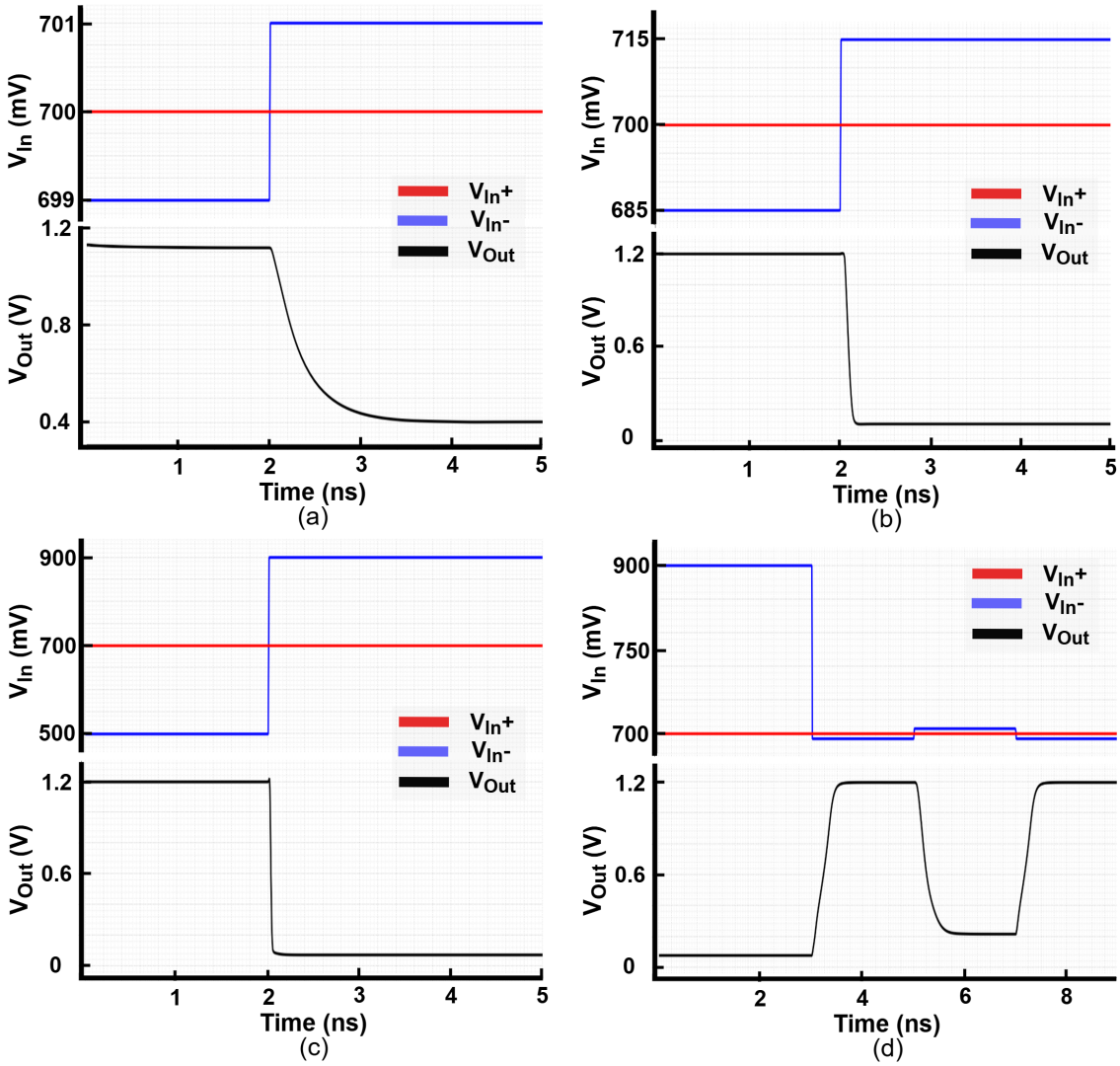

Figure 4.15: Transient response to: (a) a 2 mV input step, (b) a 30 mV input step, (c) a 400 mV input step. (d) Overdrive recovery test.

The final test, shown in Fig. 4.15 (c), applies a 400 mV differential step to assess behavior under overdrive. The output switches in less than 100 ps, and again, the transition is smooth and without any oscillations. Across all cases, from sub-millivolt steps to large swings, the comparator exhibits clean transitions, no overshoot, and no oscillatory artifacts. These results collectively confirm that the design is dynamically stable, with a regenerative feedback that accelerates switching with larger input overdrive, making it well-suited for high-speed logic applications.

Fig. 4.15 (d) shows the result of an overdrive recovery test designed to evaluate whether the comparator experiences memory effects, hysteresis, or degraded regeneration behavior after being driven into saturation. In this simulation, a large differential input is first applied by setting $V_{\text{in+}} = 800\,\text{mV}$ and holding it constant for 3 ns, fully saturating the output. At the 3 ns mark, the input transitions to small-swing differential signals ($\pm 3\,\text{mV}$) to observe whether normal regeneration resumes. As shown, the comparator output correctly saturates during the overdrive phase, and then immediately returns to full logic-level transitions once the small-signal inputs are applied. There is no evidence of latching, residual memory, or metastability. In addition, the three full output transitions observed in response to the $\pm 3\,\text{mV}$ input swings confirm that the comparator does not exhibit any noticeable hysteresis under these conditions.

As illustrated in Fig. 4.16 (a), To validate the overall behavior of the full PKD loop under realistic input conditions, a transient simulation was performed using a triangular waveform as the input signal. The full PKD loop was connected, including the comparator, PMOS pass transistor, storage capacitor, and discharging resistor. The goal of this test was to verify whether the stored peak voltage V_{peak} updates correctly during input ramps and holds its value during falling slopes. The comparator output switches only once per input peak and maintains a stable state throughout the hold phase. Additionally, no overshoot or oscillation was observed at the peak node. To further assess robustness, the triangle input was later replaced with a constant voltage. As expected, the stored peak voltage remained stable throughout the test. Furthermore, Fig. 4.16 (b), plotted on a longer time scale, shows the decay of the PKD output when the new peak is lower than the previously detected voltage. As illustrated, V_{peak} decreases until it reaches the new peak level and then remains constant. These results demonstrate the correctness and stability of the complete peak detector in both dynamic and static conditions.

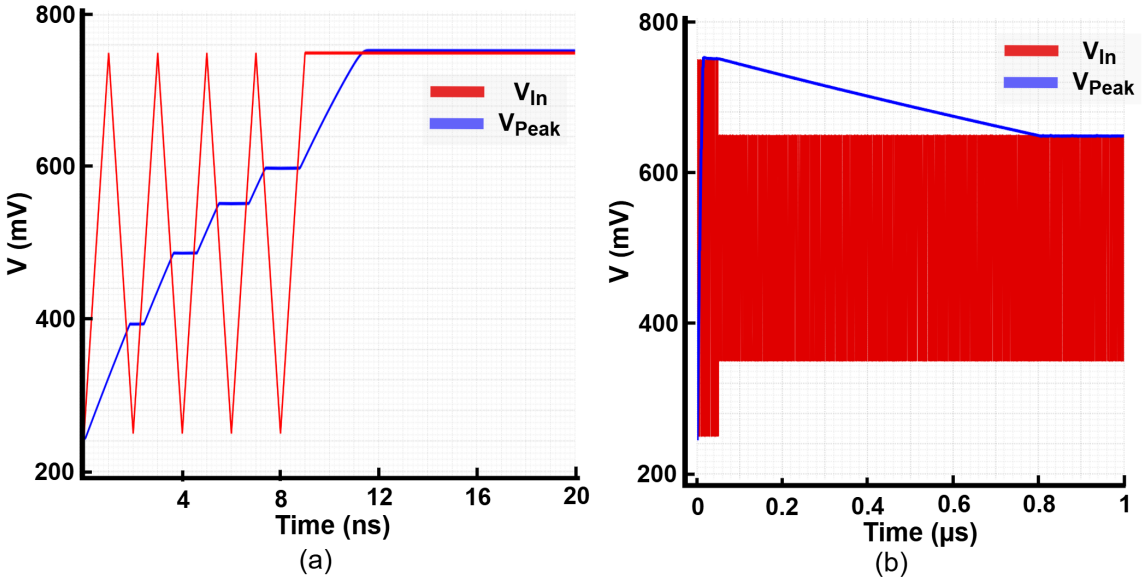

Figure 4.16: Full PKD simulation with a triangular wave input: (a) tracking and hold operation; (b) decay and detection of a new peak.

Low Detector (LWD) Design

To complement the envelope detection mechanism, a Low Voltage Detector (LWD) is implemented using a symmetric architecture to track the minimum voltage level of the input signal. Like the PKD, the LWD continuously monitors the signal envelope and updates its stored voltage, V_{low}, whenever a new minimum is observed.

Fig. 4.17 shows the high-level schematic of the LWD. The circuit operates in a complementary manner to the PKD. Specifically, the input signal is applied to the inverting input of a comparator, while the stored low voltage V_{low} is fed to the non-inverting terminal. When the input drops below V_{low}, the comparator output transitions high, turning on the NMOS pass transistor. This allows the capacitor to discharge and follow the new minimum. Once the input signal starts to increase again, the comparator output goes low, turning off the NMOS and isolating the low-voltage node. A high-value resistor in parallel with the capacitor introduces a slow upward decay, allowing the LWD to gradually adapt to long-term shifts in signal baseline. A slow RC decay causes V_{low} to rise over time in the absence of new minima. Together, the PKD and LWD define a dynamic envelope of the

input signal, from which the middle point is calculated and used for DC offset compensation.

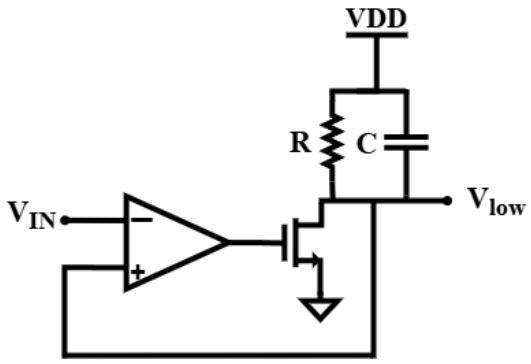

Figure 4.17: High-level schematic of the LWD, complementary to the PKD.

The sizes of the storage capacitor and discharge resistor used in the LWD are identical to those used in the PKD circuit, specifically $C = 10\,\text{pF}$ and $R = 1\,\text{M}\Omega$, to maintain consistent timing characteristics and ensure symmetrical envelope tracking.

Fig. 4.18 shows the schematic of the comparator used in the LWD. Its structure is flipped relative to the PKD comparator because the LWD must detect minima rather than maxima. In this orientation, the PMOS transistors serve as the input devices of the first stage, which is particularly advantageous since they operate effectively with low input signals. This complementary arrangement ensures proper low detection while preserving symmetry in gain, speed, and switching behavior across both detectors.

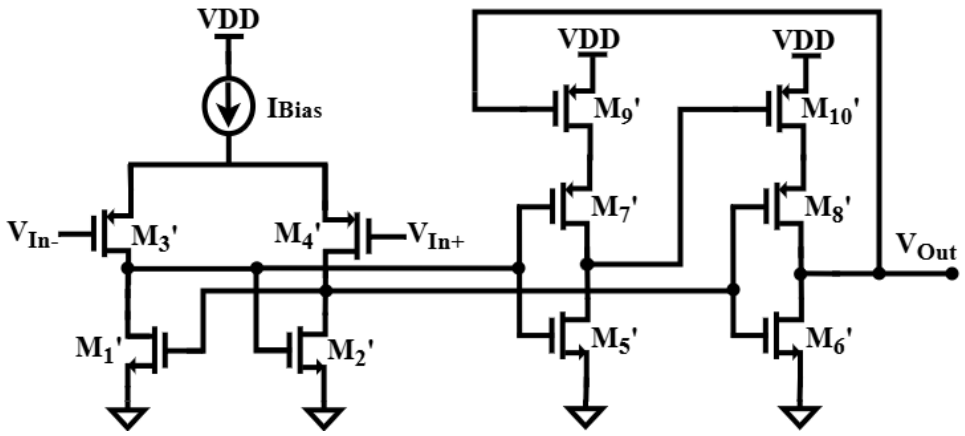

Figure 4.18: Schematic of the comparator used in the LWD circuit. It follows the same structure as the PKD comparator but with complementary devices.

Middle-Point Based DCOC Integration

As shown in Fig. 4.19, the detected peak and low voltages from the PKD and LWD circuits, rather than the main signal, are provided as inputs to a conventional DCOC block. As described in Chapter 2, this block functions as an integrator that produces a correction signal based on the error between a reference voltage and the DCOC input. In this implementation, the input to the DCOC is the average of the peak and low voltages—that is, the dynamically tracked middle point of the signal envelope.

The DCOC circuit integrates this error over time and produces a compensation signal that controls the gate of a transconductance inverter in the next stage. This inverter adjusts the bidirectional input current delivered to the TIA, effectively shifting the TIA's DC operating point toward the desired region (typically near the inverter threshold voltage), enabling proper logic-level detection even under highly unbalanced input data.

The current injected into the integrator stage is calculated based on the difference between the reference voltage and both detected peak and low voltages:

$$I_{\text{INT}} = \frac{V_{\text{ref}} - V_{\text{peak}}}{R} + \frac{V_{\text{ref}} - V_{\text{low}}}{R} = \frac{V_{\text{ref}} - V_{\text{mid}}}{R/2} \tag{39}$$

Here, V_{mid} is the middle point of V_{peak} and V_{low}, representing the true center of the signal's

logic swing. This expression ensures that the integrator reacts to deviations of the signal midpoint from the reference and provides a stable long-term correction that adapts to both static offsets and dynamic changes in input conditions. The integrator uses $R = 1$ MΩ resistors and a capacitor of $C = 10$ pF. These resistors form high-impedance DC paths from V_{peak} and V_{low} to the integrator input at V_{ref}, allowing the DC-level information to be extracted without significantly loading the previous stages or disrupting integration behavior.

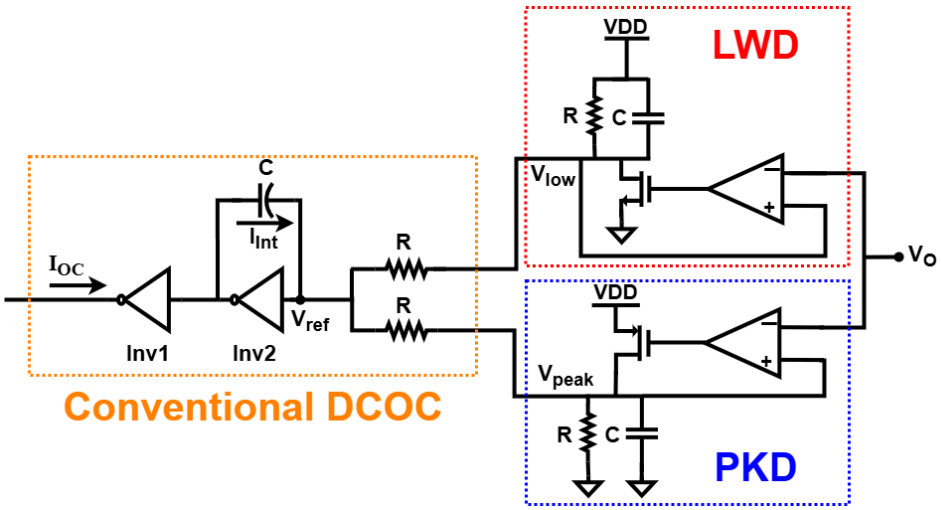

Figure 4.19: Proposed DCOC block.

4.1.5 NAND Gate and Output Inverter Design

As described throughout this chapter, the proposed logic control circuit includes all necessary building blocks to realize an optical receiver capable of processing unbalanced input data while ensuring correct signal restoration and centering. Referring back to the system-level diagram in Fig. 4.4, two such receiver chains are employed, one for each optical input signal, resulting in the generation of clean and amplified electrical signals, labeled Out_A and Out_B, suitable for further digital processing.

To implement a NAND logic function, a simple static CMOS NAND gate is constructed using the outputs Out_A and Out_B as inputs. The schematic of the NAND gate followed by a CMOS inverter is shown in Fig. 4.20. The inverter is used to invert the output and restore full rail-to-rail logic levels, thereby ensuring reliable driving capability for the MRM.

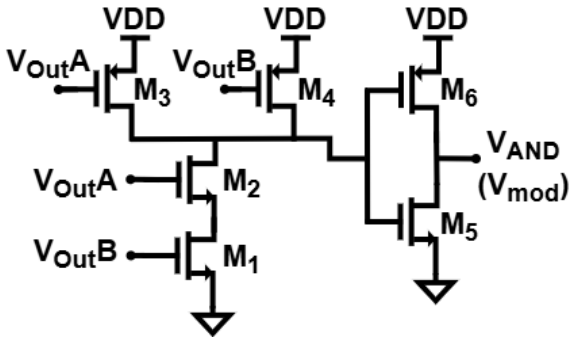

Figure 4.20: Schematic of the electrical NAND gate followed by an inverter.

While this electrical combination yields a digital AND function at the output, it is essential to consider the optical inversion characteristic of the MRM used in the following stage. As discussed in Chapter 3, due to the inverse relationship between the output optical power and the modulation voltage, the MRM effectively acts as an optical inverter, assuming the thermal controller locks the operating point on the right side of the resonance. By utilizing this property, the electrical AND output effectively drives an optical inverter. The final result is a functional NAND logic gate in the electro-optical domain.

In the logic chain, the MA stage preceding the NAND gate is implemented with identical PMOS and NMOS dimensions. The inverter that follows the NAND gate also uses a symmetric configuration, with both transistors sized at $W/L = 10 \times 2\,\mu\text{m}/60\,\text{nm}$. This uniform sizing helps maintain a consistent switching threshold across the circuit and ensures reliable modulation of the MRM.

The NAND gate was initially sized in the schematic following standard CMOS design principles. To compensate for the increased resistance of the stacked NMOS transistors in the pull-down network, each NMOS was sized at $W/L = 20 \times 2\,\mu\text{m}/60\,\text{nm}$, which is twice the width of the NMOS used in the subsequent inverter. The PMOS pull-up transistors, which are not stacked, were sized at $W/L = 10 \times 2\,\mu\text{m}/60\,\text{nm}$, the same as the PMOS width of the following inverter stage.

However, post-layout simulations revealed that the DC output level of the preceding receiver stages was slightly lower than in the schematic. This discrepancy may be attributed to layout-related effects such as parasitic coupling and localized voltage drop due to resistance in the on-chip power grid. As a result, the input to the NAND gate's PMOS transistors experienced an increased

source-gate voltage (V_{SG}), making the pull-up network comparatively stronger than intended.

To preserve balance and avoid further degradation in speed due to increased parasitics, the NMOS sizing was left unchanged. Instead, the PMOS width was reduced to $W/L = 5\times2\,\mu\text{m}/60\,\text{nm}$. This adjustment reduces the pull-up strength, compensating for the lower input midpoint. As a consequence, small glitches and slight asymmetry between the rise and fall times may occur.

4.2 Post-Layout Simulation Results

Fig. 4.21 shows the layout of one receiver arm of the proposed circuit (e.g., Arm A), along with the NAND gate and the output inverter. Arm A includes the TIA, three stages of Cherry–Hooper MAs, PKD, LWD, and the conventional DCOC block. For visual clarity, only Arm A is shown, as Arm B is an identical replica that feeds the complementary side of the NAND gate.

Each individual circuit block is labeled in the figure. The large capacitors and resistors visible in the layout correspond to the PKD, LWD, and DCOC circuits. The resistors appear as large solid blocks in the layout, but each is actually implemented as a series combination of many smaller segments arranged in a meandered pattern. As discussed in their respective subsections, these passive components are intentionally sized to support low-speed testing scenarios. For high-speed operation, their sizes can be reduced without compromising performance.

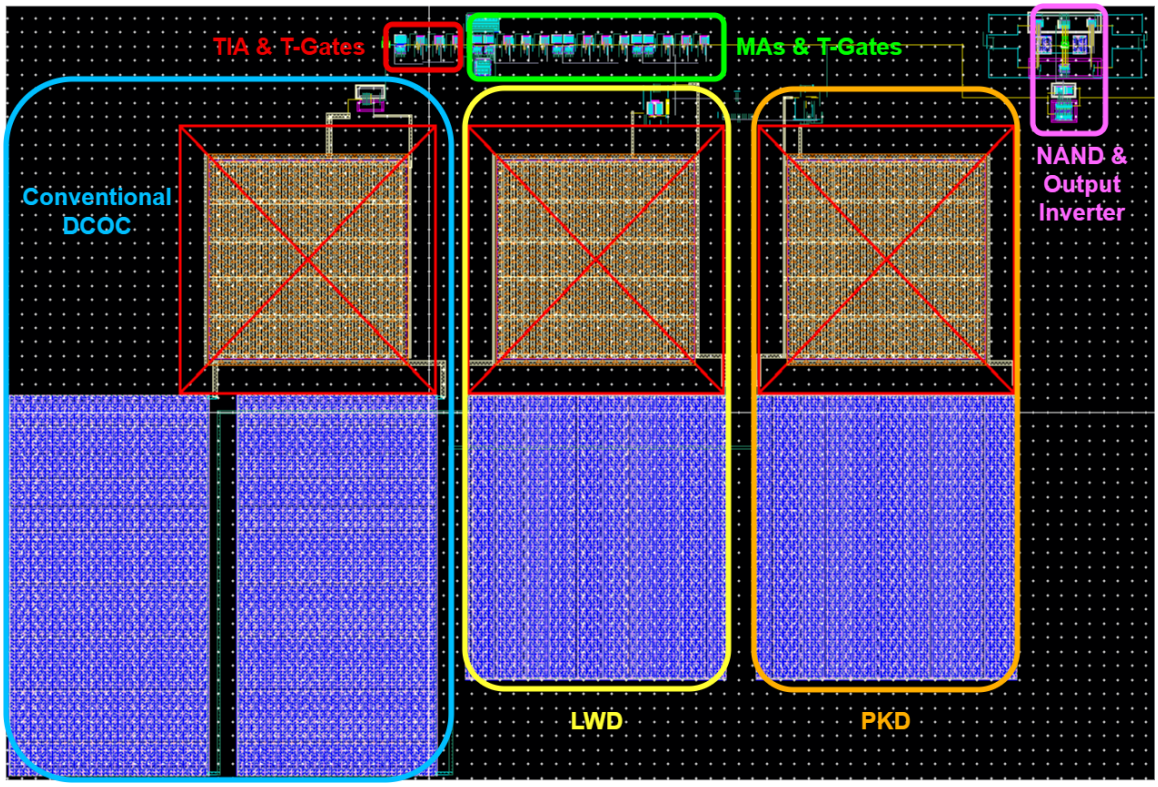

Figure 4.21: Layout of one receiver arm of the proposed circuit (e.g., Arm A), along with the NAND gate and the output inverter

To evaluate the robustness and dynamic response of the proposed circuit, a series of post-layout simulations were performed under challenging input conditions. These tests included varying the input data density of logical '1's from 10% to 90% in 10% increments, as well as directly transitioning between extreme cases (e.g., from 10% to 90% density). All density tests were conducted at data rates of 1 Gbps and 100 Mbps. This moderate speed was chosen to keep the simulation time within a reasonable range, as capturing the full behavior during slow transitions in data density under post-layout conditions required simulating a long duration. Running equivalent tests at the maximum supported data rate would have taken over 24 hours or more per scenario due to the increased time resolution.

Finally, the performance of the full circuit was simulated at the maximum data rate. Two different pseudo-random signals with 50% logical '1's were applied to the receiver inputs. This case

demonstrates the correct operation of the logic control circuit under high-speed conditions.

4.2.1 Behavior Under Input Densities of logical '1's from 10% to 90% in 10% Increments

To evaluate the resilience of the proposed receiver architecture against variations in input data density, a set of input photocurrent waveforms was applied to Arm A of the circuit. Fig. 4.3 illustrates the applied photocurrent, which starts with 10% density of logical '1's and increases progressively to 90% in steps of 10%. The initial segment (10% density) lasts for 2 us, followed by a 20% density segment lasting 1 us. Each subsequent density level increases by 10% and persists for 1 us.

As previously noted, the sharp transitions between density levels shown in Fig. 4.3 are idealized for simulation purposes. In practice, the input current of the cascaded gate would vary more gradually due to the finite response time of the thermal control circuit of the preceding gate.

Fig. 4.22 (a) shows the output voltage of the proposed receiver (i.e., output of the third MA) under the applied varying-density input. The black horizontal line in the plot indicates the inverter's threshold voltage as a reference voltage, around which the signal is expected to remain centered. Despite significant variation in input current levels and logic densities, the signal is consistently centered around the threshold voltage of the CMOS inverter. This confirms that the peak/low detector-based DCOC effectively stabilizes the offset level of the amplified signal, making sure the signal can still be correctly read even when the input is unbalanced. In contrast, Fig. 4.22 (b) displays the corresponding output of a conventional DCOC-based receiver under the same input conditions. It can be clearly observed that the signal shifts significantly as the input density changes, revealing that the signal's average level is affected by changes in input density in conventional DCOC-based receivers.

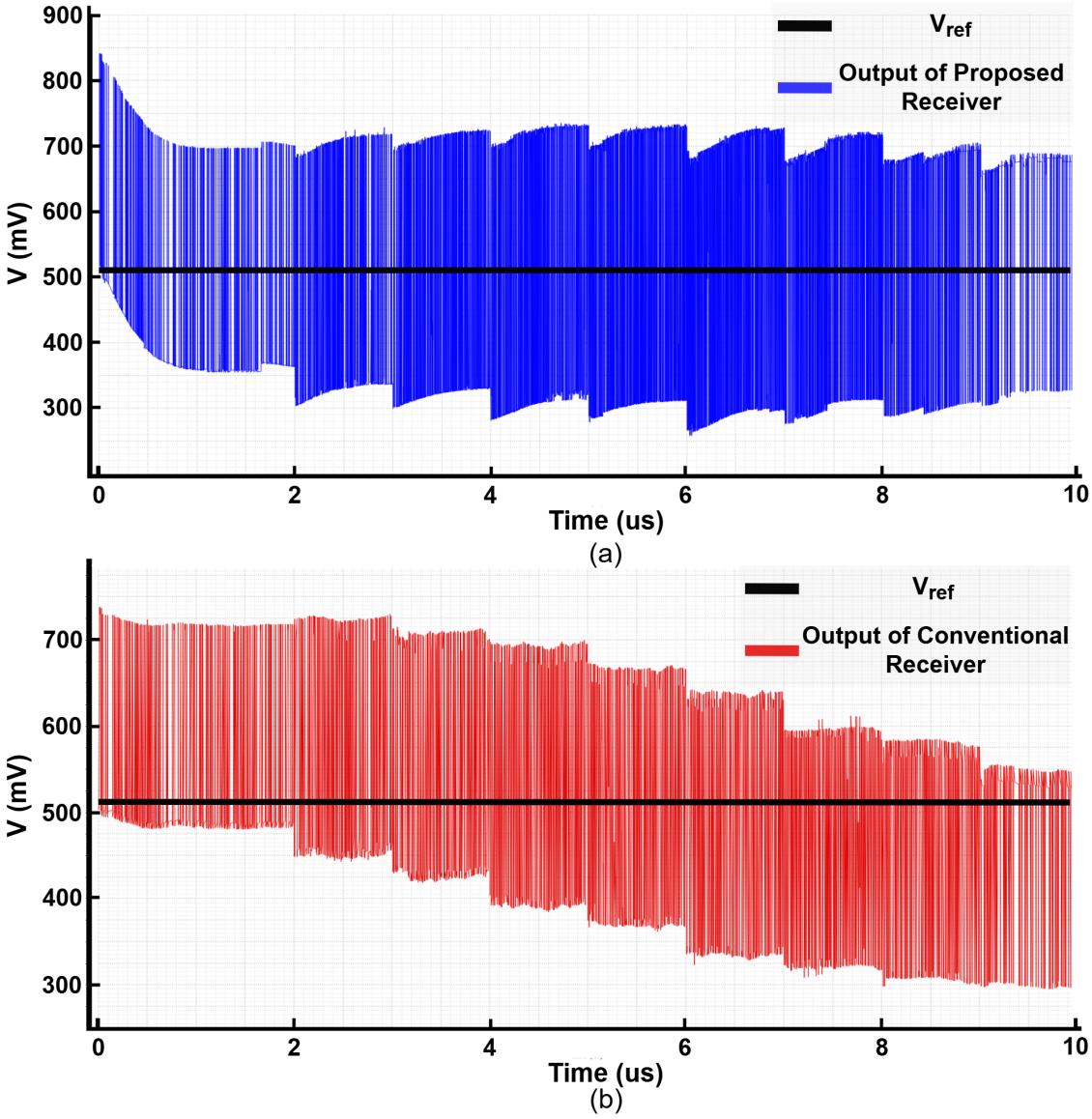

Figure 4.22: Receiver output voltages under varying input data densities (10%–90%): (a) proposed receiver, (b) conventional receiver.

To further validate signal integrity, Fig. 4.23 presents the eye diagrams corresponding to both the proposed and conventional receivers. Fig. 4.23 (a) demonstrates a wide-open eye centered around a stable threshold, indicating strong noise margins and minimal baseline drift in the proposed architecture. Conversely, Fig. 4.23 (b) shows the eye diagram for the conventional DCOC-based receiver,

where eye closure and vertical offset are evident due to the drifting signal midpoint.

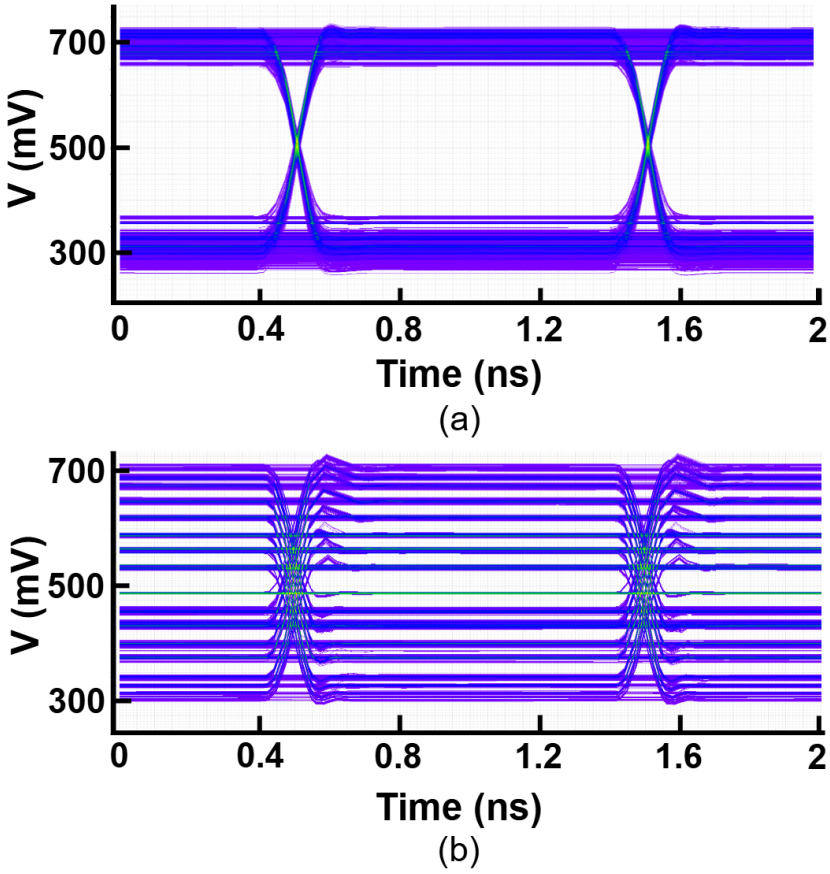

Figure 4.23: Eye diagrams for the (a) proposed and (b) conventional receivers under varying data densities.

These results confirm that the proposed logic control circuit, featuring a peak/low detector-based OC, effectively maintains signal integrity by compensating for input data asymmetry across a wide range of conditions.

4.2.2 Behavior Under a Direct Transition from 10% to 90% Input Density (Worst-Case Scenario)

Fig. 4.24, provided by Daniel Musat, illustrates a worst-case input condition where the logical '1' density of the input signal of he cascaded gate abruptly changes from 10% to 90%. This waveform corresponds to the output of the preceding logic gate, influenced by its thermal control circuit. In the first segment of the figure, the preceding MRM is not yet thermally locked. At 4 ms, the data pattern switches to 90% density. Due to the tuning mechanism of the thermal control circuit, it takes approximately 70–80 μs for the system to stabilize to the new level.

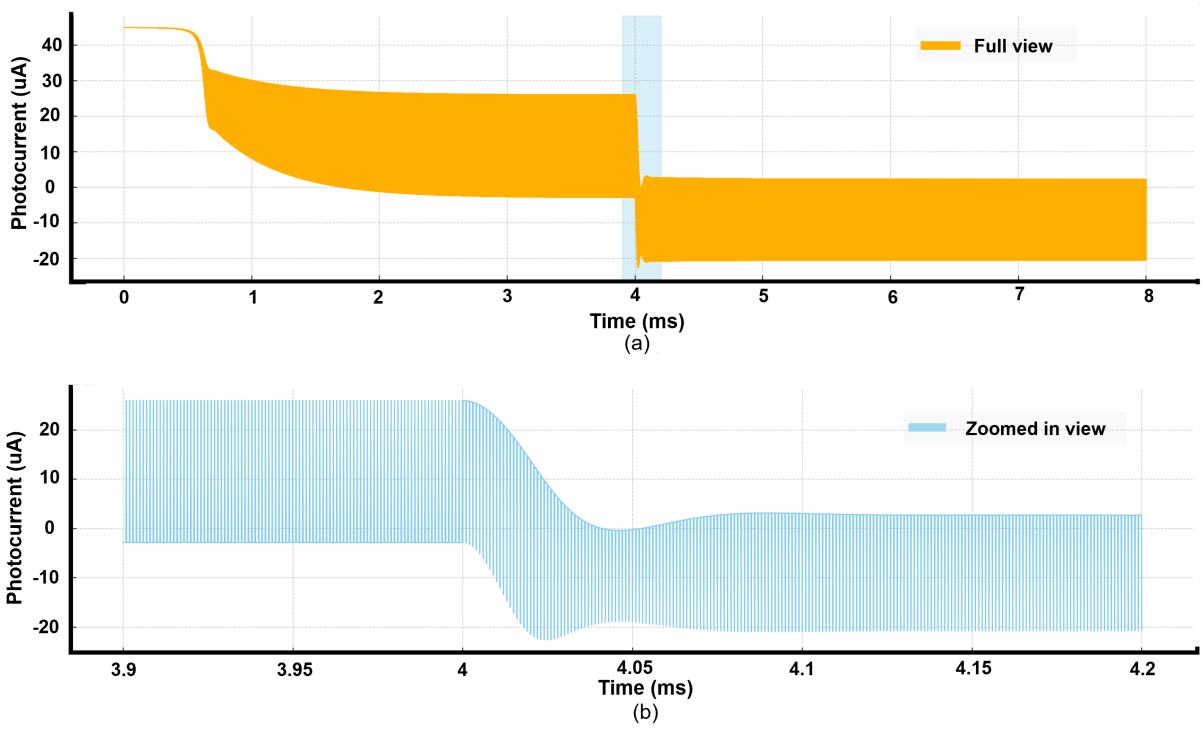

Figure 4.24: Input photocurrent waveform showing a direct transition from 10% to 90% input density; (a) full view, (b) zoomed-in view.

Simulating such a scenario with post-layout netlists at realistic time scales requires excessive simulation time. Therefore, for practical evaluation, a test with 10× compressed transition time was created. In this accelerated test, the transition occurs in approximately 7–8 μs instead of 70–80 μs,

preserving the core dynamics but reducing total simulation time.

Fig. 4.25 shows the bidirectional input current waveform used to test this accelerated worst-case transition, applied to the proposed receiver circuit at a data rate of 100 Mbps. The red curve represents a transition from 10% to 90% logic '1' density, while the blue curve shows the reverse transition from 90% to 10%. The response of the receiver demonstrates that the circuit can handle an even more abrupt transition than what would occur in a real system.

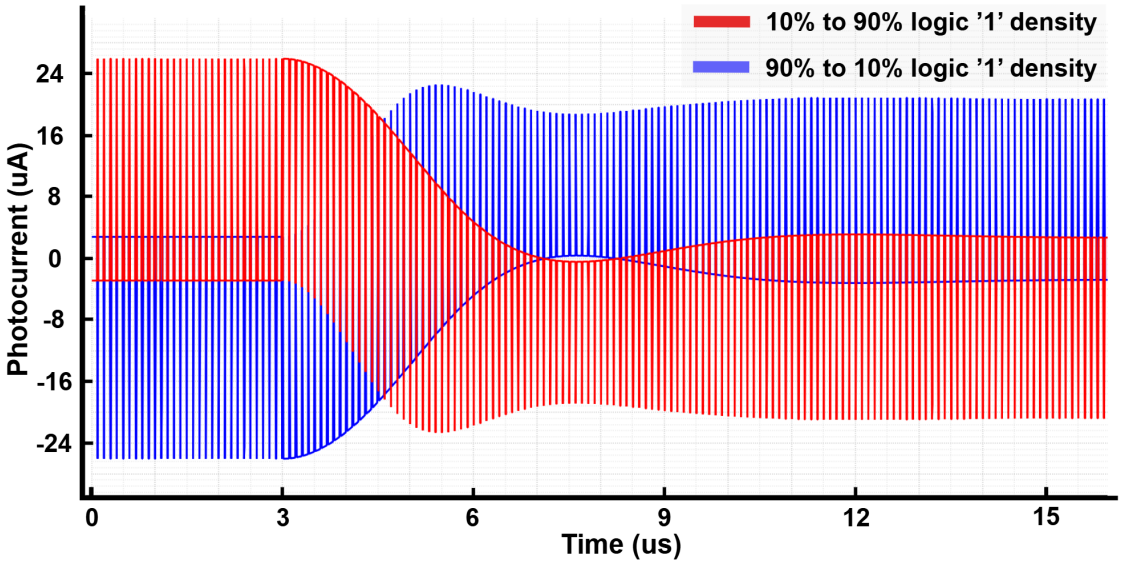

Figure 4.25: Input bidirectional photocurrent with 10× faster transition: from 10% to 90% logic '1' density (red curve) and from 90% to 10% logic '1' density (blue curve).

Fig. 4.26 (a) shows the output of the receiver during both 10% to 90% and 90% to 10% transitions. The black horizontal line in the plot indicates the inverter's threshold voltage, around which the signal is expected to remain centered. The output remains centered and stable, confirming the effectiveness of the peak/low detector-based DCOC in handling abrupt asymmetry in input density. However, a small residual overshoot is observed following each transition. As explained in the relevant subsection, the tracking time of the peak and low detectors is much faster than their decay time. For instance, when the logic '1' density increases from 10% to 90%, the signal tends to shift downward. The low detector quickly tracks the new minimum voltage, while the peak detector decays

more slowly. As a result, the calculated middle point (the average of peak and low) is slightly higher than the true center of the signal, causing the DCOC circuit to drive the level lower than needed, resulting in a temporary downward overshoot. A similar effect causes the upward overshoot during the 90% to 10% transition (this time, the peak detector tracks the new high level quickly, while the low detector decays more slowly). In realistic scenarios where the transition occurs $10\times$ more slowly, as in the actual worst-case input shown in Fig. 4.24, the detectors have enough time to respond, and the overshoot effect is no longer observed. For comparison, Fig. 4.26 (b) displays the response of a conventional DCOC-based receiver under the same input condition. In this case, a noticeable shift in signal levels is observed.

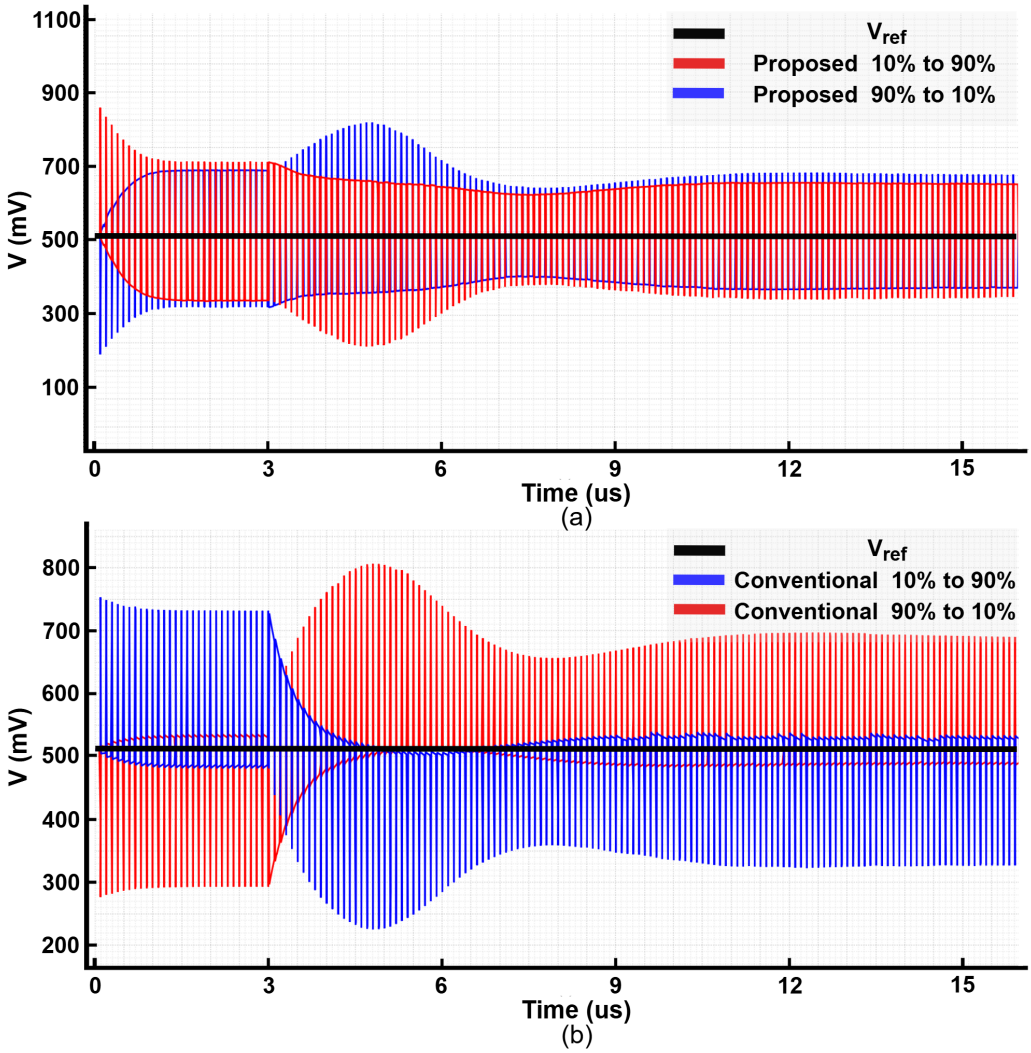

Figure 4.26: (a) The proposed and (b) conventional receiver output during worst-case density (10% to 90% and 90% to 10%) transitions.

It is important to note that this settling time is determined by the thermal control circuit and is independent of the input signal's data rate. Therefore, the circuit's ability to stabilize after abrupt density changes remains valid across different data rates. For the correct functionality of the proposed DCOC scheme, a qualitative hierarchy between the relevant time constants must be maintained. Specifically, the bit-level transitions must be much faster than the response of the peak and low detectors so that these detectors track only the slowly varying signal envelope rather than individual bits. The DCOC integrator should be slightly slower to provide stable offset cancellation

without chasing residual fluctuations. When the peak and low detectors are chosen sufficiently slow such that their outputs are effectively quasi-DC, the DCOC time constant may be set equal to theirs without degrading performance. Finally, the thermal control loop should remain the slowest process in the system. This qualitative ordering guarantees that the proposed circuit responds smoothly to envelope changes while maintaining immunity to short-term bit pattern variations.

4.2.3 High-Speed Functionality Test with Balanced Input Signals at 8 Gbps

To evaluate the performance of the proposed receiver and logic control circuit under high-speed conditions, a set of balanced input signals with 50% logical '1' density was applied to both receiver arms. The input data rate was set to 8 Gbps, representing the maximum operating speed achievable by the circuit in its stand-alone configuration, independent of synchronized system constraints.

Before analyzing eye diagrams, a time-domain transient simulation was conducted to observe the actual logic transitions in real time. Fig. 4.27 presents the time-domain waveforms captured at multiple stages of the logic path: the outputs of the two receiver arms, the NAND gate output, and the final AND signal. The waveforms clearly demonstrate correct logical operation, with sharp transitions and timing alignment across all stages, validating high-speed functionality from input detection to final logic generation. As shown in the figure, the NAND output exhibits variation in its logical '1' level. This occurs because, out of the four possible combinations of NAND inputs, only the case '11' produces a logical '0', while the remaining three cases ('00', '01', '10') all result in a logical '1'. In conventional digital systems, NAND gate inputs are driven by rail-to-rail signals (VDD and GND), producing a uniform '1' level at the output across different input cases. However, in this system, the inputs to the NAND gate, Receiver_OutA and Receiver_OutB, swing between approximately 300 mV (representing logical '0') and 700 mV (representing logical '1'). These non-ideal logic levels lead to slight variations in the output '1' level of the NAND gate, depending on the specific input combination. This variation is effectively eliminated in the subsequent logic stage, where the final AND output is regenerated to stable and consistent logic levels. It should be noted that with higher receiver gain, the NAND input amplitude increases, bringing the signal levels closer to rail-to-rail operation. This reduces the variation observed in the logical '1' output and supports the claim that rail-to-rail inputs improve output consistency prior to regeneration in

the following stage. However, higher gain can also reduce the circuit bandwidth and potentially degrade signal quality at high speeds.

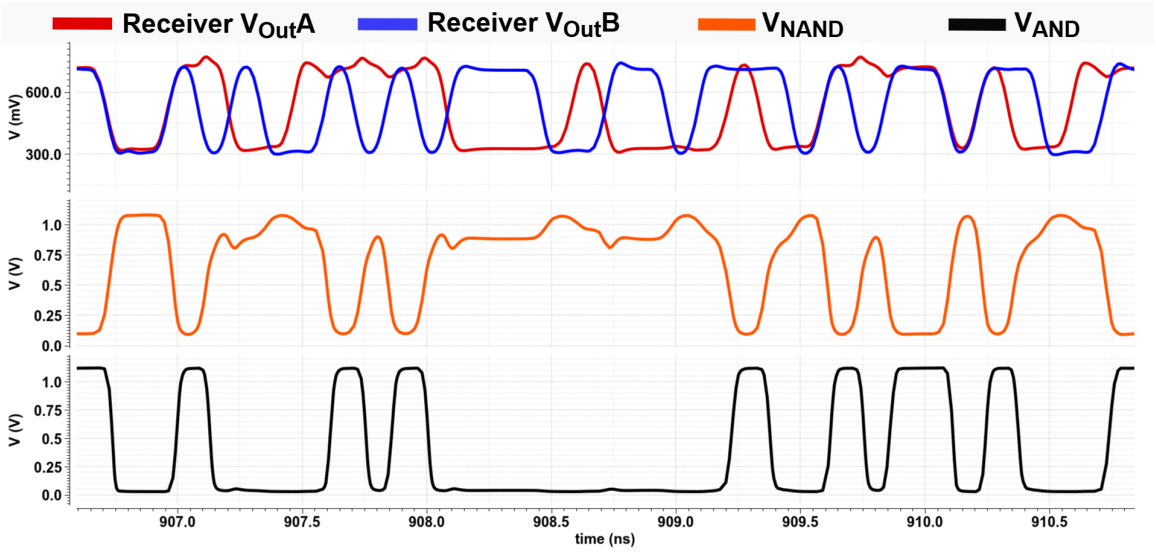

Figure 4.27: Transient simulation results under 8 Gbps balanced input conditions showing the outputs of the two receiver arms, the NAND gate output, and the final AND signal.

Fig. 4.28 (a) and (b) show the eye diagrams at the output of the Cherry–Hooper amplifier chain of both receiver arms. As seen in the figures, both receivers produce clean and wide-open eyes with well-centered thresholds, confirming the robustness of the proposed architecture and its capability to process high-speed input currents while maintaining strong signal integrity.

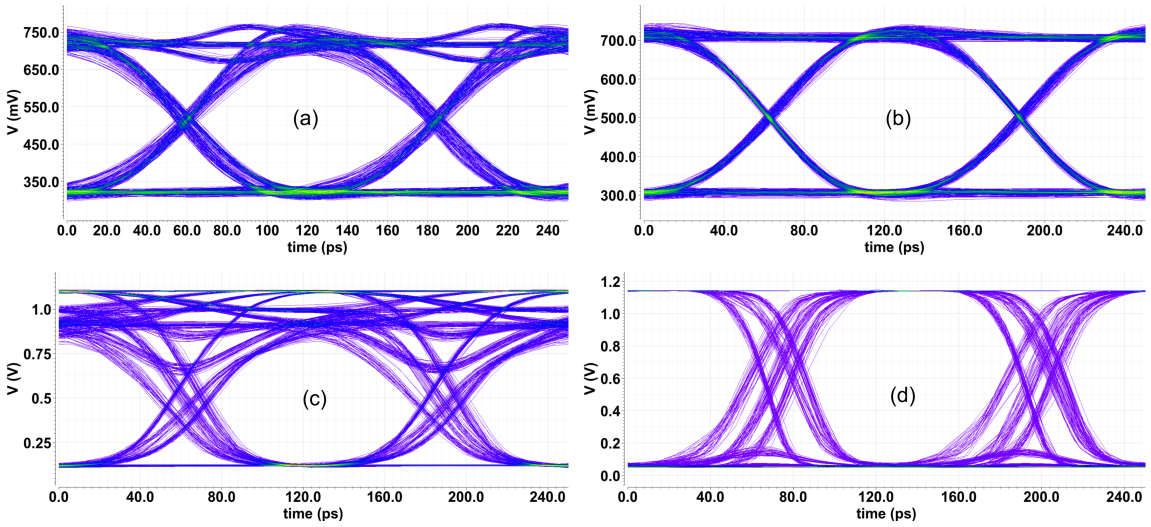

Figure 4.28: Eye diagrams under 8 Gbps balanced input signals (50% logical '1's): (a) Receiver Arm A output, (b) Receiver Arm B output, (c) NAND gate output, (d) Final AND signal.

Furthermore, Figures 4.28 (c) and (d) present the corresponding eye diagrams at the output of the NAND gate and the final AND signal, respectively. These outputs demonstrate successful high-speed logic operation, where the AND signal is asserted only when both inputs are high, as expected from the logical operation of the NAND gate followed by the output inverter.

These results confirm that the proposed peak/low detector-based OC, together with the TIA, the Cherry–Hooper amplifier chain, and the logic function stage, can reliably operate at 8 Gbps and accurately perform logic-level detection and NAND/AND processing at full speed. The total power dissipation of the circuit is approximately 59 mW. Additionally, the average delay between the input bidirectional photocurrent and the final AND output signal is simulated to be 107 ps.

As mentioned earlier, in synchronous cascaded logic systems, practical clock frequencies are typically several times slower than the inverse of the propagation delay. Applying the same 5–10$\times$ factor to the propagation delay yields a safe practical clock range of approximately 1–2 GHz for the synchronized system.

4.2.4 PTC and ONM Simulations for an Optical NOT

To evaluate the PTC and ONM of the IC-level OLG, as shown in Fig. 4.29, the electrical NAND gate within the IC implementation was replaced with an inverter having the same gain. This modified configuration was used for the subsequent simulations.

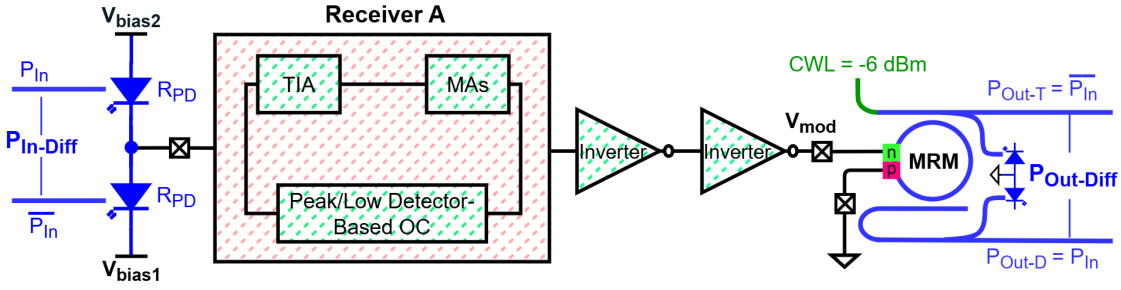

Figure 4.29: Schematic diagram of the simulated optical NOT gate configuration used for PTC and ONM analysis.

Because the PKD, LWD, and DCOC circuits operate in the time domain and require sufficient time to settle to their steady-state values, the simulation was performed in multiple time-transient runs. The input photocurrent amplitude was varied from very small values to larger ones, and for each value, a simulation was performed to allow the circuit to reach steady state before recording the corresponding output voltage.

The simulated output voltage was then mapped to the optical output power using the differential output power versus V_{rb} characteristic presented in Fig. 2.7 (b) of Chapter 2. In this mapping, the following parameters were considered:

- Input CWL power of -6 dBm,
- 2 dB insertion loss in the optical path,
- 10:90 splitter ratio after the microring modulator (10% to the thermal control circuit and 90% to the next OLG),
- Modulation voltage range of 0–1.2 V,

- PD responsivity of 0.8 A/W.

Using these values, the simulated curves in Fig. 4.30 (a) and (b) were obtained. Fig. 4.30 (a) shows the PTC for the given OLG, plotting the optical output differential power against the optical input differential power. As shown in Fig. 4.30 (b), and as expected, the maximum optical gain for this OLG is -9.2. From these results, the optical noise margins are approximately $\mathrm{ONM_H} = 13.4\ \mu\mathrm{W}$ and $\mathrm{ONM_L} = 14.4\ \mu\mathrm{W}$.

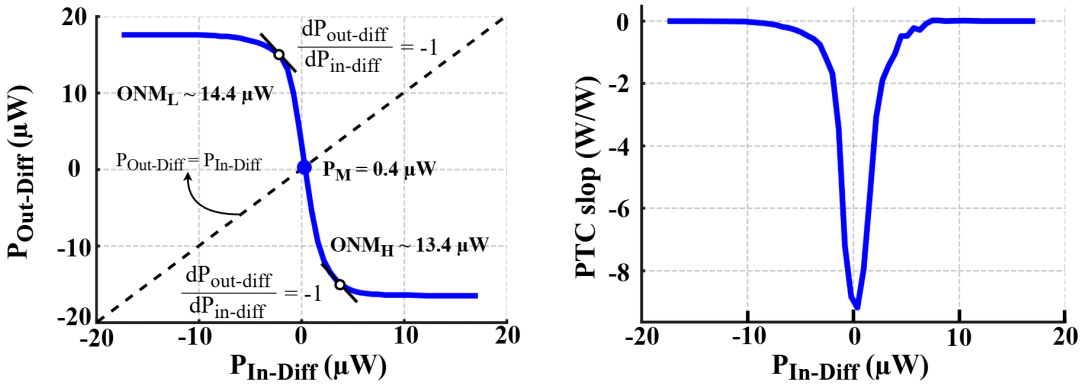

Figure 4.30: Simulated results for the IC-level optical NOT gate: (a) PTC and (b) corresponding slope.

4.3 Floor Planning

Fig. 4.31 presents the top-level block diagram of the chip floor plan, and Fig. 4.32 shows the full layout of the logic control circuit, including the seal ring and pad ring. The chip occupies a total area of 1.25 mm^2.

A total of 6 I/O pads are used to interface both the main signal paths and testing access points. To improve signal integrity and reduce crosstalk, each high-speed signal pad is positioned between a pair of GND pads. The design also includes four pads dedicated to the shift register, responsible for controlling the on-chip T-gates. For power delivery, four VDD pads and six GND pads are distributed across the layout. One additional pad is allocated for providing the bias current.

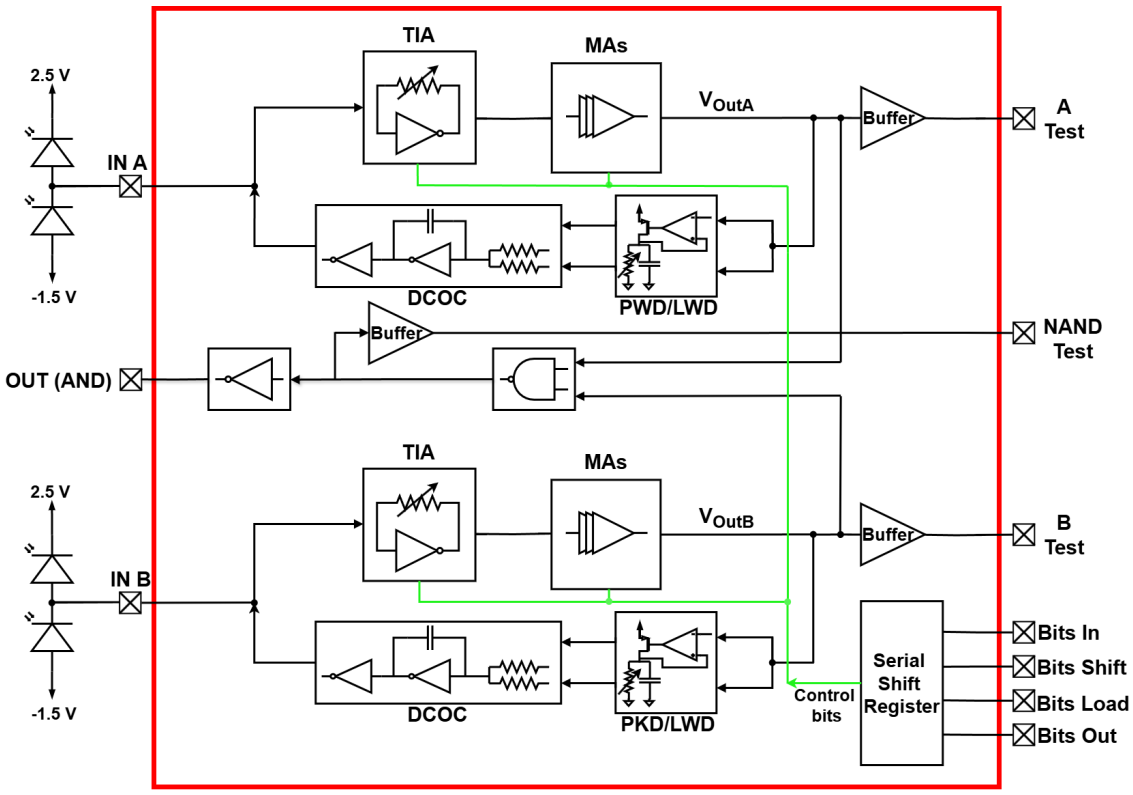

Figure 4.31: Top-level block diagram view of the floor plan.

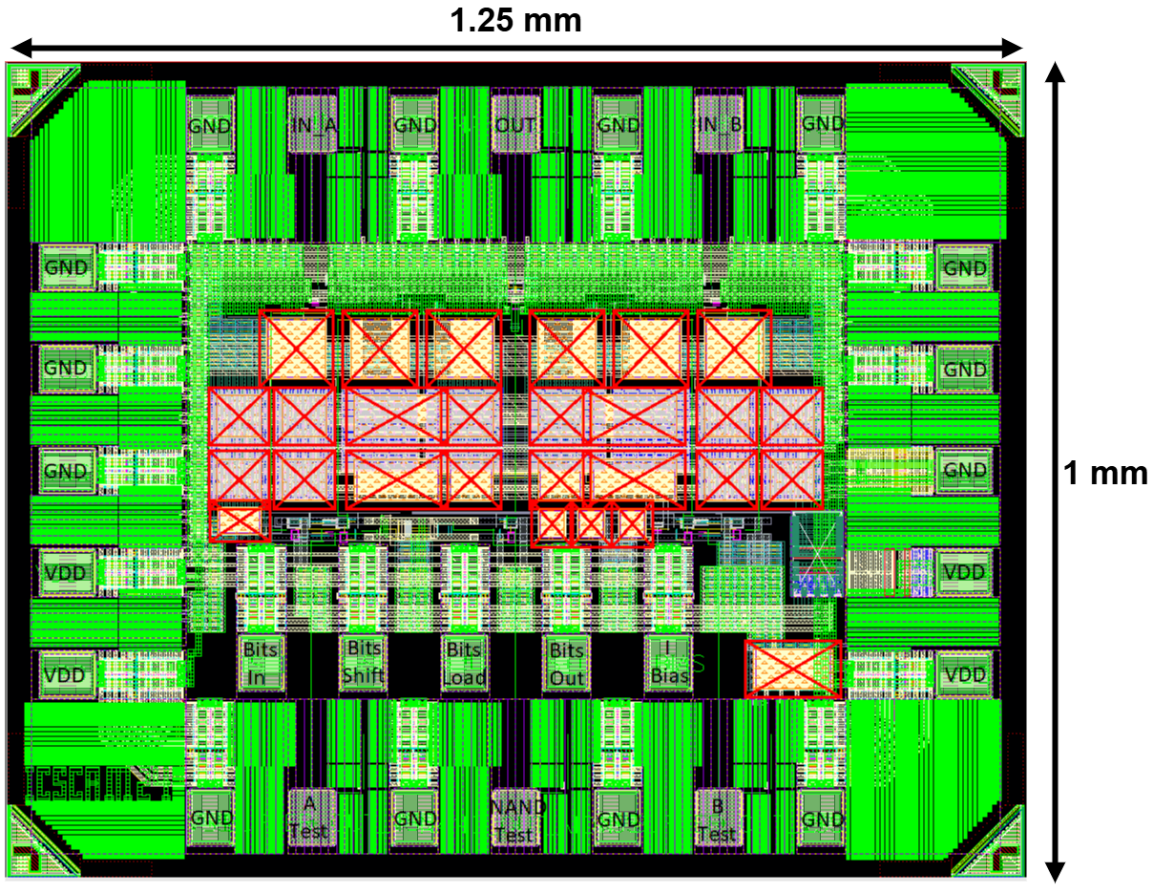

Figure 4.32: Layout of the complete logic control block, including pad ring and seal ring.

4.4 Measurement Setup and Fabricated Chip Integration

Fig. 4.33 displays the custom-designed high-speed PCB used for evaluating the electrical performance of the proposed logic control chip. The fabricated IC has been wire-bonded to the board and prepared for initial measurements. At the time of writing, characterization is still underway, and detailed results will be reported in a future publication.

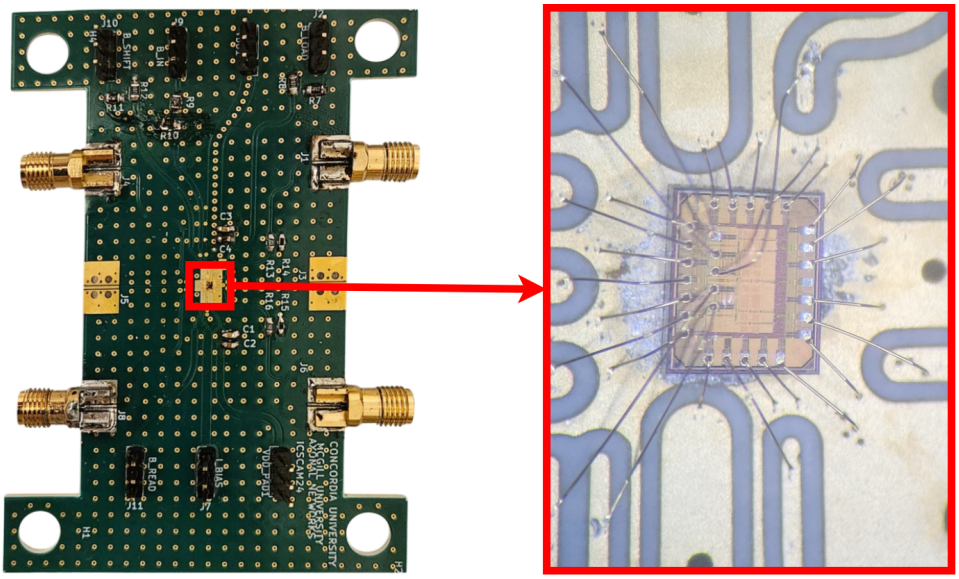

Figure 4.33: High-speed test PCB with the wire-bonded fabricated chip mounted for electrical measurements.

4.5 Conclusion

This chapter presented the design, layout, and post-layout validation of a fully integrated, logic-aware IC-level control circuit tailored for cascaded optical logic applications. A peak/low detector-based DCOC scheme was implemented in a continuous-feedback configuration, enabling dynamic signal centering and allowing the proposed receiver to overcome the limitations of conventional averaging-based compensation under unbalanced input data densities. The subtractive PD pair front-end, reconfigurable inverter-based TIA, three-stage Cherry–Hooper amplifiers, and logic-level detection circuitry were designed and optimized for robust performance across a wide range of signal conditions. Post-layout simulations verified the correct operation of the system under data densities ranging from 10% to 90%, extreme transitions, and showed a simulated propagation delay of approximately 107 ps. Despite this delay, the standalone gate was able to process narrow pulses, corresponding to a data throughput of up to 8 Gbps, confirming both signal integrity and logic functionality. These results establish the circuit's suitability for use in high-speed optical computing

platforms with unbalanced input data patterns. Finally, the floor plan and fabricated PCB demonstrate successful chip integration and readiness for experimental validation.

Chapter 5

Conclusions and Future Work

In this thesis, we experimentally verified the feasibility of cascadable OLGs and demonstrated a combinational 2×2 optical switch. As discussed in Chapter 3, the experimental setup had certain limitations that affected system performance, including the use of a logic control circuit not optimized for high-speed operation, the low bandwidth of the DAQs for generating input patterns and monitoring test points, and the reliance on long cables. This implementation was primarily intended to validate the concept of cascadable OLGs rather than to optimize delay, speed, or power dissipation. Nevertheless, the post-layout simulation results of the logic control circuit presented in Chapter 4 show that the same design approach introduced in Chapter 3 can be extended to achieve higher-speed OLGs.

Because optical signals can propagate over long distances with minimal attenuation, photonic logic gates do not require close spatial placement. This enables a more distributed system layout, which is difficult to achieve with conventional electrical interconnects that suffer from higher parasitic capacitance, signal degradation, and speed limitations. Furthermore, the use of optical interconnects inherently provides low crosstalk, allowing densely interconnected systems to maintain high signal integrity without the interference challenges typical in compact electronic layouts. Such distributed placement also reduces local power density, helping to mitigate thermal hotspots and reduce heat-induced performance degradation, issues that become increasingly critical in large-scale integrated systems.

5.1 Comparision

Table 5.1 summarizes a comparison between this work and other reported optical logic gate implementations. The MRM-based logic gates reported by [28] demonstrate OR, NOR, XOR, and XNOR functions and operate without electrical gain. While conceptually attractive, their practicality is limited by the need for precise input phase control and by the low bandwidth of zero-bias photodiodes, which restricts speed to the megahertz range. In principle, reverse-biasing the photodiodes could enable multi-gigabit operation, but this would require an I–V conversion stage, while also removing the nonlinear P-V characteristic of zero bias PDs that is essential for the logic behavior.

The MRM-based system reported in [21] implements universal optical logic gates through feedback-controlled PN-junction tuning and demonstrates NOR and NAND operations. The gates were implemented and tested on a programmable MZI mesh configured to emulate MRM behavior, while cascadability was only suggested by simulating an SR latch using two gates, with no physical hardware realization. Each gate requires three MRMs and precise phase alignment, and the limiting amplifiers used in the feedback loops were only emulated in software. As a result, while the concept supports scalability, a practical PIC implementation would entail significant area overhead, accurate phase alignment, complex biasing, and multiple control circuits.

The photonic crystal (PhC) logic gates presented in [8, 29] are compact and very fast; however, they are not CMOS-compatible, require high input power, and lack optical signal regeneration, which limits their suitability for larger-scale systems.

The MZI + QDSOA-based gates reported in [11] achieve fast NOR (and extended to XNOR) operation by exploiting QDSOA gain saturation. The results were validated only through simulation, but practical implementation would require multiple wavelengths, precise phase shifters, and two QDSOAs per gate (four for XNOR) with electrical biasing. As a result, the approach adds significant system complexity and power consumption.

In contrast, the proposed design is the only one in this comparison that experimentally verifies multi-stage cascading while maintaining signal regeneration. Moreover, this work combines MRM-based photonic logic with a CMOS electronic control circuit, enabling co-integration with

standard electronics. The measured PTC and ONM provide quantitative performance metrics that are rarely reported in previous works, offering deeper insight into cascaded OLG behavior. Combined with the high-speed potential demonstrated in the post-layout control circuit results, the proposed architecture is well-positioned for future high-speed and scalable optical computing systems.

Table 5.1: Comparison of optical logic gate implementations.

Reference	**Opt. Quant. Electron., 2020 [11]**	**Appl. Phys. B, 2021 [29]**	**Symmetry, 2023 [8]**	**Opt. Express, 2024 [28]**	**Opt. Express, 2025 [21]**	**This work**
Implementation Type	MZI + QD-SOA	PhC nonlinear ring resonator	PhC ring resonator	MRM-based	Hybrid MZI+MRM	MRM-based
Platform / Structure	InAs / GaAs QD-SOA with TPA	GaAs-based PhC ring resonator (Kerr)	2D PhC multi-ring (Si rods in SiO2)	Si MRM + zero-bias PD	Programmable MZI mesh + electronic control	Si MRM + electronic control
Logic Functions	NOR, XNOR	AND	Half-adder (AND, XOR)	OR, NOR, NOT, BUF	NOR, NAND, latch	NOT, NAND, 2×2 switch
Cascading	Potential	not cascadable	not cascadable	potential	Simulation (2-stage)	Experiment (multi-stage)
Optical Signal Regeneration	✓	✗	✗	✓	✓	✓
PTC / ONM Analysed	✗	✗	✗	PTC only	✗	✓

5.2 Future Work

This thesis has verified the viability of the proposed OLG architecture through both experimental evaluation and post-layout simulation. Nevertheless, there remain opportunities for further examination and improvement.

An important next step is the experimental validation of the fabricated integrated circuit through combined electrical and optical testing, in conjunction with a PIC configured to realize an optical D-latch using four cascaded OLGs. These measurements would help verify the efficiency of the logic control circuit under realistic high-speed optical operating conditions, offering valuable evidence of its scalability and dependability for deployment in practical systems.

A key area of future research is circuit optimization, aimed at improving logic uniformity, noise margins, and scalability. A schematic-level simulation of the NAND stage was performed with the current sizing of NMOS transistors at $W/L = 20 \times 2\,\mu\text{m}/60\,\text{nm}$ and PMOS transistors at $W/L = 5 \times 2\,\mu\text{m}/60\,\text{nm}$. An alternative sizing with stronger PMOS devices ($W/L = 8 \times 2\,\mu\text{m}/60\,\text{nm}$) confirmed that this adjustment reduces variation in the logical '1' output levels, although it does not eliminate it completely. The trade-off is a slightly elevated logical '0' level, but the benefit is more consistent and reliable '1' levels in cascaded operation. Beyond device resizing, architectural modifications of the NAND gate can also be considered. A symmetric NAND topology, implemented with two parallel NMOS branches and cross-connected inputs (A–B in one branch, B–A in the other), removes the asymmetry between the 01 and 10 cases, thereby eliminating the corresponding output mismatch observed in the conventional NAND design. In addition, access to the peak- and low-level information provided by the PKD and LWD circuits offers the possibility of implementing automatic-gain-control (AGC) versions of the TIA and MA stages. Such adaptive front-ends could dynamically adjust their gain to accommodate varying optical input levels, improving system resilience and maintaining consistent performance across diverse conditions.

Future research could also investigate fully optical OLG architectures in which the logic operation is performed directly within the PDs, sometimes assisted by an on-chip load resistor, through either reverse-bias voltage control or forward-current injection. In the planned continuation of this work, four such designs have been developed, two utilizing reverse-biased MRMs and two based

on forward-biased MRMs, with two of these architectures originally proposed by the author. Experimental validation focusing on key metrics such as speed and cascadability would help assess their feasibility for large-scale optical logic systems. A notable consideration is the interplay between MRM slope, electrical gain, and bandwidth. The modest slope in the output power versus modulation voltage characteristic (Fig. 2.7 (b)) places heavy demands on the electronics, since high electrical gain is often required to ensure reliable logic operation and unity gain for cascaded behavior, and as mentioned in chapter 2, this constraint limits the electrical bandwidth to the MHz range by the RC time constant. One way to improve this is by increasing the Q-factor of the MRMs, which steepens the slope of the mentioned curve. This reduces the required load resistance, thereby relaxing the electrical gain requirements and simultaneously increasing the electrical bandwidth of simple PD–resistor–MRM configurations. Although a higher Q reduces the optical bandwidth of the MRM, in this case, the optical bandwidth already far exceeds the electrical bandwidth, so the reduction does not limit performance. As a result, careful Q-factor optimization can improve the MRM slope, reduce the required electrical gain, and increase the overall system bandwidth, supporting more scalable and cascadable optical logic operation. Any future optical–electronic hybrid or fully optical design should take these amplification requirements into account when targeting signal regeneration and scalability.

Appendix A

KiCad Design of the Logic Control PCB

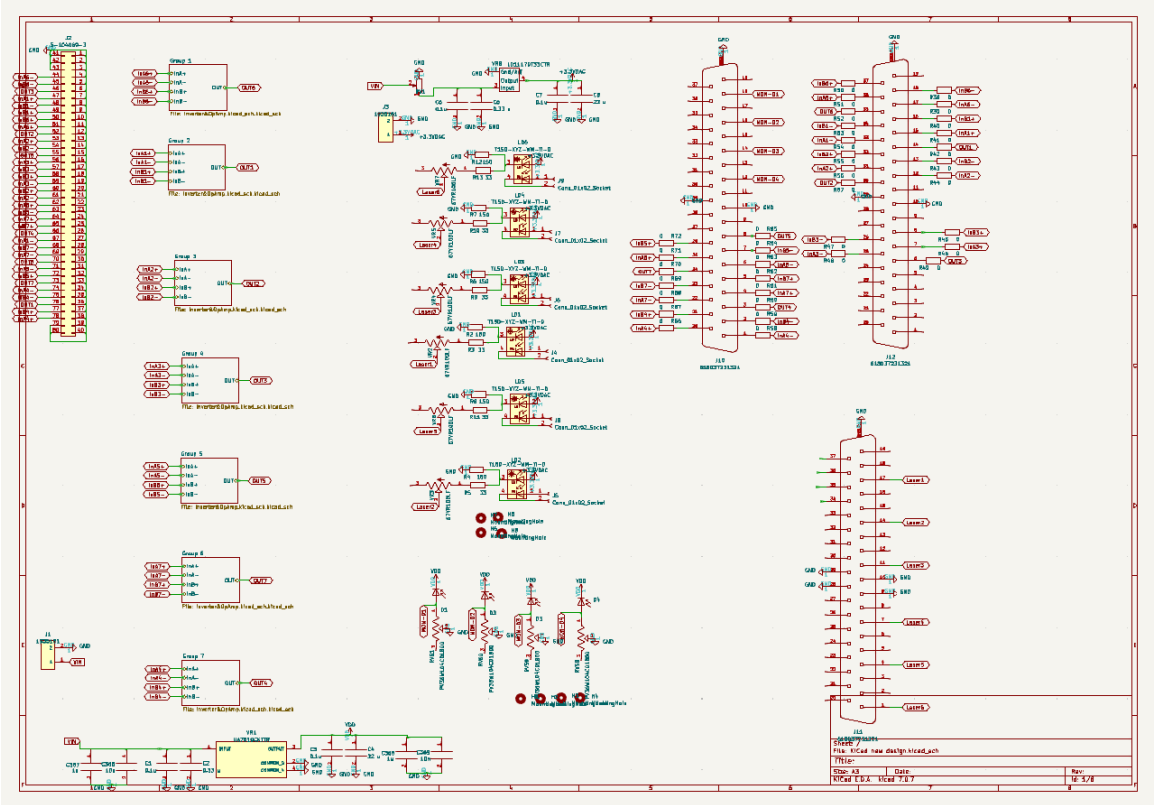

Figure A.1: High-level schematic of the logic control board used for the experiments in Chapter III

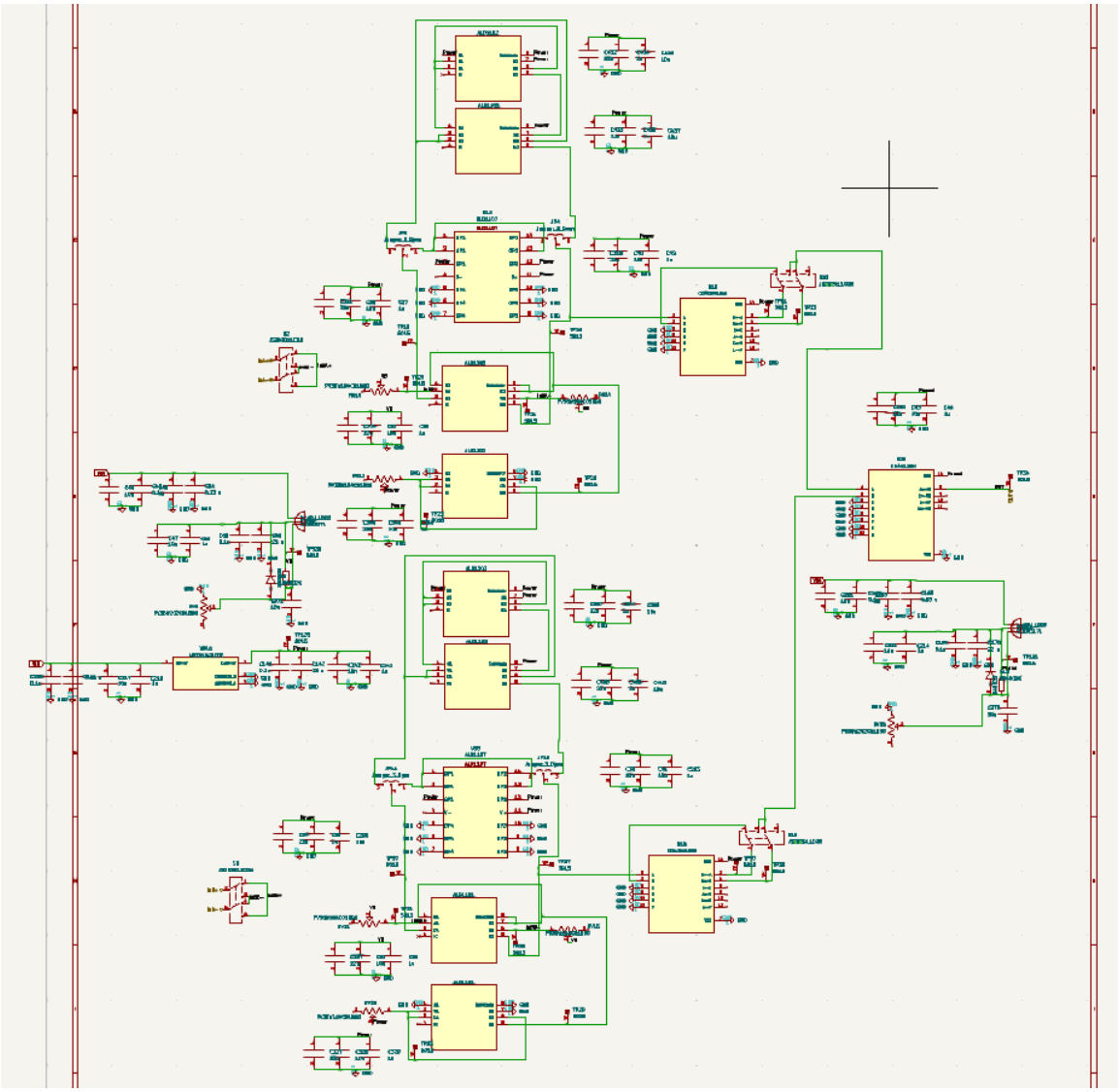

Figure A.2: Detailed schematic of a single logic control board implementing one AND gate.

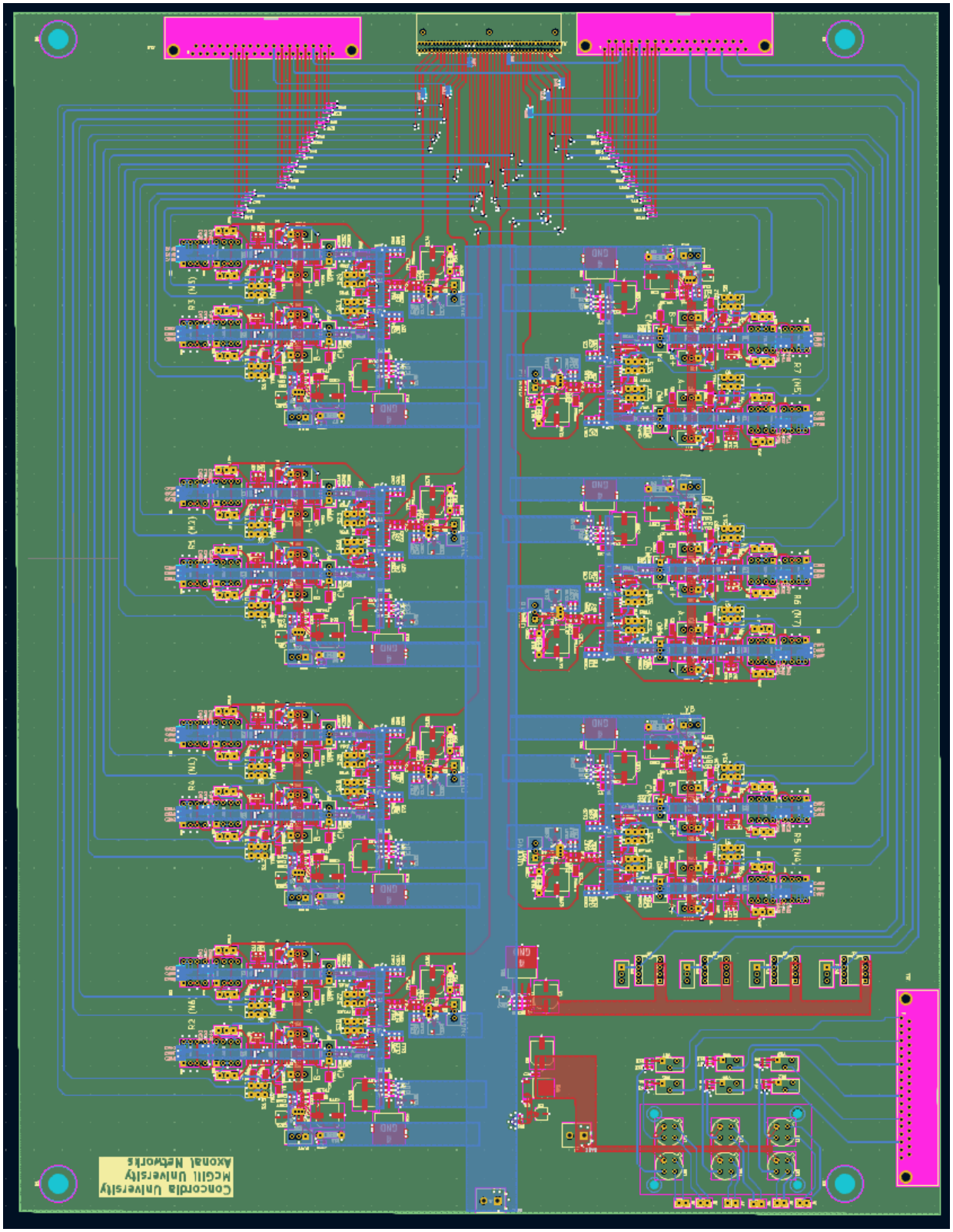

Figure A.3: PCB layout of the logic control board.

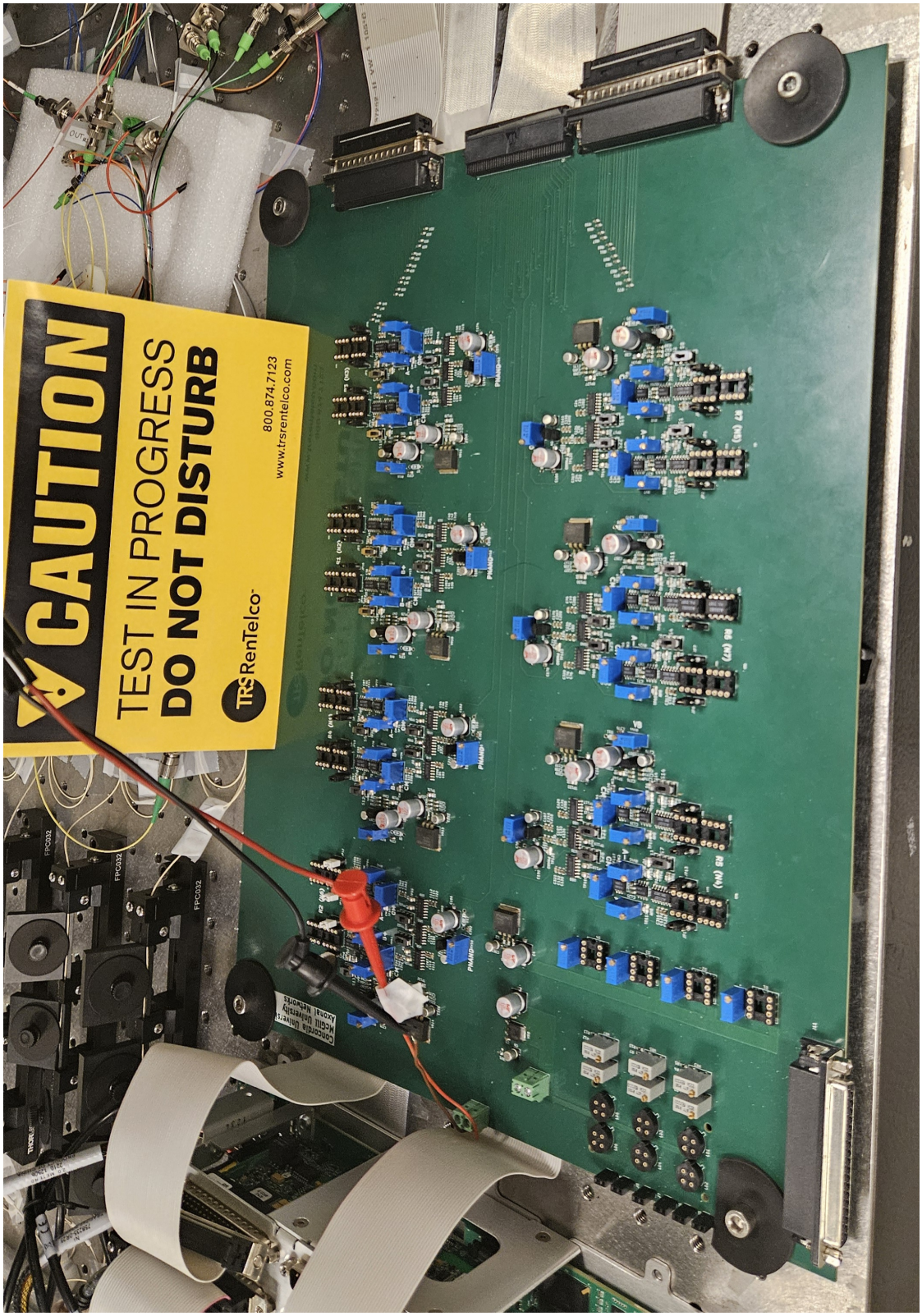

Figure A.4: Fabricated logic control PCB.

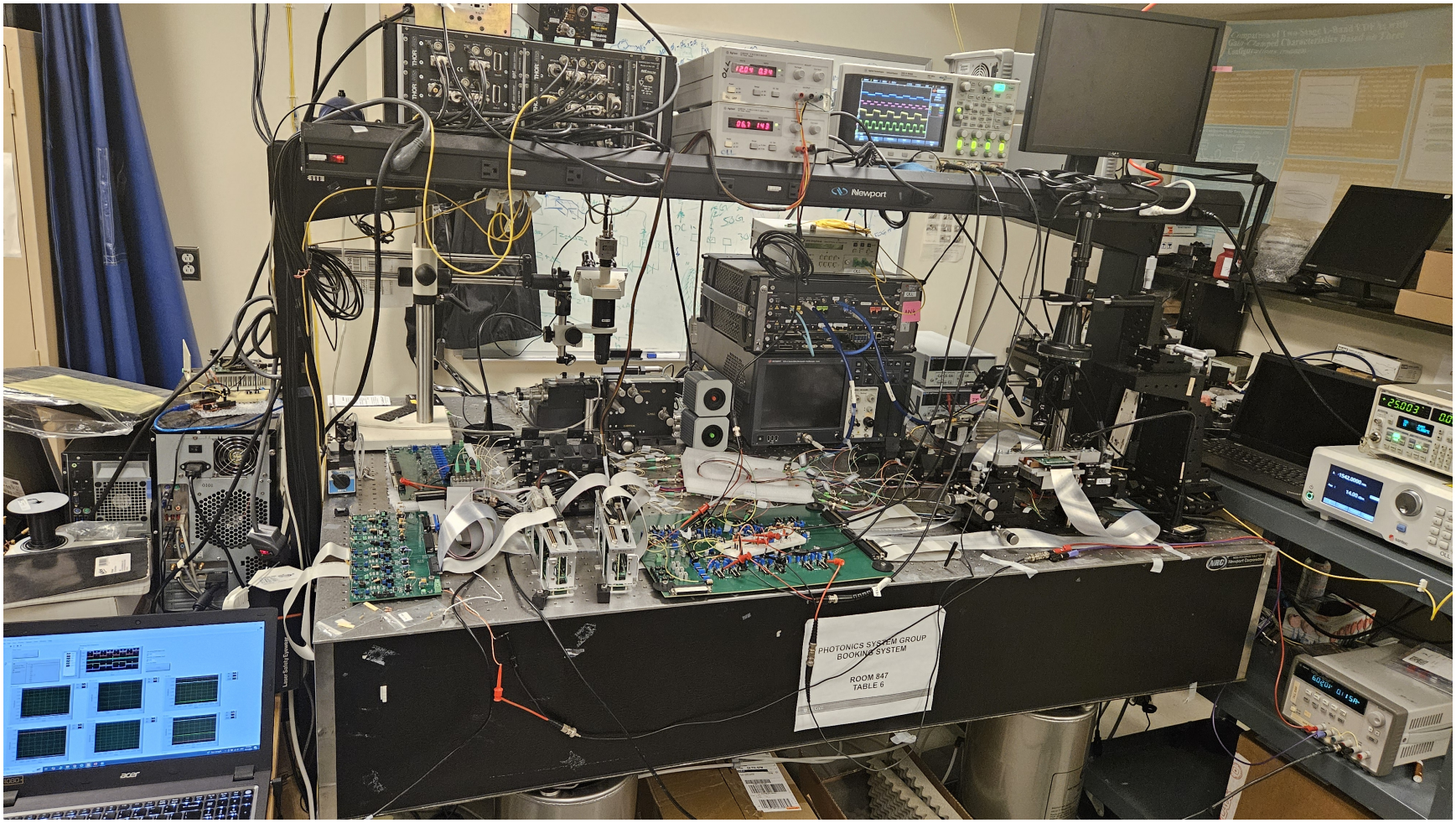

Figure A.5: Experimental setup of 2×2 optical switch

Appendix B

KiCad Design of the High-Speed PCB

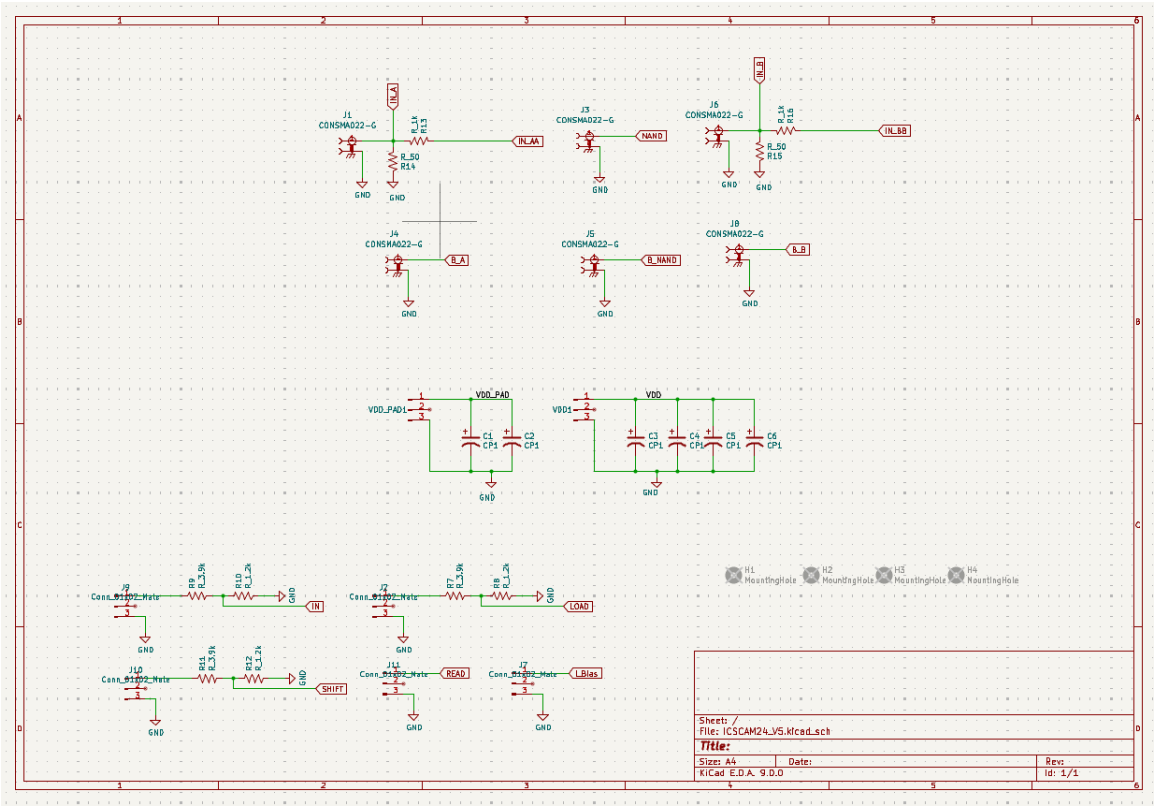

Figure B.1: High-speed PCB schematic.

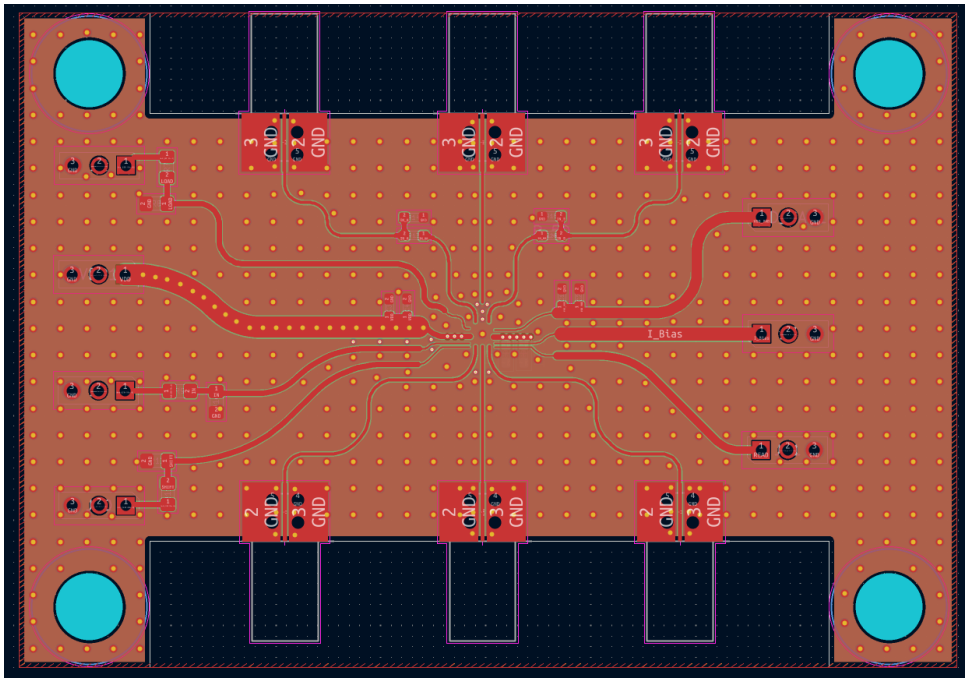

Figure B.2: High-speed PCB design.

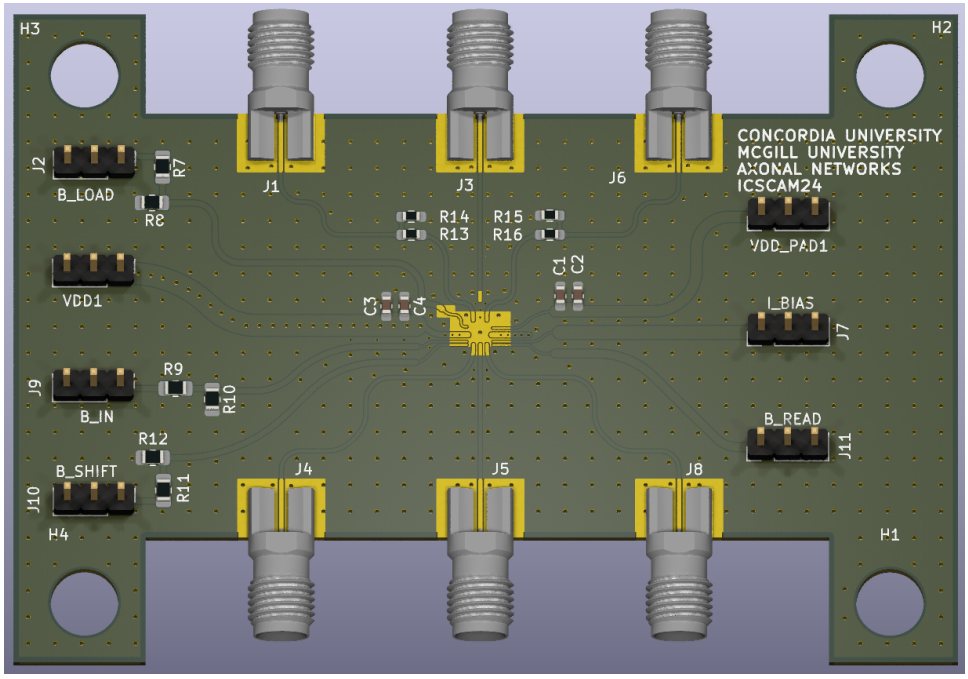

Figure B.3: 3D rendering of the high-speed PCB design.

Bibliography

[1] D. A. B. Miller, "Device requirements for optical interconnects to silicon chips," *Proceedings of the IEEE*, vol. 97, no. 7, pp. 1166–1185, 2009.

[2] J. D. Meindl, "Beyond moore's law: the interconnect era," *Computing in Science & Engineering*, vol. 5, no. 1, pp. 20–24, 2003.

[3] J. G. Echeverría *et al.*, "Self-calibrated microring weight function for neuromorphic optical computing," *Journal of Lightwave Technology*, vol. 43, no. 2, pp. 602–610, 2025.

[4] Z. Ying *et al.*, "Electronic-photonic arithmetic logic unit for high-speed computing," *Nature Communication*, vol. 11, p. 2154, 2020.

[5] S. M. Jiao *et al.*, "All-optical logic gate computing for high-speed parallel information processing," *Opto-Electronic Science*, vol. 1, p. 220010, 2022.

[6] W. Bogaerts *et al.*, "Programmable photonic circuits," *Nature*, vol. 586, pp. 207–216, 2020.

[7] S. Shekhar *et al.*, "Roadmapping the next generation of silicon photonics," *Nature Communications*, vol. 15, p. 751, 2024.

[8] Y. Pugachov *et al.*, "Design of all-optical logic half-adder based on photonic crystal multi-ring resonator," *Symmetry*, vol. 15, no. 5, p. 1063, 2023.

[9] T. K. Liang *et al.*, "High speed logic gate using two-photon absorption in silicon waveguides," *Optics Communications*, vol. 265, no. 1, pp. 171–174, 2006.

[10] J.-Y. Kim *et al.*, "10 gbit/s all-optical composite logic gates with xor, nor, or and nand functions using soa-mzi structures," *Electronics Letters*, vol. 42, no. 5, pp. 303–304, 2006.

[11] A. Kotb and C. Guo, "All-optical NOR and XNOR logic gates at 2 tb/s based on two-photon absorption in quantum-dot semiconductor optical amplifiers," *Optical and Quantum Electronics*, vol. 52, no. 30, 2020.

[12] Y. Pugachov *et al.*, "Design of all-optical d flip flop memory unit based on photonic crystal," *Nanomaterials*, vol. 14, no. 16, p. 1321, 2024.

[13] R. Soref, "The past, present, and future of silicon photonics," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 12, no. 6, pp. 1678–1687, 2006.

[14] Rakowski *et al.*, "45nm cmos - silicon photonics monolithic technology (45clo) for next-generation, low power and high speed optical interconnects," in *Optical Fiber Communication Conference (OFC) 2020, OSA Technical Digest*, 2020, p. T3H.3.

[15] Y. Yuan *et al.*, "A 5 × 200 gbps microring modulator silicon chip empowered by two-segment z-shape junctions," *Nature Communication*, vol. 15, p. 918, 2024.

[16] W.-C. Hsu *et al.*, "High-speed low-voltage moscap-driven silicon microring modulator," in *IEEE Silicon Photonics Conference (SiPhotonics)*, Tokyo Bay, Japan, 2024, pp. 1–2.

[17] F. Xu *et al.*, "A high-speed silicon ring modulator with a large working wavelength range," *Electronics*, vol. 13, no. 15, p. 2890, 2024.

[18] L. Lu *et al.*, "16 × 16 non-blocking silicon optical switch based on electro-optic mach-zehnder interferometers," *Optics Express*, vol. 24, no. 9, pp. 9295–9307, 2016.

[19] Q. Lu *et al.*, "High-speed ultra-compact all-optical not and and logic gates designed by a multi-objective particle swarm optimized method," *Optics & Laser Technology*, vol. 116, pp. 322–327, 2019.

[20] C. Feng *et al.*, "Analysis of microresonator-based logic gate for high-speed optical computing in integrated photonics," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 26, no. 2, pp. 1–8, 2020.

[21] F. Ashtiani, "Programmable photonic latch memory," *Optics Express*, vol. 33, pp. 3501–3510, 2025.

[22] W. Bogaerts *et al.*, "Silicon microring resonators," *Laser & Photonics Reviews*, vol. 6, no. 1, pp. 47–73, 2012.

[23] G. Reed *et al.*, "Silicon optical modulators," *Nature Photonics*, vol. 4, pp. 518–526, 2010.

[24] P. Dong, R. Shafiiha, S. Liao, H. Liang, N.-N. Feng, D. Feng, G. Li, X. Zheng, A. V. Krishnamoorthy, and M. Asghari, "Wavelength-tunable silicon microring modulator," *Optics Express*, vol. 18, pp. 10 941–10 946, 2010.

[25] D. Musat, "Novel thermal controller for active stabilization of microring modulators," M.A.Sc. thesis, Department of Electrical & Computer Engineering, Concordia University, Montreal, Canada, Mar. 2024.

[26] X. Guan *et al.*, "Ultra-dense wavelength-division multiplexing with microring modulator," *Journal of Lightwave Technology*, vol. 39, no. 13, 2021.

[27] J. F. Buckwalter *et al.*, "A monolithic 25-gb/s transceiver with photonic ring modulators and ge detectors in a 130-nm cmos soi process," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 6, pp. 1309–1322, 2012.

[28] S. Idres *et al.*, "Universal all-optical zero-bias logic gates in silicon photonics," *Optics Express*, vol. 32, pp. 36 063–36 074, 2024.

[29] E. Veisi *et al.*, "A novel design of all-optical high-speed and ultra-compact photonic crystal AND logic gate based on the kerr effect," *Applied Physics B*, vol. 127, no. 70, 2021.

[30] B. Razavi, *Design of Integrated Circuits for Optical Communications*, 2nd ed. Hoboken, NJ, USA: John Wiley & Sons, 2012.

[31] G. Cowan, *Mixed-Signal CMOS for Wireline Communication: Transistor-Level and System-Level Design Considerations*. Cambridge University Press, 2024.

[32] E. Säckinger, "The transimpedance limit," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 8, pp. 1848–1856, 2010.

[33] J. Proesel *et al.*, "Optical receivers using dfe-iir equalization," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, vol. 2013, pp. 130–131, 2013.

[34] B. Razavi, *Fundamentals of Microelectronics*, 1st ed. Hoboken, NJ, USA: Wiley, 2008.

[35] G. Priem *et al.*, "Optical bistability and pulsating behaviour in silicon-on-insulator ring resonator structures," *Optics Express*, vol. 13, no. 23, pp. 9623–9628, 2005.

[36] C. Sun *et al.*, "A 45 nm cmos-soi monolithic photonics platform with bit-statistics-based resonant microring thermal tuning," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 4, pp. 893–907, 2016.

[37] J. F. Wakerly, *Digital Design: Principles and Practices*, 3rd ed. Prentice Hall, 1999.

[38] M. S. Hrishikesh *et al.*, "The optimal logic depth per pipeline stage is 6 to 8 fo4 inverter delays," *ACM SIGARCH Computer Architecture News*, vol. 30, no. 2, pp. 14–24, 2002.

[39] M. Nakamura *et al.*, "An instantaneous response cmos optical receiver ic with wide dynamic range and extremely high sensitivity using feed-forward auto-bias adjustment," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 9, pp. 991–997, Sept. 1995.

[40] W.-Z. Chen *et al.*, "A single-chip 2.5-gb/s cmos burst-mode optical receiver," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 10, pp. 2325–2331, 2009.